ISO1176T Isolated Profibus RS-485 Transceiver with Integrated Transformer Driver

1 Features

- Meets or Exceeds the Requirements of EN 50170 and TIA/EIA-485-A
- Signaling Rates up to 40 Mbps
- Easy Isolated Power Design with Integrated Transformer Driver
- Typical Efficiency > 60% (I_{LOAD} = 100 mA) - see SLUU471
- Differential Output exceeds 2.1 V (54-Ω Load)
- Low Bus Capacitance 10 pF (Maximum)
- Fail-safe Receiver for Bus Open, Short, or Idle
- 50-kV/µs Typical Transient Immunity
- Safety and Regulatory Approvals
  - 4242 V_{PK} Basic Insulation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 Standards

2 Applications

- Profibus®
- Factory Automation
- Networked Sensors
- Motor/motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

3 Description

The ISO1176T is an isolated differential line transceiver with integrated oscillator outputs that provide the primary voltage for an isolation transformer. The device is ideal for long transmission lines because the ground loop is broken to allow the device to operate with a much larger common-mode voltage range.

The symmetrical isolation barrier of each device is tested to provide 4242V_{PK} of isolation per VDE for 60 seconds between the line transceiver and the logic-level interface.

The galvanically isolated differential bus transceiver is an integrated circuit designed for bi-directional data communication on multipoint bus-transmission lines. The transceiver combines a galvanically isolated differential line driver and differential input line receiver. The driver has an active-high enable with isolated enable-state output on the ISODE pin (pin 10) to facilitate direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC2} = 0.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. The ISO1176T can significantly reduce the risk of data corruption and damage to expensive control circuits.

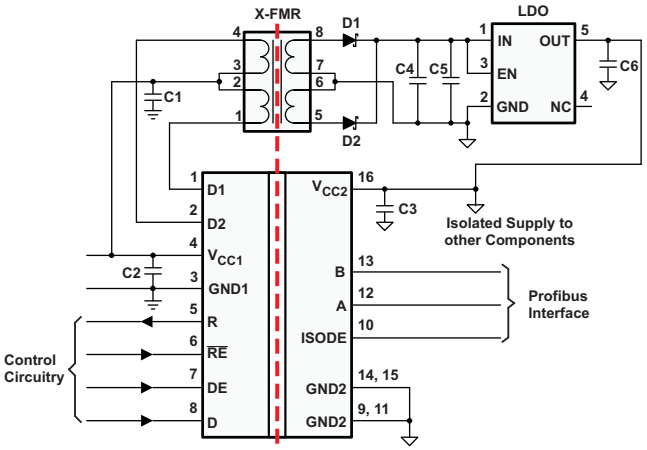
The device is characterized for operation over the ambient temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1176T	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2012) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ... 1
- Added Maximum Device Power Dissipation to Power Rating Table. ... 5

Changes from Revision E (August 2011) to Revision F — **Page**

- Changed From "ISO1176T Reference Design SLLU471" To: "ISO1176T Reference Design SLUU471" ... 28

Changes from Revision D (May 2011) to Revision E — **Page**

- Deleted the MIN and MAX values for t_{r_D}, t_{f_D} and t_{BBM} specifications in the Transformer Driver Characteristics table. ... 8
- Changed test conditions from 1.9 V to 2.4 V, and changed TYP value from 230 to 350 for f_{St} specification in the Transformer Driver Characteristics table. ... 8

Changes from Revision C (February 2011) to Revision D — **Page**

- Added Figure 33 ... 1
- Moved the Pin Description closer to the Pin drawing ... 4

Changes from Revision B (December 2010) to Revision C **Page**

- Deleted R_{OFF} from the TRANSFORMER DRIVER CHARACTERISTICS table ... 8
- Added a Typ value of 23ns to Prop delay time for V_{CC1} = 5V in the RS-485 DRIVER SWITCHING CHARACTERISTIC table ... 9
- Added a Typ value of 25ns to Prop delay time for V_{CC1} = 3.3V in the RS-485 DRIVER SWITCHING CHARACTERISTIC table ... 9
- Changed θ_{JA} = 212°C/W To: θ_{JA} = 76°C/W, Changed the I_S Max value From: 128mA To: 347mA, and changed paragraph two in the IEC SAFETY LIMITING VALUES section ... 19
- Changed Figure 29 ... 19

Changes from Revision A (December 2010) to Revision B **Page**

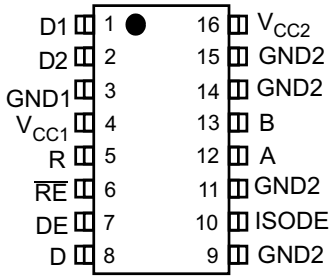
- Changed the Steady-state short-circuit output current - Test Conditions and values. ... 6
- Changed the Oscillator frequency values ... 8
- Changed the D1, D2 output rise time values ... 8

Changes from Revision initial (October 2010) to Revision A **Page**

- Updated transformer driver characteristics ... 8
- Added Thermal Table data ... 19

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	12	I/O	Non-inverting Driver Output / Receiver Input
B	13	I/O	Inverting Driver Output / Receiver Input
D	8	I	Driver Input
D1	1	O	Transformer Driver Terminal 1, Open Drain Output
D2	2	O	Transformer Driver Terminal 2, Open Drain Output
DE	7	I	Driver Enable Input
GND1	3	—	Logic-side Ground
GND2	9, 11, 14, 15	—	Bus-side Ground. All pins are internally connected.
ISODE	10	O	Bus-side Driver Enable Output Status
R	5	O	Receiver Output
$\overline{RE}$	6	I	Receiver Enable Input. This pin has complementary logic.
V_{CC1}	4	—	Logic-side Power Supply
V_{CC2}	16	—	Bus-side Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Input supply voltage(2)	–0.5	7	V
V_O	Voltage at any bus I/O terminal	–9	14	V
	Voltage at D1, D2		14	V
V_I	Voltage input at D, DE or $\overline{RE}$ terminal	–0.5	7	V
I_O	Receiver output current	–10	10	mA
I_{D1}, I_{D2}	Transformer Driver Output Current		450	mA
T_J	Maximum junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Bus pins to GND1	±6000	V
		Bus pins to GND2	±10000	
		All pins	±4000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		±1500	
	Machine model (MM), ANSI/ESDS5.2-1996		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Logic side supply voltage, V_{CC1} (with respect to GND1)		3		5.5	V
	Bus side supply voltage, V_{CC2} (with respect to GND2)		4.75		5.25	
V_{CM}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	$\overline{RE}$	2		V_{CC1}	V
		D, DE	0.7 V_{CC1}			
V_{IL}	Low-level input voltage	$\overline{RE}$	0		0.8	V
		D, DE			0.3 V_{CC1}	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
I_O	Output Current	RS-485 driver	–70		70	mA
		Receiver	–8		8	
T_A	Ambient temperature		-40		85	°C
T_J	Operating junction temperature				150	°C
1 / t_{UI}	Signaling Rate				40	Mbps

6.4 Thermal Information

THERMAL METRIC[1]		ISO1176T DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Power Rating

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum device power dissipation	V_{CC1} = 5.5 V, V_{CC2} = 5.25 V, T_J = 150°C, C_L = 50 pf, R_L = 54 Ω Input a 20 MHz 50% duty cycle square wave	719	mW

6.6 Electrical Characteristics: ISODE-Pin

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –8mA	V_{CC2} – 0.8	4.6		V
		I_{OH} = –20µA	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 8mA		0.2	0.4	V
		I_{OL} = 20µA		0	0.1	

6.7 Electrical Characteristics: RS-485 Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OD}	Open-circuit differential output voltage	$\|V_A - V_B\|$, See Figure 9		1.5		V_{CC2}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	See Figure 10 and Figure 14		2.1			V
		See Figure 11, Common-mode loading with Vtest from –7 V to +12 V		2.1			
$\|\Delta V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	See Figure 12 and Figure 13, R_L = 54 Ω		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 12 and Figure 13, R_L = 54 Ω		2		3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See Figure 12 and Figure 13, R_L = 54 Ω		–0.2		0.2	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 12 and Figure 13, R_L = 54 Ω			0.5		
$V_{OD(ring)}$	Differential output voltage over and under shoot	See Figure 14 and Figure 17				10%	$V_{OD(pp)}$
I_I	Input current	D, DE at 0 V or V_{CC1}		–10		10	µA
$I_{O(OFF)}$	Power-off output current	V_{CC2} = 0 V		See receiver input current			
I_{OZ}	High-impedance output current	DE at 0 V		See receiver input current			
$I_{OS(P)}$	Peak short-circuit output current	See Figure 16, DE at V_{CC1}	V_{OS} = –7 V to 12 V	–250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current		V_{OS} = 12 V, D at GND1			135	mA
			V_{OS} = –7 V, D at V_{CC1}	–135			
C_{OD}	Differential output capacitance			See receiver C_{IN}			
CMTI	Common-mode transient immunity	See Figure 27		25			kV/µs

6.8 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage	See Figure 23		I_O = –8mA		–80	–10	mV
$V_{IT(–)}$	Negative-going input threshold voltage			I_O = 8mA	–200	–120		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					25		mV
V_{OH}	High-level output voltage	V_{CC1} = 3.3 V ± 10% and V_{CC2} = 5 V ± 5%	V_{ID} = 200 mV, See Figure 23	I_{OH} = –8 mA	V_{CC1} – 0.4	3		V
				I_{OH} = –20 µA	V_{CC1} – 0.1	3.3		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 23	I_{OL} = 8 mA		0.2	0.4	V
				I_{OL} = 20 µA		0	0.1	
V_{OH}	High-level output voltage	V_{CC1} = 5 V ± 10% and V_{CC2} = 5 V ± 5%	V_{ID} = 200 mV, See Figure 23	I_{OH} = –8 mA	V_{CC1} – 0.8	4.6		V
				I_{OH} = –20 µA	V_{CC1} – 0.1	5		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 23	I_{OL} = 8 mA		0.2	0.4	V
				I_{OL} = 20 µA		0	0.1	
I_A, I_B	Bus pin input current	V_I = –7 or 12 V, Other input = 0 V		V_{CC2} = 4.75 V or 5.25 V	–160		200	µA
$I_{A(off)}$, $I_{B(off)}$				V_{CC2} = 0 V				
I_I	Receiver enable input current	$\overline{RE}$ = 0 V			–50		50	µA
I_{OZ}	High-impedance state output current	$\overline{RE}$ = V_{CC1}			–1		1	µA
R_{ID}	Differential input resistance	A, B			60			kΩ
C_{ID}	Differential input capacitance	Test input signal is a 1-MHz sine wave with 1-Vpp amplitude. CD is measured across A and B.				7	10	pF
CMR	Common mode rejection	See Figure 26				4		V

6.9 Supply Current

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1} (1)	Logic-side quiescent supply current	V_{CC1} = 3.3 V ± 10%, DE, $\overline{RE}$ = 0V or V_{CC1}, No load		4.5	8	mA
		V_{CC1} = 5 V ± 10%, DE, $\overline{RE}$ = 0V or V_{CC1}, No load		7	11	mA
I_{CC2} (1)	Bus-side quiescent supply current	V_{CC2} = 5 V ± 5%, DE, $\overline{RE}$ = 0V or V_{CC1}, No load		13.5	18	mA

(1) I_{CC1} and I_{CC2} are measured when device is connected to external power supplies. D1 and D2 are disconnected from external transformer.

6.10 Transformer Driver Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	V_{CC1} = 5 V ± 10%, D1 and D2 connected to Transformer	350	450	610	kHz
		V_{CC1} = 3.3 V ± 10%, D1 and D2 connected to Transformer	300	400	550	
R_{ON}	Switch on resistance	D1 and D2 connected to 50Ω pullup resistors		1	2.5	Ω
t_{r_D}	D1, D2 output rise time	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
		V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		70		
t_{f_D}	D1, D2 output fall time	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		55		ns
		V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		
f_{St}	Startup frequency	V_{CC1} = 2.4 V, D1 and D2 connected to Transformer		350		kHz
t_{BBM}	Break before make time delay	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		38		ns
		V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		140		

6.11 Switching Characteristics: RS-485 Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Prop delay time	See Figure 17 V_{CC1} = 5V ± 10%, V_{CC2} = 5V ± 5%		23	35	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			2	5	ns
t_{PLH}, t_{PHL}	Prop delay time	See Figure 17 V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 5%		25	40	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			2	5	ns
t_r	Differential output signal rise time	See Figure 17	2	3	7.5	ns
t_f	Differential output signal fall time	See Figure 17	2	3	7.5	ns
t_{pDE}	DE to ISODE prop delay	See Figure 21			30	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew	See Figure 18			1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$, $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay, high-impedance-to-active output	See Figure 19 and Figure 20, C_L = 50pf, $\overline{RE}$ at 0 V			80	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$, $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay, active-to-high-impedance output				80	ns
$\|t_{p(AZL)} - t_{p(BZH)}\|$ $\|t_{p(AZH)} - t_{p(BZL)}\|$	Enable skew time			0.55	1.5	ns
$t_{(CFB)}$	Time from application of short-circuit to current fold back	See Figure 16		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	See Figure 16, T_A = 25°C	100			µs

6.12 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 23 V_{CC1} = 5 V ± 10%, V_{CC2} = 5 V ± 5%		50	65	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			2	5	ns
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 23 V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 5%		53	70	ns
$t_{sk(p)}$	Pulse skew (|tpHL - tpLH|)			2	5	ns
t_r	Output signal rise time			2	4	ns
t_f	Output signal fall time			2	4	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output	DE at V_{CC1}, See Figure 24		13	25	ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output			13	25	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output	DE at V_{CC1}, See Figure 25		13	25	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			13	25	ns

6.13 Typical Characteristics

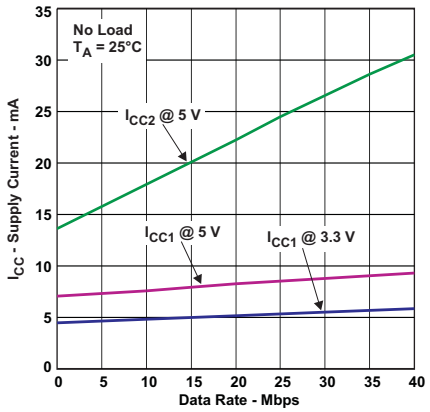


Figure 1. RMS Supply Current (I_{CC1} and I_{CC2}) vs Signaling Rate With No Load

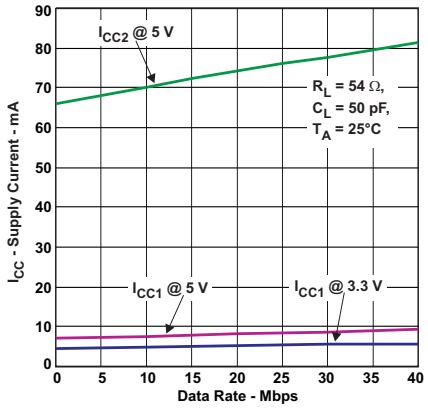


Figure 2. RMS Supply Current (I_{CC1} and I_{CC2}) vs Signaling Rate With Load

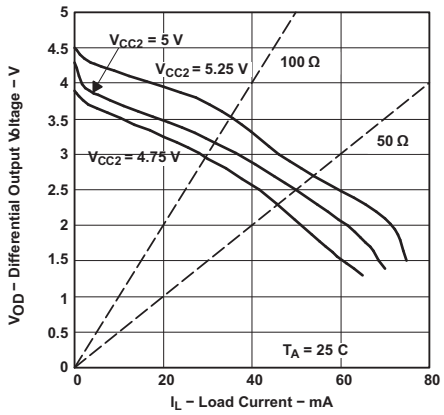


Figure 3. Differential Output Voltage vs Load Current

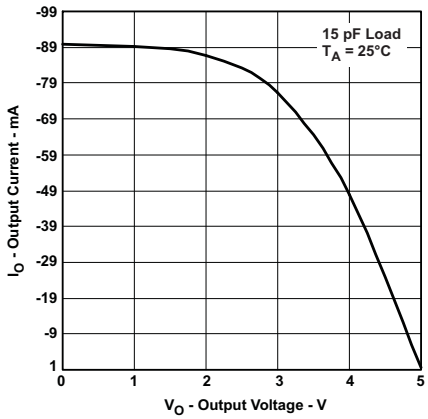


Figure 4. Receiver High-Level Output Voltage Vs High-Level Output Current

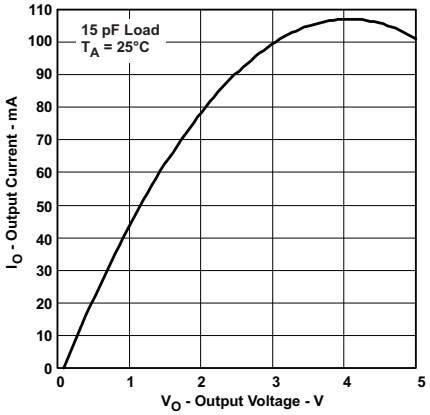


Figure 5. Receiver Low-Level Output Voltage vs Low-Level Output Current

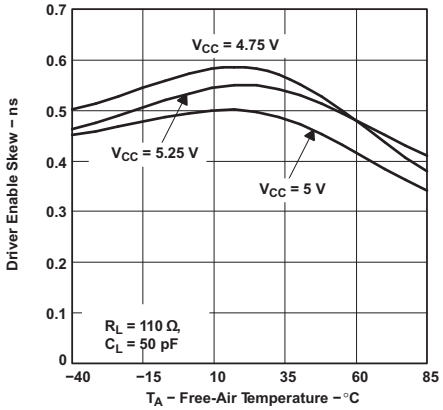


Figure 6. Driver Enable Skew vs Free-Air Temperature

Typical Characteristics (continued)

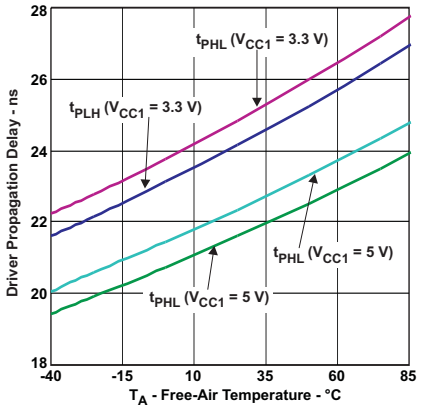


Figure 7. Driver Propagation Delay vs Free-Air Temperature

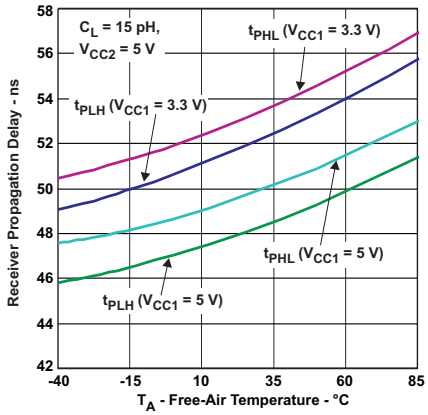


Figure 8. Receiver Propagation Delay vs Free-Air Temperature

7 Parameter Measurement Information

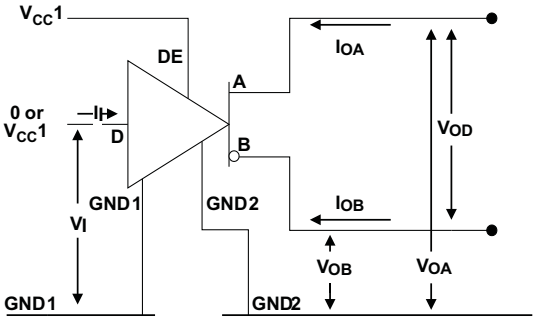


Figure 9. Open Circuit Voltage Test Circuit

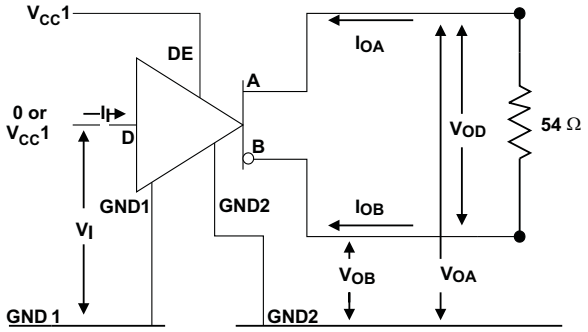


Figure 10. V_{OD} Test Circuit

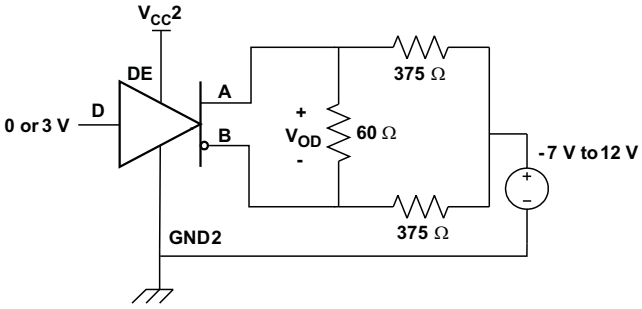


Figure 11. Driver V_{OD} with Common-mode Loading Test Circuit

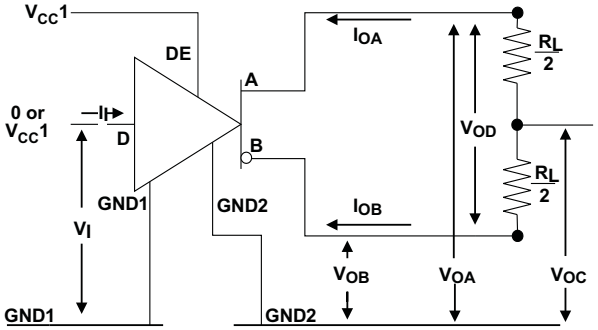


Figure 12. Driver V_{OD} and V_{OC} Without Common-Mode Loading Test Circuit

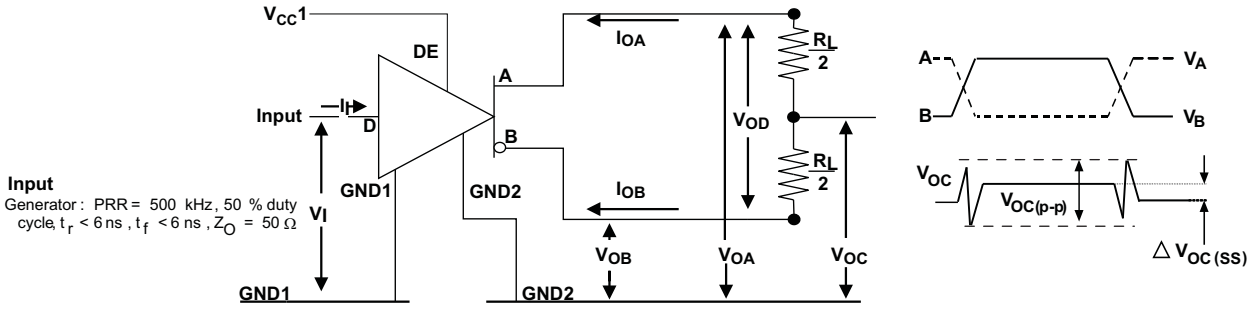


Figure 13. Steady-State Output Voltage Test Circuit and Voltage Waveforms

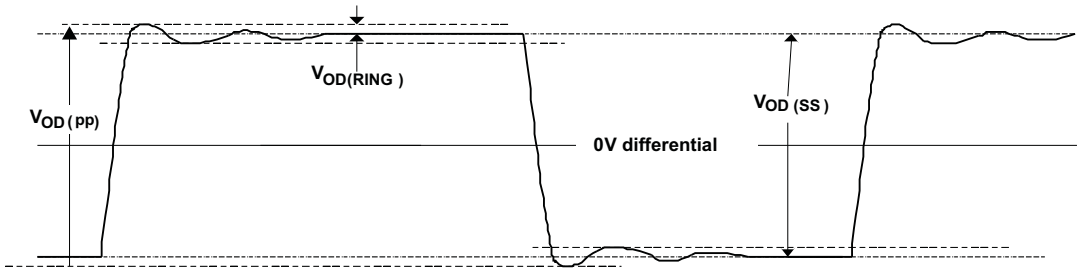


Figure 14. $V_{OD(RING)}$ Waveform and Definitions

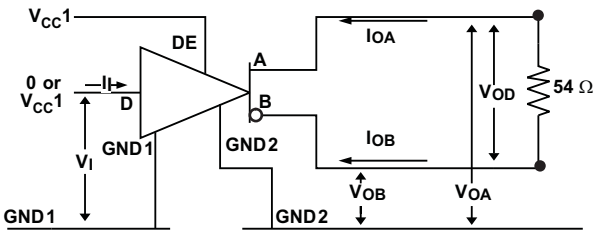


Figure 15. Input Voltage Hysteresis Test Circuit

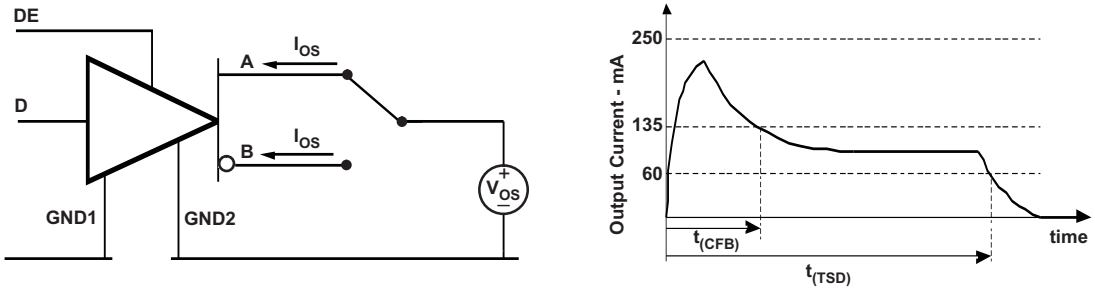


Figure 16. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0)

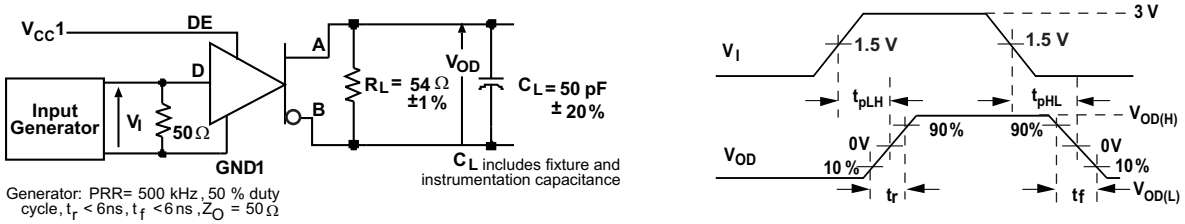


Figure 17. Driver Switching Test Circuit and Waveforms

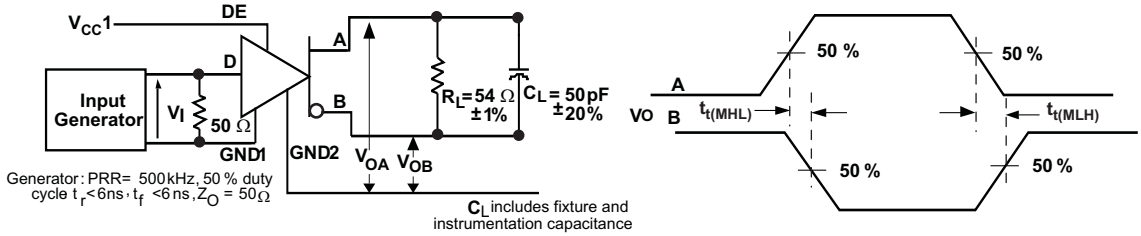


Figure 18. Driver Output Transition Skew Test Circuit and Waveforms

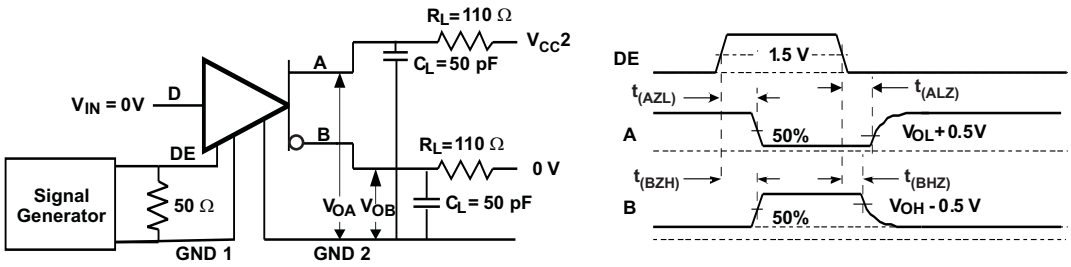


Figure 19. Driver Enable/Disable Test, D at Logic Low Test Circuit and Waveforms

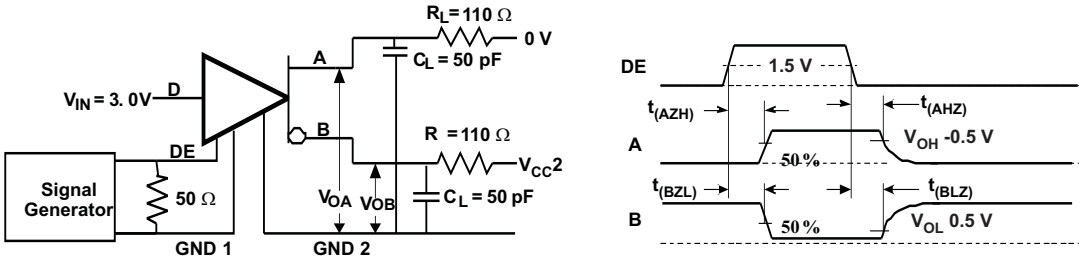


Figure 20. Driver Enable/Disable Test, D at Logic High Test Circuit and Waveforms

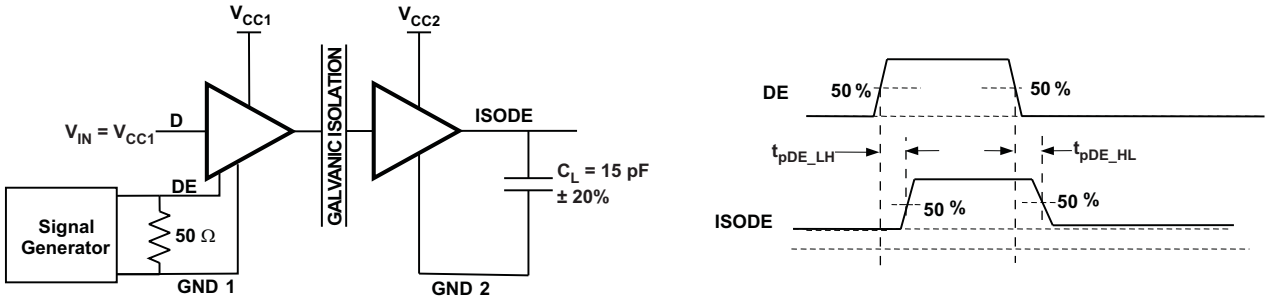


Figure 21. DE to ISODE Prop Delay Test Circuit and Waveforms

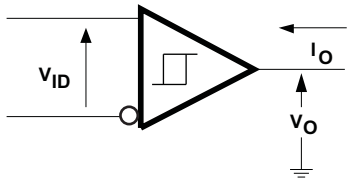


Figure 22. Receiver DC Parameter Definitions

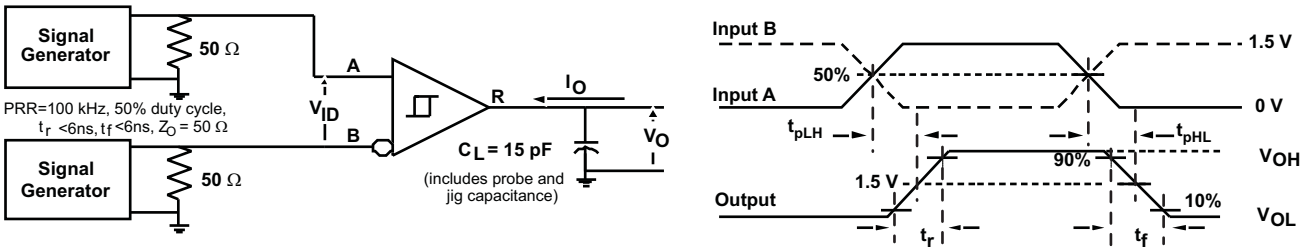


Figure 23. Receiver Switching Test Circuit and Waveforms

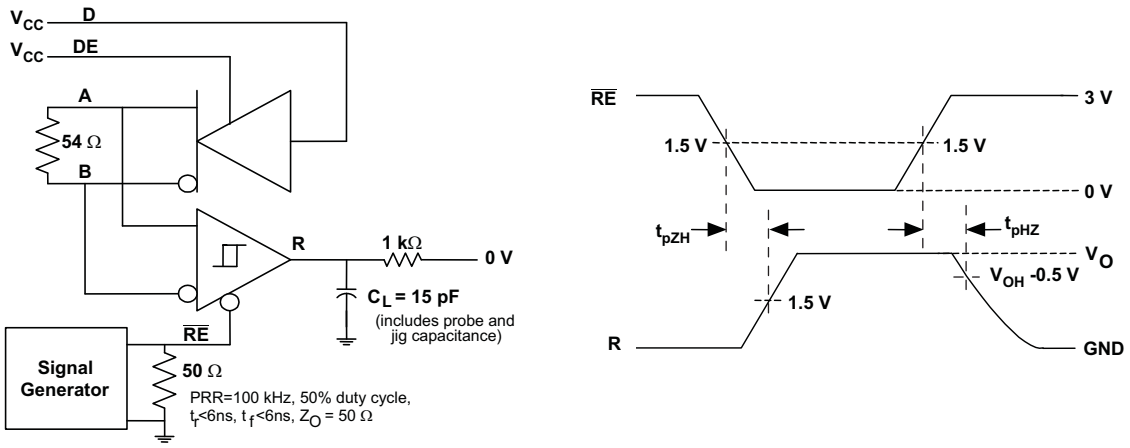


Figure 24. Receiver Enable Test Circuit and Waveforms, Data Output High

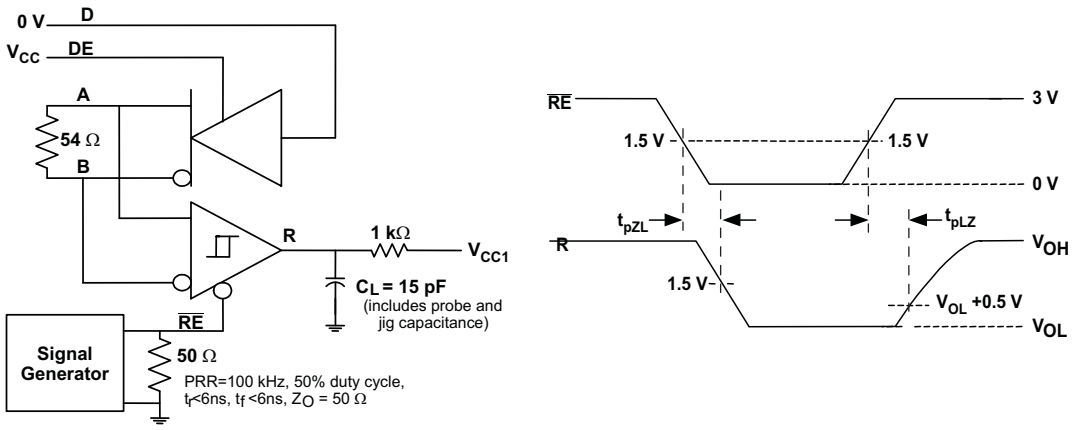


Figure 25. Receiver Enable Test Circuit and Waveforms, Data Output Low

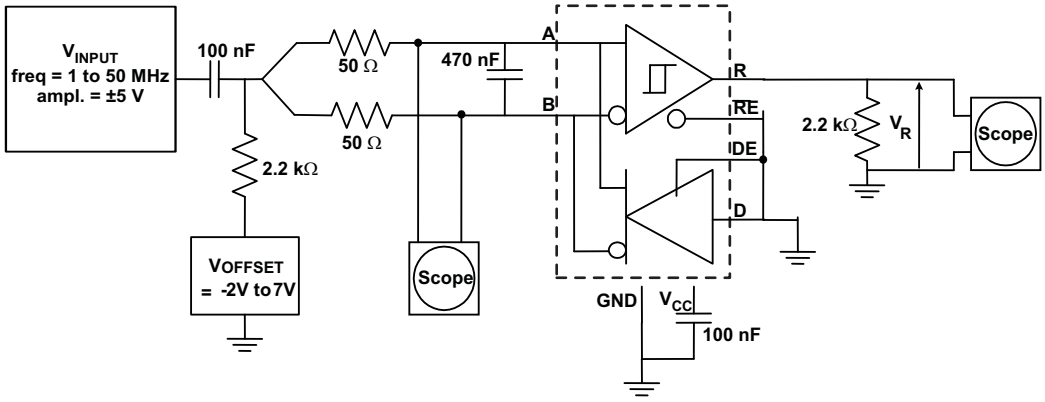


Figure 26. Common-Mode Rejection Test Circuit

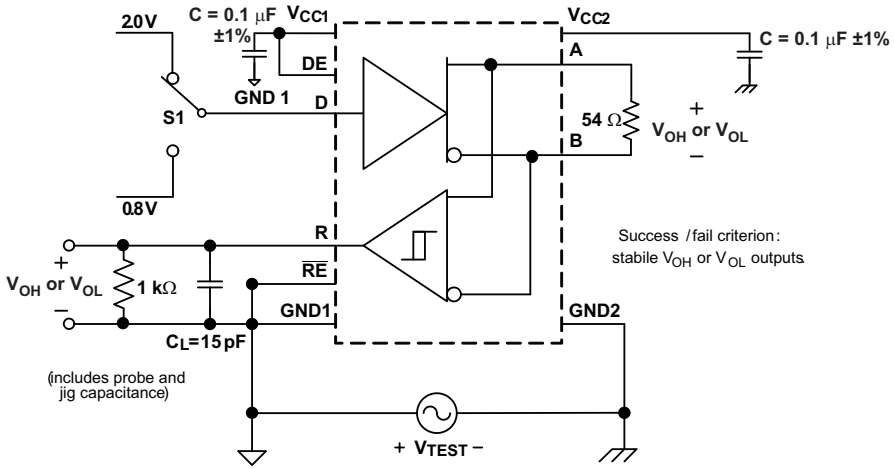


Figure 27. Common-Mode Transient Immunity Test Circuit

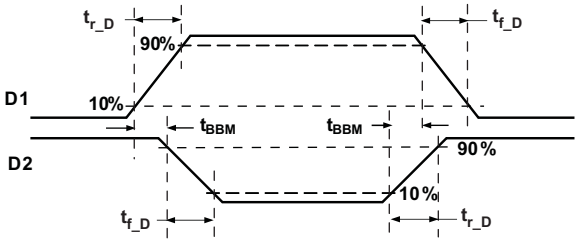


Figure 28. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

8 Detailed Description

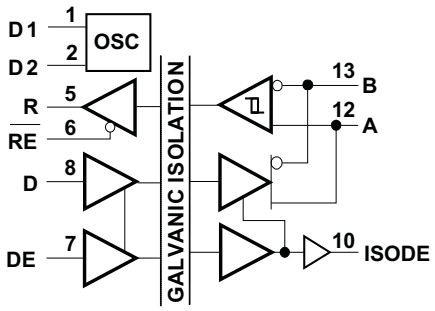
8.1 Overview

The ISO1176T is an isolated half-duplex differential line transceiver that meets the requirements of EN 50170 and TIA/EIA 485/422 applications. It has integrated transformer driver for convenient secondary power supply design. The device is rated to provide galvanic isolation of up to 4242 V_{PK} per VDE and 2500 V_{RMS} per UL 1577. The device has active-high driver enable and active-low receiver enable functions to control the data flow. It has maximum data transmission speed of 40 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_{(A)} – V_{(B)}$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Insulation and Safety-Related Specifications for 16-DW Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)(1)	Shortest terminal to terminal distance through air	8			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest terminal to terminal distance across the package surface	8			mm
CTI	Comparative Tracking Index (Tracking resistance)	DIN EN 60112 (VDE 0303-11); IEC 60112	400			V
DTI	Distance through the insulation	Minimum Internal Gap (Internal Clearance)	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A = 25 °C		>10^{12}		Ω
C_{IO}	Barrier capacitance Input to output	$V_{IO} = V_{CC}/2 + 0.4 \sin(2\pi ft)$, f = 1MHz, V_{CC} = 5 V		2		pF
C_I	Input capacitance to ground	$V_I = 0.4 \sin(2\pi ft)$, f = 1MHz		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Material group		II
Overvoltage category / Installation classification for basic insulation	Rated mains voltage ≤ 150V_{rms}	I-IV
	Rated mains voltage ≤ 300V_{rms}	I-III

8.3.3 DIN V VDE V 0884-10 Insulation Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working isolation voltage		566	V_{PK}
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1s, Partial discharge < 5pC	1062	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10s, Partial discharge < 5pC	906	
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10s, Partial discharge < 5pC	680	
V_{IOTM}	Maximum transient isolation voltage	t = 60s (qualification), t = 1s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Tested per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 4000\ V_{PK}$ (Qualification Test)	3077	V_{PK}
R_S	Insulation resistance	V_{IO} = 500V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

8.3.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Approved according to CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1	Approved under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Isolation Voltage, 4242 V_{PK} Maximum Surge Isolation Voltage, 3077 V_{PK} Maximum Working Voltage, 566 V_{PK}	3000 V_{RMS} Isolation Rating; Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 2nd Ed. 150 V_{RMS} working voltage; Basic insulation per CSA 61010-1-04 and IEC 61010-1 2nd Ed. 600 V_{RMS} working voltage; Basic insulation per CSA 60950-1-07 and IEC 60950-1 2nd Ed. 760 V_{RMS} working voltage	Single Protection, 2500 V_{RMS} (1)
Certificate Number: 40016131	Master Contract Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 V_{rms} for 1 second in accordance with UL 1577.

8.3.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 76°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			347	mA
T_S	Maximum safety temperature	DW-16				150	°C

The safety-limiting constraint is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

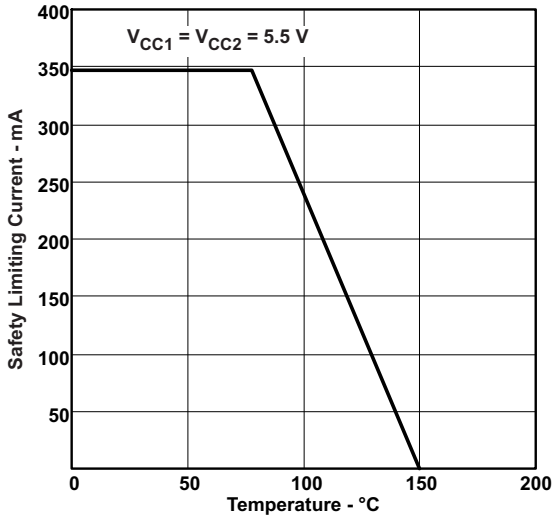


Figure 29. Thermal Derating Curve per VDE

8.4 Device Functional Modes

Table 1 and Table 2 are the function tables for the ISO1176T driver and receiver.

Table 1. Driver Function Table(1)

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	ENABLE OUTPUT (ISODE)	OUTPUTS	
					A	B
PU	PU	H	H	H	H	L
PU	PU	L	H	H	L	H
PU	PU	X	L	L	Z	Z
PU	PU	X	open	L	Z	Z
PU	PU	open	H	H	H	L
PD	PU	X	X	L	Z	Z
PU	PD	X	X	L	Z	Z
PD	PD	X	X	L	Z	Z

(1) PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off)

Table 2. Receiver Function Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$-0.01V \le V_{ID}$	L	H
PU	PU	$-0.2V < V_{ID} < -0.01V$	L	?
PU	PU	$V_{ID} \le -0.2V$	L	L
PU	PU	X	H	Z
PU	PU	X	open	Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Z
PU	PD	X	L	H
PD	PD	X	X	Z

(1) PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off), ? = Indeterminate

8.4.1 Device I/O Schematics

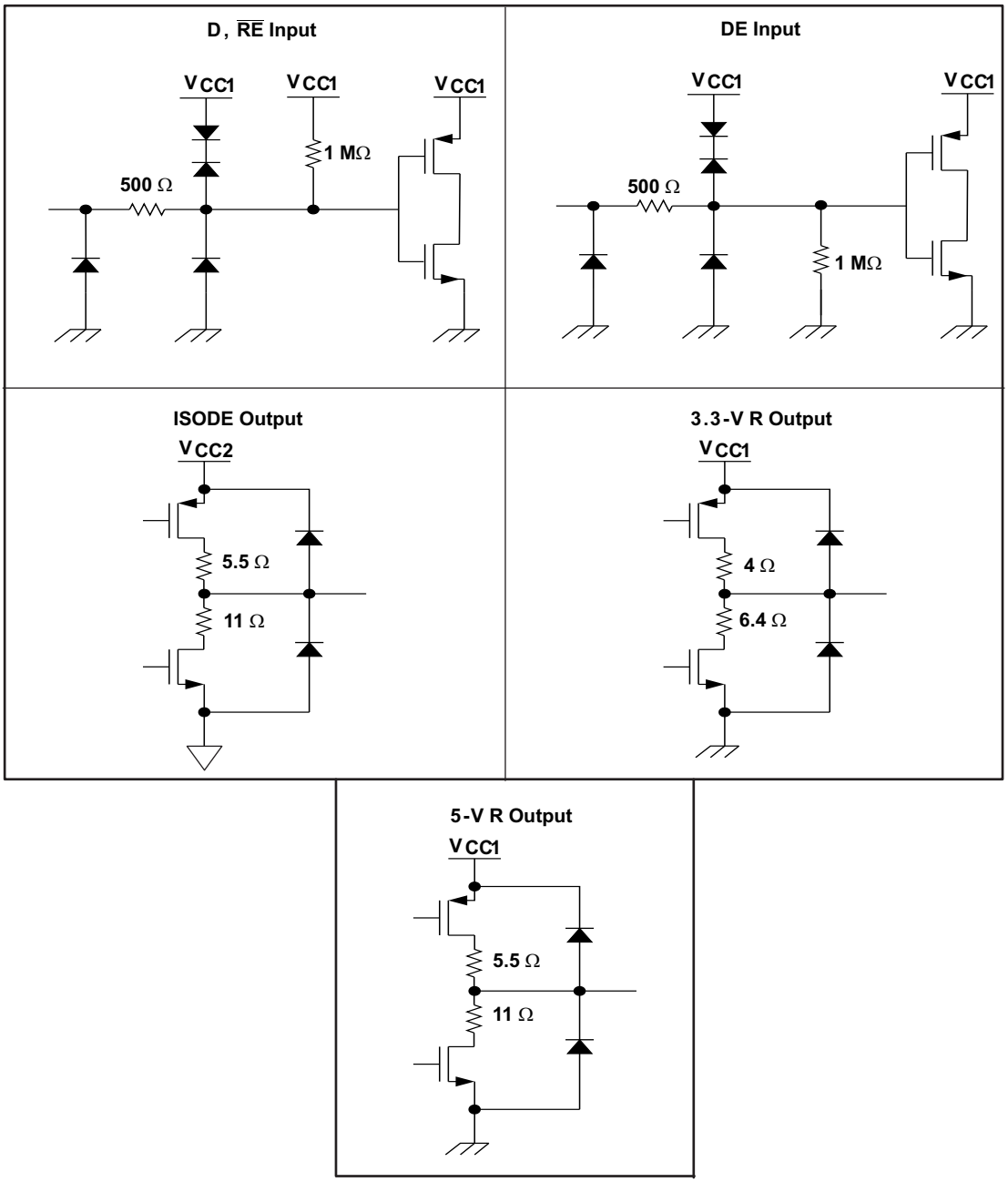


Figure 30. Equivalent Circuit Schematics

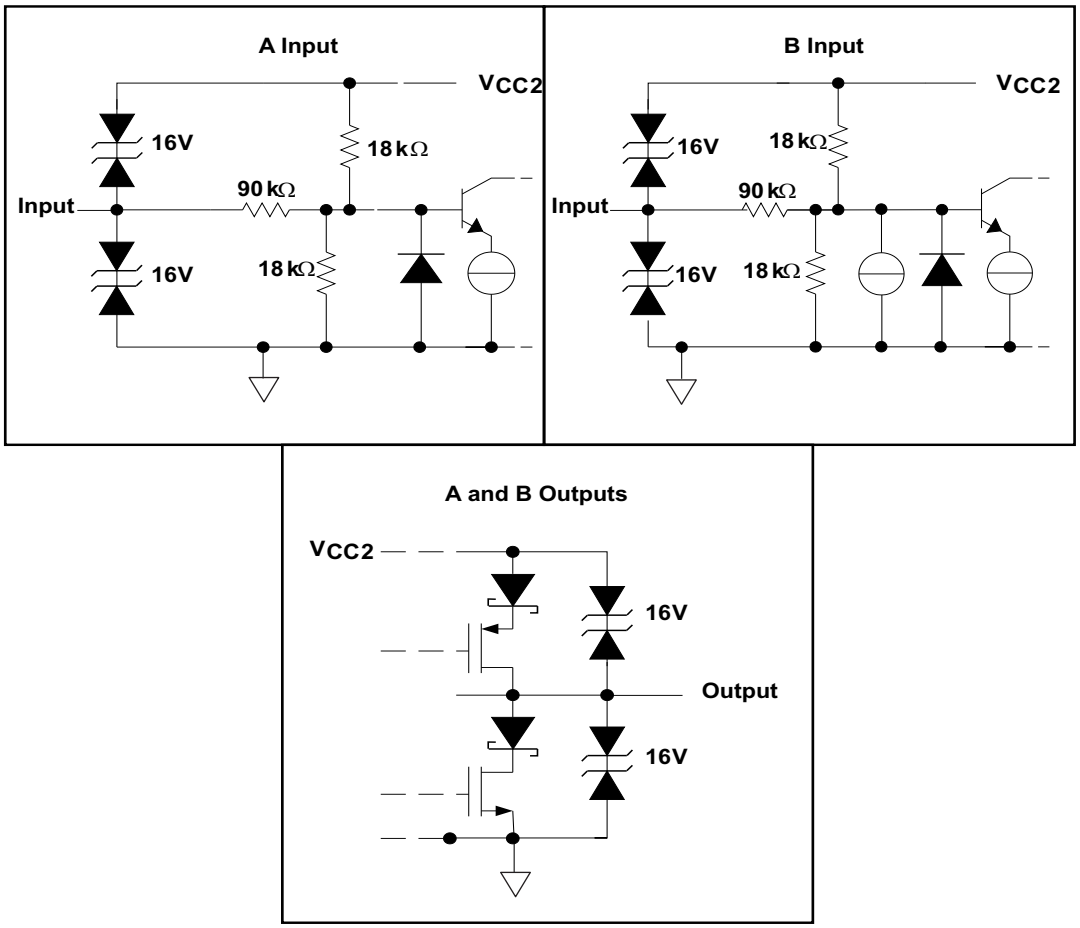


Figure 31. Equivalent Circuit Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO1176T device consists of a RS-485 transceiver, commonly used for asynchronous data transmissions. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

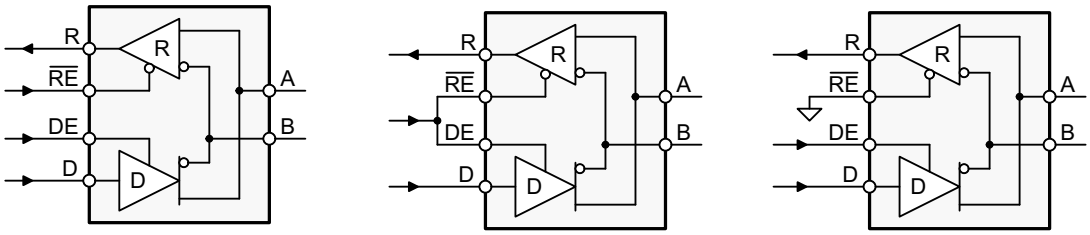


Figure 32. Half-Duplex Transceiver Configurations

9.2 Typical Application

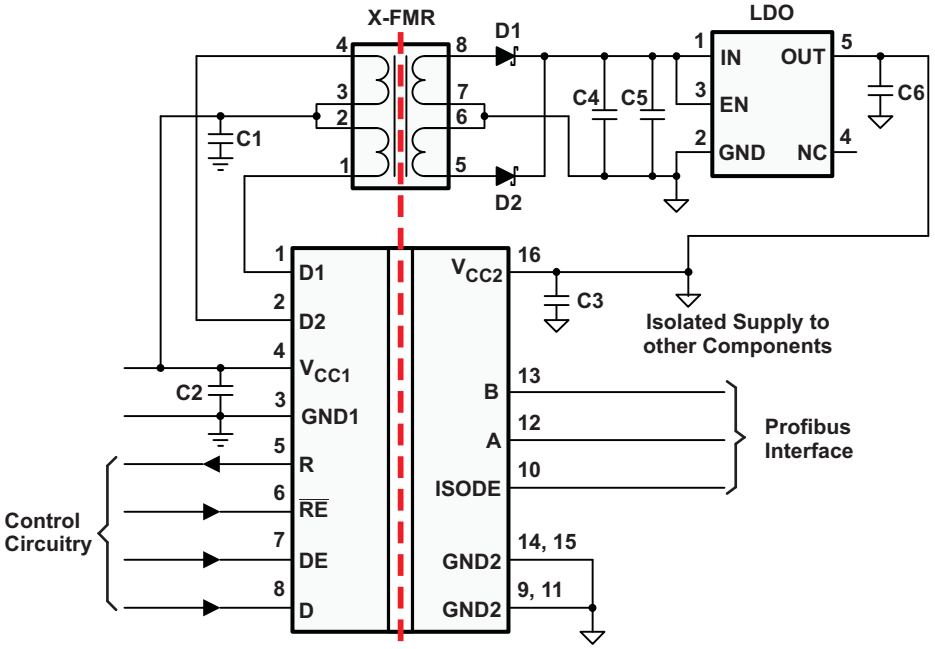


Figure 33. Typical Application

Typical Application (continued)

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Table 3. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltages

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO1176T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high voltage transients.

Figure 34 models the ISO1176T bus IO connected to a noise generator. C_{IN} and R_{IN} is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of ISO1176T plus those of any other insulation (transformer, or similar), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is shown in Equation 1:

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \tag{1}$$

and will always be less than 16 V from V_N. If ISO1176T is tested as a stand-alone device, $R_{IN} = 6 \times 10^4 \Omega$, $C_{IN} = 16 \times 10^{-12}$ F, $R_{ISO} = 10^9 \Omega$ and $C_{ISO} = 10^{-12}$ F.

Note from Figure 34 that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency, as shown in Equation 2,

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4} \tag{2}$$

or essentially all of noise appears across the barrier. At high frequency, as shown in Equation 3,

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94 \tag{3}$$

and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

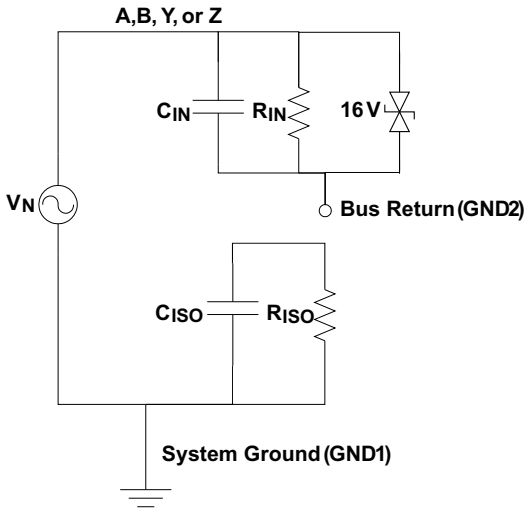


Figure 34. Noise Model

9.2.3 Application Curve

At maximum working voltage, ISO1176T isolation barrier has more than 28 years of life.

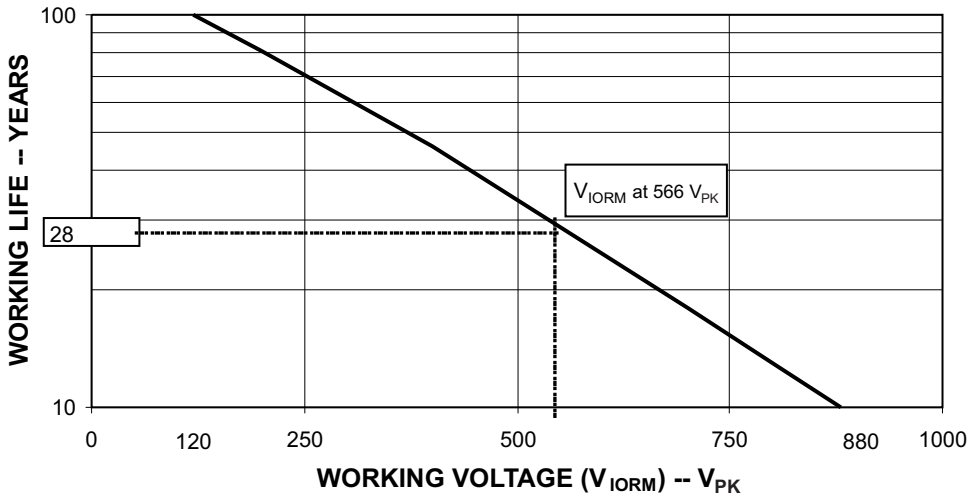


Figure 35. Time-Dependent Dielectric Breakdown Test Results

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-µF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. This device is used in applications where only a single primary-side power supply is available. Isolated power can be generated for the secondary-side with the help of integrated transformer driver.

11 Layout

11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 36).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

NOTE

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

11.2 Layout Example

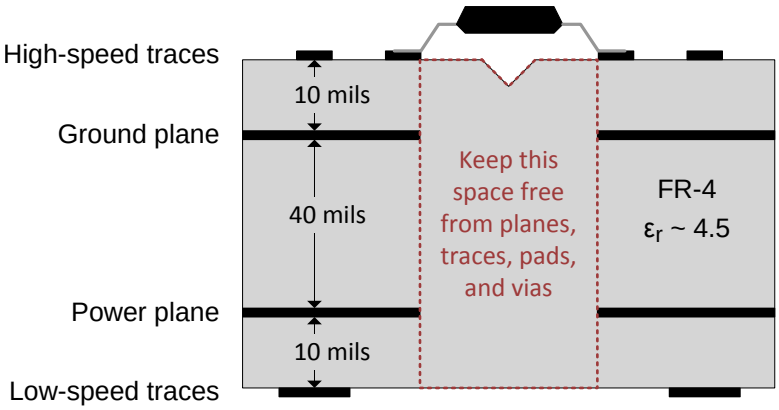


Figure 36. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Isolated, 40-Mbps, 3.3-V to 5-V Profibus Interface* (SLUU471)
- *Digital Isolator Design Guide* (SLLA284)
- *Isolation Glossary* (SLLA353)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1176TDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T	Samples
ISO1176TDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

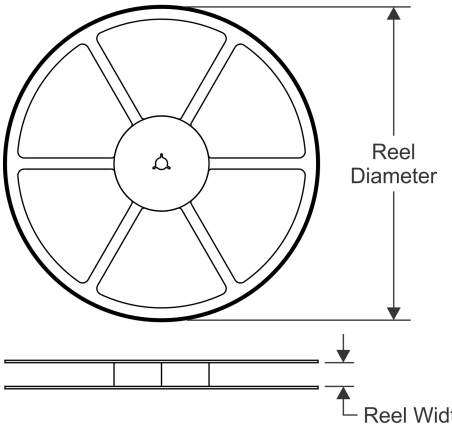
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

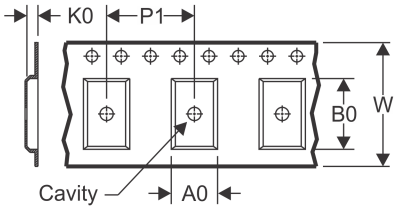
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

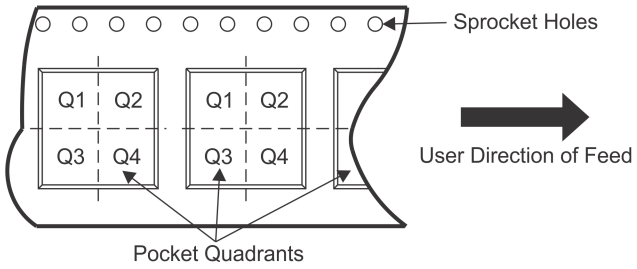


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

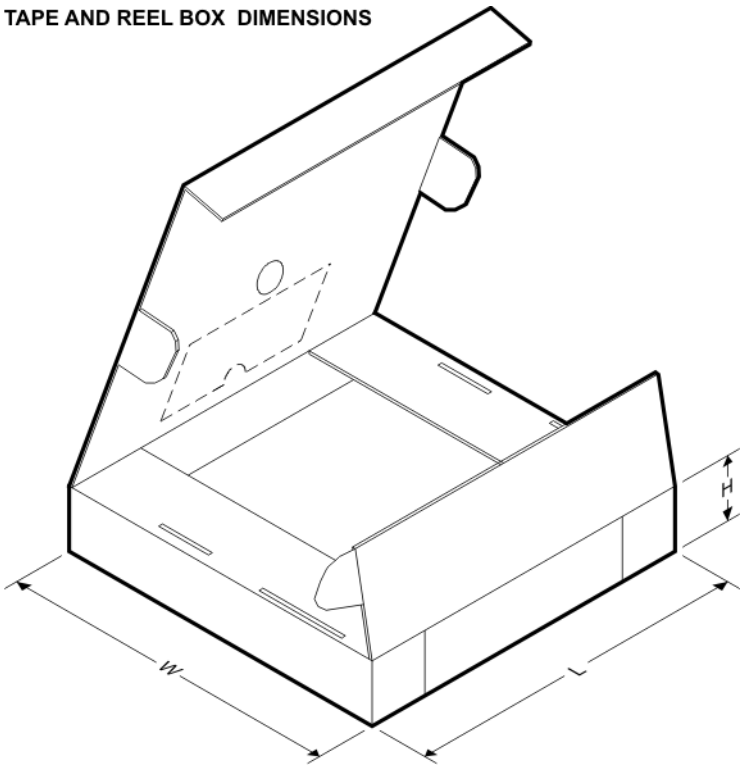
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1176TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

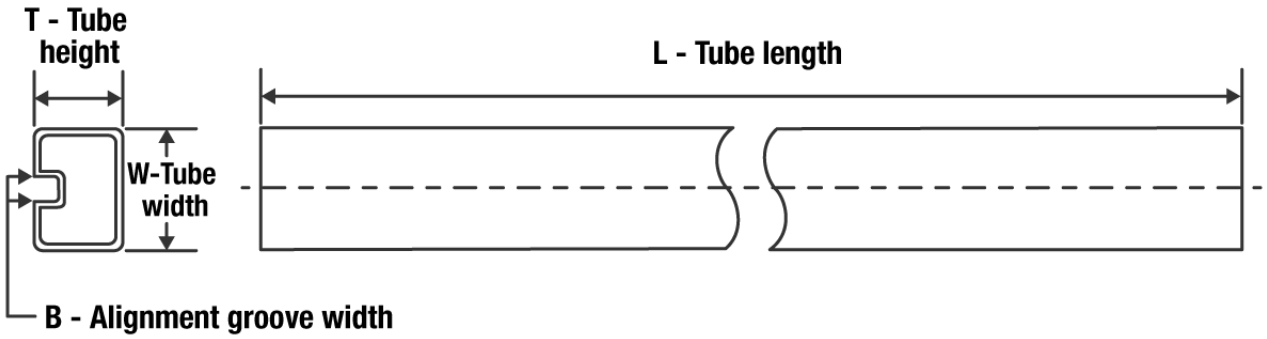
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1176TDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO1176TDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

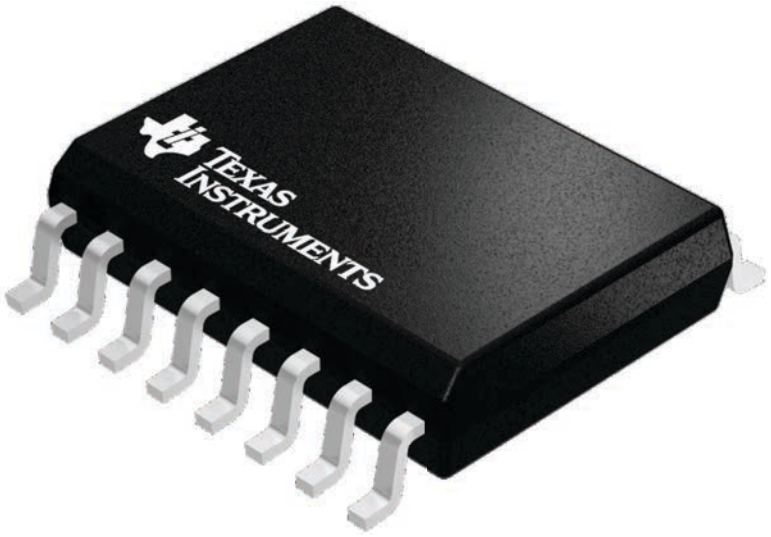
DW 16

SOIC - 2.65 mm max height

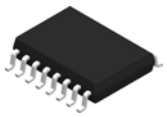
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

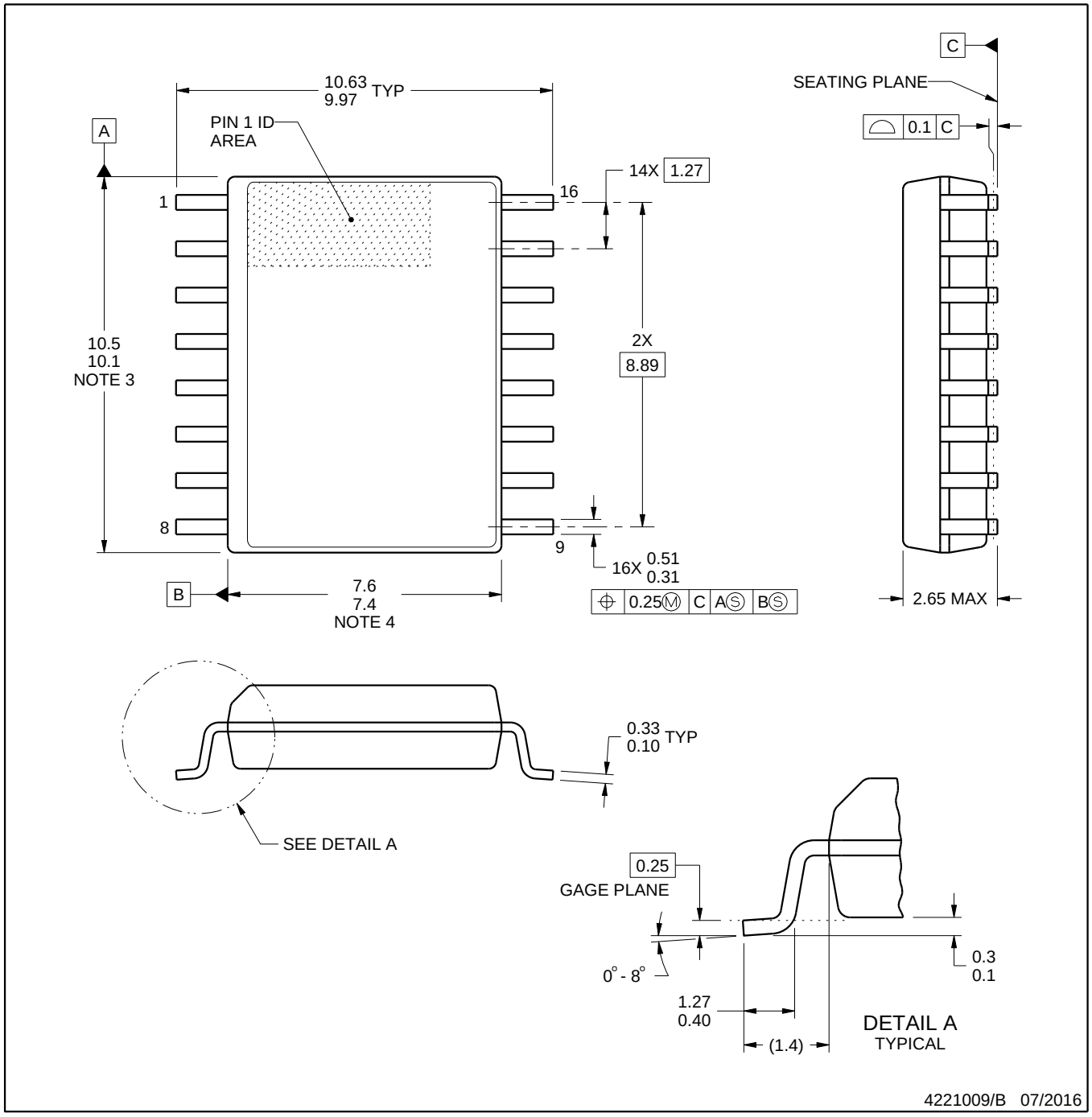


PACKAGE OUTLINE

DW0016B

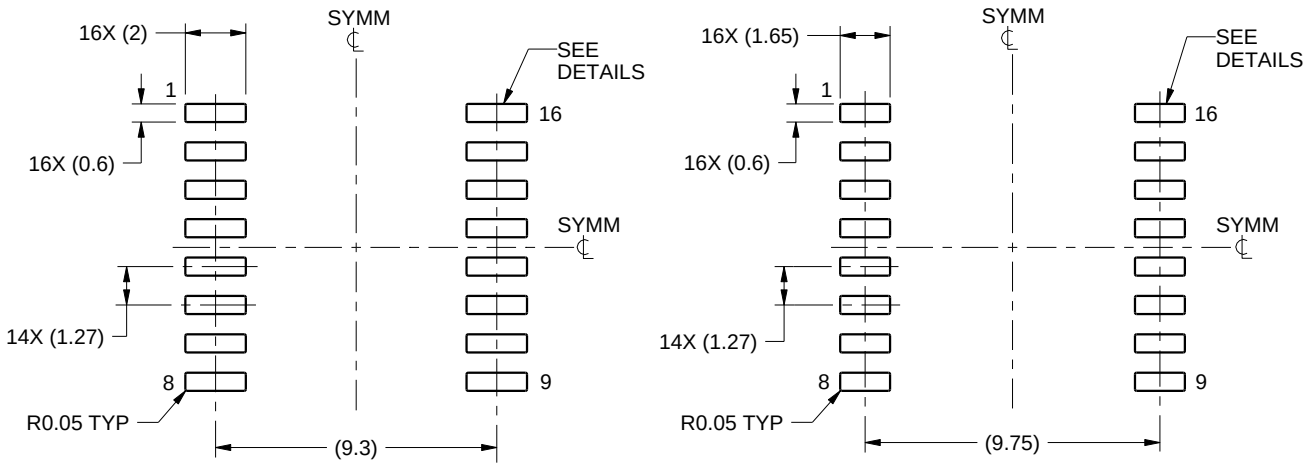
SOIC - 2.65 mm max height

SOIC



NOTES:

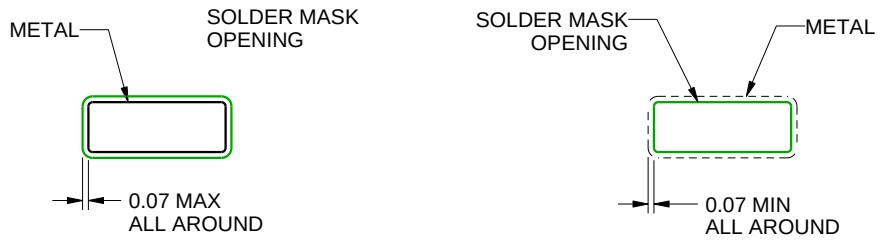
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

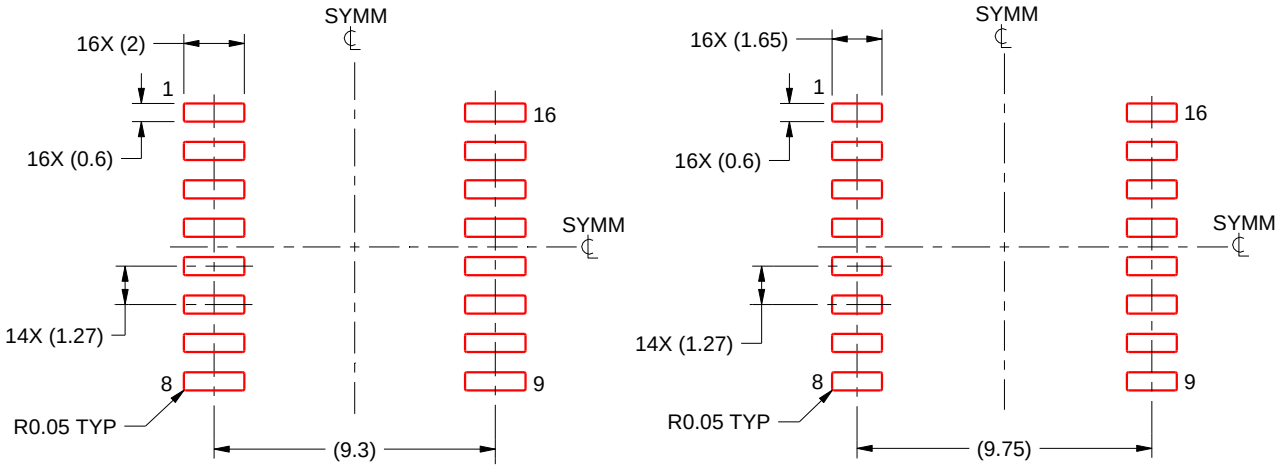
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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>>TI(德州仪器)