TPS92519-Q1 4.5-V to 65-V Dual Automotive 2-A Synchronous Buck LED Driver

1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C2
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 4.5-V to 65-V wide input voltage range
- Up to 2-A output current with 4% accuracy
- Adaptive on-time average current control
- Nominal switching frequency
  - 385 kHz and 435 kHz for channel 1 and channel 2
  - 2 MHz and 2.1 MHz for channel 1 and channel 2
- Advanced dimming operation
  - Precision analog dimming
  - Supports external PWM dimming input
  - Optimized for external shunt dimming including LED matrix manager
- Cycle-by-cycle switch overcurrent protection
- Switch thermal protection
- LED open and short fault monitoring and reporting

2 Applications

- Automotive headlight and adaptive LED driving module

3 Description

The TPS92519-Q1 is a monolithic dual synchronous buck LED driver with a wide 4.5-V to 65-V operating input voltage range that can independently power two strings of series connected LEDs. The TPS92519-Q1 implements an adaptive on-time average current mode control and is designed to be compatible with shunt FET dimming techniques and LED matrix manager-based dynamic beam headlamps. The adaptive on-time control provides near constant switching frequency that can be set using FSET input. Inductor current sensing and closed-loop feedback enables better than ±4% accuracy over wide input voltage, output voltage and ambient temperature range.

The high performance LED driver can independently modulate LED current using both analog or PWM dimming techniques. Linear analog dimming response with over 16:1 range is obtained by varying the voltage from 140 mV to 2.45 V across the high Impedance Analog Adjust (IADJ) input. PWM dimming of LED current is achieved by directly modulating the corresponding UDIM input pin with the desired duty cycle and frequency. The device supports high frequency shunt FET dimming and is compatible with pixel control techniques using LED matrix manager.

The TPS92519-Q1 supports parallel operation of two or more channels thus enabling flexibility required to drive high current LEDs or laser diodes. Current is shared between parallel channels based on IADJ input independent of component tolerances and parasitics.

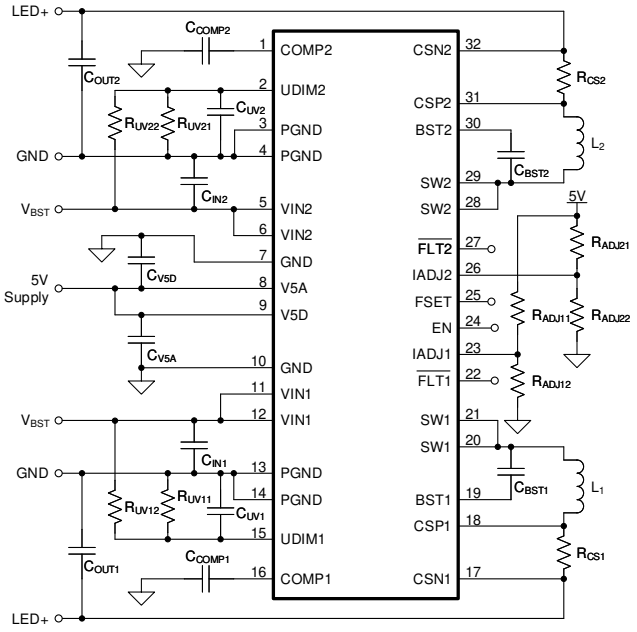
The TPS92519-Q1 incorporates advanced fault protection featuring: cycle-by-cycle switch current limit, bootstrap undervoltage and thermal shutdown. The device includes an open drain fault output to indicate output open and short conditions.

The TPS92519-Q1 is available in a 8.1-mm × 11-mm thermally-enhanced 32-pin HTSSOP package with a 2.75-mm × 3.45-mm bottom-exposed pad.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS92519-Q1	HTSSOP	8.1 mm × 11 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2021) to Revision A (December 2021)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Pin Configuration and Functions

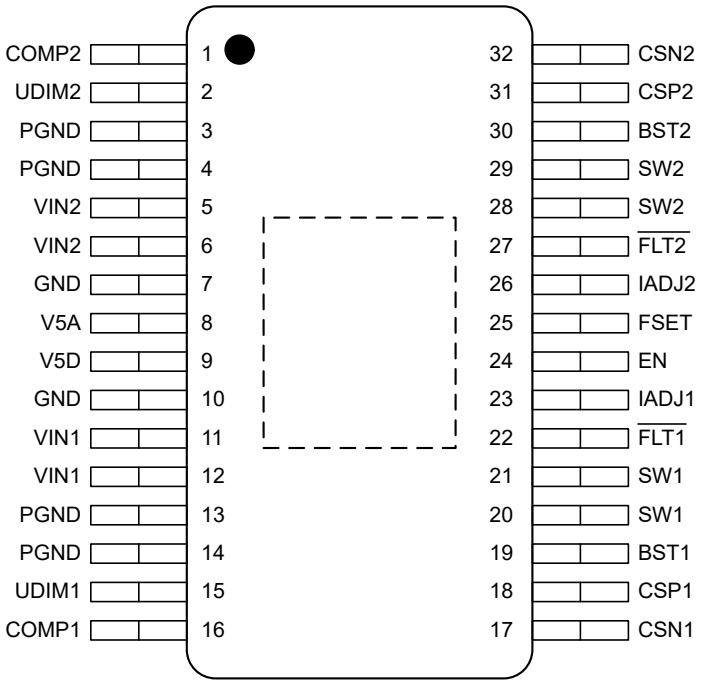


Figure 5-1. DAP Package 32-Pin HTSSOP Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO. DAP		
BST1	19	P	Supply input for high-side MOSFET gate drive circuit. Connect a ceramic capacitor between BSTx and SWx pins. An internal diode is connected between V5D and BSTx.
BST2	30	P	
COMP1	16	I/O	Output of internal transconductance error amplifier. Connect an integral compensation network to ensure stability.
COMP2	1	I/O	
CSN1	17	I	Negative input (–) of internal rail-to-rail transconductance error amplifier. Connect directly to the negative node of the LED current sense resistor, R_{CS}.
CSN2	32	I	
CSP1	18	I	Positive input (+) of internal rail-to-rail transconductance error amplifier. Connect directly to the positive node of the LED current sense resistor, R_{CS}.
CSP2	31	I	
EN	24	I	An active high logic input enables the devices. Pull this pin low to enter low power sleep state.
$\overline{\text{FLT1}}$	22	O	Open-drain fault indicator. Connect to V5D with a resistor to create an active low fault signal output.
$\overline{\text{FLT2}}$	27	O	
FSET	25	I	Frequency select input. Connect to V5D to operate at nominal frequency of 440 kHz. Connect to GND to operate at nominal frequency of 2.1 MHz.
GND	7, 10	G	Signal ground. Return for the internal voltage reference and analog circuits. Connect to circuit ground to complete return path.
IADJ1	23	I	Analog adjust input. Input below 100 mV disables the channel. The analog input can be varied between 140 mV to 2.4 V to set current reference from 10 mV to 173 mV. Connect a 0.1-µF capacitor from pin to GND.
IADJ2	26	I	
PGND	3, 4, 13, 14	G	Ground returns for low-side MOSFETs
SW1	20, 21	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to the power inductor.
SW2	28, 29	P	

Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
	DAP		
UDIM1	15	I	Undervoltage lockout and external PWM dimming input. Connect to VIN through a resistor divider to implement input undervoltage protection. Diode couple external PWM signal to enable dimming. Locally decouple to GND using a 1-nF ceramic capacitor. Do not float.
UDIM2	2	I	
V5A	8	P	Analog supply voltage. Locally decouple to GND using a 100-nF to 1-µF ceramic capacitor located close to the controller.
V5D	9	P	Digital supply voltage. Locally decouple to GND using a 2.2-µF to 4.7-µF ceramic capacitor located close to the controller.
VIN1	11, 12	P	Power inputs and connections to high-side MOSFET drain node. Connect to the power supply and bypass capacitors C_{IN}. The path from the VIN pin to high frequency bypass C_{IN} and PGND must be as short as possible.
VIN2	5, 6	P	

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	V5A, V5D to GND	–0.3	5.5	V
Boot voltage	BSTx to SWx	–0.3	5.5	V
	BSTx to PGND	–0.3	70	V
Switch node voltage	SWx to PGND	–0.5	65	V
	SWx to PGND (< 10ns)	–3.5		V
Drain node voltage	VINx to PGND	–0.3	65	V
Current	CSNx to VINx (< 10µs)		1.5	A
	GND to CSPx, GND to CSNx (< 10µs)		430	mA
Inputs	CSNx - VINx		0.5	V
	CSPx, CSNx to GND	–0.5	65	V
	CSPx to CSNx	–0.3	0.3	V
	UDIMx to GND	–0.3	65	V
	COMPx, IADJx, FSET, EN to GND	–0.3	5.5	V
Outputs	$\overline{FLTx}$ to GND	–0.3	5.5	V
Junction temperature	T_J		150	°C
Lead temperature	Soldering, 10 s		260	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 16, 17, and 32)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5		63	V
V_{5A}, V_{5D}	Bias supply	4.5	5	5.3	V
d_{V5x}/dt	Bias supply slew-rate	20			V/s
$\Delta V_{(CSP-CSN)}$	Sensed inductor current ripple	20			mV
dv_{CSP}/dt	CSP slew-rate			10	V/µs
I_{LED}	LED current			2	A
f_{UDIM}	External PWM dimming frequency			1000	Hz
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		DEVICE DAP (HTSSOP) 32	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	26.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The package thermal impedance is calculated in accordance with JESD51-7 standard with a 4-layer board and 2 W power dissipation.
(3) A heatsink or airflow would yield a much better $R_{\theta JA}$.

6.5 Electrical Characteristics

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} =C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL ANALOG AND GATE DRIVE SUPPLIES (V5D, V5A)						
$V_{V5D,A(UVLO)}$	V_{5D} and V_{5A} UVLO threshold	Rising		4.10	4.26	V
		Falling	3.84	4.00		V
		Hysteresis		100		mV
$I_{V5A(STBY)}$	Analog supply stand-by current	V_{UDIM1} = V_{UDIM2} = 0 V		4	5.5	mA
$I_{V5D(STBY)}$	Gate drive supply stand-by current	V_{UDIM1} = V_{UDIM2} = 0 V		0.9	1.3	mA
$I_{V5A(SLEEP)}$	Analog supply sleep state current	V_{EN} = 0 V		14	300	nA
$I_{V5D(SLEEP)}$	Gate drive supply sleep state current	V_{EN} = 0 V		17	24	µA
$I_{VINx(SLEEP)}$	VIN pin sleep state current	V_{INx} = 15 V, V_{EN} = 0 V		2	4	µA
$I_{V5D(SW)}$	Gate drive supply switching current	V_{V5D} = 5 V, V_{FSET} = 5 V, CH1 and CH2 switching		6	10	mA
ENABLE INPUT (EN)						
V_{EN}	Enable voltage rising threshold				1.8	V
	Enable voltgae falling threshold		0.8			mV
I_{EN}	Enable input bias current			10		µA
HIGH-SIDE FET (SWx, BOOTx)						
$R_{DSx(ON-HS)}$	High-side MOSFET on resistance	V_{INx} = 6 V, V_{BSTx} = 11 V, I_{HSx} = 100 mA		240	465	mΩ
$V_{BSTx(UV)}$	Bootstrap UVLO threshold	Falling, V_{INx} = 6 V, V_{SWx} = 0 V	2.60	2.95	3.30	V
		Hysteresis, V_{INx} = 6 V, V_{SWx} = 0 V	115	184	245	mV
$I_{Q(xBST)}$	Bootstrap pin quiescent current	V_{BSTx} = 5 V, V_{SWx} = 0 V	200	250	300	µA
LOW-SIDE FET (SWx)						
$R_{DSx(ON-LS)}$	Low-side MOSFET on resistance	V_{INx} = 6 V, I_{LSx} = 100 mA		240	465	mΩ
HIGH-SIDE FET CURRENT LIMIT						
$I_{HSx(ILIM)}$	High-side current limit threshold	V_{INx} = 6 V	2.8	3.5	4.2	A
$t_{HSx(LEB)}$	High-side current sense leading-edge blanking period	V_{INx} = 6 V	35	60	80	ns
$t_{HSx(RES)}$	Current limit response time	V_{INx} = 6 V		20		ns
LOW-SIDE FET CURRENT LIMIT						

6.5 Electrical Characteristics (continued)

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} =C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LSx(ILIM)}$	Low-side sinking current limit threshold	V_{INx} = 6 V	1.67	2.50	3.5	A
$t_{LSx(LEB)}$	Low-side current sense leading-edge blanking period	V_{INx} = 6 V		76		ns
SWITCHING FREQUENCY (FSET)						
V_{FSET}	Frequency set input rising threshold				1.8	V
	Frequency set input falling threshold		0.8			V
I_{FSET}	Frequency set input bias current			10		µA
$t_{ON(SW1)}$	Channel 1 on-time	V_{FSET} = 0 V, V_{IN} = 50 V, V_{CSP} = 38 V		384		ns
		V_{FSET} = 5 V, V_{IN} = 50 V, V_{CSP} = 25 V		1.36		µs
$t_{ON(SW2)}$	Channel 2 on-time	V_{FSET} = 0 V, V_{IN} = 50 V, V_{CSP} = 38 V		365		ns
		V_{FSET} = 5 V, V_{IN} = 50 V, V_{CSP} = 25 V		1.20		µs
ANALOG ADJUST SETTING AND CURRENT SENSE AMPLIFIER (IADJx, CSPx, CSNx)						
$V_{IADJx(CLP)}$	IADJx internal limit		2.38	2.45	2.52	V
$V_{IADJx(SD)}$	Shutdown threshold	Rising, V_{INx} = 6 V		140		mV
		Falling, V_{INx} = 6 V		100		mV
$V_{(CSPx-CSNx)}$	Current sense threshold	V_{CSPx} = 6 V, V_{IADJx} > 2.45V	167.5	173.0	178.5	mV
		V_{CSPx} = 6 V, V_{IADJx} = 1.22V	83.0	88.5	94.0	mV
		V_{CSPx} = 6 V, V_{IADJx} = 460mV	29.0	34.5	40.0	mV
		V_{CSPx} = 6 V, V_{IADJx} = 150mV	6.5	12.5	18.5	mV
$g_{mx(LV)}$	Level shift amplifier transconductance	V_{INx} = 63 V, V_{CSNx} = 5 V		50		µA/V
$V_{CSPx(SHT)}$	Output short circuit detection threshold	Rising		1.71		V
		Falling		1.50		V
ON-TIME GENERATOR						
$t_{ONx(MIN)}$	Minimum on-time.	V_{INx} = 4.5 V	90	110	130	ns
OFF-TIME GENERATOR						
$t_{OFFx(MIN)}$	Minimum off-time	V_{INx} = 4.5 V	57	78	86	ns
PWM DIMMING and PROGRAMMABLE UVLO INPUT (DIMx)						
$V_{UDIMx(DO)}$	UDIM dropout detection threshold	Rising		2.45	2.52	V
		Falling	1.95	2.35		V
$V_{UDIMx(EN)}$	UDIM undervoltage lockout threshold	Rising		1.22	1.27	V
		Falling	0.97	1.02		V
$I_{UDIMx(UVLO)}$	UDIM source current (UVLO hysteresis)	V_{UDIMx} = 1.5 V	6.3	10	12	µA
ERROR AMPLIFIER (COMPx)						
g_M	Transconductance	V_{INx} = 63 V		450		µA/V
$I_{COMPx(SRC)}$	COMPx current source capacity	V_{INx} = 63 V, $V_{(CSPx–CSNx)}$ = 0 V, V_{IADJx} = 1.4 V		45		µA
$I_{COMPx(SINK)}$	COMPx current sink capacity	V_{INx} = 63 V, $V_{(CSPx–CSNx)}$ = 200 mV, V_{IADJx} = 1.4 V		45		µA

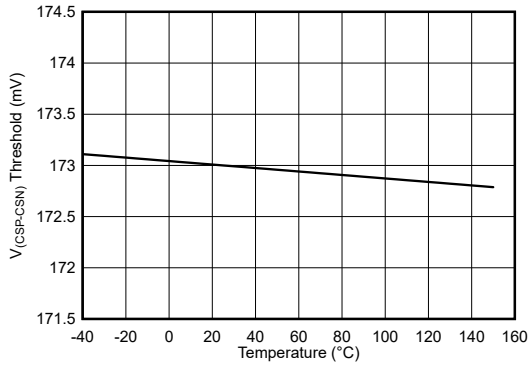
6.5 Electrical Characteristics (continued)

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} =C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$EA_{x(BW)}$	Bandwidth	Unity gain		3		MHz
$EA_{(VD)}$	Input differential sense range		–225		225	mV
$EA_{(CM)}$	Input common mode range	V_{INx} = 63 V	0		V_{INx} – 0.5	V
$I_{COMPx(LKG)}$	COMPx leakage current	V_{UDIMx} = 0 V		2.5		nA
$V_{COMPx(ST)}$	COMPx startup threshold	Rising		2.45		V
		Hysteresis		425		mV
$V_{COMPx(OV)}$	COMPx over-voltage detection threshold	Rising	3.0	3.2		V
		Hysteresis		75		mV
$R_{COMPx(DCH)}$	COMPx discharge FET resistance			230		Ω
$V_{COMPx(RST)}$	Reset voltage	Falling		100		mV
FAULT INDICATOR ($\overline{FLT}$)						
$R_{(\overline{FLTx})}$	Fault pin pull-down resistance			3	7	Ω
T_{OC}	Hiccup retry delay time			3.6		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			175		°C

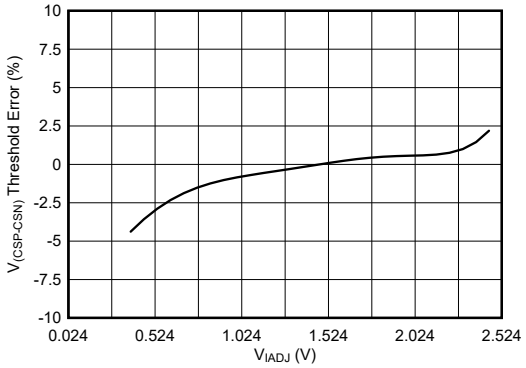
6.6 Typical Characteristics

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)



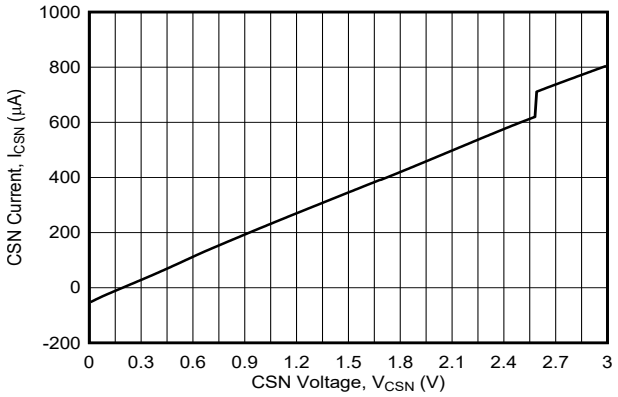
V_{CSN} = 3 V

Figure 6-1. $V_{(CSP–CSN)}$ Current Sense Threshold vs Temperature



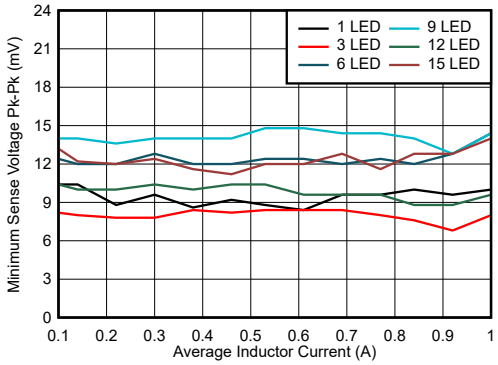
V_{CSN} = 3 V V_{IN} = 60 V

Figure 6-2. $V_{(CSP–CSN)}$ Current Sense Error vs IADJ Count



V_{IADJ} =0 V

Figure 6-3. CSN Source Current vs CSN Voltage



L = 68 µH V_{IN} = 60 V

Figure 6-4. Minimum Ripple Voltage vs Average Inductor Current

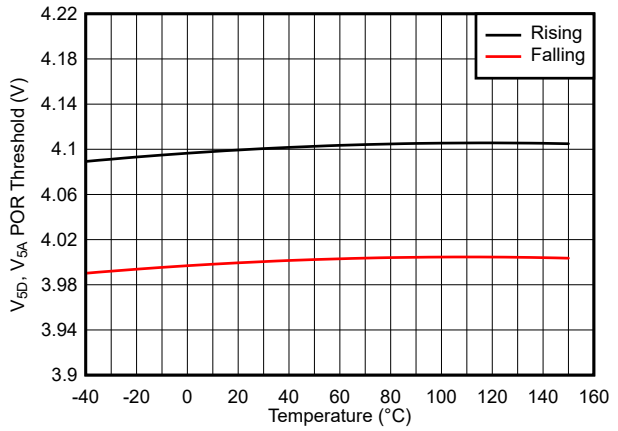


Figure 6-5. $V_{5D,A}$ POR Threshold vs Temperature

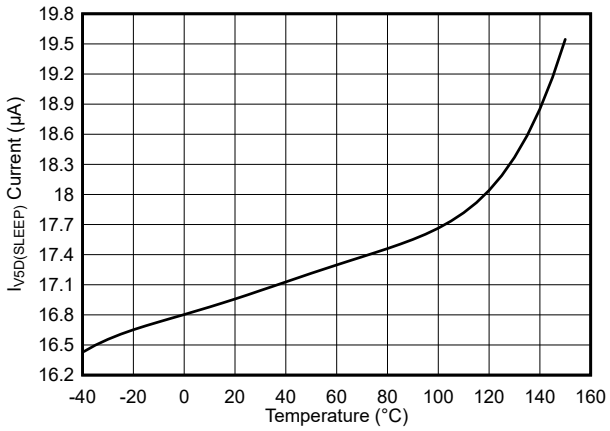


Figure 6-6. V5D Sleep Current vs Temperature

6.6 Typical Characteristics (continued)

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)

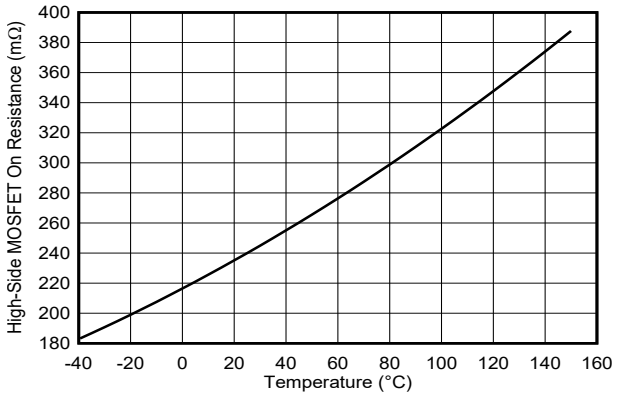


Figure 6-7. High Side MOSFET On Resistance vs Temperature

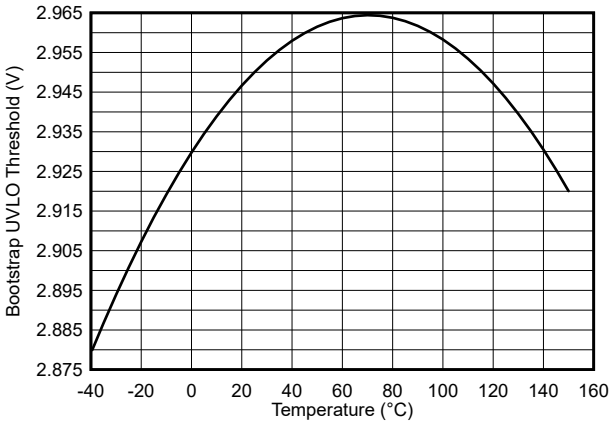


Figure 6-8. Bootstrap UVLO Threshold vs Temperature

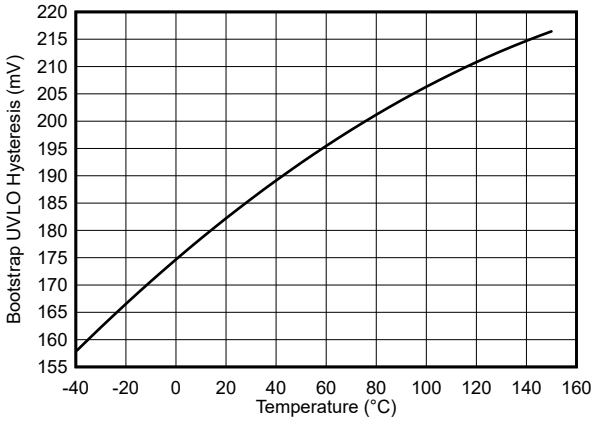


Figure 6-9. Bootstrap UVLO Hysteresis vs Temperature

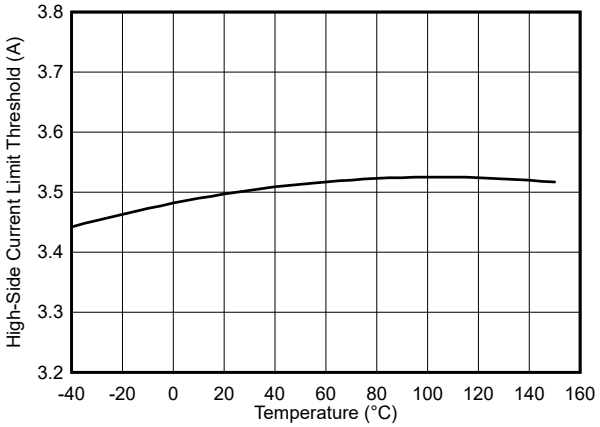


Figure 6-10. High-Side Current Limit Threshold vs Temperature

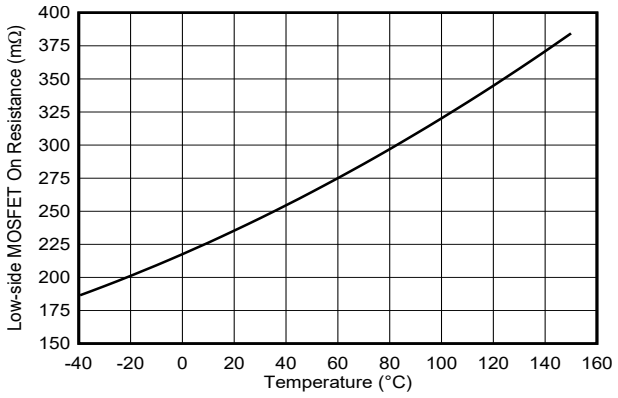


Figure 6-11. Low-Side MOSFET On Resistance vs Temperature

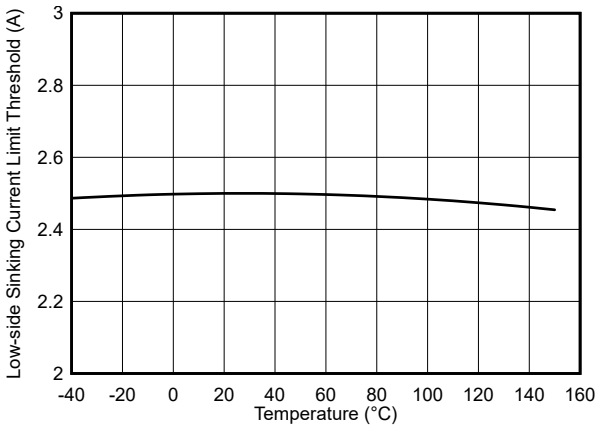


Figure 6-12. Low-Side Sinking Current Limit Threshold vs Temperature

6.6 Typical Characteristics (continued)

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)

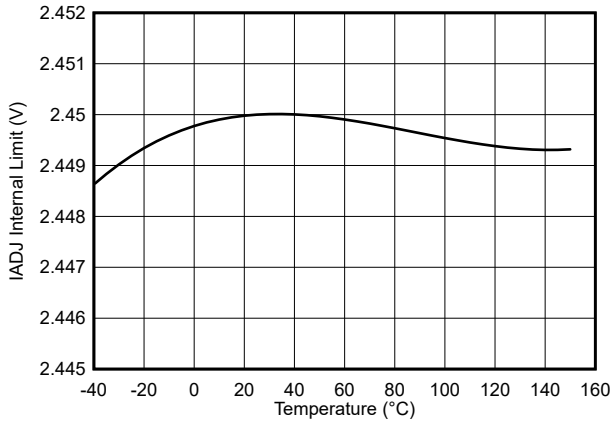


Figure 6-13. IADJ Internal Limit vs Temperature

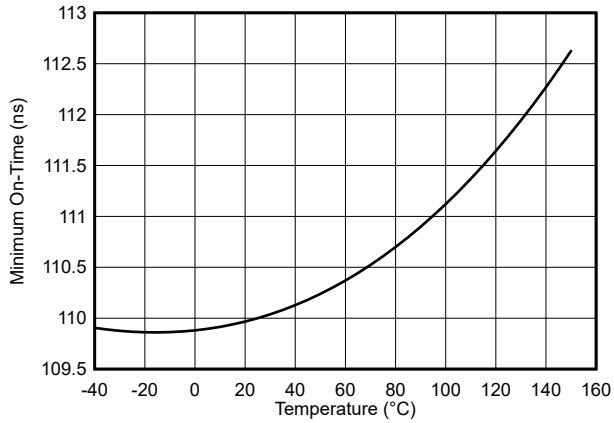


Figure 6-14. Minimum On-time vs Temperature

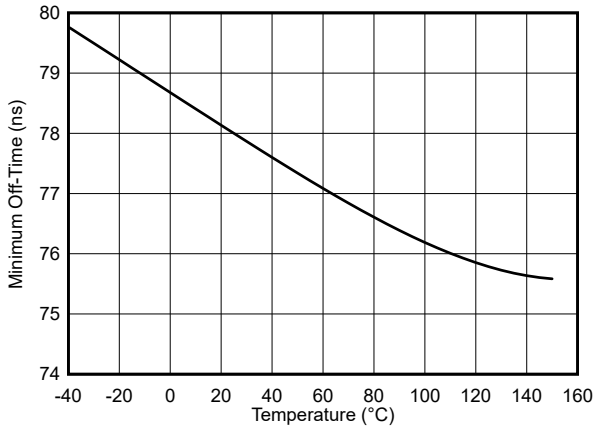


Figure 6-15. Minimum Off-time vs Temperature

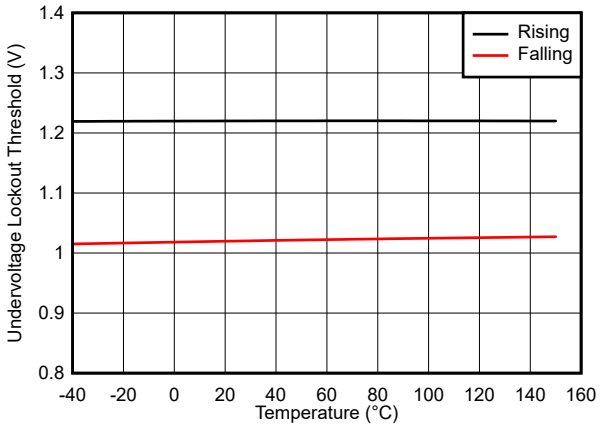


Figure 6-16. UDIM Undervoltage Lockout Threshold vs Temperature

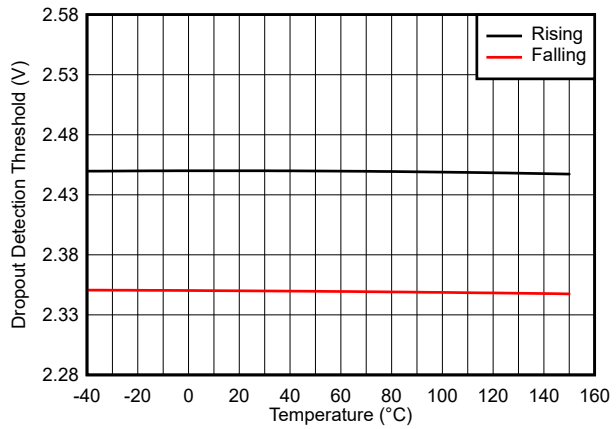


Figure 6-17. UDIM Dropout Detection Threshold vs Temperature

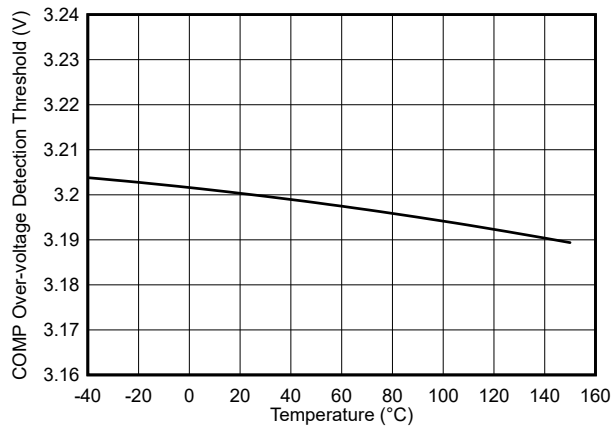


Figure 6-18. COMP Overvoltage Detection Threshold vs Temperature

6.6 Typical Characteristics (continued)

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, $\overline{FLTx}$ pin floating (unless otherwise noted)

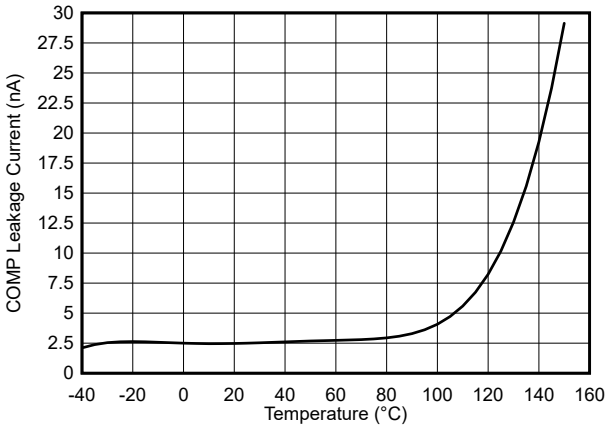
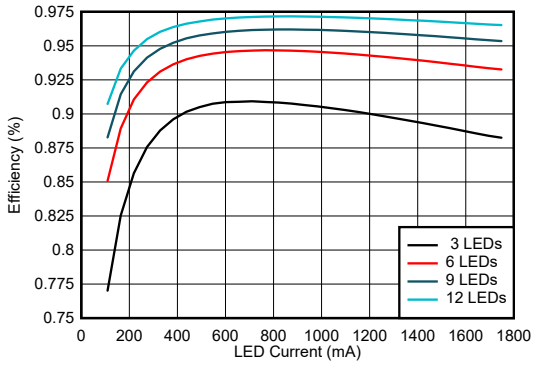


Figure 6-19. COMP Leakage Current vs Temperature



$V_{FPIN} = 5$ V $V_{IN} = 60$ V

Figure 6-20. Efficiency vs LED Current

7 Detailed Description

7.1 Overview

The TPS92519-Q1 is a dual synchronous buck LED driver with a 4.5-V to 65-V input voltage range. The device can deliver up to 2 A of continuous current per channel and power two independent strings of one to 16 series-connected LEDs. The device implements an adaptive on-time current regulation control technique to achieve fast transient response. This architecture uses a comparator and a one-shot on-timer that varies inversely with input and output voltage to maintain a near-constant frequency. With the FSET pin connected to V5D the on-time generator ensure near constant frequency of 385 kHz for channel 1 and 440 kHz for channel 2. With the FSET pin grounded the on-time generator is programmed to operate channel 1 at approximately 2 MHz and channel 2 at 2.15 MHz. The on-time between two channels is offset to ensure low EMI signature. The integrated low offset rail-to-rail error amplifier enables closed-loop regulation of LED current and ensures better than 4% accuracy over a wide input, output, and temperature range.

The LED current reference is set by forcing voltage on IADJ input and can be varied from 140 mV to 2.45 V to achieve over a 16:1 linear analog dimming range. Pulse Width Modulation (PWM) dimming of the LED current is achieved by modulating the duty cycle of external voltage signal at UDIMx input. The external UDIMx input acts as an enable and directly controls the LED current. This device optimizes the inductor current response and is capable of achieving over a 1000:1 PWM dimming ratio.

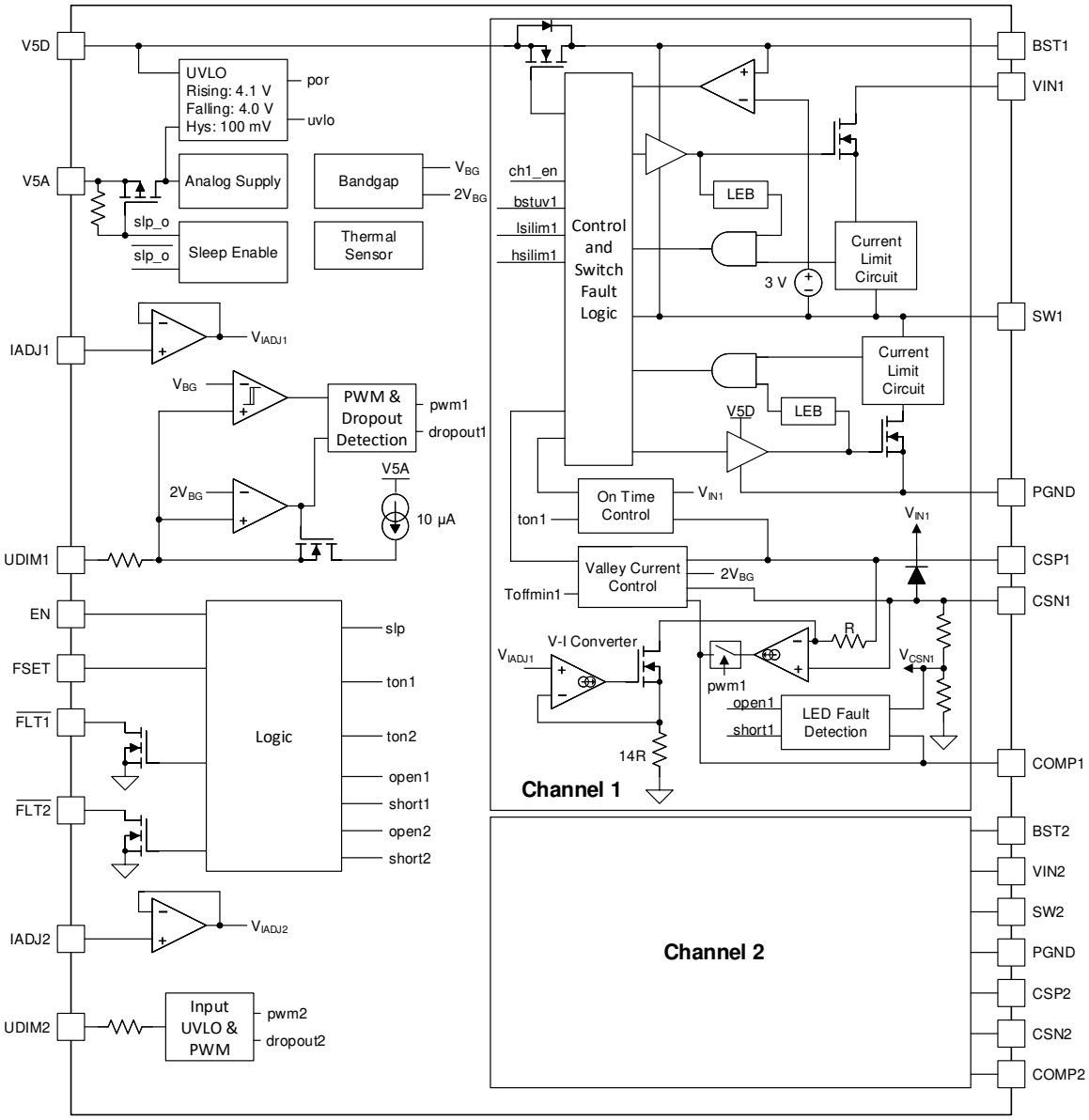
The device incorporates an enhanced programmable fault feature including the following:

- Cycle-by-cycle switch overcurrent limit
- Input undervoltage protection
- Boot undervoltage protection
- Comp overvoltage protection
- Output open circuit indication
- Output short circuit indication

In addition, Thermal Shutdown (TSD) protection is implemented to limit the junction temperature at 175°C (typical). The open-drain fault output, $\overline{\text{FLTx}}$, indicates the status of the LEDs and is forced low whenever an output open or short fault is detected by the device.

Toggling the enable input, EN, low forces the device in low-power sleep state. In this state, both channels are disabled and analog supply, V5A, is disconnected to reduce the bias current drawn by the device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Buck Converter Switching Operation

The following operating description of the TPS92519-Q1 refers to the *Functional Block Diagram* and the waveforms in Figure 7-1. The main control loop of the TPS92519-Q1 is based on an adaptive on-time pulse width modulation (PWM) technique that combines a constant on-time control with an inductor valley current sense circuit for pseudo-fixed frequency operation. This proprietary control technique enables closed-loop regulation of LED current and fast dynamic response necessary to meet the requirements for LED pixel control and LED matrix beam applications.

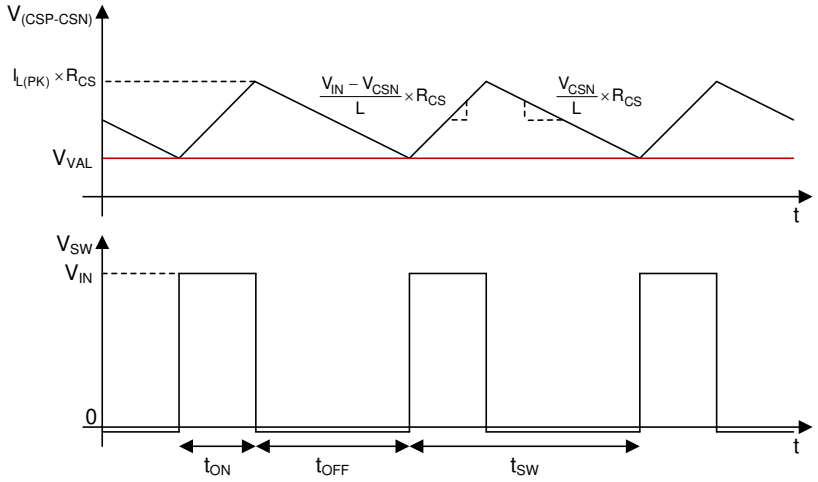


Figure 7-1. Adaptive On Time Control Buck Converter Waveforms

In steady state, the high-side MOSFET is turned on at the beginning of each cycle. The on-time duration of this MOSFET is controlled by an internal one-shot timer and the high-side MOSFET is turned off after the timer expires. The one-shot timer duration is set by the output voltage measured at the CSP pin, V_{CSP}, and the input voltage measured at the VIN pin, V_{IN}, to maintain a pseudo-fixed frequency. During the on-time interval, the inductor current increases with a slope proportional to the voltage applied across its terminals ($V_{IN} – V_{CSP}$).

The low-side MOSFET is turned on after a fixed deadtime and the inductor current then decreases with the constant slope proportional to the output voltage, V_{CSP}. Inductor current measured by the external sense resistor is compared to the valley threshold, V_{VAL}, by an internal high-speed comparator. This MOSFET is turned off and the one-shot timer is initiated when the sensed inductor current falls below the valley threshold voltage. The high-side MOSFET is turned on again after a fixed deadtime.

The internal rail-to-rail error amplifier sets the valley threshold voltage and regulates the average inductor current based on a reference set by IADJx input. A simple integral loop compensation circuit consisting of a capacitor connected from the COMP pin to GND provides a stable and high-bandwidth response. As the inductor current is directly sensed by an external resistor, the device operation is not sensitive to the ESR of the output capacitors and is compatible with common multi-layered ceramic capacitors (MLCC).

7.3.2 Switching Frequency and Adaptive On-Time Control

The TPS92519-Q1 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The one-shot timer is programmed by the voltage on FSET input. The on-time is calculated internally using Equation 1 and is inversely proportional to the measured input voltage, V_{IN}, and proportional to the measured CSP voltage, V_{CSP}.

$$t_{ON} = \kappa \times \frac{V_{CSP}}{V_{IN}} \tag{1}$$

Constant, κ, is set by the FSET pin logic.

$$\kappa = \left.\begin{matrix} 2.606 \times 10^{-6} \text{ for channel 1} \\ 2.285 \times 10^{-6} \text{ for channel 2} \end{matrix}\right\} V_{FSET} > 1.8 \text{ V}$$

$$\kappa = \left.\begin{matrix} 4.890 \times 10^{-7} \text{ for channel 1} \\ 4.676 \times 10^{-7} \text{ for channel 2} \end{matrix}\right\} V_{FSET} < 0.8 \text{ V} \tag{2}$$

Given the duty ratio of the buck converter is V_{CSP} / V_{IN}, the switching period, T_{SW}, remains nearly constant over all operating points. Use Equation 3 to calculate the switching period.

$$T_{SW} = t_{ON} \times \frac{V_{IN}}{V_{CSP}} = \kappa \tag{3}$$

Use Equation 4 to calculate the switching frequency.

$$f_{SW} = \frac{1}{\kappa} \tag{4}$$

7.3.3 Minimum On-Time, Off-Time, and Inductor Ripple

Buck converter operation is impacted by minimum on-time, minimum off-time, and minimum peak-to-peak inductor ripple limitations. The converter reaches the minimum on-time when operating with high input voltage and low-output voltage. In this control scheme, the off-time continues to increase and the switching frequency reduces to regulate the inductor current and LED current to the desired value.

$$f_{SW(MIN)} = \frac{V_{OUT(MIN)}}{t_{ON(MIN)} \times V_{IN(MAX)}}; \; t_{ON} = t_{ON(MIN)} \tag{5}$$

The converter reaches the minimum off-time when operating in dropout (low input voltage and high output voltage). As the on-time and off-time are fixed, the duty cycle is constant and the buck converter operates in open-loop mode. The inductor current and LED current are not in regulation. The converter continues to switch unless disabled by the IADJx input.

The behavior and response of valley comparator is dependent on sensed peak-to-peak voltage ripple, $\Delta V_{(CSP-CSN)}$, and is a function of current sense resistor, R_{CS}, and peak-to-peak inductor current ripple, $\Delta i_{L(PK-PK)}$. To ensure periodic switching, the sensed peak-to-peak ripple must exceed the minimum value. At high (near 100%) or low (near 0%) duty cycles, the inductor current ripple is not sufficient to ensure periodic switching. Under such operating conditions, the converter transitions from periodic switching to a burst sequence, forcing multiple on-time and off-time cycles at a rate higher than the programmed frequency. Although the converter cannot operate in a periodic manner, the closed-loop control continues regulating the average LED current with a larger ripple value corresponding to higher peak-to-peak inductor ripple. TI recommends choosing an inductor, output capacitor, and switching frequency to ensure minimum sensed peak-to-peak ripple voltage under nominal operating condition is greater than 20 mV. The *Application and Implementation* section summarizes the detailed design procedure.

7.3.4 Enable

The TPS92519-Q1 has an enable input EN for start-up and shutdown control of the output. If the enable input is greater than 1.8 V then both channels are enabled. If the enable pin is pulled below 0.8 V, the channels are disabled and the TPS92519-Q1 is switched to a low I_Q shutdown mode. In this mode, the device draws a 2-µA typical current from the VIN pin and 17-µA typical from V5D pin. TI does not recommend leaving EN pin floating.

7.3.5 LED Current Regulation and Error Amplifier

The reference voltage, V_{IADJ}, is internally scaled by a gain factor of 1/14 through a resistor network. An internal rail-to-rail error amplifier generates an error signal proportional to the difference between the scaled reference voltage (V_{IADJ} / 14) and the inductor current measured by the differential voltage drop between CSP and CSN, $V_{(CSP-CSN)}$. This error drives the COMP pin voltage, V_{COMP}, and directly controls the valley threshold of the inductor current. Zero average DC error and closed-loop regulation is achieved by implementing an integral compensation network consisting of a capacitor connected from the output of the error amplifier to GND. As a good starting point, TI recommends a capacitor value between 1 nF and 10 nF between the COMP pin and GND. The choice of compensation network must ensure a minimum of 60° of phase margin and 10 dB of gain margin. The *Application and Implementation* section summarizes the detailed design procedure.

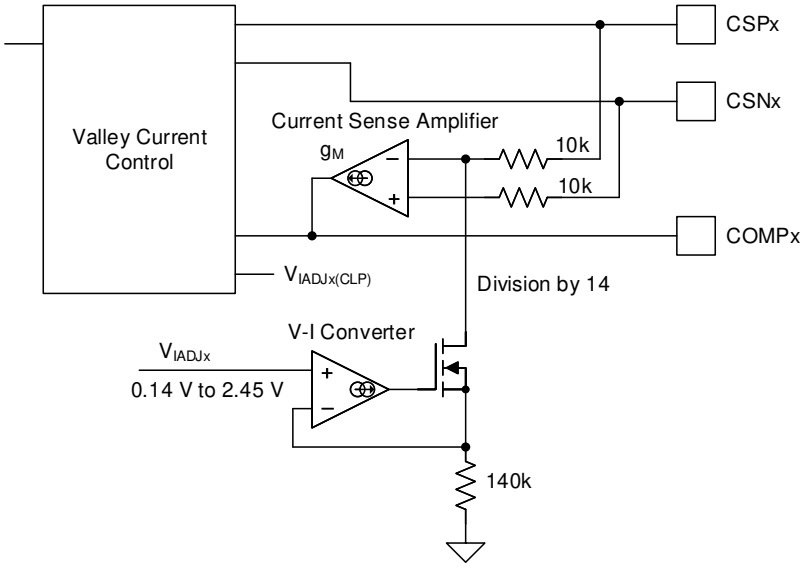


Figure 7-2. Closed-loop LED Current Regulation

LED current is dependent on the current sense resistor, R_{CS}. Use Equation 6 to calculate the LED current.

$$I_{LED} = \frac{V_{(CSP-CSN)}}{R_{CS}} = \frac{V_{IADJ}}{14 \times R_{CS}} \quad (6)$$

LED current accuracy is a function of the tolerance of the external sense resistor, R_{CS}, and the variation in the sense threshold, $V_{(CSP-CSN)}$, caused by internal mismatch and temperature dependency of the analog components. The TPS92519-Q1 is capable of achieving LED current accuracy of ±4% at full scale over common-mode range and a junction temperature range of –40°C to 150°C.

7.3.6 Start-up Sequence

The start-up circuit allows the COMP pin voltage to gradually increase, thus reducing the LED current overshoot and current surges. The switching operation is initiated after the COMP pin voltage exceeds 2.45 V. A 450-mV hysteresis window allows the device to operate when COMP voltage is within the expected operating range of 2.2 V to 2.7 V. Switching is disabled on detection of low COMP voltage to avoid excessive negative inductor current.

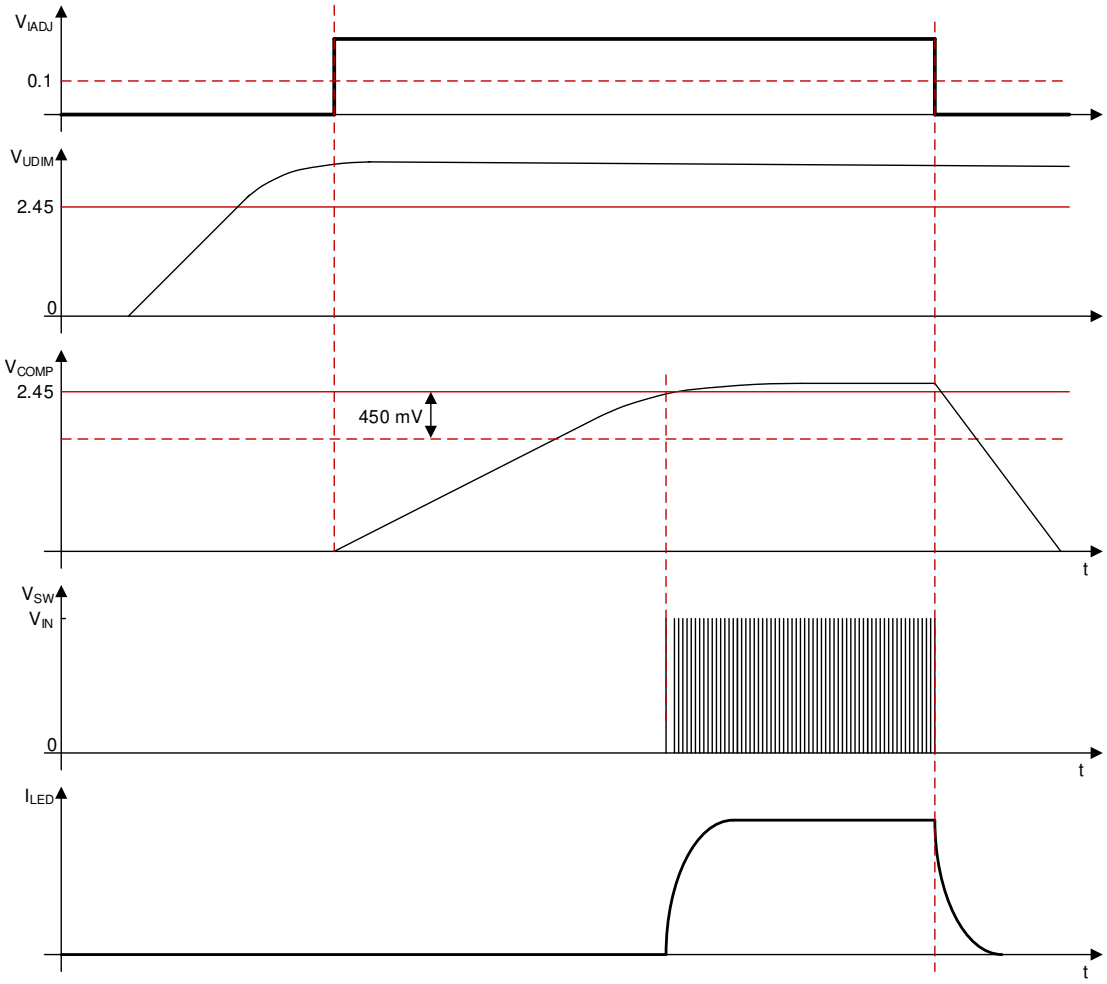


Figure 7-3. Soft-Start Sequence

The duration of soft start, t_{ss}, depends on the size of the compensation capacitor and the error amplifier source current, $I_{COMP(SRC)}$.

$$t_{SS} = \frac{2.45 \times C_{COMP}}{I_{COMP(SRC)}} \tag{7}$$

The source current, $I_{COMP(SRC)}$ is a function of the transconductance, g_M, of the error amplifier and error generated between the reference and the current sensed voltage.

$$I_{COMP(SRC)} = g_M \times \left(\frac{V_{IADJ}}{14} - V_{(CSP-CSN)} \right) \tag{8}$$

With no current flowing through the LEDs, the soft start duration depends on the choice of compensation capacitor, C_{COMP}, and the reference voltage, V_{IADJ}.

The open drain fault indicator, $\overline{FLTx}$, is set low when the COMP voltage deviates from the nominal range and exceeds $V_{COMP(OV)}$ threshold. This setting indicates a fault condition where the converter is operating in open-loop and the LED current is out of regulation. The corresponding channel can be disabled by setting IADJx input below 100 mV or controlling the UDIMx input.

7.3.7 Analog Dimming and Forced Continuous Conduction Mode

Analog dimming is accomplished by modulating the voltage connected to IADJx input. The TPS92519-Q1 improves the linear range of analog dimming by supporting forced continuous conduction mode of operation. With synchronous MOSFETs, the inductor current is allowed to go negative for part of the switching cycle, thus enabling linear dimming with over 16:1 dimming range.

7.3.8 External PWM Dimming and Input Undervoltage Lockout (UVLO)

The UDIM pin is a multi-function input that features an accurate input voltage detection based on bandgap thresholds with programmable hysteresis as shown in Figure 7-4. This pin functions as the external PWM dimming input for the LEDs and monitors VIN to detect dropout and undervoltage conditions. When the rising pin voltage exceeds the 2.45-V threshold, 10 µA (typical) of current is driven out of the UDIM pin into the resistor divider providing programmable hysteresis. TI recommends a bypass capacitor value of 1 nF between the UDIMx pin and GND to improve noise immunity.

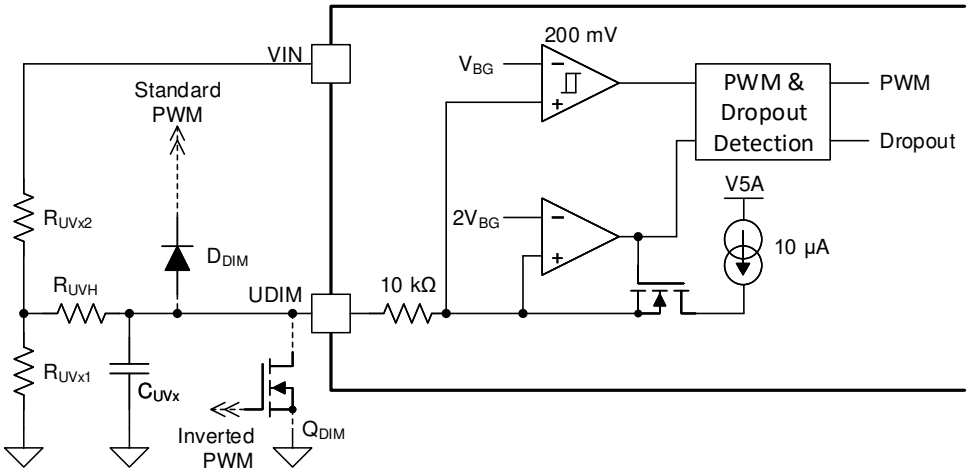


Figure 7-4. External PWM Dimming

The brightness of LEDs can be varied by modulating the duty cycle of the signal directly connected to the UDIM input. In addition, either an n-channel MOSFET or a Schottky diode can be used to couple an external PWM signal when using UDIM input in conjunction with UVLO functionality. With an n-channel MOSFET, the brightness is proportional to the negative duty cycle of the external PWM signal. With a Schottky diode, the brightness is proportional to the positive duty cycle of the external PWM signal.

Dropout and input undervoltage protection is achieved by connecting the resistor divider network from VIN to UDIM pin and UDIM pin to GND. Dropout protection is activated when UDIM pin voltage drops below $V_{UDIMx(DO,\ FALLING)}$ threshold but is held above $V_{UDIMx(EN)}$ threshold. In dropout protection mode, the device disables the error amplidier and disconnects the COMP pin to maintain charge on the compensation network. The device continues switching, ensuring fast response with minimum LED current overshoot as the converter recovers from dropout condition. The minimum input voltage, below which dropout protection is activated is programmed using Equation 9.

$$V_{INx(DO,FALL)} = V_{INx(DO,RISE)} - I_{UDIMx(DO)} \times \left(R_{UVx2} + \frac{\left(R_{UVHx} + 10 \times 10^3\right) \times \left(R_{UVx1} + R_{UVx2}\right)}{R_{UVx1}} \right) \quad (9)$$

Equation 10 shows the input voltage rising threshold. When VIN exceeds the rising threshold, the error amplifier is enabled and COMP pin is connected to compensation network to regulate LED current.

$$V_{INx(DO,RISE)} = V_{UDIMx(DO,RISE)} \times \frac{R_{UVx1} + R_{UVx2}}{R_{UVx1}} \quad (10)$$

Additional hysteresis to internal 100 mV is programmed by connecting an extra resistor, R_{UVHx}, in series with UDIM pin. This connection allows the standard resistor divider to have smaller values, minimizing PWM delays.

Input undervoltage protection is triggered when UDIM pin voltage drops below $V_{UDIMx(EN)}$ threshold. The device responds to very low VIN voltage or to the external PWM input signal by disabling the error amplifier, disconnecting the COMP pin and tri-stating the switch node. With switching disabled, inductor current and the LED current drop to zero and the charge on the compensation network is maintained. On rising edge of PWM or when VIN exceeds the internal hystersis of 200 mV, the converter resumes switching operation ramping inductor current to the previous steady-state value.

Equation 11 defines the VIN UVLO rising threshold.

$$V_{INx(UVLO,RISE)} = V_{UDIMx(EN,RISE)} \times \frac{R_{UVx1} + R_{UVx2}}{R_{UVx1}} \tag{11}$$

Use Equation 12 to determine the VIN UVLO falling threshold.

$$V_{INx(UVLO,FALL)} = V_{UDIMx(EN,FALL)} \times \left(\frac{R_{UVx1} + R_{UVx2}}{R_{UVx1}} \right) - I_{UDIMx(DO)} \times \left(R_{UVx2} + \frac{\left(R_{UVHx} + 10 \times 10^{3} \right) \times \left(R_{UVx1} + R_{UVx2} \right)}{R_{UVx1}} \right) \tag{12}$$

7.3.9 Shunt FET Dimming or Matrix Beam Application

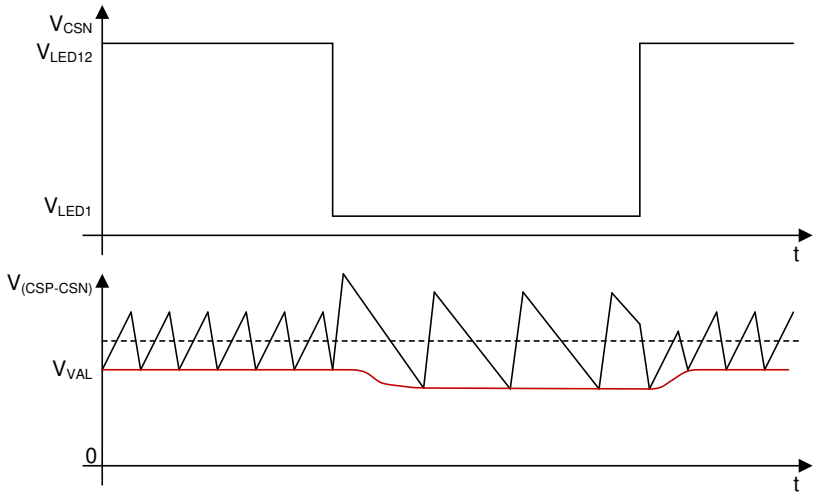


Figure 7-5. Shunt FET Dimming Transient Response

The TPS92519-Q1 is compatible with shunt FET dimming and LED Matrix Manager devices. The fast dynamic response and adaptive on-time control topology ensure near ideal current source behavior with minimum inductor current overshoot or undershoot. In contrast to constant off-time control, the control loop is able to maintain LED current regulation under shorted output condition. The off-time of the converter naturally adapts to the inductor slope and valley command while keeping the average LED current constant. Figure 7-5 shows the shunt-FET dimming transient with all LEDs switched from on to off.

The device behavior is impacted by the falling slew-rate of CSN node, V_{CSN}. A large slew-rate in conjunction with the parasitic capacitances from CSP and CSN to GND results in differential voltage forcing the converter to burst with minimum on-time and minimum off-time. To avoid switch node bursting TI recommends a maximum slew-rate (dv/dt) of 15 V/µs.

7.3.10 Bias Supply

The device is powered by an external 5-V supply connected to V5D and V5A pins. Operation is enabled when V5D and V5A exceed the 4.1-V (typical) rising threshold and is disabled when either V5D or V5A drops below the 4-V (typical) falling threshold. The comparator provides 100 mV of hysteresis to avoid chatter during

transitions. The V5D supply powers the internal digital logic and the high-side and low-side gate driver circuits. The V5A supply powers sensitive analog circuits. The two bias pins can be connected together on the PCB or through a series 10-Ω resistor between V5D and V5A with 5-V external supply connected directly to the V5D pin. TI recommends a capacitor from each pin to GND . The recommended range for the bypass capacitor from V5D pin to ground is between 1 µF and 4.7 µF. The recommended range from the V5A pin to ground is between 100 nF and 1 µF. The bypass capacitor from V5D to GND must be 10 times larger than the bootstrap capacitor, C_{BST}, to support proper operation during PWM dimming. The voltage on V5D and V5A must never exceed 5.5 V.

In device sleep state, the V5A input is internally disconnected to reduce power consumption.

7.3.11 Bootstrap Supply

The TPS92519-Q1 contains both high-side and low-side N-channel MOSFETs. The high-side gate driver works in conjunction with an internal bootstrap diode and an external bootstrap capacitor, C_{BST}. During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V and C_{BST} is charged from the V5D supply through the internal diode. TI recommends a 0.1-µF to 1-µF capacitor connected with short traces between the BST and SW pins. A larger capacitor is required to prevent a bootstrap undervoltage fault when operating at low PWM dimming frequencies.

7.3.12 Faults and Diagnostics

Table 7-1 summarizes the device behavior under fault conditions.

Table 7-1. Fault Description

FAULT	DETECTION	DESCRIPTION
Thermal protection	T_J > 175°C	Each channel is protected by an individual thermal sensor located close to the switching MOSFETs. The thermal protection is activated in the event the maximum MOSFET temperature exceeds the typical value of 175°C. The corresponding channel is forced into shutdown mode. This feature is designed to prevent overheating and damage to the internal switching MOSFETs.
V5D undervoltage lockout	$V_{5D(RISE)}$ < 4.1 V $V_{5D(FALL)}$ > 4 V	The device enters the Undervoltage Lockout (UVLO). The switching operation is disabled, the COMP capacitor is discharged.
V5A undervoltage lockout	$V_{5A(RISE)}$ < 4.1 V $V_{5A(FALL)}$ > 4 V	In sleep mode, the internal V5A node is disconnected to reduce the current consumption. The switching operation is disabled and the COMP capacitor is discharged.
VINx dropout protection	V_{UDIMx} < 2.35 V	The device disables error amplifier and disconnects the compensation network for the corresponding channel. Error amplifier is enabled and compensation network is internally connected when the input voltage rises above the dropout rising threshold, $V_{INx(DO,RISE)}$.
VINx undervoltage lockout	V_{UDIMx} < 1.02 V	The device disables switching operation for the corresponding channel. Switching is enabled when the input voltage rises above the turn-on threshold, $V_{INx(UVLO,RISE)}$.
BSTx undervoltage lockout	$V_{BSTx(RISE)}$ > 3.14 V $V_{BSTx(FALL)}$ < 2.95 V	The device turns off the high-side MOSFET and turns on the low-side MOSFET for the corresponding channel. Normal switching operation is resumed after the bootstrap voltage exceeds 3.14 V.
COMPx overvoltage	V_{COMPx} > 3.2 V	The $\overline{FLTx}$ flag is set low to indicate that the COMP voltage exceeded the normal operating range. This condition indicates output open circuit fault.
Short CHx output	V_{CSNx} < 2.45 V	The $\overline{FLTx}$ flag is set low to indicate an output short circuit condition based on sensed CSNx voltage.
High-side switch current limit	I_{HS} > 3.5 A	The device turns off the high-side MOSFET and discharges the COMP capacitor when the drain current exceeds 3.5-A typical. The low-side switch is turned on to discharge the inductor and output capacitor. The device attempts to restart after delay of 3.6 ms
Low-side switch current limit	I_{LS} > 2.5 A	The device turns off both high-side and low-side MOSFETs and discharges the COMP capacitor when the drain current exceeds 2.5 A typical. The device attempts to restart after delay of 3.6 ms.

The TPS92519-Q1 triggers an auto-restart on detection of the thermal shutdown, high-side, or low-side current limit faults. In the case of thermal shutdown fault, the restart is initiated after the MOSFET temperature decreases by the fixed hysteresis of 10°C. A soft-start sequence is initiated and switching operation is enabled.

For a high-side or low-side current limit fault, a fixed 3.6-ms timer is initiated on detection of the fault. A restart is initiated by the expiration of the fault timer and switching operation is enabled.

The output open circuit and short circuit faults force the $\overline{FLTx}$ pin low when biased through an external resistor and connected to a 5-V supply. The $\overline{FLTx}$ output can be used in conjunction with a microcontroller or system basis chip (SBC) as an interrupt and can be used to aid in fault diagnostics.

Table 7-2. Faults and Diagnostic Summary

LIST	DESCRIPTION	FAULT OR DIAGNOSTIC	ENABLE FAULT TIMER	$\overline{FLT}$ INDICATION
	Thermal protection	Fault	No	No
$VINx_{(DO)}$	VIN supply dropout protection	Diagnostics	No	No
$VINx_{(UVLO)}$	VIN supply undervoltage lockout	Fault	No	No
CHxBSTUV	BST supply undervoltage lockout	Fault	No	No
CHxCOMPOV	COMP overvoltage	Diagnostics	No	Yes
CHxSHORT	Short circuit detected	Diagnostics	No	Yes
CHxHSILIM	High-side current limit	Fault	Yes	No
CHxLSILIM	Low-side current limit	Fault	Yes	No
V5AUV	V5A undervoltage	Diagnostics	No	No

7.3.13 Output Short Circuit Fault

The TPS92519-Q1 monitors the CSNx voltage to detect output short circuit faults. A short failure is indicated when the CSNx voltage drops below 1.5 V. The corresponding is $\overline{FLTx}$ flag is set low. The device continues to regulate current and operate without interruption in case of short circuit.

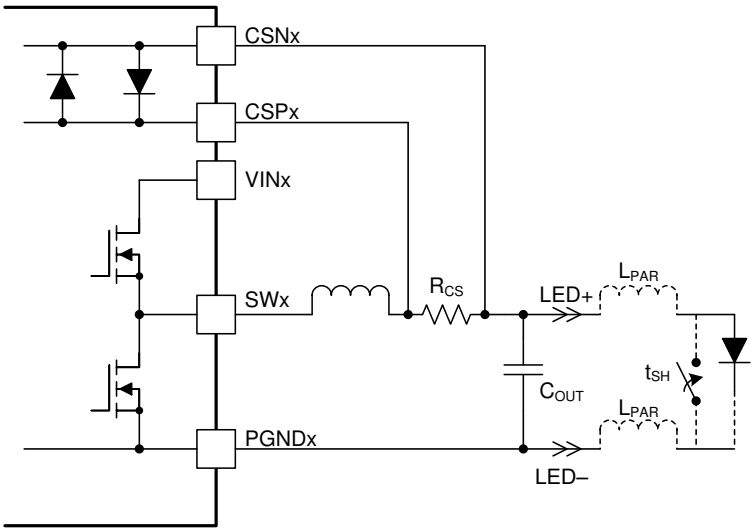


Figure 7-6. Cable Harness Parasitic Inductance

The voltage transient imposed on CSPx and CSNx inputs during short circuit is dependent on the output capacitance and is influenced by the cable harness impedance. The inductance associated with a long cable harness resonates with the charge stored on the output capacitor and forces CSPx and CSNx voltage to ring below ground. The negative voltage and current are dependent on the parasitic cable harness inductance and resistance.

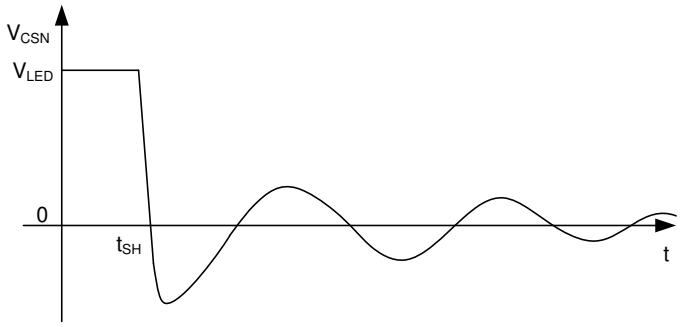


Figure 7-7. Short Circuit Fault Transient Behavior

When using a long cable harness, TI recommends a diode to clamp the negative voltage across CSPx and CSNx input, as shown in Figure 7-8. TI recommends a low forward voltage Schottky diode or a fast recovery silicon diode with reverse blocking voltage rating greater than the maximum output voltage. The diode is required to be placed close to the output capacitor and must ensure that the current flowing through CSP and CSN nodes under negative transient condition is below the absolute maximum rating of the device.

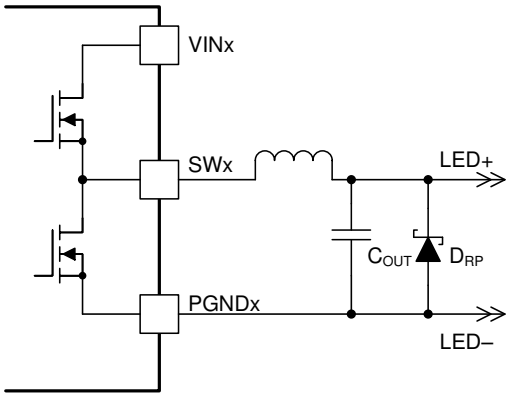


Figure 7-8. CSP and CSN Transient Protection Using an External Diode

7.3.14 Output Open Circuit Fault

An LED open circuit fault ultimately causes the output voltage to increase and settle close to the input voltage. When this occurs, the TPS92519-Q1 switching operation is then controlled by the fixed on-time and minimum off-time resulting in a duty cycle close to 100%. Under this condition, COMP voltage exceeds $V_{COMPx(OV)}$ threshold forcing $\overline{FLTx}$ flag low.

The dynamic behavior of the device and buck converter is influenced by the input voltage, V_{IN}, and the output capacitor, C_{OUT}, value. The device response to open circuit can be categorized into the following three distinct cases.

Case 1: For a Buck converter design with a small output capacitor, the switching operation in open load condition excites the inductor and the output capacitor resonance, forcing the output voltage to oscillate. The frequency and amplitude of the oscillation are based on the resonant frequency and Q-factor of the tank.

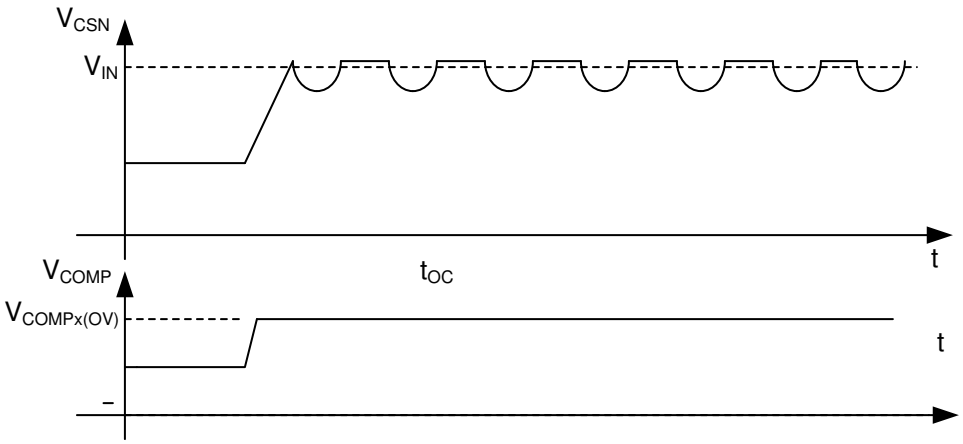


Figure 7-9. Open Circuit Condition With Output Voltage Oscillation

Case 2: For a buck converter design with larger output capacitor, the inductor Q-factor and resonant frequency are much lower than the switching frequency. In this case, output voltage rises to input voltage and the converter continues to switch with minimum off-time.

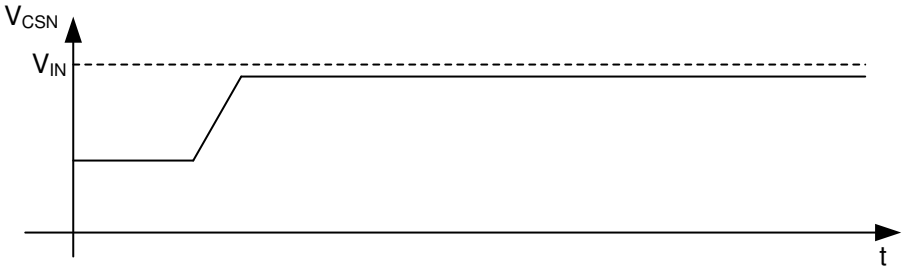


Figure 7-10. Open Circuit Condition With Minimum Off-time Operation

7.3.15 Parallel Operation

The adaptive on-time control technique enables parallel operation of two or more channels with independent current sharing and regulation. Each channel operates independently and delivers current based on the corresponding IADJx set point. To equally share current amongst channels, the IADJx for all channels must be connected to the external reference voltage.

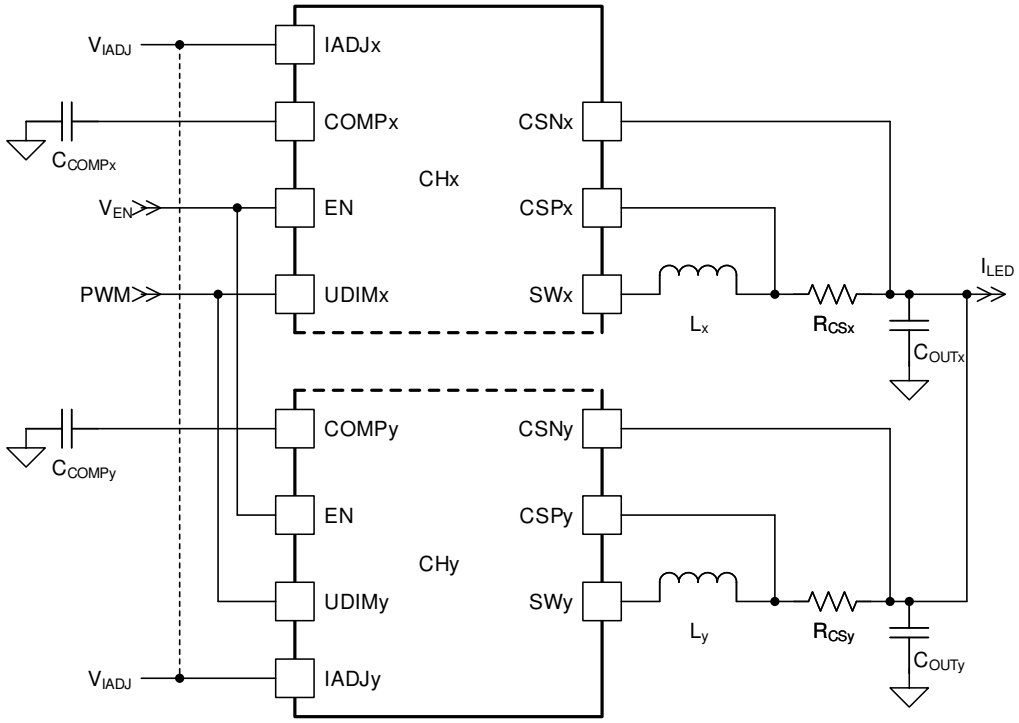


Figure 7-11. Parallel Channel Configuration

Startup requires all channels to be enabled simultaneously by synchronizing the rising edge of IADJx voltage above $V_{IADJx(SD)}$ rising threshold. This simultaneous enabling ensures that the soft-start ramp is synchronized and current sharing is achieved after COMP voltage increases above the rising startup threshold, $V_{COMPx(ST)}$.

PWM dimming is achieved by connecting the external PWM signal to UDIMx pin of all parallel channels. All parallel channels have to be controlled by single PWM dimming reference. TI does not recommend to PWM dim individual parallel channels.

Additional considerations are necessary to account for bootstrap capacitor tolerance and the impact of the capacitor variation when PWM dimming multiple parallel channels. Ensure that bootstrap capacitor voltage is above the undervoltage threshold, $V_{BSTx(UV)}$ for all operating conditions. For application requiring very low PWM duty cycle or low PWM dimming frequency, TI recommends to connect the COMPx pin of all parallel channels using nonparallel diodes, as shown in Figure 7-12. This connection allows the parallel channels to respond and recovery from bootstrap undervoltage fault when operating at low PWM dimming duty cycles.

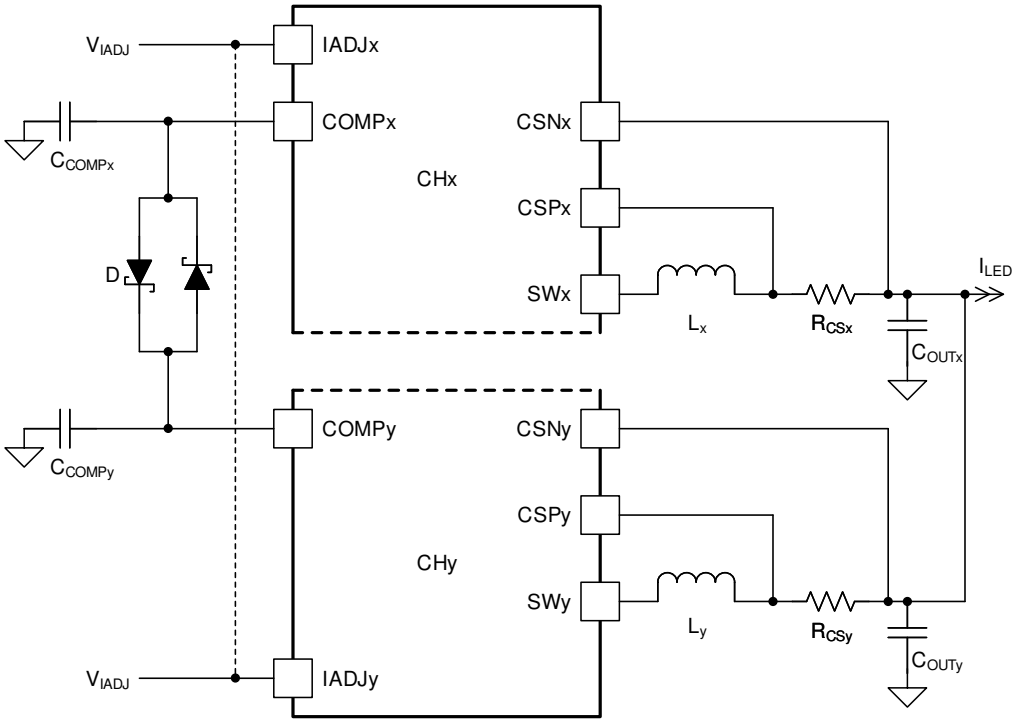


Figure 7-12. Parallel Channel Configuration for PWM Dimming Operation

7.4 Device Functional Modes

The device has three functional modes: Power On Reset (POR) state, run mode and sleep mode.

7.4.1 Power On Reset (POR)

The device is in POR state when V5A or V5D input is below the undervoltage lockout threshold. In POR, both channels are turned off. The device exits POR and enters functional modes when the V5D supply exceeds 4.1 V (typical).

7.4.2 Run Mode

The device advances to run mode EN input is set high. In this mode, all the necessary conditions for initiating the soft-start sequence are checked. If a fault occurs in this state, the device attempts to resume operation after waiting for the fault timer to timeout.

Transition to sleep mode is by pulling EN input low. This action causes the device to enter a low-power state.

7.4.3 Sleep Mode

In sleep mode, the following occurs:

1. The internal regulators are disconnected from the V5A pin.
2. The oscillator is disabled.
3. The channels are disabled.
4. The high side and low side MOSFETs are turned off.

In sleep mode, the output voltage rises above 3 V as all internal loads are switched off and the leakage current associated with high-side gate drive is forced through the switch node, SWx.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Figure 8-1 shows a schematic of a typical application for the TPS92519-Q1.

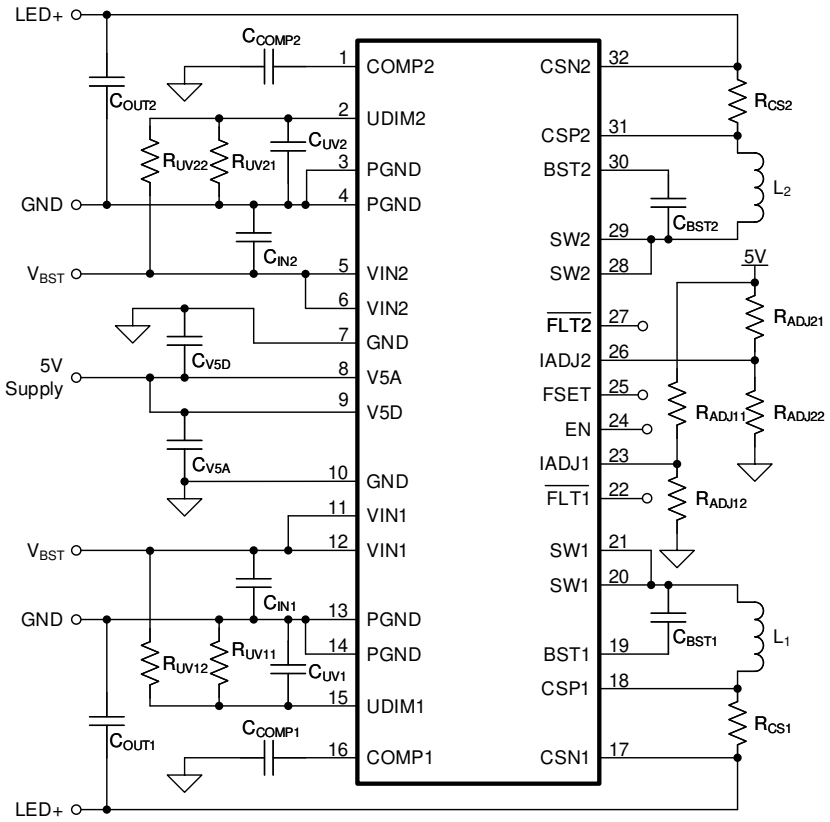


Figure 8-1. Buck LED Driver

8.1.1 Duty Cycle Consideration

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is defined using Equation 13:

$$D = \frac{V_{CSN}}{V_{IN}} \tag{13}$$

There is no limitation for small duty cycles, because at low duty cycles, the switching frequency is reduced as needed to always ensure current regulation. The maximum duty cycle attainable is limited by the minimum off-time duration and is a function of switching frequency.

8.1.2 Switching Frequency Selection

Nominal switching frequency (t_{ON} > $t_{ON(MIN)}$) is set by input voltage, V_{IN}, output voltage, V_{CSP} and the FSET pin. The switching varies slightly over operating range and temperature based on converter efficiency. Table 8-1 shows the nominal switching frequency for channel 1 and channel 2 based on FSET pin setting.

Table 8-1. Frequency Setting

FSET	CHANNEL	FREQUENCY
V_{FSET} > 1.8 V	Channel 1	384 kHz
	Channel 2	438 kHz
V_{FSET} < 0.8 V	Channel 1	2.04 MHz
	Channel 2	2.14 MHz

8.1.3 LED Current Set Point

The LED current is set by the external resistor, R_{CS}, and the IADJx pin. The current sense resistor, R_{CS}, is selected to meet the maximum LED current specification and 90% of the full-scale range of IADJx clamp voltage.

$$R_{CS} = \frac{0.9 \times V_{IADJx(CLP)}}{14 \times I_{LEDx(MAX)}} \tag{14}$$

The LED current can be varied between minimum and maximum specified limits by modulating the voltage on IADJx pin.

8.1.4 Inductor Selection

The inductor is sized to meet the ripple specification at 50% duty cycle. TI recommends a minimum of 30% peak-to-peak inductor ripple to ensure periodic switching operation. Use Equation 15 to calculate the inductor value.

$$L = \frac{V_{IN(TYP)}}{4 \times \Delta i_L \times f_{SW}} \tag{15}$$

Use Equation 16 and Equation 17 to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$i_{L(RMS)} = \sqrt{\left(I^2_{LED(MAX)} + \frac{\Delta i^2_{L(MAX)}}{12} \right)} \tag{16}$$

$$i_{L(PK)} = I_{LED(MAX)} + \frac{\Delta i_{L(MAX)}}{2} \tag{17}$$

8.1.5 Output Capacitor Selection

The output capacitor value depends on the total series resistance of the LED string, r_D, and the switching frequency, f_{SW}. Equation 18 calculates the capacitance required for the target LED ripple current.

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED}} \tag{18}$$

For applications where the converter supports pixel beam or matrix LED loads, additional design considerations influence the selection of output capacitor. The size of the output capacitor depends on the slew-rate control of the LED bypass switches and must be carefully selected while considering the overshoot current created by the dv/dt of the bypass switch.

When choosing the output capacitors, it is important to consider the ESR and ESL characteristics because they directly impact the LED current ripple. Ceramic capacitors are the best choice due to the following:

- Low ESR
- High ripple current rating
- Long lifetime
- Good temperature performance

With ceramic capacitor technology, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with a voltage rating greater than maximum LED stack voltage.

8.1.6 Input Capacitor Selection

The input capacitor buffers the input voltage for transient events and decouples the converter from the supply. TI recommends a 2.2-µF input capacitor across the VIN pin and PGND placed close to the device, and connected using wide traces. X7R-rated ceramic capacitors are the best choice due to the low ESR, high ripple current rating, and good temperature performance. Additional capacitance can be required to further limit the input voltage deviation during PWM dimming operation.

8.1.7 Bootstrap Capacitor Selection

The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. The required capacitance depends on the PWM dimming frequency, PWM_{FREQ}, and is sized to avoid boot undervoltage and fault during PWM dimming operation. Equation 19 calculates the bootstrap capacitance, C_{BST}.

$$C_{BST} = \frac{I_{Q(BST)}}{\left(V_{5D} + V_{BST(HYS)} - V_{BST(UV)}\right) \times PWM_{FREQ}} \quad (19)$$

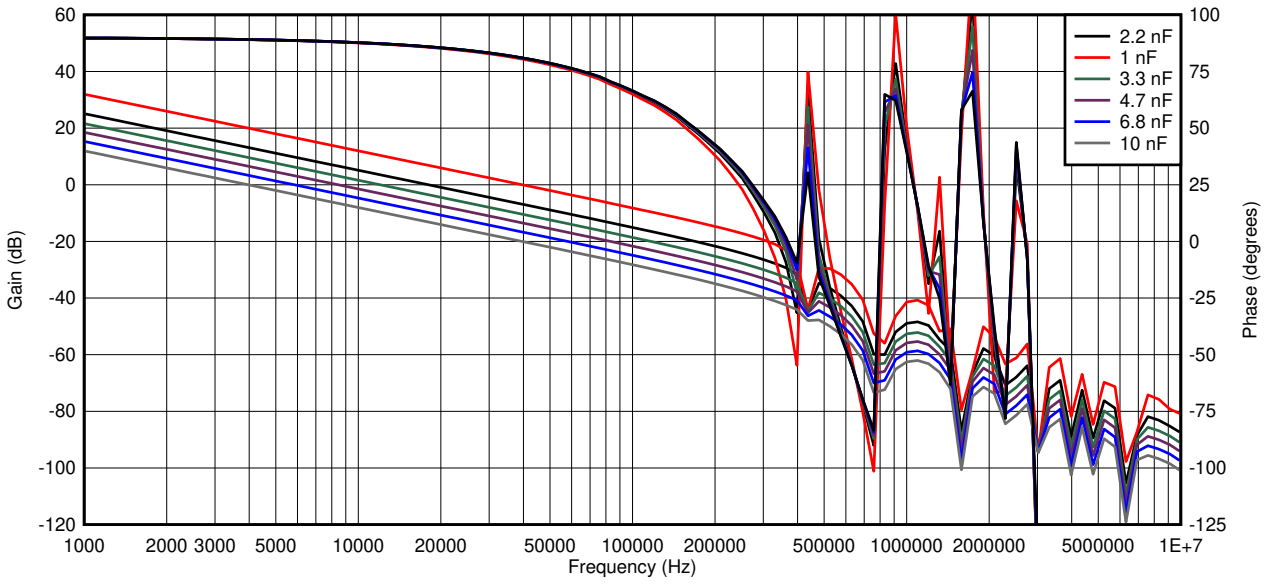
Table 8-2 summarizes the TI recommended bootstrap capacitor value for different PWM dimming frequencies.

Table 8-2. Bootstrap Capacitor Value

PWM DIMMING FREQUENCY (Hz)	BOOTSTRAP CAPACITOR (µF)
1507	0.1
1318	0.15
1055	0.22
879	0.22
659	0.33
439	0.47
215	1
108	2

8.1.8 Compensation Capacitor Selection

A simple integral compensator is recommended to achieve stable operation across the wide operating range. The bode plot of the loop gain with different compensation capacitors is shown in Figure 8-2. The buck converter behaves as a single pole system with additional phase lag caused by the switching behavior. The gain and phase margin is then determined by the choice of the switching frequency and is independent of other design parameters. TI recommends a 1-nF to 10-nF capacitor to achieve bandwidth between 4 kHz and 40 kHz. The choice of compensation capacitor impacts the transient response, the shunt FET dimming behavior and PWM dimming performance. A larger compensation capacitor (lower bandwidth) is recommended to limit the LED current overshoot on the rising edge of internal or external PWM signal. A smaller compensation capacitor (higher bandwidth) is recommend to improve shunt FET dimming response.



L = 68 µH, f_{SW} = 438 kHz

Figure 8-2. Simulated Bode Plot of Loop Gain

8.1.9 Input Undervoltage Protection

Figure 8-1 shows that the undervoltage protection threshold is programmed using a resistor divider, R_{UV1} and R_{UV2}, from the input voltage, V_{IN}, to ground. Use Equation 20 and Equation 21 to calculate the resistor values.

$$R_{UVx2} = \frac{2 \times V_{INx(UVLO,RISE)}}{I_{UDIMx(HYS)}} - \frac{V_{INx(DO,FALL)}}{I_{UDIMx(HYS)}} - 10 \times 10^{3} \quad (20)$$

$$R_{UVx1} = \frac{V_{UDIMx(EN,RISE)}}{V_{INx(UVLO,RISE)} - V_{UDIM(EN,RISE)}} \times R_{UVx2} \quad (21)$$

8.1.10 CSN Protection Diode

An external Schottky diode is selected to protect the CSP / CSN node by clamping the negative voltage during short circuit transient. The Schottky diode must be selected based on the length of the cable harness and the choice of output capacitor. TI recommends a Schottky diode with low forward voltage drop at room-temperature and non-repetitive peak surge current rating of 10 A for duration of 5 µs. The diode must be located close to the CSN pin.

8.2 Typical Application

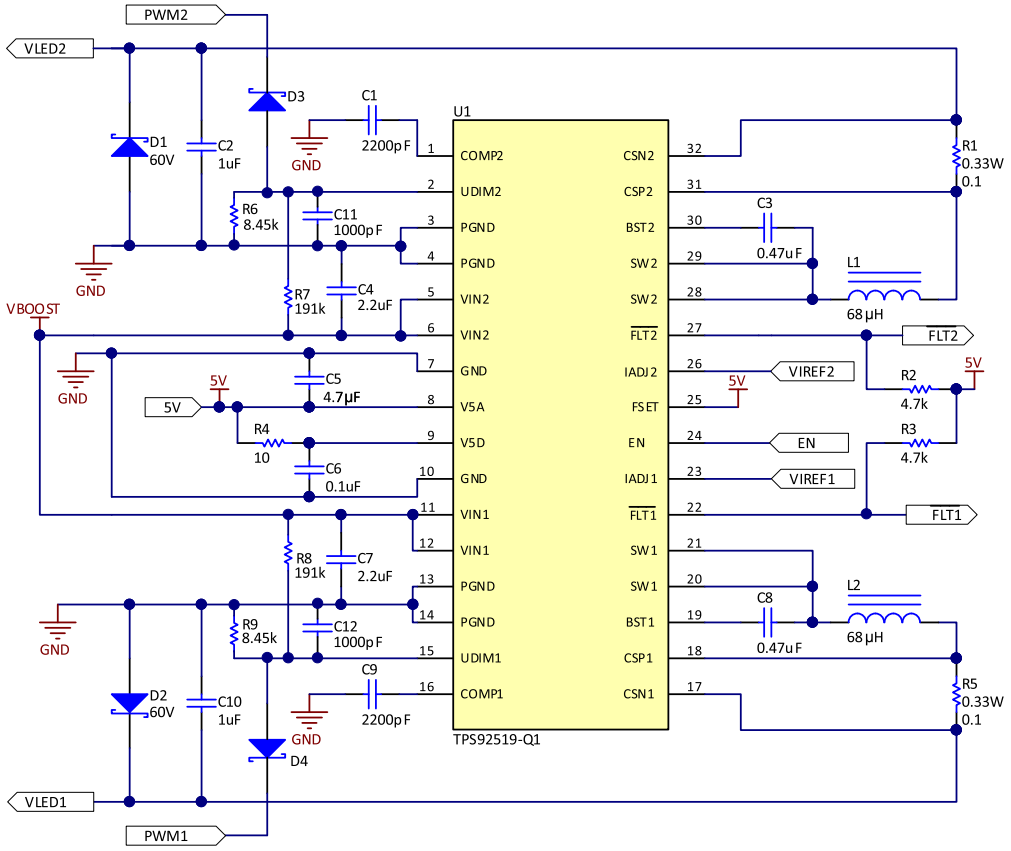


Figure 8-3. Application Schematic

8.2.1 Design Requirements

Table 8-3. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		58	60	62	V
$V_{IN(DO)}$	Dropout protection threshold	Falling		55		V
N_S	Number of LEDs		1		16	
V_{FLED}	LED forward voltage drop		2.8	3	3.4	V
r_D	LED string series resistance	$N \times r_{D(LED)}$	0.1		1.6	Ω
V_{OUT}	Output voltage	$Ns \times V_{FLED}$	2.8		54.4	V
I_{LED}	LED current		100		1600	mA
Δi_{LED}	LED current ripple	Defined as percentage peak-to-peak at maximum LED current. 5 % of maximum LED current.			80	mA
Δi_L	Inductor current ripple	Defined as percentage peak-to-peak at maximum LED current		30		%
$V_{IN(UVLO,RISE)}$	Start input voltage	Input voltage rising		28.5		V
$V_{IN(UVLO,HYS)}$	Input voltage undervoltage lockout hysteresis			5		V
f_{PWM}	PWM frequency			439		Hz
D_{PWM}	PWM dimming duty cycle		4		100	%
V_{SW}	Switching frequency			438		kHz
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Calculating Duty Cycle

Solve for duty cycle D, D_{MAX}, and D_{MIN}:

$$D_{MAX} = \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} = \frac{54.4}{58} = 0.938 \quad (22)$$

$$D_{MIN} = \frac{V_{OUT(MIN)}}{V_{IN(MAX)}} = \frac{2.8}{62} = 0.0452 \quad (23)$$

8.2.2.2 Calculating Minimum On-Time and Off-Time

Solve for minimum on-time, $t_{ON(DMIN)}$ at minimum duty cycle and maximum on-time, $t_{ON(DMAX)}$ at maximum duty cycle:

$$t_{ON(DMIN)} = \frac{V_{OUT(MIN)}}{V_{IN(MAX)}} \times \frac{1}{f_{SW}} = \frac{2.8}{62} \times \frac{1}{438 \times 10^3} = 103.1 \times 10^{-9} \quad (24)$$

$$t_{ON(DMAX)} = \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} \times \frac{1}{f_{SW}} = \frac{54.4}{58} \times \frac{1}{438 \times 10^3} = 2.141 \times 10^{-6} \quad (25)$$

8.2.2.3 Minimum Switching Frequency

Confirm minimum switching frequency at $t_{ON(DMIN)}$, $f_{SW(MIN)}$:

$$f_{SW(MIN)} = \frac{V_{OUT(MIN)}}{t_{ON(DMIN)} \times V_{IN(MAX)}} = \frac{2.8}{103.1 \times 10^{-9} \times 62} = 438 \times 10^3 \quad (26)$$

For the design specification, $t_{ON(DMIN)} > t_{ON(MIN)}$ and $f_{SW(MIN)} = f_{SW}$.

8.2.2.4 LED Current Set Point

Solve for sense resistor, R_{CS}:

$$R_{CS} = \frac{0.9 \times V_{IADJ(CLP)}}{14 \times I_{LED(MAX)}} = \frac{0.9 \times 2.45}{14 \times 1.6} = 0.0984 \quad (27)$$

A standard resistor of 100 mΩ with tolerance better than 1 % and low temperature coefficient is selected.

8.2.2.5 Inductor Selection

The inductor is selected to meet the recommended 30% peak-to-peak inductor ripple specification:

$$L = \frac{V_{IN(TYP)}}{4 \times \Delta i_L \times f_{SW}} = \frac{V_{IN(TYP)}}{4 \times 0.3 \times I_{LED(MAX)} \times f_{SW}} = \frac{60}{4 \times 0.3 \times 1.6 \times 438x10^3} = 71.3 \times 10^{-6} \quad (28)$$

The closest standard capacitor is 68 µH.

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost at the expense of reduced efficiency and larger output capacitor.
- Higher inductance values decrease the peak-to-peak inductor current, which increases efficiency but reduces the operating range based on minimum sense voltage ripple, $\Delta V_{(CSP-CSN)}$ specification.

8.2.2.6 Output Capacitor Selection

The minimum output capacitance is selected to meet the LED current ripple specification:

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_{D(MAX)} \times \Delta i_{LED(MAX)}} = \frac{0.48}{8 \times 438 \times 10^{3} \times 1.6 \times 80 \times 10^{-3}} = 1.07 \times 10^{-6} \quad (29)$$

A standard 1-µF, 100-V X7R capacitor is selected.

8.2.2.7 Bootstrap Capacitor Selection

Referring to Table 8-2, a standard 470-nF, 16-V X7R capacitor is selected to support PWM frequency of 439 Hz.

8.2.2.8 Compensation Capacitor Selection

A compensation capacitor of 2.2 nF is selected to achieve balanced transient response between PWM dimming and shunt FET dimming.

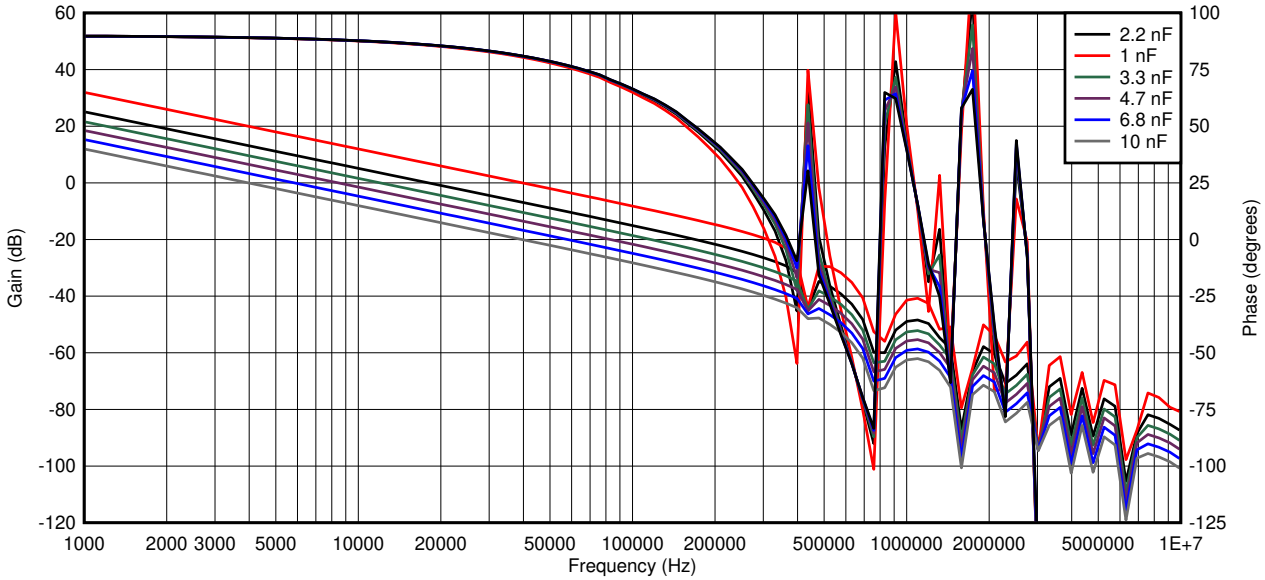


Figure 8-4. Simulated Buck Converter Bode Plot

8.2.2.9 PWM Dimming and Input Voltage Protection

The device channel enable function and external PWM signal is achieved by controlling UDIM input. The device modulates the LED current based on the PWM duty cycle of the external signal.

Input undervoltage lockout function is implemented by selecting R_{UV1} and R_{UV2} resistor along with internal hysteresis.

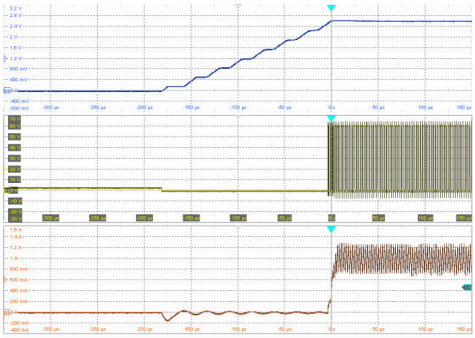
$$R_{UV2} = \frac{2 \times V_{IN(UVLO,RISE)}}{I_{UDIM(DO)}} - \frac{V_{IN(DO,FALL)}}{I_{UDIM(DO)}} - 10 \times 10^{3} = \frac{2 \times 28.5}{10 \times 10^{-6}} - \frac{55}{10 \times 10^{-6}} - 10 \times 10^{3} = 190 \times 10^{3} \quad (30)$$

A standard 191-kΩ resistor is selected for R_{UV2}.

$$R_{UV1} = \frac{V_{UDIM(EN,RISE)}}{V_{IN(UVLO,RISE)} - V_{UDIM(EN,RISE)}} \times R_{UV2} = \frac{1.22}{28.5 - 1.22} \times 191 \times 10^{3} = 8.54 \times 10^{3} \quad (31)$$

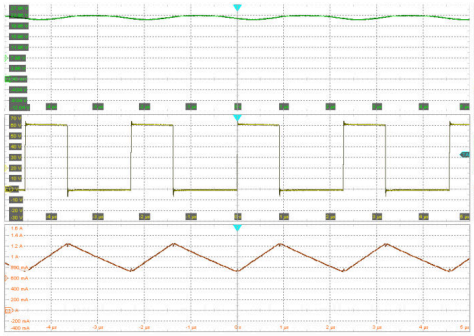
A standard 8.45-kΩ resistor is selected for R_{UV1}.

8.2.3 Application Curves



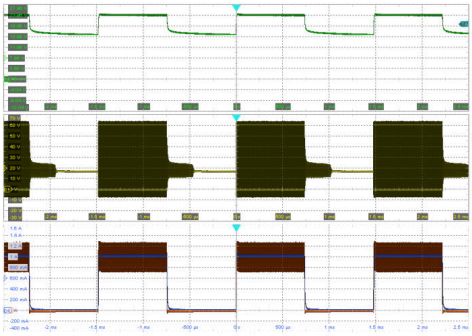
Ch1: SW voltage (10 V/div); Ch3: Inductor current (200 mA/div); Ch4: COMP voltage (400 mV/div); Time: 50 µs/div

Figure 8-5. Start-up Transient



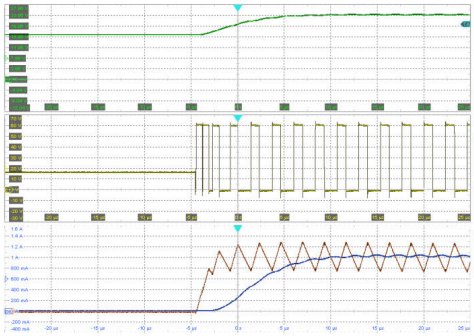
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Time: 1 µs/div

Figure 8-6. Normal Operation



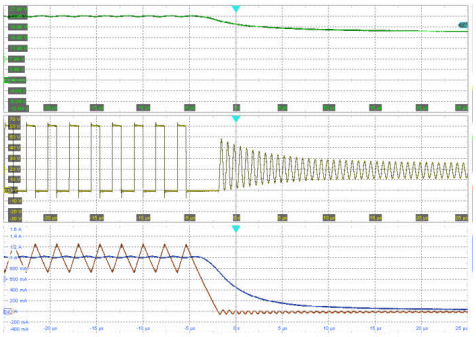
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 500 µs/div

Figure 8-7. PWM Dimming Transient



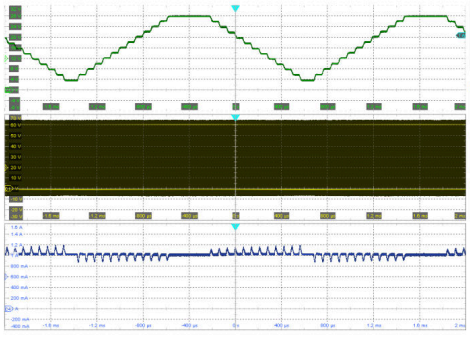
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 5 µs/div

Figure 8-8. PWM Dimming (Rising Edge)



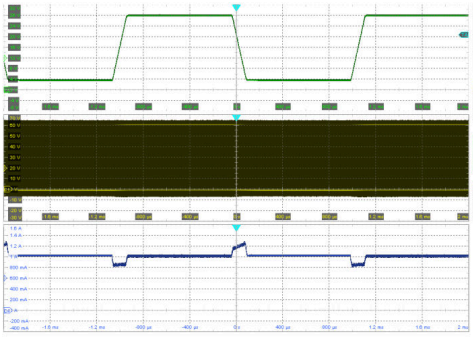
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 5 µs/div

Figure 8-9. PWM Dimming (Falling Edge)



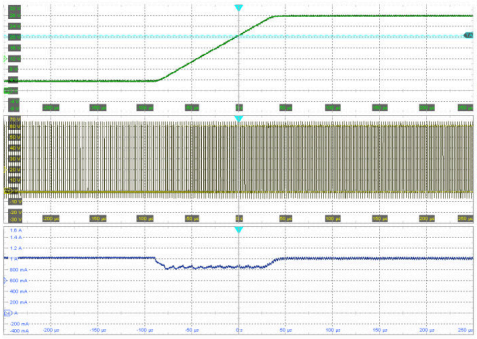
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 400 µs/div

Figure 8-10. Shunt Dimming With Matrix Manager



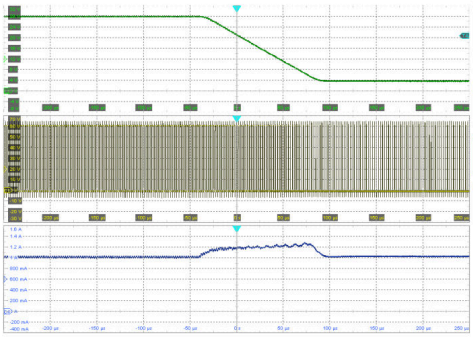
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 400 µs/div

Figure 8-11. Shunt Dimming (LEDs ON-OFF Transient)



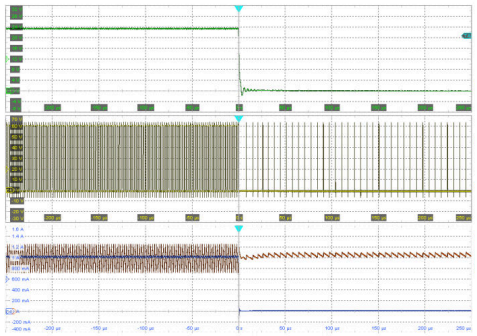
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 50 µs/div

Figure 8-12. Shunt Dimming (LEDs OFF to LEDs ON)



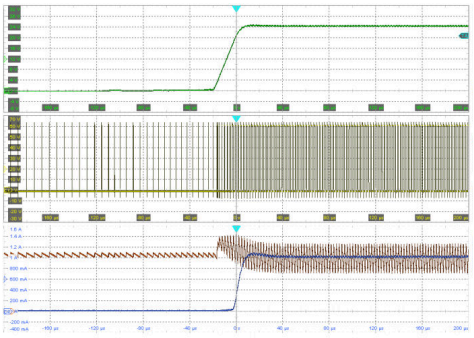
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 50 µs/div

Figure 8-13. Shunt Dimming (LEDs ON to LEDs OFF)



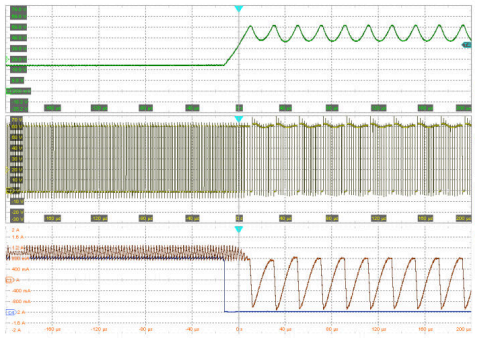
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 50 µs/div

Figure 8-14. Output Short Circuit Fault



Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 40 µs/div

Figure 8-15. Output Short Circuit Fault Recovery



Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (400 mA/div); Ch4: LED current (200 mA/div); Time: 40 µs/div

Figure 8-16. Output Open Circuit Fault

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 V and 65 V. The input can be a car battery or another preregulated power supply. Additional bulk capacitance or an input filter can be required in addition to the ceramic bypass capacitors to address converter stability, noise, and EMI concerns.

10 Layout

10.1 Layout Guidelines

The performance of any switching converter depends as much on the layout of the PCB as the component selection. The following guidelines can help you design a PCB with the best power converter performance:

- Place ceramic high-frequency bypass capacitors as close as possible to the TPS92519-Q1 VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pins.
- Place bypass capacitors for V5D and V5A close to the pins and ground the capacitors to device ground.
- Differentially route the CSP and CSN pins to sense resistor. Route the traces away from noisy nodes, preferably through a layer on the other side of a shielding or ground layer.
- Use ground plane in one of the middle layers for noise shielding.
- Make VIN and ground connection as wide as possible. This action reduces any voltage drops on the input of the converter and maximizes efficiency.

10.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt from pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of the path. In buck converters, the pulsing current path is from the VIN side of the input capacitors through the HS switch, through the LS switch, and then returns to the ground of the input capacitor.

High-frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic capacitors as close as possible to the VIN and PGND pins is the key to EMI reduction.

The PCB copper connection of the SW pin to the inductor must be as short as possible and just wide enough to carry the LED current without excessive heating. Short, thick traces or, copper pours (shapes), must be used for high current conduction path to minimize parasitic resistance. Place the output capacitor close to the CSN pin and grounded closely to the PGND pin.

10.1.1.1 Ground Plane

TI recommends using one of the middle layers as a solid ground plane. The ground plane provides shielding for sensitive circuits and traces. The ground plane also provides a quiet reference potential for the control circuitry. Connect the GND and PGND pins to the ground plane using vias right next to the bypass capacitors. PGND pins are connected to the source of the internal LS switch. The pins must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations.

10.2 Layout Example

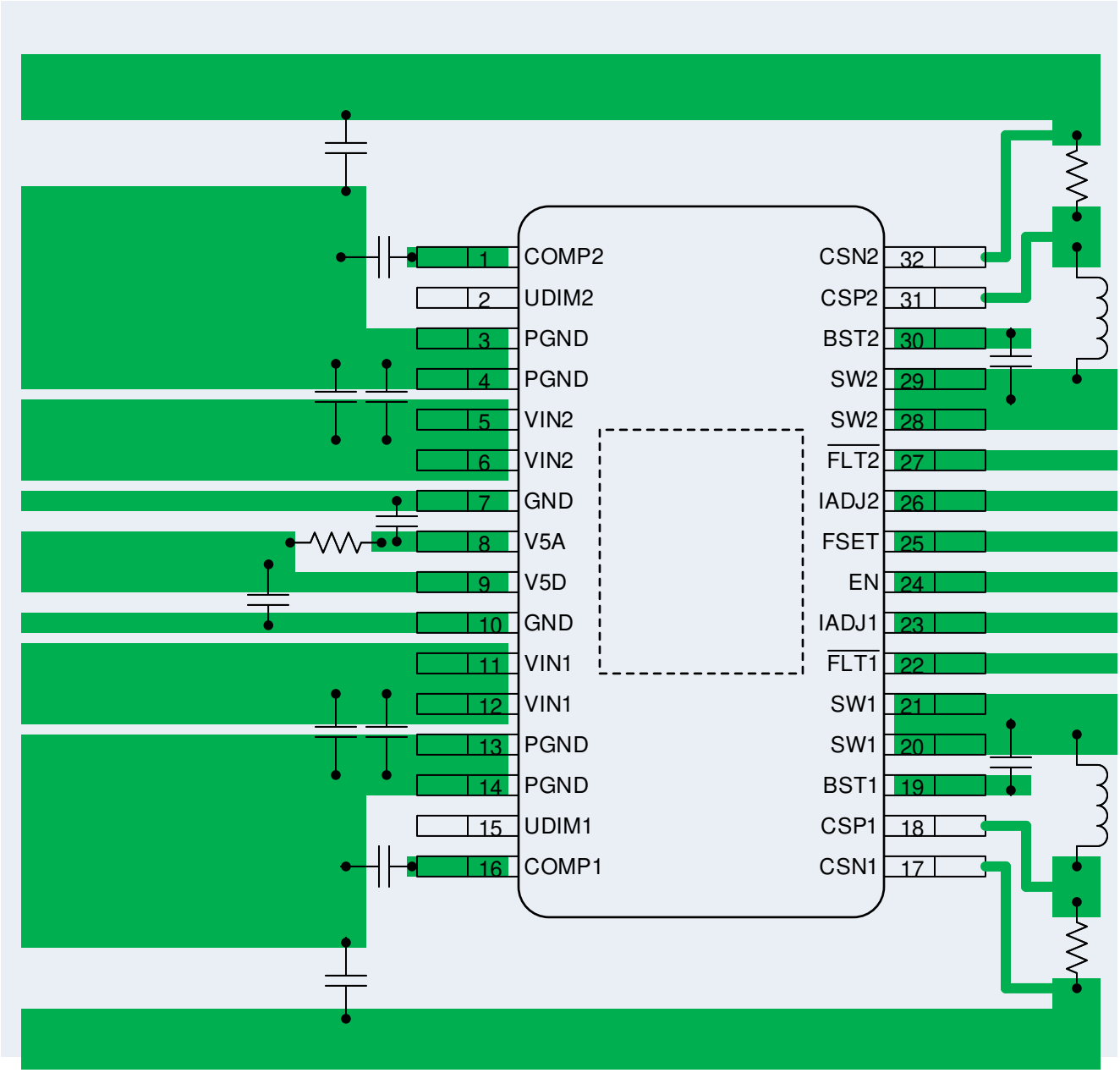


Figure 10-1. TPS92519-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS92519-Q1 Evaluation Module User's Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92519QDAPRQ1	ACTIVE	HTSSOP	DAP	32	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	125 to -40	92519Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

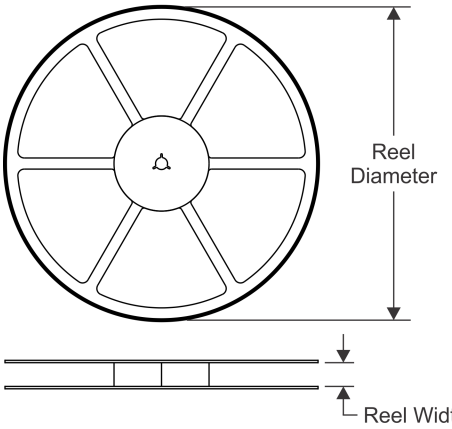
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

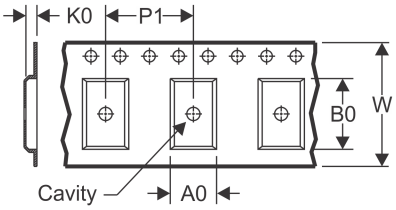
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

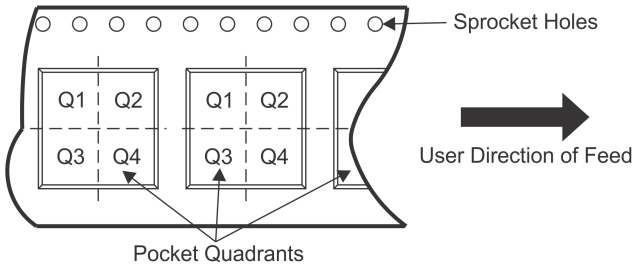


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

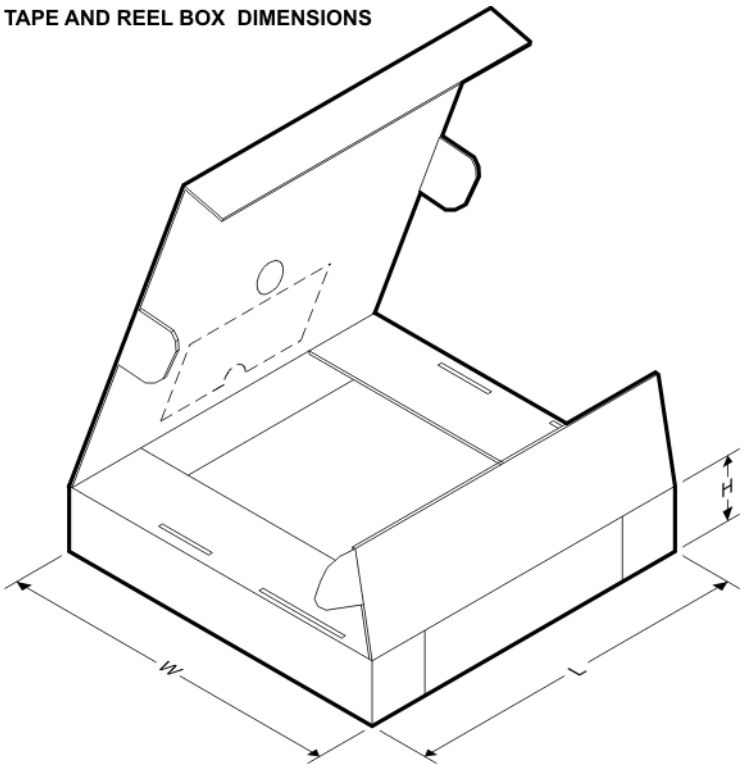
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92519QDAPRQ1	HTSSOP	DAP	32	2500	330.0	24.4	8.8	11.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92519QDAPRQ1	HTSSOP	DAP	32	2500	367.0	367.0	45.0

GENERIC PACKAGE VIEW

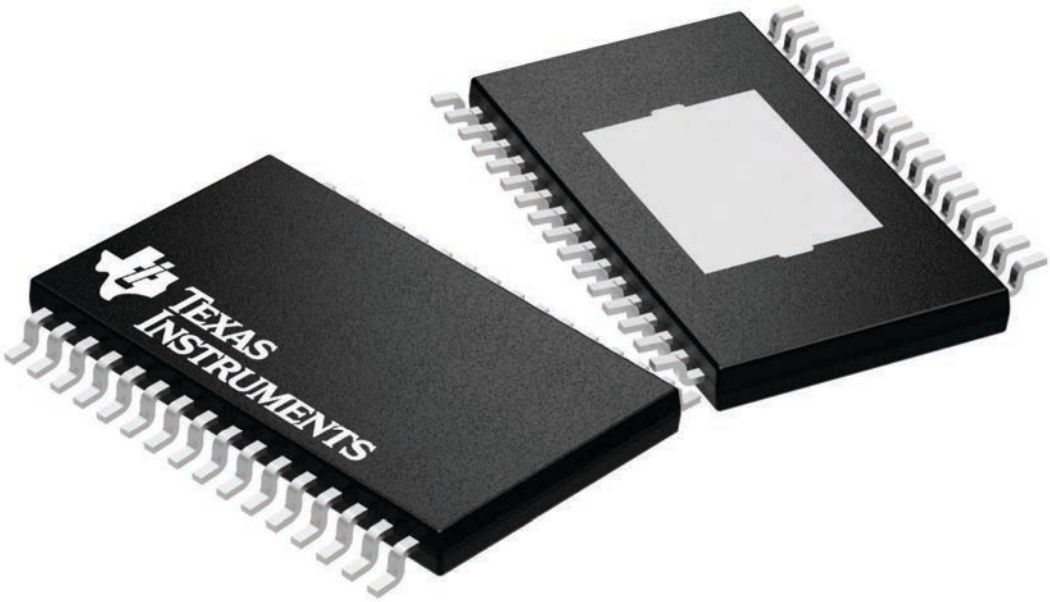
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

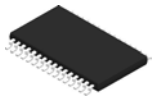
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

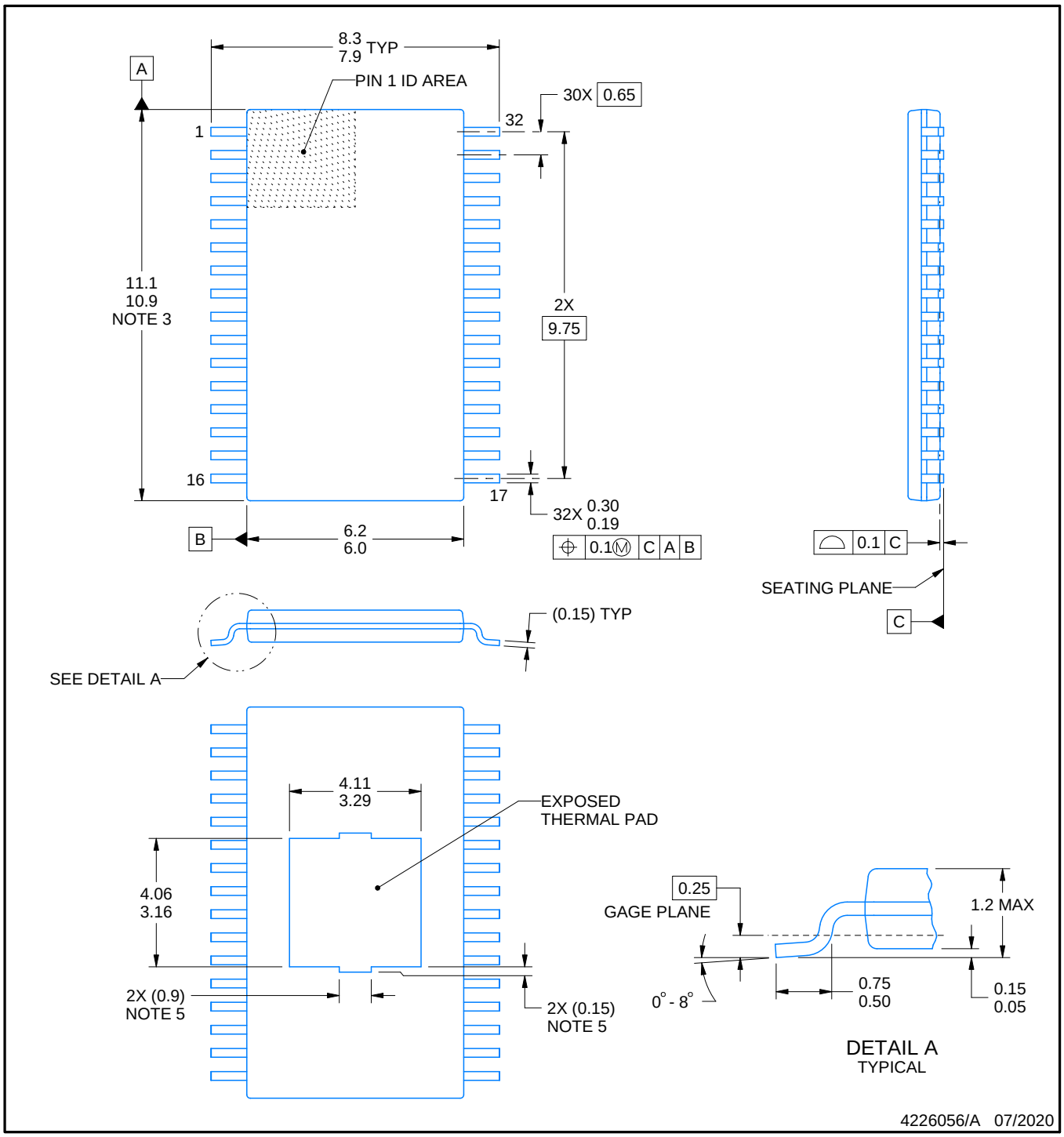


PACKAGE OUTLINE

DAP0032F

PowerPAD™ TSSOP - 1.2 mm max height

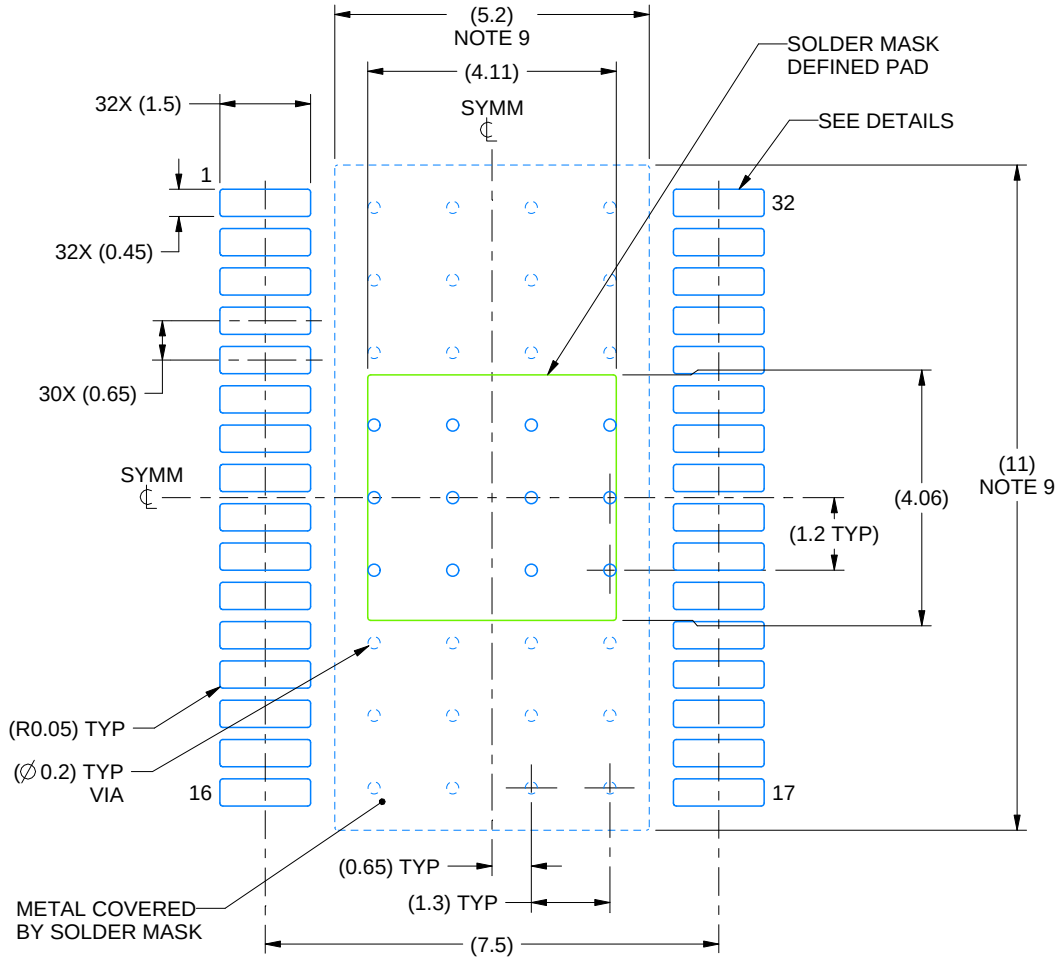
PLASTIC SMALL OUTLINE



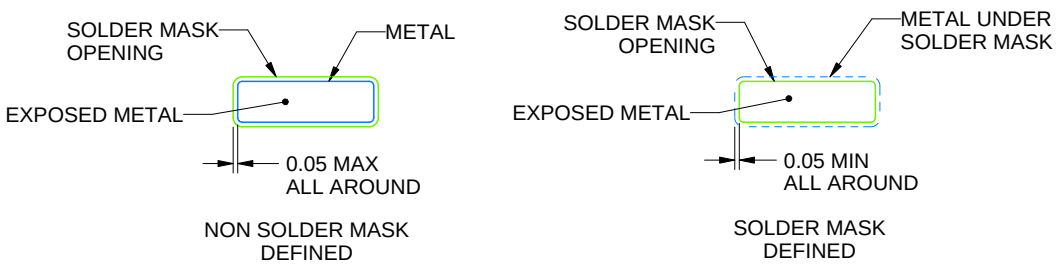
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

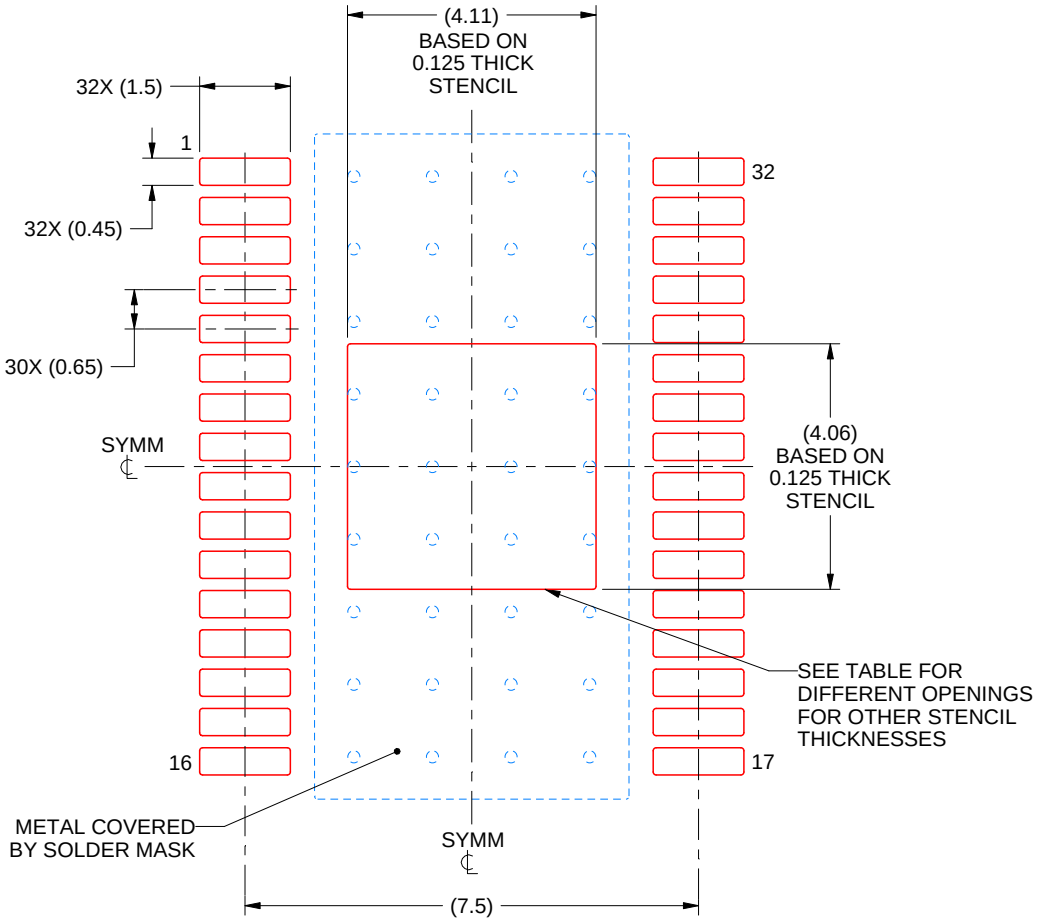


SOLDER MASK DETAILS
NOT TO SCALE

4226056/A 07/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.60 X 4.54
0.125	4.11 X 4.06 (SHOWN)
0.15	3.75 X 3.71
0.175	3.47 X 3.43

4226056/A 07/2020

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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