

SNx4AHC125 具有三态输出的四路总线缓冲门

1 特性

- 工作电压范围：2V 至 5.5V
- 闩锁性能超过 250mA，符合 JESD 17 规范的要求
- 四个独立输出使能引脚

2 应用

- 流量计
- 可编程逻辑控制器
- 以太网供电 (PoE)
- 电机驱动与控制
- 电子销售终端

3 说明

SNx4AHC125 器件是四路总线缓冲门，采用具有三态输出的独立线路驱动器。当每个输出的相关输出使能 (\overline{OE}) 输入为高电平时，输出被禁用。当 \overline{OE} 为低电平时，相应的逻辑门会将来自 A 输入的数据传递到 Y 输出。

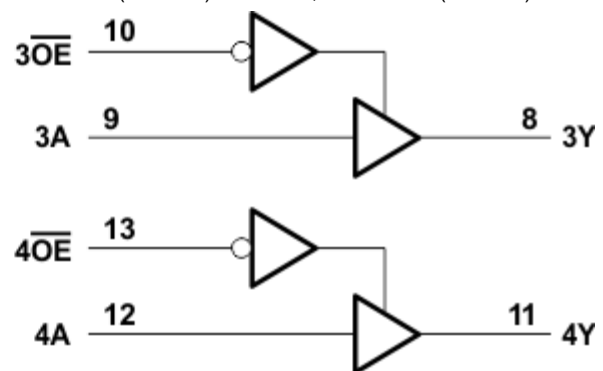
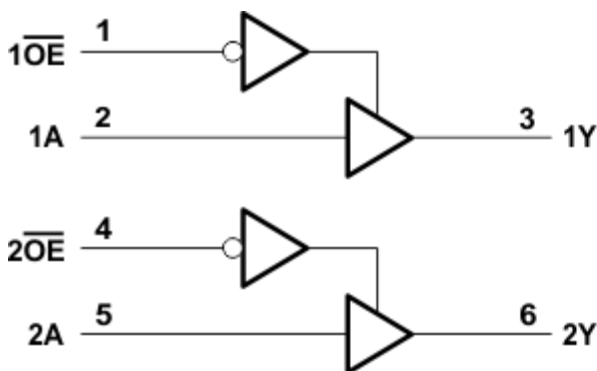
为了确保加电或断电期间的高阻抗状态， \overline{OE} 必须通过一个上拉电阻器被连接至 V_{CC} ；该电阻器的最小值由驱动器的电流灌入能力来决定。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值) ²
SN54AHC125	J (CDIP, 14)	8.89mm x 8.89mm
	W (CFP, 14)	19.56mm x 6.67mm
	FK (LCCC, 20)	9.21mm x 5.97mm
SN74AHC125	DB (SSOP, 14)	6.20mm x 5.30mm
	D (SOIC, 14)	8.65mm x 3.91mm
	NS (SO, 14)	10.30mm x 5.30mm
	DGV (TVSOP, 14)	3.60mm x 4.40mm
	PW (TSSOP, 14)	5.00mm x 4.40mm
	N (PDIP, 14)	19.30mm x 6.35mm
	RGY (VQFN, 14)	3.50mm x 3.50mm
BQA (WQFN, 14)	3mm x 2.5mm	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 x 宽) 为标称值，并包括引脚 (如适用)。



所示引脚编号用于 D、DB、DGV、J、N、NS、PW、RGY 和 W 封装。

逻辑图 (正逻辑)



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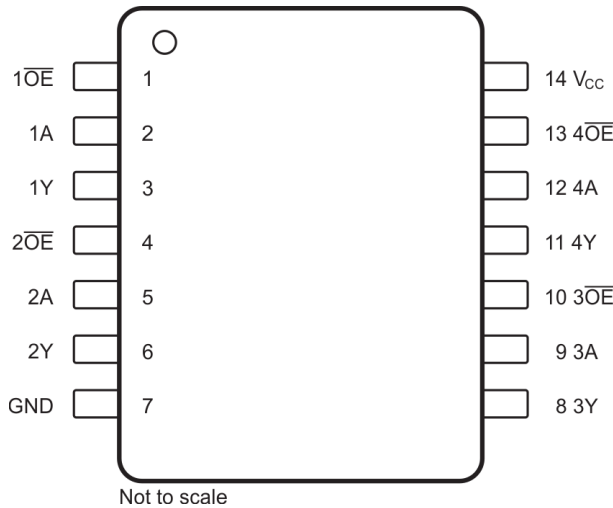
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (June 2023) to Revision N (October 2023)	Page
• Updated D and PW packages for R0JC(top), R0JB, Ψ JT, Ψ JB, and R0JC(bot), all values in °C/W	6

Changes from Revision L (November 2016) to Revision M (June 2023)	Page
• 向封装信息表中添加了 BQA 封装.....	1
• Updated R0JA values: D = 92.6 to 124.5, PW = 121.5 to 147.7, all values in °C/W	6
• Added thermal value for R0JA: BQA = 88.3, all values in °C/W.....	6

5 Pin Configuration and Functions



Not to scale

图 5-1. D, DB, DGV, N, NS, J, W, or PW Package 14-Pin SOIC, SSOP, TVSOP, PDIP, SO, CDIP, CFP, or TSSOP Top View

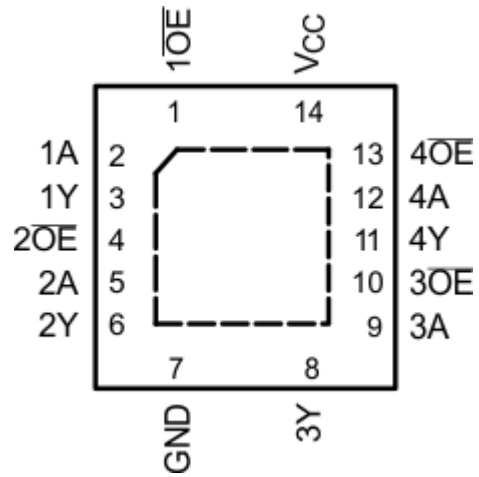
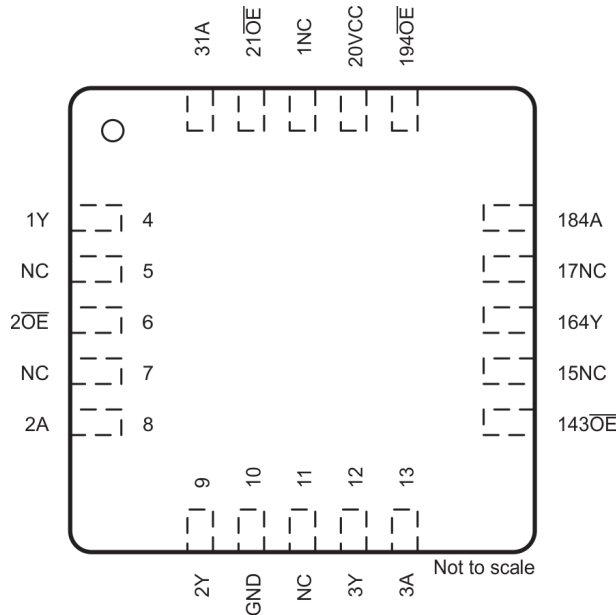


图 5-2. RGY or BQA Package 14-Pin VQFN Top View



Not to scale

图 5-3. FK Package 20-Pin LCCC Top View

表 5-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, SSOP, TVSOP, PDIP, SO, CDIP, CFP, TSSOP, VQFN	LCCC		
1 \overline{OE}	1	2	I	Output enable for gate 1
1A	2	3	I	Gate 1 input
1Y	3	4	O	Gate 1 output
2 \overline{OE}	4	6	I	Output enable for gate 2
2A	5	8	I	Gate 2 input
2Y	6	9	O	Gate 2 output
3 \overline{OE}	10	14	I	Output enable for gate 3
3A	9	13	I	Gate 3 input
3Y	8	12	O	Gate 3 output
4 \overline{OE}	13	19	I	Output enable for gate 4
4A	12	18	I	Gate 4 input
4Y	11	16	O	Gate 4 output
GND	7	10	—	Ground pin
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V _{CC}	14	20	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage		-0.5	7	V
Input voltage ⁽²⁾		-0.5	7	V
Output voltage ⁽²⁾		-0.5	$V_{CC} + 0.5$	V
Input clamp current	$V_I < 0$		-20	mA
Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
Continuous current through V_{CC} or GND			±50	mA
Virtual operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} Supply voltage		2	5.5	V
V_{IH} High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
	$V_{CC} = 3\text{ V}$	2.1		
	$V_{CC} = 5.5\text{ V}$	3.85		
V_{IL} Low-level Input voltage	$V_{CC} = 2\text{ V}$		0.5	V
	$V_{CC} = 3\text{ V}$		0.9	
	$V_{CC} = 5.5\text{ V}$		1.65	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 2\text{ V}$		-50	µA
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	mA
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	
I_{OL} Low-level output current	$V_{CC} = 2\text{ V}$		50	µA
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	mA
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	
$\Delta t/\Delta v$ Input Transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	ns/V
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	
T_A Operating free-air temperature		-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4AHC125								UNIT
		D (SOIC)	DB (SSOP)	NS (SO)	DGV (TVSOP)	PW (TSSOP)	N (PDIP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	107.3	89.9	134.6	147.7	56.3	55.1	88.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	59.3	47.7	53.9	77.4	43.9	52.3	90.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81	54.7	48.6	63.8	90.9	36.1	30.9	56.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37	24	17.5	6.3	27.2	29.2	2.4	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.6	54.1	48.3	63.2	90.2	36	31	56.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	12.7	33.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -50 \mu A$	$V_{CC} = 2 V$	$T_A = 25^\circ C$	1.9	2		V
			$T_A = -55^\circ C$ to $125^\circ C$ (SN54AHC125)	1.9			
			$T_A = -40^\circ C$ to $85^\circ C$ (SN74AHC125)	1.9			
			$T_A = -40^\circ C$ to $125^\circ C$ (recommended SN74AHC125)	1.9			
		$V_{CC} = 3 V$	$T_A = 25^\circ C$	2.9	3		
			$T_A = -55^\circ C$ to $125^\circ C$ (SN54AHC125)	2.9			
			$T_A = -40^\circ C$ to $85^\circ C$ (SN74AHC125)	2.9			
			$T_A = -40^\circ C$ to $125^\circ C$ (recommended SN74AHC125)	2.9			
		$V_{CC} = 4.5 V$	$T_A = 25^\circ C$	4.4	4.5		
			$T_A = -55^\circ C$ to $125^\circ C$ (SN54AHC125)	4.4			
			$T_A = -40^\circ C$ to $85^\circ C$ (SN74AHC125)	4.4			
			$T_A = -40^\circ C$ to $125^\circ C$ (recommended SN74AHC125)	4.4			
	$I_{OH} = -4 mA$ and $V_{CC} = 3 V$	$T_A = 25^\circ C$	2.58				
		$T_A = -55^\circ C$ to $125^\circ C$ (SN54AHC125)	2.48				
		$T_A = -40^\circ C$ to $85^\circ C$ (SN74AHC125)	2.48				
		$T_A = -40^\circ C$ to $125^\circ C$ (recommended SN74AHC125)	2.48				
$I_{OH} = -8 mA$ and $V_{CC} = 4.5 V$	$T_A = 25^\circ C$	3.94					
	$T_A = -55^\circ C$ to $125^\circ C$ (SN54AHC125)	3.8					
	$T_A = -40^\circ C$ to $85^\circ C$ (SN74AHC125)	3.8					
	$T_A = -40^\circ C$ to $125^\circ C$ (recommended SN74AHC125)	3.8					

6.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OL}	I _{OL} = 50 μA	V _{CC} = 2 V	T _A = 25°C		0.1	V
			T _A = -55°C to 125°C (SN54AHC125)		0.1	
			T _A = -40°C to 85°C (SN74AHC125)		0.1	
			T _A = -40°C to 125°C (recommended SN74AHC125)		0.1	
		V _{CC} = 3 V	T _A = 25°C		0.1	
			T _A = -55°C to 125°C (SN54AHC125)		0.1	
			T _A = -40°C to 85°C (SN74AHC125)		0.1	
			T _A = -40°C to 125°C (recommended SN74AHC125)		0.1	
	V _{CC} = 4.5 V	T _A = 25°C		0.1		
		T _A = -55°C to 125°C (SN54AHC125)		0.1		
		T _A = -40°C to 85°C (SN74AHC125)		0.1		
		T _A = -40°C to 125°C (recommended SN74AHC125)		0.1		
	I _{OH} = 4 mA and V _{CC} = 3 V	T _A = 25°C		0.36		
		T _A = -55°C to 125°C (SN54AHC125)		0.5		
		T _A = -40°C to 85°C (SN74AHC125)		0.44		
		T _A = -40°C to 125°C (recommended SN74AHC125)		0.5		
I _{OH} = 8 mA and V _{CC} = 4.5 V	T _A = 25°C		0.36			
	T _A = -55°C to 125°C (SN54AHC125)		0.5			
	T _A = -40°C to 85°C (SN74AHC125)		0.44			
	T _A = -40°C to 125°C (recommended SN74AHC125)		0.5			
I _I	V _I = 5.5 V or GND and V _{CC} = 0 V to 5.5 V	T _A = 25°C		±0.1	μA	
		T _A = -55°C to 125°C (SN54AHC125)		±1 ⁽¹⁾		
		T _A = -40°C to 85°C (SN74AHC125)		±1		
		T _A = -40°C to 125°C (recommended SN74AHC125)		±1		
I _{oz}	V _O = V _{CC} or GND and V _{CC} = 5.5 V	T _A = 25°C		±0.25	μA	
		T _A = -55°C to 125°C (SN54AHC125)		±2.5		
		T _A = -40°C to 85°C (SN74AHC125)		±2.5		
		T _A = -40°C to 125°C (recommended SN74AHC125)		±2.5		
I _{CC}	V _I = V _{CC} or GND, I _O = 0, and V _{CC} = 5.5 V	T _A = 25°C		4	μA	
		T _A = -55°C to 125°C (SN54AHC125)		40		
		T _A = -40°C to 85°C (SN74AHC125)		40		
		T _A = -40°C to 125°C (recommended SN74AHC125)		40		
C _i	V _I = V _{CC} or GND and V _{CC} = 5 V	T _A = 25°C		4	pF	
		T _A = -40°C to 85°C (SN74AHC125)		10		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

6.6 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range and $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted; see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL} , t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		5.6 ⁽¹⁾	8 ⁽¹⁾	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1 ⁽¹⁾		9.5 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		9.5	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		9.5	
t_{PZL} , t_{PZH}	\overline{OE}	Y	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		5.4 ⁽¹⁾	8 ⁽¹⁾	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1 ⁽¹⁾		9.5 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)			9.5	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)			9.5	
t_{PLZ} , t_{PHZ}	\overline{OE}	Y	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		7.0 ⁽¹⁾	9.7 ⁽¹⁾	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1 ⁽¹⁾		11.5 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1 ⁽¹⁾		11.5 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1 ⁽¹⁾		11.5 ⁽¹⁾	
t_{PHL} , t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		8.1	11.5	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1		13	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		13	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		13	
t_{PZL} , t_{PZH}	\overline{OE}	Y	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		7.9	11.5	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1		13	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		13	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		13	
t_{PLZ} , t_{PHZ}	\overline{OE}	Y	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		9.5	13.2	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1		15	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		15	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		15	
$t_{sk(o)}$	\overline{OE}	Y	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$			1.5 ⁽²⁾	ns
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)			1.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

6.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range and $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted; see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	A	Y	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		3.8 ⁽¹⁾	5.5 ⁽¹⁾	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1 ⁽¹⁾		6.5 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		6.5	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		6.5	
t_{PZH} , t_{PZL}	\overline{OE}	Y	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		3.6 ⁽¹⁾	5.1 ⁽¹⁾	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1 ⁽¹⁾		6 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		6	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		6	
t_{PHZ} , t_{PLZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		4.6 ⁽¹⁾	6.8 ⁽¹⁾	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1 ⁽¹⁾		8 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1 ⁽¹⁾		8 ⁽¹⁾	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1 ⁽¹⁾		8 ⁽¹⁾	
t_{PLH} , t_{PHL}	A	Y	$C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$		5.3	7.5	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1		8.5	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		8.5	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		8.5	
t_{PZH} , t_{PZL}	\overline{OE}	Y	$C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$		5.1	7.1	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1		8	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		8	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		8	
t_{PHZ} , t_{PLZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$		6.1	8.8	ns
				$T_A = -55^\circ\text{C}$ to 125°C (SN54AHC125)	1		10	
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)	1		10	
				$T_A = -40^\circ\text{C}$ to 125°C (recommended SN74AHC125)	1		10	
$t_{sk(o)}$	\overline{OE}	Y	$C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$			1 ⁽²⁾	ns
				$T_A = -40^\circ\text{C}$ to 85°C (SN74AHC125)			1	

6.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, and $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic (V_{OL})		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic (V_{OL})		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic (V_{OH})	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

6.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT	
C_{pd}	Power dissipation capacitance	No load and $f = 1\text{ MHz}$	9.5	pF

6.10 Typical Characteristics

图 6-1 shows I_{CC} for varying V_{IN} values when V_{CC} is $5\text{ V} \pm 0.5\text{ V}$ and $T_A = 25^\circ\text{C}$.

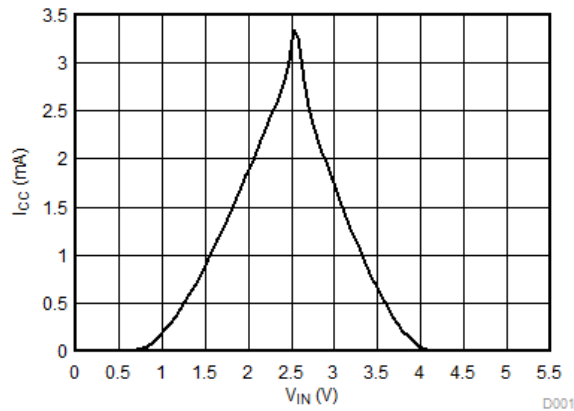
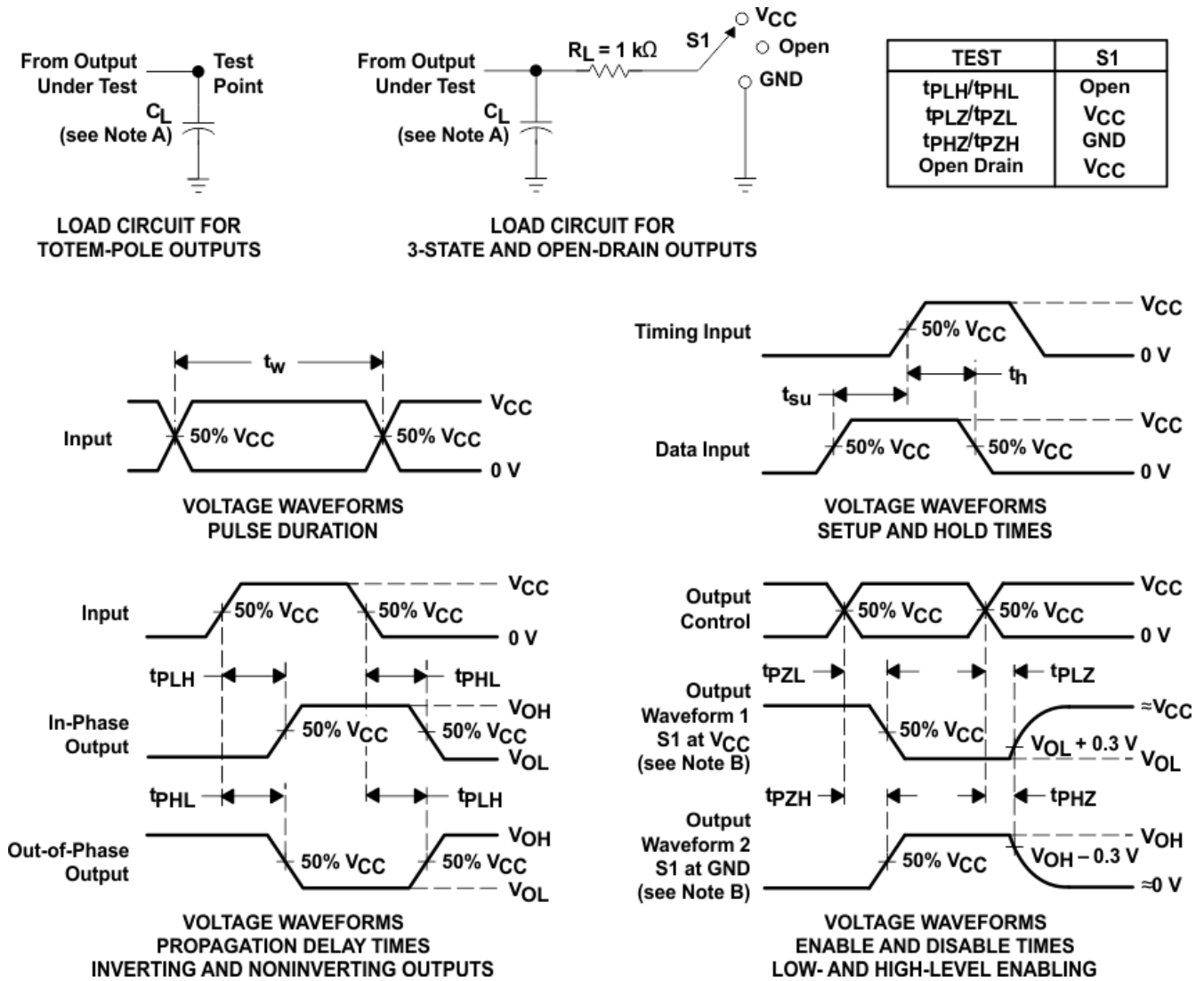


图 6-1. V_{IN} vs I_{CC}

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

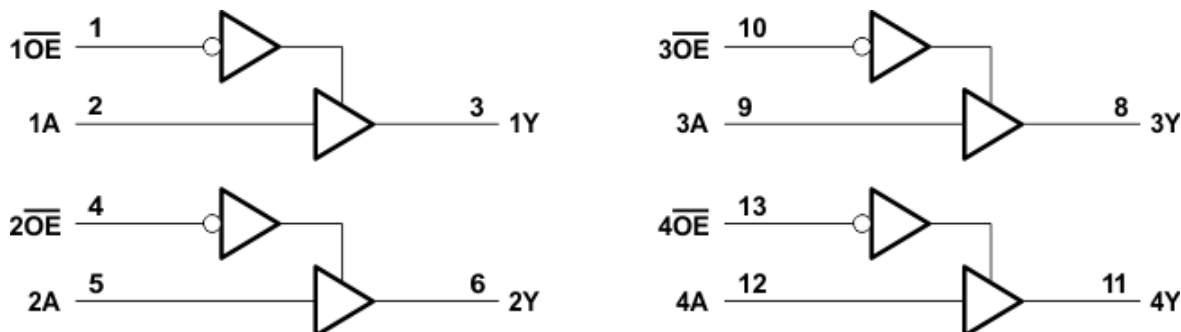
图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4AHC125 devices have four integrated bus buffer gates. Each gate can be individually controlled from their respective output enable pins or tied together and controlled simultaneously. This allows for control of up to four different lines from one device. Often times a microcontroller have multiple function options for a single pin. By using GPIO pins to enable specific buffers, the SNx4AHC125 can act as a multiplexer to select a specific data line depending on what pin function is selected on the microcontroller. At the same time, the lines that are not selected are isolated from the pin.

8.2 功能方框图



所示引脚编号用于 D、DB、DGV、J、N、NS、PW、RGY 和 W 封装。

8.3 特性说明

每个缓冲器都有自己的输出使能。这允许单独控制每个缓冲器。当输出使能为低电平时，输入被传递到输出。当输出使能为高电平时，输出为高阻抗。此功能在可能需要隔离的应用中非常有用。

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SNx4AHC125.

**表 8-1. Function Table
(Each Buffer)**

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

9 Application and Implementation

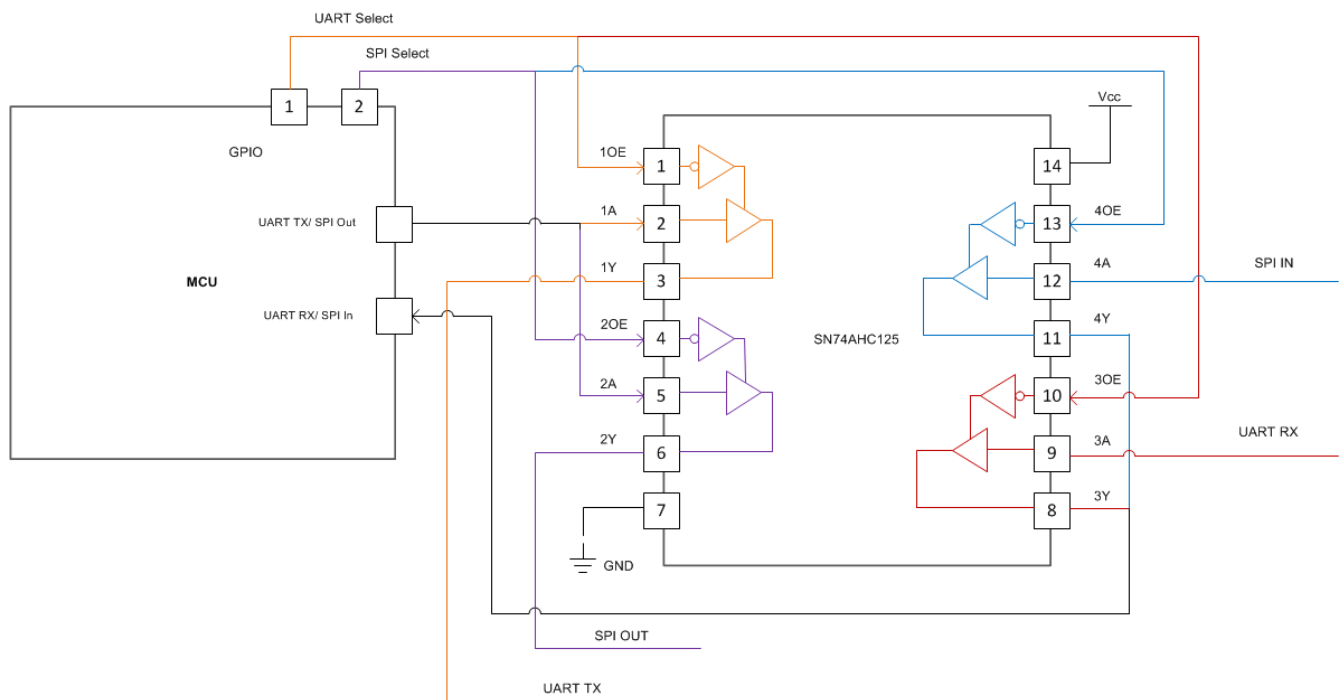
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The wide operating range of the SNx4AHC125 devices allows for implementation into a variety of applications. In addition to the wide operating range, these devices differentiate from similar devices because they have four buffers that can be individually controlled through their independent output enable (\overline{OE}) pins. Each buffer is either enabled and passes data from A to Y, or disabled and set to a high-impedance state.

9.2 Typical Application



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图 9-1. Digital MUX

9.2.1 Design Requirements

It is best to set V_{CC} for the SN74AHC125 to the same level as the microcontroller logic levels. This allows for optimal performance. The SN74AHC125 can safely handle input levels from -0.5 V to 7 V. However, if the logic levels that are being received vary from the V_{CC} level of the device then errors can occur. For example, if V_{CC} is 5.5 V then the minimum high-level input voltage (V_{IH}) level is 3.85 V. This means if the microcontroller is sending a HIGH signal, but HIGH = 3.3 V, it would be too low a level for the SNx4AHC125 to register it as what it must be. In this case V_{CC} would need to be lowered in order to lower the V_{IH} minimum. The opposite is also true for low-level input voltage (V_{IL}). If V_{CC} is set to 2 V, then V_{IL} maximum is 0.5 V. Depending on the microcontroller logic levels, a LOW signal may not go low enough for the SNx4AHC125 to register it.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:

- For V_{IH} and V_{IL} levels at varying V_{CC} , see [Recommended Operating Conditions](#).
- Be mindful of rise time and fall time specifications for the output enable pins to ensure that the right buffers are enabled and the others are disabled in time. This minimizes interference on the microcontroller pin and to exterior circuitry. See [Switching Characteristics, \$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}\$](#) and [Switching Characteristics, \$V_{CC} = 5\text{ V} \pm 0.5\text{ V}\$](#) table for more details.

2. Recommended Output Conditions:

- Load currents must not exceed I_O maximum per output and must not exceed continuous current through V_{CC} or GND total current for the part. These limits are located in the [Absolute Maximum Ratings](#).
- Outputs must not be pulled above V_{CC} .

9.2.3 Application Curves

Typical device at 25°C

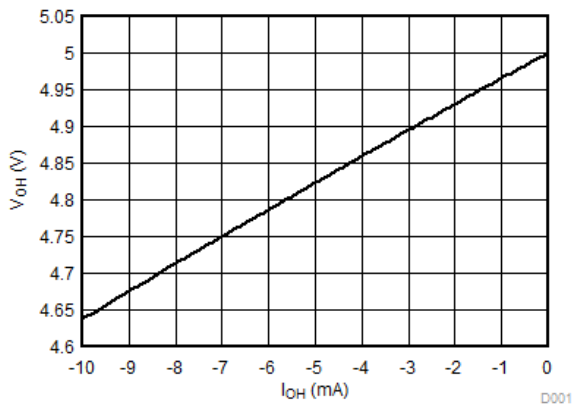


图 9-2. I_{OH} vs V_{OH}

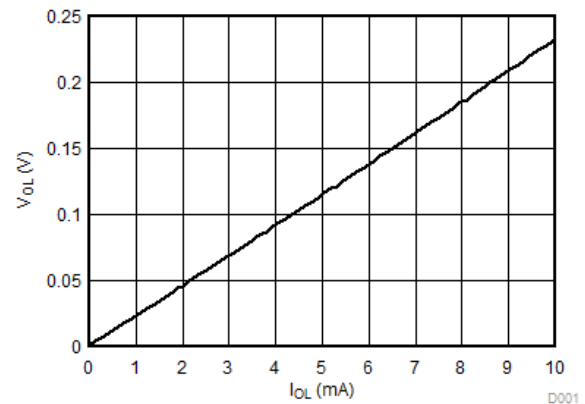


图 9-3. I_{OL} vs V_{OL}

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01- μF or 0.022- μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} (whichever make more sense or is more convenient).

9.4.1.1 Layout Example

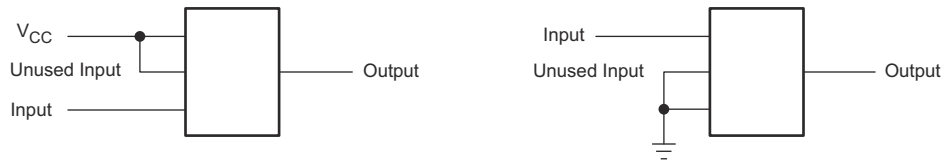


图 9-4. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support (Analog)

10.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

10.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC125	Click here	Click here	Click here	Click here	Click here
SN74AHC125	Click here	Click here	Click here	Click here	Click here

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686801Q2A SNJ54AHC 125FK	Samples
5962-9686801QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QC A SNJ54AHC125J	Samples
5962-9686801QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QD A SNJ54AHC125W	Samples
SN74AHC125BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	Samples
SN74AHC125DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	Samples
SN74AHC125DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	Samples
SN74AHC125DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	Samples
SN74AHC125DRG4	LIFEBUY	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	
SN74AHC125N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC125N	Samples
SN74AHC125NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC125N	Samples
SN74AHC125NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	Samples
SN74AHC125PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	Samples
SN74AHC125PWRE4	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	
SN74AHC125PWRG4	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	
SN74AHC125RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA125	Samples
SNJ54AHC125FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686801Q2A SNJ54AHC 125FK	Samples
SNJ54AHC125J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QC A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC125W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54AHC125J 5962-9686801QD A SNJ54AHC125W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC125, SN74AHC125 :

- Catalog : [SN74AHC125](#)
- Automotive : [SN74AHC125-Q1](#), [SN74AHC125-Q1](#)
- Enhanced Product : [SN74AHC125-EP](#), [SN74AHC125-EP](#)
- Military : [SN54AHC125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC125DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC125DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC125DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC125DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC125NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC125PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC125RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686801QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC125FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC125W	W	CFP	14	25	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

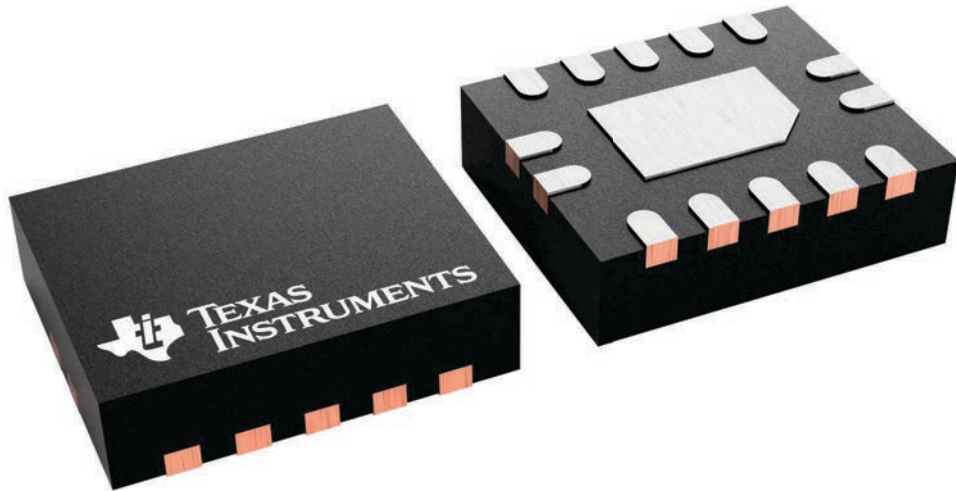
BQA 14

WQFN - 0.8 mm max height

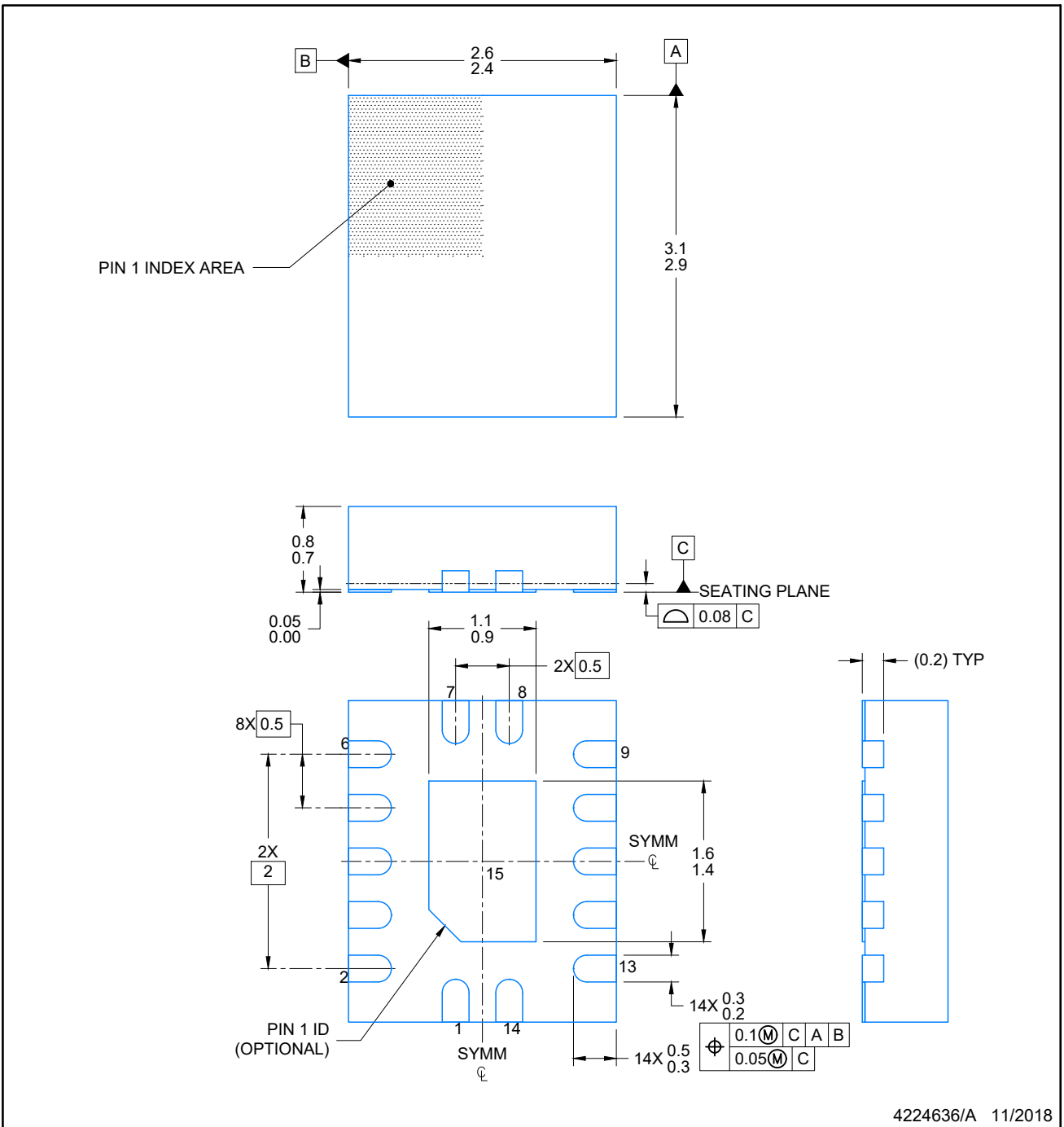
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

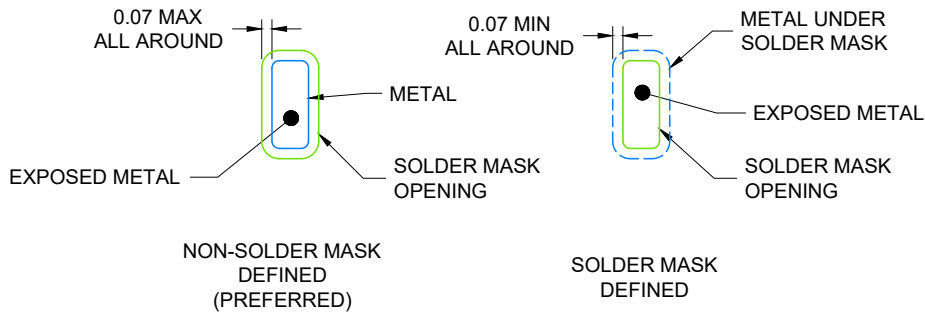
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

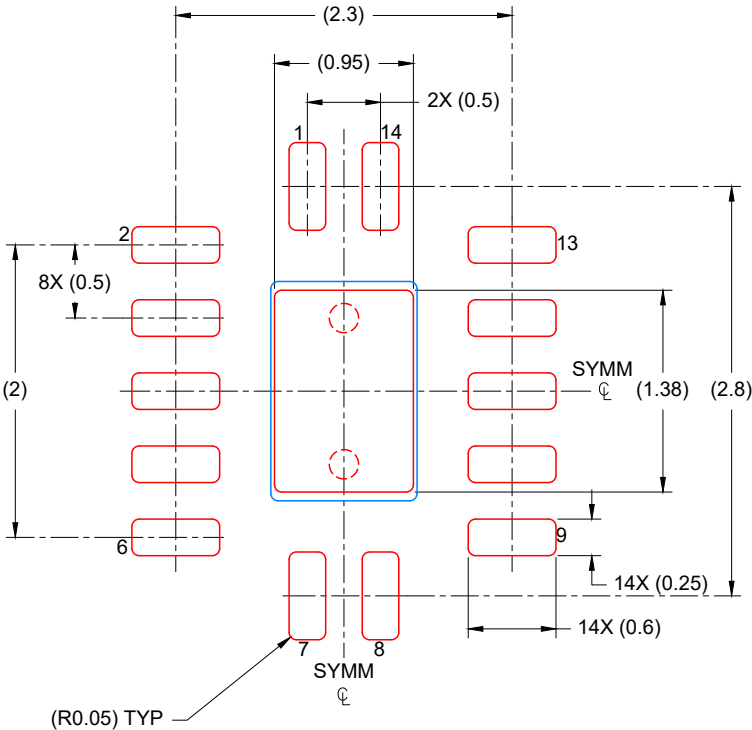
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G



J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X





4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

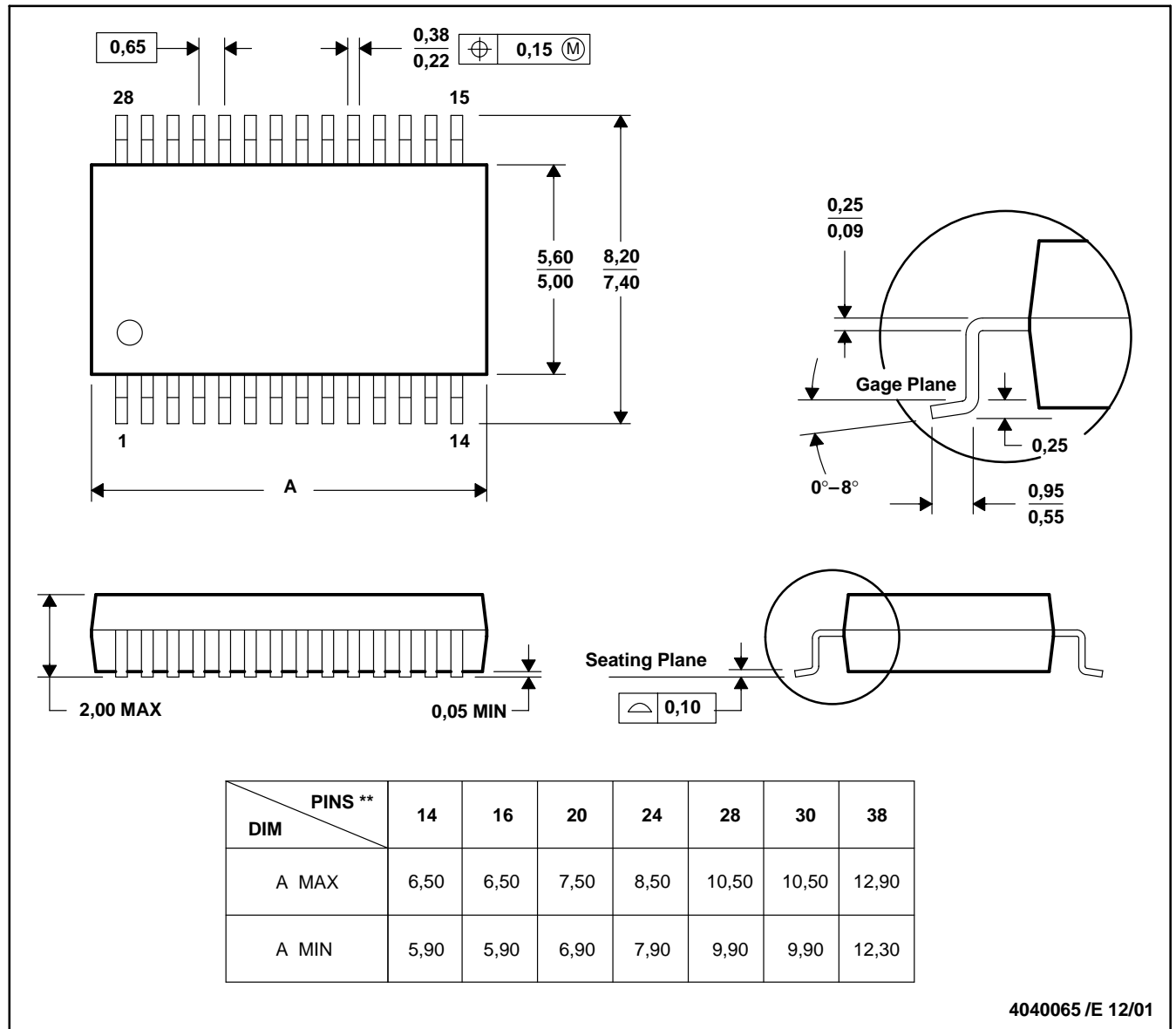


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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