TEXAS INSTRUMENTS

TCA9617A

SCPS244B – JUNE 2013 – REVISED DECEMBER 2018

TCA9617A Level-Translating FM+ I2C Bus Repeater

1 Features

- Two-Channel Bidirectional I2C Buffer
- Support for Standard Mode, Fast Mode (400 kHz), and Fast Mode+ (1 Mhz) I2C Operation
- Operating Supply Voltage Range of 0.8 V to 5.5 V on A-Side
- Operating Supply Voltage Range of 2.2 V to 5.5 V on B-Side
- Voltage-Level Translation From 0.8 V to 5.5 V and 2.2 V to 5.5 V
- Footprint and Function Replacement for TCA9517
- Active-High Repeater-Enable Input
- Open-Drain I2C I/O
- 5.5-V Tolerant I2C and Enable Input Support
- Mixed-Mode Signal Operation
- Lockup-Free Operation
- Support for Clock Stretching and Multiple Master Arbitration Across The Device
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  – 4000-V Human-Body Model (A114-A)
  – 1500-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products With Many I2C Slaves and/or Long PCB Traces

3 Description

The TCA9617A is a BiCMOS dual bidirectional buffer intended for I2C bus and SMBus systems. It can provide bidirectional voltage-level translation (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (2.2 V to 5.5 V) in mixed-mode applications. This device enables I2C and similar bus systems to be extended, without degradation of performance even during level shifting.
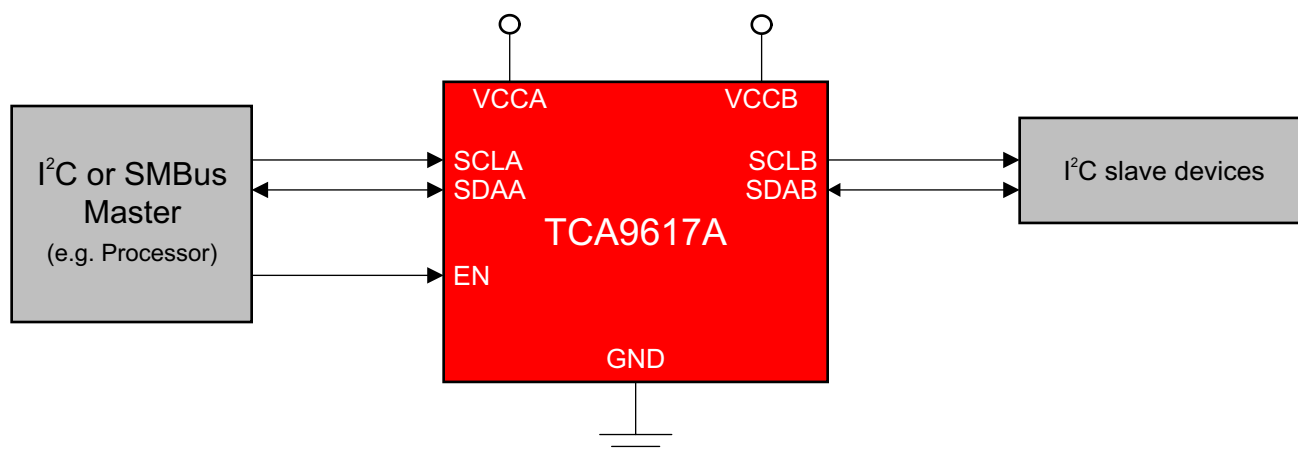
The TCA9617A buffers both the serial data (SDA) and the serial clock (SCL) signals on the I2C bus, allowing two buses of 550-pF or greater bus capacitance to be connected in an I2C application. This device can also be used to isolate two halves of a bus for voltage and capacitance.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9617A	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

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4 Revision History

Changes from Revision A (July 2014) to Revision B   **Page**

Changes from Original (June 2013) to Revision A   **Page**

5 Pin Configuration and Functions

**DGK Package
8-Pin VSSOP
Top View**

VCCA	1	8	VCCB
SCLA	2	7	SCLB
SDAA	3	6	SDAB
GND	4	5	EN

Not to scale
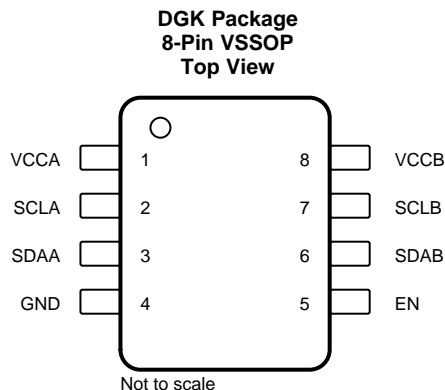
Pin Functions

PIN		DESCRIPTION
NAME	NO.	
VCCA	1	A-side supply voltage (0.8 V to 5.5 V)
SCLA	2	I^{2}C SCL line, A side. Connect to V$_{CCA}$ through a pull-up resistor.
SDAA	3	I^{2}C SDA line, A side. Connect to V$_{CCA}$ through a pull-up resistor.
GND	4	Supply ground
EN	5	Active-high repeater enable input
SDAB	6	I^{2}C SDA line, B side. Connect to V$_{CCB}$ through a pull-up resistor.
SCLB	7	I^{2}C SCL line, B side. Connect to V$_{CCB}$ through a pull-up resistor.
VCCB	8	B-side and device supply voltage (2.2 V to 5.5 V)

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V$_{CCB}$	Supply voltage range			−0.5	7	V
V$_{CCA}$	Supply voltage range			−0.5	7	V
V$_I$	Enable input voltage range[2]			−0.5	7	V
V$_{I/O}$	I^{2}C bus voltage range[2]			−0.5	7	V
I$_{IK}$	Input clamp current	V$_I$ < 0			−50	mA
I$_{OK}$	Output clamp current	V$_O$ < 0			−50	
I$_O$	Continuous output current				±50	mA
	Continuous current through V$_{CC}$ or GND				±100	mA
T$_{stg}$	Storage temperature range			−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

Product Folder Links: *TCA9617A*

6.2 ESD Ratings

			MIN	MAX	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus	0.8	V_{CCB}	V
V_{CCB}	Supply voltage, B-side bus	2.2	5.5	V
I_{OLA}	Low-level output current		30	mA
I_{OLB}	Low-level output current	0.1	30	mA
T_A	Operating free-air temperature	−40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TCA9617A	UNIT
		DGK	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Product Folder Links: *TCA9617A*

6.5 Electrical Characteristics

V_{CCB} = 2.2 V to 5.5 V, GND = 0 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK} Input clamp voltage		I_I = −18 mA	2.2 V to 5.5 V			−1.2	V
V_{OL} Low-level output voltage	SDAB, SCLB	I_{OL} =100uA or 30mA, V_{ILA} = 0 V	2.2 V to 5.5 V	0.48	0.53	0.58	V
	SDAA, SCLA	I_{OL} = 30mA			0.1	0.2	
V_{IH} High-level input voltage	SDAA, SCLA		2.2 V to 5.5 V	0.7 × V_{CCA}		V_{CCB}	V
	SDAB, SCLB			0.7 × V_{CCB}		V_{CCB}	
	EN			0.7 × V_{CCB}		5.5	
V_{IL} Low-level input voltage	SDAA, SCLA		2.2 V to 5.5 V			0.3 × V_{CCA}	V
	SDAB, SCLB					0.4	
	EN					0.3 × V_{CCB}	
I_{CCA} Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND	2.2 V to 5.5 V			13	µA
I_{CCB} Quiescent supply current		Both Channels high, SDAA = SCLA = V_{CCA} B-side pulled up to V_{CCB} with pullup resistors	5.5 V		+4.5	+7	mA
		Both channels low, SDAA = SCLA = GND, I_{OLB} = 100 µA			+5.7	+8.1	
I_I Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.2 V to 5.5 V	−1		+1	µA
		V_I = 0.2 V, EN = 0		−10		+10	
		V_I = V_{CCB} − 0.2 V		−1		+1	
	SDAA, SCLA	V_I = V_{CCA}		−1		+1	
		V_I = 0.2 V		−10		+10	
		V_I = V_{CCA} − 0.2 V		−1		+1	
	EN	V_I = V_{CCB}		−1		+1	
		V_I = 0.2 V		−25			
C_I Input capacitance	EN	V_I = 3 V or 0 V	3.3 V			7	pF
	SCLA, SCLB	V_I = 3 V or 0 V	3.3 V			9	
			0 V			9	
C_I Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V			14	pF
			0 V			14	

Product Folder Links: TCA9617A

6.6 Timing Requirements

V_{CCA} = 0.8 V to 5.5 V, V_{CCB} = 2.2 V to 5.5 V, GND = 0V, T_A = –40°C to 85° (unless otherwise noted)[1][2]

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP[3]	MAX	UNIT
t_{PLH}	Propagation delay		SDAB, SCLB	SDAA, SCLA		42	55	90	ns
			SDAA, SCLA	SDAB, SCLB	V_{CCB} ≤ 3 V	61	88	137	
					V_{CCB} > 3 V	61	94	250	
t_{PHL}	Propagation delay		SDAB, SCLB	SDAA, SCLA		69	93	144	ns
			SDAA, SCLA	SDAB, SCLB		68	90	140	
t_{TLH} [4]	Transition time	B side	30%	70%			88		ns
		A side					37		ns
t_{THL}	Transition time	B side	70%	30%		5.40	6.41	13.8	ns
		A side				1.40	4.71	11.3	
t_{su}	Setup time, EN high before Start condition[5]					100			ns

(1) Times are specified with loads of 240 Ω ±1% and 400 pF ±10% on B-side and 240 Ω ±1% and 200 pF ±10% on A-side. Different load resistance and capacitance alter the rise time, thereby changing the propagation delay and transition times.
(2) Times are specified with A-side signals pulled up to V_{CCA}; V_{CCA} = 0.9 V and B-side signals pulled up to V_{CCB}; V_{CCB} = 2.5 V.
(3) Typical values were measured with V_{CCA} = 0.9 V and V_{CCB} = 2.5 V at T_A = 25°C, unless otherwise noted.
(4) T_{TLH} is determined by the pullup resistance and load capacitance.
(5) EN should change state only when the global bus and the repeater port are in an idle state.

6.7 Typical Characteristics

Figure 1. Port A V_{OL} vs I_{OL}
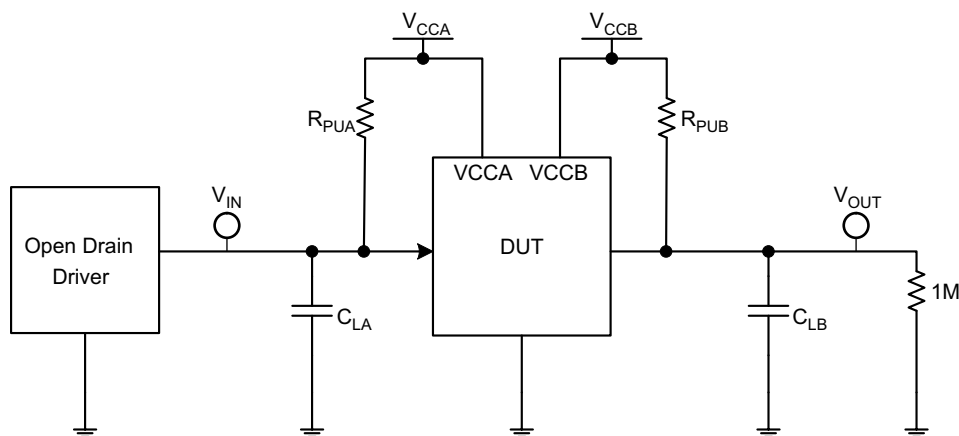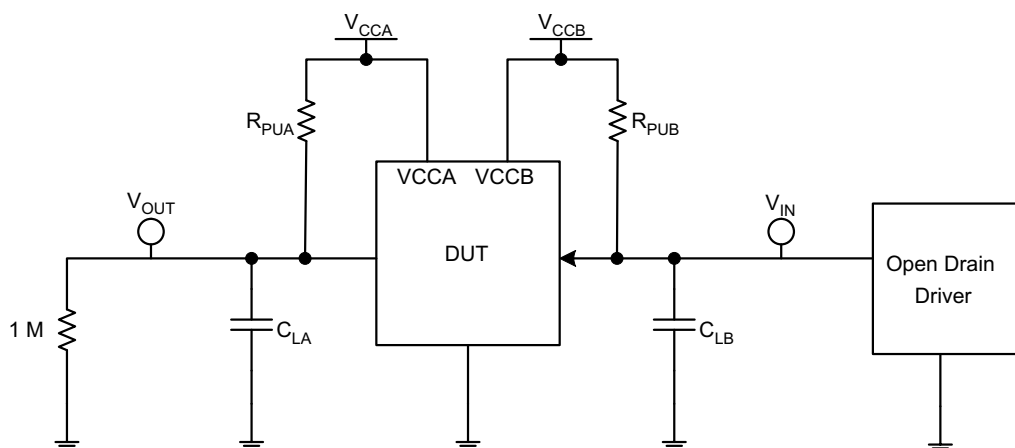

Figure 2. Port B V_{OL} vs I_{OL}

Product Folder Links: *TCA9617A*
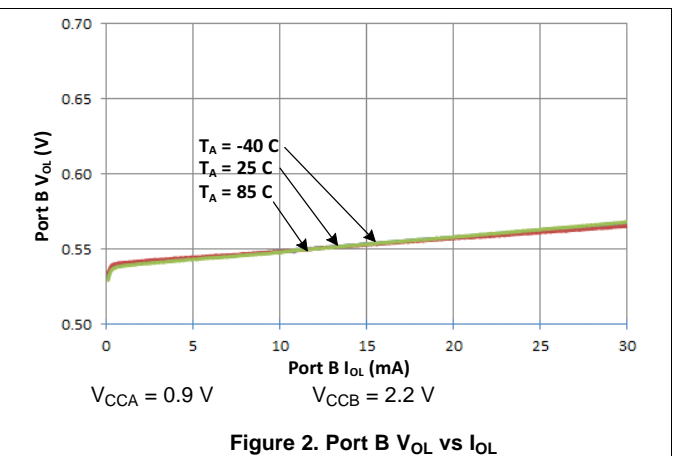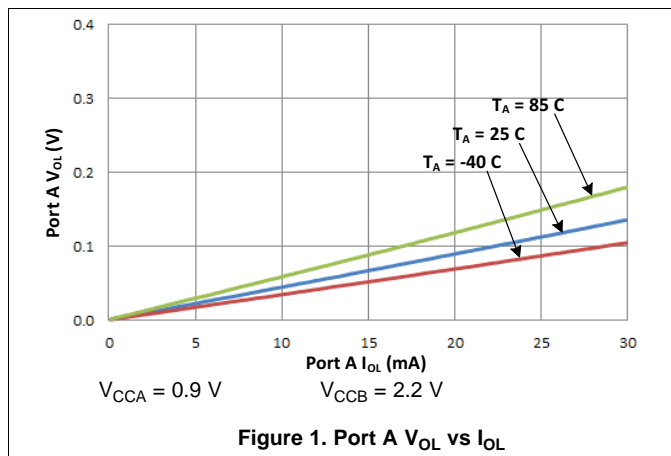
7 Parameter Measurement Information

Figure 3. Test Circuit for Open-Drain Output from A to B

A. V_{CCA} = 0.9 V

B. V_{CCB} = 2.5 V

C. R_{PUA} = R_{PUB} = 240 Ω on the A-side and the B-side

D. C_{LA} = 200 pF on A-side and C_{LB} = 400 pF on B-side (includes probe and jig capacitance)

E.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns

F.   The outputs are measured one at a time, with one transition per measurement.

Figure 4. Test Circuit for Open-Drain Output from B to A

Product Folder Links: *TCA9617A*

Parameter Measurement Information (continued)

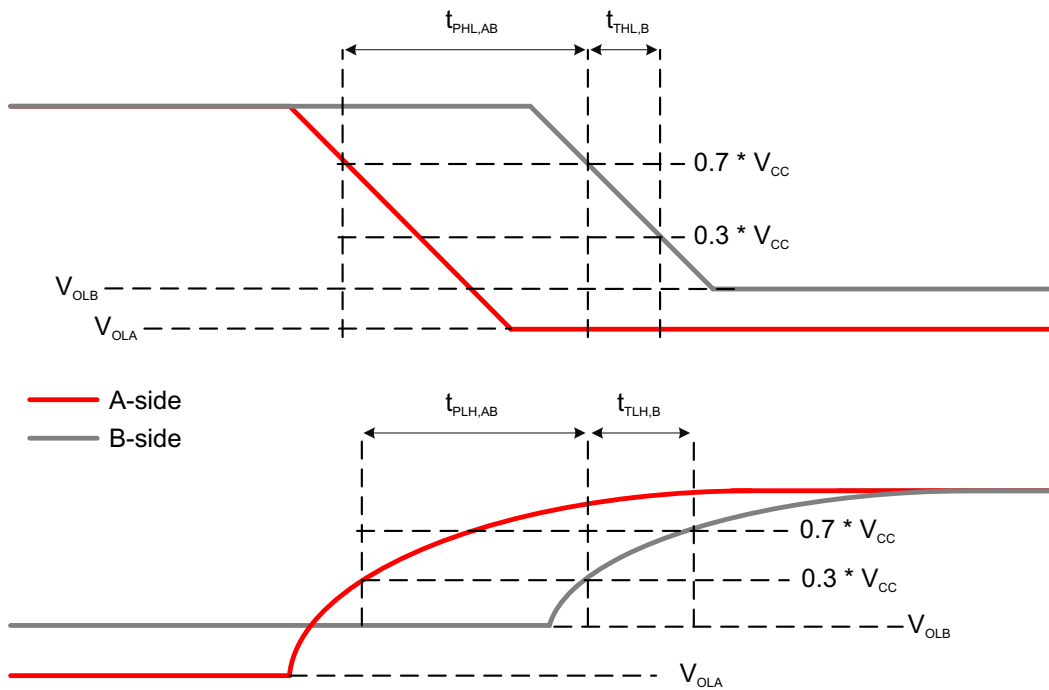**Figure 5. Propagation Delay And Transition Times (A to B)**
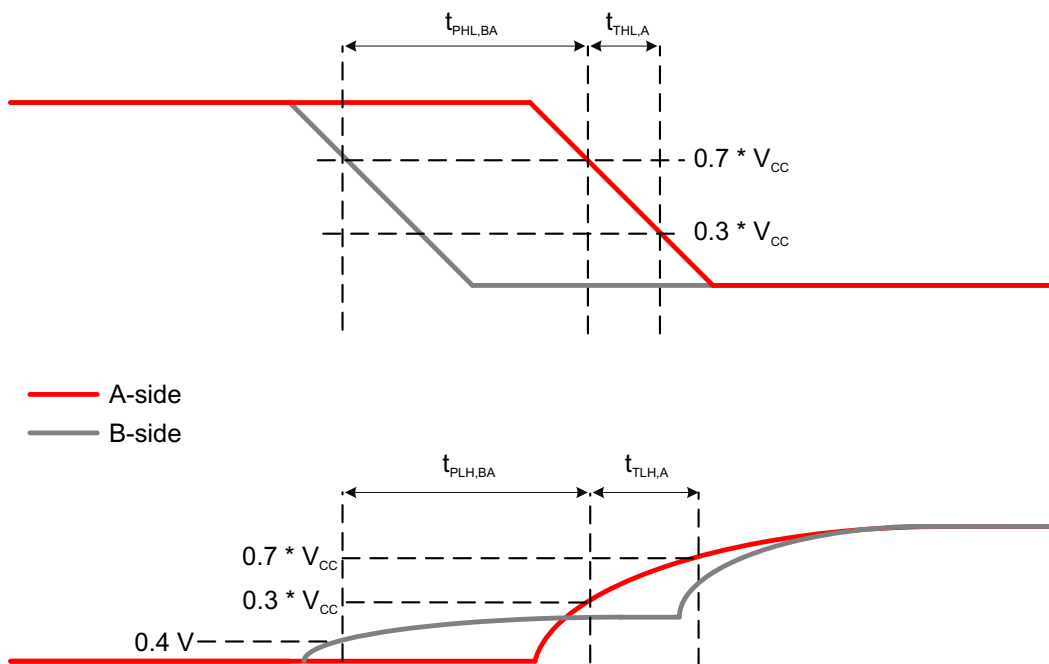
Figure 6. Propagation Delay And Transition Times (B to A)

Product Folder Links: *TCA9617A*

8 Detailed Description

8.1 Overview

The TCA9617A is a BiCMOS dual bidirectional buffer intended for I^{2}C bus and SMBus systems. As with the standard I^{2}C system, pullup resistors are required to provide the logic high levels on the buffered bus. The TCA9617A has standard open-drain configuration of the I^{2}C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode, Fast mode and Fast Mode+ I^{2}C devices.

The TCA9617A B-side drivers operate from 2.2 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output is externally driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design on the B side prevents it from being used in series with another TCA9617A B-side or other buffers that incorporate a static or dynamic offset voltage. This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The TCA9617A A-side drivers operate from 0.8 V to 5.5 V and do not have the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0-V low on the A side, which accommodates smaller voltage swings of low-voltage logic. The output pulldown on the A side drives a hard low, and the input level is set to 0.3 V_{CCA} to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.8 V.

The A side of two or more TCA9617As can be connected together to allow a star topology, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static or dynamic offset voltage. Multiple TCA9617As can be connected in series, A side to B side, with no buildup in offset voltage with only time-of-flight delays to consider.

The TCA9617A includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.0 V and V_{CCA} is above 0.7 V. V_{CCA} is only used to provide references for the A-side input comparators and the power-good-detect circuit. The TCA9617A internal circuitry and all I/Os are powered by the V_{CCB} pin; however, due to ESD protection requirements on the SCLA and SDAA, it is required to power-up V_{CCB} prior to V_{CCA}. IF SDA and SCL (on A-side or B-side) are pulled up to a positive voltage before V_{CCB} is powered, there can be significant current leakage into the SCA and SCL pins that could cause them to be pulled down. The SDA and SCL lines shall not be pulled up to a voltage higher than V_{CCB}, even when the device is powered down.

After power up and with the EN high, the A side falling below 0.7 V_{CCA} turns on the corresponding B-side driver (either SDA or SCL) and drives the B-side down momentarily to 0 V before settling to approximately 0.5 V. When the A-side rises above 0.3 V_{CCA}, the B-side pulldown driver is turned off and the external pullup resistor pulls the pin high. If the B side falls first and goes below 0.7 V_{CCB}, the A-side driver is turned on and drives the A-side to 0 V. When the B-side rises above 0.45 V, the A-side pulldown driver is turned off and the external pullup resistor pulls the pin high.

Product Folder Links: *TCA9617A*

8.2 Functional Block Diagram
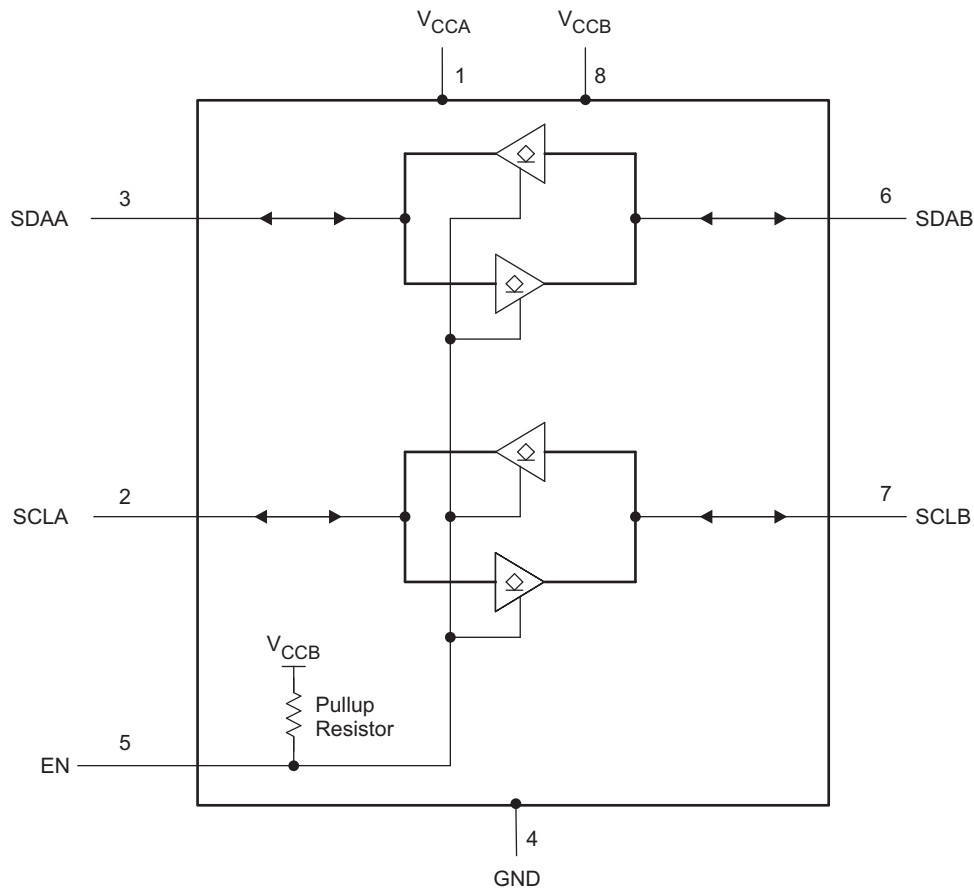
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8.3 Feature Description

8.3.1 Bidirectional Level Translation

The TCA9617A can provide bidirectional voltage level translation (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (2.2 V to 5.5 V) in mixed-mode applications.

8.3.2 V_{OL} B-side Offset Voltage

Figure 8 depicts the offset voltage on the B side of the device. As shown in Figure 8 the slave releases and the B-side rises, and it will rise to 0.5 V and stay there until the A-side rises above 0.3 V_{CCA}. This effect can cause the low level signal to have a "pedestal." Once the voltage on the A-side crosses 0.3 V_{CCA}, the B-side will continue to rise to V_{CCB}.

Due to nature of the B-side pedestal and the static offset voltage, there will be a slight overshoot (point 2) as the B-side rises from being externally driven low to the 0.5 V offset. The TCA9617A is designed to control this behavior provided the system is designed with rise times greater than 20 ns. Therefore, care should be taken to limit the pullup strength when devices with rise time accelerators are present on the B side. Excessive overshoot on the B-side pedestal may cause devices with rise time accelerators to trip prematurely if the accelerator thresholds are below 0.3 V_{CCB}. Since the A-side does not have a static offset low voltage, no pedestal is seen on the A-side as shown in Figure 7.

Product Folder Links: *TCA9617A*

Feature Description (continued)

8.3.3 High to Low Transition Characteristics

When the A side of the bus is driven to 0.7 V_{CCA}, the B side driver will turn on. This will drive the B-side to 0 V for a short period (see Figure 8) and then the B-side will rise to the static offset voltage of 0.5 V (V_{OL} of TCA9617A). This effect, called an inverted pedestal, allows the B-side to drive to logic low much faster than driving to the static offset. Driving to the static offset voltage requires that the fall time be slowed to prevent ringing.
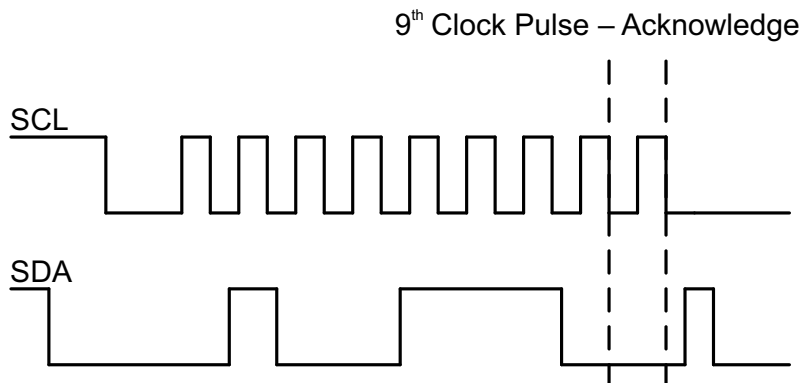

Figure 7. Bus A (0.8 V to 5.5 V Bus) Waveform
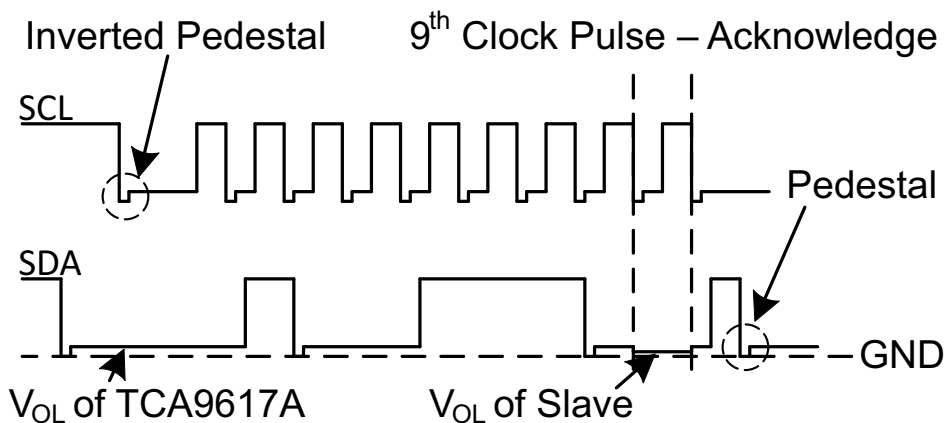
Figure 8. Bus B (2.2 V to 5.5 V Bus) Waveform

8.4 Device Functional Modes

The TCA9617A has an active-high enable (EN) input with an internal pull-up to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an I²C operation, because disabling during a bus operation may hang the bus, and enabling part way through the bus cycles could confuse the I²C parts being enabled. The EN input should change state only when the global bus and repeater port are in the idle state to prevent system failures.

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

9 Application and Implementation

9.1 Application Information

A typical application is shown in Figure 9. In this example, the system master is running on a 0.9-V I^{2}C bus, and the slave is connected to a 2.5-V bus. Both buses are running at 400 kHz. Decoupling capacitors are required but are not shown in Figure 14 for simplicity.

The TCA9617A is 5-V tolerant so no additional circuits are required to translate between 0.8-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the A side of the TCA9617A is pulled low by a driver on the I^{2}C bus, a comparator detects the falling edge when it goes below 0.7 V_{CCA} and cause the internal driver on the B side to turn on. The B-side will first pull down to 0 V and then settle to 0.5 V. When the B side of the TCA9617A falls below 0.45 V, the TCA9617A will detect the falling edge, turn on the internal driver on the A side and pull the A-side pin down to ground. In order to illustrate what would be seen for an A to B transition refer to Figure 11, and for a B to A transition see Figure 10.

On the B-side bus of the TCA9617A, the clock and data lines will have a positive offset from ground equal to the V_{OL} of the TCA9617A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver of the TCA9617A for a short delay (approximately 0.5 V), while the A-side bus rises above 0.3 V_{CCA} and then continues high.

Although the TCA9617 has a single application, the device can exist in multiple configurations. Figure 9 shows the standard configuration for the TCA9617. Multiple TCA9617s can be connected either in star configuration (Figure 12) or in series configuration (Figure 13). The design requirements , detailed design procedure, and application curves in Standard Application are valid for all three configurations.

9.2 Typical Application
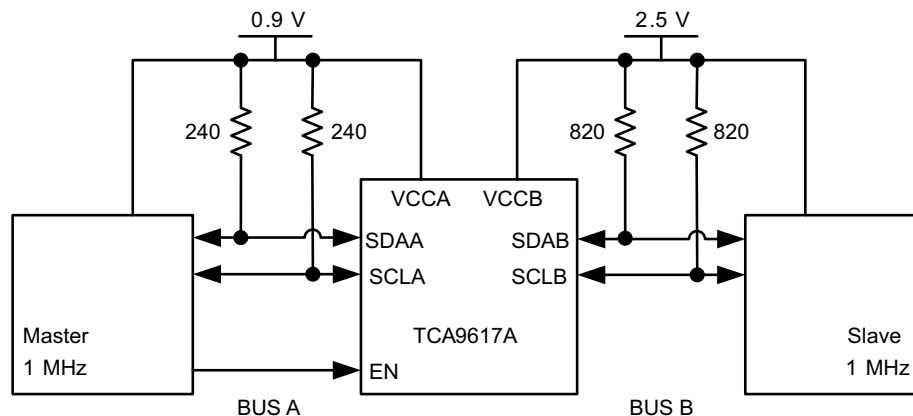
9.2.1 Standard Application

Figure 9. Bidirectional Voltage Level Translator

9.2.1.1 Design Requirements

For the level-translating application, the following should be true:
- V_{CCA} = 0.8 V to 5.5 V
- V_{CCB} = 2.2 V to 5.5 V
- $I_{OL} > I_O$

Typical Application (continued)

### 9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Pullup Resistor Sizing

For the TCA9617A to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (0.45 V). This means that the V_{OL} of any device on the B-side must be below 0.4 V to ensure proper operation.

The V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistor value. The pull-up resistor on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

The B-side pull-up resistor sizing must also ensure that the rise time is greater than 20 ns. Shorter rise times will increase the pedestal overshoot shown in point 2 of Figure 10.

9.2.1.3 Application Curves

Figure 10. B-side Pedestal

Figure 11. B-side Inverted Pedestal

Product Folder Links: *TCA9617A*
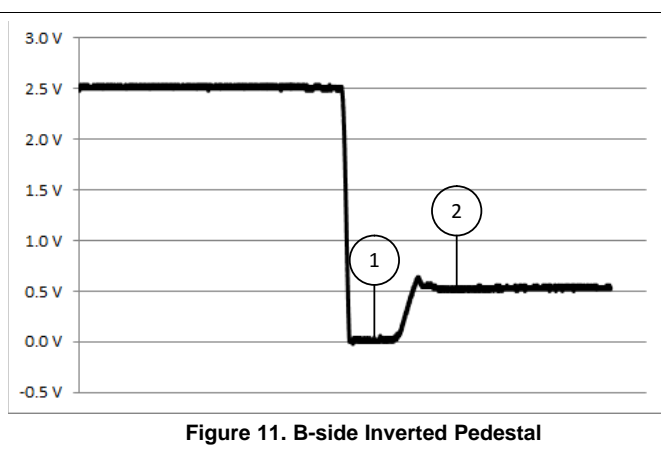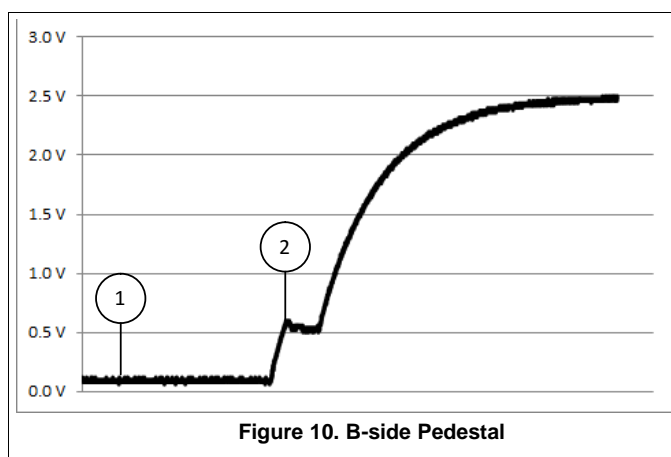
Typical Application (continued)

9.2.2 Star Application

Multiple TCA9617A A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

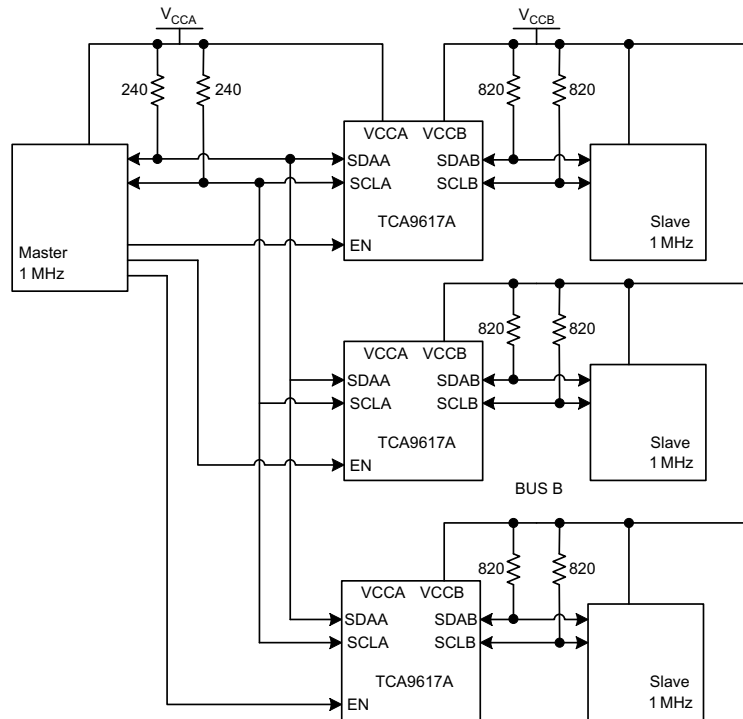**Figure 12. Typical Star Application**

9.2.2.1 Design Requirements

Refer to *Design Requirements*.

9.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.2.3 Application Curves

Refer to *Application Curves*.

Typical Application (continued)

9.2.3 Series Application

Multiple TCA9617As can be connected in series as long as the A side is connected to the B side. I^{2}C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.
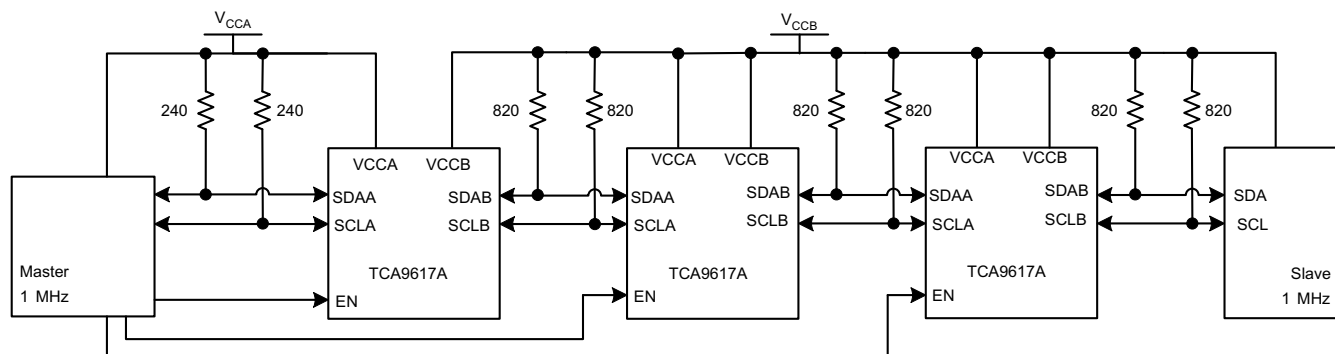
Figure 13. Typical Series Application

9.2.3.1 Design Requirements

Refer to *Design Requirements*.

9.2.3.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.3.3 Application Curves

Refer to *Application Curves*.

10 Power Supply Recommendations

For VCCA, an 0.8-V to 5.5-V power supply is required. For VCCB, a 2.2-V to 5.5-V power supply is required.

VCCB should always be higher than VCCA. VCCB cannot be lower than VCCA even when the device is disabled. During power-up, VCCB must rise before VCCA.

Standard decoupling capacitors are recommended. These capacitors typically range from 0.1 µF to 1 µF, but the ideal capacitance depends on the amount of noise from the power supply.

11 Layout

11.1 Layout Guidelines

The recommended decoupling capacitors should be placed as close to the VCCA and VCCB pins of the TCA9617A as possible.

11.2 Layout Example

Figure 14. Layout Schematic

Product Folder Links: *TCA9617A*

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

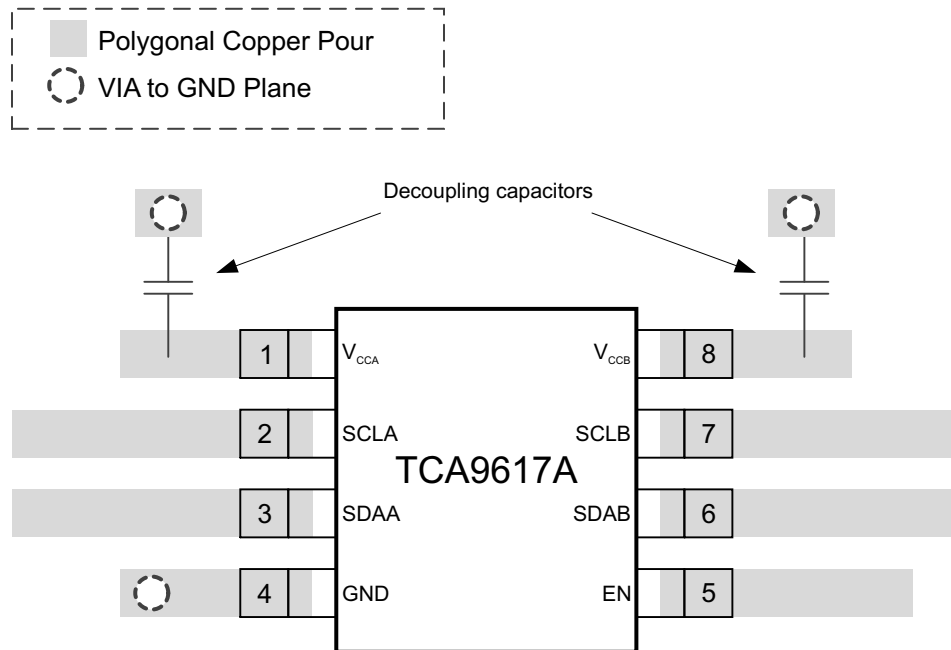To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert* me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.
    This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9617ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 85	(7EA, DWK)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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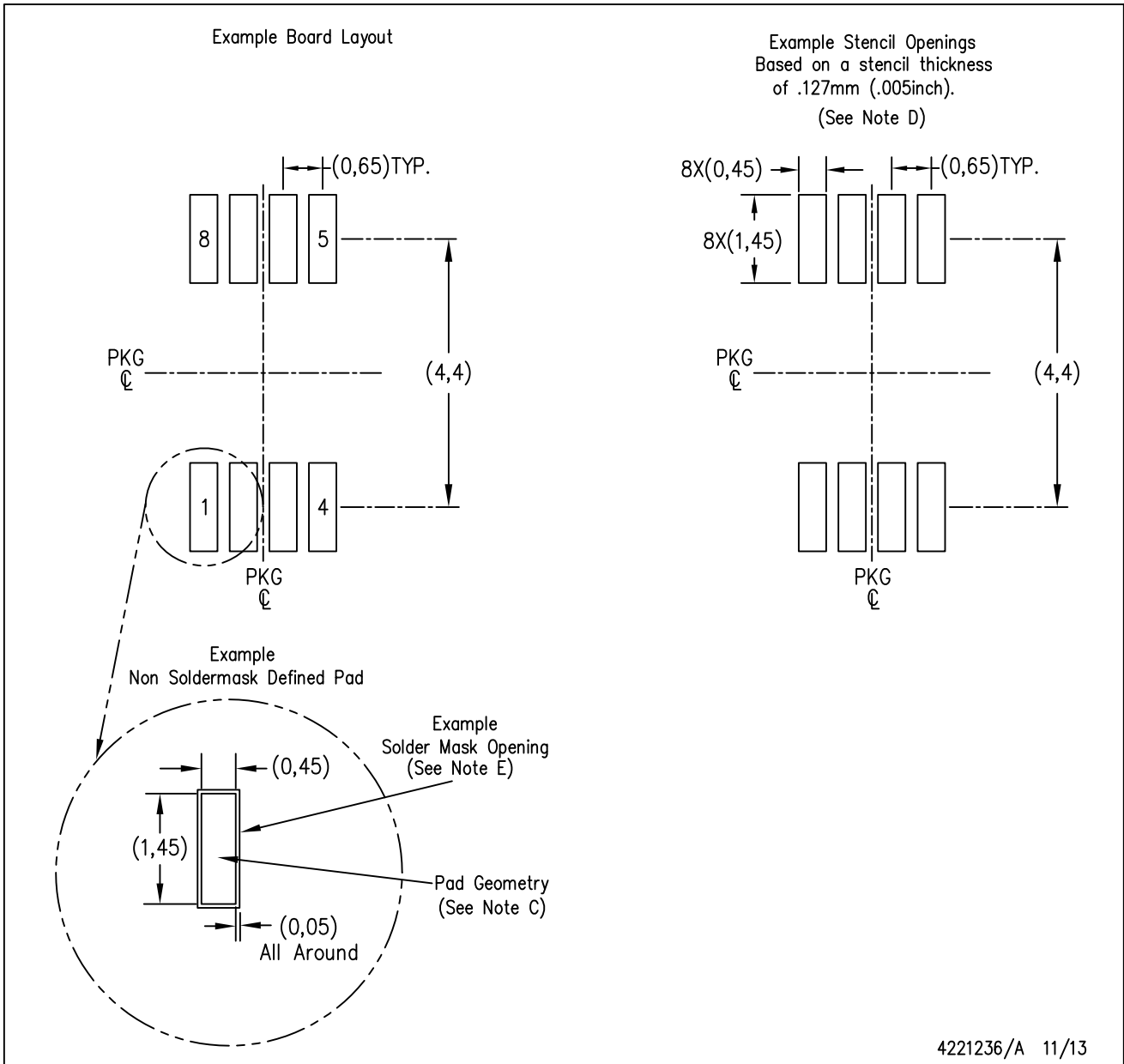
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0,65

8

0,38
0,25

⊕ 0,13 Ⓜ

5

3,10
2,90

5,05
4,75

1

4

3,10
2,90

1,10 MAX

0,15
0,05

0,23
0,13

Gauge Plane

0,25

0°−8°

0,70
0,40

Seating Plane

⌒ 0,10

4073329/E 05/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.15 per end.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
         E.   Falls within JEDEC MO−187 variation AA, except interlead flash.

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DGK (S–PDSO–G8)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

(0,65)TYP.

8   5

8X(0,45)   (0,65)TYP.

8X(1,45)

PKG
℄

(4,4)

PKG
℄

(4,4)

1   4

PKG
℄

PKG
℄

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

(0,45)

(1,45)

Pad Geometry
(See Note C)

(0,05)
All Around

4221236/A 11/13

NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Publication IPC–7351 is recommended for alternate designs.
           D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
                contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
           E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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