UCC25600 8-Pin High-Performance Resonant Mode Controller

1 Features

- Variable Switching Frequency Control
- Programmable Minimum Switching Frequency With 4% Accuracy (3% Accuracy at Temperature Range: –20°C to 105°C)
- Programmable Maximum Switching Frequency
- Programmable Dead Time for Best Efficiency
- Programmable Soft-Start Time
- Easy ON and OFF Control
- Overcurrent Protection
- Overtemperature Protection
- Bias Voltage UVLO and Overvoltage Protection
- Integrated Gate Driver With 0.4-A Source and 0.8-A Sink Capability
- Operating Temperature Range: –40°C to 125°C
- SOIC 8-Pin Package

2 Applications

- 100-W to 1-kW Power Supplies
- LCD, Plasma, and DLP® TVs
- Adaptors, Computing, and ATX Power Supplies
- Home Audio Systems
- Electronic Lighting Ballasts

3 Description

The UCC25600 high performance, resonant mode controller is designed for dc-to-dc applications using resonant topologies, especially the LLC half-bridge resonant converter. This highly integrated controller implements frequency modulation control and complete system functions in only an 8-pin package. Switching to the UCC25600 will greatly simplify the system design and layout, and improve time to market, all at a price point lower than competitive 16-pin device offerings.

The internal oscillator supports the switching frequencies from 40 kHz to 350 kHz. This high-accuracy oscillator realizes the minimum switching frequency limiting with 4% tolerance, allowing the designer to avoid over-design of the power stage and, thus, further reducing overall system cost. The programmable dead time enables zero-voltage switching with minimum magnetizing current. This maximizes system efficiency across a variety of applications. The programmable soft-start timer maximizes design flexibility demanded by the varied requirements of end equipment using a half-bridge topology. By incorporating a 0.4-A source and 0.8-A sink driving capability, a low cost, reliable gate driver transformer is a real option.

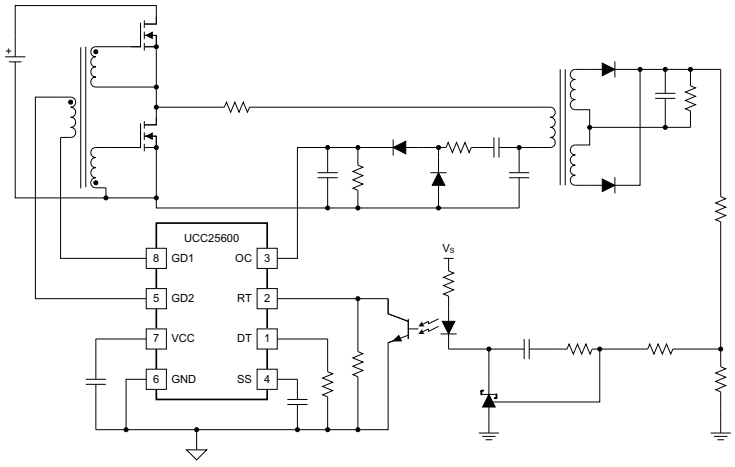
The UCC25600 delivers complete system protection functions including overcurrent, UVLO, bias supply OVP, and overtemperature protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC25600	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2011) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision A (September 2008) to Revision B — **Page**

- Changed Operating Temperature Range to match the Electrical Specifications. ... 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View

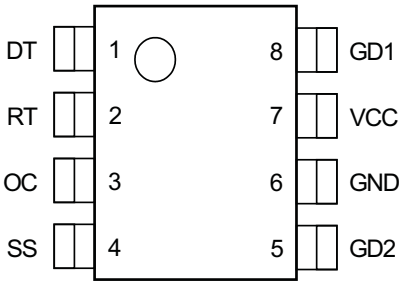


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DT	1	I	This pin sets the dead time of high-side and low-side switch driving signals. Connect a resistor to ground. With internal 2.25-V voltage reference, the current flowing through the resistor sets the dead time. To prevent shoot through when this pin is accidentally shorted to ground, the minimum dead time is set to 120 ns. Any dead time setting less than 120 ns will automatically have 120-ns dead time.
GD1	8	O	High-side and low-side switch gate driver. Connect gate driver transformer primary side to these two pins to drive the half-bridge.
GD2	5		
GND	6	–	Ground
OC	3	I	Overcurrent protection pin. When the voltage on this pin is above 1 V, gate driver signals are actively pulled low. After the voltage falls below 0.6 V, the gate driver signal recovers with soft-start. When OC pin voltage is above 2 V, the device is latched off. Bringing VCC below the UVLO level resets the overcurrent latch to off.
RT	2	I	The current flowing out of this pin sets the frequency of the gate driver signals. Connect the opto-coupler collector to this pin to control the switching frequency for regulation purposes. Parallel a resistor to ground to set the minimum current flowing out of the pin and set the minimum switching frequency. To set the maximum switching frequency limiting, simply series a resistor with the opto-coupler transistor. This resistor sets the maximum current flowing out of the pin and limits the maximum switching frequency.
SS	4	I	Soft-start pin. This pin sets the soft-start time of the system. Connect a capacitor to ground. Pulling this pin below 1 V will disable the device to allow easy ON/OFF control. The soft-start function is enabled after all fault conditions, including bias supply OV, UVLO, overcurrent protection, and overtemperature protection.
VCC	7	–	Bias Supply. Connect this pin to a power supply less than 20 V. Parallel a 1-µF capacitor to ground to filter out noise.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, VCC		22	V
Voltage, GD1, GD2	–0.5	VCC + 0.5	V
Gate drive current – continuous, GD1, GD2		±25	mA
Current, RT		–5	mA
Current, DT		–0.7	mA
Lead temperature (10 seconds)		260	°C
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VCC input voltage from a low-impedance source	11.5		18.0	V
RT resistance	1		8.666	kΩ
DT resistance	3.3		39	kΩ
SS capacitor	0.01		1	µF

6.4 Thermal Information

THERMAL METRIC(1)		UCC25600 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY (VCC)						
	VCC current, disabled	SS = 0 V		1	1.5	mA
	VCC current, enabled	SS = 5 V, C_{GD1} = C_{GD2} = 1 nF	2.5	5	7.5	
	VCC current, UVLO	VCC = 9 V		100	400	µA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC rising	9.9	10.5	11.1	V
	UVLO turn-off threshold	Measured at VCC falling	8.9	9.5	10.1	
	UVLO hysteresis	Measured at VCC	0.7	1	1.3	
V_{OVP}	OVP turn-off threshold	Measured at VCC rising	18	20	22	
	OVP turn-on threshold	Measured at VCC falling	16	18	20	
	OVP hysteresis	Measured at VCC	1.5	2	2.5	
DEAD TIME (DT)						
T_{DT}	Dead time	R_{DT} = 16.9 kΩ	390	420	450	ns
OSCILLATOR						
$F_{SW(min)}$	Minimum switching frequency at GD1, GD2	–40°C to 125°C	40.04	41.70	43.36	kHz
		–20°C to 105°C	40.45	41.70	42.95	
K_{ICO}	Switching frequency gain/I (RT)	R_{RT} = 4.7 kΩ, I_{RT} = 0 to 1 mA	60	80	100	Hz/µA
	GD1, GD2 on time mismatching		–50		50	ns
F_{SW_BM}	Switching frequency starting burst mode	SS = 5 V	300	350	400	kHz
	Switching frequency to come out of burst mode	SS = 5 V	280	330	380	
$F_{SW(start)}$	Switching frequency at soft-start	–40°C to 125°C	122	142.5	162	
		–20°C to 105°C	125	142.5	160	
EXTERNAL DISABLE/SOFT START						
	Enable threshold	Measure at SS rising	1.1	1.2	1.3	V
	Disable threshold	Measured at SS falling	0.85	1	1.1	
	Disable hysteresis	Measured at SS	0.15		0.35	
	Disable prop. delay	Measured between SS (falling) and GD2 (falling)	250	500	750	ns
I_{SS}	Source current on ISS pin	V_{SS} = 0.5 V	–225	–175	–125	µA
	Source current on ISS pin	V_{SS} = 1.35 V	–5.5	–5	–4.5	
PEAK CURRENT LIMIT						
$V_{OC1(off)}$	Level 1 overcurrent threshold – V_{OC} rising		0.9	1	1.1	V
$V_{OC2(off)}$	Level 2 overcurrent latch threshold – V_{OC} rising		1.8	2.0	2.2	
$V_{OC1(on)}$	Level 1 overcurrent threshold – V_{OC} falling		0.5	0.6	0.7	
T_{d_OC}	Propagation delay		60	200	500	ns
I_{OC}	OC bias current	V_{OC} = 0.8 V	–200		200	nA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVE					
GD1, GD2 output voltage high	I_{GD1}, I_{GD2} = −20 mA	9		11	V
GD1, GD2 on resistance high	I_{GD1}, I_{GD2} = −20 mA		12	30	Ω
GD1, GD2 output voltage low	I_{GD1}, I_{GD2} = 20 mA		0.08	0.2	V
GD1, GD2 on resistance low	I_{GD1}, I_{GD2} = 20 mA		4	10	Ω
Rise time GDx	1 V to 9 V, C_{LOAD} = 1 nF		18	35	ns
Fall time GDx	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
GD1, GD2 output voltage during UVLO	VCC = 6 V, I_{GD1}, I_{GD2} = 1.2 mA	0.5		1.75	V
THERMAL SHUTDOWN					
Thermal shutdown threshold			160		°C
Thermal shutdown recovery threshold			140		

6.6 Typical Characteristics

At V_{CC} = 12 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, V_{SS} = 5 V, V_{OC} = 0 V; all voltages are with respect to GND, $T_J = T_A$ = 25°C, unless otherwise noted.

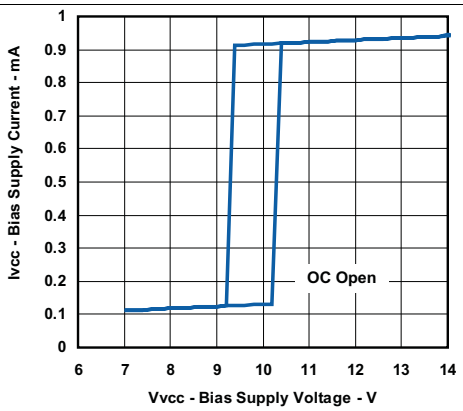


Figure 1. Bias Supply Current vs Bias Supply Voltage

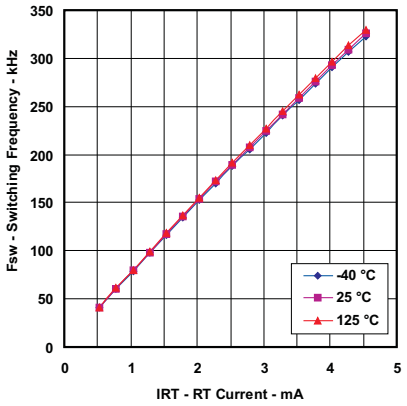


Figure 2. Switching Frequency vs RT Current

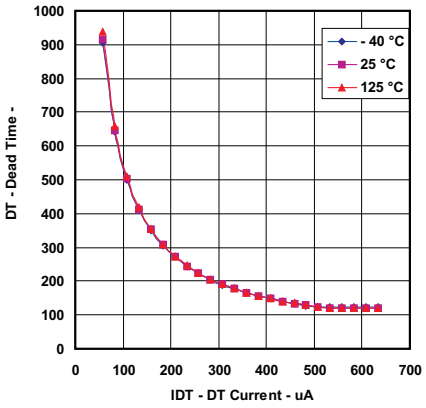


Figure 3. Dead Time vs DT Current

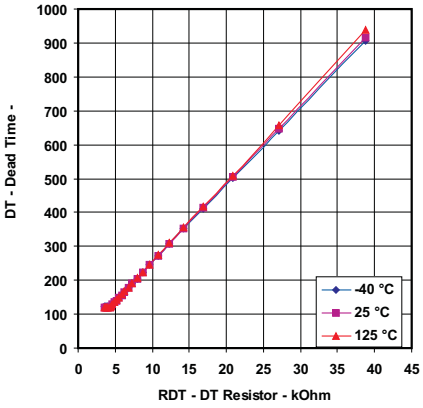


Figure 4. Dead Time vs DT Resistor

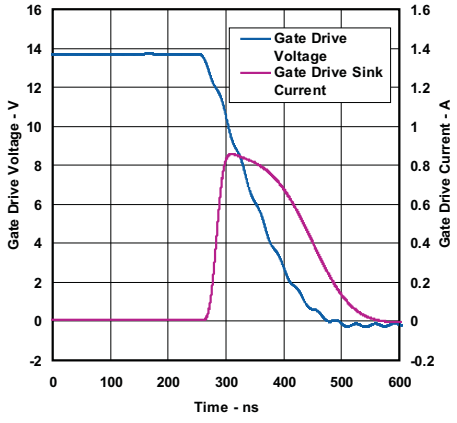


Figure 5. Gate Drive Falling, VCC = 15 V

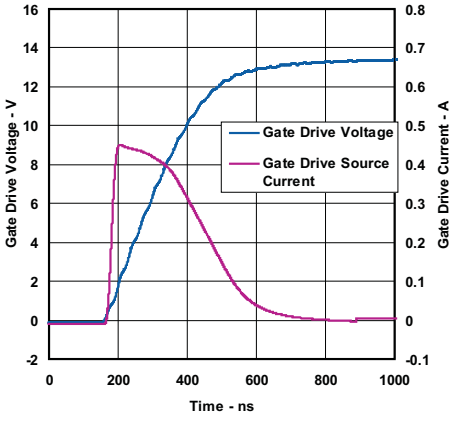


Figure 6. Gate Drive Rising, VCC = 15 V

Typical Characteristics (continued)

At V_{CC} = 12 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, V_{SS} = 5 V, V_{OC} = 0 V; all voltages are with respect to GND, $T_J = T_A$ = 25°C, unless otherwise noted.

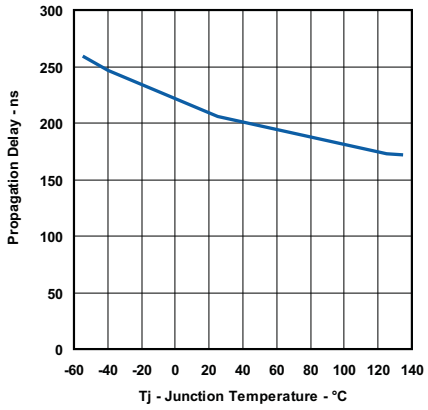


Figure 7. Overcurrent Propagation Delay vs Temperature

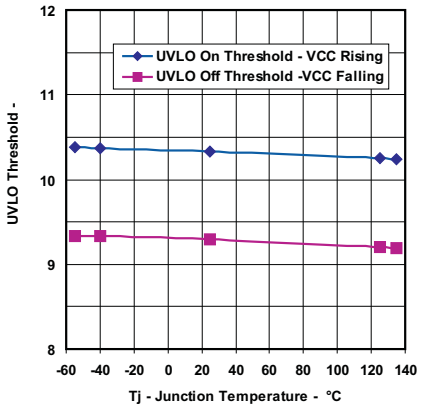


Figure 8. UVLO Threshold vs Temperature

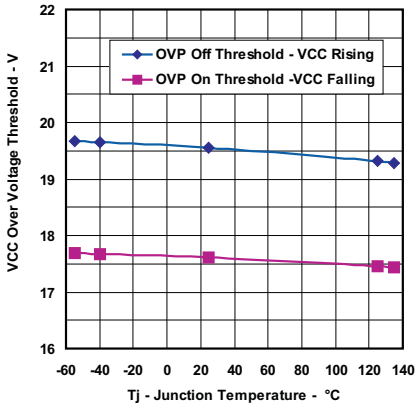


Figure 9. VCC Overvoltage Threshold vs Temperature

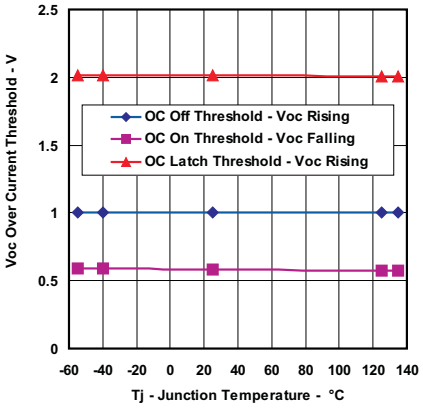


Figure 10. Overcurrent Threshold vs Temperature

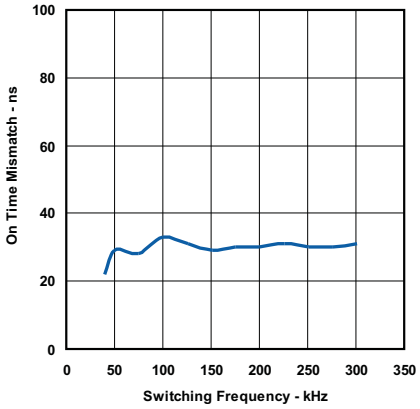


Figure 11. On-time Mismatch vs Switching Frequency

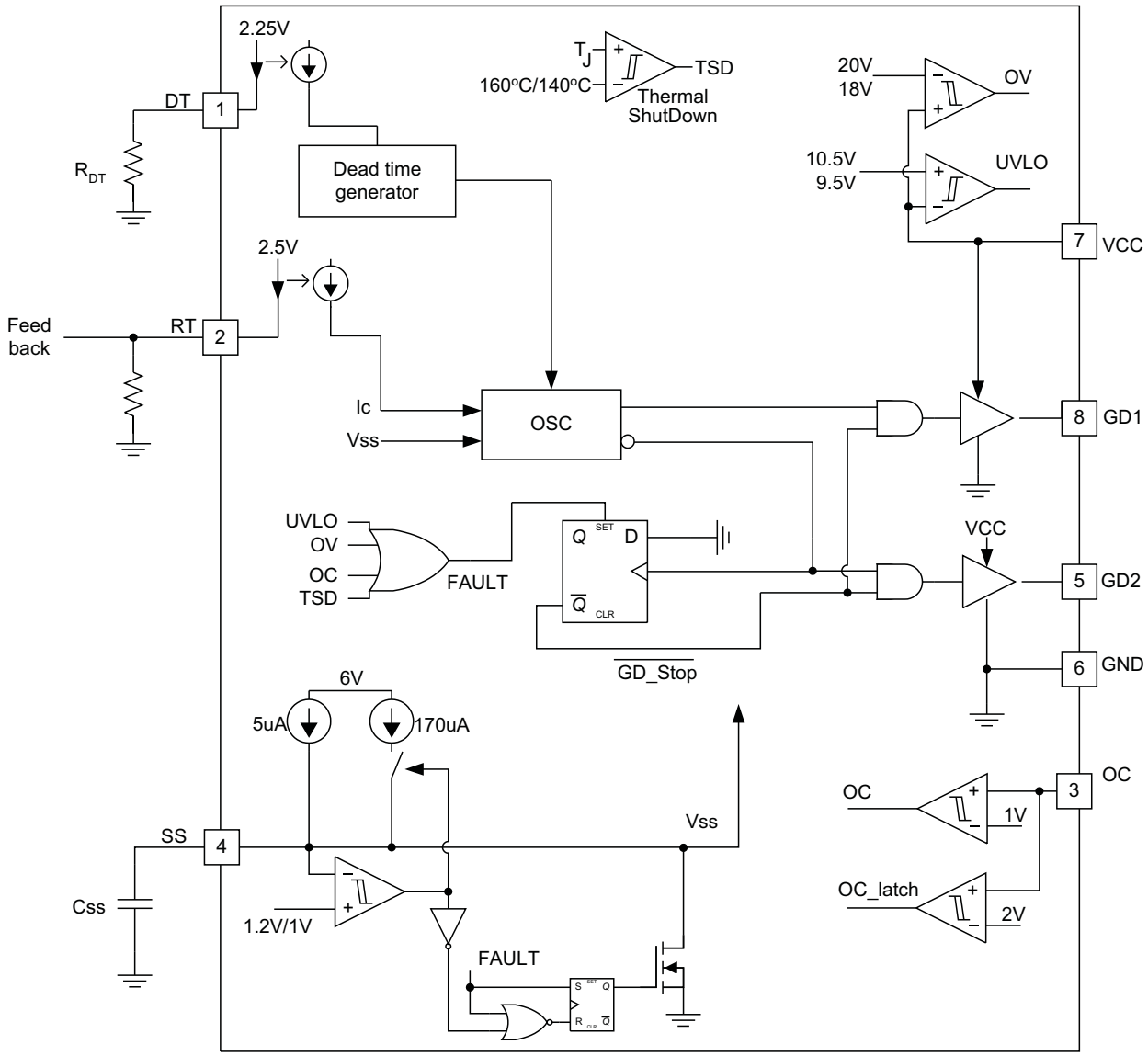
7 Detailed Description

7.1 Overview

Due to high power density and high efficiency requirements, LLC topology is employed in many applications. The LLC resonant converter has many unique characteristics and improvements compared with hard-switch bridge topology and phase-shift full bridge. For example, LLC has a simple structure, and could achieve primary MOSFET zero voltage switching (ZVS) and the secondary rectifier zero current switching (ZCS) from no load to full load.

The UCC25600 device is an LLC-resonant half-bridge controller which integrates built-in, state-of-the-art efficiency boost features with high-level protection features to provide cost-effective solutions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start

During start-up and fault recovery conditions, soft start is always implemented to prevent excessive resonant tank current and to ensure zero-voltage switching (ZVS). During soft start, the switching frequency is increased. The soft-start time can be programmed by placing a capacitor from the SS pin to ground.

The soft-start pin also serves as an ON/OFF control pin of the device. By actively pulling the SS pin below 1 V, the device is disabled. When the pulldown is removed, SS pin voltage is increased because of internal charging current. Once the SS pin is above 1.2 V, the device starts to generate a gate-driver signal and enters soft-start mode. The time sequence of soft start is shown in Figure 12.

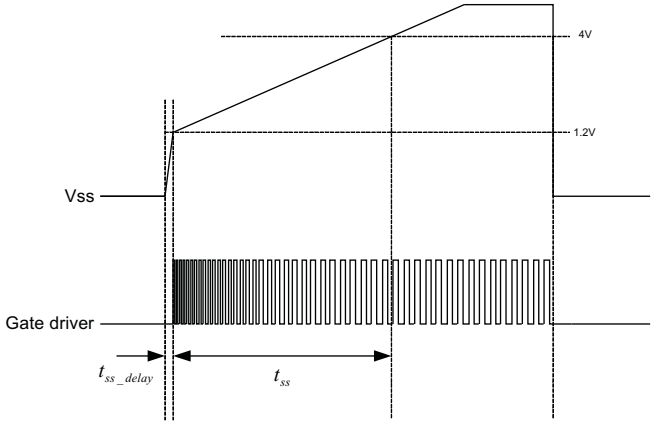


Figure 12. Soft-Start Sequence

To prevent a long delay between the ON command and appearance of a gate driver signal, the SS pin current is set as two different levels. When the SS pin voltage is below 1.2 V, its output current is 175 µA. This high current could charge the soft-start pin capacitor to 1.2 V in a short period of time, and reduce the time delay. This time delay can be calculated using following equation:

$$t_{SS\_delay} = \frac{1.2V}{175\mu A} C_{SS} \quad (1)$$

Feature Description (continued)

The switching frequency during soft start is determined by both the current flowing out of the RT pin and the voltage on the SS pin. The switching frequency can be calculated based on the following equation:

$$f_S = \frac{1}{2} \frac{1}{\frac{6ns \times 1A}{I_{RT} + \left(1.81mA - \frac{V_{SS}}{2.2k\Omega}\right)} + 150ns} \quad (2)$$

After the SS pin voltage reaches 4 V, the soft-start period is finished and switching frequency becomes the same as demanded by the RT pin current. The time used to charge the SS pin from 1.2 V to 4 V is defined as soft-start time and can be calculated as:

$$t_{SS} = \frac{2.8V}{5\mu A} C_{SS} \quad (3)$$

To ensure reliable operation, the gate drivers restart with GD2 turning high. This prevents uncertainty during system start up.

7.3.2 Overcurrent Protection

To prevent power stage failure under excessive load current condition, the UCC25600 includes an overcurrent protection function. With a dedicated OC pin, the power stage is shut down when OC pin voltage is above 1 V. Once the OC pin voltage becomes lower than 0.6 V, the gate driver recovers with a soft start. To enhance system safety, the UCC25600 latches up the whole system when the OC pin becomes above 2 V. Bring VCC below the UVLO level to reset the device.

The current can be indirectly sensed through the voltage across the resonant capacitor by using the sensing network shown in Figure 13.

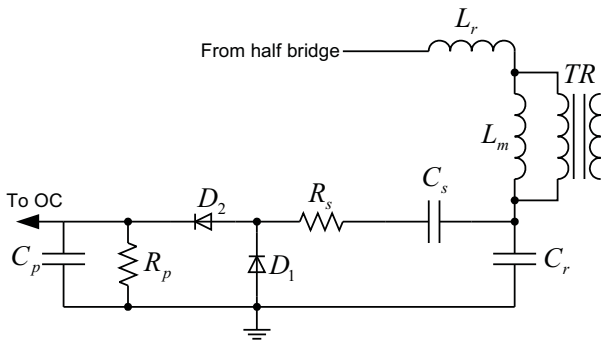


Figure 13. Current Sensing for LLC Resonant Converter

The general concept of this sensing method is that the ac voltage across the resonant capacitor is proportional to load current.

According to the FHA model, peak voltage of the ac component on the resonant capacitor can be calculated as:

$$V_{Cr\_pk} = \frac{4}{\pi} n V_o \left| \frac{j f_n L_n Q_e + 1}{f_n^2 L_n} \right| \quad (4)$$

Therefore, the resonant capacitor voltage reaches its maximum value at the minimum switching frequency and maximum load. According to this equation, the current sensing network components can be calculated. Due to the nature of FHA, the final circuit parameters need to be verified through actual hardware test.

Feature Description (continued)

Table 2. Calculated Current Sensing Network Components

NAME	FUNCTION	DESIGN EQUATION
R_S	Transfer ac voltage across resonant capacitor into current source	$R_s = \frac{V_{Cr\_pk}(max)^2}{2P_{Rs}(max)}$ (5)
C_S	Blocking dc voltage on resonant capacitor	$C_s = \frac{10}{R_s f_{\min}}$ (6)
R_P	Load resistor of the current source	$R_p = \frac{R_s}{V_{Cr\_pk}(max)}\pi$ (7)
C_P	Filter capacitor	$C_p = \frac{10}{R_p f_{\min}}$ (8)

7.3.3 Gate Driver

The half-bridge resonant converter is controlled by the nearly 50% duty-cycle variable frequency square-wave voltage. This allows the half bridge to be easily driven by the gate-driver transformer. Compared with a half-bridge driver device, a gate-driver transformer provides a simple and reliable solution, which:

- Eliminates the need for gate driver power supply
- Enables simplified layout
- Prevents shoot-through due to the transformer coupling
- Requires no latch up

The UCC25600 integrates two-gate drivers with 0.4-A source and 0.8-A sink capability to directly drive the gate-driver transformer.

For the LLC resonant converter, it is critical for the gate-driver signal to be precisely symmetrical. Otherwise, the resonant tank operation will be symmetrical. The load current distribution will be unbalanced for the output rectifiers, which in turn require the over-design of the power stages and thermal management.

In UCC25600, the gate-driver output is precisely trimmed to have less than 50-ns mismatch. Although the gate-driver signal is quite symmetrical, it is still recommended to insert the dc blocking capacitor in the gate-driver transformer primary side to prevent transformer saturation during fast transients.

7.3.4 Overtemperature Protection

UCC25600 continuously senses its junction temperature. When its junction temperature rises above 160°C, the device will enter overtemperature protection mode with both gate drivers actively pulled low. When junction temperature drops below 140°C, gate driver restarts with soft start.

7.4 Device Functional Modes

7.4.1 Burst-Mode Operation

During light load condition, the resonant converter tends to increase its switching frequency and maintain the output voltage regulation. However, due to ringing caused by the transformer parasitic capacitor and the rectification-diode-junction capacitors, the energy could be directly transferred to the load through these capacitors. When this power becomes more than the load requires, the output voltage become higher than the regulation level. In this case, further increasing the switching frequency will not help the situation because energy transfer to the load is not through the power stage itself.

To prevent output overvoltage during this condition, the UCC25600 includes the burst-mode operation function. When the control loop demands switching frequency higher than 350 kHz, the gate driver is disabled and the power stage stops switching. When the output voltage drops, the control loop begins to demand switching frequency less than 330 kHz, the gate driver recovers and the power stage begins to deliver power again. This allows the output voltage to be regulated.

This burst mode can be easily disabled by limiting the maximum switching frequency to less than 350 kHz. In this way, the control loop will never demand a switching frequency higher than 350 kHz and burst mode operation will not occur.

7.4.2 VCC

When VCC becomes above 10.5 V, the device is enabled and, after all fault conditions are cleared, the gate driver starts with soft start. When VCC drops below 9.5 V, the device enters the UVLO protection mode and both gate drivers are actively pulled low. When VCC rises above 20 V, the device enters VCC overvoltage protection mode and the device is disabled with both gate drivers actively pulled low. The VCC overvoltage protection will recover with soft start when the VCC voltage returns below 18 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC25600 device is a high performance, resonant-mode controller designed for DC/DC applications using resonant topologies, especially the LLC half-bridge resonant converter.

8.1.1 Principal of Operation

The soft-switching capability, high efficiency, and long holdup time make the LLC resonant converter attractive for many applications, such as digital TV, ac-to-dc adapters, and computer power supplies. Figure 14 shows the schematic of the LLC resonant converter.

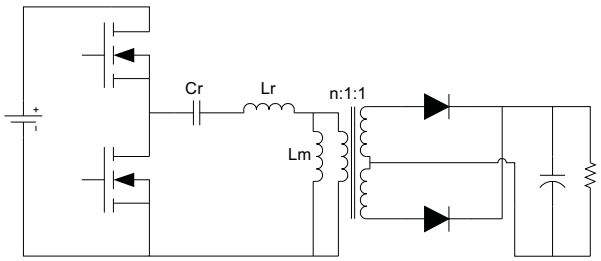


Figure 14. LLC Resonant Converter

The LLC resonant converter is based on the series resonant converter (SRC). By using the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than resonant frequency. This simplifies the converter design to avoid the zero-current switching region which can lead to system damage. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered, the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage, boost PFC pre-regulator, allowing it to hold up through brief periods of ac line-voltage dropout.

Due to the nature of resonant converter, all the voltages and currents on the resonant components are approximately sinusoidal. The gain characteristic of the LLC resonant converter is analyzed based on the first harmonic approximation (FHA), which means all the voltages and currents are treated as a sinusoidal shape with the frequency the same as the switching frequency.

According to the operation principle of the converter, the LLC resonant converter can be drawn as the equivalent circuit shown in Figure 15.

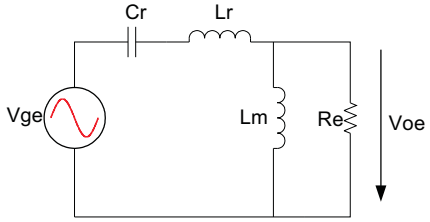


Figure 15. LLC Resonant Converter Equivalent Circuit

Application Information (continued)

In this equivalent circuit, the V_{ge} and V_{oe} are the fundamental harmonics of the voltage generated by the half-bridge and the voltage on the transformer primary side, respectively. These voltages can be calculated through Fourier analysis. The load resistor R_e is the equivalent resistor of the load, and it can be calculated as:

$$R_e = \frac{8}{\pi^2} n^2 R \tag{9}$$

Based on this equivalent circuit, the converter gain at different switching frequencies can be calculated as:

$$\frac{V_o}{V_{DC}/2} = \left| \frac{\frac{j\omega L_m R_e}{j\omega L_m + R_e}}{\frac{j\omega L_m R_e}{j\omega L_m + R_e} + \frac{1}{j\omega C_r} + j\omega L_r} \right| \tag{10}$$

In this equation $V_{DC}/2$ is the equivalent input voltage due to the half-bridge structure.

Table 3. Circuit Definition Calculations

NORMALIZED GAIN	RESONANT FREQUENCY	QUALITY FACTOR	NORMALIZED FREQUENCY	INDUCTOR RATIO
$M = \frac{V_o}{V_{DC}/2}$ (11)	$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$ (12)	$Q_e = \frac{\sqrt{L_r / C_r}}{R_e}$ (13)	$f_n = \frac{f}{f_0}$ (14)	$L_n = \frac{L_m}{L_r}$ (15)

Following the definitions in Table 3, the converter gain at different switching frequencies can be written as:

$$M = \left| \frac{L_n \times f_n^2}{\left[(L_n + 1) \times f_n^2 - 1\right] + j\left[(f_n^2 - 1) \times f_n \times Q_e \times L_n\right]} \right| \tag{16}$$

Because of the FHA, this gain equation is an approximation. When the switching frequency moves away from the resonant frequency, the error becomes larger. However, this equation can be used as a design tool. The final results need to be verified by the time-based simulation or hardware test.

From Equation 16, when the switching frequency is equal to the resonant frequency, f_n = 1 and converter voltage gain is equal to 1. Converter gain at different loads and inductor ratio conditions are shown in Figure 16 through Figure 19.

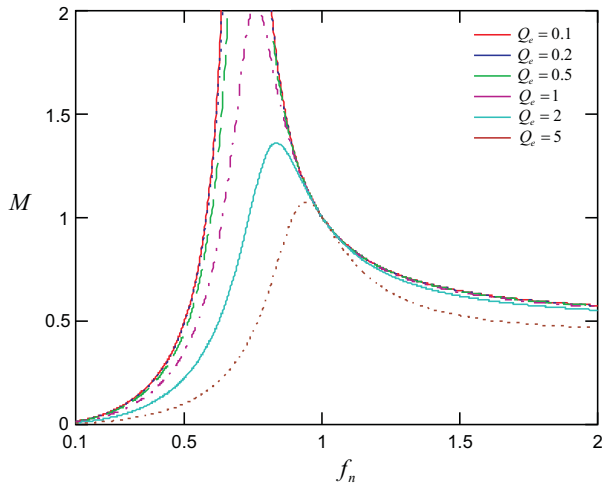


Figure 16. M vs f_N

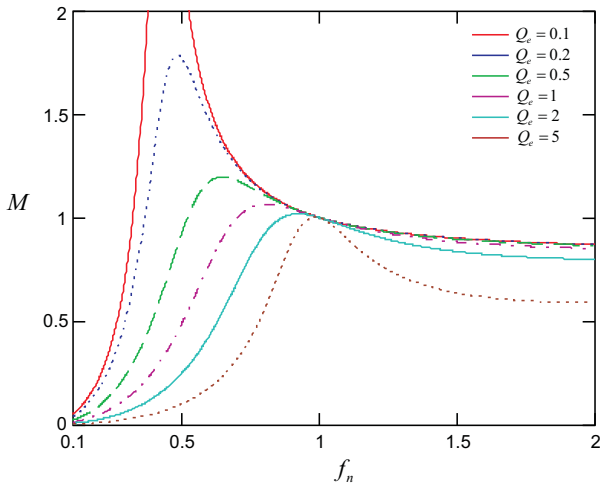


Figure 17. M vs f_N

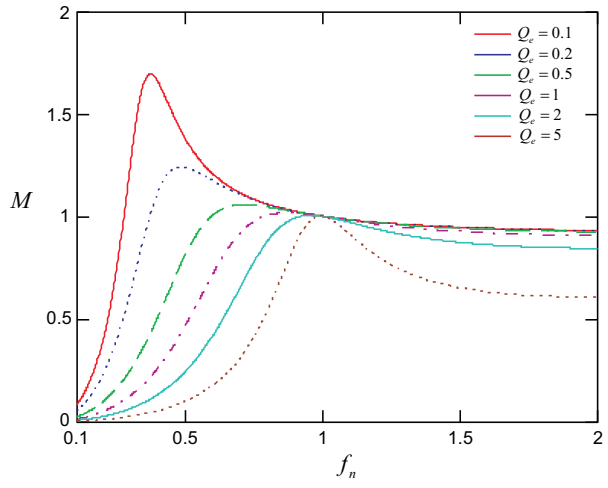


Figure 18. M vs f_N

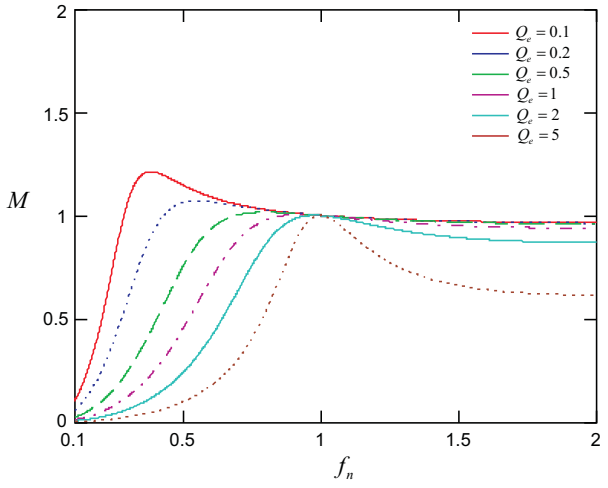


Figure 19. M vs f_N

Based on its theory of operation, the LLC resonant converter is controlled through pulse frequency modulation (PFM). The output voltage is regulated by adjusting the switching frequency according to the input and output conditions. Optimal efficiency is achieved at the nominal input voltage by setting the switching frequency close to the resonant frequency. When the input voltage drops low, the switching frequency is decreased to boost the gain and maintain regulation.

The UCC25600 resonant half-bridge controller uses variable switching frequency control to adjust the resonant tank impedance and regulate output voltage. This 8-pin package device integrates the critical functions for optimizing the system performance while greatly simplifying the design and layout.

8.1.2 Adjustable Dead Time

Resonant half-bridge converter relies on the resonant tank current at MOSFETs turn-off to achieve soft switching and reduce switching loss. Higher turn-off current provides more energy to discharge the junction capacitor, while it generates more turn-off loss. Smaller turn-off current reduces turn-off loss, but it requires longer time to discharge MOSFETs junction capacitors and achieve soft switching. By choosing an appropriate dead time, turn-off current is minimized while still maintaining zero-voltage switching, and best system performance is realized.

In UCC25600, dead time can be adjusted through a single resistor from the DT pin to ground. With internal 2.25-V voltage reference, the current flow through the resistor sets the dead time.

$$t_d = 20ns + R_{dt} \times 24ns / k\Omega \tag{17}$$

To prevent shoot through when the DT pin accidentally connects to ground, a minimum 120-ns dead time is inserted into the 2 gate driver outputs. Any dead-time setting less than 120 ns will be limited to 120 ns.

8.1.3 Oscillator

With variable switching frequency control, UCC25600 relies on the internal oscillator to vary the switching frequency. The oscillator is controlled by the current flowing out of the RT pin. Except during soft start, the relationship between the gate signal frequency and the current flowing out of the RT pin can be represented as:

$$f_S = \frac{1}{2} \frac{1}{\frac{6ns \times 1A}{I_{RT}} + 150ns} \approx I_{RT} \times 83Hz / \mu A \tag{18}$$

Because the switching frequency is proportional to the current, by limiting the maximum and minimum current flowing out of the RT pin, the minimum and maximum switching frequency of the converter could be easily limited. As shown in Figure 20, putting a resistor from the RT pin to ground limits the minimum current and putting a resistor in series with the opto-coupler limits the maximum current.

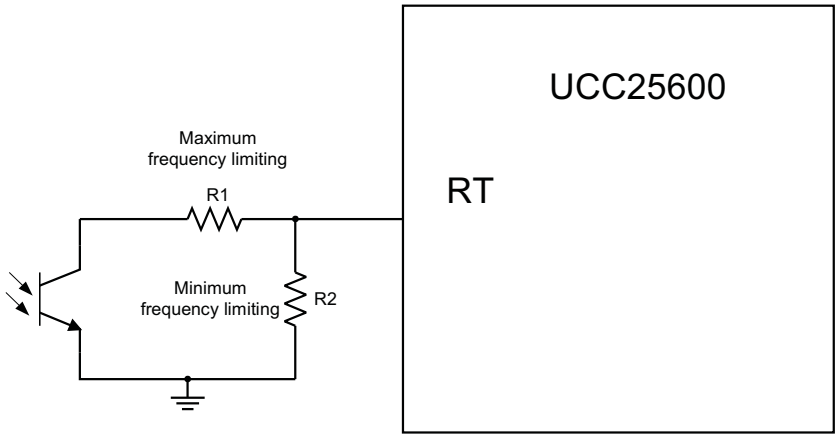


Figure 20. Maximum and Minimum Frequency Setting for UCC25600

The frequency limiting resistor can be calculated based on following equations.

$$I_{f\,max} = \frac{6ns}{\frac{1}{2f_{max}} - 150ns} \tag{19}$$

$$I_{f\,min} = \frac{6ns}{\frac{1}{2f_{min}} - 150ns} \tag{20}$$

$$I_{f\,max} = 2.5V\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{21}$$

$$I_{f\,min} = \frac{2.5V}{R_2} \tag{22}$$

8.2 Typical Application

This design example describes the HPA341 EVM design and outlines the design steps required to design a 300-W LLC resonant half-bridge converter, which provides a regulated output voltage nominally at 12 V at maximum 300 W of load power, with reinforced isolation of AC-DC off-line applications between the primary and the secondary, operating from a DC source of 390 V.

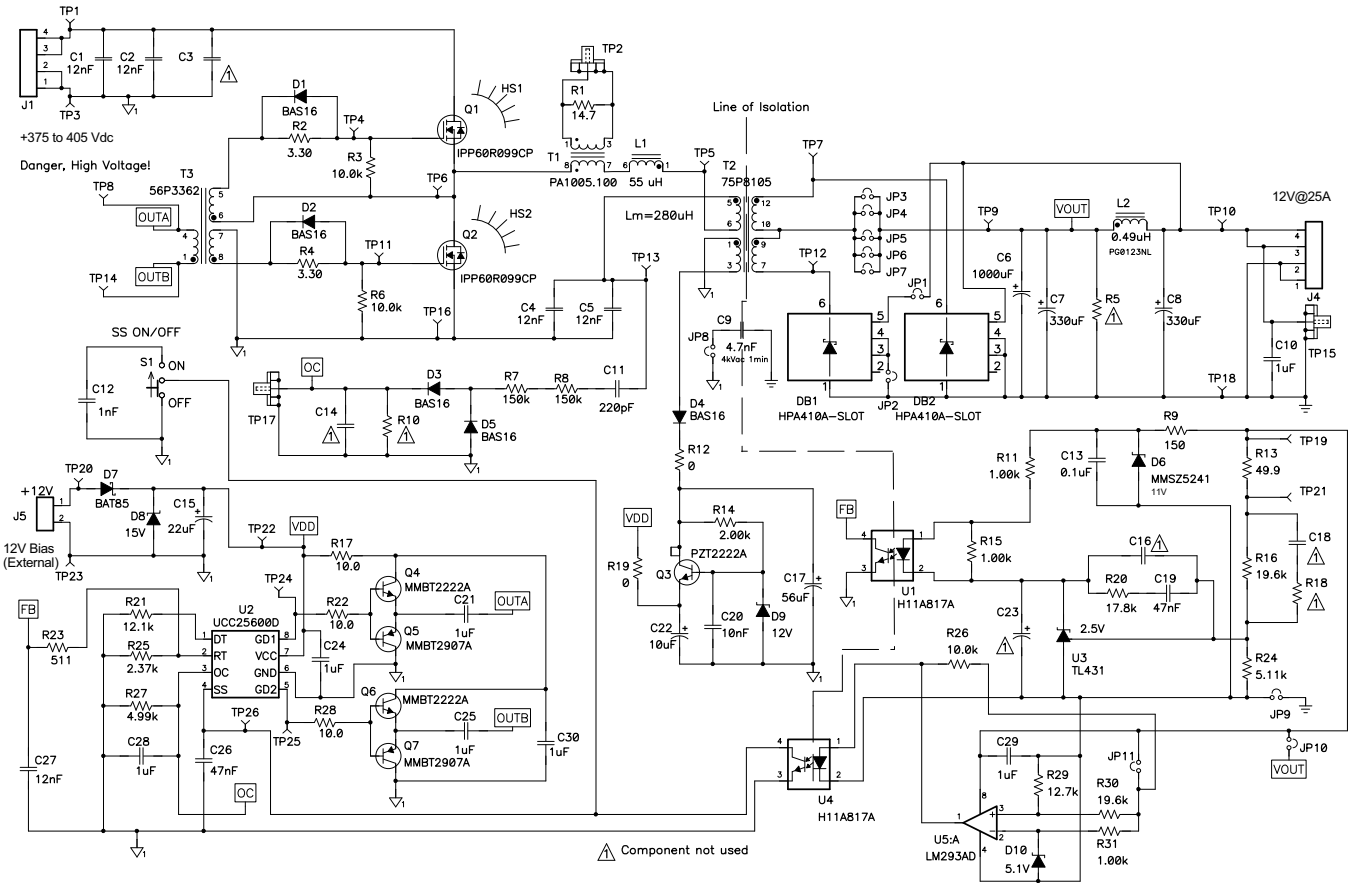


Figure 21. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 4. Design Requirements

DESIGN PARAMETER	TARGET VALUE
Output voltage	12 V
Rated output power	300 W
Input DC voltage range	375 V to 405 V
Typical efficiency at full load	91%
Switching frequency	85 kHz to 350 kHz
Resonant frequency	130 kHz

8.2.2 Detailed Design Procedure

1. Resonant inductor(Lr), resonant capacitor(Cr), and (Lm) of half-bridge LLC
   (a) Turns ratio of Main transformer:
   $n = Np/Ns = 16.5$ (23)
   (b) Maximum resonant gain required:
   $M\_max = 110\% \times n \times (2 \times Vout)/(Vin\_min) = 110\% \times 16.5 \times (2 \times 12\ V)/375\ V = 1.17$ (24)
   (c) Choose Ln and Q. The Ln range is typically selected from 3 to 9. Choose Q based on the curves below, where the peak gain must be higher than or equal to the maximum resonant gain required. Based on the below curves, Q selects 0.45.
   $Ln = Lm/Lr = 5$ (25)
   $Q = \sqrt{(Lr / Cr)} / Req = 0.45$ (26)

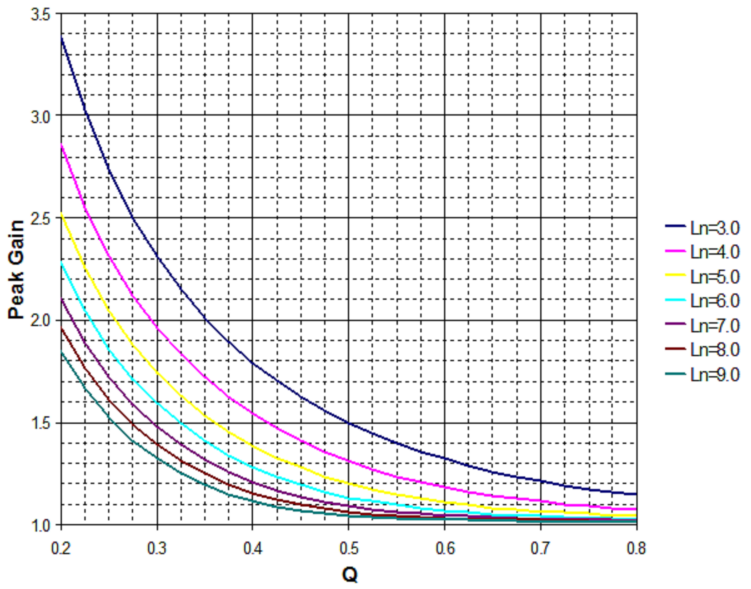


Figure 22. Peak Gain vs Q

   (d) Calculate equivalent primary resistance:
   $Req = (8 \times n^2 \times Vout^2)/(\pi^2 \times Pout) = (8 \times 4.6^2 \times 12^2)/(\pi^2 \times 300) = 108.6\Omega$ (27)
   (e) Select Cr:
   $Cr = 24nF$ (28)
   (f) Calculate Lr:

$$fr = \frac{1}{2\pi \times \sqrt{Lr \times Cr}} \quad (29)$$

(g) Combine the above two equations:

$$Lr = 55\mu H \quad (30)$$

(h) Calculate Lm:

$$Lm = Ln \times Lr = 275\ \mu H \quad (31)$$

2. Calculate Rdt. In the UCC25600, dead time can be adjusted through a single resistor from DT pin to ground. With an internal 2.25-V voltage reference, the current flow through the resistor sets the dead time.

   $td = 20ns + Rdt \times 24ns/k\Omega$

   where
   - td = 300 ns
   - Rdt = 11.7 kΩ (32)

3. Calculate C_{SS}. Refer to *Soft Start* for more details.

   $tss = 25\ ms$ (33)

   $tss = 2.8\ V/5\ \mu A \times Css$ (34)

   $Css = 44.6\ nF$ (35)

4. A 47nF capacitor is selected. Calculate RT1 and RT2. Refer to *Oscillator* for more details. RT1 and RT2 are used to limit maximum switching frequency and minimum switching frequency. RT1 and RT2 can be calculated based on following equations:

   $Ifmax = 6\ ns/(1/2fmax - 150\ ns)$ (36)

   $Ifmin = 6\ ns/(1/2fmin - 150\ ns)$ (37)

   $Ifmax = 2.5\ V(1/RT1 + 1/RT2)$ (38)

   $Ifmin = 2.5\ V/RT2$ (39)

5. Combine the four equations above:

   $RT1 = 511\Omega$ (40)

   $RT2 = 2.37\ k\Omega$ (41)

6. Calculate Rs, Cs, Rp, and Cp. Refer to *Overcurrent Protection* for more details.

   $Rs = 300\ k\Omega$ (42)

   $Cs = 22\ pF$ (43)

   $Rp = 4.99\ k\Omega$ (44)

   $Cp = 1\ \mu F$ (45)

8.2.3 Application Curves

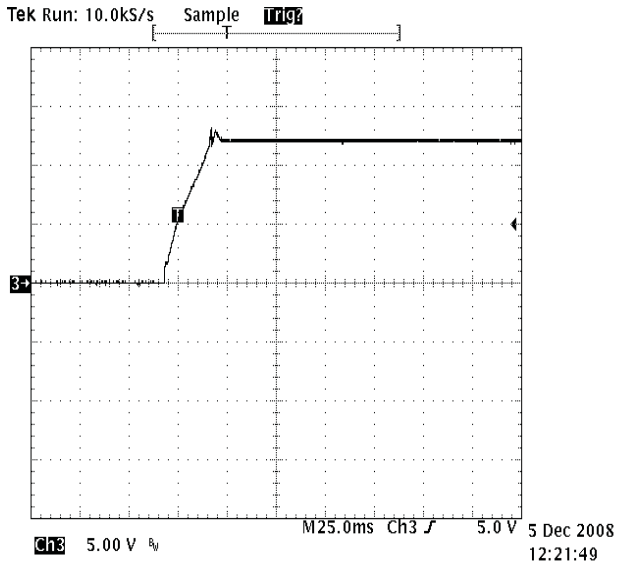


Figure 23. Typical Output Voltage Turn On (TP15)

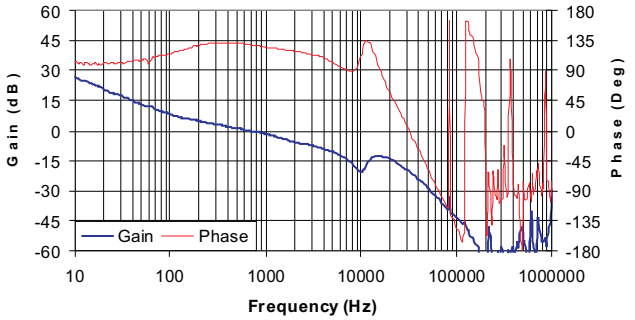


Figure 24. Full System Loop Compensation (TP19 and TP21)

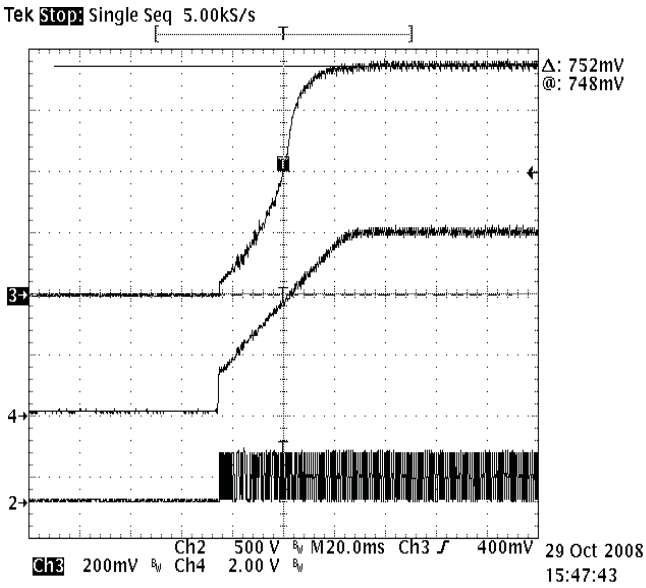


Figure 25. Typical Soft-Start Waveform

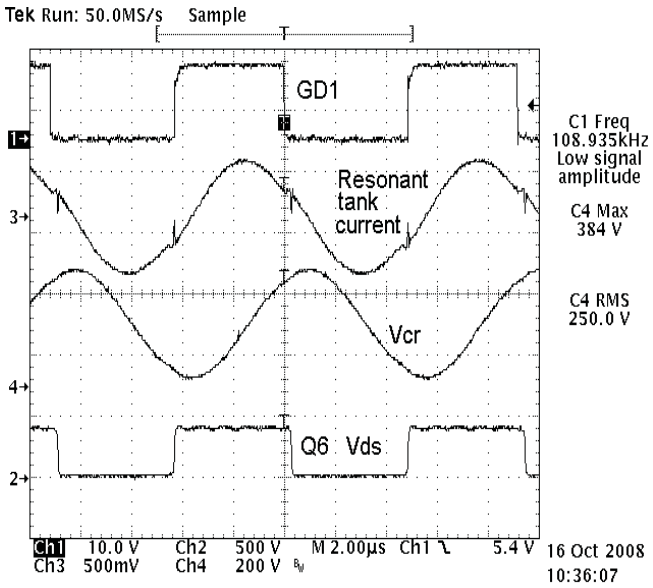


Figure 26. Typical Resonant Tank Current and Resonant Capacitor Voltage

9 Power Supply Recommendations

The VCC power terminal for the device requires the direct placement of low-ESR noise-decoupling capacitance from the VCC terminal to the GND terminal. Ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. Depending on the operating temperature range of the application, X5R may be acceptable, but the drop in capacitance value at high temperature and with applied DC-bias may not be tolerable. Avoid dielectrics with poor temperature stability.

The recommended decoupling capacitor is a 1-µF 0805-sized 50-V X7R capacitor, ideally with (but not essential) a second, smaller, parallel 100-nF 0603-sized 50-V X7R capacitor. Higher voltage-rated parts can also be used. The use of 25-V rated parts is not recommended, due to reduction in effective capacitance value with applied DC bias.

10 Layout

10.1 Layout Guidelines

Four-layer layout is recommended

A 1-µF ceramic decoupling capacitor is recommended, to be placed as close as possible between the VCC terminal and GND, and tracked directly to both terminals.

Place C_{SS}, RDT, Rp, Cp, RT1, and RT2 as close as possible to the UCC25600.

Connect a regulated bias supply to the VCC pin.

10.2 Layout Example

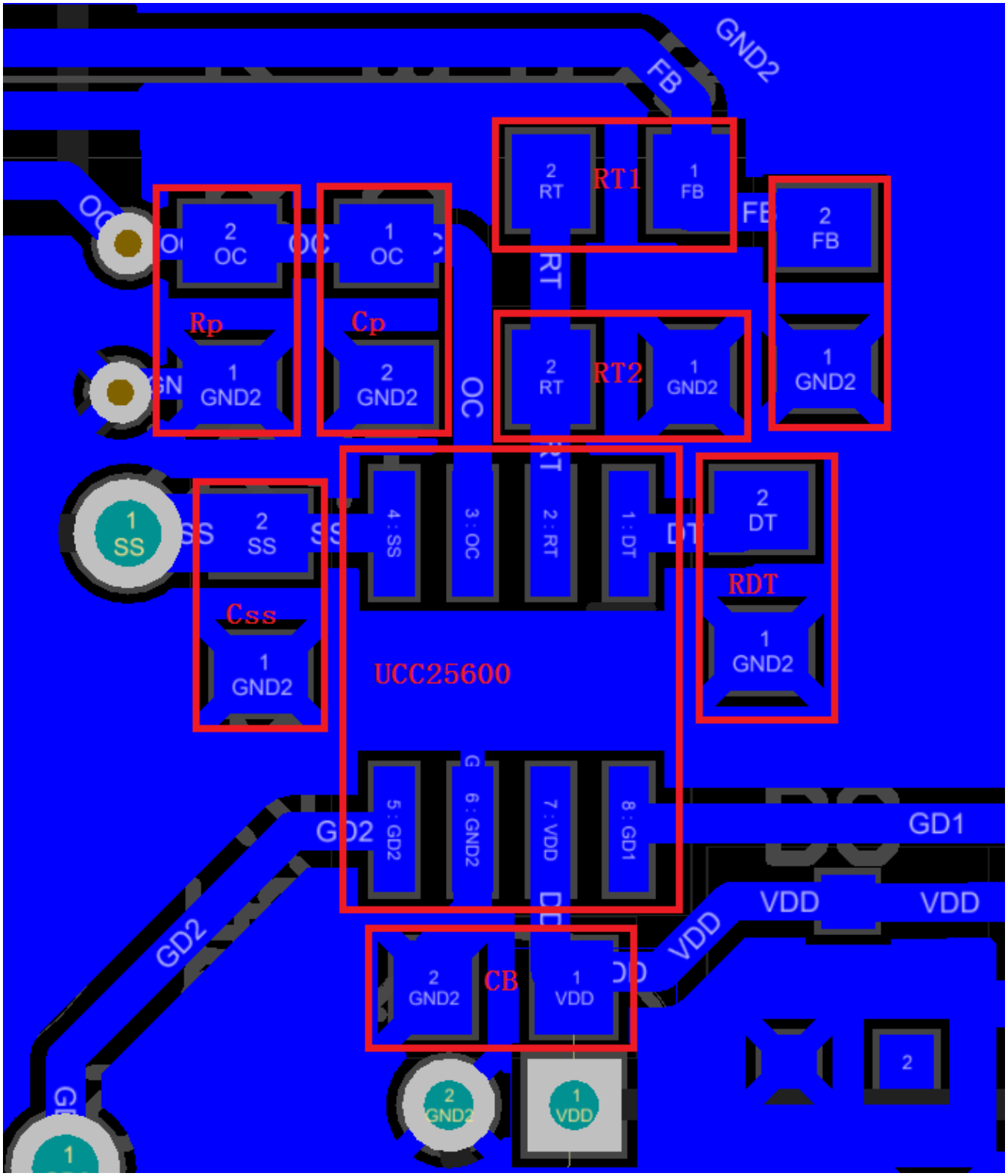


Figure 27. Board Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
is a registered trademark of ~Texas Iinstruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC25600D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25600	Samples
UCC25600DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25600	Samples
UCC25600DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25600	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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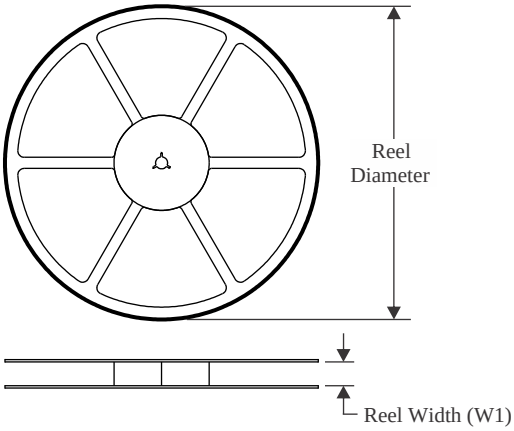
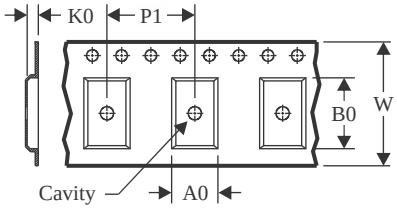
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

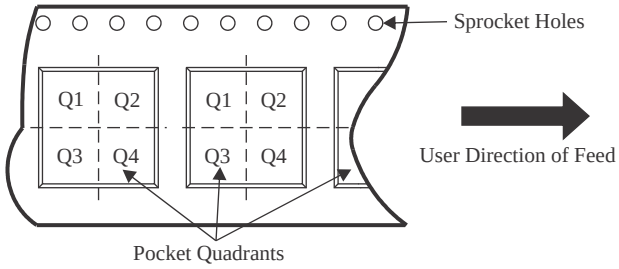


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

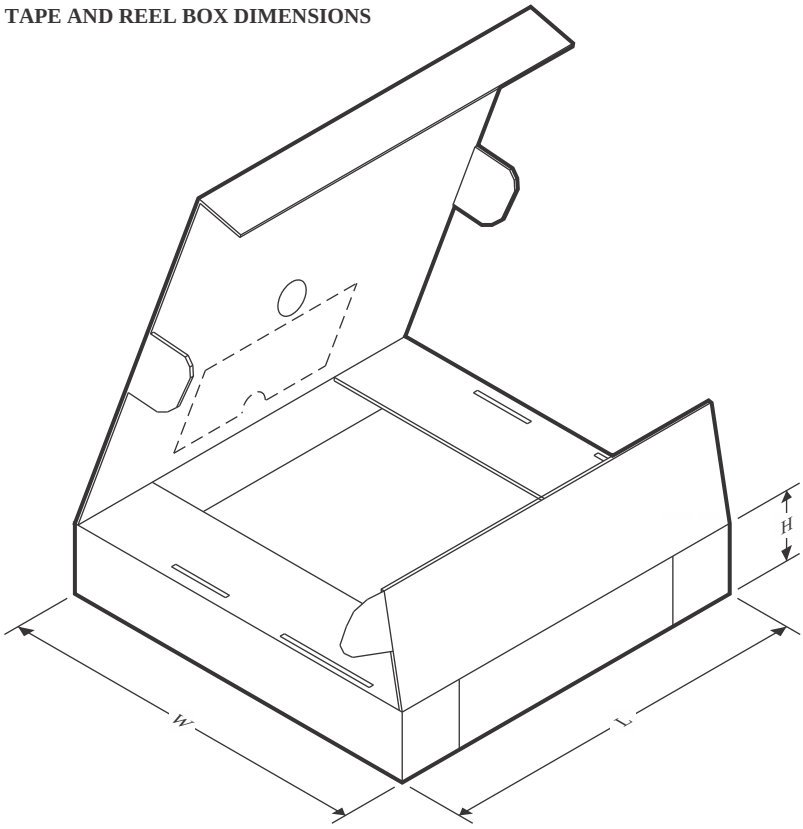
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25600DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

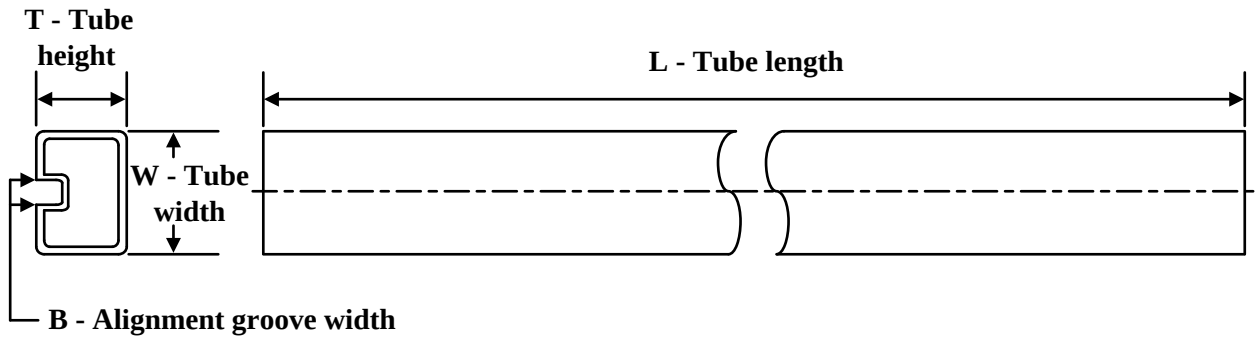
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25600DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

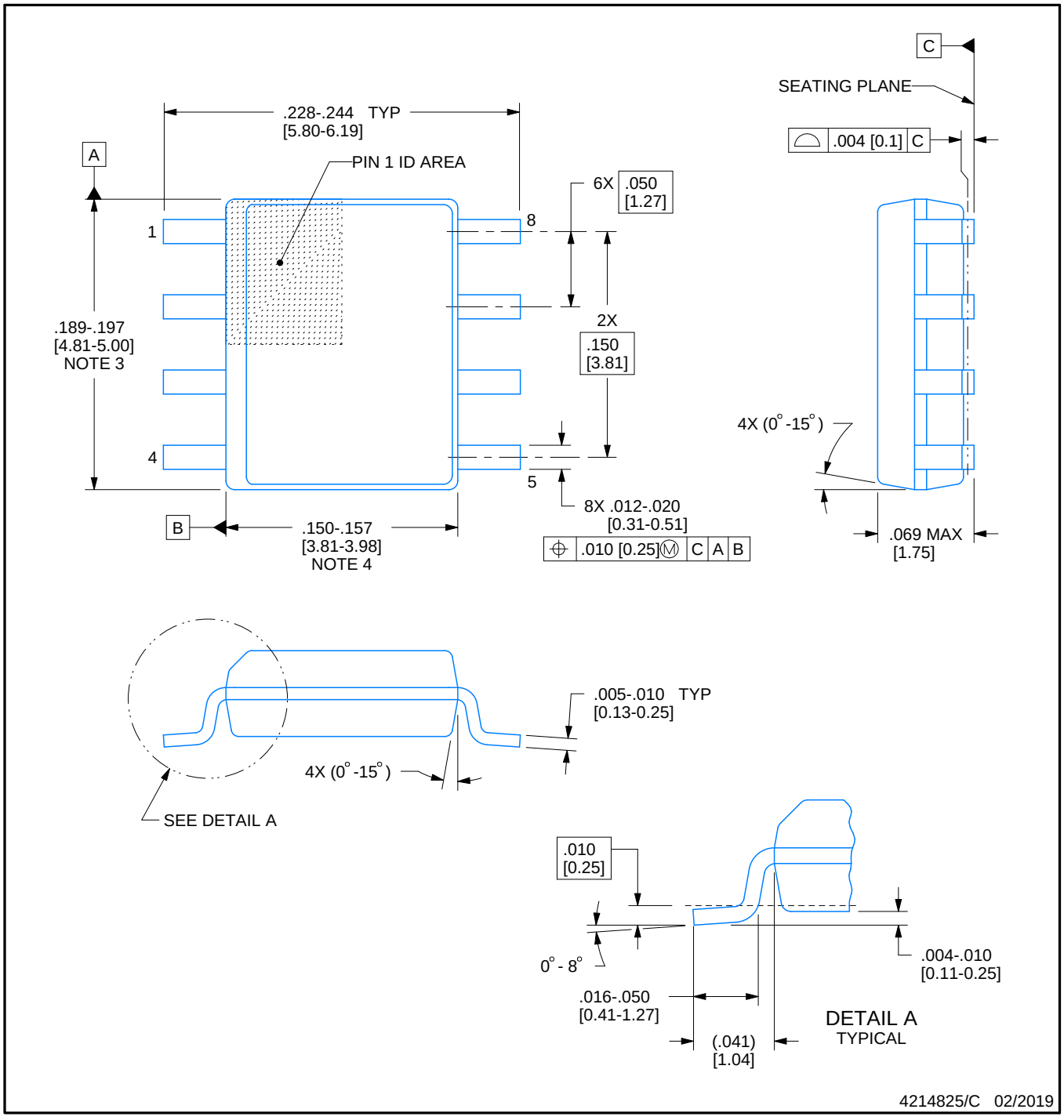
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC25600D	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

D0008A

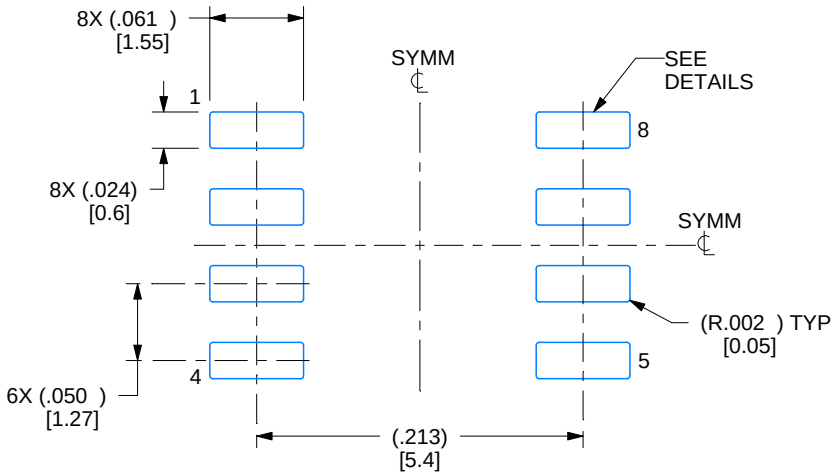
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

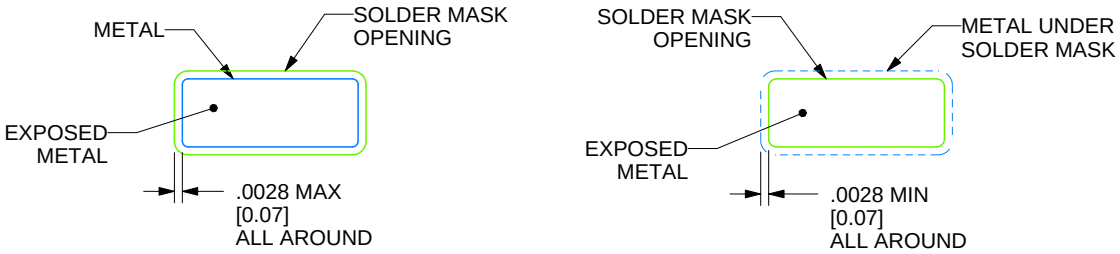


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

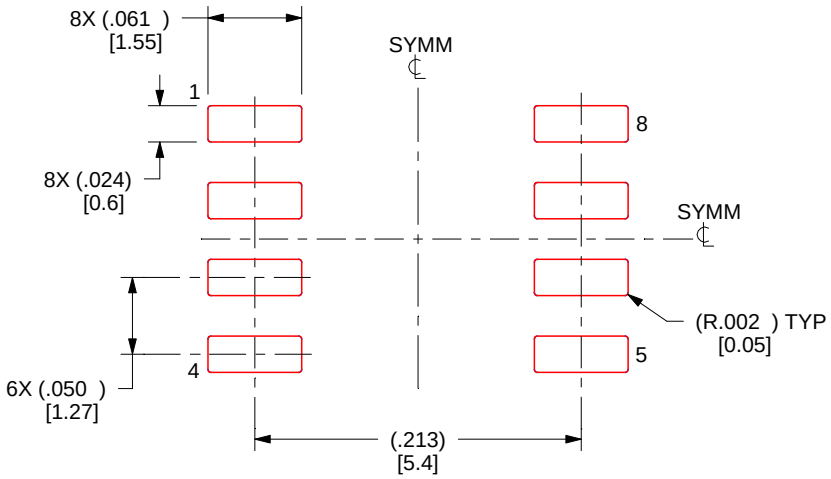
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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