TPS548B22 1.5-V to 18-V V_{IN}, 4.5-V to 22-V V_{DD}, 25-A SWIFT™ Synchronous Step-Down Converter With Full Differential Sense

1 Features

- Conversion Input Voltage Range (PV_{IN}): 1.5 V to 18 V
- Input Bias Voltage (V_{DD}) Range: 4.5 V to 22 V
- Output Voltage Range: 0.6 V to 5.5 V
- Integrated, 4.1-mΩ and 1.9-mΩ Power MOSFETs With 25-A Continuous Output Current
- Voltage Reference 0.6 V to 1.2 V in 50-mV Steps Using VSEL Pin
- ±0.5%, 0.9-V_{REF} Tolerance Range: –40°C to +125°C Junction Temperature
- True Differential Remote Sense Amplifier
- D-CAP3™ Control Loop to Support Large Bulk Capacitors and/or Small MLCCs Without External Compensation
- Adaptive On-Time Control With 4 Selectable Frequency Settings: 425 kHz, 650 kHz, 875 kHz and 1.05 MHz
- Temperature Compensated and with Programmable Positive and Negative Current Limit and OC Clamp
- Choice of Hiccup or Latch-Off OVP or UVP
- VDD UVLO External Adjustment by Precision EN Hysteresis
- Prebias Start-up Support
- Eco-Mode and FCCM Selectable
- Full Suite of Fault Protection and PGOOD
- 7 mm × 5 mm × 1.5 mm, 40-Pin, Stack Clipped LQFN-CLIP Package

2 Applications

- Enterprise Storage, SSD, NAS
- Wireless and Wired Communication Infrastructure
- Industrial PCs, Automation, ATE, PLC, Video Surveillance
- Enterprise Server, Switches, Routers
- AISIC, SoC, FPGA, DSP Core and I/O Rails

3 Description

The TPS548B22 device is a compact single buck converter with adaptive on-time, D-CAP3 mode control. It is designed for high accuracy, high efficiency, fast transient response, ease-of-use, low external component count, and space-conscious power systems.

This device features full differential sense, TI integrated FETs with a high-side on-resistance of 4.1 mΩ and a low-side on-resistance of 1.9 mΩ. The device also features accurate 0.5%, 0.9-V reference with an ambient temperature range between –40°C and +125°C. Competitive features include: very low external component count, accurate load regulation and line regulation, output voltage setpoint accuracy, auto-skip or FCCM mode operation, and internal soft-start control.

The TPS548B22 device is available in 7 mm × 5 mm, 40-pin, LQFN-CLIP (RVF) package (RoHs exempt).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS548B22	LQFN-CLIP (40)	7.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

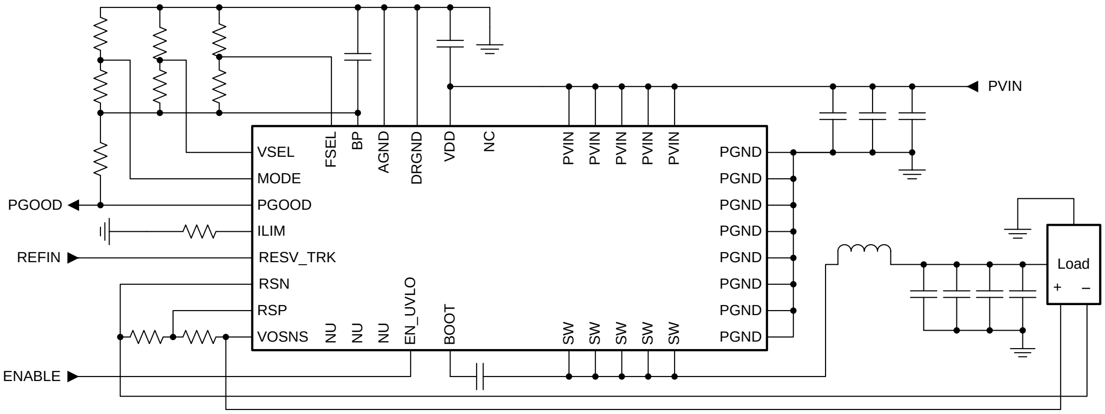


Table of Contents

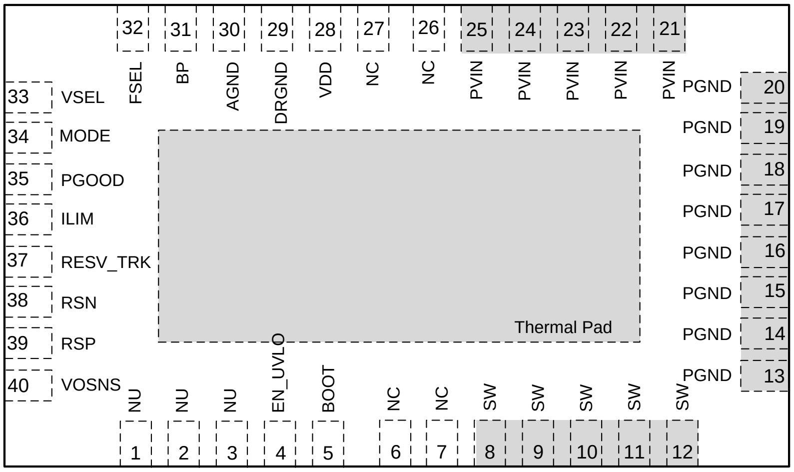
4 Revision History

Changes from Original (January 2017) to Revision A — Page

- Corrected package name in title of pin connection diagram from "DQP" to "RVF" ... 3
- Added MIN and MAX values for VDD UVLO rising threshold ... 6
- Added MIN and MAX for all SS settings and table notes 3 and 4 in *Timing Requirements* ... 9
- Changed "V_{OUT} = 5 V" to "V_{OUT} = 5.5 V" ... 13
- Added notes for 8 ms and 4 ms in Table 4; added *Application Workaround to Support 4-ms and 8-ms SS Settings* ... 19
- Added Figure 17 and Figure 18 ... 19

5 Pin Configuration and Functions

RVF Package
40-Pin LQFN-CLIP With Thermal Pad
Top View



Pin Functions

PIN		I/O/P[1]	DESCRIPTION
NO.	NAME		
1, 2, 3	NU	O	Not used pins.
4	EN_UVLO	I	Enable pin that can turn on the DC/DC switching converter. Use also to program the required PVIN UVLO when PVIN and VDD are connected together.
5	BOOT	P	Supply rail for high-side gate driver (boot terminal). Connect boot capacitor from this pin to SW node. Internally connected to BP via bootstrap PMOS switch.
6, 7, 26, 27	NC		No connect.
8, 9, 10, 11, 12	SW	I/O	Output switching terminal of power converter. Connect the pins to the output inductor.
13, 14, 15, 16, 17, 18, 19, 20	PGND	P	Power ground of internal FETs.
21, 22, 23, 24, 25,	PVIN	P	Power supply input for integrated power MOSFET pair.
28	VDD	P	Controller power supply input.
29	DRGND	P	Internal gate driver return.
30	AGND	G	Ground pin for internal analog circuits.
31	BP	O	LDO output
32	FSEL	I	Program switching frequency, internal ramp amplitude and SKIP or FCCM mode.
33	VSEL	I	Program the initial start-up and or reference voltage without feedback resistor dividers (from 0.6 V to 1.2 V in 50-mV increments).
34	MODE	I	Mode selection pin. Select the control mode (DCAP3 or DCAP), internal VREF operation, external REFIN and tracking operation and soft-start timing selection.
35	PGOOD	O	Open drain power-good status signal.
36	ILIM	I/O	Program overcurrent limit by connecting a resistor to ground.
37	RESV_TRK	I	Do not connect.
38	RSN	I	Inverting input of the differential remote sense amplifier.
39	RSP	I	Non-inverting input of the differential remote sense amplifier.
40	VOSNS	I	Output voltage monitor input pin.

(1) I = input, O = output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
Input voltage	PVIN		–0.3	25	V
	VDD		–0.3	25	
	BOOT		–0.3	34	
	BOOT to SW	DC	–0.3	7.7	
		< 10 ns	–0.3	9.0	
	NU		–0.3	6	
	EN_UVLO, VOSNS, MODE, FSEL, ILIM		–0.3	7.7	
	RSP, RESV_TRK, VSEL		–0.3	3.6	
	RSN		–0.3	0.3	
	PGND, AGND, DRGND		–0.3	0.3	
	SW	DC	–0.3	25	
		< 10 ns	–5	27	
Output voltage	PGOOD, BP		–0.3	7.7	
Junction temperature, T_J			–55	150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Input voltage	PVIN with no snubber circuit: SW ringing peak voltage equals 23 V at 25-A output		1.5	14	V
	PVIN with snubber circuit: SW ringing peak voltage equals 23 V at 25-A output		1.5	18	
	VDD		4.5	22	
	BOOT		–0.1	24.5	
	BOOT to SW	DC	–0.1	6.5	
		< 10 ns	–0.1	7	
	NU		–0.1	5.5	
	EN_UVLO, VOSNS, MODE, FSEL, ILIM		–0.1	5.5	
	RSP, RESV_TRK, VSEL		–0.1	3.3	
	RSN		–0.1	0.1	
	PGND, AGND, DRGND		–0.1	0.1	
	SW	DC	–0.1	18	
		< 10 ns	–5	27	
Output voltage	PGOOD, BP		–0.1	7	V
Junction temperature, T_J			–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS548B22	UNIT
		RVF (QFN)	
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.96	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
MOSFET ON-RESISTANCE ($R_{DS(on)}$)						
$R_{DS(on)}$	High-side FET	(V_{BOOT} – V_{SW}) = 5 V, I_D = 25 A, T_J = 25°C		4.1		mΩ
	Low-side FET	V_{VDD} = 5 V, I_D = 25 A, T_J = 25°C		1.9		mΩ
INPUT SUPPLY AND CURRENT						
V_{VDD}	VDD supply voltage	Nominal VDD voltage range	4.5		22	V
I_{VDD}	VDD bias current	No PVIN, EN_UVLO = High, T_A = 25°C,		2		mA
$I_{VDDSTBY}$	VDD standby current	No PVIN, EN_UVLO = Low, T_A = 25°C		700		µA
UNDERVOLTAGE LOCKOUT						
V_{VDD_UVLO}	VDD UVLO rising threshold		4.23	4.25	4.34	V
$V_{VDD\_UVLO(HYS)}$	VDD UVLO hysteresis			0.2		V
$V_{EN\_ON\_TH}$	EN_UVLO on threshold		1.45	1.6	1.75	V
V_{EN_HYS}	EN_UVLO hysteresis		270	300	340	mV
I_{EN_LKG}	EN_UVLO input leakage current	V_{EN_UVLO} = 5 V	–1	0	1	µA
INTERNAL REFERENCE VOLTAGE, EXTERNAL REFIN, AND TRACKING RANGE						
V_{INTREF}	Internal REF voltage			900.4		mV
$V_{INTREFTOL}$	Internal REF voltage tolerance	–40°C ≤ T_J ≤ 125°C	–0.5%		0.5%	
V_{INTREF}	Internal REF voltage range		0.6		1.2	V
OUTPUT VOLTAGE						
V_{IOS_LPCMP}	Loop comparator input offset voltage(1)		–2.5		2.5	mV
I_{RSP}	RSP input current	V_{RSP} = 600 mV	–1		1	µA
$I_{VO(dis)}$	VO discharge current	V_{VO} = 0.5 V, power conversion disabled	8	12		mA
DIFFERENTIAL REMOTE SENSE AMPLIFIER						
f_{UGBW}	Unity gain bandwidth(1)		5	7		MHz
A_0	Open loop gain(1)		75			dB
SR	Slew rate(1)			±4.7		V/µsec
V_{IRNG}	Input range(1)		–0.2		1.8	V
V_{OFFSET}	Input offset voltage(1)		–3.5		3.5	mV
INTERNAL BOOT STRAP SWITCH						
V_F	Forward voltage	$V_{BP\text{-}BOOT}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{BOOT}	VBST leakage current	V_{BOOT} = 30 V, V_{SW} = 25 V, T_A = 25°C		0.01	1.5	µA

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(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
MODE, VSEL, FSEL DETECTION							
V_{DETECT_TH}	MODE, VSEL, and FSEL detection voltage	V_{BP} = 2.93 V, R_{HIGH} = 100 kΩ	Open		V_{BP}		V
			R_{LOW} = 187 kΩ		1.9091		
			R_{LOW} = 165 kΩ		1.8243		
			R_{LOW} = 147 kΩ		1.7438		
			R_{LOW} = 133 kΩ		1.6725		
			R_{LOW} = 121 kΩ		1.6042		
			R_{LOW} = 110 kΩ		1.5348		
			R_{LOW} = 100 kΩ		1.465		
			R_{LOW} = 90.9 kΩ		1.3952		
			R_{LOW} = 82.5 kΩ		1.3245		
			R_{LOW} = 75 kΩ		1.2557		
			R_{LOW} = 68.1 kΩ		1.187		
			R_{LOW} = 60.4 kΩ		1.1033		
			R_{LOW} = 53.6 kΩ		1.0224		
			R_{LOW} = 47.5 kΩ		0.9436		
			R_{LOW} = 42.2 kΩ		0.8695		
			R_{LOW} = 37.4 kΩ		0.7975		
			R_{LOW} = 33.2 kΩ		0.7303		
			R_{LOW} = 29.4 kΩ		0.6657		
			R_{LOW} = 25.5 kΩ		0.5953		
			R_{LO}W = 22.1 kΩ		0.5303		
			R_{LOW} = 19.1 kΩ		0.4699		
			R_{LOW} = 16.5 kΩ		0.415		
			R_{LOW} = 14.3 kΩ		0.3666		
			R_{LOW} = 12.1 kΩ		0.3163		
			R_{LOW} = 10 kΩ		0.2664		
			R_{LOW} = 7.87 kΩ		0.2138		
			R_{LOW} = 6.19 kΩ		0.1708		
			R_{LOW} = 4.64 kΩ		0.1299		
			R_{LOW} = 3.16 kΩ		0.0898		
			R_{LOW} = 1.78 kΩ		0.0512		
			R_{LOW} = 0 Ω		GND		
PGOOD COMPARATOR							
V_{PGTH}	PGOOD threshold	PGOOD in from higher		105	108	111	%V_{REF}
		PGOOD in from lower		89	92	95	
		PGOOD out to higher			120		
		PGOOD out to lower			68		
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V			6.9		mA
I_{PGLK}	PGOOD leakage current	V_{PGOOD} = 5 V		–1	0	1	µA

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VDD} = 12 V, V_{EN_UVLO} = 5 V (unless otherwise noted)

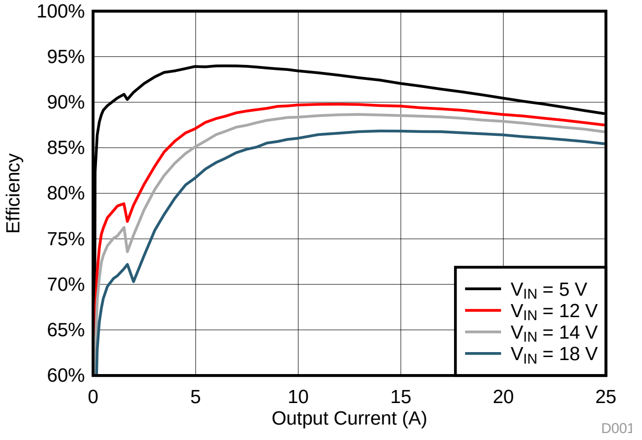
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CURRENT DETECTION						
V_{ILM}	V_{ILIM} voltage range	On-resistance ($R_{DS(on)}$) sensing	0.1		1.2	V
I_{OCL_VA}	Valley current limit threshold	R_{LIM} = 61.9 kΩ		30		A
		OC tolerance		±15%		
		R_{LIM} = 51.1 kΩ		25		A
		OC tolerance		±15%		
		R_{LIM} = 40.2 kΩ	17	20	23	A
$I_{OCL\_VA\_N}$	Negative valley current limit threshold	R_{LIM} = 61.9 kΩ		–30		A
		R_{LIM} = 51.1 kΩ		–25		
		R_{LIM} = 40.2 kΩ		–20		
I_{CLMP_LO}	Clamp current at V_{LIM} clamp at lowest	V_{ILIM_CLMP} = 0.1 V, T_A = 25°C		5		A
I_{CLMP_HI}	Clamp current at V_{LIM} clamp at highest	V_{ILIM_CLMP} = 1.2 V, T_A = 25°C		50		A
V_{ZC}	Zero cross detection offset			0		mV
PROTECTIONS AND OOB						
V_{BPUVLO}	BP UVLO threshold voltage	Wake-up		3.32		V
		Shutdown		3.11		
V_{OVP}	OVP threshold voltage	OVP detect voltage	117%	120%	123%	V_{REF}
V_{UVP}	UVP threshold voltage	UVP detect voltage	65%	68%	71%	V_{REF}
V_{OOB}	OOB threshold voltage			8%		V_{REF}
BP VOLTAGE						
V_{BP}	BP LDO output voltage	V_{IN} = 12 V, 0 A ≤ I_{LOAD} ≤ 10 mA,		5.07		V
V_{BPDO}	BP LDO drop-out voltage	V_{IN} = 4.5 V, I_{LOAD} = 30 mA, T_A = 25°C			365	mV
I_{BPMAX}	BP LDO over-current limit	V_{IN} = 12 V, T_A = 25°C		100		mA
THERMAL SHUTDOWN						
T_{SDN}	Built-In thermal shutdown threshold(1)	Shutdown temperature	155	165		°C
		Hysteresis			30	

6.6 Timing Requirements

				MIN	NOM	MAX	UNIT
SWITCHING FREQUENCY							
f_{SW}	VO switching frequency(1)	V_{IN} = 12 V, V_{VO} = 1 V, T_A = 25°C		380	425	475	kHz
				585	650	740	
				790	875	995	
				950	1050	1250	
$t_{ON(min)}$	Minimum on time(2)				60		ns
$t_{OFF(min)}$	Minimum off time(2)	DRVH falling to rising				300	ns
SOFT-START							
t_{SS}	Soft-start time	V_{OUT} rising from 0 V to 95% of final set point, R_{MODE_HIGH} = 100 kΩ	R_{MODE_LOW} = 60.4 kΩ	7	8(3)	10	ms
			R_{MODE_LOW} = 53.6 kΩ	3.6	4(4)	5.2	ms
			R_{MODE_LOW} = 47.5 kΩ	1.6	2	2.8	ms
			R_{MODE_LOW} = 42.2 kΩ	0.8	1	1.6	ms
PGOOD COMPARATOR							
t_{PGDLY}	PGOOD delay time	Delay for PGOOD going in			1		ms
		Delay for PGOOD coming out				2	µs
POWER-ON DELAY							
t_{PODLY}	Power-on delay time				1.024		ms
PROTECTIONS AND OOB							
t_{OVPDLY}	OVP response time	100-mV over drive				1	µs
t_{UVPDLY}	UVP delay filter delay time				1		ms
t_{HICDLY}	Hiccup blanking time	t_{SS} = 1 ms			16		ms
		t_{SS} = 2 ms			24		ms
		t_{SS} = 4 ms			38		ms
		t_{SS} = 8 ms			67		ms

(1) Correlated with closed-loop EVM measurement at load current of 20 A.
(2) Specified by design. Not production tested.
(3) In order to use the 8-ms SS setting, follow the steps outlined in *Application Workaround to Support 4-ms and 8-ms SS Settings*.
(4) In order to use the 4-ms SS setting, follow the steps outlined in *Application Workaround to Support 4-ms and 8-ms SS Settings*.

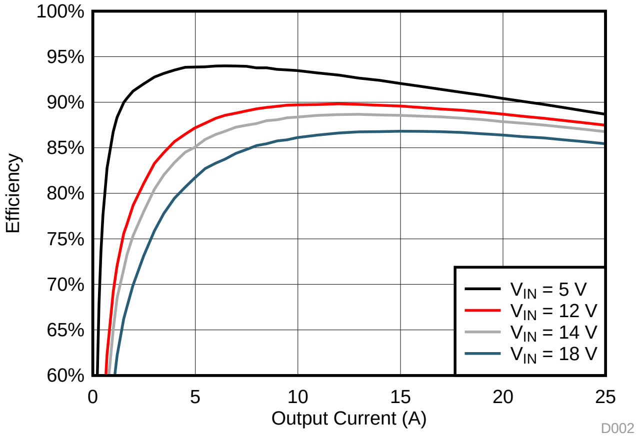
6.7 Typical Characteristics



V_{OUT} = 1 V V_{DD} = V_{IN} SKIP Mode

f_{SW} = 650 kHz

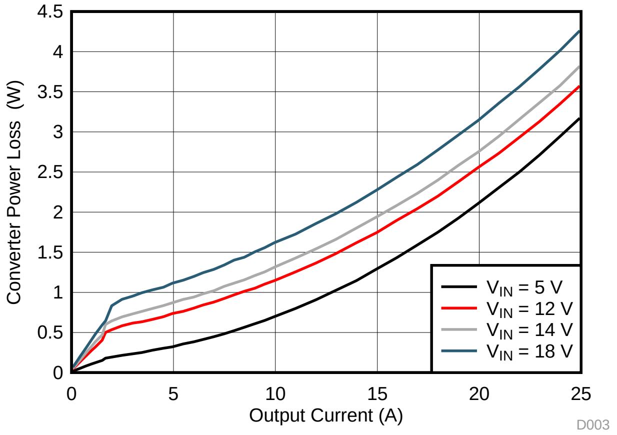
Figure 1. Efficiency vs Output Current



V_{OUT} = 1 V V_{DD} = V_{IN} FCCM Mode

f_{SW} = 650 kHz

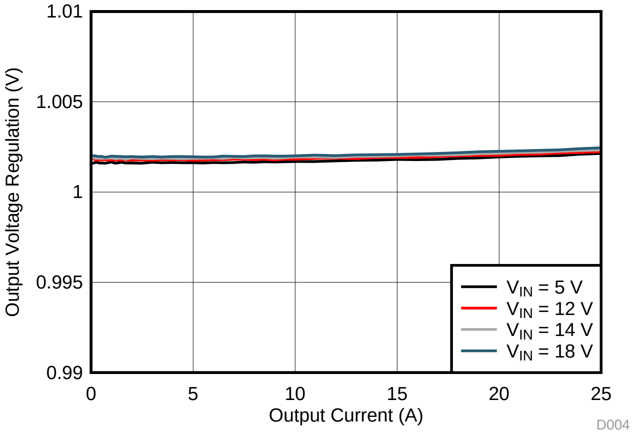
Figure 2. Efficiency vs Output Current



V_{OUT} = 1 V V_{DD} = V_{IN} SKIP Mode

f_{SW} = 650 kHz

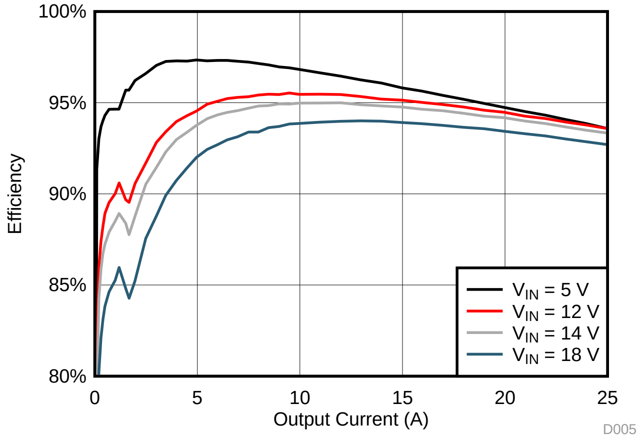
Figure 3. Converter Power Loss vs Output Current



V_{OUT} = 1 V V_{DD} = V_{IN} FCCM Mode

f_{SW} = 650 kHz

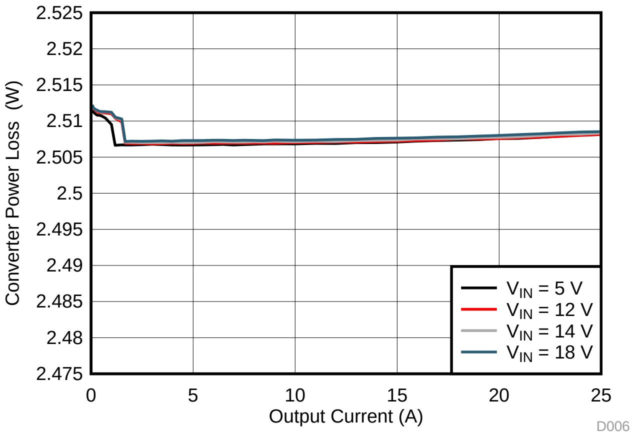
Figure 4. Output Voltage Regulation vs Output Current



V_{DD} = V_{IN} f_{SW} = 650 kHz SKIP Mode

V_{OUT} = 2.5 V L= 820 nH, 0.9 mΩ

Figure 5. Efficiency vs Output Current

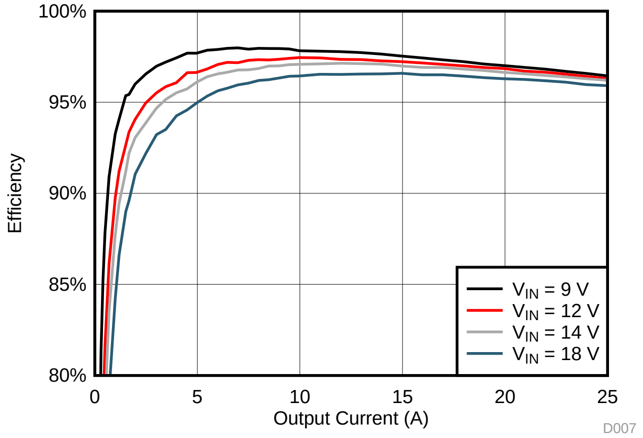


V_{DD} = V_{IN} f_{SW} = 650 kHz SKIP Mode

V_{OUT} = 2.5 V L= 820 nH, 0.9 mΩ

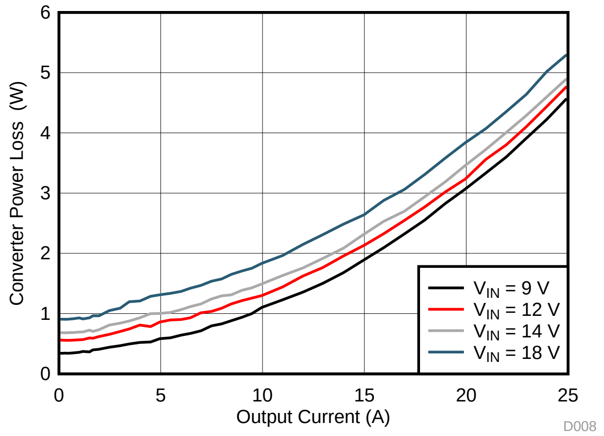
Figure 6. Output Voltage Regulation vs Output Current

Typical Characteristics (continued)



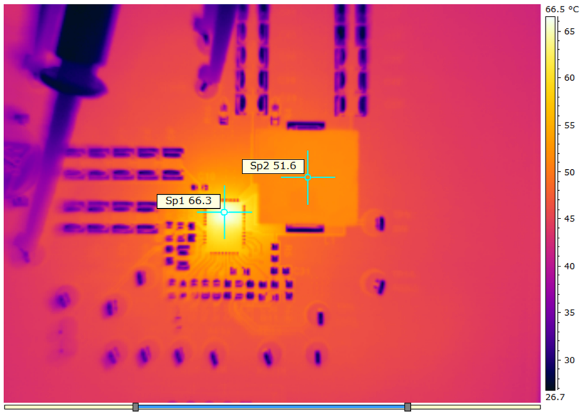
V_{DD} = V_{IN} f_{SW} = 650 kHz FCCM Mode
V_{OUT} = 5 V L= 820 nH, 0.9 mΩ

Figure 7. Efficiency vs Output Current



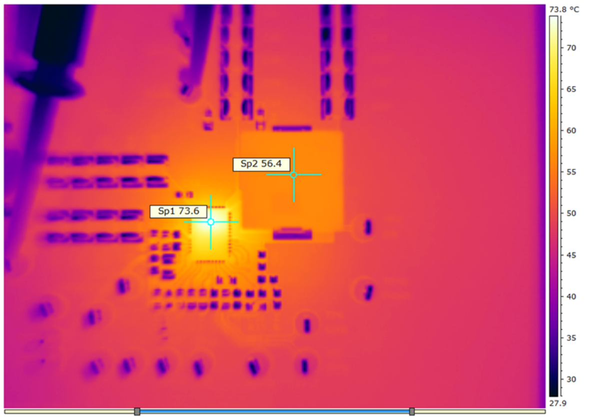
V_{DD} = V_{IN} f_{SW} = 650 kHz FCCM Mode
V_{OUT} = 5 V L= 820 nH, 0.9 mΩ

Figure 8. Power Loss vs Output Current



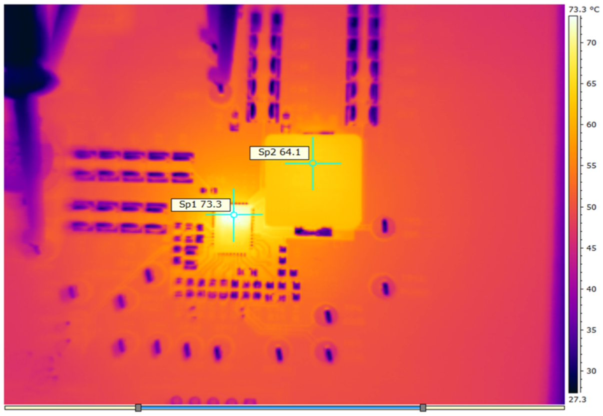
V_{DD} = V_{IN} = 12 V f_{SW} = 650 kHz I_{OUT} = 25 A
V_{OUT} = 1 V Natural convection at room temperature

Figure 9. Thermal Image



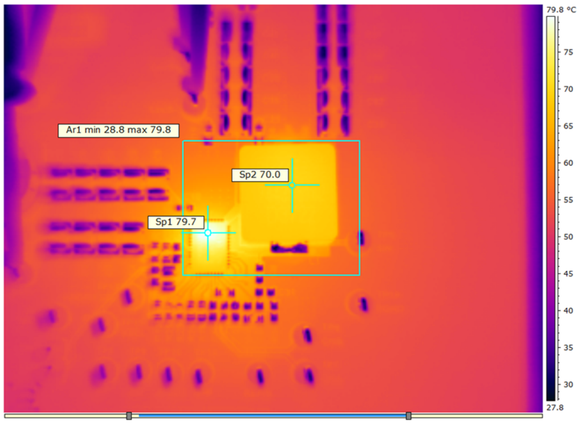
V_{DD} = V_{IN} = 18 V f_{SW} = 650 kHz I_{OUT} = 25 A
V_{OUT} = 1 V Natural convection at room temperature

Figure 10. Thermal Image



V_{DD} = V_{IN} = 12 V f_{SW} = 650 kHz I_{OUT} = 25 A
V_{OUT} = 2.5 V Natural convection at room temperature

Figure 11. Thermal Image



V_{DD} = V_{IN} = 12 V f_{SW} = 650 kHz I_{OUT} = 25 A
V_{OUT} = 5 V Natural convection at room temperature

Figure 12. Thermal Image

7 Detailed Description

7.1 Overview

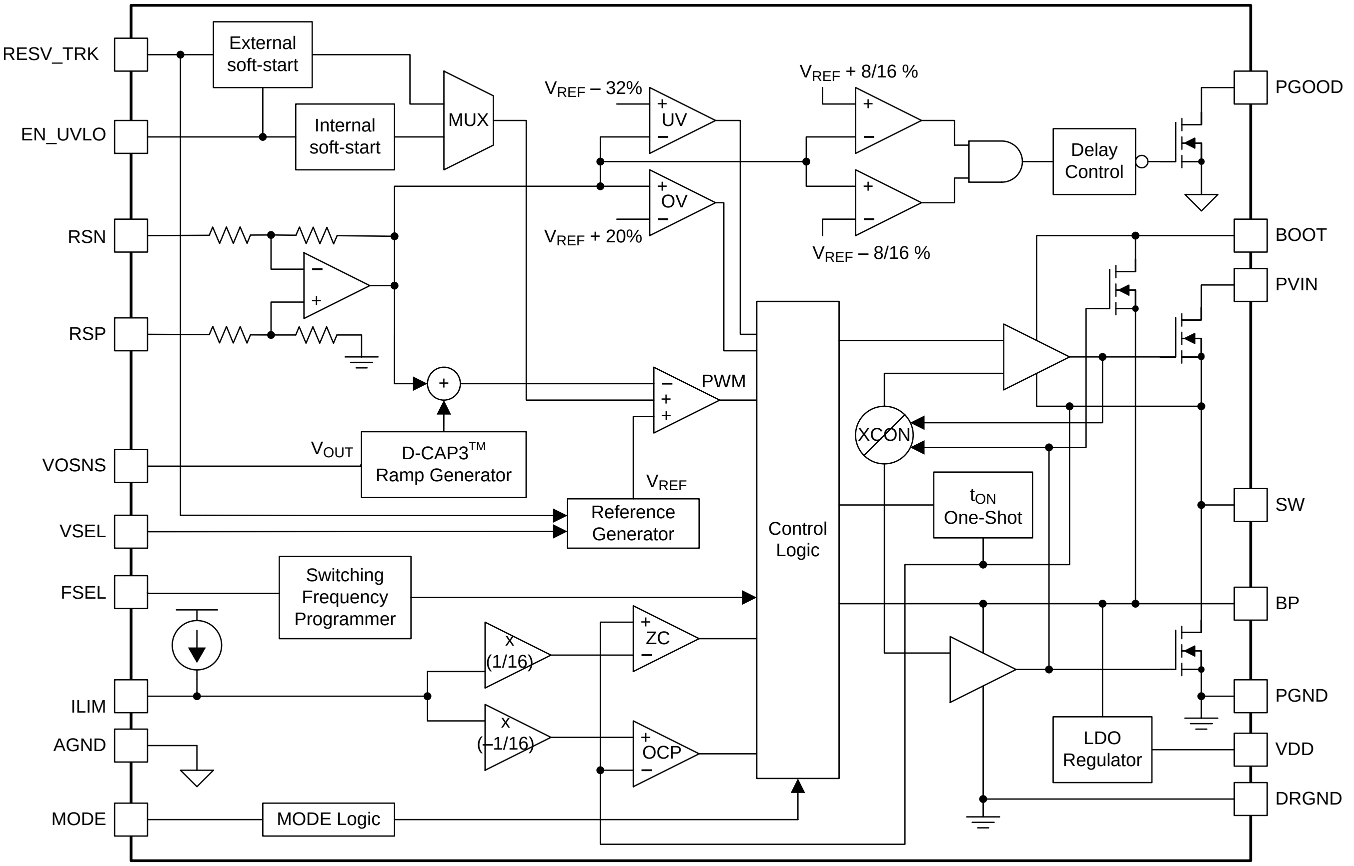
The TPS548B22 device is a high-efficiency, single-channel, FET-integrated, synchronous buck converter. It is suitable for point-of-load applications with 25 A or lower output current in storage, telecomm and similar digital applications. The device features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination is ideal for building modern high/low duty ratio, ultra-fast load step response DC-DC converters.

The TPS548B22 device has integrated MOSFETs rated at 25-A TDC.

The converter input voltage range is from 1.5 V up to 18 V, and the VDD input voltage range is from 4.5 V to 22 V. The output voltage ranges from 0.6 V to 5.5 V.

Stable operation with all ceramic output capacitors is supported, because the D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require phase compensation network outside which makes it easy to use and also enables low external component count. The designer selects the switching frequency from 4 preset values via resistor settings by FSEL pin. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load step transient.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 25-A FET

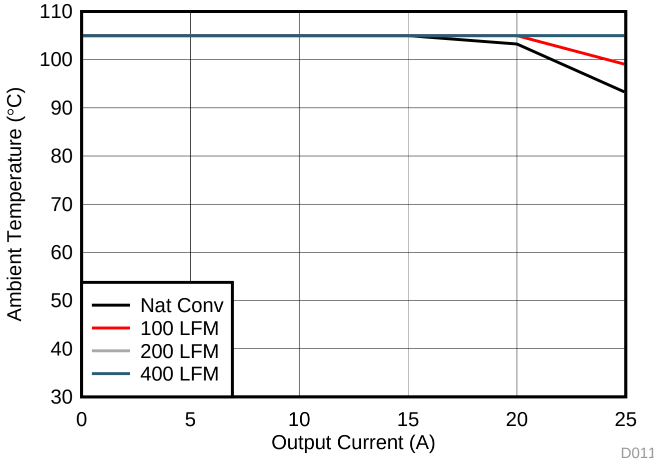
The TPS548B22 device is a high-performance, integrated FET converter supporting current rating up to 25 A thermally. It integrates two N-channel NexFET™ power MOSFETs, enabling high power density and small PCB layout area. The drain-to-source breakdown voltage for these FETs is 25 V DC and 27 V transient for 10 ns. Avalanche breakdown occurs if the absolute maximum voltage rating exceeds 27 V. In order to limit the switch node ringing of the device, TI recommends adding a R-C snubber from the SW node to the PGND pins. Refer to the *Layout Guidelines* section for the detailed recommendations.

7.3.2 On-Resistance

The typical on-resistance ($R_{DS(on)}$) for the high-side MOSFET is 4.1 mΩ and typical on-resistance for the low-side MOSFET is 1.9 mΩ with a nominal gate voltage (V_{GS}) of 5 V.

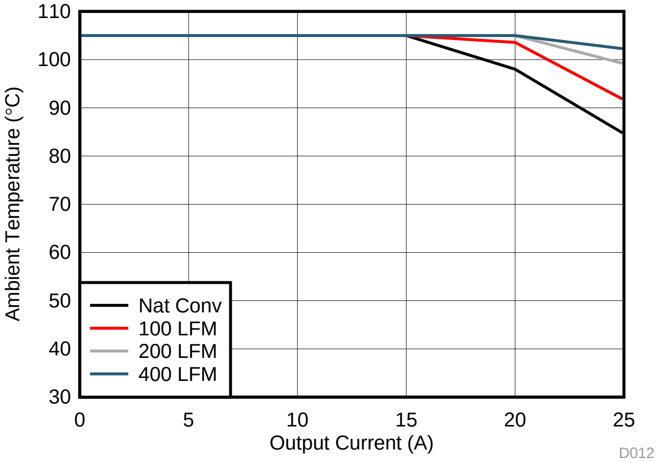
7.3.3 Package Size, Efficiency and Thermal Performance

The TPS548B22 device is available in a 7 mm × 5 mm VQFN package with 40 power and I/O pins. It employs TI proprietary MCM packaging technology with thermal pad. With a properly designed system layout, applications achieve optimized safe operating area (SOA) performance. The curves shown in Figure 13 and Figure 14 are based on the orderable evaluation module design. (See SLUUBI9 to order the EVM.)



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 650 kHz

Figure 13. Safe Operating Area



V_{IN} = 12 V V_{OUT} = 5.5 V f_{SW} = 650 kHz

Figure 14. Safe Operating Area

7.3.4 Soft-Start Operation

In the TPS548B22 device the soft-start time controls the inrush current required to charge the output capacitor bank during start-up. The device offers selectable soft-start options of 1 ms, 2 ms, 4 ms and 8 ms. When the device is enabled (either by EN or VDD UVLO), the reference voltage ramps from 0 V to the final level defined by VSEL pin strap configuration, in a given soft-start time. The TPS548B22 device supports several soft-start times between 1 msec and 8 msec selected by MODE pin configuration. Refer to Table 4 for details.

7.3.5 V_{DD} Supply Undervoltage Lockout (UVLO) Protection

The TPS548B22 device provides fixed VDD undervoltage lockout threshold and hysteresis. The typical VDD turn-on threshold is 4.25 V, and hysteresis is 0.2 V. The VDD UVLO can be used in conjunction with the EN_UVLO signal to provide proper power sequence to the converter design. UVLO is a non-latched protection.

7.3.6 EN_UVLO Pin Functionality

The EN_UVLO pin drives an input buffer with accurate threshold and can be used to program the exact required turnon and turnoff thresholds for switcher enable, VDD UVLO, or VIN UVLO (if VIN and VDD are tied together). If desired, an external resistor divider can be used to set and program the turn-on threshold for VDD or VIN UVLO.

Feature Description (continued)

Figure 15 shows how to program the input voltage UVLO using the EN_UVLO pin.

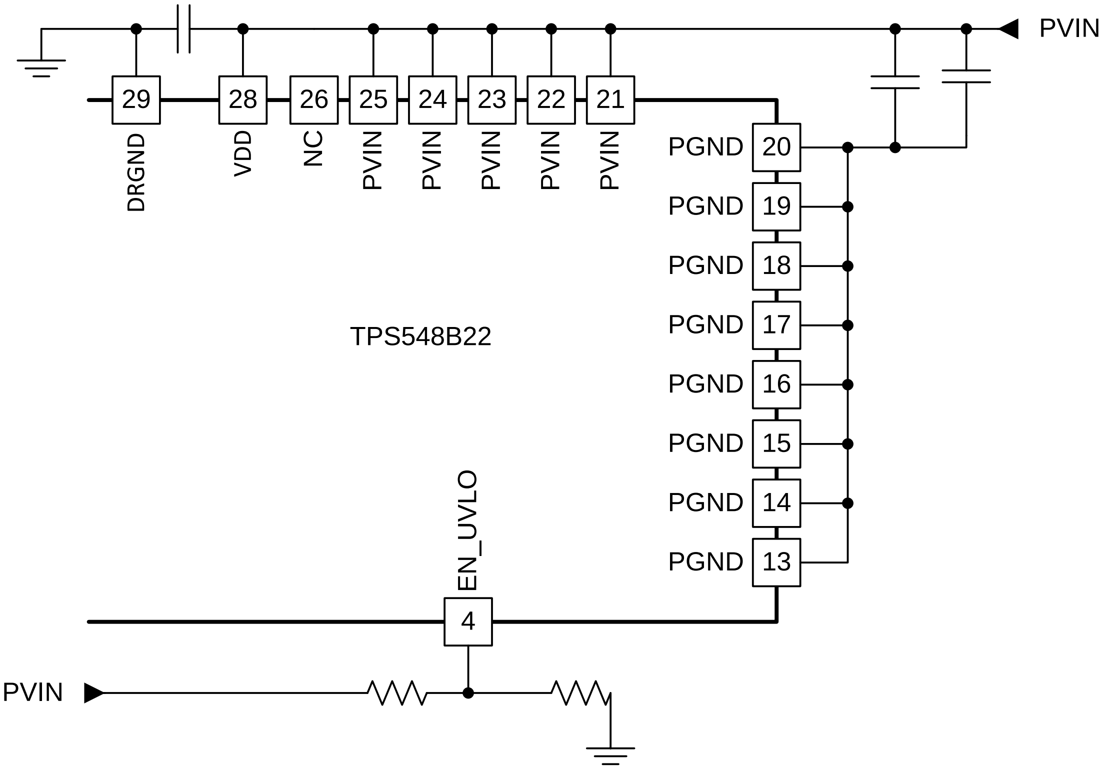


Figure 15. Programming the UVLO Voltage

7.3.7 Fault Protections

This section describes positive and negative overcurrent limits, overvoltage protections, out-of-bounds limits, undervoltage protections and over temperature protections.

7.3.7.1 Current Limit (ILIM) Functionality

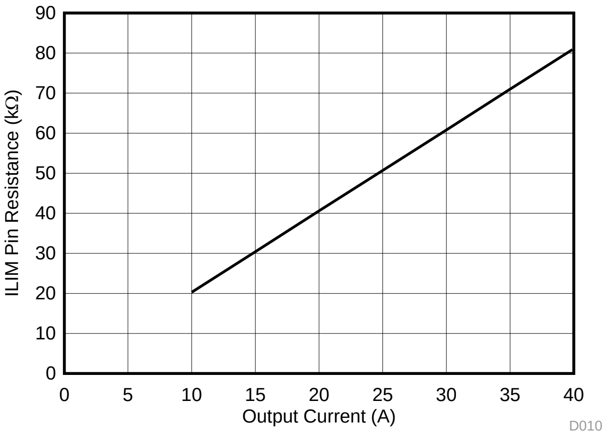


Figure 16. Current Limit Resistance vs OCP Valley Overcurrent Limit

Feature Description (continued)

The ILIM pin sets the OCP level. Connect the ILIM pin to GND through the voltage setting resistor, R_{ILIM}. In order to provide both good accuracy and cost effective solution, TPS548B22 supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

Also, the device performs both positive and negative inductor current limiting with the same magnitudes. The positive current limit normally protects the inductor from saturation that causes damage to the high-side FET and low-side FET. The negative current limit protects the low-side FET during OVP discharge.

The voltage between GND pin and SW pin during the OFF time monitors the inductor current. The current limit has 1200 ppm/°C temperature slope to compensate the temperature dependency of the on-resistance ($R_{DS(on)}$). The GND pin is used as the positive current sensing node.

TPS548B22 uses cycle-by-cycle over-current limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent ILIM level. V_{ILIM} sets the valley level of the inductor current.

7.3.7.2 Overvoltage Protection (OVP) and Undervoltage Protection (UVP)

Table 1. Overvoltage Protection Details

REFERENCE VOLTAGE (V_{REF})	SOFT-START RAMP	START-UP OVP THRESHOLD	OPERATING OVP THRESHOLD	OVP DELAY 100 mV OD (µs)	OVP RESET
Internal	Internal	1.2 × Internal V_{REF}		1	UVP

The device monitors a feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the device latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft start is complete.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again for a minimum on-time. The TPS548B22 device operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 1 ms. After the 1-ms UVP delay time, the high-side FET is latched off and low-side FET is latched on. The fault is cleared with a reset of VDD or by retoggling the EN pin.

7.3.7.3 Out-of-Bounds Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.7.4 Overtemperature Protection

TPS548B22 has overtemperature protection (OTP) by monitoring the die temperature. If the temperature exceeds the threshold value (default value 165°C), the device is shut off. When the temperature falls about 25°C below the threshold value, the device turns on again. The OTP is a non-latch protection.

7.4 Device Functional Modes

7.4.1 DCAP3 Control Topology

The TPS548B22 employs an artificial ramp generator that stabilizes the loop. The ramp amplitude is automatically adjusted as a function of selected switching frequency (f_{SW}). The ramp amplitude is a function of duty cycle (V_{OUT}-to-V_{IN} ratio). Consequently, two additional pin-strap bits (FSEL[2:1]) are provided for fine tuning the internal ramp amplitude. The device uses an improved DCAP3 control loop architecture that incorporates a steady-state error integrator. The slow integrator improves the output voltage DC accuracy greatly and presents minimal impact to small signal transient response. To further enhance the small signal stability of the control loop, the device uses a modified ramp generator that supports a wider range of output LC stage.

7.4.2 DCAP Control Topology

For advanced users of this device, the internal DCAP3 ramp can be disabled using the MODE[4] pin strap bit. This situation requires an external RCC network to ensure control loop stability. Place this RCC network across the output inductor. Use a range between 10 mV and 15 mV of injected RSP pin ripple. If no feedback resistor divider network is used, insert a 10-kΩ resistor between the VOUT pin and the RSP pin.

7.5 Programming

7.5.1 Programmable Pin-Strap Settings

FSEL, VSEL and MODE. Description: a 1% or better 100-kΩ resistor is needed from BP to each of the three pins. The bottom resistor from each pin to ground (see Table 2) in conjunction with the top resistor defines each pin strap selection. The pin detection checks for external resistor divider ratio during initial power up (VDD is brought down below approximately 3 V) when BP LDO output is at approximately 2.9 V.

7.5.1.1 Frequency Selection (FSEL) Pin

The TPS548B22 device allows users to select the switching frequency, light load and internal ramp amplitude by using FSEL pin. Table 2 lists the divider resistor values for the selection. The 1% tolerance resistors with typical temperature coefficient of ±100ppm/°C are recommended. Higher performance resistors can be used if tighter noise margin is required for more reliable frequency selection detection.

FSEL pin strap configuration programs the switching frequency, internal ramp compensation and light load conduction mode.

.

Programming (continued)

Table 2. FSEL Pin Strap Configurations

FSEL[4]	FSEL[3]	FSEL[2]	FSE[L1]	FSEL[0]	R_{FSEL} (kΩ) (1)
FSEL[1:0]		**RCSP_FSEL[1:0]**		**CM**	
11: 1.05 MHz		11: R × 3		1: FCCM	Open
				0: SKIP	187
		10: R × 2		1: FCCM	165
				0: SKIP	147
		01: R × 1		1: FCCM	133
				0: SKIP	121
		00: R/2		1: FCCM	110
				0: SKIP	100
10: 875 kHz		11: R × 3		1: FCCM	90.9
				0: SKIP	82.5
		10: R×2		1: FCCM	75
				0: SKIP	68.1
		01: R × 1		1: FCCM	60.4
				0: SKIP	53.6
		00: R/2		1: FCCM	47.5
				0: SKIP	42.2
01: 650 kHz		11: R × 3		1: FCCM	37.4
				0: SKIP	33.2
		10: R × 2		1: FCCM	29.4
				0: SKIP	25.5
		01: R × 1		1: FCCM	22.1
				0: SKIP	19.1
		00: R/2		1: FCCM	16.5
				0: SKIP	14.3
00: 425 kHz		11: R × 3		1: FCCM	12.1
				0: SKIP	10
		10: R × 2		1: FCCM	7.87
				0: SKIP	6.19
		01: R × 1		1: FCCM	4.64
				0: SKIP	3.16
		00: R/2		1: FCCM	1.78
				0: SKIP	0

(1) 1% or better and connect to ground

7.5.1.2 VSEL Pin

VSEL pin strap configuration is used to program initial boot voltage value, hiccup mode and latch off mode. The initial boot voltage is used to program the main loop voltage reference point. VSEL voltage settings provide TI designated discrete internal reference voltages. Table 3 lists internal reference voltage selections.

Table 3. Internal Reference Voltage Selections

VSEL[4]	VSEL[3]	VSE[L2]	VSEL[1]	VSEL[0]	R_{VSEL} (kΩ) (1)
1111: **0.975 V**				1: Latch-Off	Open
				0: Hiccup	187
1110: 1.1992 V				1: Latch-Off	165
				0: Hiccup	147
1101: 1.1504 V				1: Latch-Off	133
				0: Hiccup	121
1100: 1.0996 V				1: Latch-Off	110
				0: Hiccup	100
1011: 1.0508 V				1: Latch-Off	90.9
				0: Hiccup	82.5
1010: 1.0000 V				1: Latch-Off	75
				0: Hiccup	68.1
1001: 0.9492 V				1: Latch-Off	60.4
				0: Hiccup	53.6
1000: 0.9023 V				1: Latch-Off	47.5
				0: Hiccup	42.2
0111: 0.9004 V				1: Latch-Off	37.4
				0: Hiccup	33.2
0110: 0.8496 V				1: Latch-Off	29.4
				0: Hiccup	25.5
0101: 0.8008 V				1: Latch-Off	22.1
				0: Hiccup	19.1
0100: 0.7500 V				1: Latch-Off	16.5
				0: Hiccup	14.3
0011: 0.6992 V				1: Latch-Off	12.1
				0: Hiccup	10
0010: 0.6504 V				1: Latch-Off	7.87
				0: Hiccup	6.19
0001: 0.5996 V				1: Latch-Off	4.64
				0: Hiccup	3.16
0000: **0.975 V**				1: Latch-Off	1.78
				0: Hiccup	0

(1) 1% or better and connect to ground

7.5.1.3 DCAP3 Control and Mode Selection

The MODE pinstrap configuration programs the control topology and internal soft-start timing selections. The device supports both DCAP3 and DCAP operation modes.

MODE[4] selection bit is used to set the control topology. If MODE[4] bit is 0, it selects DCAP operation. If MODE[4] bit is 1, it selects DCAP3 operation.

MODE[1] and MODE[0] selection bits are used to set the internal soft-start timing.

Table 4. Allowable MODE Pin Selections

MODE[4]	MODE[3]	MODE[2]	MODE[1]	MODE[0]	R_{MODE} (kΩ) (1)
1: DCAP3	0: Internal Reference	0: Internal SS	11: 8 ms (2)		60.4
			10: 4 ms (2)		53.6
			01: 2 ms		47.5
			00: 1 ms		42.2
0: DCAP	0: Internal Reference	0: Internal SS	11: 8 ms (2)		4.64
			10: 4 ms (2)		3.16
			01: 2 ms		1.78
			00: 1 ms		0

(1) R_{MODE} settings in lighter shade are not permitted (24 settings).
(2) See *Application Workaround to Support 4-ms and 8-ms SS Settings*.

7.5.1.4 Application Workaround to Support 4-ms and 8-ms SS Settings

In order to properly design for 4-ms and 8-ms SS settings, additional application consideration is needed. The recommended application workaround to support the 4-ms and 8-ms soft-start settings is to ensure sufficient time delay between the VDD and EN_UVLO signals. The minimum delay between the rising maximum VDD_UVLO level and the minimum turnon threshold of EN_UVLO is at least T_{DELAY_MIN}.

$$T_{DELAY\_MIN} = K \times V_{REF}$$

where

- K = 9 ms/V for SS setting of 4 ms
- K = 18 ms/V for SS setting of 8 ms
- V_{REF} is the internal reference voltage programmed by VSEL pin strap (1)

For example, if SS setting is 4 ms and V_{REF} = 1 V, program the minimum delay at least 9 ms; if SS setting is 8 ms, the minimum delay should be programmed at least 18 ms. See Figure 17 and Figure 18 for detailed timing requirement.

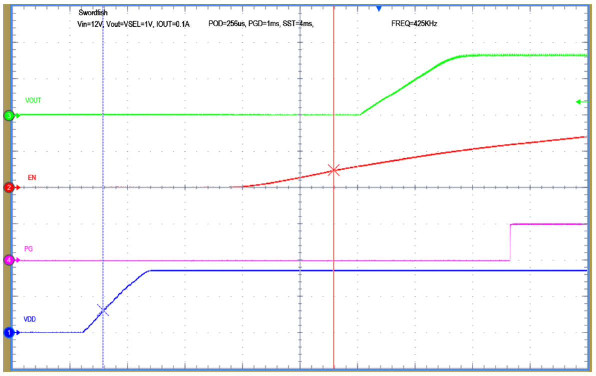


Figure 17. Proper Sequencing of V_{DD} and EN_UVLO to Support the use of 4-ms SS Setting

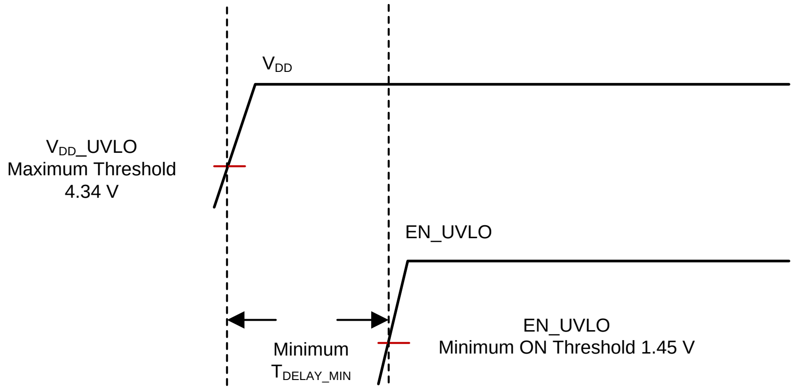


Figure 18. Minimum Delay Between V_{DD} and EN_UVLO to Support the use of 4-ms and 8-ms SS settings

The workaround/consideration described previously is not required for SS settings of 1 ms and 2 ms.

7.5.2 Programmable Analog Configurations

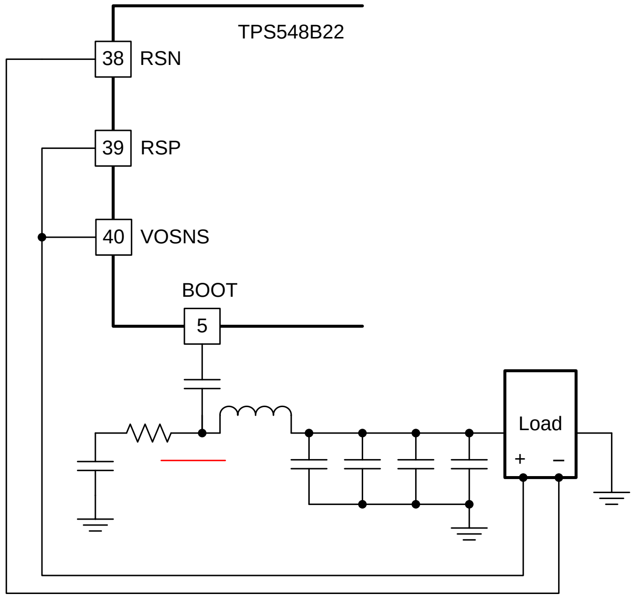
7.5.2.1 RSP/RSN Remote Sensing Functionality

RSP and RSN pins are used for remote sensing purpose. In the case where feedback resistors are required for output voltage programming, connect the RSP pin to the mid-point of the resistor divider; always connect the RSN pin to the load return. When feedback resistors are not required as when the VSEL programs the output voltage setpoint, always connect the RSP pin to the positive sensing point of the load, and always connect the RSN pin to the load return.

RSP and RSN pins are extremely high-impedance input terminals of the true differential remote sense amplifier. The feedback resistor divider must use resistor values much less than 100 kΩ.

7.5.2.1.1 Output Differential Remote Sensing Amplifier

The examples in this section show simplified remote sensing circuitry that each use an internal reference of 1 V. Figure 19 shows remote sensing without feedback resistors, with an output voltage setpoint of 1 V. Figure 20 shows remote sensing using feedback resistors, with an output voltage set point of 5 V.



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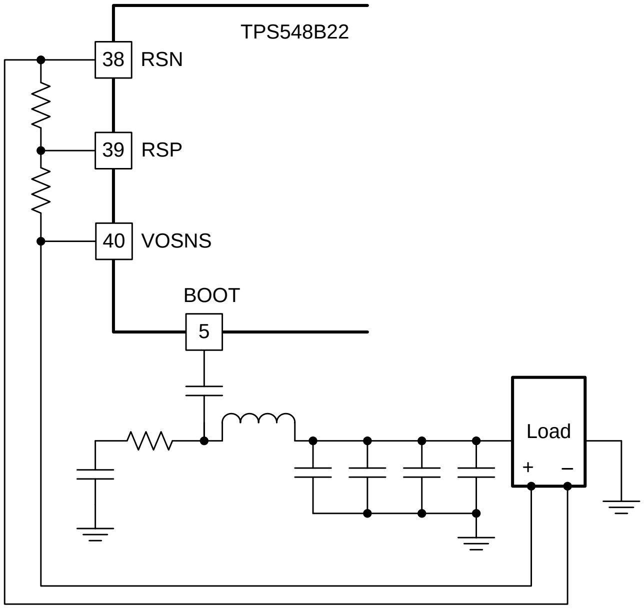

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Figure 19. Remote Sensing Without Feedback Resistors

Figure 20. Remote Sensing With Feedback Resistors

7.5.2.2 Power Good (PGOOD Pin) Functionality

The TPS548B22 device has power-good output that registers high when switcher output is within the target. The power-good function is activated after soft-start has finished. When the soft-start ramp reaches 300 mV above the internal reference voltage, SSend signal goes high to enable the PGOOD detection function. If the output voltage becomes within ±8% of the target value, internal comparators detect power-good state, and the power-good signal becomes high after a 1-ms programmable delay. If the output voltage goes outside of ±16% of the target value, the power good signal becomes low after two microsecond (2-µs) internal delay. The open-drain, power-good output must be pulled up externally.

The internal N-channel MOSFET does not pull down until the VDD supply is above 1.2 V.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS548B22 device is a highly integrated synchronous step-down DC-DC converters. These devices are used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 25 A. Use the following design procedure to select key component values for this family of devices.

8.2 Typical Applications

8.2.1 TPS548B22 1.5-V to 18-V Input, 1-V Output, 25-A Converter

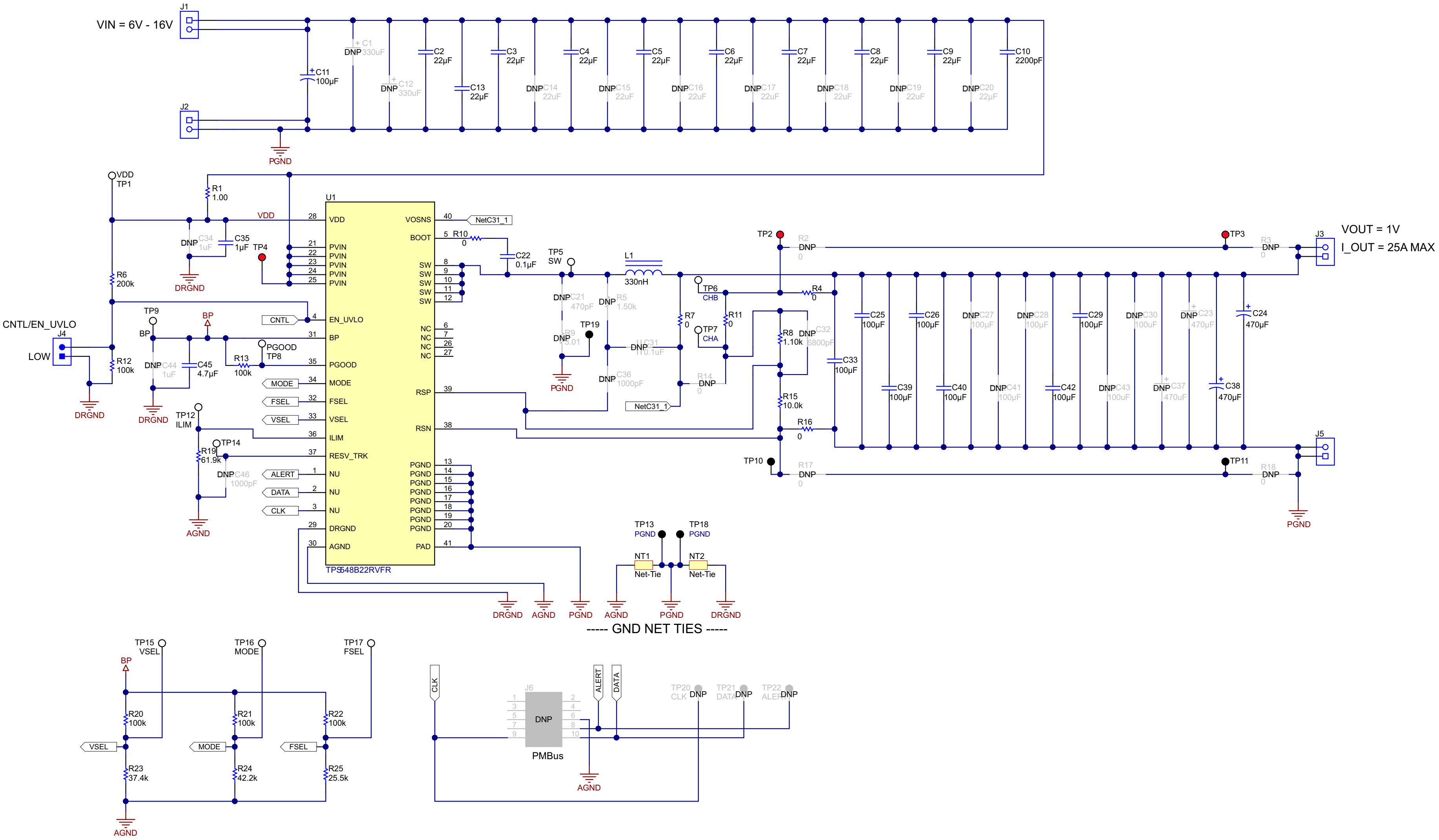


Figure 21. Typical Application Schematic

8.2.2 Design Requirements

For this design example, use the input parameters shown in Table 5.

Table 5. Design Example Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		5	12	18	V
$V_{IN(ripple)}$	Input ripple voltage	I_{OUT} = 25 A			0.4	V
V_{OUT}	Output voltage			1		V
	Line regulation	5 V ≤ V_{IN} ≤ 18 V			0.5%	
	Load regulation	0 V ≤ I_{OUT} ≤ 25 A			0.5%	
V_{PP}	Output ripple voltage	I_{OUT} = 25 A		10		mV
V_{OVER}	Transient response overshoot	I_{STEP} = 15 A		30		mV
V_{UNDER}	Transient response undershoot	I_{STEP} = 15 A		30		mV
I_{OUT}	Output current	5 V ≤ V_{IN} ≤ 18 V			25	A
t_{SS}	Soft-start time			1		ms
I_{OC}	Overcurrent trip point(1)			32		A
η	Peak efficiency	I_{OUT} = 7 A		90%		
f_{SW}	Switching frequency			650		kHz

(1) DC overcurrent level

8.2.3 Design Procedure

8.2.3.1 Switching Frequency Selection

Select a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impact thermal performance. In this design, a moderate switching frequency of 650 kHz achieves both a small solution size and a high-efficiency operation with the frequency selected.

Select one of four switching frequencies and FSEL resistor values from Table 6. The recommended high-side R_{FSEL} value is 100 kΩ (1%). Choose a low-side resistor value from Table 6 based on the choice of switching frequency. For each switching frequency selection, there are multiple values of $R_{FSEL(LS)}$ to choose from. In order to select the correct value, additional considerations (internal ramp compensation and light load operation) other than switching frequency need to be included.

Table 6. FSEL Pin Selection

SWITCHING FREQUENCY f_{SW} (kHz)	FSEL VOLTAGE V_{FSEL} (V)		HIGH-SIDE RESISTOR $R_{FSEL(HS)}$ (kΩ) 1% or better	LOW-SIDE RESISTOR $R_{FSEL(LS)}$ (kΩ) 1% or better
	MAXIMUM	MINIMUM		
1050	2.93	1.465	100	Open
				187
				165
				147
				133
				121
				110
				100
875	1.396	0.869	100	90.9
				82.5
				75
				68.1
				60.4
				53.6
				47.5
				42.2
650	0.798	0.366	100	37.4
				33.2
				29.4
				25.5
				22.1
				19.1
				16.5
				14.3
425	0.317	0	100	12.1
				10
				7.87
				6.19
				4.64
				3.16
				1.78
				0

There is some limited freedom to choose FSEL resistors that have other than the recommended values. The criteria is to ensure that for particular selection of switching frequency, the FSEL voltage is within the maximum and minimum FSEL voltage levels listed in Table 6. Use Equation 2 to calculate the FSEL voltage. Select FSEL resistors that include tolerances of 1% or better.

$$V_{FSEL} = V_{BP(det)} \times \frac{R_{FSEL(LS)}}{R_{FSEL(HS)} + R_{FSEL(LS)}}$$

where

- $V_{BP(det)}$ is the voltage used by the device to program the level of valid FSEL pin voltage during initial device start-up (2.9 V typical) (2)

In addition to serving the frequency select purpose, the FSEL pin can also be used to program internal ramp compensation (DCAP3) and light-load conduction mode. When DCAP3 mode is selected (see section 8.2.3.9), internal ramp compensation is used for stabilizing the converter design. The internal ramp compensation is a function of the switching frequency (f_{SW}) and the duty cycle range (the output voltage-to-input voltage ratio). Table 7 summarizes the ramp choices using these functions.

Table 7. Switching Frequency Selection

SWITCHING FREQUENCY SETTING (f_{SW}) (kHz)	RAMP SELECT OPTION	TIME CONSTANT t (µs)	V_{OUT} RANGE (FIXED V_{IN} = 12 V)		DUTY CYCLE RANGE (V_{OUT}/V_{IN}) (%)	
			MIN	MAX	MIN	MAX
425	R/2	9	0.6	0.9	5	7.5
	R × 1	16.8	0.9	1.5	7.5	12.5
	R × 2	32.3	1.5	2.5	12.5	21
	R × 3	55.6	2.5	5.5	>21	
650	R/2	7	0.6	0.9	5	7.5
	R × 1	13.5	0.9	1.5	7.5	12.5
	R × 2	25.9	1.5	2.5	12.5	21
	R × 3	44.5	2.5	5.5	>21	
875	R/2	5.6	0.6	0.9	5	7.5
	R × 1	10.4	0.9	1.5	7.5	12.5
	R × 2	20	1.5	2.5	12.5	21
	R × 3	34.4	2.5	5.5	>21	
1050	R/2	3.8	0.6	0.9	5	7.5
	R × 1	7.1	0.9	1.5	7.5	12.5
	R × 2	13.6	1.5	2.5	12.5	21
	R × 3	23.3	2.5	5.5	>21	

The FSEL pin programs the light-load selection. TPS548B22 device supports either SKIP mode or FCCM operations. For optimized light-load efficiency, it is recommended to program the device to operate in SKIP mode. For better load regulation from no load to full load, it is recommended to program the device to operate in FCCM mode.

$R_{FSEL(LS)}$ can be determined after determining the switching frequency, ramp and light-load operation. Table 2 lists the full range of choices.

8.2.3.2 Inductor Selection

To calculate the value of the output inductor, use Equation 3. The coefficient K_{IND} represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, maintain a K_{IND} coefficient greater than 0 and 0.4 for balanced performance. Using this target ripple current, the required inductor size can be calculated as shown in Equation 3:

$$L1 = \frac{V_{OUT}}{\left(V_{IN(max)} \times f_{SW}\right)} \times \frac{V_{IN} - V_{OUT}}{\left(I_{OUT(max)} \times K_{IND}\right)} = \frac{1\text{ V} \times \left(18\text{ V} - 1\text{ V}\right)}{18\text{ V} \times 650\text{ kHz} \times 25\text{ A} \times 0.2} = 0.29\ \mu\text{H} \tag{3}$$

Selecting a K_{IND} of 0.2, the target inductance L_1 = 290 nH. Using the next standard value, the 330 nH is chosen in this application for its high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using Equation 4, Equation 5 and Equation 6. These values should be used to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{V_{OUT}}{\left(V_{IN(max)} \times f_{SW}\right)} \times \frac{V_{IN(max)} - V_{OUT}}{L1} = \frac{1\text{ V} \times \left(18\text{ V} - 1\text{ V}\right)}{18\text{ V} \times 650\text{ kHz} \times 330\text{ nH}} = 4.4\text{ A} \tag{4}$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times (I_{RIPPLE})^2} = 25\text{ A} \tag{5}$$

$$I_{L(PEAK)} = (I_{OUT}) + \frac{1}{2} \times (I_{RIPPLE}) = 27.2\text{ A} \tag{6}$$

8.2.3.3 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

8.2.3.3.1 Minimum Output Capacitance to Ensure Stability

To prevent sub-harmonic multiple pulsing behavior, TPS548B22 application designs must strictly follow the small signal stability considerations described in Equation 7.

$$C_{OUT(min)} > \frac{t_{ON}}{2} \times \frac{8\tau}{L_{OUT}} \times \frac{V_{REF}}{V_{OUT}}$$

where

- $C_{OUT(min)}$ is the minimum output capacitance needed to meet the stability requirement of the design
- t_{ON} is the on-time information based on the switching frequency and duty cycle (in this design, 128 ns)
- τ is the ramp compensation time constant of the design based on the switching frequency and duty cycle, (in this design, 25.9 µs, refer to Table 7)
- L_{OUT} is the output inductance (in the design, 0.33 µH)
- V_{REF} is the user-selected reference voltage level (in this design, 1 V)
- V_{OUT} is the output voltage (in this design, 1 V) (7)

The minimum output capacitance calculated from Equation 7 is 40 µF. The stability is ensured when the amount of the output capacitance is 40 µF or greater. And when all MLCCs (multi-layer ceramic capacitors) are used, both DC and AC derating effects must be considered to ensure that the minimum output capacitance requirement is met with sufficient margin.

8.2.3.3.2 Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

Use Equation 8 and Equation 9 to estimate the amount of capacitance needed for a given dynamic load step and release.

NOTE

There are other factors that can impact the amount of output capacitance for a specific design, such as ripple and stability.

$$C_{OUT(min\_under)} = \frac{L_{OUT} \times (\Delta I_{LOAD(max)})^2 \times \left(\frac{V_{OUT} \times t_{SW}}{V_{IN(min)}} + t_{OFF(min)}\right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{OFF(min)}\right) \times V_{OUT}} \tag{8}$$

$$C_{OUT\,(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD\,(max)}\right)^2}{2 \times \Delta V_{LOAD\,(release)} \times V_{OUT}}$$

where

- $C_{OUT(min\_under)}$ is the minimum output capacitance to meet the undershoot requirement
- $C_{OUT(min_over)}$is the minimum output capacitance to meet the overshoot requirement
- L is the output inductance value (0.33 µH)
- $\Delta I_{LOAD(max)}$ is the maximum transient step (15 A)
- V_{OUT} is the output voltage value (1 V)
- t_{SW} is the switching period (1.54 µs)
- $V_{IN(min)}$ is the minimum input voltage for the design (10.8 V)
- $t_{OFF(min)}$ is the minimum off time of the device (300 ns)
- $\Delta V_{LOAD(insert)}$ is the undershoot requirement (30 mV)
- $\Delta V_{LOAD(release)}$ is the overshoot requirement (30 mV) (9)

Most of the above parameters can be found in Table 5.

The minimum output capacitance to meet the undershoot requirement is 516 µF. The minimum output capacitance to meet the overshoot requirement is 1238 µF. This example uses a combination of POSCAP and MLCC capacitors to meet the overshoot requirement.

- POSCAP bank no. 1: 2 × 470 µF, 2.5 V, 6 mΩ per capacitor
- MLCC bank no. 2: 7 × 100 µF, 6.3 V, 2 mΩ per capacitor with DC+AC derating factor of 60%

Recalculating the worst case overshoot using the described capacitor bank design, the overshoot is 29 mV, which meets the 30-mV overshoot specification requirement.

8.2.3.3.3 Output Voltage Ripple

The output voltage ripple is another important design consideration. Equation 10 calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement when the impedance of the output capacitance is dominated by ESR.

$$C_{COUT(min)RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times V_{OUT(RIPPLE)}} = 82\ \mu F \tag{10}$$

In this case, the maximum output voltage ripple is 10 mV. For this requirement, the minimum capacitance for ripple requirement yields 82 µF. Because this capacitance value is significantly lower compared to that of transient requirement, determine the capacitance bank from *Response to a Load Transient*. Because the output capacitor bank consists of both POSCAP and MLCC type capacitors, it is important to consider the ripple effect at the switching frequency due to effective ESR. Use Equation 11 to determine the maximum ESR of the output capacitor bank for the switching frequency.

$$ESR_{MAX} = \frac{V_{out(ripple)} - \dfrac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}}{I_{RIPPLE}} = 2.2\ m\Omega \tag{11}$$

Estimate the effective ESR at the switching frequency by obtaining the impedance vs frequency characteristics of the output capacitors. The parallel impedance of capacitor bank #1 and capacitor bank #2 at the switching frequency of the design example is estimated to be 1.2 mΩ, which is less than that of the maximum ESR value. Therefore, the output voltage ripple requirement (10 mV) can be met. For detailed calculation on the effective ESR please contact the factory to obtain a user-friendly Excel based design tool.

8.2.3.4 Input Capacitor Selection

The TPS548B22 requires a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 µF of effective capacitance on the VDD pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the PVIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using Equation 12.

$$I_{CIN(rms)} = I_{OUT(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 10 \text{ Arms} \tag{12}$$

The minimum input capacitance and ESR values for a given input voltage ripple specification, $V_{IN(ripple)}$, are shown in Equation 13 and Equation 14. The input ripple is composed of a capacitive portion, $V_{RIPPLE(cap)}$, and a resistive portion, $V_{RIPPLE(esr)}$.

$$C_{IN(min)} = \frac{I_{OUT(max)} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN(max)} \times f_{SW}} = 21.4 \ \mu F \tag{13}$$

$$ESR_{CIN(max)} = \frac{V_{RIPPLE(ESR)}}{I_{OUT(max)} + \left(\frac{I_{RIPPLE}}{2}\right)} = 3.4 \ m\Omega \tag{14}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, allow 0.1-V input ripple for $V_{RIPPLE(cap)}$, and 0.1-V input ripple for $V_{RIPPLE(esr)}$. Using Equation 13 and Equation 14, the minimum input capacitance for this design is 21.4 µF, and the maximum ESR is 3.4 mΩ. For this example, four 22-µF, 25-V ceramic capacitors and one additional 100-µF, 25-V low-ESR polymer capacitors in parallel were selected for the power stage.

8.2.3.5 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

8.2.3.6 BP Pin

Bypass the BP pin to DRGND with 4.7-µF capacitance. In order for the regulator to function properly, it is important that these capacitors be localized to the , with low-impedance return paths. See *Layout Guidelines* section for more information.

8.2.3.7 R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the TPS548B22 within absolute maximum ratings without ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the SW area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this example twoone 2.2-nF, 25-V, 0603-sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness. Its ideal placement is shown in Figure 21.

Additionally, an R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 1-nF capacitor and a 1-Ω resistor are chosen. In this example a 0805-sized resistor is chosen, which is rated for 0.125 W, nearly twice the estimated power dissipation. See SLUP100 for more information about snubber circuits.

8.2.3.8 Optimize Reference Voltage (VSEL)

Optimize the reference voltage by choosing a value for R_{VSEL}. The TPS548B22 device is designed with a wide range of precision reference voltage support from 0.6 V to 1.2 V with an available step change of 50 mV. Program these reference voltages using the VSEL pin strap configurations. See Table 3 for internal reference voltage selections. In addition to providing initial boot voltage value, use the VSEL pin to program hiccup and latch-off mode.

There are two ways to program the output voltage set point. If the output voltage set point is one of the 16 available reference and boot voltage options, no feedback resistors are required for output voltage programming. In the case where feedback resistors are not needed, connect the RSP pin to the positive sensing point of the load. Always connect the RSN pin to the load return sensing point.

In this design example, since the output voltage set point is 1 V, selecting $R_{VSEL(LS)}$ of either 75 kΩ (latch off) or 68.1 kΩ (hiccup). If the output voltage set point is NOT one of the 16 available reference or boot voltage options, feedback resistors are required for output voltage programming. Connect the RSP pin to the mid-point of the resistor divider. Always connect the RSN pin to the load return sensing point as shown in Figure 19 and Figure 20.

The general guideline to select boot and internal reference voltage is to select the reference voltage closest to the output voltage set point. In addition, because the RSP and RSN pins are extremely high-impedance input terminals of the true differential remote sense amplifier, use a feedback resistor divider with values much less than 100 kΩ.

8.2.3.9 MODE Pin Selection

MODE pin strap configuration is used to program control topology and internal soft-start timing selections. TPS548B22 supports both DCAP3 and DCAP operation. For general POL applications, it is strongly recommended to configure the control topology to be DCAP3 due to its simple to use and no external compensation features. In the rare instance where DCAP is needed, an RCC network across the output inductor is needed to generate sufficient ripple voltage on the RSP pin. In this design example, $R_{MODE(LS)}$ of 22.1 kΩ is selected for DCAP3 and soft start time of 1 ms.

8.2.3.10 Overcurrent Limit Design.

The TPS548B22 device uses the ILIM pin to set the OCP level. Connect the ILIM pin to GND through the voltage setting resistor, R_{ILIM}. In order to provide both good accuracy and cost effective solution, this device supports temperature compensated MOSFET on-resistance ($R_{DS(on)}$) sensing. Also, this device performs both positive and negative inductor current limiting with the same magnitudes. Positive current limit is normally used to protect the inductor from saturation therefore causing damage to the high-side and low-side FETs. Negative current limit is used to protect the low-side FET during OVP discharge.

The inductor current is monitored by the voltage between PGND pin and SW pin during the OFF time. The ILIM pin has 1200 ppm/°C temperature slope to compensate the temperature dependency of the on-resistance. The PGND pin is used as the positive current sensing node.

TPS548B22 has cycle-by-cycle over-current limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent ILIM level. The voltage on the ILIM pin (V_{ILIM}) sets the valley level of the inductor current. The range of value of the R_{ILIM} resistor is between 9.53 kΩ and 105 kΩ. The range of valley OCL is between 5 A and 50 A (typical). If the R_{ILIM} resistance is outside of the recommended range, OCL accuracy and function cannot be assured. (see Table 8)

Table 8. OCP Valley Settings

1% R_{ILIM} (kΩ)	OVERCURRENT PROTECTION VALLEY (A)
82.1	40
71.5	35
61.9	30
51.1	25
40.2	20
30.1	15
20.5	10

Use Equation 15 to relate the valley OCL to the R_{ILIM} resistance.

$$R_{ILIM} = 2.0664 \times OCL_{VALLEY} - 0.6036$$

where

- R_{ILIM} is in kΩ
- OCL_{VALLEY} is in A (15)

In this design example, the desired valley OCL is 30 A, the calculated R_{ILIM} is 61.9 kΩ. Use Equation 16 to calculate the DC OCL to be 32.1 A.

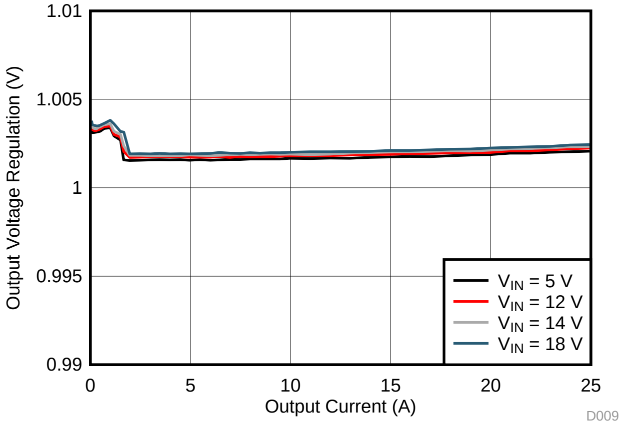
$$\text{OCL}_{\text{DC}} = \text{OCL}_{\text{VALLEY}} + 0.5 \times \text{I}_{\text{RIPPLE}}$$

where

- R_{ILIM} is in kΩ
- OCL_{DC} is in A (16)

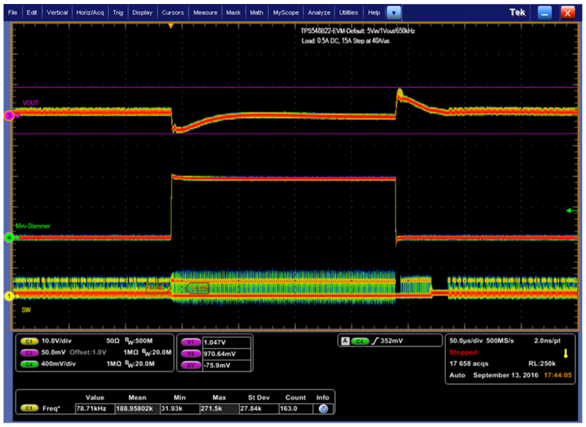
In an overcurrent condition, the current to the load exceeds the inductor current and the output voltage falls. When the output voltage crosses the under-voltage fault threshold for at least 1msec, the behavior of the device depends on the VSEL pin strap setting. If hiccup mode is selected, the device will restart after 16-ms delay (1-ms soft-start option). If the overcurrent condition persists, the OC hiccup behavior repeats. During latch-off mode operation the device shuts down until the EN pin is toggled or VDD pin is power cycled.

8.2.4 Application Curves



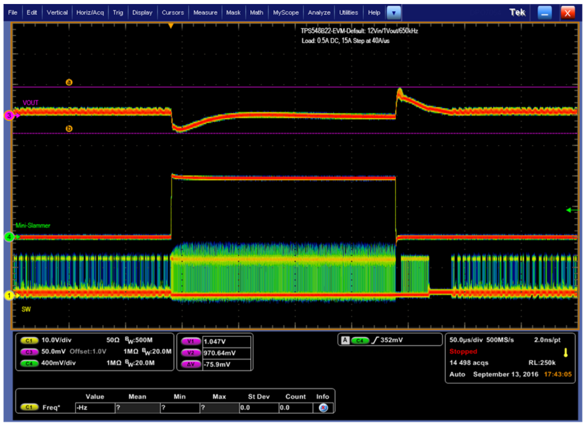
$V_{DD} = V_{IN}$ f_{SW} = 650 kHz SKIP Mode
V_{OUT} = 1 V

Figure 22. Output Voltage Regulation vs Output Current



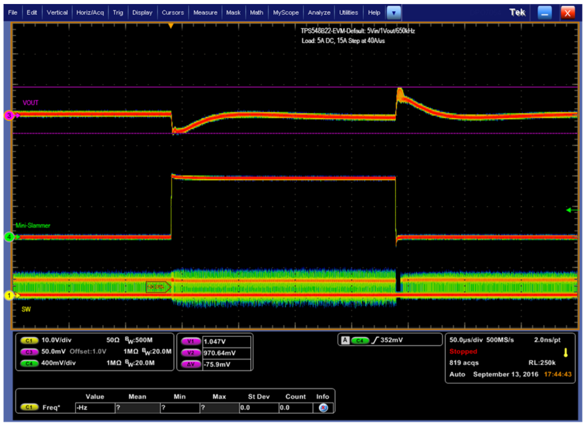
$V_{DD} = V_{IN}$ = 5 V f_{SW} = 650 kHz SKIP Mode
V_{OUT} = 1 V 0.5 A DC with 15-A step at 40A/µs

Figure 23. Transient Response Peak-to-Peak



$V_{DD} = V_{IN}$ = 12 V f_{SW} = 650 kHz SKIP Mode
V_{OUT} = 1 V 0.5 A DC with 15-A step at 40A/µs

Figure 24. Transient Response Peak-to-Peak



$V_{DD} = V_{IN}$ = 5 V f_{SW} = 650 kHz FCCM Mode
V_{OUT} = 1 V 5 A DC with 15-A step at 40A/µs

Figure 25. Transient Response Peak-to-Peak

$V_{DD} = V_{IN}$ = 12 V f_{SW} = 650 kHz FCCM Mode
V_{OUT} = 1 V 5 A DC with 15-A step at 40A/µs

Figure 26. Transient Response Peak-to-Peak

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply between 1.5 V and 18 V. Ensure the supply is well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is the quality of the PCB layout and grounding scheme. See the recommendations in the *Layout* section.

10 Layout

10.1 Layout Guidelines

Consider these layout guidelines before starting a layout work using TPS548B22.

- It is absolutely critical that all GND pins, including AGND (pin 30), DRGND (pin 29), and PGND (pins 13, 14, 15, 16, 17, 18, 19, and 20) are connected directly to the thermal pad underneath the device via traces or plane.
- Include as many thermal vias as possible to support a 25-A thermal operation. For example, a total of 35 thermal vias are used (outer diameter of 20 mil) in the TPS548B22EVM-847 available for purchase at ti.com. (SLUUBE4)
- Place the power components (including input/output capacitors, output inductor and TPS548B22 device) on one side of the PCB (solder side). Insert at least two inner layers (or planes) connected to the power ground, in order to shield and isolate the small signal traces from noisy power lines.
- Place the VIN pin decoupling capacitors as close as possible to the PVIN and PGND pins to minimize the input AC current loop. Place a high-frequency decoupling capacitor (with a value between 1 nF and 0.1 µF) as close to the PVIN pin and PGND pin as the spacing rule allows. This placement helps surpress the switch node ringing.
- Place VDD and BP decoupling capacitors as close as possible to the device pins. Do not use PVIN plane connection for the VDD pin. Separate the VDD signal from the PVIN signal by using separate trace connections. Provide GND vias for each decoupling capacitor and make the loop as small as possible.
- Ensure that the PCB trace defined as switch node (which connects the SW pins and up-stream of the output inductor) are as short and wide as possible. In the TPS548B22EVM-847 design, the SW trace width is 200 mil. Use a separate via or trace to connect SW node to snubber and bootstrap capacitor. Do not combine these connections.
- Place all sensitive analog traces and components (including VOSNS, RSP, RSN, ILIM, MODE, VSEL and FSEL) far away from any high voltage switch node (itself and others), such as SW and BOOT to avoid noise coupling. In addition, place MODE, VSEL and FSEL programming resistors near the device pins.
- The RSP and RSN pins operate as inputs to a differential remote sense amplifier that operates with very high impedance. It is essential to route the RSP and RSN pins as a pair of diff-traces in Kelvin-sense fashion. Route them directly to either the load sense points (+ and –) or the output bulk capacitors. The internal circuit uses the VOSNS pin for on-time adjustment. It is critical to tie the VOSNS pin directly tied to VOUT (load sense point) for accurate output voltage result.
- Pins 6, 7, and 26 are not connected in the 25-A TPS548B22, while pins 6 and 7 connect to SW and pin 26 connects to PVIN in the 40-A TPS548D22.

10.2 Layout Example

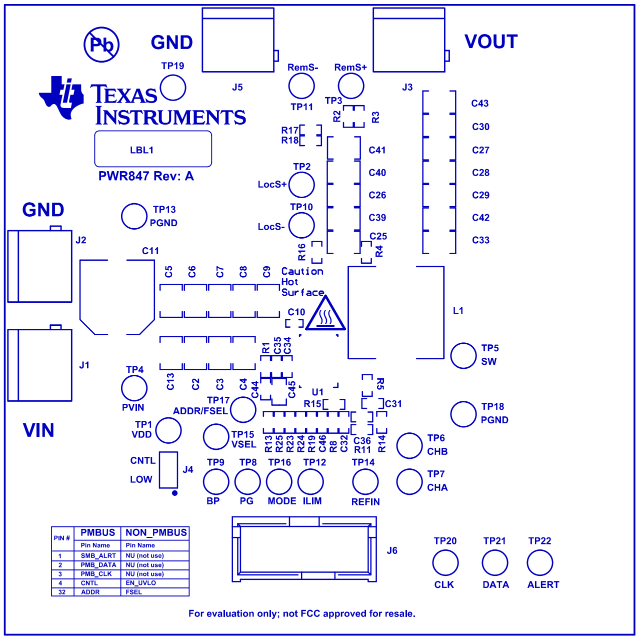


Figure 27. EVM Top View

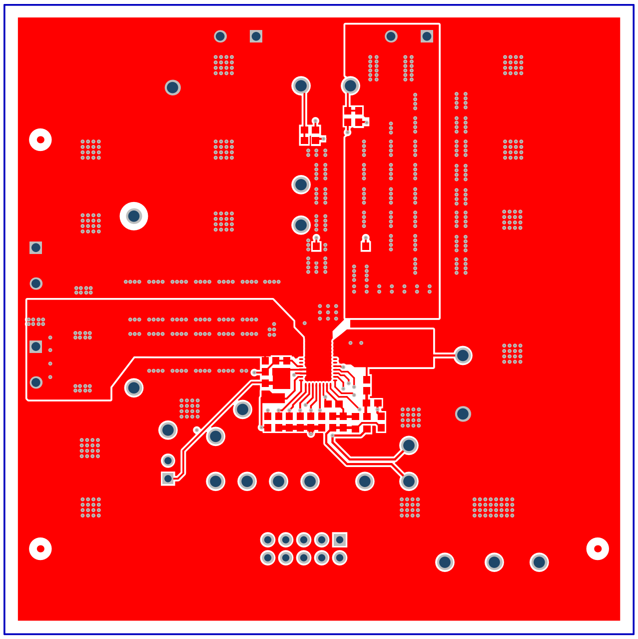


Figure 28. EVM Top Layer

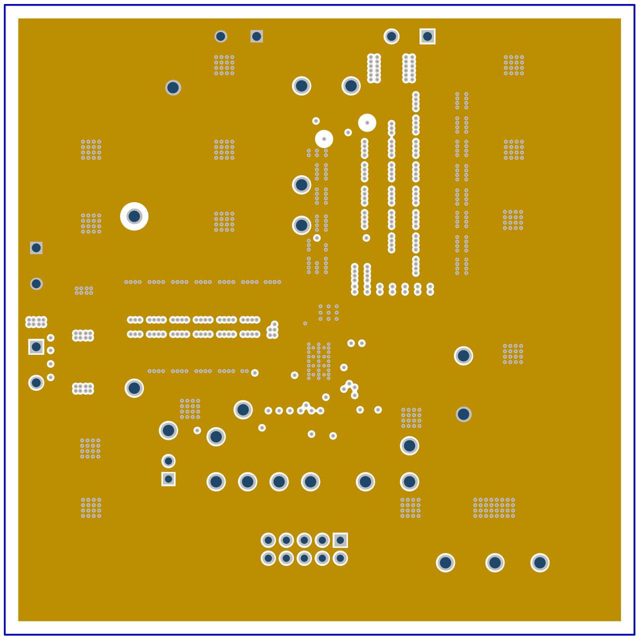


Figure 29. EVM Inner Layer 1

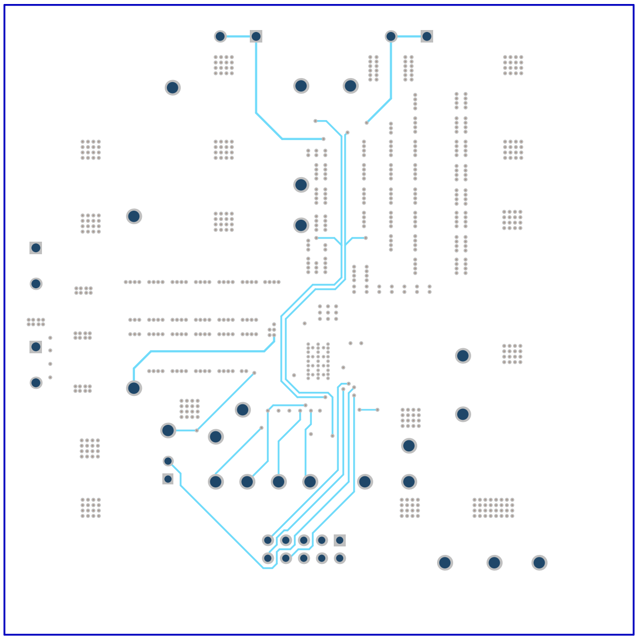


Figure 30. EVM Inner Layer 2

Layout Example (continued)

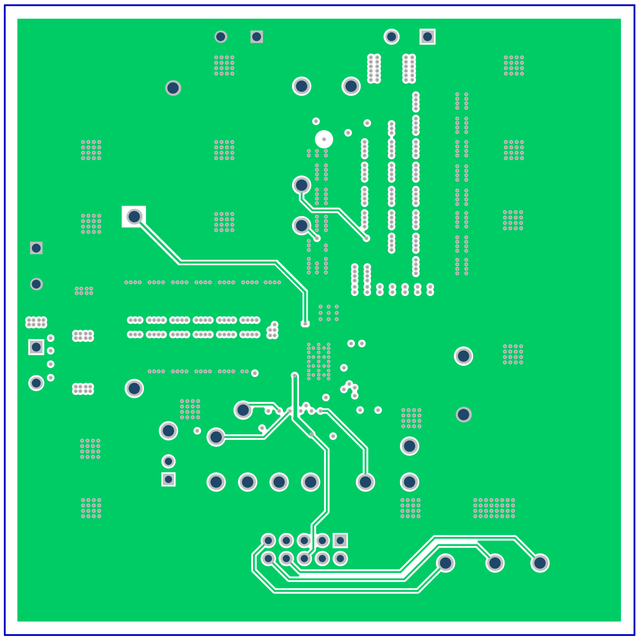


Figure 31. EVM Inner Layer 3

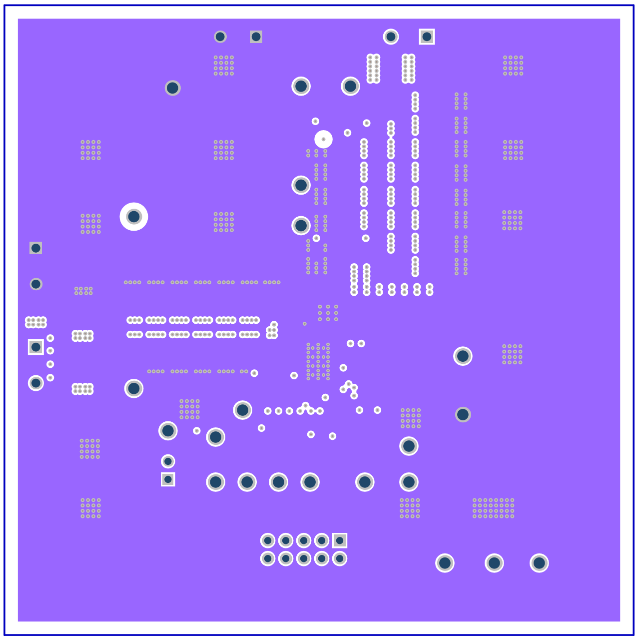


Figure 32. EVM Inner Layer 4

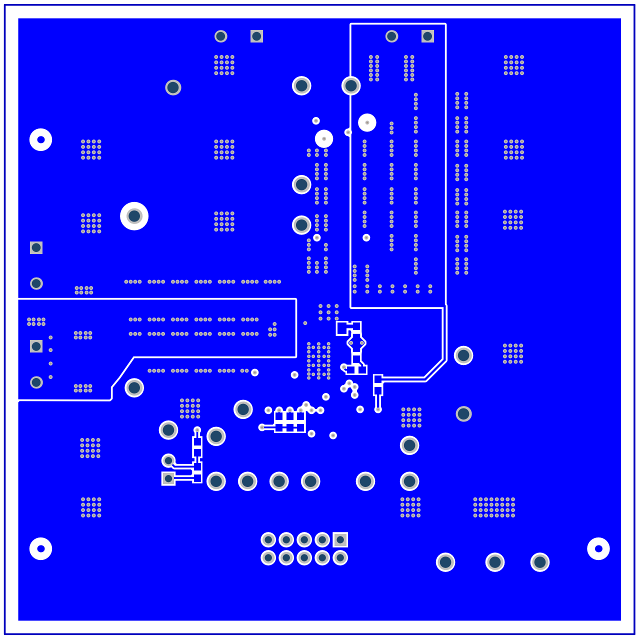


Figure 33. EVM Bottom Layer

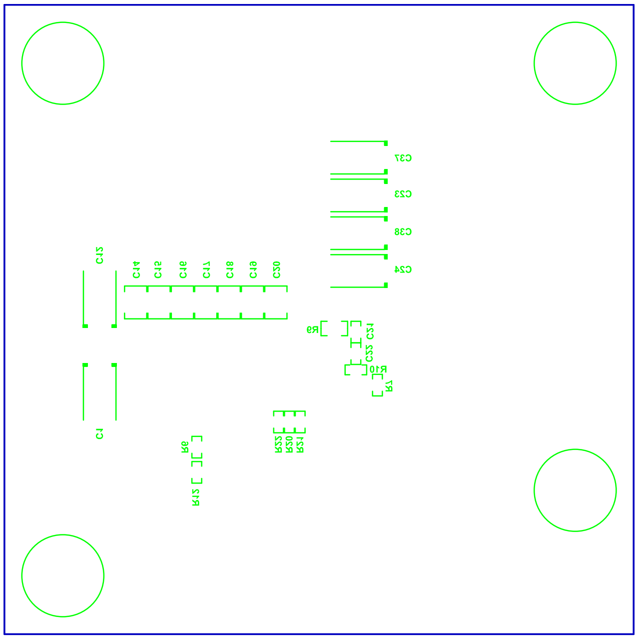


Figure 34. EVM Bottom Symbols

Layout Example (continued)

10.2.1 Mounting and Thermal Profile Recommendation

Proper mounting technique adequately covers the exposed thermal tab with solder. Excessive heat during the reflow process can affect electrical performance. Figure 35 shows the recommended reflow oven thermal profile. Proper post-assembly cleaning is also critical to device performance. See TI Application Report *QFN/SON PCB Attachment* for more information.

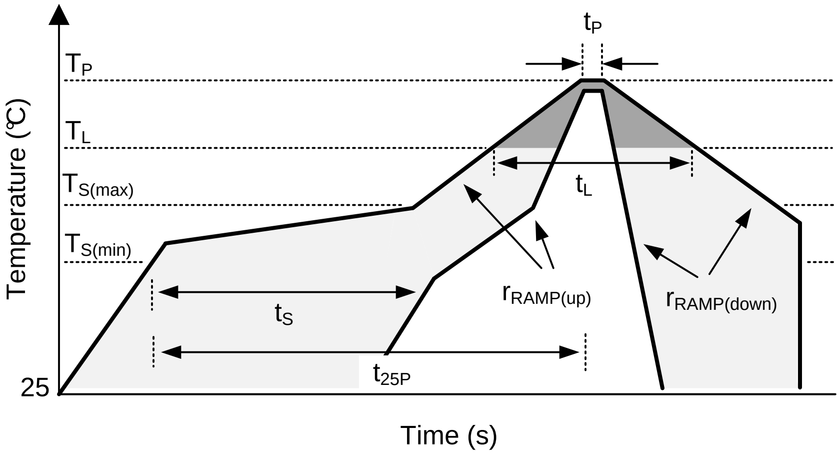


Figure 35. Recommended Reflow Oven Thermal Profile

Table 9. Recommended Thermal Profile Parameters

PARAMETER		MIN	TYP	MAX	UNIT
RAMP UP AND RAMP DOWN					
$r_{RAMP(up)}$	Average ramp-up rate, $T_{S(max)}$ to T_P			3	°C/s
$r_{RAMP(down)}$	Average ramp-down rate, T_P to $T_{S(max)}$			6	°C/s
PRE-HEAT					
T_S	Pre-heat temperature	150		200	°C
t_S	Pre-heat time, $T_{S(min)}$ to $T_{S(max)}$	60		180	s
REFLOW					
T_L	Liquidus temperature		217		°C
T_P	Peak temperature			260	°C
t_L	Time maintained above liquidus temperature, T_L	60		150	s
t_P	Time maintained within 5 °C of peak temperature, T_P	20		40	s
t_{25P}	Total time from 25 °C to peak temperature, T_P			480	s

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TI User Guide *TPS548B22EVM-847, 25-A Single Synchronous Step-Down Converter*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

D-CAP3, NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS548B22RVFR	ACTIVE	LQFN-CLIP	RVF	40	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	548B22A1	Samples
TPS548B22RVFT	ACTIVE	LQFN-CLIP	RVF	40	250	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	548B22A1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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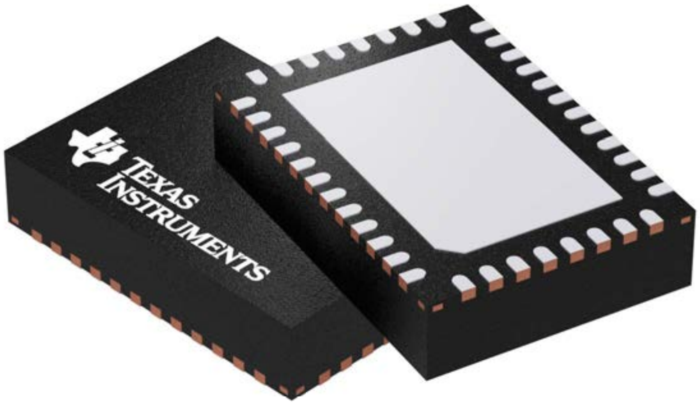
RVF 40

LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

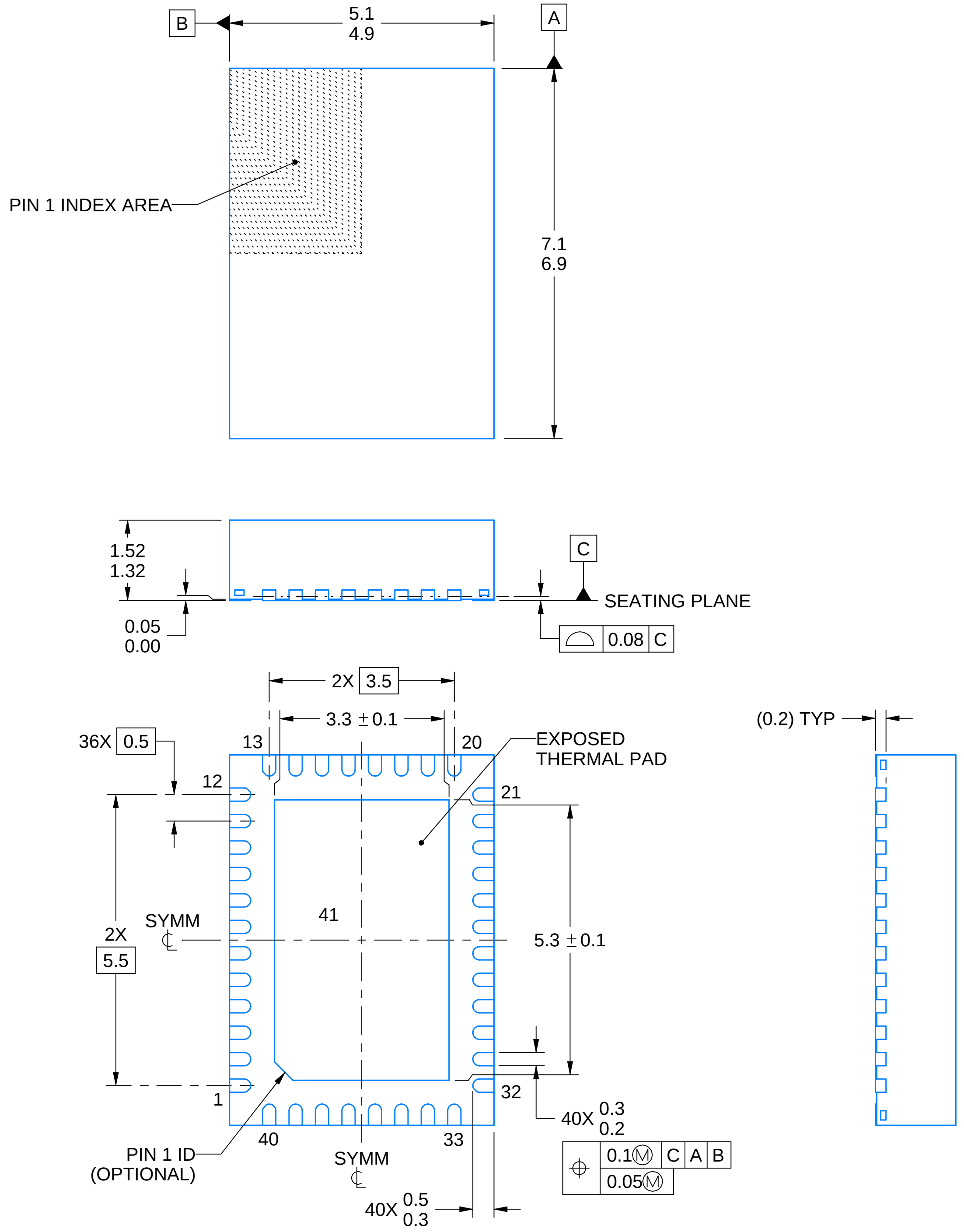


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

LQFN-CLIP - 1.52 mm max height

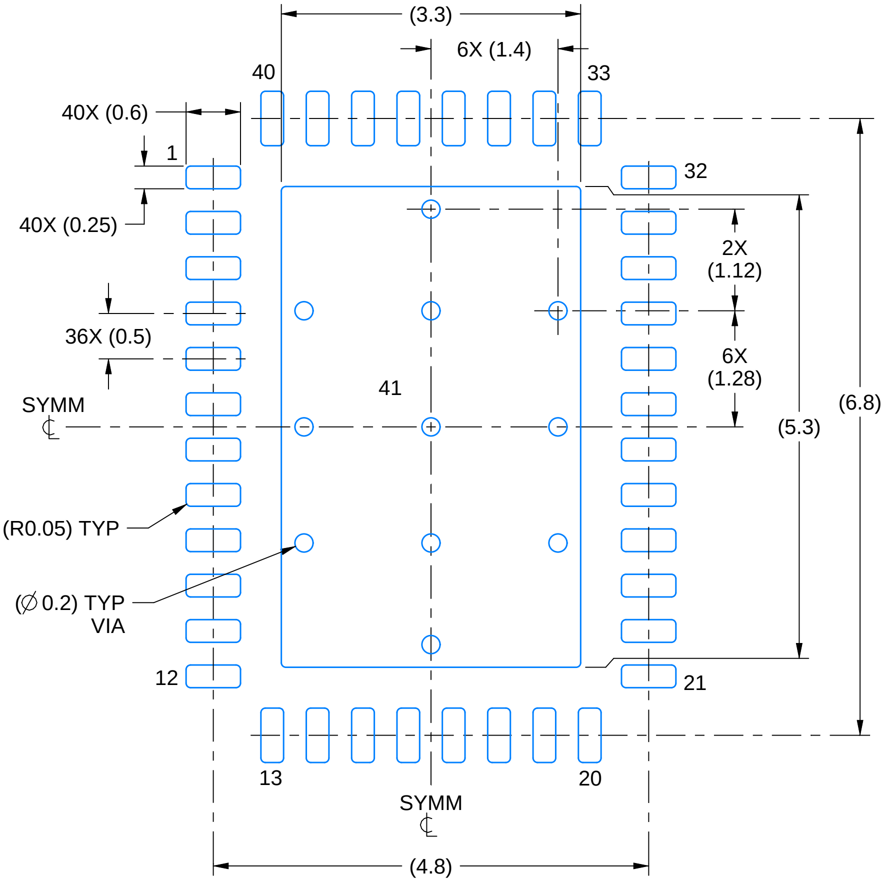
PLASTIC QUAD FLATPACK - NO LEAD



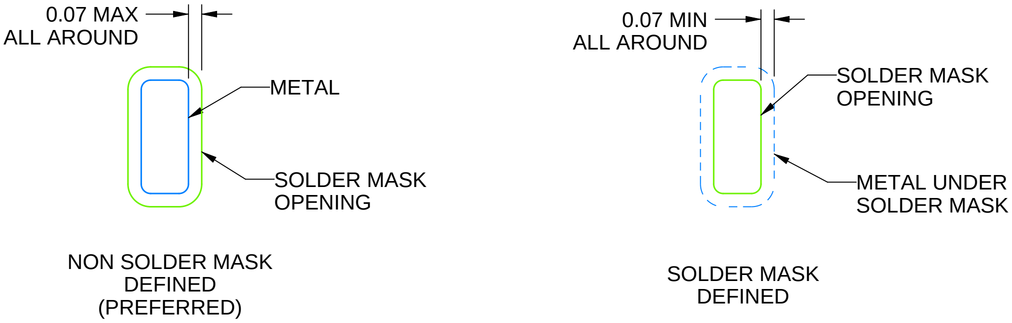
4222989/B 10/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



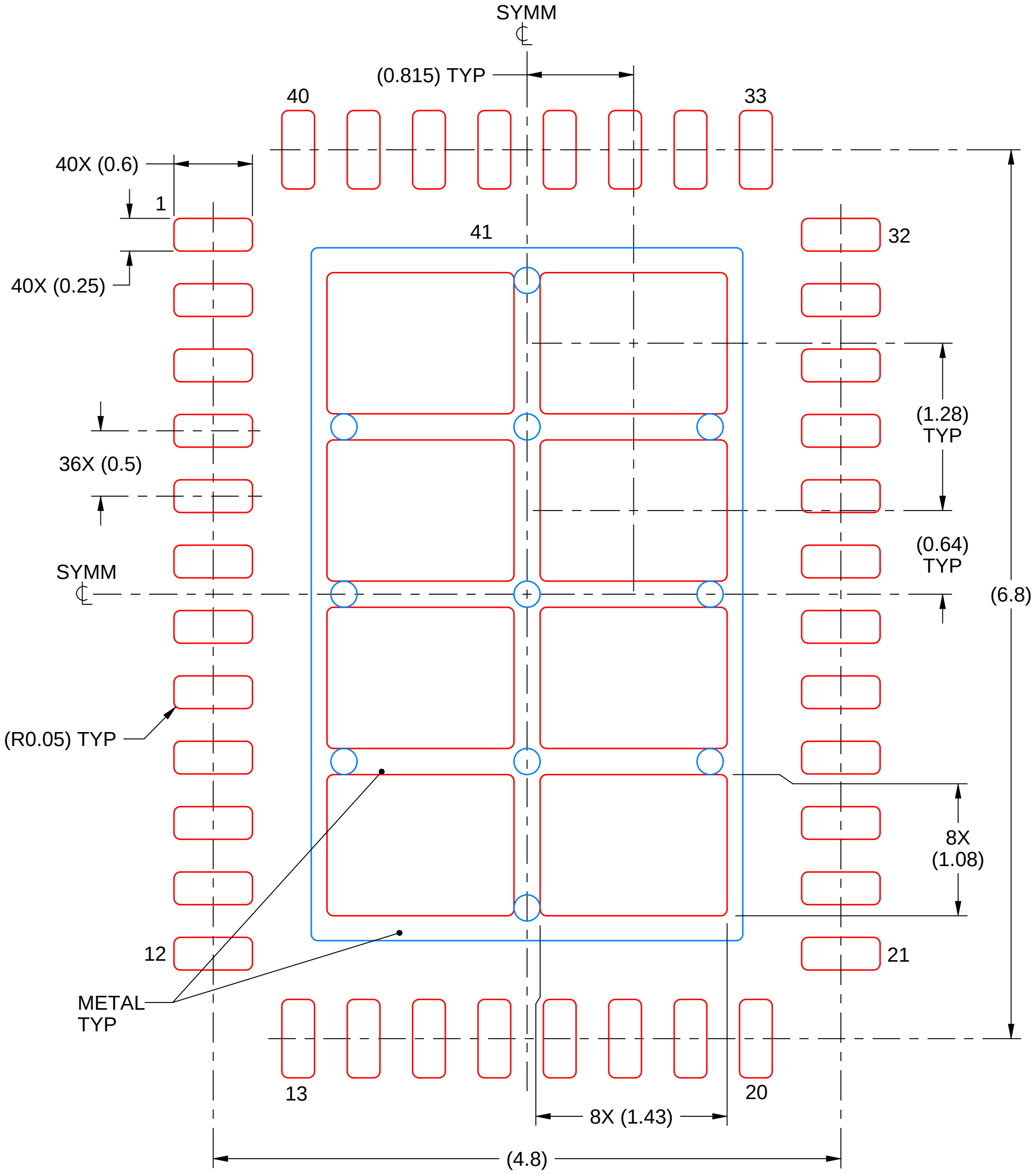
LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222989/B 10/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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