LP5907 250mA, Low-Noise, Low-I_Q LDO

1 Features

- For a more updated portfolio device, see the TPS7A20
- Input voltage range: 2.2V to 5.5V
- Output voltage range: 1.2V to 4.5V
- Stable with 1-µF ceramic input and output capacitors
- No noise bypass capacitor required
- Remote output capacitor placement
- Thermal-overload and short-circuit protection
- Operating junction temperature: –40°C to 125°C
- Low output voltage noise: < 6.5µV_{RMS}
- PSRR: 82dB at 1kHz
- Output voltage tolerance: ±2%
- Very low I_Q (enabled): 12µA
- Low dropout: 120mV (typical)
- Create a custom design using the LP5907 with the WEBENCH® Power Designer

2 Applications

- Smartphones
- Tablets
- Communications equipment
- Digital still cameras
- Factory automation

3 Description

The LP5907 is a low-noise LDO that can supply up to 250mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

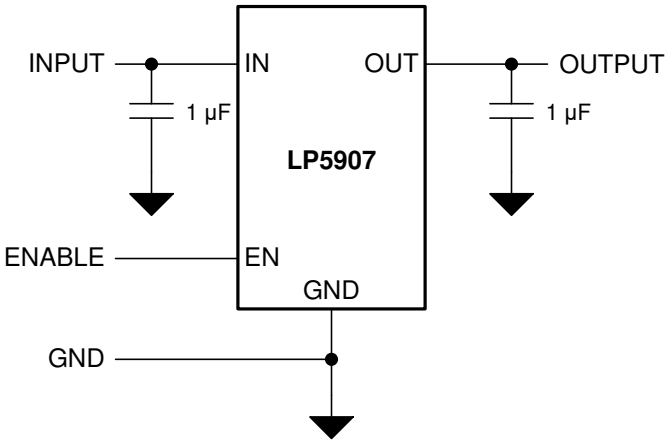
The device is designed to work with a 1µF input and a 1µF output ceramic capacitor (no separate noise bypass capacitor is required).

This device is available with fixed output voltages from 1.2V to 4.5V in 25mV steps. Contact Texas Instruments Sales for specific voltage option needs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LP5907	YKE, YKG, YKM, YCR (DSBGA, 4)	0.685mm × 0.685mm
	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DQN (X2SON, 4)	1mm × 1mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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Table of Contents

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4 Pin Configuration and Functions

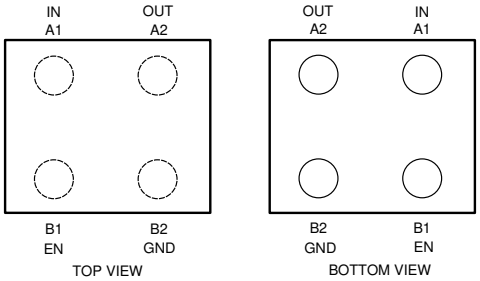

Figure 4-1. YKE, YKG, YKM, and YCR Packages, 4-Pin DSBGA

Table 4-1. Pin Functions: DSBGA

PIN		TYPE	DESCRIPTION
DSBGA	NAME		
A1	IN	I	Input voltage supply. Connect a 1µF capacitor at this input.
A2	OUT	O	Regulated output voltage. Connect a minimum 1µF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
B1	EN	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal 230Ω pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. This pin has an internal 1MΩ pulldown resistor to hold the regulator off by default.
B2	GND	—	Common ground

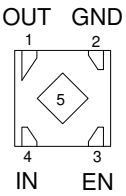

Figure 4-2. DQN Package, 4-Pin X2SON (Bottom View)

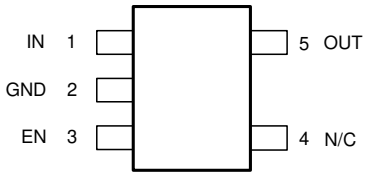

Figure 4-3. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-2. Pin Functions: X2SON, SOT-23

PIN			TYPE	DESCRIPTION
NAME	X2SON	SOT-23		
EN	3	3	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal 230Ω pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. This pin has an internal 1MΩ pulldown resistor to hold the regulator off by default.
GND	2	2	—	Common ground.
IN	4	1	I	Input voltage supply. Connect a 1µF capacitor at this input.
N/C	—	4	—	No internal electrical connection.
OUT	1	5	O	Regulated output voltage. Connect a minimum 1µF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in shutdown mode (V_{EN} low).
Thermal Pad	5	—	—	Thermal pad for the X2SON package, connect to GND or leave floating. Do not connect to any potential other than GND.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	See(2)	V
V_{EN}	Enable input voltage	–0.3	6	V
	Continuous power dissipation(4)	Internally limited		W
T_{JMAX}	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Abs Max V_{OUT} is the lessor of V_{IN} + 0.3V, or 6V.
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	2.2	5.5	V
V_{EN}	Enable input voltage	0	5.5	V
I_{OUT}	Output current	0	250	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature(3)	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) In applications where high power dissipation and poor package thermal resistance is present, the maximum ambient temperature can need to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the device or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$. See the *Application and Implementation* section.

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5.4 Thermal Information

THERMAL METRIC[1]		LP5907						UNIT
		DBV (SOT-23)	DQN (X2SON)	YCR (DSBGA)	YKE (DSBGA)	YKG (DSBGA)	YKM (DSBGA)	
		5 PINS	4 PINS	4 PINS	4 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.4	216.1	189.4	206.1	191.6	194.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.1	161.7	2.4	1.5	2.4	3.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	162.1	56.6	37.0	58.9	62.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	5.1	1.1	15.0	1.1	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.3	161.7	56.5	36.8	58.9	62.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)[1] [2] [3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	T_A = 25°C		2.2		5.5	V
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1V) to 5.5V, I_{OUT} = 1mA to 250mA		–2		2	%V_{OUT}
		V_{IN} = ($V_{OUT(NOM)}$ + 1V) to 5.5V, I_{OUT} = 1mA to 250mA (V_{OUT} < 1.8V, SOT-23, X2SON packages)		–3		3	
	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1V) to 5.5V, I_{OUT} = 1mA			0.02		%/V
	Load regulation	I_{OUT} = 1mA to 250mA			0.001		%/mA
I_{LOAD}	Load current	See[4]		0		250	mA
	Maximum output current			250			mA
I_Q	Quiescent current[5]	V_{EN} = 1.2V, I_{OUT} = 0mA			12	25	µA
		V_{EN} = 1.2V, I_{OUT} = 250mA			250	425	
		V_{EN} = 0.3V (disabled)			0.2	1	
I_G	Ground current[6]	V_{EN} = 1.2V, I_{OUT} = 0mA			14		µA
V_{DO}	Dropout voltage[7]	I_{OUT} = 100mA			50		mV
		I_{OUT} = 250mA (DSBGA package)			120	200	
		I_{OUT} = 250mA (SOT-23, X2SON packages)				250	
I_{SC}	Short-circuit current limit	T_A = 25°C[8]		250	500		mA
PSRR	Power-supply rejection ratio[9]	f = 100Hz, I_{OUT} = 20mA			90		dB
		f = 1kHz, I_{OUT} = 20mA			82		
		f = 10kHz, I_{OUT} = 20mA			65		
		f = 100kHz, I_{OUT} = 20mA			60		
e_N	Output noise voltage[9]	BW = 10Hz to 100kHz	I_{OUT} = 1mA		10		μV_{RMS}
			I_{OUT} = 250mA		6.5		
R_{AD}	Output automatic discharge pulldown resistance	V_{EN} < V_{IL} (output disabled)			230		Ω
T_{SD}	Thermal shutdown	T_J rising			160		°C
	Thermal hysteresis	T_J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V_{IL}	Low input threshold	V_{IN} = 2.2V to 5.5V, V_{EN} falling until the output is disabled				0.4	V

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5.5 Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High input threshold	V_{IN} = 2.2V to 5.5V V_{EN} rising until the output is enabled	1.2			V
I_{EN}	Input current at EN pin(10)	V_{EN} = 5.5V and V_{IN} = 5.5V		5.5		µA
		V_{EN} = 0V and V_{IN} = 5.5V		0.001		
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line transient(9)	V_{IN} = ($V_{OUT(NOM)}$ + 1V) to ($V_{OUT(NOM)}$) + 1.6V) in 30µs	–1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6V) to ($V_{OUT(NOM)}$) + 1.6V) in 30µs			1	
	Load transient(9)	I_{OUT} = 1mA to 250mA in 10µs	–40			
		I_{OUT} = 250mA to 1mA in 10µs			40	
	Overshoot on start-up(9)	Stated as a percentage of $V_{OUT(NOM)}$			5%	
	Overshoot on start-up with EN(9)	Stated as a percentage of $V_{OUT(NOM)}$, V_{IN} = V_{OUT} + 1V to 5.5V, 0.7µF < C_{OUT} < 10µF, 0mA < I_{OUT} < 250mA, EN rising until the output is enabled			1%	
t_{ON}	Turn-on time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$, T_A = 25°C		80	150	µs

(1) All voltages are with respect to the device GND terminal, unless otherwise stated.
(2) Minimum and maximum limits are specified through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature can possibly have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the device or package in the application $R_{\theta JA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{\theta JA}$ × P_{D-MAX}). See the *Application and Implementation* section.
(4) The device maintains a stable, regulated output voltage without a load current.
(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below the nominal value.
(8) Short-circuit current (I_{SC}) for the LP5907 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100mV below the nominal voltage.
(9) This specification is verified by design.
(10) There is a 1MΩ resistor between EN and ground on the device.

5.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX	UNIT
C_{IN}	Input capacitance(2)	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance(2)		0.7	1	10	µF
ESR	Output/Input capacitance(2)		5		500	mΩ

(1) The minimum capacitance must be greater than 0.5µF over the full range of operating conditions. The capacitor tolerance must be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application must be considered during device selection to make sure this minimum capacitance specification is met. X7R capacitors are recommended, however capacitor types X5R, Y5V, and Z5U can be used with consideration of the application and conditions.
(2) This specification is verified by design.

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5.7 Typical Characteristics

V_{IN} = 3.7V, V_{OUT} = 2.8V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)

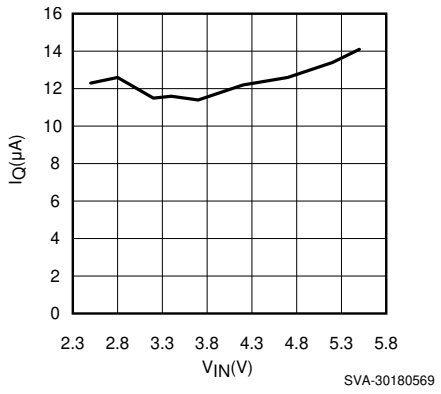


Figure 5-1. Quiescent Current vs Input Voltage

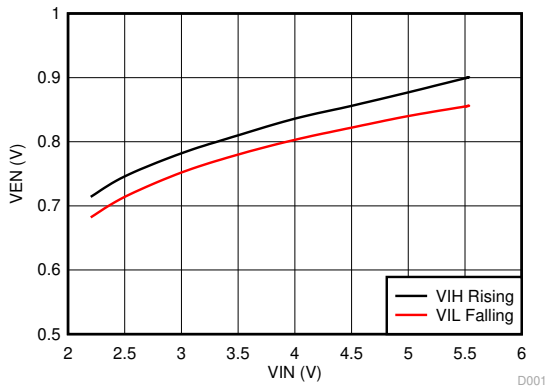
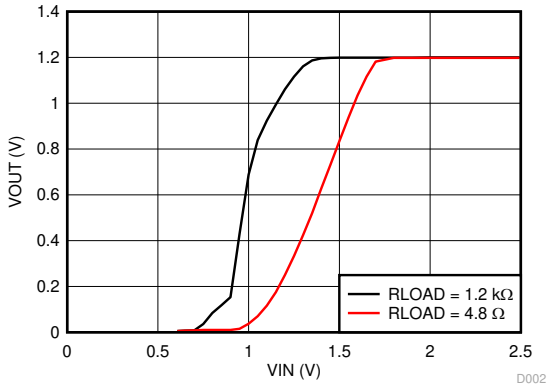
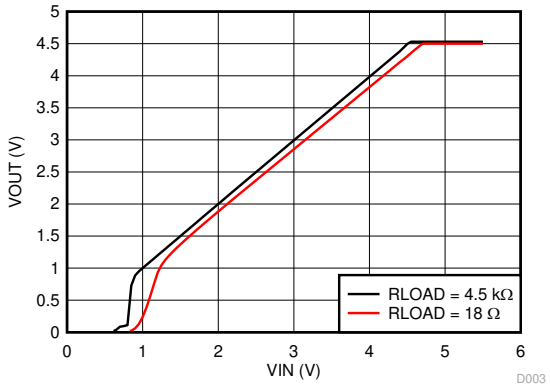


Figure 5-2. V_{EN} Thresholds vs V_{IN}



V_{OUT} = 1.2V, V_{EN} = V_{IN}

Figure 5-3. V_{OUT} vs V_{IN}



V_{OUT} = 4.5V, V_{EN} = V_{IN}

Figure 5-4. V_{OUT} vs V_{IN}

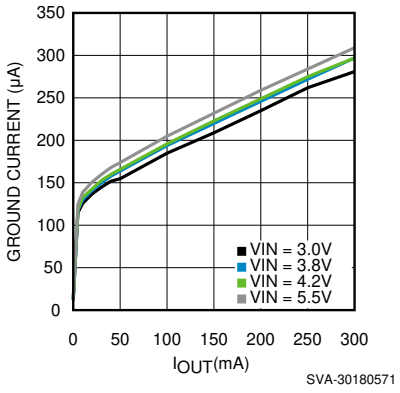


Figure 5-5. Ground Current vs Output Current

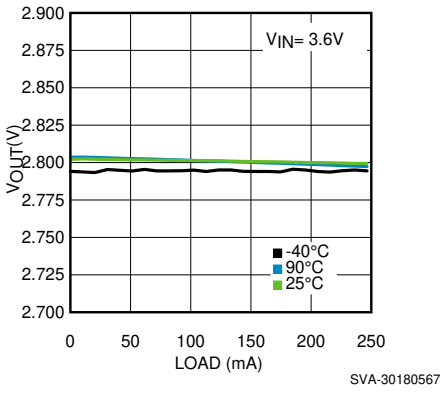


Figure 5-6. Load Regulation

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5.7 Typical Characteristics (continued)

V_{IN} = 3.7V, V_{OUT} = 2.8V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)

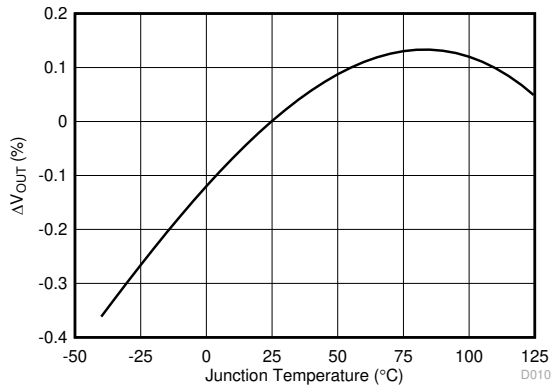


Figure 5-7. ΔV_{OUT} vs Temperature

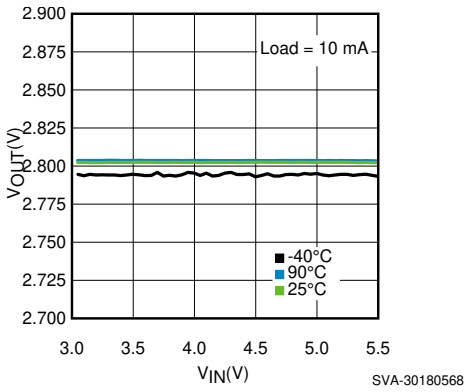


Figure 5-8. Line Regulation

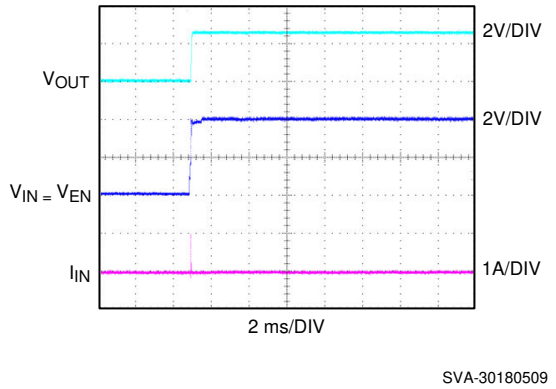
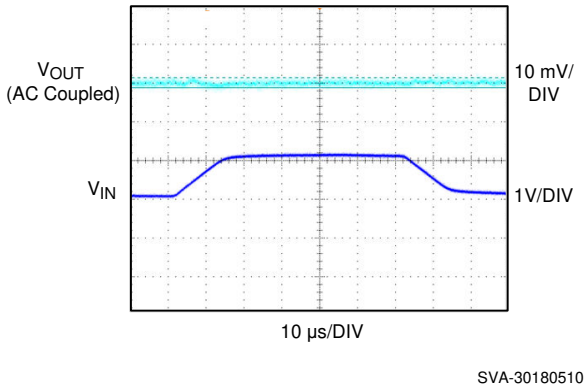
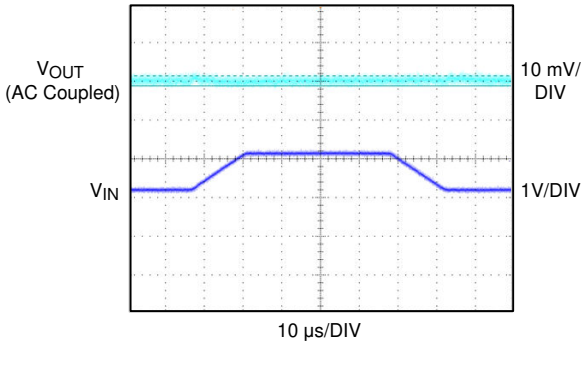


Figure 5-9. Inrush Current



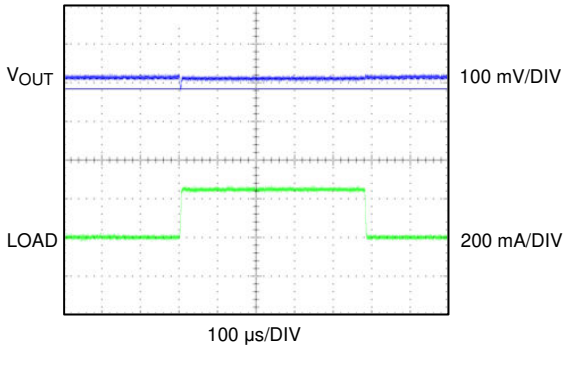
V_{IN} = 3.2V ↔ 4.2V, load = 1mA

Figure 5-10. Line Transient



V_{IN} = 3.2V ↔ 4.2V, load = 250mA

Figure 5-11. Line Transient



Load = 0mA ↔ 250mA, –40°C

Figure 5-12. Load Transient

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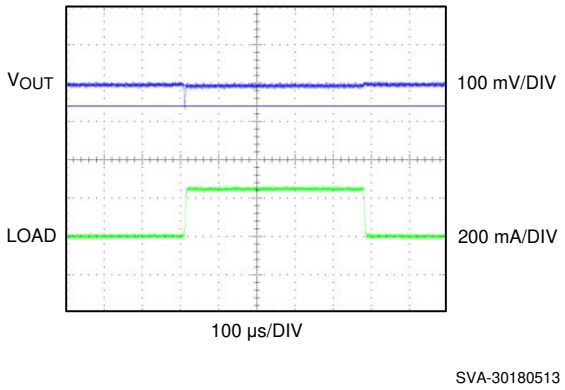
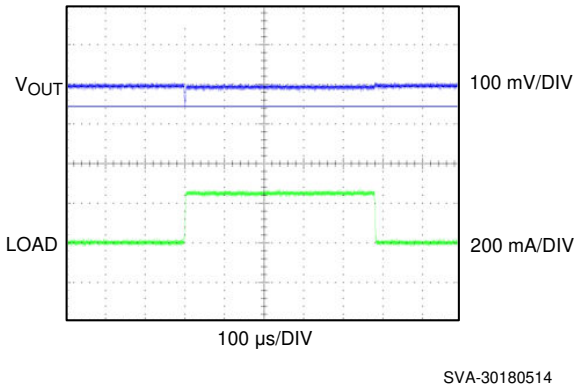
5.7 Typical Characteristics (continued)

V_{IN} = 3.7V, V_{OUT} = 2.8V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)



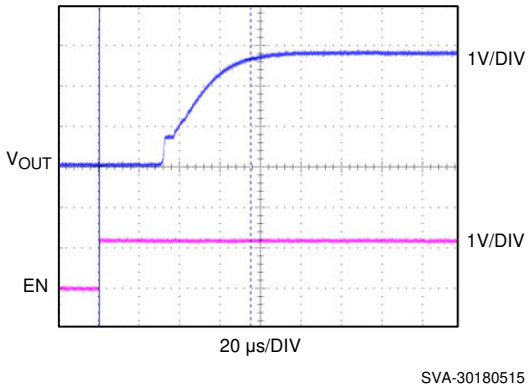
Load = 0mA ↔ 250mA, 90°C

Figure 5-13. Load Transient



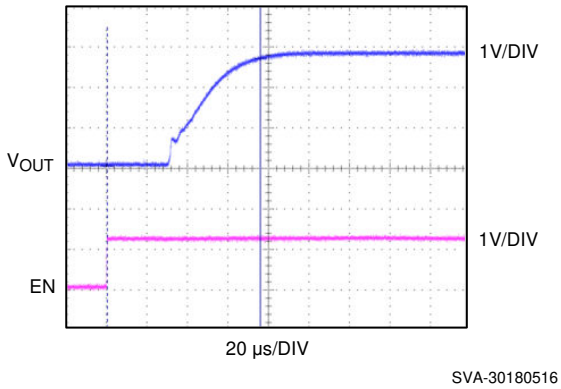
Load = 0mA ↔ 250mA, 25°C

Figure 5-14. Load Transient



Load = 0mA

Figure 5-15. Start-Up



Load = 250mA

Figure 5-16. Start-Up

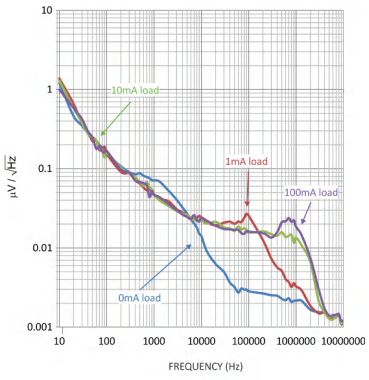


Figure 5-17. Noise Density Test

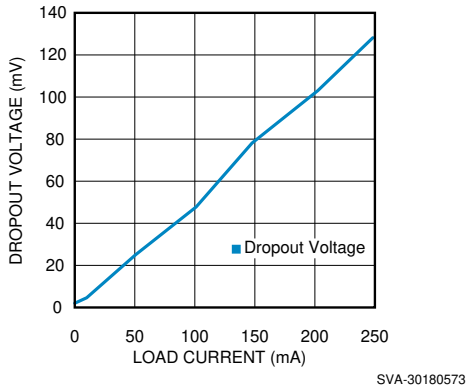


Figure 5-18. Dropout Voltage vs Load Current

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5.7 Typical Characteristics (continued)

V_{IN} = 3.7V, V_{OUT} = 2.8V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 1µF, and T_A = 25°C (unless otherwise noted)

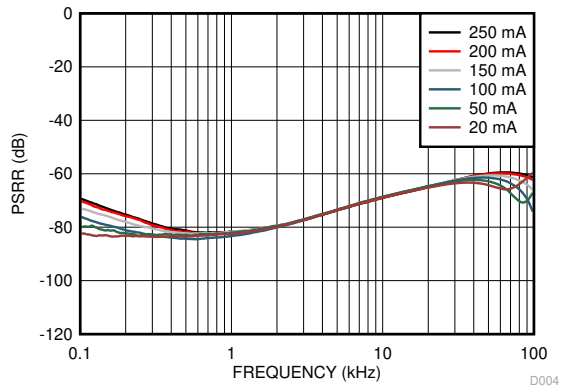

Figure 5-19. PSRR Loads Averaged 100Hz to 100kHz

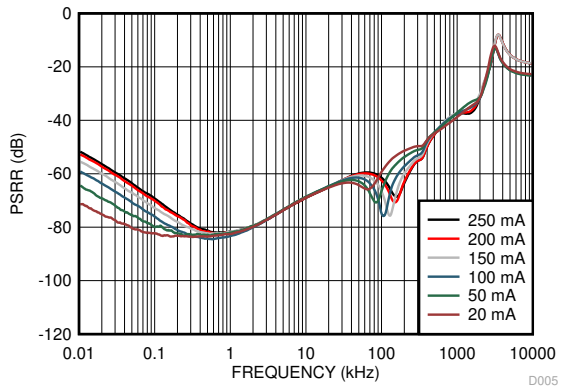

Figure 5-20. PSRR Loads Averaged 10Hz to 10MHz

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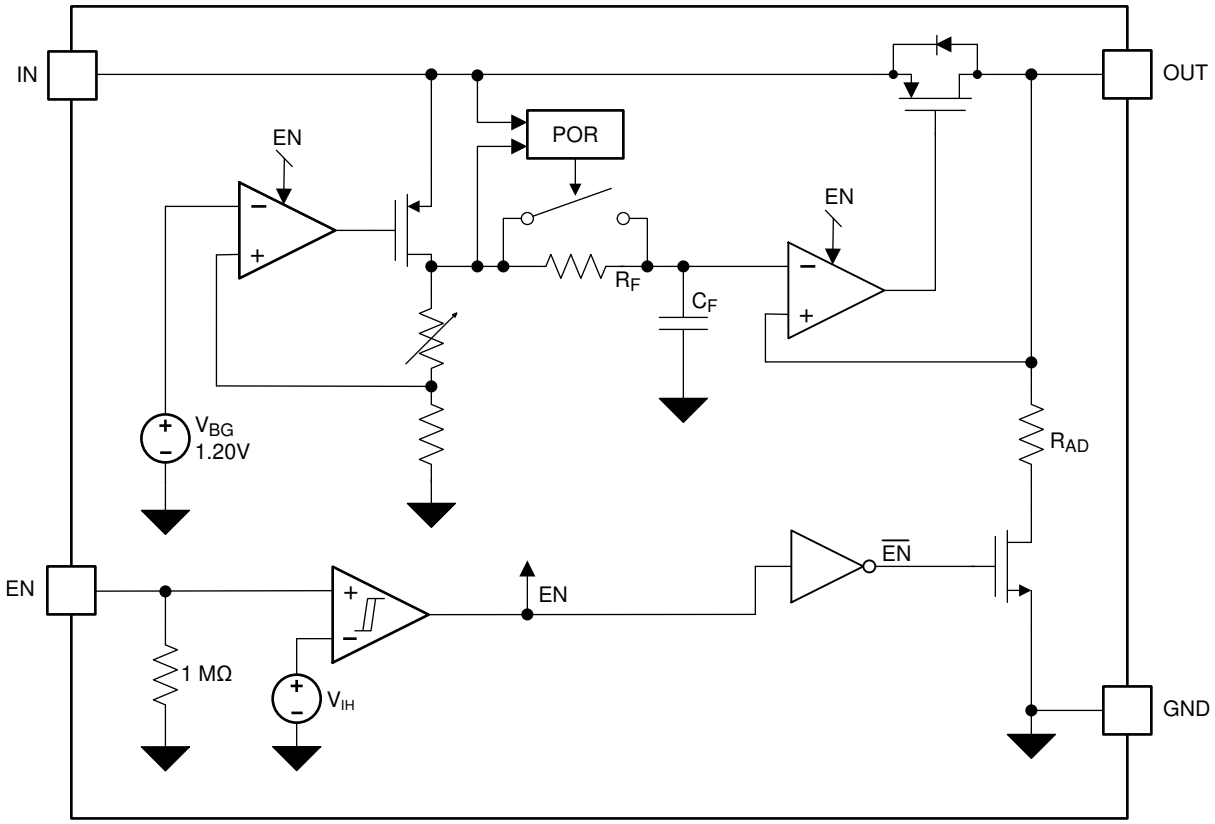
6 Detailed Description

6.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907 provides low noise, high PSRR, low quiescent current, and low line and load transient response figures. Using innovative design techniques, the LP5907 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907 is designed to perform with a single 1µF input capacitor and a single 1µF ceramic output capacitor. With a reasonable PCB layout, the single 1µF ceramic output capacitor can be placed up to 10cm away from the LP5907 device.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Enable (EN)

The LP5907 EN pin is internally held low by a 1MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to make sure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to make sure that the device is fully disabled and the automatic output discharge is activated.

6.3.2 Low Output Noise

Any internal noise at the LP5907 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cut-off frequency of approximately 0.1Hz.

6.3.3 Output Automatic Discharge

The LP5907 output employs an internal 230Ω (typical) pulldown resistance to discharge the output when the EN pin is low and the device is disabled.

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6.3.4 Remote Output Capacitor Placement

The LP5907 requires at least a 1µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor can be located up to 10cm away from the LDO.

6.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This thermal cycling limits the dissipation of the regulator, and protects the regulator from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907 is designed to protect against temporary thermal overload conditions. The T_{SD} circuitry is not intended to replace proper heat-sinking. Continuously running the LP5907 into thermal shutdown can degrade device reliability.

6.4 Device Functional Modes

6.4.1 Enable (EN)

The LP5907 enable (EN) pin is internally held low by a 1MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to make sure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230Ω (typical) pulldown resistance.

6.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907 does not include any dedicated UVLO circuitry. The LP5907 internal circuitry is not fully functional until V_{IN} is at least 2.2V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2V or (V_{OUT} + V_{DO}).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LP5907 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1µF. The LP5907 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of –40°C to 125°C.

7.2 Typical Application

Figure 7-1 shows the typical application circuit for the LP5907. Input and output capacitances can be increased, if needed, above the 1µF minimum for some applications.

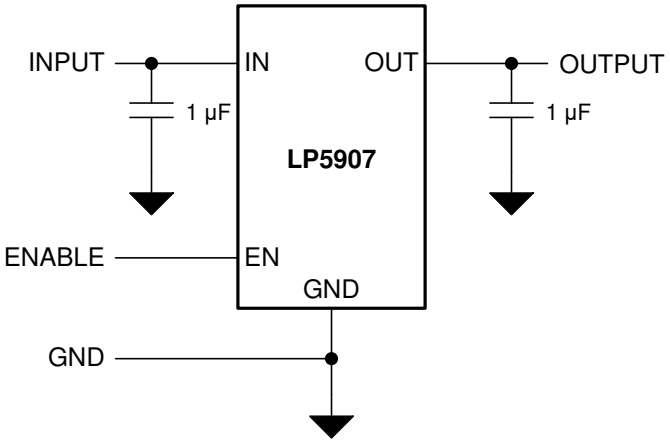

Figure 7-1. LP5907 Typical Application

7.2.1 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-1.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2V to 5.5V
Output voltage	1.8V
Output current	200mA
Output capacitor range	0.7µF to 10µF
Input/output capacitor ESR range	5mΩ to 500mΩ

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7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP5907 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed in regards to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Use these two equations to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the device or package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ cannot be derated, the P_D value must be reduced. This reduction can be accomplished by reducing V_{IN} in the V_{IN}–V_{OUT} term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

7.2.2.3 External Capacitors

Like most low-dropout regulators, the LP5907 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

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7.2.2.4 Input Capacitor

An input capacitor is required for stability. The input capacitor must be at least equal to, or greater than, the output capacitor for good load transient performance. Connect at least a 1µF capacitor between the LP5907 input pin and ground for stable operation over the full load current range. Basically, having more output capacitance than input is acceptable, as long as the input is at least 1µF.

The input capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor can be used at the input.

Note

To provide stable operation, good PCB practices must be used to minimize ground impedance and to keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power source to the LP5907, increase the input capacitor to at least 10µF. Also, tantalum capacitors can suffer catastrophic failures resulting from surge current when connected to a low-impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, verify by the manufacturer that the capacitor has a surge current rating sufficient for the application. The initial tolerance, applied voltage derating, and temperature coefficient must all be considered when selecting the input capacitor to make sure that the actual capacitance is never less than 0.7µF over the entire operating range.

7.2.2.5 Output Capacitor

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1µF to 10µF range, and with ESR between 5mΩ to 500mΩ, is suitable in the LP5907 application circuit. For this device, connect the output capacitor between the OUT pin with a good connection back to the GND pin.

Tantalum or film capacitors can also be used at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the *Capacitor Characteristics* section).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range of 5mΩ to 500mΩ for stability. Like the input capacitor, the initial tolerance, applied voltage derating, and temperature coefficient must all be considered when selecting the input capacitor to make sure that the actual capacitance is never less than 0.7µF over the entire operating range.

7.2.2.6 Capacitor Characteristics

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits these components offer. For capacitance values in the range of 1µF to 10µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high-frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP5907.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 10µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. Which means that although a tantalum capacitor can possibly be found with an ESR value within the stable range, the capacitor must be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases by approximately 2:1 when the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

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7.2.2.7 Remote Capacitor Operation

The LP5907 requires at least a 1µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor can be located up to 10cm away from the LDO. Which means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (such as a capacitor at the input of supplied device). The remote capacitor feature helps minimize the number of capacitors in the system.

In general, keep the wiring parasitic inductance at a minimum, which means use traces as wide as possible from the LDO output to the capacitors, thus keeping the LDO output trace layer as close to ground layer as possible and avoiding vias on the path. If vias must be used, use as many vias as possible between the connection layers. Keep parasitic wiring inductance less than 35nH. For applications with fast load transients, use an input capacitor equal to or larger to the sum of the capacitance at the output node for best load transient performance.

7.2.2.8 No-Load Stability

The LP5907 remains stable, and in regulation, with no external load.

7.2.2.9 Enable Control

The LP5907 can be switched on or off by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, and a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1µA. Additionally, an output pulldown circuit is activated that makes sure any charge stored on C_{OUT} is discharged to ground.

If the application does not require the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1MΩ pulldown resistor ties the EN input to ground, making sure the device remains off if the EN pin is left open circuit. To provide proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on or turn-off voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

7.2.3 Application Curves

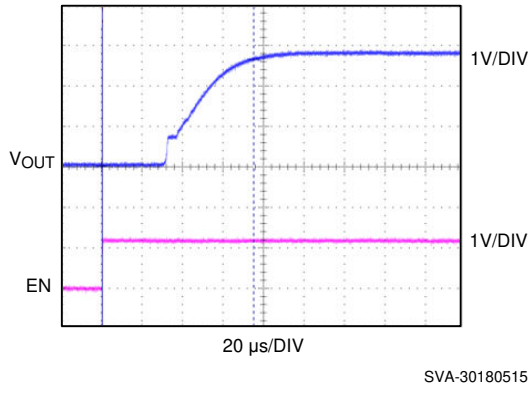

Figure 7-2. Start-Up

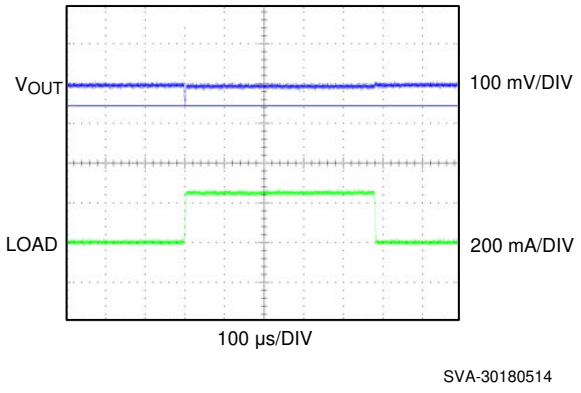

Figure 7-3. Load Transient Response

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2V to 5.5V. The input supply must be well regulated and free of spurious noise. To make sure that the LP5907 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 1V. A minimum capacitor value of 1µF is required to be within 1cm of the IN pin.

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7.4 Layout

7.4.1 Layout Guidelines

The dynamic performance of the LP5907 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs can degrade the PSRR, noise, or transient performance of the LP5907.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close to the package as practical. The ground connections for C_{IN} and C_{OUT} must route back to the LP5907 ground pin using as wide and short of a copper trace as practical.

Connections using long trace lengths, narrow trace widths, and connections through vias must be avoided. These connections add parasitic inductances and resistance that results in inferior performance, especially during transient conditions.

7.4.1.1 X2SON Mounting

The X2SON package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance. For more information, see the *QFN/SON PCB Attachment* application note.

7.4.1.2 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* application note. For best results during assembly, alignment ordinals on the PC board can be used to facilitate placement of the DSBGA device.

7.4.1.3 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light can cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if these sources are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

7.4.2 Layout Examples

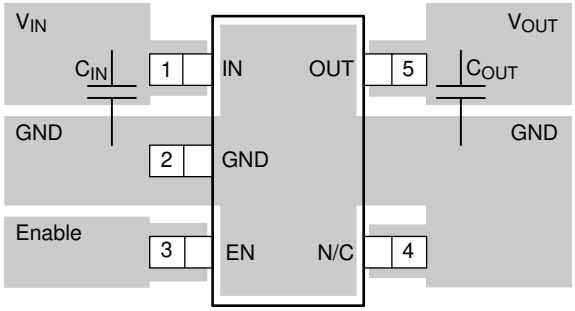

Figure 7-4. SOT-23 Typical Layout

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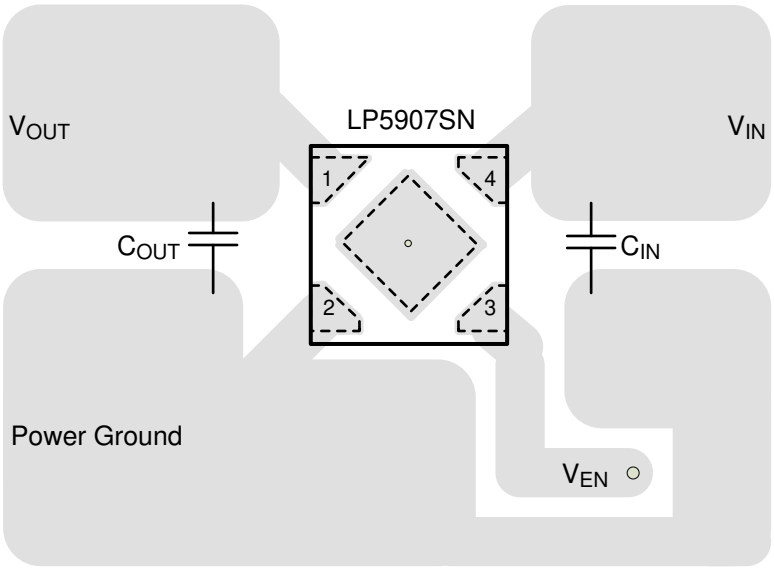

Figure 7-5. X2SON Typical Layout

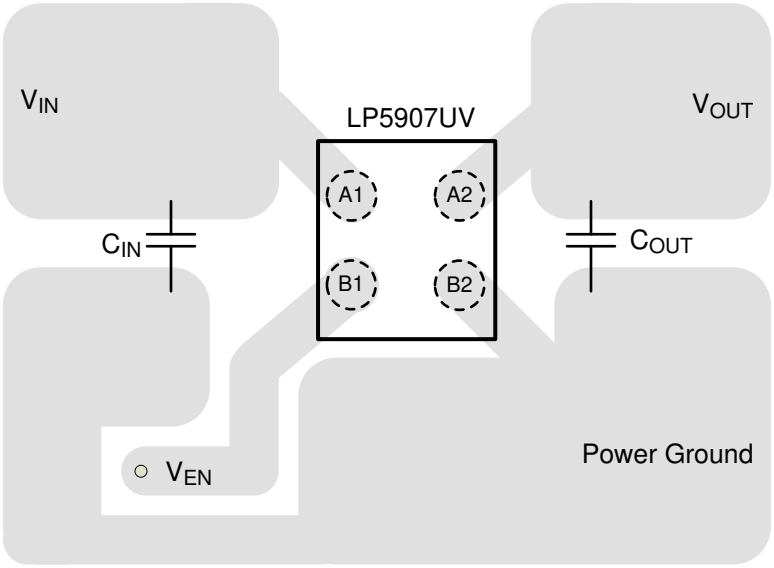

Figure 7-6. DSBGA Typical Layout

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Custom Design With WEBENCH® Tools

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1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.1.2 Related Documentation

For related documentation, see the following:

- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (June 2020) to Revision P (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added YCR to pinout caption of *Pin Configuration and Functions* section	3
• Added YCR column to *Thermal Information* table	5

Changes from Revision N (April 2018) to Revision O (June 2020)	Page
• Changed *Applications* section	1
• Changed DSBGA body size in *Device Information* table	1
• Added YKG to pinout caption of *Pin Configuration and Functions* section	3
• Added YKG column to *Thermal Information* table	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907A28YKMR	ACTIVE	DSBGA	YKM	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	Q	Samples
LP5907A33YKMR	ACTIVE	DSBGA	YKM	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	N	Samples
LP5907MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LLTB	Samples
LP5907MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LN8B	Samples
LP5907MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LLUB	Samples
LP5907MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LN7B	Samples
LP5907MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LLYB	Samples
LP5907MFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LN4B	Samples
LP5907MFX-2.9/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1E5X	Samples
LP5907MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LLZB	Samples
LP5907MFX-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LN5B	Samples
LP5907MFX-3.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LN6B	Samples
LP5907MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LLVB	Samples
LP5907MFX-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LLXB	Samples
LP5907SNX-1.2/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF	Samples
LP5907SNX-1.8/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CG	Samples
LP5907SNX-1.9	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3Z	Samples
LP5907SNX-2.2/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EP	Samples
LP5907SNX-2.5/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F9	Samples
LP5907SNX-2.7/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907SNX-2.75	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HI	Samples
LP5907SNX-2.8/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
LP5907SNX-2.85/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
LP5907SNX-2.9/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GV	Samples
LP5907SNX-3.0/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
LP5907SNX-3.1/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
LP5907SNX-3.2/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM	Samples
LP5907SNX-3.3/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CN	Samples
LP5907SNX-4.0/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GU	Samples
LP5907SNX-4.5/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CO	Samples
LP5907UVE-1.2/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVE-1.8/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVE-2.8/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVE-2.85/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVE-3.0/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVE-3.1/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVE-3.2/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVE-3.3/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVE-4.5/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX-1.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVX-1.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907UVX-2.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
LP5907UVX-2.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVX-2.85/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVX-3.0/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVX-3.1/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVX-3.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVX-3.3/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVX-4.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX19/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5907UVX37/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples
LP5907YKGR-2.8	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	3	Samples
LP5907YKGR-2.825	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP5907YKGR-2.85	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LP5907 :

- Automotive : LP5907-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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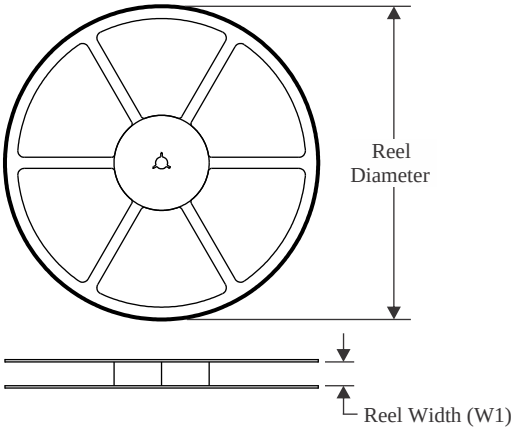
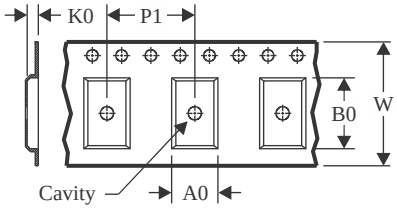
TAPE AND REEL INFORMATION

REEL DIMENSIONS

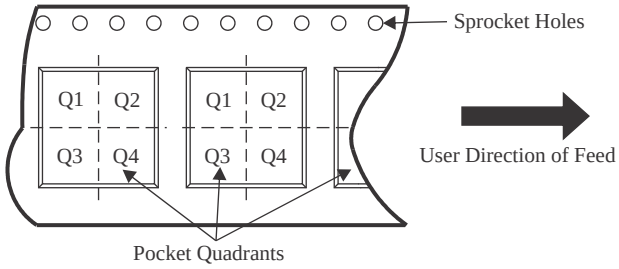


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907A28YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907A33YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.9	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-1.9	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1

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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907YKGR-2.8	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.825	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.85	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1

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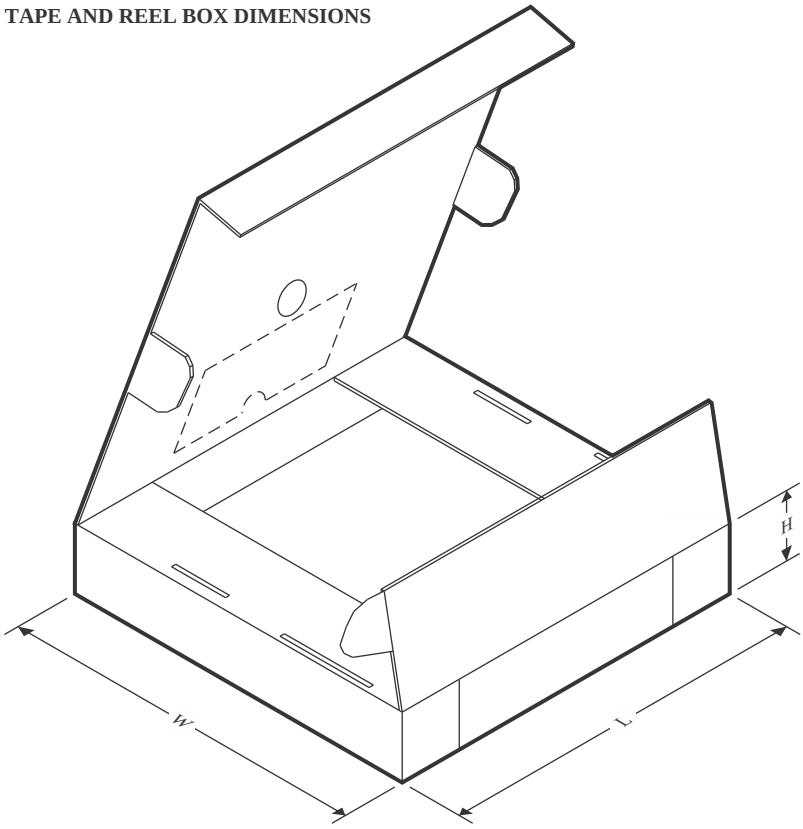
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907A28YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907A33YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.9	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-1.9	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.75	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.75	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907YKGR-2.8	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.825	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.85	DSBGA	YKG	4	3000	220.0	220.0	35.0

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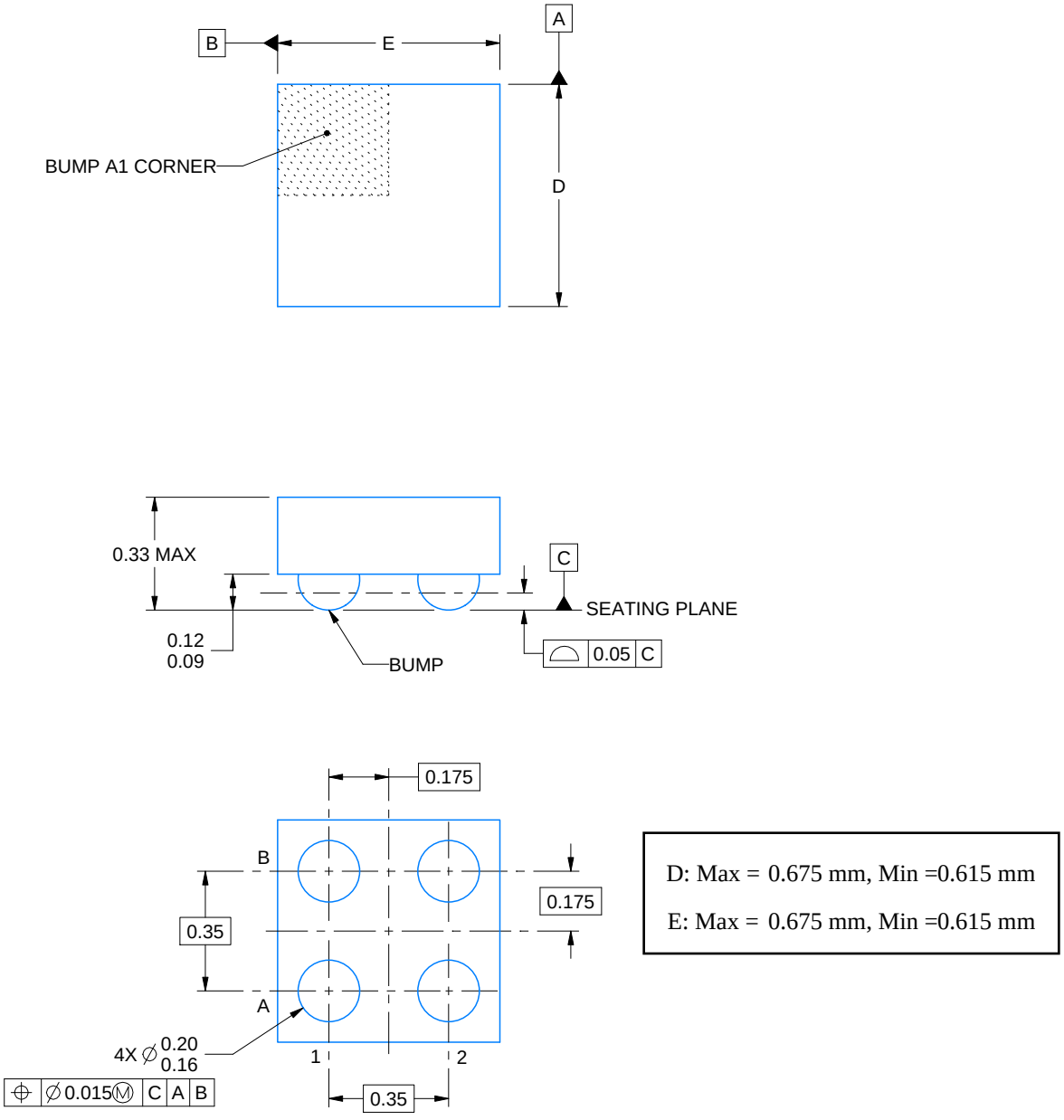
PACKAGE OUTLINE

YKG0004

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

4218366/E 05/2020

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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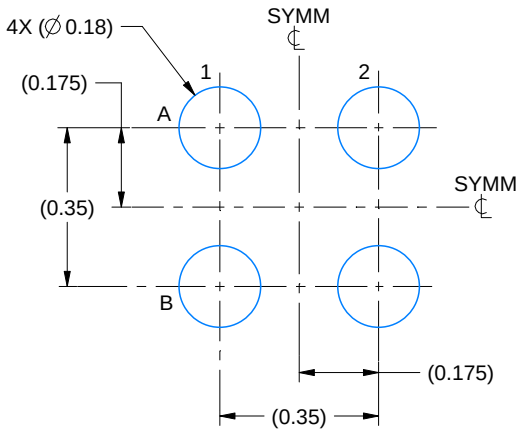
EXAMPLE BOARD LAYOUT

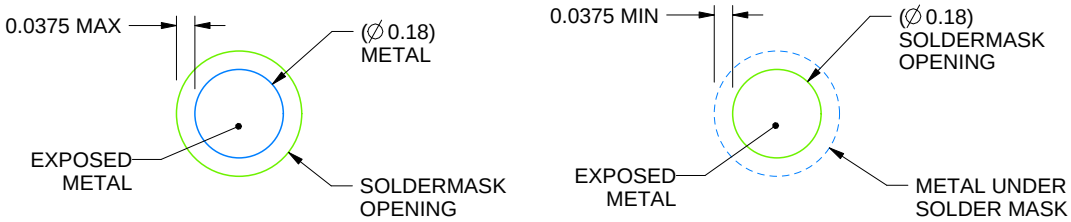
YKG0004

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDERMASK DETAILS
NOT TO SCALE

4218366/E 05/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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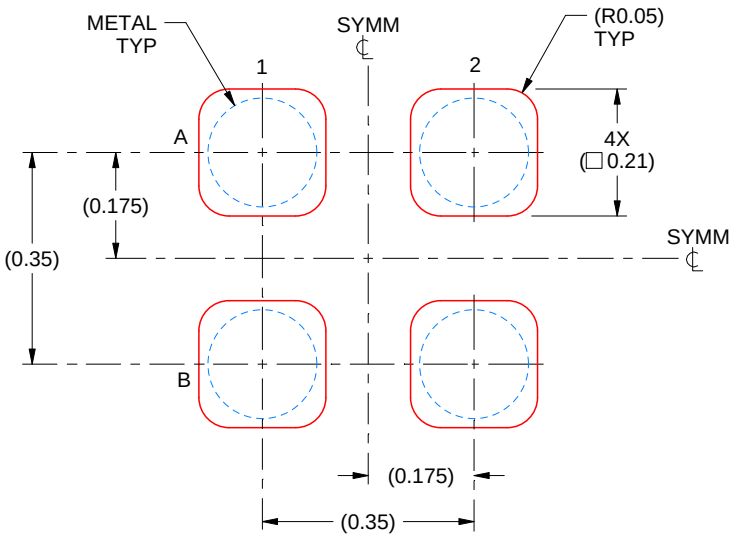
EXAMPLE STENCIL DESIGN

YKG0004

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



SOLDERPASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE:80X

4218366/E 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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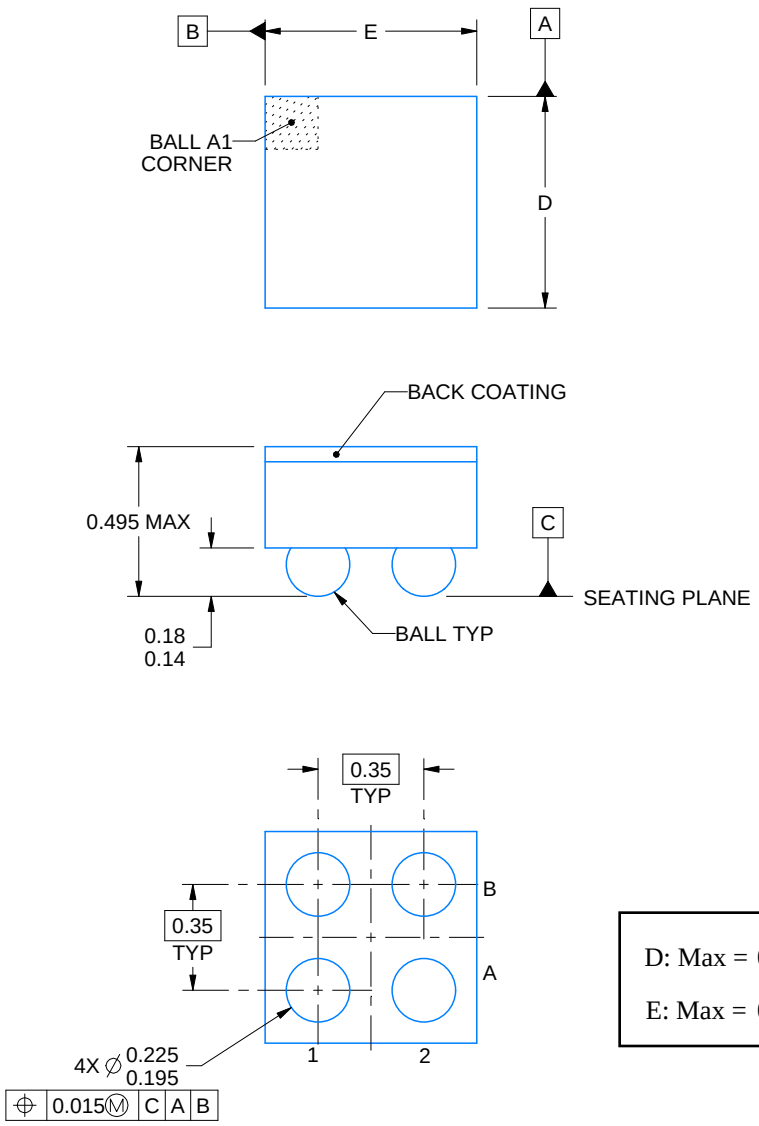
PACKAGE OUTLINE

YKM0004

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

4223494/A 11/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Texas Instruments

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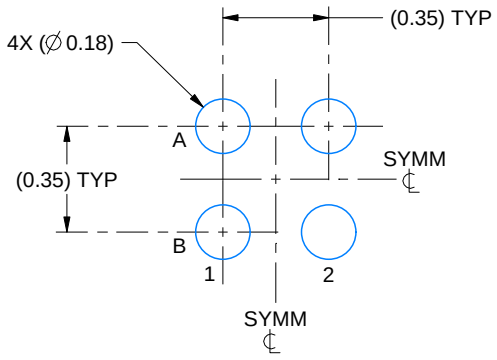
EXAMPLE BOARD LAYOUT

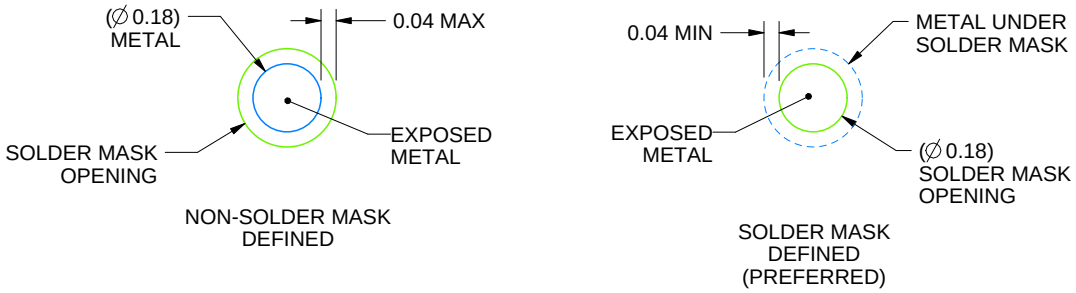
YKM0004

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223494/A 11/2014

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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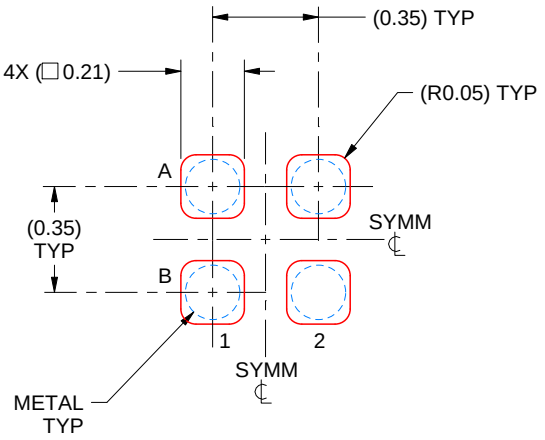
EXAMPLE STENCIL DESIGN

YKM0004

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4223494/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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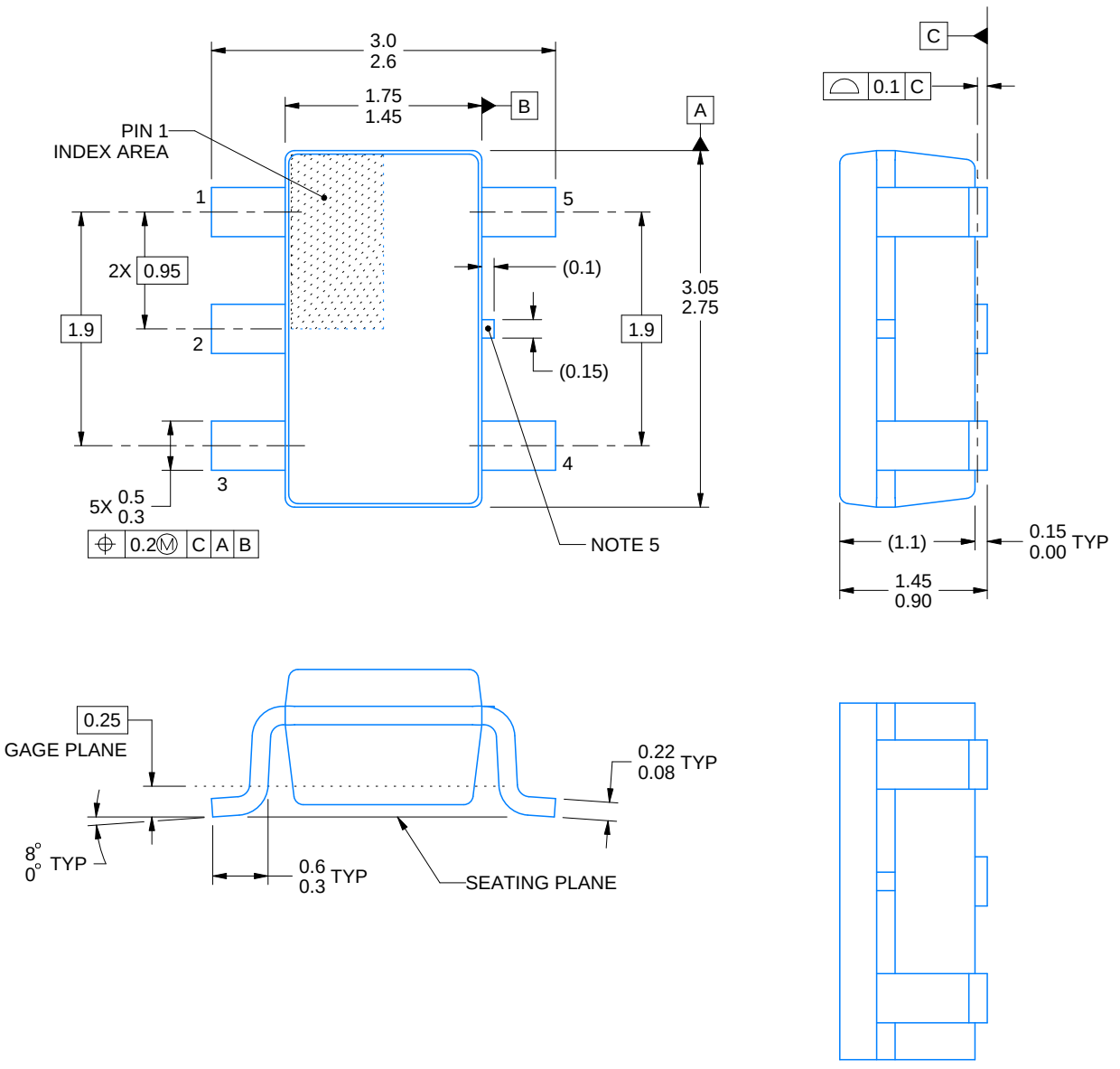
PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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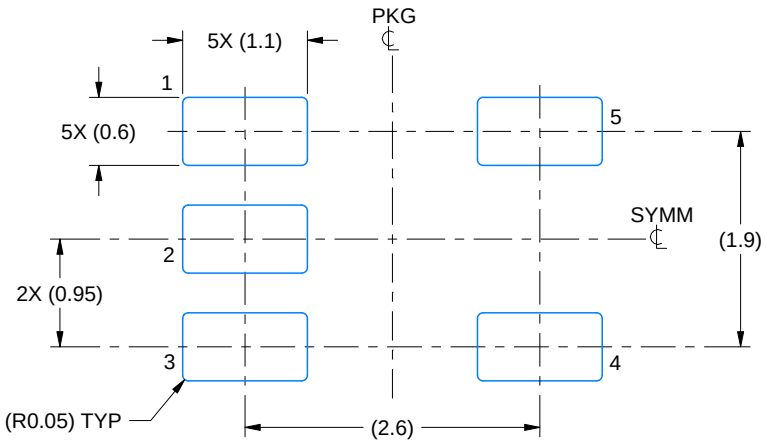
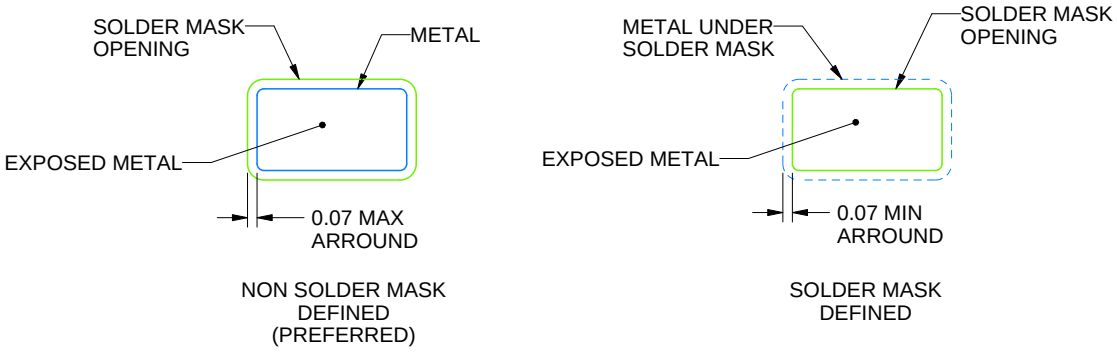


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Texas Instruments

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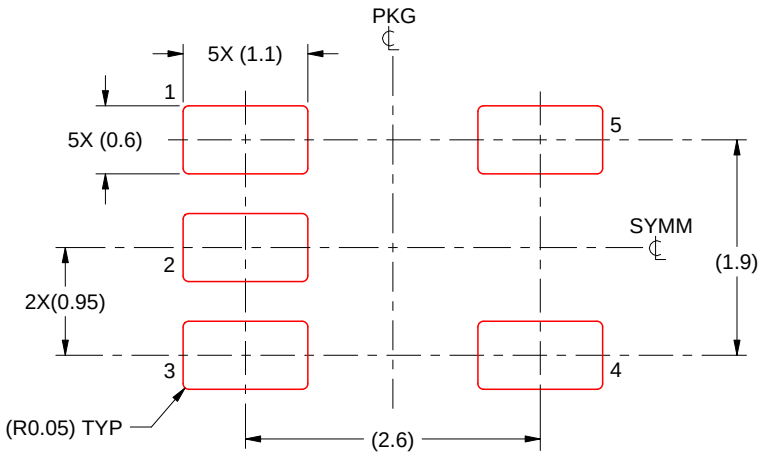

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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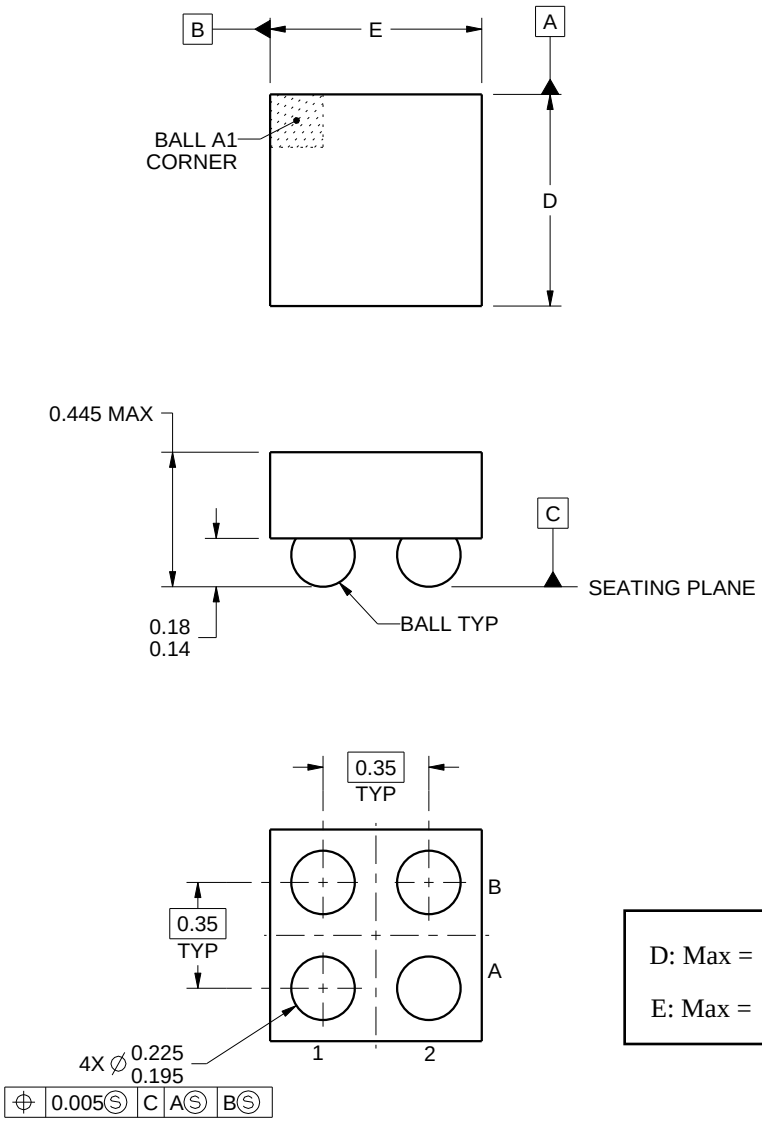
PACKAGE OUTLINE

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

4220102/A 11/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Texas Instruments

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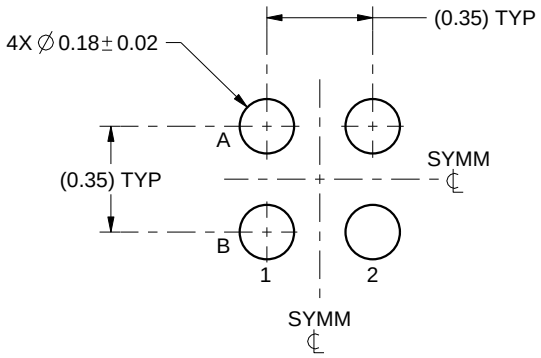
EXAMPLE BOARD LAYOUT

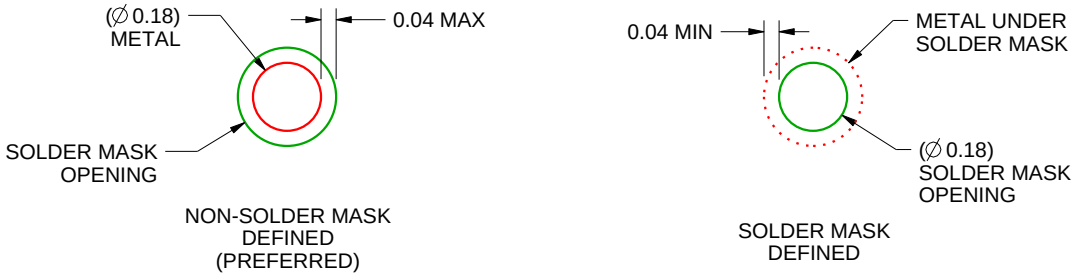
YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4220102/A 11/2014

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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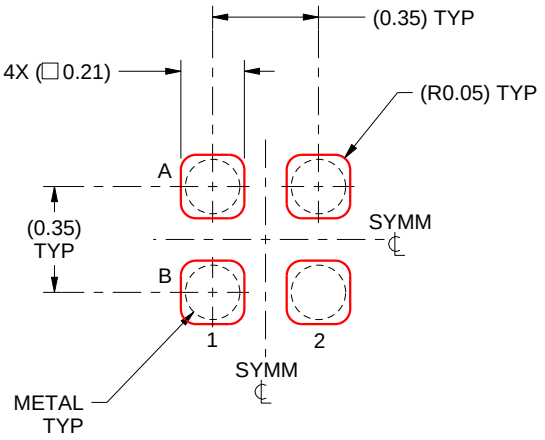
EXAMPLE STENCIL DESIGN

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4220102/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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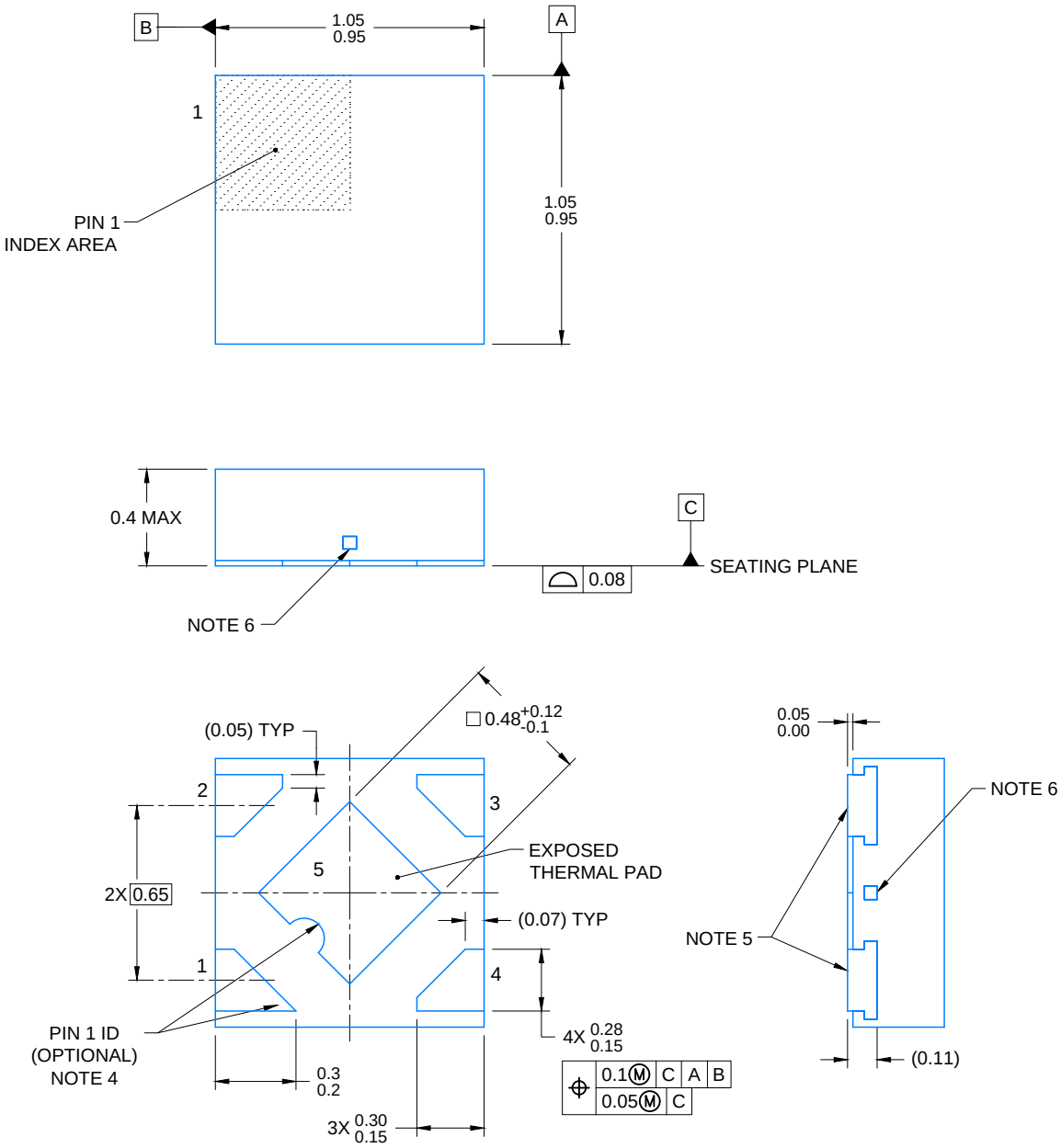
PACKAGE OUTLINE

DQN0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.

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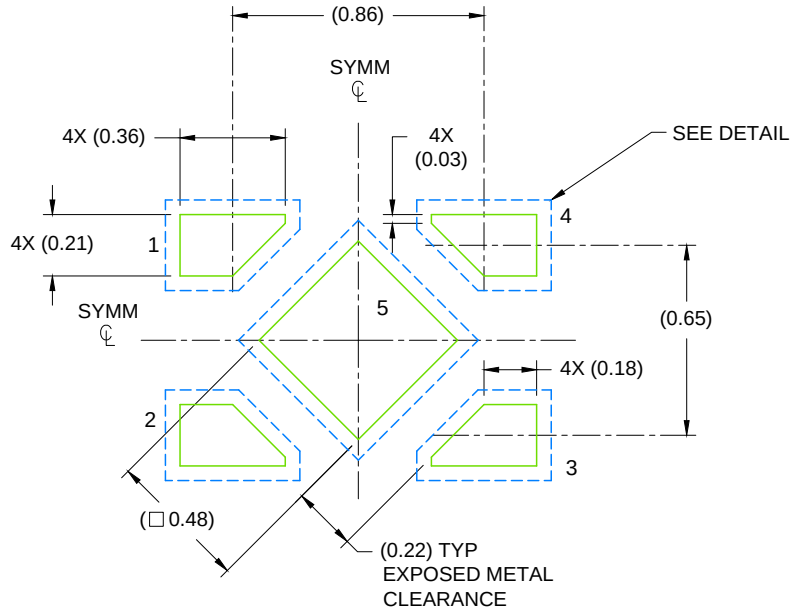
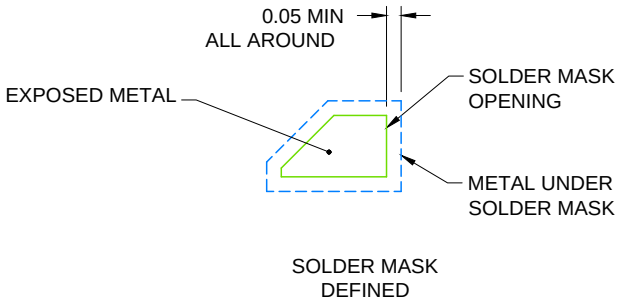


LAND PATTERN EXAMPLE
SCALE: 40X



SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.

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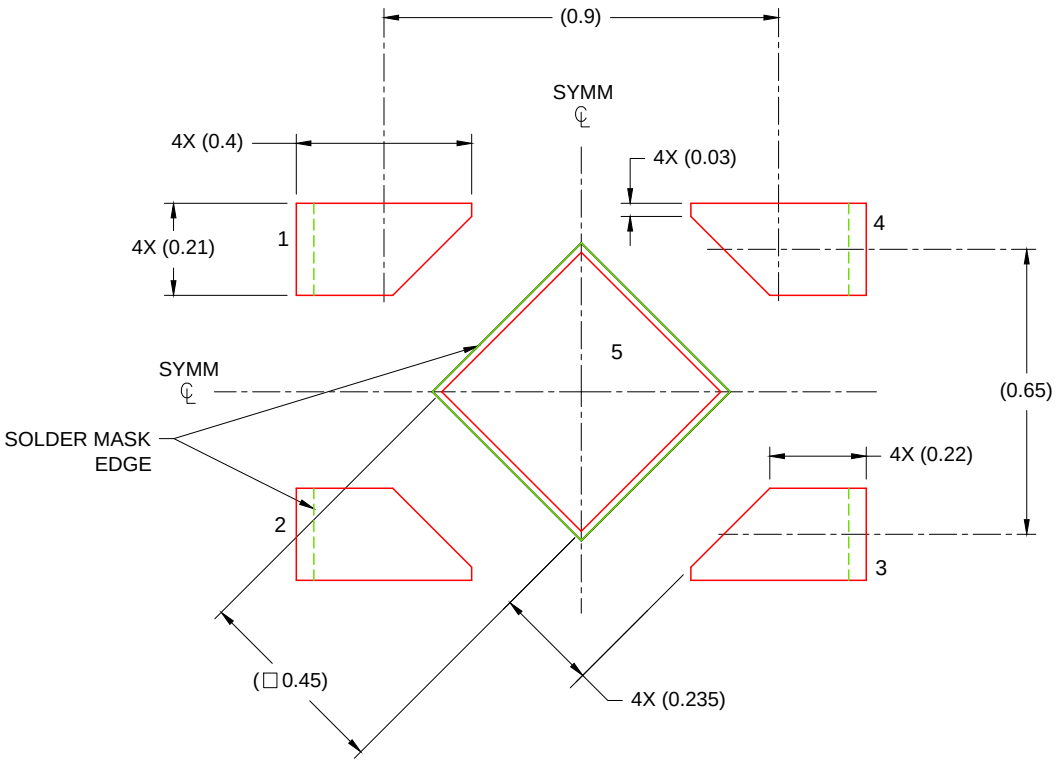

SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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