DAC161S997 16-Bit SPI-Programmable DAC for 4-20 mA Loops

1 Features

- 16-Bit Resolution
- Very-Low Supply Current of 100 µA
- 5 ppmFS/°C Gain Error
- Pin-Programmable Power-Up Condition
- Loop-Error Detection and Reporting
- Programmable Output-Current Error Levels
- Simple HART Modulator Interfacing
- Highly Integrated Feature Set in Small Footprint WQFN-16 (4- × 4-mm, 0.5-mm Pitch)

2 Applications

- Two-Wire 4- to 20-mA Current-Loop Transmitter
- Loop-Power Transmitters
- Industrial Process Control
- Actuator Control

3 Description

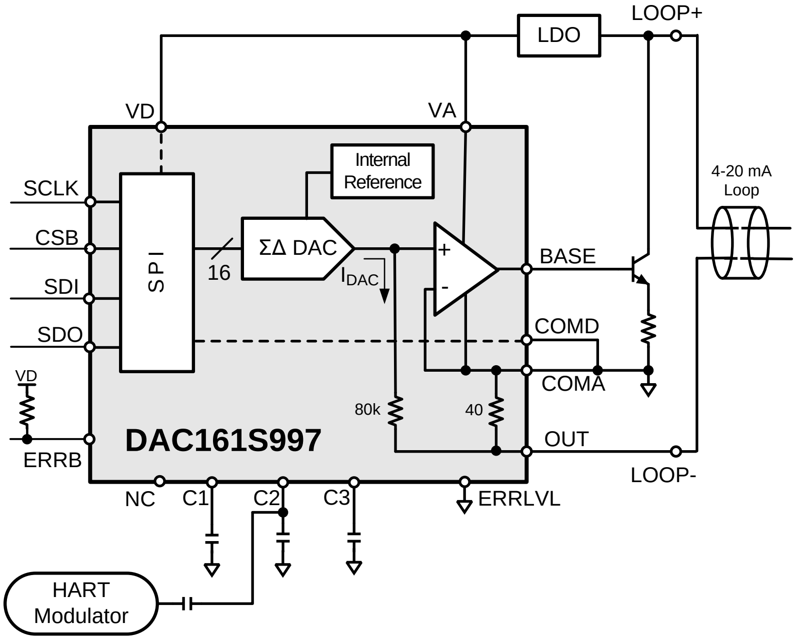
The DAC161S997 is a very low power 16-bit ΣΔ digital-to-analog converter (DAC) for transmitting an analog output current over an industry standard 4-20 mA current loop. The DAC161S997 has a simple 4-wire SPI for data transfer and configuration of the DAC functions. To reduce power and component count in compact loop-powered applications, the DAC161S997 contains an internal ultra-low power voltage reference and an internal oscillator. The low power consumption of the DAC161S997 results in additional current being available for the remaining portion of the system. The loop drive of the DAC161S997 interfaces to a Highway Addressable Remote Transducer (HART) modulator, allowing injection of FSK modulated digital data into the 4-20 mA current loop. This combination of specifications and features makes the DAC161S997 ideal for 2- and 4-wire industrial transmitters. The DAC161S997 is available in a 16-pin 4-mm × 4-mm WQFN package and is specified over the extended industrial temperature range of –40°C to +105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC161S997	WQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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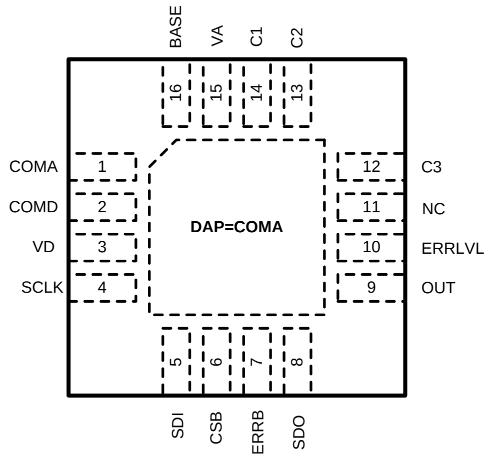
5 Revision History

Changes from Original (June 2013) to Revision A — Page

- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device* and *Documentation Support section,* and *Mechanical, Packaging, and Orderable Information section* 1

6 Pin Configuration and Functions

RGH Package
16-Pin WQFN
(Top View)



Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BASE	16	A	External NPN base drive
COMA	1	P	Analog-block negative supply rail (local COMMON)
COMD	2	P	Digital-block negative supply rail (local COMMON)
CSB	6	I	SPI chip select
C1	14	A	External capacitor
C2	13	A	External capacitor, HART input
C3	12	A	External capacitor
EERB	7	O	Error flag output, open drain, active LOW
ERRLVL	10	I	Sets output-current level at power up and under-error conditions.
NC	11	–	Do not connect to this pin.
OUT	9	A	Loop output current source output
SCLK	4	I	SPI clock input
SDI	5	I	SPI data input
SDO	8	O	SPI data output
VA	15	P	Analog-block positive supply rail
VD	3	P	Digital-block positive supply rail.
DAP	DAP	P	Die attach pad. Connect directly to local COMMON (COMA, COMD).

(1) G = Ground, I = Digital Input, O = Digital Output, P = Power, A = Analog

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage (VA, VD to COMA, COMD)	–0.3	6	V
Voltage between any two pins(2)		6	V
Current IN or OUT of any pin — except OUT pin(3)		5	mA
Output current at OUT		50	mA
Junction Temperature		150	°C
Operating Temperature	–40	105	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to COMA = COMD = 0 V, unless otherwise specified.
(3) When the input voltage (VIN) at any pin exceeds power supplies (VIN < COMA or VIN > VA), the current at that pin must not exceed 5 mA, and the voltage (VIN) at that pin relative to any other pin must not exceed 6 V. See for Pin Descriptions for additional details of input structures.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The Human Body Model (HBM) is a 100 pF capacitor charged to the specified voltage then discharged through a 1.5 kΩ resistor into each pin.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
	BASE load to COMA	0	15	pF
	(COMA - COMD)		0	V
	OUT load to COMA		none	
	(VA - VD)		0	V
VA, VDD	Supply voltage	2.7	3.6	V
T_A	Temperature	–40	105	°C

7.4 Thermal Information

		DAC161S997	UNIT
		WQFN	
		16 PINS	
$R_{\theta JA}$	Package thermal impedance(1)	35	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

Unless otherwise noted, these specifications apply for VA = VD = 3.3 V, COMA = COMD = 0 V, T_A= 25°C, external bipolar transistor: 2N3904, RE = 22 Ω, C1 = C2 = C3 = 2.2 nF.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
POWER SUPPLY						
VA, VD	Supply voltage	VA = VD -40°C ≤ T_A ≤ 105°C	2.7		3.6	V
	VA supply current	DACCODE = 0x0200(2)		43		µA
	VD supply current			57		µA
ICC	Total supply current			100	125	µA
DC ACCURACY						
N	Resolution			16		bits
INL	Integral non-linearity(3)	0x2AAA < DACCODE < 0xD555 (4 mA < I_{LOOP} < 20 mA)	–1.5		2.6	µA
DNL	Differential non-linearity	see (4)	–0.2		0.2	µA
TUE	Total unadjusted error	0x2AAA < DACCODE < 0xD555		0.01		%FS
OE	Offset error	see (5)	–7.86	0.84	7.86	µA
ΔOE	Offset error temperature coefficient	-40°C ≤ T_A ≤ 105°C		0.48		ppmFS/°C
GE	Gain error	see (6)		0.007		%FS
ΔGE	Gain error temperature coefficient	-40°C ≤ T_A ≤ 105°C		5		ppmFS/°C
IERRL	LOW ERROR current	ERR_LOW = default	3.36	3.375	3.39	mA
IERRH	HIGH ERROR current	ERR_HIGH = default	21.70	21.75	21.82	mA
LTD	Long term drift — mean shift of 12 mA output current after 1000 hours at 150°C			90		ppmFS
LOOP CURRENT OUTPUT (OUT)						
I_{OUTMIN}	Minimum output current	Tested at DACCODE = 0x01C2(7)			0.19	mA
I_{OUTMAX}	Maximum output current	Tested at DACCODE = 0xFFFF	23.95			mA
R_{OUT}	Output impedance			200		MΩ
	COMA to OUT voltage drop	I_{OUT} = 24 mA		960		mV
BASE OUTPUT						
I_{OUTSC}	BASE short circuit output current	BASE forced to COMA potential		10		mA
DYNAMIC CHARACTERISTICS						
	Output noise density	1 kHz		20		nA/rtHz
	Integrated output noise	1 Hz to 1 kHz band		300		nA_{RMS}
INTERNAL TIMER						
TM	Timeout period	Default setting of TIMEOUT in CONFIG register		100		ms
DIGITAL INPUT CHARACTERISTICS						
I_{IN}	Digital input leakage current		–10		10	µA
V_{IL}	Input low voltage				0.2 × VD	V
V_{IH}	Input high voltage		0.7 × VD			V
C_{IN}	Input capacitance			5		pF

(1) Limits are ensured by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(2) At code 0x0200 the BASE current is minimal, for example, device current contribution to power consumption is minimized. SPI is inactive, for example, after transmitting code 0x200 to the DAC161S997, there are no more transitions in the channel during the supply current measurement.
(3) INL is measured using the *best-fit* method in the output current range of 4 mA to 20 mA.
(4) Specified by design.
(5) Offset is the y-intercept of the straight line defined by 4 mA and 20 mA points of the measured transfer characteristic.
(6) Gain Error is the difference in slope of the straight line defined by measured 4 mA and 20 mA points of transfer characteristic, and that of the ideal characteristic.
(7) This must be treated as the minimum LOOP current ensured in self-powered mode.

Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for VA = VD = 3.3 V, COMA = COMD = 0 V, T_A= 25°C, external bipolar transistor: 2N3904, RE = 22 Ω, C1 = C2 = C3 = 2.2 nF.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP	MAX[1]	UNIT
DIGITAL OUTPUT CHARACTERISTICS						
V_{OL}	Output Low voltage	I_{sink} = 200 µA			0.4	V
V_{OH}	Output HIGH voltage	I_{sink} = 200 µA	2.6			V
I_{OZH}, I_{OZL}	TRI-STATE leakage current		–10		10	µA
C_{OUT}	TRI-STATE output capacitance			5		pF

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
f_{CLK}	SCLK frequency	0		10	MHz
t_H	SCLK high time	0.4 / F_{CLK}	50		ns
t_L	SCLK low time	0.4 / F_{CLK}	50		ns
t_{CSB}	CSB pulse width	5	40		ns
t_{CSS}	CSB set-up time prior to SCLK rising edge	5			ns
t_{SCH}	24th rising edge of SCLK to CSB rising edge	15			ns
t_{CSH}	CSB hold time after the 24th falling edge of SCLK	6	10		ns
t_{ZSDO}	CSB falling edge to SDO valid		10	35	ns
t_{SDOZ}	CSB rising edge to SDO HiZ		10		ns
t_{DS}	SDI data set-up time prior to SCLK rising edge	10			ns
t_{DH}	SDI data hold time after SCLK rising edge	6	10		ns
t_{DO}	SDO output data valid			30	ns

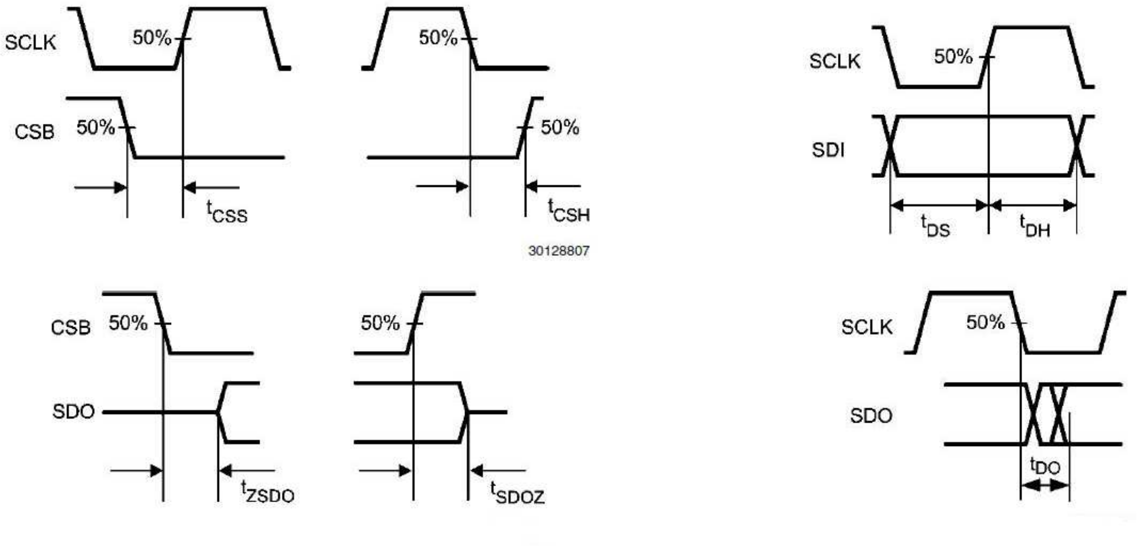


Figure 1. SPI Timing Diagrams

7.7 Typical Characteristics

Unless otherwise noted, data presented here was collected under these conditions VA = VD = 3.3 V, T_A = 25°C, external bipolar transistor: 2N3904, RE = 22 Ω, C1 = C2 = C3 = 2.2 nF.

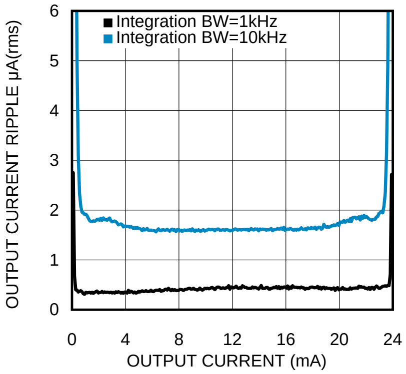


Figure 2. Intergrated Noise vs ILOOP

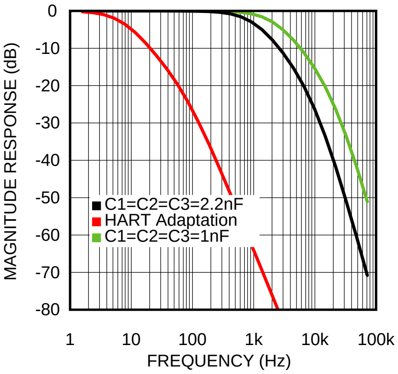


Figure 3. ΣΔ Modulator Filter Response

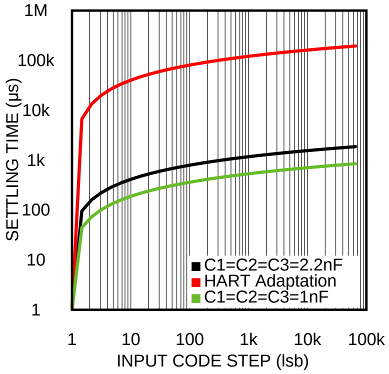


Figure 4. Settling Time vs Input Step Size

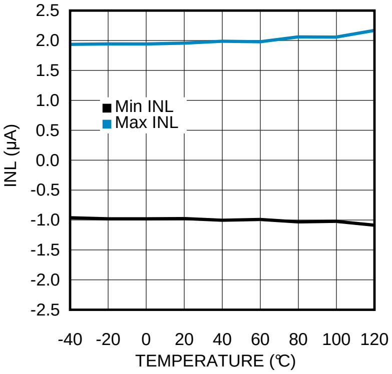


Figure 5. Output Linearity vs Temperature

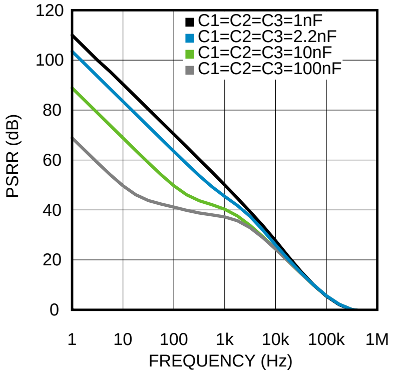


Figure 6. PSRR: I_{LOOP} = 4 mA

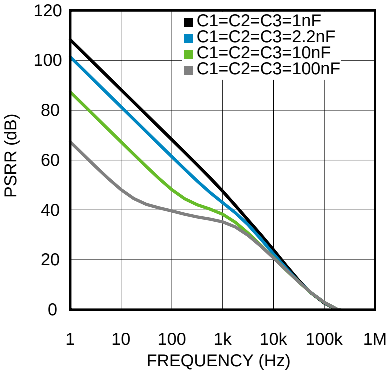


Figure 7. PSRR: I_{LOOP} = 20 mA

8 Detailed Description

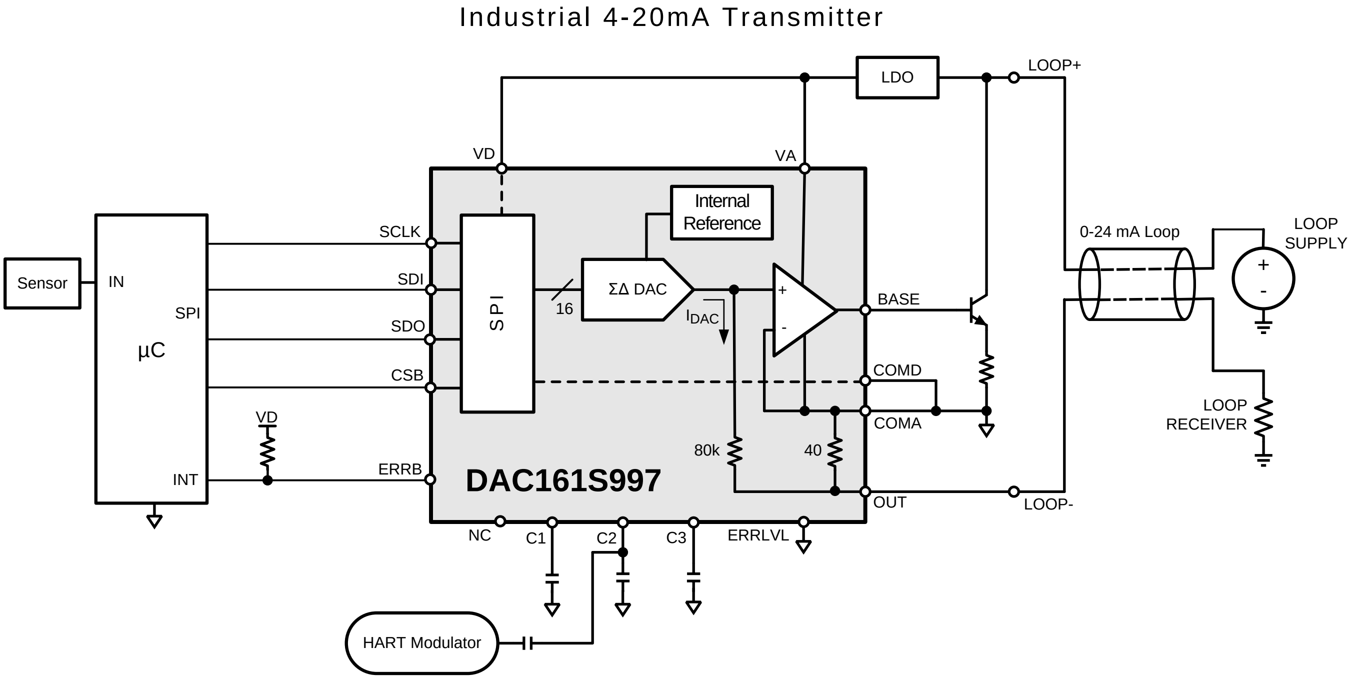
8.1 Overview

The DAC161S997 is a 16-bit DAC realized as a ∑Δ modulator. The DAC's output is a current pulse train that is filtered by the on-board low pass RC filter. The final output current is a multiplied copy of the filtered modulator output. This architecture ensures an excellent linearity performance, while minimizing power consumption of the device.

The DAC161S997 eases the design of robust, precise, long-term stable industrial systems by integrating all precision elements on-chip. Only a few external components are needed to realize a low-power, high-precision industrial 4 - 20 mA transmitter.

In case of a fault, or during initial power-up the DAC161S997 will output current in either upper or lower error current band. The choice of band is user selectable via a device pin. The error current value is user programmable via SPI.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Error Detection And Reporting

By default, the DAC161S997 detects and reports several types of errors.

8.3.1.1 Loop Error

A loop error occurs when the device is unable to sustain the required output current at OUT pin, typically caused by a drop in loop supply, or an increase in load impedance.

When a loop error occurs, the DAC161S997 changes the OUT-pin current to the value in the ERROR_LOW register, unless the MASK_LOOP_ERR is set to 1. If the MASK_LOOP_ERR is not set, then the device also periodically attempts to reassert the OUT current set in DACCODE by default. If the DACCODE-current output is set, the DAC161S997 then stops reporting a loop error. The interval between reasserts is controlled by the L_RETRY_TIME field in the ERROR_CONFIG register. If the DIS_RETRY_LOOP field in the ERROR_CONFIG register is changed to 1, the device does not periodically check the loop and, instead, only checks the loop after a read of the ERR_STATUS (0x09) register. If the loop error is not resolved, then the loop-error current persists.

Feature Description (continued)

When a loop error occurs, the DAC161S997 sets the CURR_LOOP_STATUS and LOOP_STATUS fields in the STATUS register to 1. The LOOP_STATUS field remains set to 1 until the STATUS register is read or the device is reset. If the loop error is cleared, either by the device reasserting the loop current or by changing the OUT current , then the CURR_LOOP_STATUS field clears.

8.3.1.2 SPI Timeout Error (Channel Error)

The DAC161S997 expects to receive periodic SPI write commands to ensure that the SPI connection is functioning normally. If no SPI write command occurs within the time indicated by the SPI_TIMEOUT field in the ERROR_CONFIG register, the device reports a SPI timeout error. Note that the SPI write command must be properly formatted to avoid SPI Timeout errors (such as a write command that generates a frame error does not prevent an imminent SPI Timeout error).

SPI Timeout error reporting is inhibited by MASK_SPI_TOUT. SPI Timeout errors are not reported on the loop if MASK_SPI_ERR is set to 1.

Note that a write command to address 0 is not considered a valid write command and will not prevent a SPI Timeout error.

8.3.1.3 Frame Error

If a SPI write command has an incorrect number of SCLK pulses, the device reports a frame error. The number of SCLK pulses must be an integer and a multiple of 24. A frame error is always reported by ERRB being pulled low. A frame error does not affect the loop current.

8.3.1.4 Alarm Current

By default, the DAC161S997 reports faults to the plant controller by forcing the OUT current into one of two error bands. The error current bands are defined as either greater than 20 mA, or less than 4 mA. Loop errors are reported by setting current of ERR_LOW.

If SPI Timeout Errors are reported on the loop (this is the default; it can be changed by setting the register ERR_CONFIG:MASK_LOOP_ERR), the error band is controlled by the ERRLVL pin. When ERRLVL is tied to the COMD voltage, the ERR_LOW current is the reporting current. If ERRLVL is tied to VD then the ERR_HIGH current is the current-on pin, OUT, if a SPI timeout error occurs.

The exact value of the output current used to indicate fault is dictated by the contents of ERR_HIGH and ERR_LOW registers.

In the case of a conflicting alarm-current setting (such as a loop error and SPI timeout error occurring simultaneously and ERRLVL is tied high), the current-on pin, OUT, is determined by ERR_LOW current.

8.4 Device Functional Modes

The DAC161S997 reports errors in 3 different ways, by changing the OUT pin current, pulling the ERRB pin low, and by updating the read-only register STATUS. The reporting on ERRB and OUT pin is customized by setting the ERROR_CONFIG register.

The ERRB pin connects to a GPIO pin on the microcontroller to function as an interrupt if an error occurs.

If a Loop error and a SPI Timeout error occur simultaneously and the device is configured with conflicting error output currents, the OUT pin current reports the Loop Error.

	STATUS Register	Loop Reporting	ERRB Reporting
Frame Error	Reported in FERR_STS	Not reported	Always reported
Loop Error	Reported in LOOP_STS and CURR_LOOP_STS	Reported by default unless ERR_CONFIG:MASK_LOOP_ERR is set to 1	Reported by default unless ERR_CONFIG:DIS_LOOP_ERR_ERRB is set to 1
SPI Timeout Error	Reported in SPI_TIMEOUT_ERR	Reported by default unless either ERR_CONFIG:MASK_SPI_ERR or ERR_CONFIG:MASK_SPI_TOUT are set to 1	Reported by default unless ERR_CONFIG:MASK_SPI_TOUT is set to 1

8.5 Programming

8.5.1 Serial Interface

The 4-wire interface is compatible with SPI, QSPI, and MICROWIRE, as well as most DSPs. See the *Timing Requirements* section for timing information about the read and write sequences. The serial interface is comprised of CSB, SCLK, SDIs and SDO. The DAC161S997 supports both Mode 0 and Mode 3 of the SPI protocol.

A bus transaction is initiated by the falling edge of CSB. When CSB is low, the input data is sampled at the SDI pin by the rising edge of the SCLK. The output data is asserted on the SDO pin at the falling edge of SCLK.

A valid transfer requires an integer multiple of 24 SCLK cycles. If CSB is raised before the 24th rising edge of the SCLK, the transfer aborts and a Frame Error is reported. If CSB is held low after the 24th falling edge of the SCLK and additional SCLK edges occur, the data continues to flow through the FIFO and out the SDO pin. When CSB transitions high, the internal controller decodes the most recent 24 bits that were received before the rising edge of CSB. CSB must transition to high after an integer multiple of 24 clock cycles, otherwise a Frame Error is reported and the transaction is considered invalid. When a valid number of SCLK pulses occur with CSB low, the DAC then performs the requested operation after CSB transitions high.

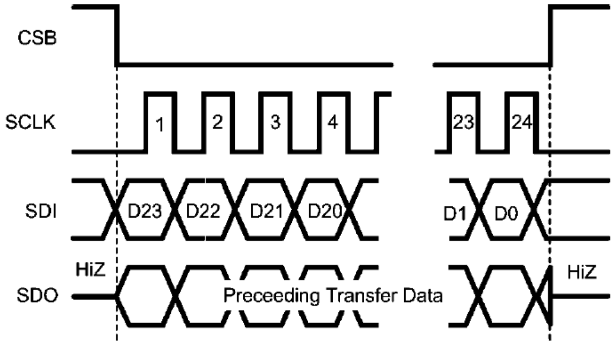


Figure 8. SPI Data Format

The acquired data is shifted into an internal 24-bit shift register (MSB first) which is configured as a 24-bit deep FIFO. As the data is being shifted into the FIFO via the SDI pin, the prior contents of the register are being shifted out through the SDO output. While CSB is high, SDO is in a high Z-state. At the falling edge of CSB, SDO presents the MSB of the data present in the shift register. SDO is updated on every subsequent falling edge of SCLK.

NOTE

The first SDO transition will happen on the first falling edge AFTER the first rising edge of SCLK when CSB is low.

The 24 bits of data contained in the FIFO are interpreted as an 8-bit COMMAND word followed by 16-bits of DATA. The general format of the 24-bit data stream is shown in Figure 9. Complete instruction set is tabulated in the *Detailed Description* section.

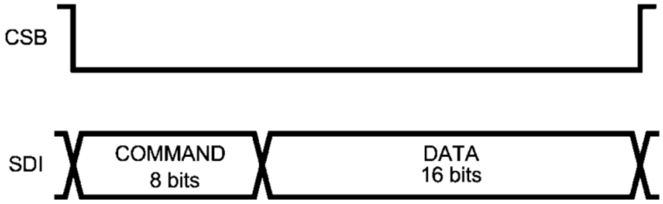


Figure 9. SPI Command and Data Words

Programming (continued)

8.5.1.1 SPI Write

SPI write operation is used to change the state of the device. Handshaking does not occur between the master and the slave (DAC161S997), and the master must control the communication on the following inputs: SCLK, CSB, SDI. The format of the data transfer is described in the *Serial Interface* section.

A write is composed of two sections, 8-bits corresponding to a command and 16-bits of data. A command is simply the address of the desired register to update. Note that some registers are read-only; a write to these registers will have no effect on the device operation and the register contents will not change. The user instruction set is shown in the *Detailed Description* section.

During power up or device reset, the register contents of all writable registers are set to the listed values in the *Detailed Description* section.

If the DAC161S997 is used in a highly noisy environment in which SPI errors are potentially an issue, the DAC161S997 supports a more robust protocol (see *Optional Protected SPI Writes*).

8.5.1.2 SPI Read

The read operation requires all 4 wires of the SPI interface, which are SCLK, SCB, SDI, and SDO. The simplest READ operation occurs automatically during any valid transaction on the SPI bus because the SDO pin of DAC161S997 always shifts out the contents of the internal FIFO. Therefore the data being shifted in to the FIFO is verified by initiating another transaction and acquiring data at SDO, allowing only for the verification of FIFO contents.

The internal registers are accessed by the user through a register read command. A register read command is formed by setting bit 7 of the command to 1 (effectively ORing with 0x80) with the address of the desired register to be read and sending the resulting 8 bits as the command (see *Detailed Description*). For example, the register read command of the STATUS register (address 0x05) would be 0x85.

A register read requires two SPI transactions to recover the register data. The first transaction shifts in the register read command; an 8-bits of command byte followed by 16-bits of *dummy* data. The register read command transfers the contents of the internal register into the FIFO. The second transaction shifts out the FIFO contents; an 8-bit command byte (which is a copy of previous transaction) followed by the register data. The Register Read operation is shown in Figure 10.

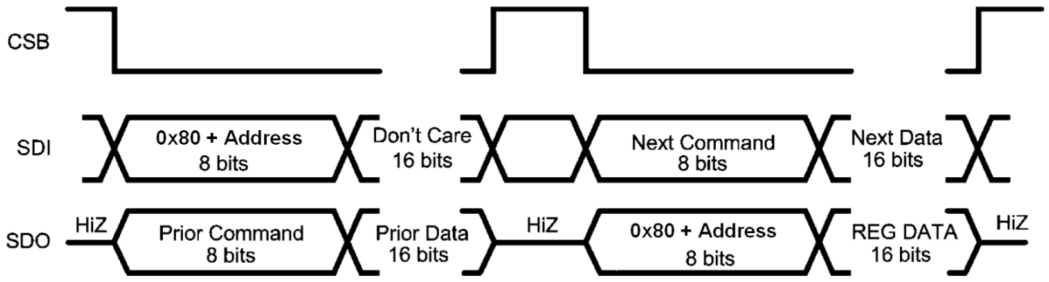


Figure 10. SPI Register Read Operation

8.5.1.3 Optional Protected SPI Writes

The DAC161S997 supports an optional SPI protocol intended to provide robust support against SPI write errors.

When PROTECT_REG_WR is set to 1, all register writes require a subsequent XFER_REG command (a write of 0x00FF to XFER_REG[0x01]) to load the transferred data into the register address (see Figure 11). This requirement provides protection against write errors in an electrically noisy environment.

Programming (continued)

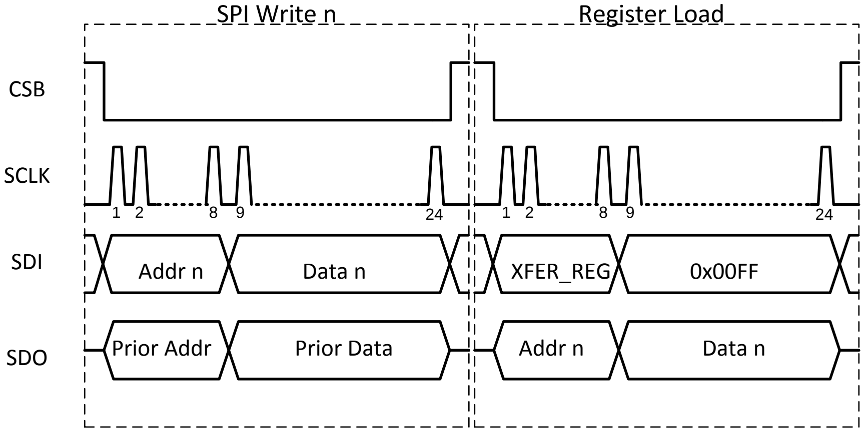


Figure 11. Protected SPI writes

8.5.1.3.1 SPI Write Error Correction

To minimize the chance of a SPI write error, TI recommends to append a NOP command onto the end of every register write sequence to verify that the XFER_REG is properly executed, as shown in Figure 12.

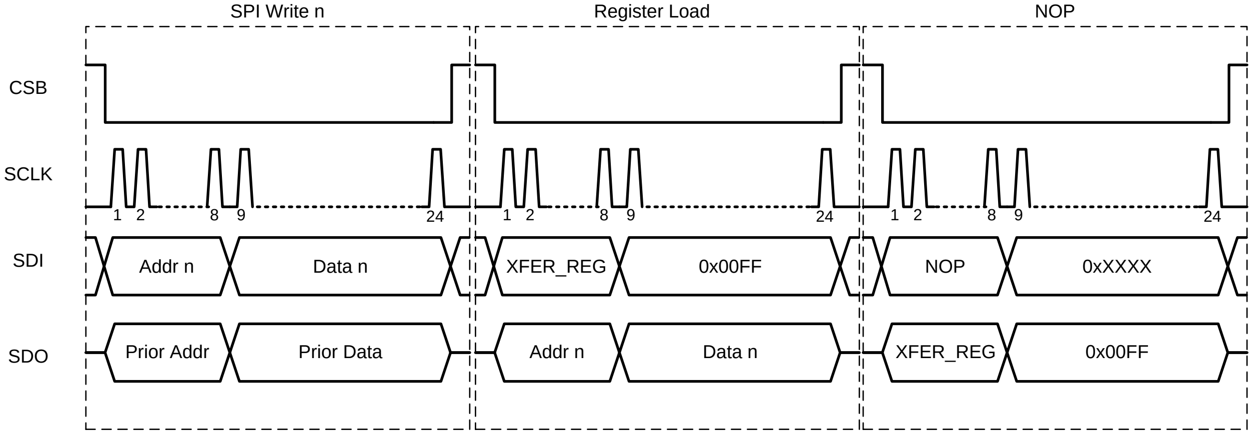


Figure 12. Protected SPI writes with NOP command

The XFER_REG command combined with the automatic SDO loopback of the previous SPI write data prevents loading of incorrect data into a register. If the loopback indicates a communication error has occurred (see Figure 13), the CSB pin is held low and the previous write command is repeated. Although the second SPI transaction had 48 SCLK pulses instead of 24 pulses, this is not considered a frame error. A frame error is indicated when the number of SCLK pulses is not an integer multiple of 24.

Programming (continued)

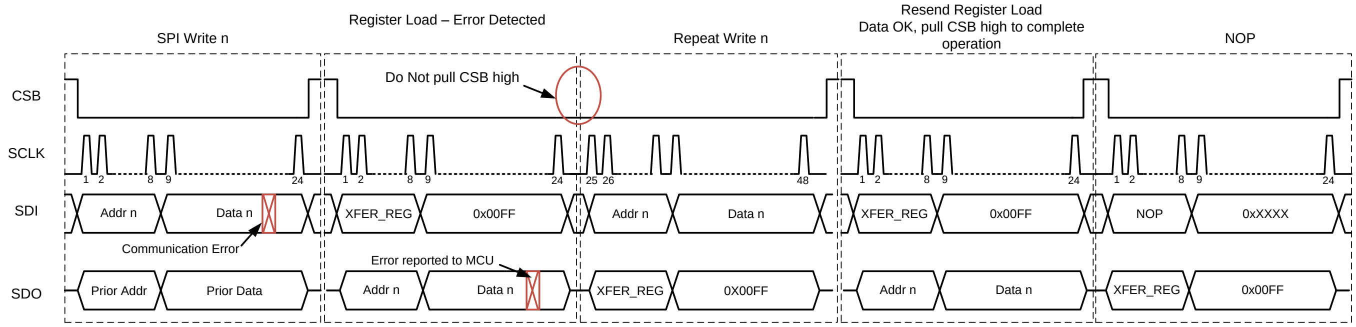


Figure 13. Detection of Error in Register Load

If a communication error occurs in the XFER_REG command, it is detected during the trailing NOP command (see Figure 14). Although the register load is incomplete, the device has not changed operations. Repeat the original data and XFER_REG command.

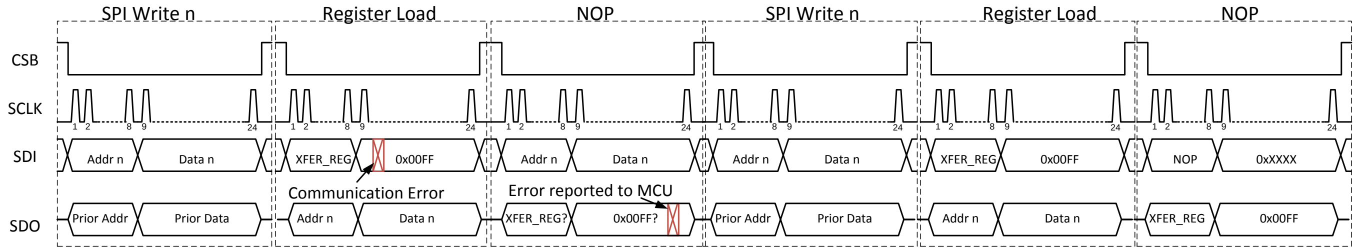


Figure 14. Detection of Error in Register Readback

8.6 Register Maps

Unless otherwise indicated, bits outside the register fields listed below are *do not care*, and will not change device configuration. Register read operations on such *do not care* fields will be 0. Registers are read/write unless indicated otherwise.

Table 1. XFER_REG (Write Only)

Address = 0x01		
Bit Field	**Field Name**	**Description**
15:0	XFER[15:0]	When PROTECT_REG_WR is set to 1, then a XFER_REG command is necessary to transfer the previous register write data into the appropriate address. Set this register to 0x00FF to perform a XFER_REG command.

Table 2. NOP

Address = 0x02		
Bit Field	**Field Name**	**Description**
15:0	NOP[15:0]	No Operation. A write to this register will not change any device configuration. This command indicates that the SPI connection is functioning and is used to avoid SPI_INACTIVE errors.

Table 3. WR_MODE

Address = 0x03; Default = 0x0000		
Bit Field	**Field Name**	**Description**
0	PROTECT_REG_WR	0: Register write data transfers to appropriate address immediately after CSB goes high. **Default value.** 1: Enable protected register transfers: all register writes require a subsequent XFER_REG command to finalize the loading of register data. Refer to *Optional Protected SPI Writes*.

Table 4. DACCODE

Address = 0x04; Default = 0x2400, 0xE800		
Bit Field	**Field Name**	**Description**
15:0	DACCODE[15:0]	16-bit natural binary word, where D15 is the MSB, which indicates the desired DAC output code. Note the default value of this register is based on the state of the ERR_LVL pin during startup or reset.

Table 5. ERR_CONFIG

Address = 0x05; Default = 0x0102		
Bit Field	**Field Name**	**Description**
10:8	L_RETRY_TIME[2:0]	L_RETRY_TIME sets the time interval between successive attempts to reassert the desired DACCODE output current when a loop error is present. This has no effect if either MASK_LOOP_ERR is set to 1 or if DIS_RETRY_LOOP is set to 1. LOOP Retry time = (L_RETRY_TIME + 1) × 50 ms **Default value** = 1 (100 ms)
7	DIS_RETRY_LOOP	0: When a loop error is occurring, periodically attempt to send desired DACCODE output current instead of the set ERR_LOW current. The interval between attempts is set by L_RETRY_TIMER. **Default value.** 1: Do not periodically reassert DACCODE output when a loop error is present; reassert DACCODE after STATUS Register is read out.
6	MASK_LOOP_ERR	0: When a LOOP error is detected the DAC161S997 outputs the current indicated by ERR_LOW instead of DACCCODE. **Default value.** 1: When a Loop Error is detected the DAC161S997 tries to maintain DACCODE current on pin OUT.
5	DIS_LOOP_ERR_ERRB	0: When a LOOP error is detected the DAC161S997 drives ERRB pin low. **Default value.** 1: When a LOOP error is detected the DAC161S997 does not drive ERRB pin low.
4	MASK_SPI_ERR	0: SPI timeout errors change the OUT pin current to an error value, which is determined by ERRLVL pin and contents of ERR_LOW or ERR_HIGH. **Note:** MASK_SPI_TOUT must be set to 0 for this to be reported. **Default value.** 1: SPI timeout errors do not change the OUT pin current to an error value.
3:1	SPI_TIMEOUT[2:0]	SPI_TIMEOUT sets the time interval for SPI timeout error reporting. After each SPI write command, an internal timer is reset; if no subsequent write occurs before the timer reaches SPI timeout, a SPI timeout error is reported. SPI_ERROR reporting is inhibited by setting MASK_SPI_TOUT. A NOP write is considered a valid write and resets the timer without changing the device configuration. SPI Timeout = (SPI_TIMEOUT + 1) × 50 ms **SPI_TIMEOUT default value = 1 (100 ms)**
0	MASK_SPI_TOUT	0: SPI timeout error reporting is enabled. A SPI timeout error drives ERRB low when a SPI Timeout error occurs. **Default value.** 1: SPI timeout error reporting is inhibited.

Table 6. ERR_LOW

Address = 0x06; Default = 0x2400		
Bit Field	**Field Name**	**Description**
15:8	ERR_LOW[7:0]	Under some error conditions the output current corresponding to this value is the DAC output, regardless of the value of DACCODE. The ERR_LOW value is used as the upper byte of the DACCODE, while the lower byte is forced to 0x00. ERR_LOW must be between 0x00(0 mA) and 0x80(12 mA). The DAC161S997 ignores any value outside of that range and retains the previous value in the register. Refer to the *Error Detection And Reporting* section for additional details. The default value is 0x24, which corresponds to approximately 3.37 mA on pin OUT.

Table 7. ERR_HIGH

Address = 0x07; Default = 0xE800		
Bit Field	**Field Name**	**Description**
15:8	ERR_HIGH[7:0]	Under some error conditions the output current corresponding to this value is the DAC output, regardless of the value of DACCODE. The ERR_HIGH value is used as the upper byte of the DACCODE, while the lower byte is forced to 0x00. ERR_HIGH must be greater than or equal to 0x80 (12 mA). The DAC161S997 ignores any value below 0x80 and retains the previous value in the register. Refer to the *Error Detection And Reporting* section for additional details. The default value is 0xE8, which corresponds to approximately 21.8 mA on pin OUT.

Table 8. RESET

Address = 0x08		
Bit Field	**Field Name**	**Description**
15:0	RESET[15:0]	Write 0xC33C to the RESET register followed by a NOP to reset the device. All writable registers are returned to default values.

Table 9. STATUS (Read-Only)

Address = 0x09 or 0x7F		
Bit Field	**Field Name**	**Description**
7:5	DAC_RES[2:0]	DAC resolution On DAC161S997, returns a 111.
4	ERRLVL_PIN	Returns the state of the ERRLVL pin: 1 = ERRLVL pin is tied HIGH 0 = ERRLVL pin is tied LOW
3	FERR_STS	Frame-error status sticky bit 1 = A frame error has occurred since the last STATUS read. 0 = No frame error occurred since the last STATUS read. This error is cleared by reading the STATUS register. A frame error is caused by an incorrect number of clocks during a register write. A register write without an integer multiple of 24 clock cycles will cause a Frame error.
2	SPI_TIMEOUT_ERR	SPI time out error 1 = The SPI interface has not received a valid command within the interval set by SPI_TIMEOUT. 0 = The SPI interface has received a valid command within the interval set by SPI_TIMEOUT If this error occurs, it is cleared with a properly formatted write command to a valid address.

Table 9. STATUS (Read-Only) (continued)

Address = 0x09 or 0x7F		
Bit Field	**Field Name**	**Description**
1	LOOP_STS	Loop status sticky bit 1 = A loop error has occurred since last read of STATUS. 0 = No loop error has occurred since last read of STATUS. Returns the loop error status. When the value in this register is 1, the DAC161S997 is unable to maintain the output current set by DACCODE at some point since the last STATUS read. This indicator clears after reading the STATUS register.
0	CURR_LOOP_STS	Current loop status 1 = A loop error is occurring. 0 = No loop error is occurring. Returns the current Loop error status. When the value in this register is 1, the DAC161S997 is unable to maintain the output current set by DACCODE.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 16-bit Dac And Loop Drive

9.1.1.1 DC Characteristics

The DAC converts the 16-bit input code in the DACCODE registers to an equivalent current output. The ΣΔ DAC output is a current pulse which is then filtered by a third-order RC lowpass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin.

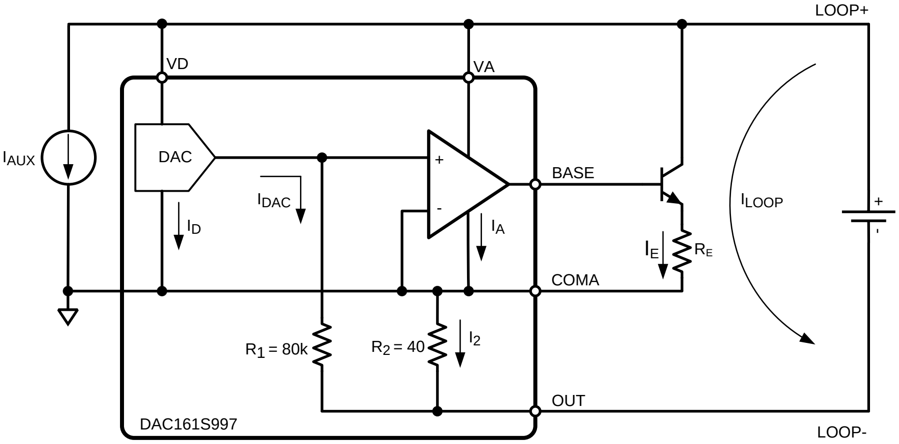


Figure 15. Loop-Powered Transmitter

Figure 15 shows the principle of operation of the DAC161S997 in the Loop-Powered Transmitter (the circuit details are omitted for clarity). In Figure 15, I_D and I_A represent supply (quiescent) currents of the internal digital and analog blocks. I_{AUX} represents supply (quiescent) current of companion devices present in the system, such as the voltage regulator and the digital interface. Because both the control loop formed by the amplifier and the bipolar transistor force the voltage across R_1 and R_2 to be equal, under normal conditions, the I_{LOOP} is dependent only on I_{DAC} through the following relationship (see Equation 1).

$$I_{LOOP} = (1 + R1 / R2)\, I_{DAC}$$

where

- $I_{DAC} = f(\text{DACCODE})$ (1)

Although I_{Loop} has a number of component currents, $I_{LOOP} = I_{DAC} + I_D + I_A + I_{AUX} + I_E$, only I_E is regulated by the loop to maintain the relationship shown in Equation 1. Because only the magnitude of I_E is controlled, not the direction, there is a lower limit to I_{LOOP}. This limit is dependent on the fixed components I_A and I_D, and on system implementation through I_{AUX}.

Application Information (continued)

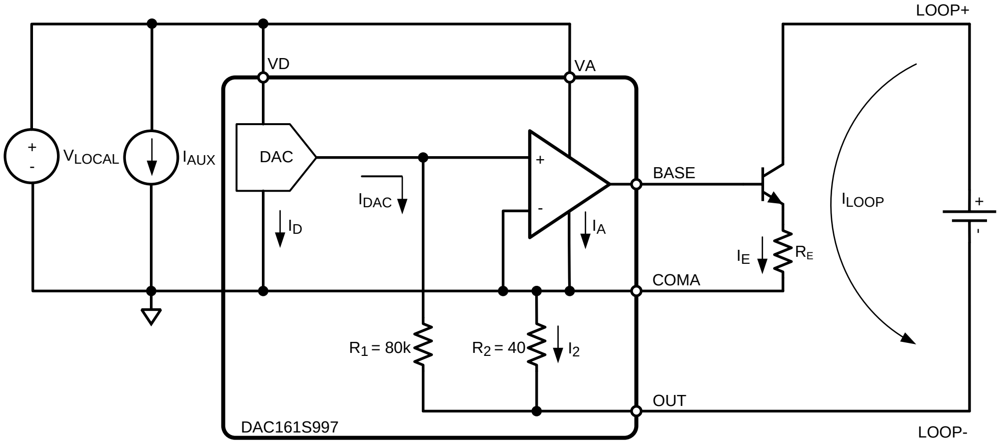


Figure 16. Self-Powered Transmitter

Figure 16 shows the variant of the transmitter where the local supply provides supply currents to the system blocks, and not the 4-20mA loop Self-Powered Transmitter. The ame basic relationship between the I_{LOOP} and I_{DAC} continues, but the component currents of I_{LOOP} are only I_{DAC} and I_E.

9.1.1.2 DC Input-Output Transfer Function

The output current sourced by the OUT pin of the device is expressed by Equation 2.

$$I_{LOOP} = 24\ \text{mA}\ (\text{DACCODE} / 2^{16}) \tag{2}$$

The valid DACCODE range is the full 16-bit code space (0x0000 to 0xFFFF), resulting in the I_{DAC} range of 0 to approximately 12 µA, which, however, does not result in the I_{LOOP} range of 0 to 24 mA. The maximum output current sourced out of OUT pin, I_{LOOP}, is 24 mA. The minimum output current is dependent on the system implementation. The minimum output current is the sum of the supply currents of the DAC161S997 internal blocks, I_A, I_D, and companion devices present in the system, I_{AUX}. The last component current, I_E, is theoretically controlled down to 0, however, due to the stability considerations of the control loop, not allowing the I_E to drop below 200 µA is advised.

The graph in Figure 17 shows the DC transfer characteristic of the 4-20mA transmitter, including minimum current limits. The minimum current limit for the Loop-Powered Transmitter is typically around 400 µA (I_D+ I_A + I_{AUX} + I_E). The minimum current limit for the Self-Powered Transmitter is typically around 200 µA (I_E). Typical values for I_D and I_A are listed in the *Electrical Characteristics* table. I_E depends on the BJT device used.

Application Information (continued)

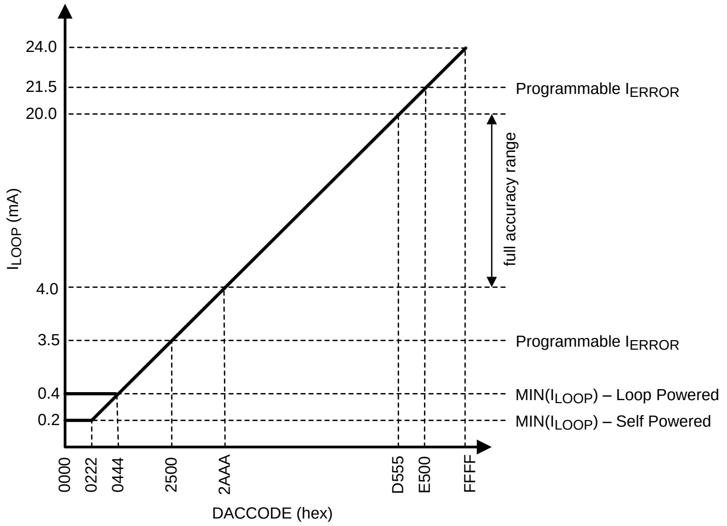


Figure 17. DAC-DC Transfer Function

9.1.1.3 Loop Interface

The DAC161S997 cannot directly interface to the typical 4 - 20 mA loop due to the excessive loop supply voltage. The loop interface has to provide the means of stepping down the LOOP Supply to 3.6V. This can be accomplished with either a linear regulator (LDO) or switching regulator while keeping in mind that the regulator's quiescent current will have direct effect on the minimum achievable I_{LOOP} (see *DC Input-Output Transfer Function*).

The second component of the loop interface is the external NPN transistor (BJT). This device is part of the control circuit that regulates the transmitter's output current (I_{LOOP}). Since the BJT operates over the wide current range, spanning at least 4 - 20 mA, it is necessary to degenerate the emitter in order to stabilize transistor's transconductance (g_m). The degeneration resistor of 22Ω is suggested in typical applications. For circuit details, see Figure 21.

The NPN BJT should not be replaced with an N-channel FET (Field Effect Transistor) for the following reasons: discrete FET's typically have high threshold voltages (VT), in the order of 1.5V to 2V, which is beyond the BASE output maximum range; discrete FET's present higher load capacitance which may degrade system stability margins; and BASE output relies on the BJT's base current for biasing.

9.1.1.4 Loop Compliance

The maximum V(LOOP+,LOOP-) potential is limited by the choice of step-down regulator, and the external BJT's Collector Emitter breakdown voltage. For minimum V(LOOP+, LOOP−) potential consider TROUBLE Figure 16. Here, observe that V(LOOP+,LOOP−) ≅ min(V_{CE}) + $I_{LOOP}R_E$ + $I_{LOOP}R_2$ = min(V_{CE}) + 0.53V + 0.96V = 3.66V, at I_{LOOP} = 24mA. The voltage drop across internal R_2 is specified in *Electrical Characteristics*.

9.1.1.5 AC Characteristics

The approximate frequency dependent characteristics of the loop drive circuit can be analyzed using the circuit in Figure 18.

Application Information (continued)

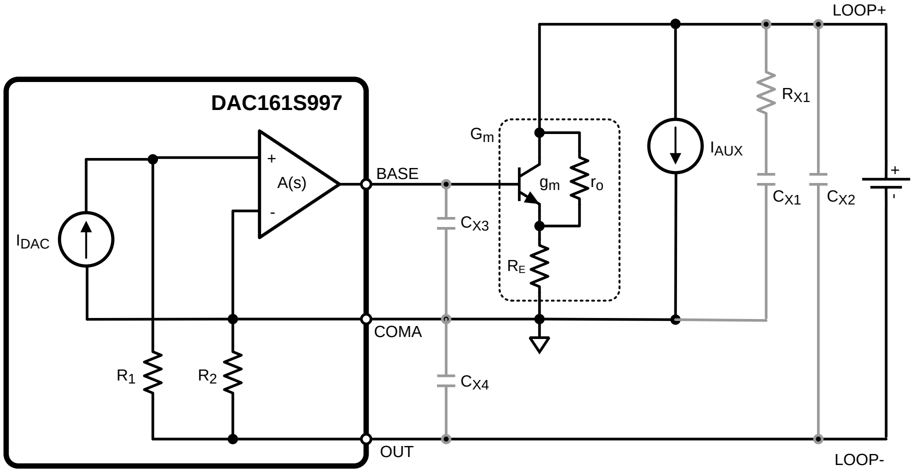


Figure 18. Capacitances Affecting Control Loop

Here it is assumed that the internal amplifier dominates the frequency response of the system, and it has a single pole response. The BJT's response, in the bandwidth of the control loop, is assumed to be frequency independent and is characterized by the transconductance g_m and the output resistance r_o.

As in previous sections I_{DAC} and I_{AUX} represent the filtered output of the ∑Δ modulator and the quiescent current of the companion devices.

The circuit in Figure 18 can be further simplified by omitting the on-board capacitances, whose effect will be discussed in *Stability*, and by combining the amplifier, the external transistor and resistor R_E into one G_m block. The resulting circuit is shown in Figure 19.

By assuming that the BJT's output resistance (r_o) is large, the loop current I_{LOOP} can be expressed as:

$$I_{LOOP} = I_{AUX} + A(s)\,G_m v_e \tag{3}$$

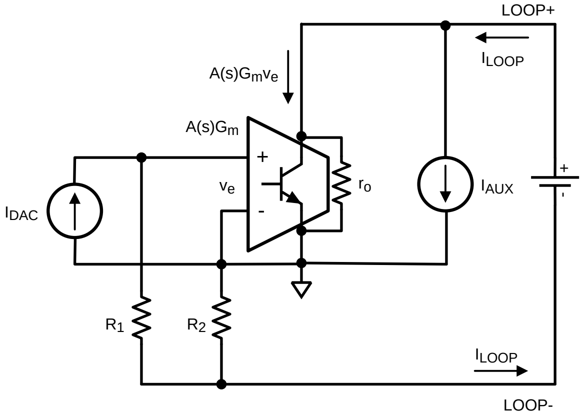


Figure 19. AC Analysis Model of a Transmitter

The sum of voltage drops around the path containing R_1, R_2 and v_e is:

$$v_e = I_{DAC} R_1 - \left[I_{AUX} + A(s)\,G_m v_e - I_{DAC}\right] R_2 \tag{4}$$

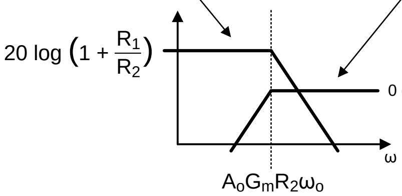
An assumption is made on the response of the internal amplifier:

$$A(s) = \frac{A_0 \omega_0}{s} \tag{5}$$

Application Information (continued)

By combining the above the final expression for the I_{LOOP} as a function of 2 inputs I_{DAC} and I_{AUX} is:

$$I_{LOOP} = I_{DAC}\underbrace{\left(1+\frac{R_1}{R_2}\right)\frac{A_oG_mR_2\omega_o}{s + A_oG_mR_2\omega_o}} + I_{AUX}\underbrace{\frac{s}{s + A_oG_mR_2\omega_o}}$$



(6)

The result above reveals that there are 2 distinct paths from the inputs I_{DAC} and I_{AUX} to the output I_{LOOP}. I_{DAC} follows the low-pass, and the I_{AUX} follows the high-pass path.

In both cases the corner frequency is dependent on the effective transconductance, G_m, of the external transistor. This implies that control loop dynamics could vary with the output current I_{LOOP} if G_m were allowed to be just native device transconductance g_m. This undesirable behavior is mitigated by the degenerating resistor R_E which stabilizes G_m as follows:

$$G_m \cong \frac{1}{1/g_m + R_E} \cong \frac{1}{R_E} \tag{7}$$

This results in the frequency response which is largely independent of the output current I_{LOOP}:

$$I_{LOOP} = I_{DAC}\left(1+\frac{R_1}{R_2}\right)\frac{A_o\frac{R_2}{R_E}\omega_o}{s + A_o\frac{R_2}{R_E}\omega_o} + I_{AUX}\frac{s}{s + A_o\frac{R_2}{R_E}\omega_o} \tag{8}$$

While the bandwidth of the I_{DAC} path may not be of great consequence given the low frequency nature of the 4-20 mA current loop systems, the location of the pole in the I_{AUX} path directly affects PSRR of the transmitter circuit. This is further discussed in PSRR .

9.1.1.5.1 Step Response

The transient input-output characteristics of the DAC161S997 are dominated by the response of the RC filter at the output of the ∑Δ DAC. Settling times due to step input are shown in *Typical Characteristics*.

9.1.1.5.2 Output Impedance

The output impedance is described as:

$$R_{OUT} = \frac{\Delta V_{LOOP}}{\Delta I_{LOOP}} \tag{9}$$

By considering the circuit in Figure 19, and setting $I_{DAC} = I_{AUX} = 0$, the following expression can be obtained:

$$R_{OUT}(s) = R_2 + \left[1 + A(s)G_mR_2\right]r_o \tag{10}$$

As in *AC Characteristics* an assumption can be made on the frequency response of the internal amplifier, and the effective transconductance G_m should be stabilized with external R_E leading to:

$$R_{OUT}(s) \approx \frac{A_o\left(\frac{R_2}{R_E}\right)\omega_o r_o}{s} \tag{11}$$

The output impedance of the transmitter is a product of the external BJT's output resistance r_o, and the frequency characteristics of the internal amplifier. At low frequencies this results in a large impedance that does not significantly affect the output current accuracy.

Application Information (continued)

9.1.1.5.3 PSRR

Power Supply Rejection Ratio is defined as the ability of the current control loop to reject the variations in the supply current of the companion devices, I_{AUX}. Specifically:

$$PSRR = 20\ x\log_{10}\left(\frac{\Delta I_{LOOP}}{\Delta I_{AUX}}\right) \tag{12}$$

It was shown in *AC Characteristics* that the I_{AUX} affects I_{LOOP} via the high-pass path whose corner frequency is dependent on the effective Gm of the external BJT. If that dependence were not mitigated with the degenerating resistor R_E, the PSRR would be degraded at low output current I_{LOOP}.

The typical PSRR performance of the transmitter shown in Figure 6 is shown in *Typical Characteristics*.

9.1.1.5.4 Stability

The current control loop's stability is affected by the impedances present in the system. Figure 18 shows the simplified diagram of the control loop, formed by the on-board amplifier and an external BJT, and the lumped capacitances C_{X1} through C_{X4} that model any other external elements.

C_{X1} typically represents a local step-down regulator, or LDO, and any other companion devices powered from the LOOP+. This capacitance reduces the stability margins of the control loop, and therefore it should be limited. RX1 can be used to isolate C_{X1} from LOOP+ node and thus remedy the stability margin reduction. If $R_{X1} = 0$, C_{X1} cannot exceed 10 nF. $R_{X1} = 200\Omega$ is recommended if it can be tolerated. Minimum $R_{X1} = 40\Omega$ if C_{X1} exceeds 10 nF.

C_{X3} also adversely affects stability of the loop and it must be limited to 20 pF. C_{X4} affects the control loop in the same way as C_{X1}, and it should be treated in the same way as C_{X1}. C_{X2} is the only capacitance that improves stability margins of the control loop. Its maximum size is limited only by the safety requirements.

Stability is a function of I_{LOOP} as well. Since I_{LOOP} is approximately equal to the collector current of the external BJT, G_m of the BJT, and thus loop dynamics, depend on I_{LOOP}. This dependence can be reduced by degenerating the emitter of the BJT with a small resistance as discussed in *Loop Interface*. Inductance in series with the LOOP+ and LOOP− do not significantly affect the control loop.

9.1.1.5.5 Noise and Ripple

The output of the DAC is a current pulse train. The transition density varies throughout the DAC input code range (I_{LOOP} range). At the extremes of the code range, the transition density is the lowest which results in low frequency components of the DAC output passing through the RC filter. Hence, the magnitude of the ripple present in I_{LOOP} is the highest at the ends of the transfer characteristic of the device (see *Typical Characteristics*).

It should be noted that at wide noise measurement bandwidth, it is the ripple due to the ∑Δ modulator that dominates the noise performance of the device throughout the entire code range of the DAC. This results in the “U” shaped noise characteristic as a function of output current. At narrow bandwidths, and particularly at mid-scale output currents, it is the amplifier driving the external BJT that starts to dominate as a noise source.

9.1.1.5.6 Digital Feedthrough

Digital feedthrough is indiscernible from the ripple induced by the ∑Δ modulator.

9.1.1.5.7 HART Signal Injection

The HART specification requires minimum suppression of the sensor signal in the HART signal band (1-2 kHz) of about 60 dB. The filter in Figure 20 below meets that requirement.

Application Information (continued)

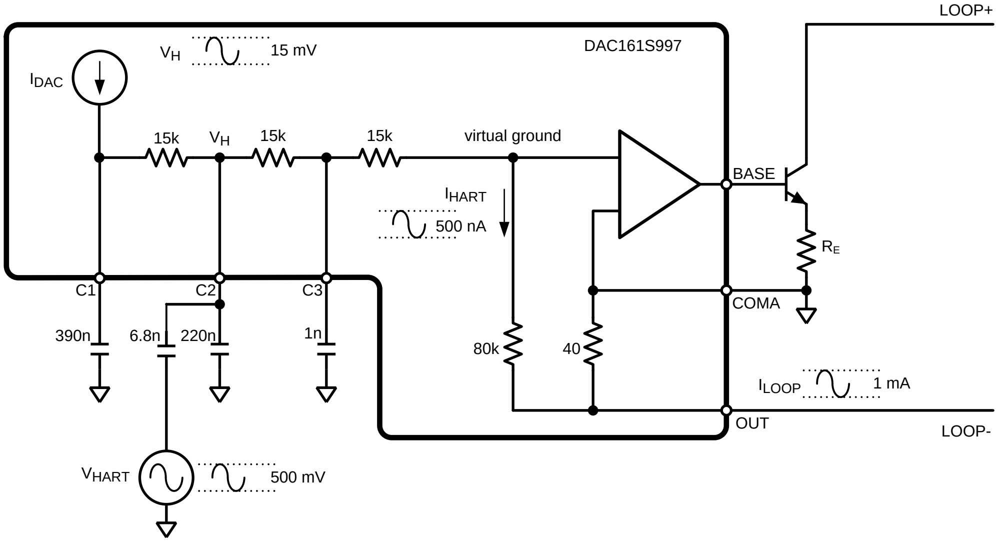


Figure 20. HART Signal Injection

9.1.1.5.8 RC Filter Limitation

In an effort to speed up the transient response of the device the user can reduce the capacitances associated with the low-pass filter at the output of the ∑Δ modulator. However, to maintain stability margins of the current control loop it is necessary to have at least $C_1 = C_2 = C_3 = 1nF$.

9.2 Typical Application

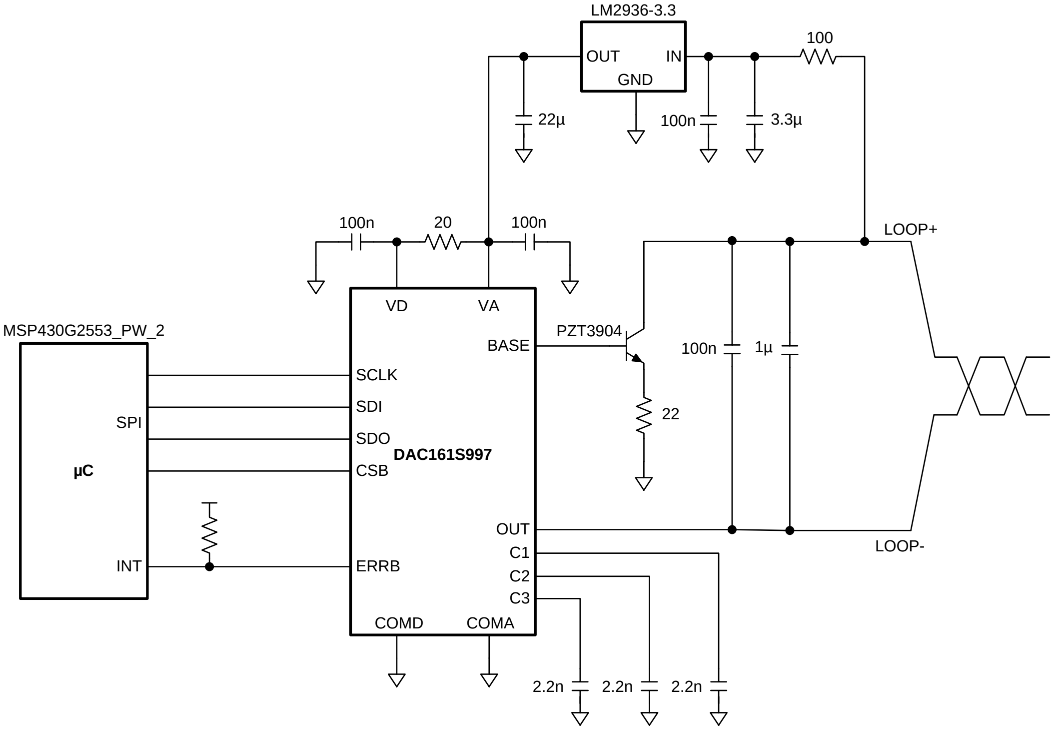


Figure 21. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

The objective of the example below is to focus on the design of a robust, low-power, precise, long- term stable, 2-wire, loop-powered, 4- to 20-mA current-output temperature transmitter by making best use of signal chain, power and computing solutions. This design uses a RTD-temperature sensor with a 4- to 20-mA current-loop transmitter.

9.2.2 Detailed Design Procedure

The DAC161S997output is a current pulse which is then filtered by a third-order RC low-pass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin. Figure 22 shows the principle of operation of the DAC161S997 in the loop-powered transmitter. The I_{LOOP} has a number of component currents as given in Equation 13.

$$I_{LOOP} = I_{DAC} + I_D + I_A + I_E = 24\text{ mA} \times \left[\frac{DAC\_CODE}{2^{16}}\right]$$

where

- I_{DAC} = f(DAC_CODE),
- I_D and I_A represent the supply currents of internal digital and analog blocks,
- I_{AUX}represents the supply current of companion devices present in the system,
- I_E is the only component which is regulated by the control loop to ensure that the actual loop current corresponds to the DAC input code applied by the MCU.

(13)

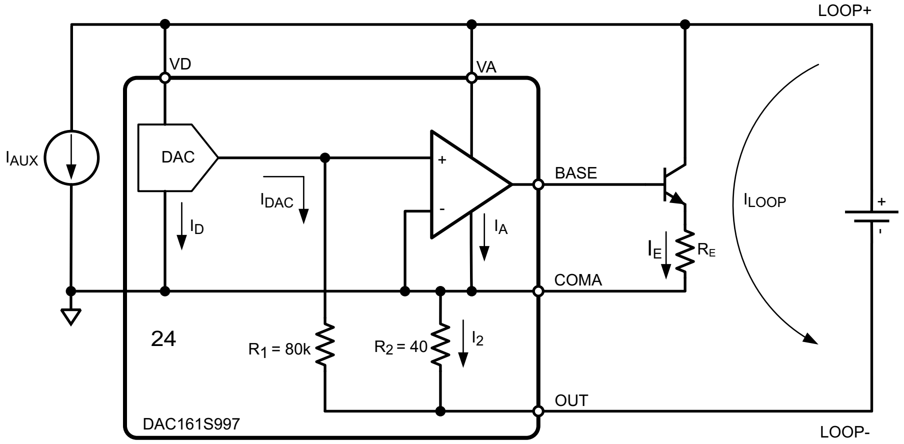


Figure 22. Loop Powered Transmitter

9.2.2.1 Reasons for Choosing a 3.9-V Zener Diode

The first and most important requirement for the proper functioning of the entire circuitry is a stable power supply. A good design ensures that the LDO gets the sufficient input voltage (V_{IN_LDO}) to generate a stable 3.3 V under minimum-loop, power-supply voltage and minimum-loop current conditions.

$$V_{IN\_LDO\ (MIN\ REQUIRED\ at\ 3.3\ mA)} = V_{CC} + V_{DO(MIN)} = 3.3\text{ V} + 0.1\text{ V} = 3.4\text{ V} \tag{14}$$

From the circuit implementation, it is evident that the LDO input voltage V_{IN_LDO} is function of loop current and collector-emitter drop (V_{CE}) of the bipolar junction transistor (BJT). Apply Kirchhoff ' s Voltage Law (KVL) in the inner loop:

$$V_{(IN\_LDO)} = [(R_C \times I_{LOOP}) + V_{ZENER} + V_{CE} + (R_E \times I_{LOOP})] \tag{15}$$

At minimum loop power supply voltage, BJT operation is pushed towards saturation, which means that V_{CE} is approximately 0 V (minimum). Due to the stability considerations of the current control loop, the minimum output current ($I_{LOOP(MIN)}$) below 200 μ A is not advised as shown in Figure 23.

$$V_{(IN\_LDO)}\text{ (at minimum }V_{SUPPLY}\text{ \& minimum }I_{LOOP}) = [(R_C \times I_{LOOP(MIN)}) + V_{ZENER} + V_{CE(MIN)} + (R_E \times I_{LOOP(MIN)})] \tag{16}$$

Typical Application (continued)

To ensure stable 3.3-V LDO output under these conditions, the following relation must be fulfilled.

$$V_{(IN\_LDO)} \text{ (at minimum } V_{SUPPLY} \text{ \& minimum } I_{LOOP}\text{)} > V_{IN\_LDO\ (MIN\ REQUIRED\ at\ 3.3\ mA)} \qquad (17)$$

$$[(100\ \Omega \times 200\ \mu A) + V_{ZENER} + 0\ V + (20\ \Omega\ X\ 200\ \mu A)] > 3.4\ V$$

$$[V_{ZENER} + 0.024\ V] > 3.4\ V$$

From Equation 17, it is clear that without having a zener diode, a voltage greater than 3.4 V at the input of the LDO cannot be ensured. Therefore, choose a zener diode having a zener voltage (V_{ZENER}) greater than 3.4 V and able to handle power dissipation, $P_{DZ} = V_{ZENER} \times I_{LOOP(MAX)}$. In this application, the design uses a 3.9-V, 500-mW zener diode.

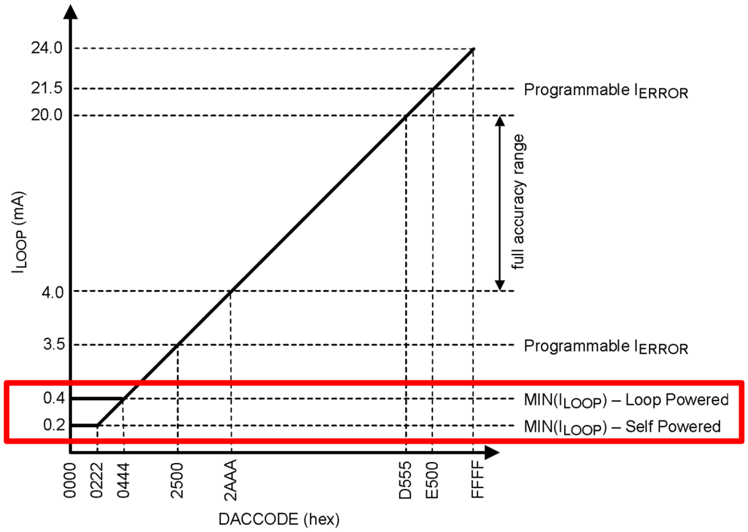


Figure 23. DAC DC Transfer Function

9.2.2.2 Loop Compliance Voltage

To calculate the minimum-loop, compliance-voltage (loop-power supply voltage), add all voltage drops in the loop at the maximum-expected loop current.

From a current control loop stability point of view, $V_{CE(MIN)}$ must stay greater than maximum $V_{CE(SAT)}$:

$$V_{CE(MIN)} > 0.2\ V \qquad (18)$$

Applying Kirchhoff 's Voltage Law in the outer loop, to find out the $V_{CE(MIN)}$:

$$V_{CE(MIN)} = V_{SUPPLY(MIN)} - (2 \times V_{WIRE}) - (2 \times V_F) - V_{RC(MAX)} - V_{ZENER} - V_{RE(MAX)} - V_{SENSE(MAX)} - V_{LOAD(MAX)}$$

where

- $2 \times V_{WIRE}$ is voltage drop across system wiring. If system wiring runs over a length (L) along one way, wire resistance per unit length is ρ and current in the loop is I_{LOOP}, then the voltage drop for one conductor can be given as:
- $V_{WIRE(MAX)} = \rho \times L \times I_{LOOP(MAX)}$
- For example, a 24-AWG wire has resistance per unit length (ρ) of 0.026 Ω /ft or 0.0755 Ω /m.
- V_{LOAD} is the voltage drop caused by the internal resistance of the loop receiver. The internal resistance of the loop receiver may vary from 50 Ω to 250 Ω .
- $V_{LOAD(MAX)} = R_{LOAD} \times I_{LOOP(MAX)}$
- V_{SENSE} is the voltage drop across 40- Ω sense resistor internal to the DAC.
- V_F is the forward-voltage drop across the reverse polarity protection diode.
- $V_F = 0.7$ V at 30 mA forward current (from TVS data sheet, *SM6T39CA Data Sheet,* SM6T39CA). (19)

Rewriting Equation 19,

$$V_{SUPPLY(MIN)} > 0.2\ V + (2 \times \rho \times L \times I_{LOOP(MAX)}) + (2 \times 0.7\ V) + (100\ \Omega \times I_{LOOP(MAX)}) + 3.9\ V + (20\ \Omega \times I_{LOOP(MAX)}) + (40\ \Omega \times I_{LOOP(MAX)}) + (R_{LOAD} \times I_{LOOP(MAX)}) + (40\ \Omega \times I_{LOOP(MAX)}) + (R_{LOAD} \times I_{LOOP(MAX)}) \qquad (20)$$

Typical Application (continued)

The maximum output current that can be sourced out of the OUT pin by DAC161S997, I LOOP (MAX) , is approximately 24 mA.

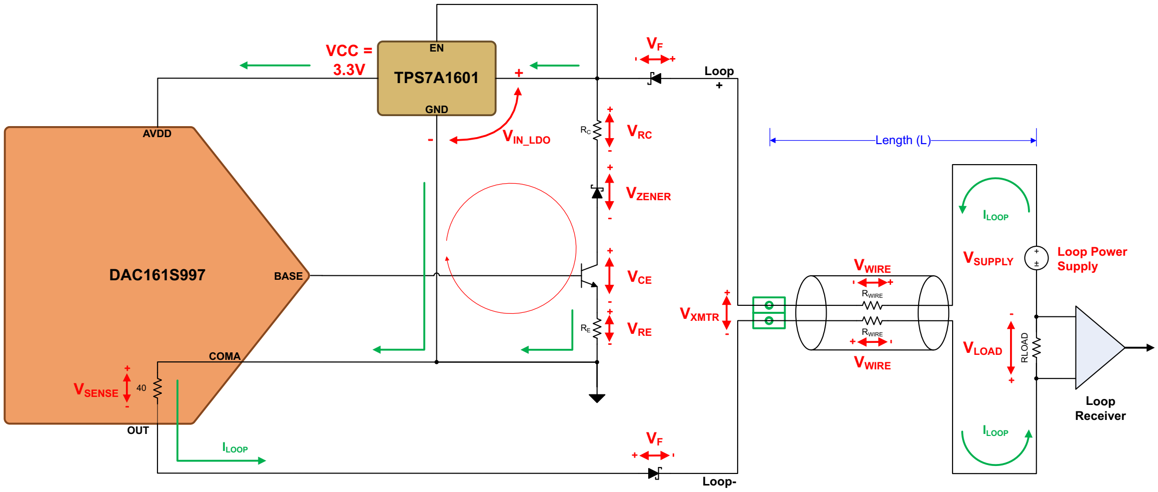
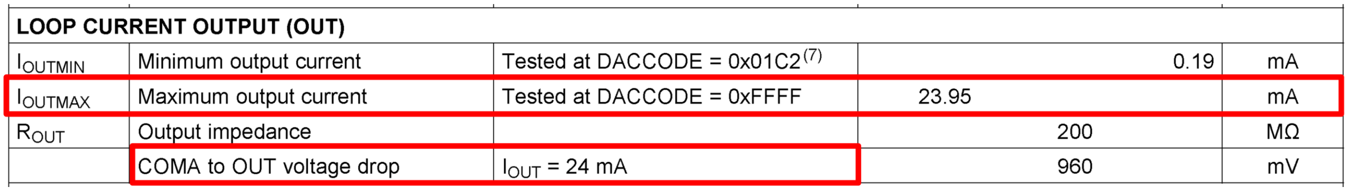


Figure 24. Series Voltage Drops in Current Loop System



LOOP CURRENT OUTPUT (OUT)				
I_{OUTMIN}	Minimum output current	Tested at DACCODE = 0x01C2[7]	0.19	mA
I_{OUTMAX}	Maximum output current	Tested at DACCODE = 0xFFFF	23.95	mA
R_{OUT}	Output impedance		200	MΩ
	COMA to OUT voltage drop	I_{OUT} = 24 mA	960	mV

Figure 25. Specification for Loop Current Output

Next, examine what NAMUR NE43 has to say about loop current. NAMUR NE43 is an international association of process instrumentation user companies that have worked on improving the diagnostic coverage in 4- to 20-mA analog output transmitters to address associated safety issues. NAMUR NE43 provides the guideline for signaling-failure information to the safety-interlock systems over a 4- to 20-mA loop. NAMUR NE43 recommends using 3.8 mA to 20.5 mA as an extended measurement information range. NAMUR NE43 recommends using loop current below 3.6 mA or above 21 mA is in the diagnostic failure information range. Choose $I_{LOOP(MAX)}$ = 24 mA, depending upon DAC capability and also to comply with the NAMUR NE43 recommendation as shown in Figure 26.

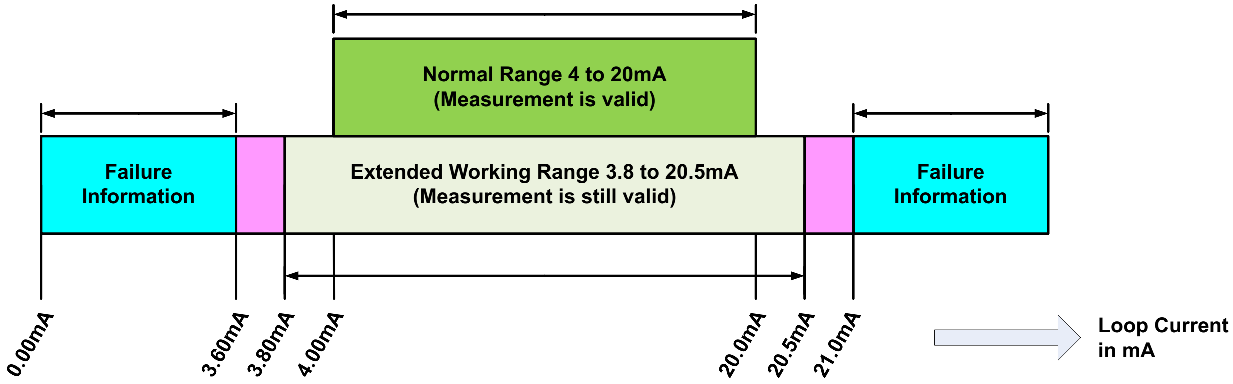


Figure 26. NAMUR NE43 Recommendation

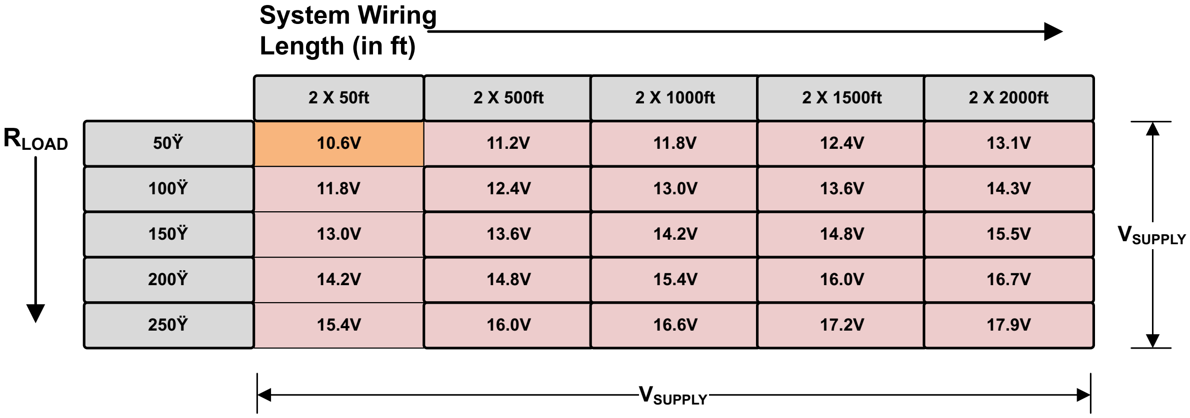
Typical Application (continued)

Rewriting Equation 20,

$$V_{SUPPLY(MIN)} > 0.2\text{ V} + (2 \text{ x } \rho \text{ x } L \text{ x } 24\text{ mA}) + (2 \text{ x } 0.7\text{ V}) + (100\ \Omega \text{ x } 24\text{ mA}) + 3.9\text{ V} + (20\ \Omega \text{ x } 24\text{ mA}) + (40\ \Omega \text{ x } 24\text{ mA}) + (R\ LOAD \text{ x } 24\text{ mA}) + (40\ \Omega \text{ x } 24\text{ mA}) + (R_{LOAD} \text{ x } 24\text{ mA}) \quad (21)$$

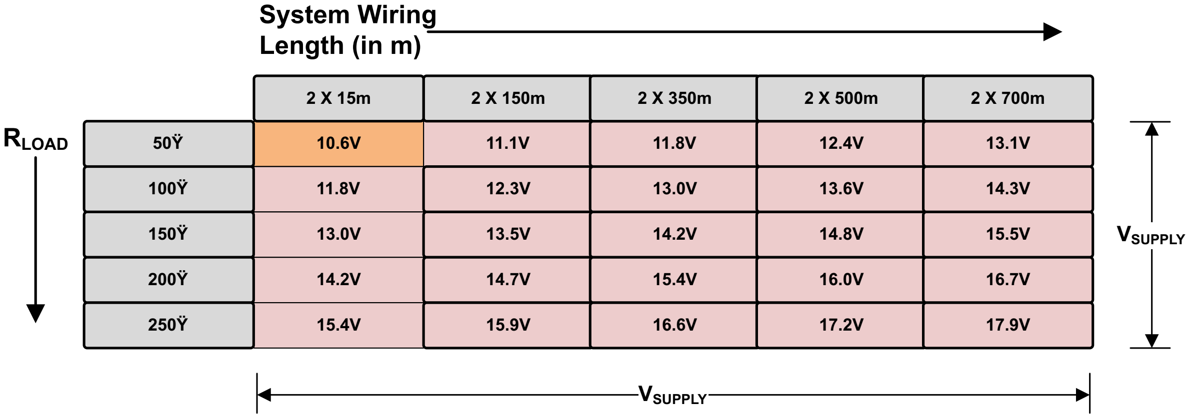
$$V_{SUPPLY(MIN)} > 2 \times 0.026\ \Omega\text{ /ft x } L \text{ x } 24\text{ mA}) + (R_{LOAD} \times 24\text{ mA}) + 9.34\text{ V} \quad (22)$$

Figure 27 and Figure 28 give the loop supply voltages calculated using Equation 22 at different receiver load resistances and system wiring lengths.



	2 X 50ft	2 X 500ft	2 X 1000ft	2 X 1500ft	2 X 2000ft
50Ω	10.6V	11.2V	11.8V	12.4V	13.1V
100Ω	11.8V	12.4V	13.0V	13.6V	14.3V
150Ω	13.0V	13.6V	14.2V	14.8V	15.5V
200Ω	14.2V	14.8V	15.4V	16.0V	16.7V
250Ω	15.4V	16.0V	16.6V	17.2V	17.9V

Figure 27. Loop Power Supply Voltage for Different Loads and System Wiring Length in Feet



	2 X 15m	2 X 150m	2 X 350m	2 X 500m	2 X 700m
50Ω	10.6V	11.1V	11.8V	12.4V	13.1V
100Ω	11.8V	12.3V	13.0V	13.6V	14.3V
150Ω	13.0V	13.5V	14.2V	14.8V	15.5V
200Ω	14.2V	14.7V	15.4V	16.0V	16.7V
250Ω	15.4V	15.9V	16.6V	17.2V	17.9V

Figure 28. Loop Power Supply Voltage for Different Loads and System Wiring Length in Meter

However, the maximum loop compliance voltage must not exceed the absolute maximum voltage rating of any device used in the loop. Therefore, select the device in order to meet the maximum loop compliance voltage requirement

9.2.2.3 Selection of External BJT

DAC161S997 has been designed to use an external NPN transistor (BJT). Transistor Q1 conducts the majority of the signal-dependent, 4-20mA loop current. Using an external transistor avoids on-chip power dissipation and thermally-induced errors. Since the external transistor is part of a current control loop, the external transistor characteristics are not critical. Virtually any transistor with sufficient voltage, current and, power rating may be used. Basic requirements are as follows:

- V_{CEO} = 40 V minimum
- β = 40 minimum
- Must be able to handle power dissipation, $P_D = V_{CE(MAX)} \times I_{LOOP(MAX)}$

Typical Application (continued)

The NPN BJT should not be replaced with an N-channel Field Effect Transistor (FET) for the following reasons. Discrete FET ’ s typically have high threshold voltages (V_{TH}), in the order of 1.5 V to 2 V, which is beyond the BASE output maximum range. Discrete FETs present higher load capacitance, which may degrade system stability margins. BASE output relies on the BJT’s base current for biasing.

For further information on a complete reference design of a Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter, refer to TIDU385A.

9.2.3 Application Curve

Unless otherwise noted, these specifications apply for VA = VD = 3.3 V, COMA = COMD = 0 V, T_A= 25°C, external bipolar transistor: 2N3904, RE = 22 Ω, C1 = C2 = C3 = 2.2 nF.

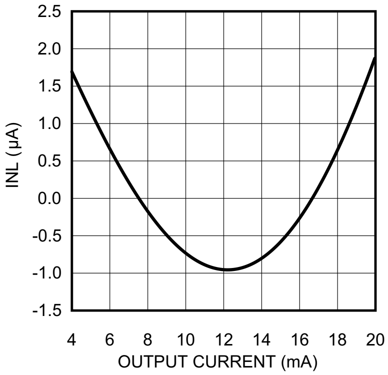


Figure 29. Linearity vs ILOOP

10 Power Supply Recommendations

The DAC161S997 requires a voltage supply within 2.7 V and 3.6 V. Multilayer ceramic bypass X7R capacitors of 0.1µF between the VA and GND pins, and between the VD and GND pins are recommended. If the supply is located more than a few inches from the DAC161S997, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10µF or 22µF is a typical choice

11 Layout

11.1 Layout Guidelines

To maximize the performance of the DAC161S997 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DAC161S997 are:

- Make sure that VD and VA have decoupling capacitors local to the respective terminals.
- Minimize trace length between the C1, C2, and C3 capacitors and the DAC161S997 pins.

11.2 Layout Example

Figure 30 to Figure 32 show the DAC161S997 evaluation module (EVM) layout

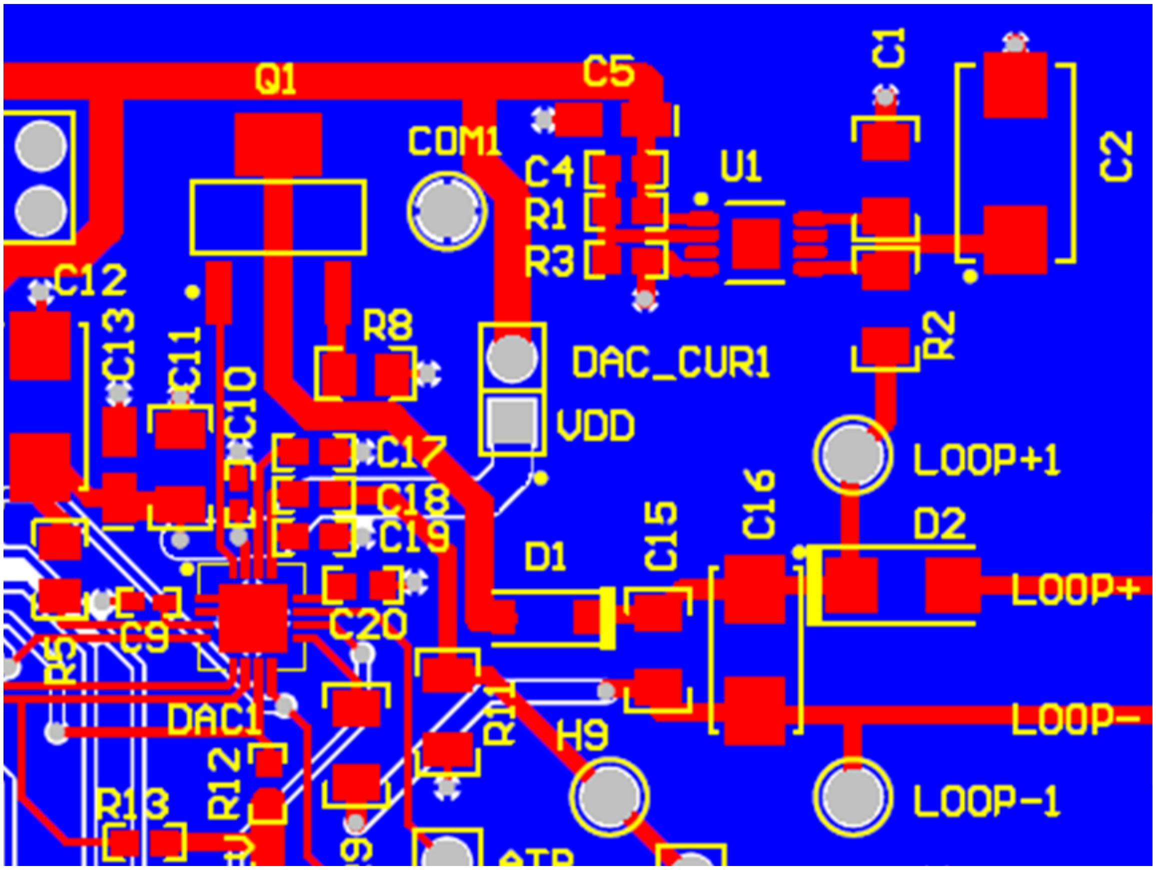


Figure 30. Example PCB layout: Top Assembly Layer

Layout Example (continued)

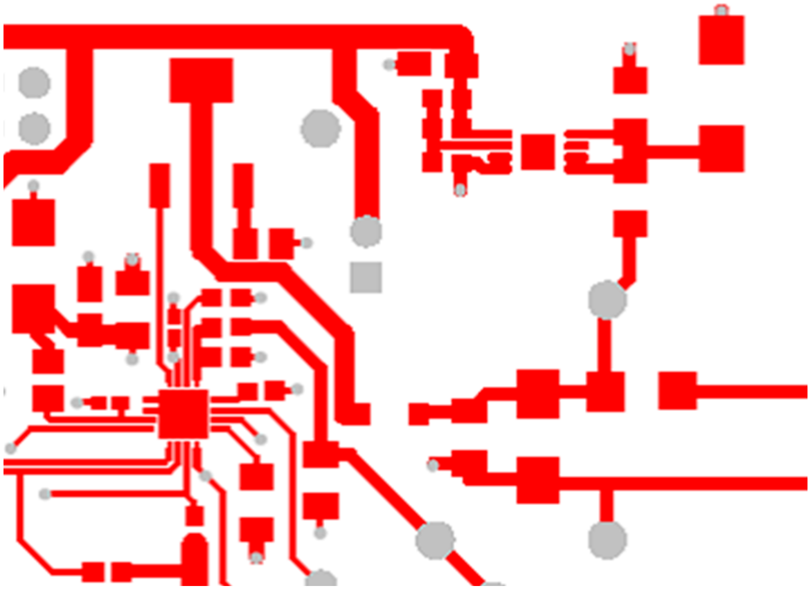


Figure 31. Example PCB layout: Top Layer

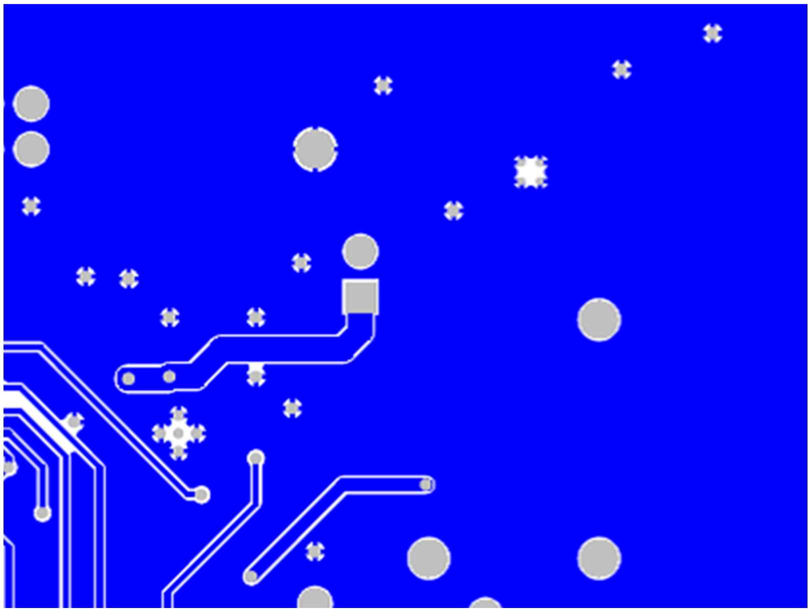


Figure 32. Example PCB layout: Bottom Layer

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC161S997RGHR	ACTIVE	WQFN	RGH	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	161S997	Samples
DAC161S997RGHT	ACTIVE	WQFN	RGH	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	161S997	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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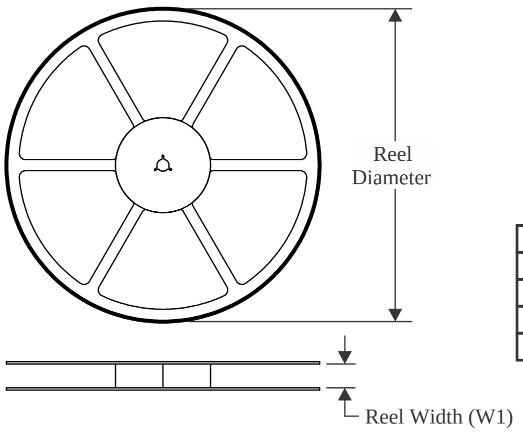
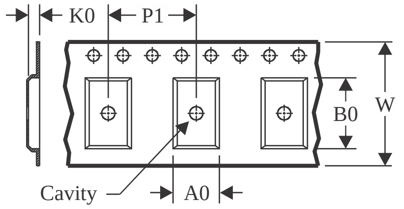
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

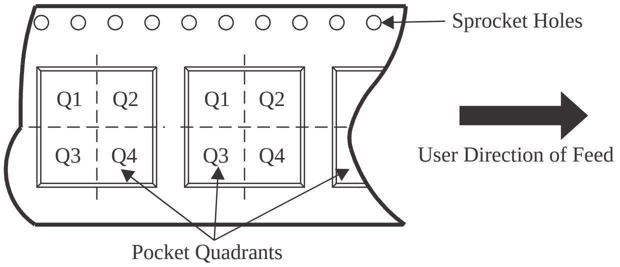


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

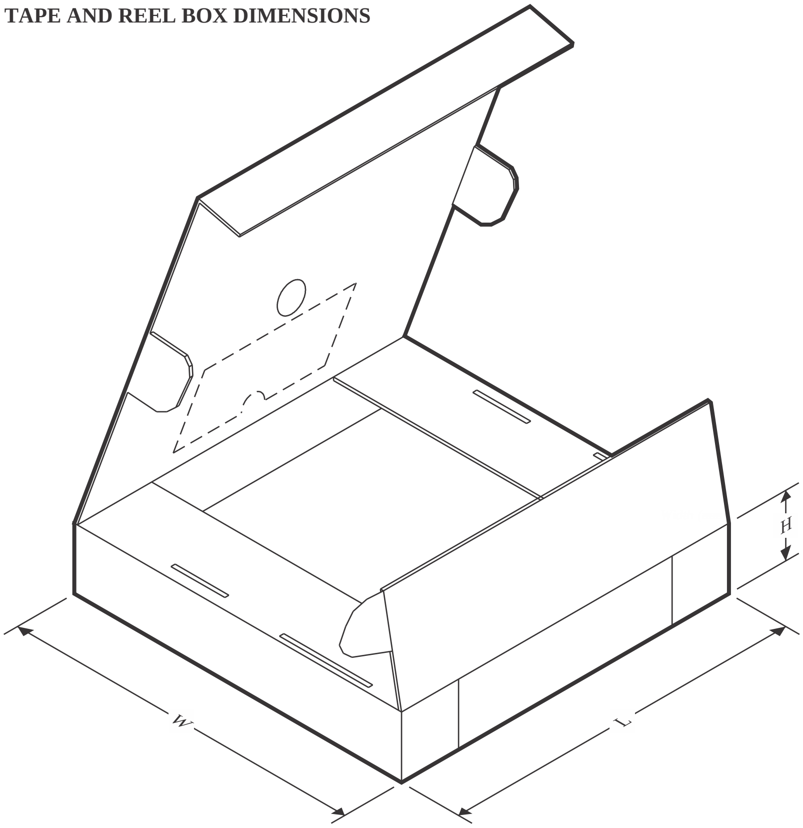
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC161S997RGHR	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DAC161S997RGHT	WQFN	RGH	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

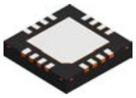
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC161S997RGHR	WQFN	RGH	16	4500	356.0	356.0	35.0
DAC161S997RGHT	WQFN	RGH	16	250	367.0	367.0	35.0

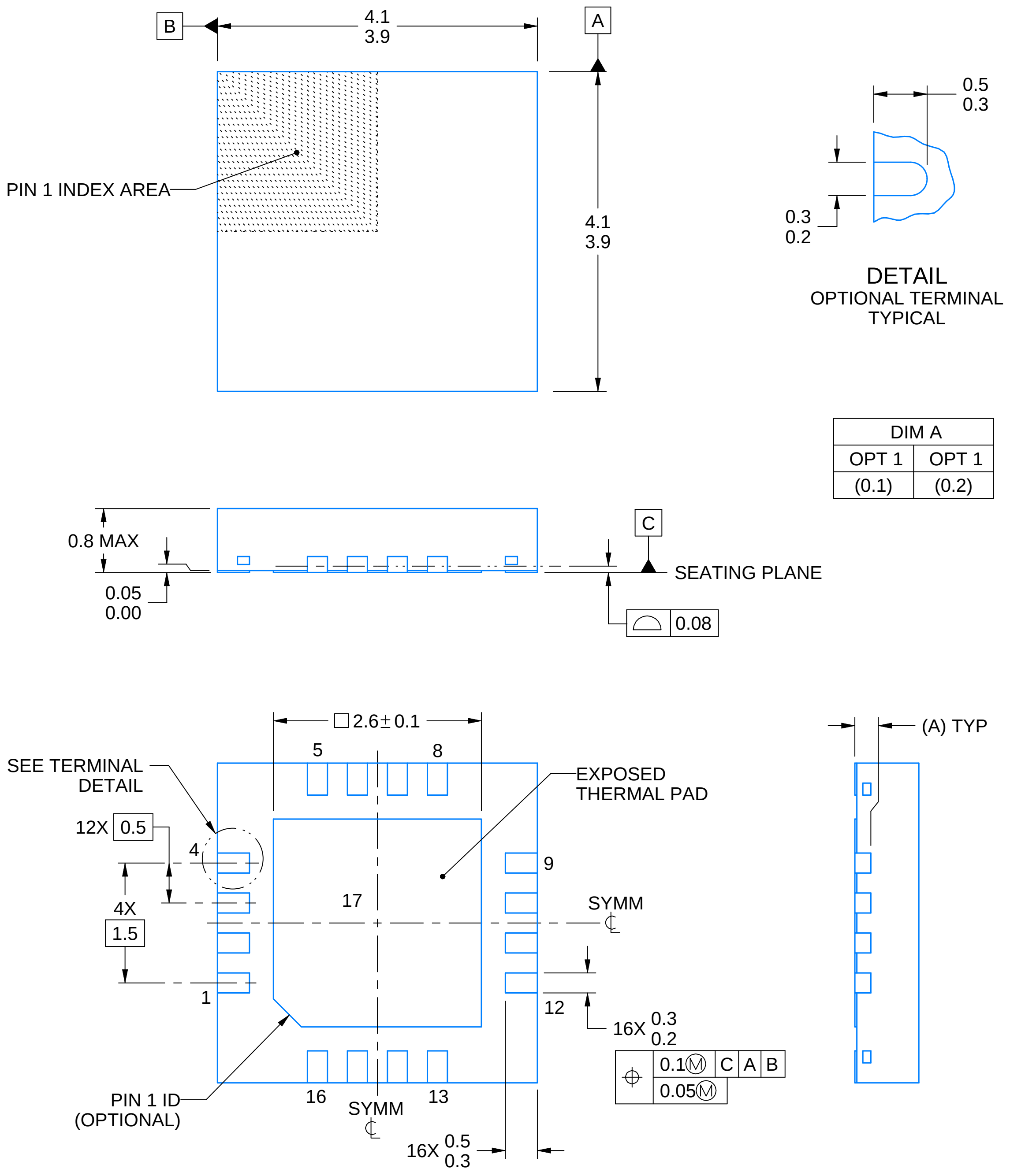
PACKAGE OUTLINE



RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

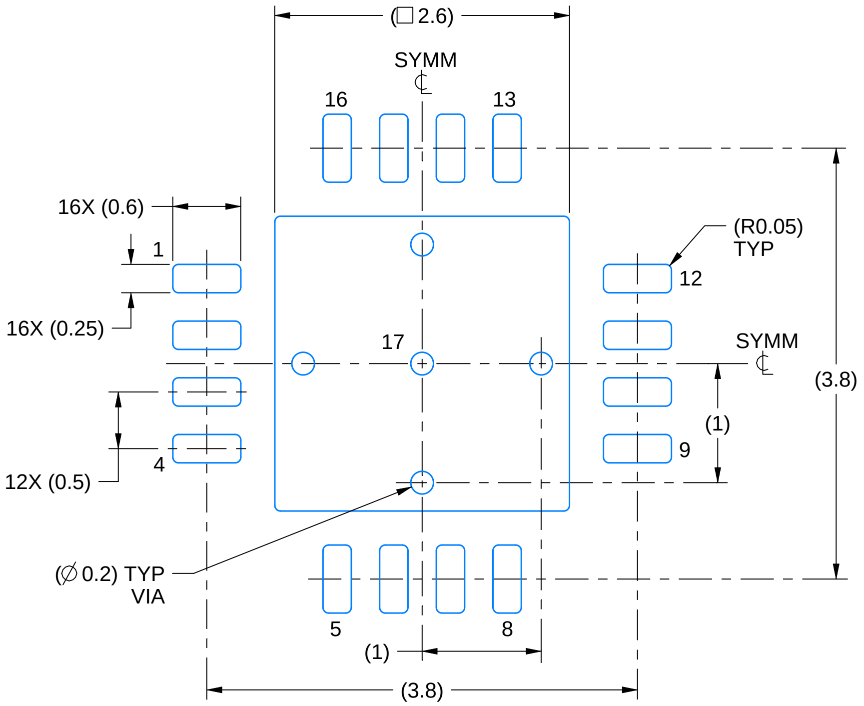


DIM A	
OPT 1	OPT 1
(0.1)	(0.2)

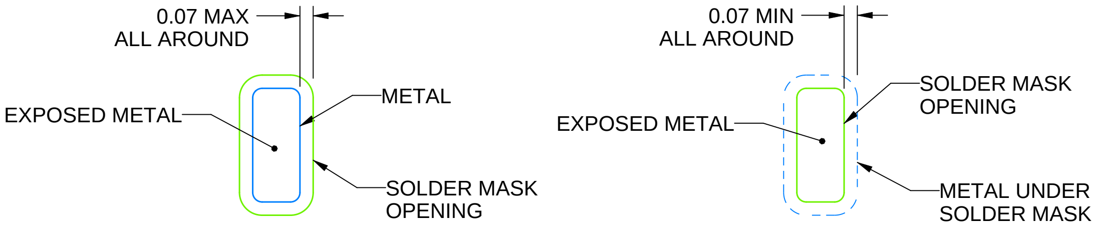
4214978/B 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



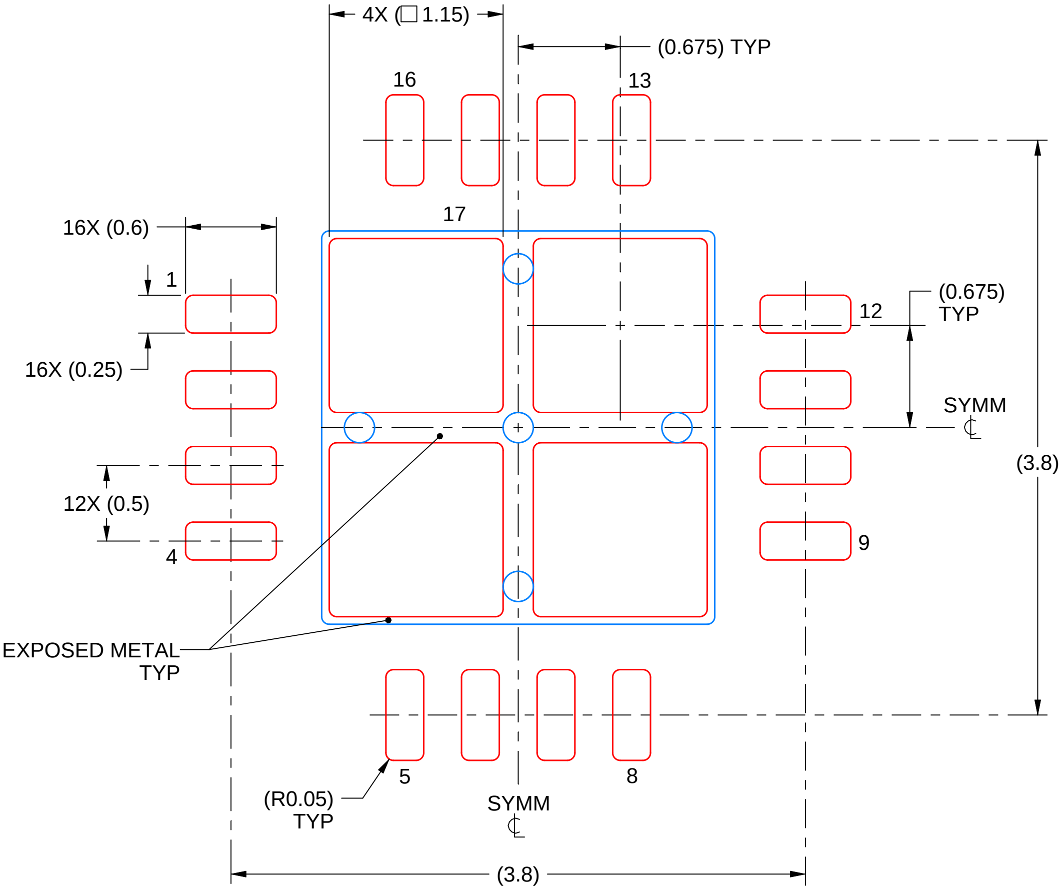
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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