# TPS6128xD Low-IQ, Wide-Voltage Battery Front-End DC/DC Converter for Single-Cell Li-Ion, Ni-Rich, Si-Anode Applications

## 1 Features

- 95% Efficiency at 2.3 MHz Operation
- 3-µA Quiescent Current in Low $I_Q$ Pass-Through Mode
- Wide $V_{IN}$ Range From 2.3 V To 4.8 V
- $I_{OUT}$ ≥ 4A (Peak) at $V_{OUT}$ = 3.35 V, $V_{IN}$ ≥ 2.65 V
- Integrated Pass-Through Mode (35 mΩ)
- Programmable Valley Inductor Current Limit and Output Voltage
- True Pass-Through Mode During Shutdown
- *Best-in-Class* Line and Load Transient
- Low-Ripple Light-Load PFM Mode
- In-Situ Customization with On-Chip $E^2$PROM (Write Protection)
- Two Interface Options:
  - $I^2C$ Compatible I/F up to 3.4 Mbps (TPS61280D)
  - Simple I/O Logic Control Interface
- Thermal Shutdown and Overload Protection
- Total Solution Size < 20 $mm^2$, Sub 1-mm Profile

## 2 Applications

- Single-Cell Ni-Rich, Si-Anode, Li-Ion, LiFePO4 Smart-Phones or Tablet PCs
- 2.5G, 3G, 4G Mini-Module Data Cards
- Current Limited Applications Featuring High Peak Power Loads

## 3 Description

The TPS6128xD device provides a power supply solution for products powered by either by a Li-Ion, Nickel-Rich, Silicon Anode, Li-Ion or LiFePO4 battery. The voltage range is optimized for single-cell portable applications like in smart-phones or tablet PCs.

Used as a high-power pre-regulator, the TPS6128xD extends the battery run-time and overcomes input current- and voltage limitations of the powered system.

While in shutdown, the TPS6128xD operates in a true pass-through mode with only 3-µA quiescent consumption for longest battery shelf life.

During operation, when the battery is at a good state-of-charge, a low-ohmic, high-efficient integrated pass-through path connects the battery to the powered system.

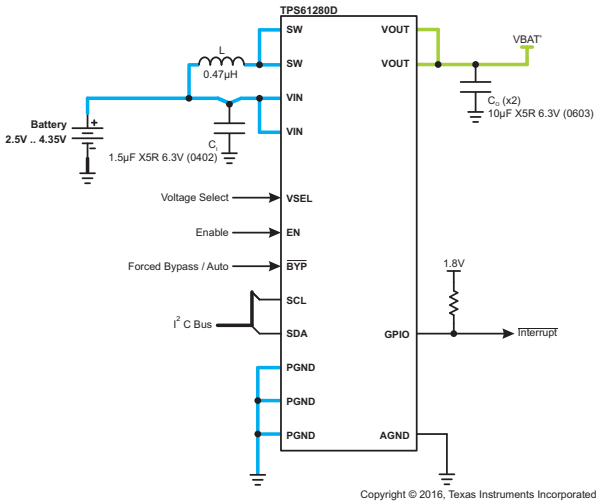
If the battery gets to a lower state of charge and its voltage becomes lower than the desired minimum system voltage, the device seamlessly transits into boost mode to uses the full battery capacity.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS61280D | DSBGA (16) | 1.66 mm x 1.66 mm |
| TPS61281D | | |
| TPS61282D | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**



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## 4 Revision History

**Changes from Original (January 2018) to Revision A** **Page**

- Changed devices TPS61281D and TPS61282D From: *Product Preview* To: *Production* data ... 1
- Changed the TPS61280D pin configuration ... 4
- Changed the TPS6128xD pin configuration ... 5

## 5 Description (continued)

TPS6128xD device supports more than 4 A pulsed load current even from a deeply discharged battery. In this mode of operation, the TPS6128xD enables the use of the full battery capacity: A high battery-cut-off voltage originated by powered components with a high minimum input voltage is overcome; new battery chemistries can be fully discharged; high current pulses forcing the system into shutdown are buffered by the device seamlessly transitioning between boost and by-pass mode back and forth.

This has significant impact on the battery on-time and translates into either a longer use-time and better user-experience at an equal battery capacity or into reduced battery costs at similar use-times.

The TPS6128xD offers a small solution size (< 20 $mm^2$) due to minimum amount of external components, enabling the use of small inductors and input capacitors, available as a 16-pin chip-scale package (CSP).

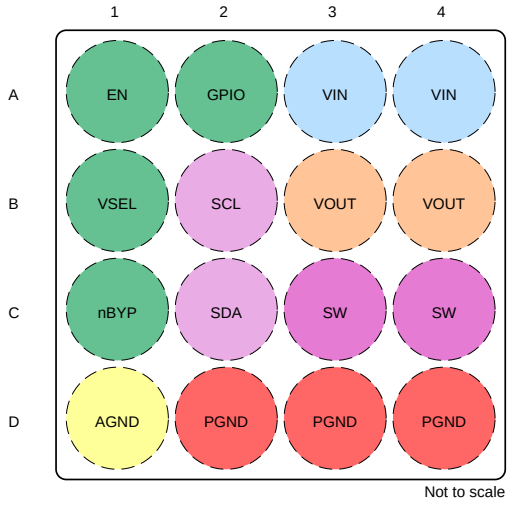
The TPS6128xD operates in synchronous, 2.3 MHz boost mode and enters power-save mode operation (PFM) at light load currents to maintain high efficiency over the entire load current range.

## 6 Device Comparison Table

| PART NUMBER | DEVICE SPECIFIC FEATURES | |
|---|---|---|
| TPS61280D | $I^2C$ Control Interface<br>User Prog. $E^2PROM$ Settings | DC/DC boost / bypass threshold = 3.15 V (VSEL = L) |
| | | DC/DC boost / bypass threshold = 3.35 V (VSEL = H) |
| | | Valley inductor current limit = 3 A |
| TPS61281D | Simple Logic Control Interface | DC/DC boost / bypass threshold = 3.15 V (VSEL = L) |
| | | DC/DC boost / bypass threshold = 3.35 V (VSEL = H) |
| | | Valley inductor current limit = 3 A |
| TPS61282D | Simple Logic Control Interface | DC/DC boost / bypass threshold = 3.3 V (VSEL = L) |
| | | DC/DC boost / bypass threshold = 3.5 V (VSEL = H) |
| | | Valley inductor current limit = 4 A |

# 7 Pin Configuration and Functions

**TPS61280D YFF Package**
**16-Bump DSBGA**
**Top View**

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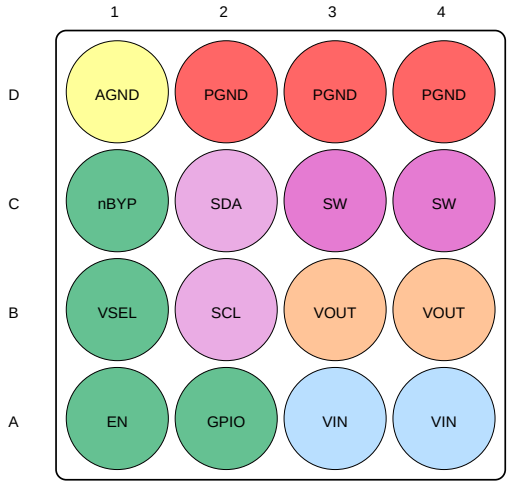
**TPS61280D YFF Package**
**16-Bump DSBGA**
**Bottom View**

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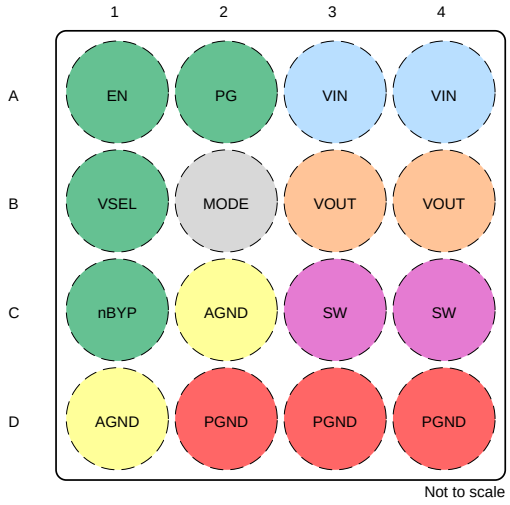
**Pin Functions, TPS61280D**

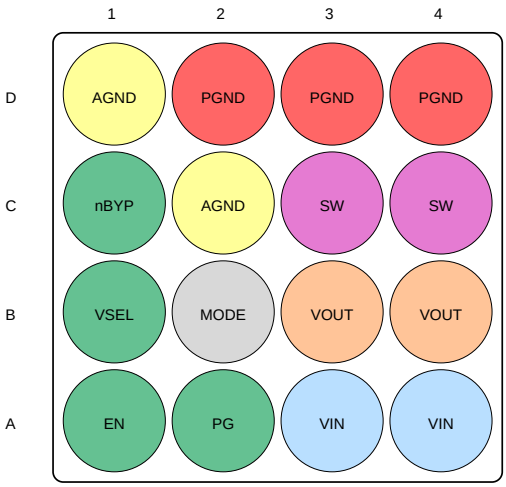
| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VIN | A3, A4 | I | Power supply input. |
| VOUT | B3, B4 | O | Boost converter output. |
| EN | A1 | I | This is the enable pin of the device. On the rising edge of the enable pin, all the registers are reset with their default values. This input must not be left floating and must be terminated.<br>EN = Low: The device is forced into shutdown mode and the I2C control interface is disabled. Depending on the logic level applied to the nBYP input, the converter can either be forced in pass-through mode or it's output can be regulated to a minimum level so as to limit the input-to-output voltage difference to less than 3.6V (typ). The current consumption is reduced to a few µA. For more details, refer to Table 2.<br>EN = High: The device is operating normally featuring automatic dc/dc boost, pass-through mode transition. For more details, refer to Table 2. |
| GPIO | A2 | I/O | This pin can either be configured as a input (mode selection) or as dual role input/open-drain output ($\overline{RST}$/$\overline{FAULT}$ ) pin. Per default, the pin is configured as $\overline{RST}$/$\overline{FAULT}$ input/output. The input must not be left floating and must be terminated.<br>Manual Reset Input: Drive $\overline{RST}$/$\overline{FAULT}$ low to initiate a reset of the converter's output. nRST/nFAULT controls a falling edge-triggered sequence consisting of a discharge phase of the capacitance located at the converter's output followed by a start-up phase.<br>Fault Output (open-drain interrupt signal to host): Indicates that a fault has occurred (e.g. thermal shutdown, output voltage out of limits, current limit triggered, and so on). To signal such an event, the device generates a falling edge-triggered interrupt by driving a negative pulse onto the GPIO line and then releases the line to its inactive state.<br>Mode selection input = Low: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents.<br>Mode selection input = High: Low-noise mode enabled, regulated frequency PWM operation forced. |
| VSEL | B1 | I | VSEL signal is primarily used to set the output voltage dc/dc boost, pass-through threshold. This pin must not be left floating and must be terminated. |
| nBYP | C1 | I | A logic low level on the $\overline{BYP}$ input forces the device in pass-through mode. This pin must not be left floating and must be terminated. |
| SCL | B2 | I | Serial interface clock line. This pin must not be left floating and must be terminated. |
| SDA | C2 | I/O | Serial interface address/data line. This pin must not be left floating and must be terminated. |
| SW | C3, C4 | I/O | Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. |
| PGND | D2, D3, D4 | | Power ground pin. |
| AGND | D1 | | Analog ground pin. This is the signal ground reference for the IC. |

**TPS6128xD YFF Package**
**16-Bump DSBGA**
**Top View**




Not to scale

**TPS6128xD YFF Package**
**16-Bump DSBGA**
**Bottom View**




Not to scale

## Pin Functions, TPS6128xD

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VIN | A3, A4 | I | Power supply input. |
| VOUT | B3, B4 | O | Boost converter output. |
| EN | A1 | I | This is the enable pin of the device. On the rising edge of the enable pin, all the registers are reset with their default values. This input must not be left floating and must be terminated.<br>EN = Low: The device is forced into shutdown mode. Depending on the logic level applied to the nBYP input, the converter can either be forced in pass-through mode or it's output can be regulated to a minimum level so as to limit the input-to-output voltage difference to less than 3.6V (typ). The current consumption is reduced to a few µA. For more details, refer to Table 2.<br>EN = High: The device is operating normally featuring automatic dc/dc boost, pass-through mode transition. For more details, refer to Table 2. |
| PG | A2 | O | Power-Good Output (open-drain output to host): A logic high on the PG output indicates that the converter's output voltage is within its regulation limits. A logic low indicates a fault has occurred (e.g. thermal shutdown, output voltage out of limits, current limit triggered, and so on). The PG signal is de-asserted automatically once the IC resumes proper operation. |
| VSEL | B1 | I | VSEL signal is primarily used to set the output voltage dc/dc boost, pass-through threshold. This pin must not be left floating and must be terminated. |
| nBYP | C1 | I | A logic low level on the $\overline{BYP}$ input forces the device in pass-through mode. For more details, refer to Table 2. This pin must not be left floating and must be terminated. |
| MODE | B2 | I | This is the mode selection pin of the device. This pin must not be left floating, must be terminated and can be connected to AGND. During start-up this pin must be held low. Once the output voltage settled and PG pin indicates that the converter's output voltage is within its regulation limits the device can be forced in PWM mode operation by applying a high level on this pin.<br>MODE = Low: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. This pin must be held low during device start-up.<br>MODE = High: Low-noise mode enabled, regulated frequency PWM operation forced. |
| SW | C3, C4 | I/O | Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. |
| PGND | D2, D3, D4 | | Power ground pin. |
| AGND | C2, D1 | | Analog ground pin. This is the signal ground reference for the IC. |

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | Voltage at VOUT(2) | DC | –0.3 | 4.7 | V |
| | Voltage at VIN(2), EN(2), VSEL(2), $\overline{BYP}$(2), PG(2), GPIO(2) | DC | –0.3 | 5.2 | V |
| | Voltage at SCL(2), SDA(2)MODE(2) | DC | –0.3 | 3.6 | V |
| | Voltage at SW(2) | DC | –0.3 | 4.7 | V |
| | | Transient: 2 ns, 2.3 MHz | –0.3 | 5.5 | V |
| | Differential voltage between VIN and VOUT | DC | –0.3 | 4 | V |
| Input current | Continuous average current into SW (3) | | | 1.8 | A |
| | Peak current into SW (4) | | | 5.5 | A |
| Power dissipation | | | Internally limited | | |
| Temperature range | Operating temperature range, $T_A$ (5) | | –40 | 85 | °C |
| | Operating virtual junction, $T_J$ | | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Limit the junction temperature to 105°C for continuous operation at maximum output power.
(4) Limit the junction temperature to 105°C for 15% duty cycle operation.
(5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | V |
| | | Machine Model - (MM) | ±200 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | 2.30 | | 4.85 | V |
| | Input voltage range for in-situ customization by $E^2$PROM write operation | 3.4 | 3.5 | 3.6 | V |
| L | Inductance | 200 | 470 | 800 | nH |
| $C_O$ | Output capacitance | 9 | 13 | 100 | µF |
| $I_L$ | Maximum load current during start-up | 250 | | | mA |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 8.4 Thermal Information

| THERMAL METRIC(1) | | TPS6128xD YFF (DSBGA) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 78 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance | 0.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13 | °C/W |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 8.5 Electrical Characteristics

Minimum and maximum values are at $V_{IN}$ = 2.3 V to 4.85 V, $V_{OUT}$ = 3.4 V (or $V_{IN}$, whichever is higher), EN = 1.8 V, VSEL = 1.8 V, nBYP = 1.8 V, –40°C ≤ $T_J$ ≤ 125°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at $V_{IN}$ = 3.2 V, $V_{OUT}$ = 3.4 V, EN = 1.8 V, $T_J$ = 25°C (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_Q$ | Operating quiescent current into $V_{IN}$ | TPS6128xD | DC/DC boost mode. Device not switching<br>$I_{OUT}$ = 0 mA, $V_{IN}$ = 3.2 V, $V_{OUT}$ = 3.4 V | –40°C ≤ $T_J$ ≤ 85°C | | 47.4 | 65.6 | µA |
| | | | Pass-through mode (auto)<br>EN = 1.8 V, $\overline{BYP}$ = 1.8 V, $V_{IN}$ = 3.6 V | | | 27.4 | 42.6 | µA |
| | | | Pass-through mode (forced)<br>EN = 1.8 V, $\overline{BYP}$ = AGND, $V_{OUT}$ = 3.6 V | | | 15.4 | 25.6 | µA |
| | Operating quiescent current into $V_{OUT}$ | | DC/DC boost mode. Device not switching<br>$I_{OUT}$ = 0 mA, $V_{IN}$ = 3.2 V, $V_{OUT}$ = 3.4 V | | | 8.9 | 19.6 | µA |
| $I_{SD}$ | Shutdown current | TPS6128xD | EN = 0 V, $\overline{BYP}$ = 0 V, $V_{IN}$ = 3.6 V | | | 3 | 6.6 | µA |
| | | | EN = 0 V, $\overline{BYP}$ = 1.8 V, $V_{IN}$ = 3.6 V | | | 8.9 | 20.6 | µA |
| $V_{UVLO}$ | Under-voltage lockout threshold | TPS6128xD | Falling | | | 2 | 2.1 | V |
| | | | Hysteresis | | | 0.1 | | V |
| **EN, VSEL, nBYP, MODE, SDA, SCL, GPIO, PG** | | | | | | | | |
| $V_{IL}$ | Low-level input voltage | TPS6128xD | | | | | 0.4 | V |
| $V_{IH}$ | High-level input voltage | | | | 1.2 | | | V |
| $V_{OL}$ | Low-level output voltage (SDA) | TPS61280D | $I_{OL}$ = 8 mA | | | | 0.3 | V |
| | Low-level output voltage (GPIO) | | $I_{OL}$ = 8 mA, GPIOCFG = 0 | | | | 0.3 | V |
| | Low-level output voltage (PG) | TPS6128xD | $I_{OL}$ = 8 mA | | | | 0.3 | V |
| $R_{PD}$ | EN, VSEL, $\overline{BYP}$, pull-down resistance | TPS6128xD | Input ≤ 0.4 V | | | 300 | | kΩ |
| $C_{IN}$ | EN, VSEL, $\overline{BYP}$, MODE, PG input capacitance | TPS6128xD | Input connected to AGND or $V_{IN}$ | | | 9 | | pF |
| | SDA, SCL, GPIO input capacitance | TPS61280D | | | | 9 | | pF |
| $V_{THPG}$ | Power good threshold | TPS6128xD | Rising $V_{OUT}$ | | 0.95 x $V_{OUT}$ | | | |
| | | | Falling $V_{OUT}$ | | 0.9 x $V_{OUT}$ | | | |
| $I_{lkg}$ | Input leakage current | TPS6128xD | Input connected to AGND | –40°C ≤ $T_J$ ≤ 85°C | | 0 | | µA |
| | | | Input connected $V_{IN}$ | | | | 0.5 | µA |
| **OUTPUT** | | | | | | | | |
| $V_{OUT(TH)}$ | Threshold DC voltage accuracy | TPS6128xD | No load. Open loop | | -1.5% | | 1.5% | |
| $V_{OUT}$ | Regulated DC voltage accuracy | TPS6128xD | 2.65 V ≤ $V_{IN}$ ≤ $V_{OUT\_TH}$ - 150 mV<br>$I_{OUT}$ = 0mA<br>PWM operation. | | -2% | | 2% | |
| | | | 2.65 V ≤ $V_{IN}$ ≤ $V_{OUT\_TH}$ - 150 mV<br>$I_{OUT}$ = 0 mA<br>PFM/PWM operation | | -2% | | 4% | |

## Electrical Characteristics (continued)

Minimum and maximum values are at $V_{IN}$ = 2.3 V to 4.85 V, $V_{OUT}$ = 3.4 V (or $V_{IN}$, whichever is higher), EN = 1.8 V, VSEL = 1.8 V, nBYP = 1.8 V, –40°C ≤ $T_J$ ≤ 125°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at $V_{IN}$ = 3.2 V, $V_{OUT}$ = 3.4 V, EN = 1.8 V, $T_J$ = 25°C (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Power-save mode output ripple voltage | TPS6128xD | PFM operation, $I_{OUT}$ = 1 mA | | 30 | | mVpk |
| | PWM mode output ripple voltage | | PWM operation, $I_{OUT}$ = 500 mA | | 15 | | mVpk |
| **POWER SWITCH** | | | | | | | |
| $r_{DS(on)}$ | Low-side switch MOSFET on resistance | TPS6128xD | $V_{IN}$ = 3.2 V, $V_{OUT}$ = 3.5 V | | 45 | 80 | mΩ |
| | High-side rectifier MOSFET on resistance | | $V_{IN}$ = 3.2 V, $V_{OUT}$ = 3.5 V | | 40 | 70 | mΩ |
| | High-side pass-through MOSFET on resistance | | $V_{IN}$ = 3.2 V | | 35 | 60 | mΩ |
| $I_{lkg}$ | Reverse leakage current into SW | TPS6128xD | EN = AGND, $V_{IN}$ = $V_{OUT}$ = SW = 3.5 V –40°C ≤ $T_J$ ≤ 85°C | | 0.1 | 2 | µA |
| | Reverse leakage current into VOUT | | EN = $\overline{BYP}$ = $V_{IN}$, $V_{IN}$ = 2.9 V, $V_{OUT}$ = 4.4 V, $V_{SW}$ = 0 V device not switching –40°C ≤ $T_J$ ≤ 85°C | | 0.11 | 2 | µA |
| $I_{SINK}$ | VOUT sink capability | TPS6128xD | EN = AGND, $V_{OUT}$ ≤ 3.6 V,$I_{OUT}$ = -10 mA | | | 0.3 | V |
| | Valley inductor current limit | TPS61280D TPS61281D | $V_{IN}$ = 2.9 V, $V_{OUT}$ = 3.5 V, –40°C ≤ $T_J$ ≤ 125°C, auto PFM/PWM | 2475 | 3000 | 3525 | mA |
| | Valley inductor current limit | TPS61282D | $V_{IN}$ = 2.9 V, $V_{OUT}$ = 3.5 V, –40°C ≤ $T_J$ ≤ 125°C, auto PFM/PWM | 3300 | 4000 | 4700 | mA |
| | Pass through mode current limit | TPS6128xD | EN = $\overline{BYP}$ = GND, $V_{IN}$ = 3.2 V | | 5000 | | mA |
| | | | EN = $V_{IN}$, $\overline{BYP}$ = don't care , $V_{IN}$ = 3.2 V | 5600 | 7400 | 9100 | mA |
| | Pre-charge mode current limit (linear mode, phase 1) | TPS6128xD | $V_{IN}$ - $V_{OUT}$ >= 300 mV | 500 | 650 | | mA |
| | Pre-charge mode current limit (linear mode, phase 2) | | | | 2000 | | mA |
| **OSCILLATOR** | | | | | | | |
| $f_{OSC}$ | Oscillator frequency | TPS6128xD | $V_{IN}$ = 2.7 V, $V_{OUT}$ = 3.5 V | | 2.3 | | MHz |
| **THERMAL SHUTDOWN, HOT DIE DETECTOR** | | | | | | | |
| | Thermal shutdown(1) | TPS6128xD | | 140 | 160 | | °C |
| | Hot die detector accuracy(1) | TPS61280D | | -10 | 105 | 10 | °C |
| **TIMING** | | | | | | | |
| | Start-up time | TPS6128xD | $V_{IN}$ = 3.2 V, VOUT_TH = 01011 (3.4 V), $R_{LOAD}$ = 50 Ω Time from active $V_{IN}$ to $V_{OUT}$ settled | | 500 | | µs |
| | GPIO rise time(1) | TPS61280D | | | | 200 | ns |

(1) Specified by characterization. Not tested in production.

## 8.6 I²C Interface Timing Characteristics(1)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(SCL)}$ | SCL Clock Frequency | Standard mode | | 100 | kHz |
| | | Fast mode | | 400 | kHz |
| | | Fast mode plus | | 1 | MHz |
| | | High-speed mode (write operation), $C_B$ – 100 pF max | | 3.4 | MHz |
| | | High-speed mode (read operation), $C_B$ – 100 pF max | | 3.4 | MHz |
| | | High-speed mode (write operation), $C_B$ – 400 pF max | | 1.7 | MHz |
| | | High-speed mode (read operation), $C_B$ – 400 pF max | | 1.7 | MHz |
| $t_{BUF}$ | Bus Free Time Between a STOP and START Condition | Standard mode | 4.7 | | µs |
| | | Fast mode | 1.3 | | µs |
| | | Fast mode plus | 0.5 | | µs |
| $t_{HD}$, $t_{STA}$ | Hold Time (Repeated) START Condition | Standard mode | 4 | | µs |
| | | Fast mode | 600 | | ns |
| | | Fast mode plus | 260 | | ns |
| | | High-speed mode | 160 | | ns |
| $t_{LOW}$ | LOW Period of the SCL Clock | Standard mode | 4.7 | | µs |
| | | Fast mode | 1.3 | | µs |
| | | Fast mode plus | 0.5 | | µs |
| | | High-speed mode, $C_B$ – 100 pF max | 160 | | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 320 | | ns |
| $t_{HIGH}$ | HIGH Period of the SCL Clock | Standard mode | 4 | | µs |
| | | Fast mode | 600 | | ns |
| | | Fast mode plus | 260 | | ns |
| | | High-speed mode, $C_B$ – 100 pF max | 60 | | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 120 | | ns |
| $t_{SU}$, $t_{STA}$ | Setup Time for a Repeated START Condition | Standard mode | 4.7 | | µs |
| | | Fast mode | 600 | | ns |
| | | Fast mode plus | 260 | | ns |
| | | High-speed mode | 160 | | ns |
| $t_{SU}$, $t_{DAT}$ | Data Setup Time | Standard mode | 250 | | ns |
| | | Fast mode | 100 | | ns |
| | | Fast mode plus | 50 | | ns |
| | | High-speed mode | 10 | | ns |
| $t_{HD}$, $t_{DAT}$ | Data Hold Time | Standard mode | 0 | 3.45 | µs |
| | | Fast mode | 0 | 0.9 | µs |
| | | Fast mode plus | 0 | | µs |
| | | High-speed mode, $C_B$ – 100 pF max | 0 | 70 | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 0 | 150 | ns |
| $t_{RCL}$ | Rise Time of SCL Signal | Standard mode | | 1000 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | 300 | ns |
| | | Fast mode plus | | 120 | ns |
| | | High-speed mode, $C_B$ – 100 pF max | 10 | 40 | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 20 | 80 | ns |
| $t_{RCL1}$ | Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT | Standard mode | 20 + 0.1 $C_B$ | 1000 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | 300 | ns |
| | | Fast mode plus | | 120 | ns |
| | | High-speed mode, $C_B$ – 100 pF max | 10 | 80 | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 20 | 160 | ns |

(1) Specified by design. Not tested in production.

## I²C Interface Timing Characteristics(1) (continued)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{FCL}$ | Fall Time of SCL Signal | Standard mode | 20 + 0.1 $C_B$ | 300 | ns |
| | | Fast mode | | 300 | ns |
| | | Fast mode plus | | 120 | ns |
| | | High-speed mode, $C_B$ – 100 pF max | 10 | 40 | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 20 | 80 | ns |
| $t_{RDA}$ | Rise Time of SDA Signal | Standard mode | | 1000 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | 300 | ns |
| | | Fast mode plus | | 120 | ns |
| | | High-speed mode, $C_B$ – 100 pF max | 10 | 80 | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 20 | 160 | ns |
| $t_{FDA}$ | Fall Time of SDA Signal | Standard mode | | 300 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | 300 | ns |
| | | Fast mode plus | | 120 | ns |
| | | High-speed mode, $C_B$ – 100 pF max | 10 | 80 | ns |
| | | High-speed mode, $C_B$ – 400 pF max | 20 | 160 | ns |
| $t_{SU,}$ $t_{STO}$ | Setup Time of STOP Condition | Standard mode | 4 | | µs |
| | | Fast mode | 600 | | ns |
| | | Fast mode plus | 260 | | ns |
| | | High-Speed mode | 160 | | ns |
| $C_B$ | Capacitive Load for SDA and SCL | Standard mode | | 400 | pF |
| | | Fast mode | | 400 | pF |
| | | Fast mode plus | | 550 | pF |
| | | High-Speed mode | | 400 | pF |

## 8.7 I²C Timing Diagrams

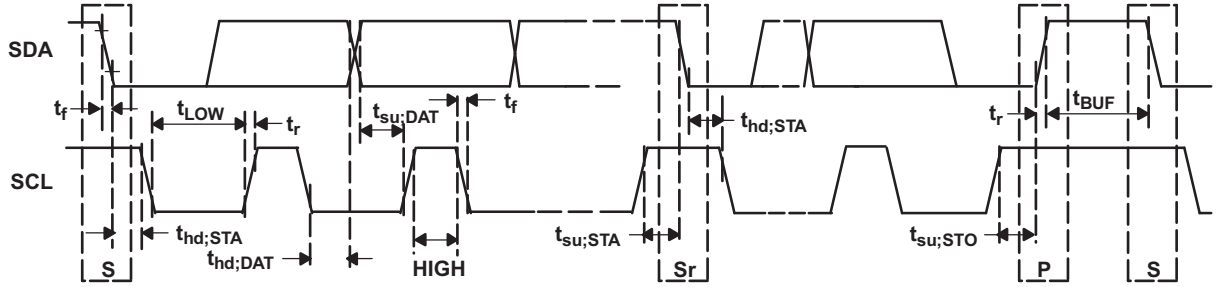
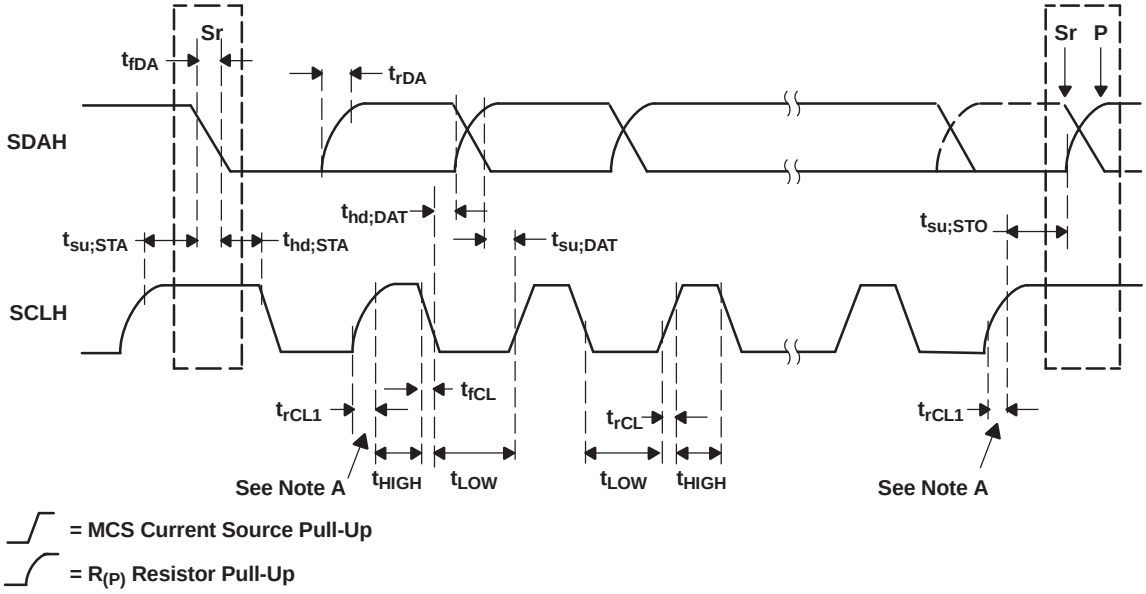


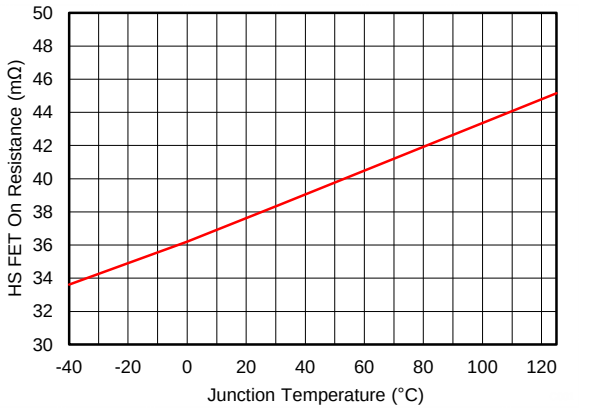

**Figure 1. Serial Interface Timing Diagram for Standard-, Fast-, Fast-Mode Plus**




Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

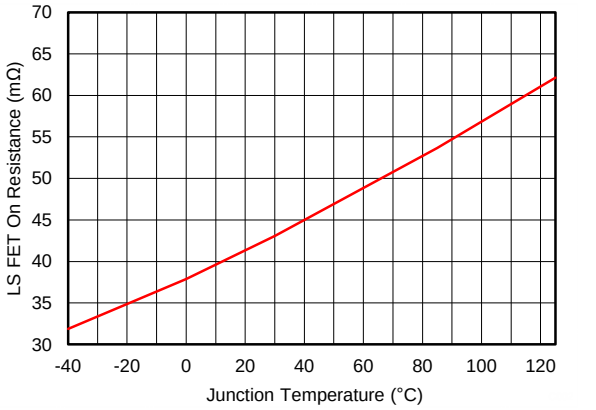
**Figure 2. Serial Interface Timing Diagram for H/S-Mode**

## 8.8 Typical Characteristics



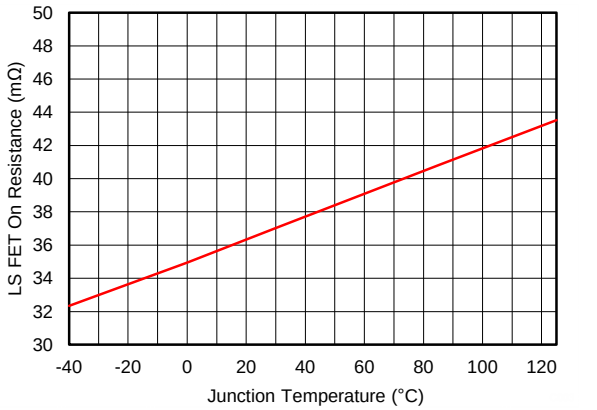

$V_{IN}$ = 3.2 V $V_{OUT}$ = 3.5 V $T_J$ = –40 to 125°C

**Figure 3. High side $R_{ds(on)}$ vs Junction Temperature**



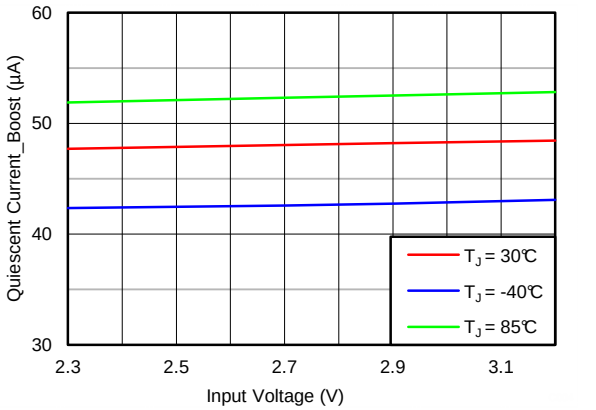

$V_{IN}$ = 3.2 V $V_{OUT}$ = 3.5 V $T_J$ = –40 to 125°C

**Figure 4. Low side $R_{ds(on)}$ vs Junction Temperature**



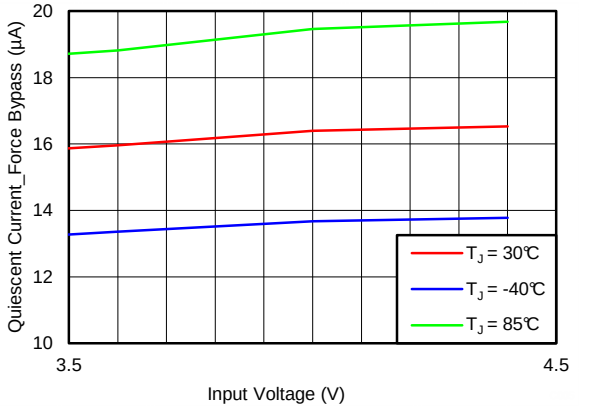

$V_{IN}$ = 3.2 V Bypass $T_J$ = –40 to 125°C

**Figure 5. Bypass FET $R_{ds(on)}$ vs Junction Temperature**



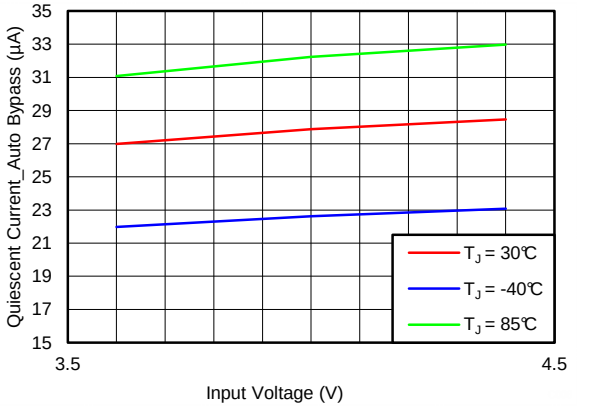

$V_{IN}$ = 2.3 - 3.4 V $V_{OUT}$ = 3.4 V $I_{OUT}$ = 0 mA
EN = High Bypass = High

**Figure 6. Quiescent Current at Boost Mode vs Input Voltage**




$V_{IN}$ = 3.5 - 4.4 V $V_{OUT}$ = 3.4 V $I_{OUT}$ = 0 mA
EN = High Bypass = Low

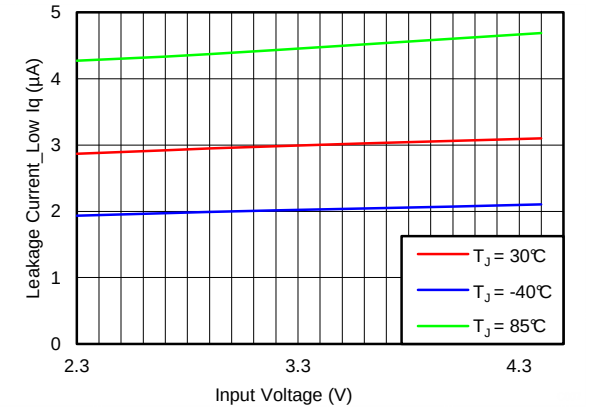
**Figure 7. Quiescent Current at Forced Bypass Mode vs Input Voltage**




$V_{IN}$ = 3.6 - 4.4 V $V_{OUT}$ = 3.4 V $I_{OUT}$ = 0 mA
EN = High Bypass = High

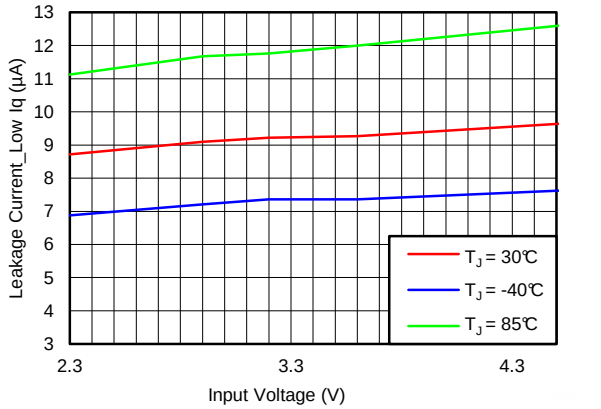
**Figure 8. Quiescent Current at Auto Bypass Mode vs Input Voltage**

## Typical Characteristics (continued)



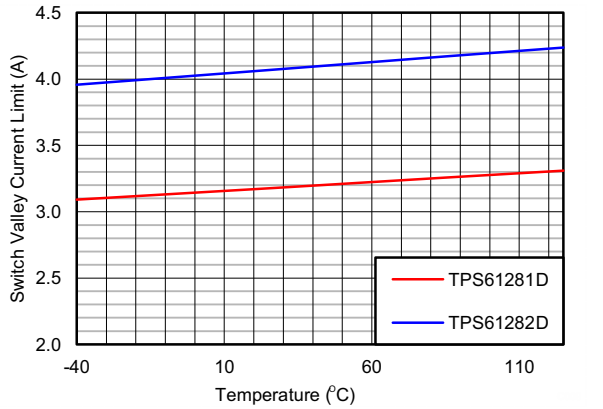

$V_{IN}$ = 2.3 - 4.4 V $V_{OUT}$ = 4.4 V $V_{SW}$ = 0 V
EN = Low Bypass = Low

**Figure 9. Shutdown Current at Low $I_Q$ mode vs Input Voltage**



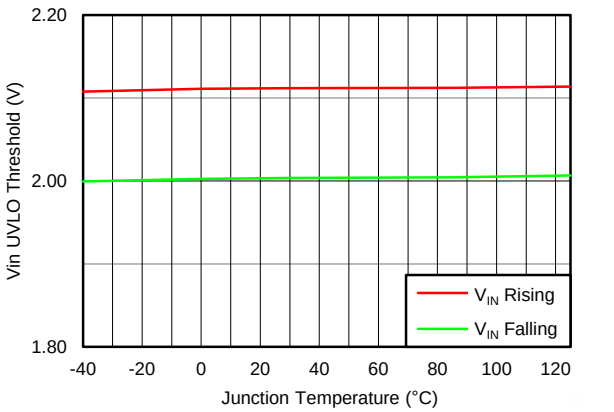

$V_{IN}$ = 2.3 - 4.4 V $V_{OUT}$ = 4.4 V $V_{SW}$ = 0 V
EN = Low Bypass = High

**Figure 10. Shutdown Current vs Input Voltage**



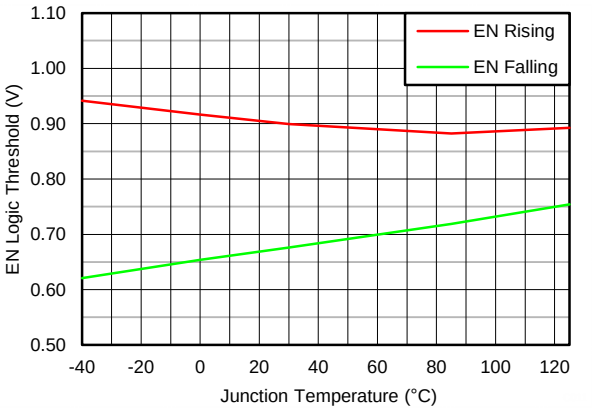

$V_{IN}$ = 3.2 V $V_{OUT}$ = 3.5 V $T_J$ = –40 to 125°C
EN = High Bypass = High

**Figure 11. Switch Valley Current Limit: TPS61281D, TPS61282D vs Input Voltage**



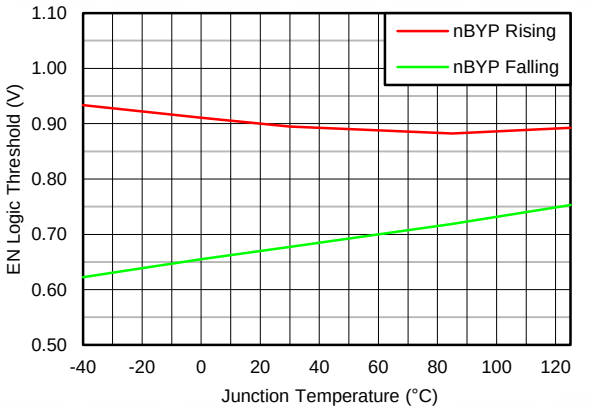

$V_{IN}$ = 3.2 V $V_{OUT}$ = 3.5 V $T_J$ = –40 to 125°C

**Figure 12. $V_{IN}$ UVLO Threshold Rising/Falling vs Junction Temperature**




$V_{IN}$ = 3.2 V $V_{OUT}$ = 3.5 V $T_J$ = –40 to 125°C

**Figure 13. EN Logic High Threshold Rising/Falling vs Junction Temperature**




$V_{IN}$ = 3.2 V $T_J$ = –40 to 125°C

**Figure 14. $\overline{BYP}$ Logic High Threshold Rising/Falling vs Junction Temperature**

# 9 Detailed Description

## 9.1 Overview

The TPS6128xD is a high-efficiency step-up converter featuring pass-through mode optimized to provide low-noise voltage supply for 2G RF power amplifiers (PAs) in mobile phones and/or to pre-regulate voltage for supplying subsystem like eMMC memory, audio codec, LCD bias, antenna switches, RF engine PMIC and so on. It is designed to allow the system to operate at maximum efficiency for a wide range of power consumption levels from a low-, wide- voltage battery cell.

The capability of the TPS6128xD to step-up the voltage as well as to pass-through the input battery voltage when its level is high enough allow systems to operate at maximum performance over a wide range of battery voltages, thereby extending the battery life between charging. The device also addresses brownouts caused by the peak currents drawn by the APU and GPU which can cause the battery rail to droop momentarily. Using the TPS6128xD device as a pre-regulator eliminates system brownout condition while maintaining a stable supply rail for critical sub-system to function properly.

The TPS6128xD synchronous step-up converter typically operates at a quasi-constant 2.3-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6128xD converter operates in power-save mode with pulse frequency modulation (PFM).

In general, a dc/dc step-up converter can only operate in "true" boost mode, that is the output “boosted” by a certain amount above the input voltage. The TPS6128xD device operates differently as it can smoothly transition in and out of zero duty cycle operation. Depending upon the input voltage, output voltage threshold and load current, the integrated bypass switch automatically transitions the converter into pass-through mode to maintain low-dropout and high-efficiency. The device exits pass-through mode (0% duty cycle operation) if the total dropout resistance in bypass mode is insufficient to maintain the output voltage at it's nominal level. Refer to the typical characteristics section (DC Output Voltage vs. Input Voltage) for further details.

During PWM operation, the converter uses a novel quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small ceramic inductor and capacitors. Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

The current mode architecture provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components.

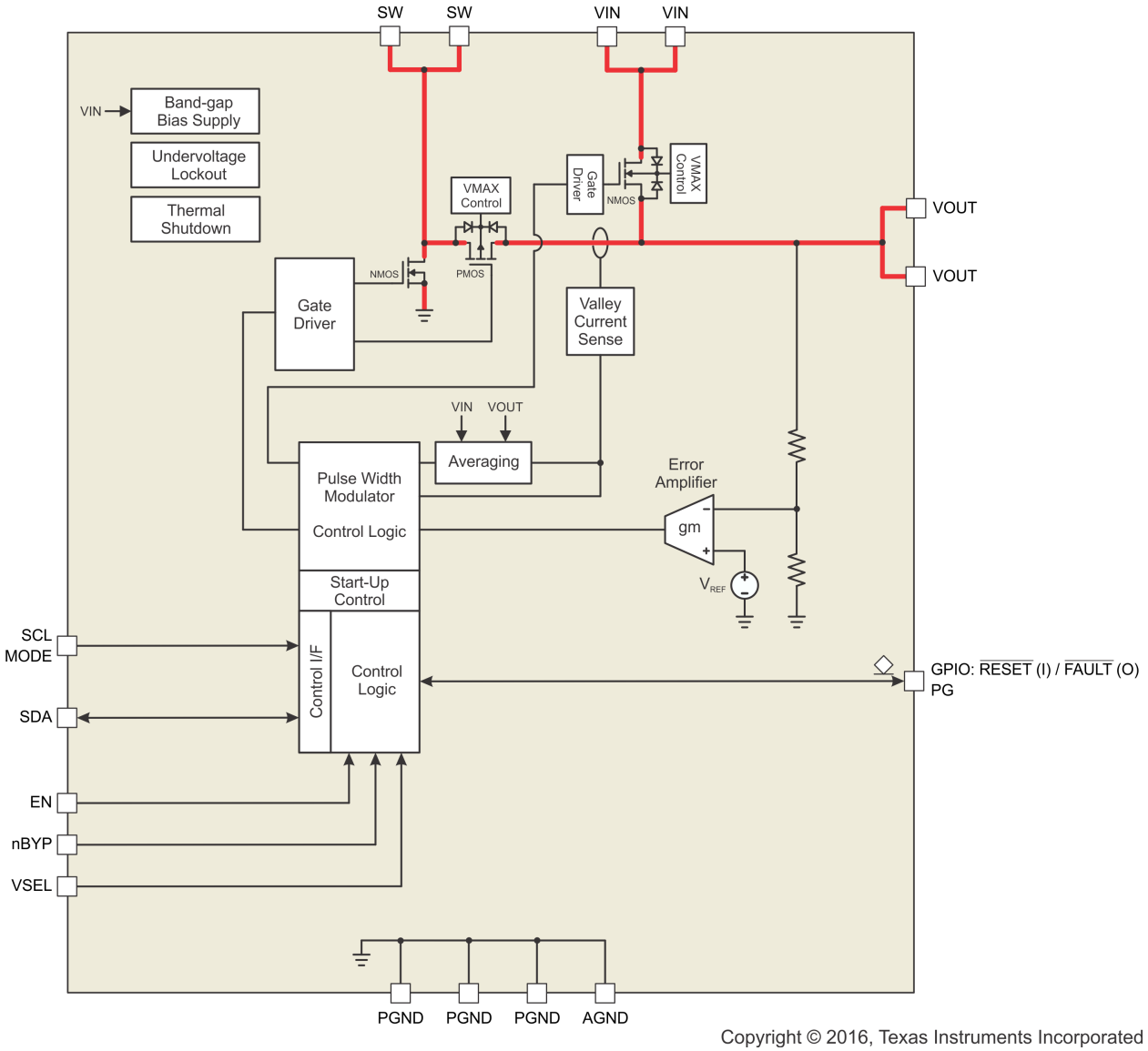
The TPS6128xD directly and accurately controls the average input current through intelligent adjustment of the valley current limit, allowing an accuracy of ±17.5%. Together with an external bulk capacitor, the TPS6128xD allows an application to be interfaced directly to its load, without overloading the input source due to appropriate set average input current limit. An open-drain output (PG or GPIO/nFAULT) provides a signal to issue an interrupt to the system if any fault is detected on the device (thermal shutdown, output voltage out-of limits, and so on).

The output voltage can be dynamically adjusted between two values (floor and roof voltages) by toggling a logic control input (VSEL) without the need for external feedback resistors. This features can either be used to raise the output voltage in anticipation of a positive load transient or to dynamically change the PA supply voltage depending on its mode of operation and/or transmitting power.

The TPS61280D integrates an $I^2C$ compatible interface allowing transfers up to 3.4Mbps. This communication interface can be used to set the output voltage threshold at which the converter transitions between boost and pass-through mode, for reprogramming the mode of operation (PFM/PWM or forced PWM), for settings the average input current limit or resetting the output voltage for instance.

Configuration parameters can be changed by writing the desired values to the appropriate $I^2C$ register(s). The $I^2C$ registers are volatile and their contents are lost when power is removed from the device. By writing to the E2PROMCTRL Register [reset = 0xFF], it is possible to store the active configuration in non-volatile $E^2PROM$; during power-up, the contents of the $E^2PROM$ are copied into the $I^2C$ registers and used to configure the device.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Voltage Scaling Management (VSEL)

In order to maintain a certain minimum output voltage under heavy load transients, the output voltage set point can be dynamically increased by asserting the VSEL input. The functionality also helps to mitigate undershoot during severe line transients, while minimizing the output voltage during more benign operating conditions to save power.

The output voltage ramps up (floor to roof transition) at pre-defined rate defined by the average input current limit setting. The required time to ramp down the voltage (roof to floor transition) largely depends on the amount of capacitance present at the converter's output as well as on the load current. Table 1 shows the ramp rate control when transitioning to a lower voltage.

**Table 1. Ramp Down Rate vs. Target Mode**

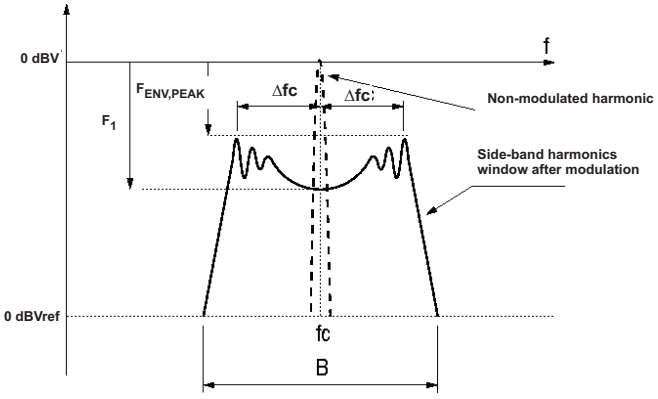
| Mode Associated with Floor Voltage | Output Voltage Ramp Rate |
|---|---|
| Forced PWM | Output capacitance is being discharged at a rate of approx. 50mA (or higher) constant current in addition to the load current drawn |
| PFM | Output capacitance is being discharged (solely) by the load current drawn |

### 9.3.2 Spread Spectrum, PWM Frequency Dithering

The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

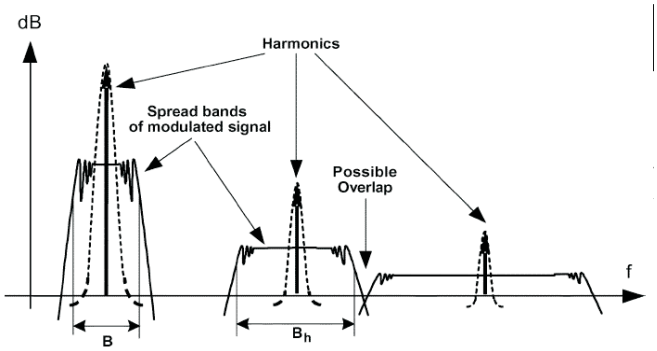
Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by ca. ±15% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency $f_m$.




$$B = 2 \cdot f_m \cdot (1 + m_f) = 2 \cdot (\Delta f_c + f_m)$$

**Figure 15. Spectrum of a Frequency Modulated Sin. Wave with Sinusoidal Variation in Time**




$$B = 2 \cdot f_m \cdot (1 + m_f) = 2 \cdot (\Delta f_c + f_m)$$
$$B_h = 2 \cdot f_m \cdot (1 + m_f \cdot h)$$

**Figure 16. Spread Bands of Harmonics in Modulated Square Signals (1)**

The above figures show that after modulation the sideband harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

(1) Spectrum illustrations and formulae (Figure 15 and Figure 16) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005.

$$m_f = \frac{\delta \times f_c}{f_m}$$

where

- $f_c$ is the carrier frequency (approx. 2.3MHz)
- $f_m$ is the modulating frequency (approx. 40kHz)
- $\delta$ is the modulation ratio (approx 0.15) (1)

$$\delta = \frac{\Delta f_c}{f_c} \quad (2)$$

The maximum switching frequency $f_c$ is limited by the process and finally the parameter modulation ratio ($\delta$), together with $f_m$ , which is the side-band harmonics bandwidth around the carrier frequency $f_c$. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \quad (3)$$

$f_m$ < RBW: The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

$f_m$ > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

## 9.4 Device Functional Modes

### 9.4.1 Power-Save Mode

The TPS6128xD integrates a power-save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

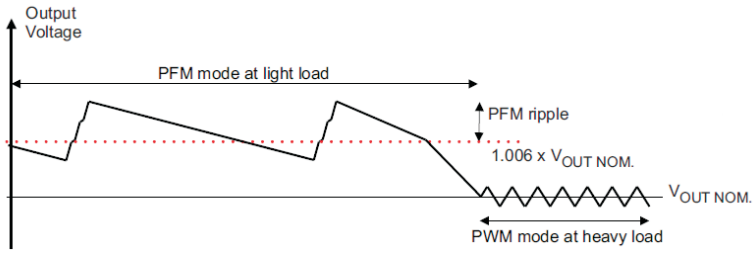



**Figure 17. Power-Save Mode Ripple**

### 9.4.2 Pass-Through Mode

The TPS6128xD contains an internal switch for bypassing the dc/dc boost converter during pass-through mode. When the input voltage is larger than the preset output voltage, the converter seamlessly transitions into 0% duty cycle operation and the bypass FET is fully enhanced. Entry in pass-through mode is triggered by condition where $V_{OUT}$ >(1+2%)* $V_{OUT\_NORM}$ and no switching has occurred during past 8µs.

In this mode of operation, the load (2G RF PA for instance) is directly supplied from the battery for maximum RF output power, highest efficiency and lowest possible input-to-output voltage difference. The device consumes only a standby current of 15µA (typ). In pass-through mode, the device is short-circuit protected by a very fast current limit detection scheme.

During this operation, the output voltage follows the input voltage and will not fall below the programmed output voltage threshold as the input voltage decreases. The output voltage drop during pass-through mode depends on the load current and input voltage, the resulting output voltage is calculated as:

## Device Functional Modes (continued)

$$V_{OUT} = V_{IN} - (R_{DSON(BP)} \times I_{OUT}) \quad (4)$$

Conversely, the efficiency in pass-through mode is defined as:

$$\eta = 1 - R_{DSON(BP)} \frac{I_{OUT}}{V_{IN}} \quad (5)$$

- in which $R_{DSON(BP)}$ is the typical on-resistance of the bypass FET

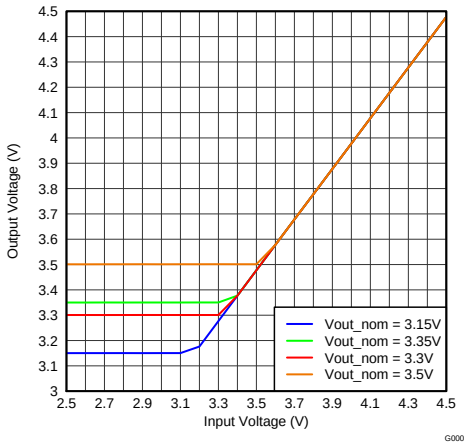



**Figure 18. DC Output Voltage vs. Input Voltage**

Pass-through mode exit is triggered when the output voltage reaches the pre-defined threshold (that is, 3.4V).

During pass-through mode, the TPS6128xD device is short-circuit protected by a fast current limit detection scheme. If the current in the pass-through FET exceeds approximately 7.3 Amps a fault is declared and the device cycles through a start-up procedure.

### 9.4.3 Mode Selection

Depending on the settings of CONFIG Register [reset = 0x01] the device can be operated at a quasi-constant 2.3-MHz frequency PWM mode or in automatic PFM/PWM mode. In this mode, the converter operates in pseudo-fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range. For more details, see the CONFIG Register [reset = 0x01] description.

The quasi-constant frequency PWM mode has the tightest regulation and the best line/load transient performance. In forced PWM mode, the device features a unique $R_{DS(ON)}$ management function to maintain high broadband efficiency as well as low resistance in pass-through mode.

In the TPS61280D device, the GPIO pin can be configured (via the CONFIG Register [reset = 0x01] ) to select the operating mode of the device. In the other TPS6128xD devices, the MODE pin is used to select the operating mode. Pulling this pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique allowing simple filtering of the switching harmonics in noise-sensitive applications.

For additional flexibility, it is possible to switch from power-save mode (GPIO or MODE input = L) to PWM mode (GPIO or MODE input = H) during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements (that is, 2G RF PA Rx/Tx operation).

Entry to forced pass-through mode (nBYP = L) initiates with a current limited transition followed by a true bypass state. To prevent reverse current to the battery, the devices waits until the output discharges below the input voltage level before entering forced pass-through mode. Care should be taken to prohibit the output voltage from collapsing whilst transitioning into forced pass-through mode under heavy load conditions and/or limited output capacitance. This can be easily done by adding capacitance to the output of the converter. In forced pass-through mode, the output follows the input below the preset output threshold voltage (VOUT_TH).

## Device Functional Modes (continued)

### 9.4.4 Current Limit Operation

The TPS6128xD device features a valley inductor current limit scheme.

In dc/dc boost mode, the TPS6128xD device employs a current limit detection scheme in which the voltage drop across the synchronous rectifier is sensed during the off-time. In the TPS61280D the current limit threshold can be set via an $I^2C$ register. TPS6128xD devices have a fixed current limit threshold. See *Device Comparison Table* for detailed information.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(MAX)}$), before entering current limit (CL) operation, can be defined by Equation 6.

$$I_{OUT(MAX\_DC)} = I_{LIMIT} \times \frac{V_{IN}}{V_{OUT}} \times \eta \quad (6)$$

where

- $\eta$ is the efficiency
- The inductor peak-to-peak current ripple ($\Delta I_L$) is calculated by Equation 7

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \quad (7)$$

The output current, $I_{OUT(DC)}$, is the average of the rectifier ripple current waveform. When the load current is increased such that the trough is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

Figure 19 illustrates the inductor and rectifier current waveforms during current limit operation.

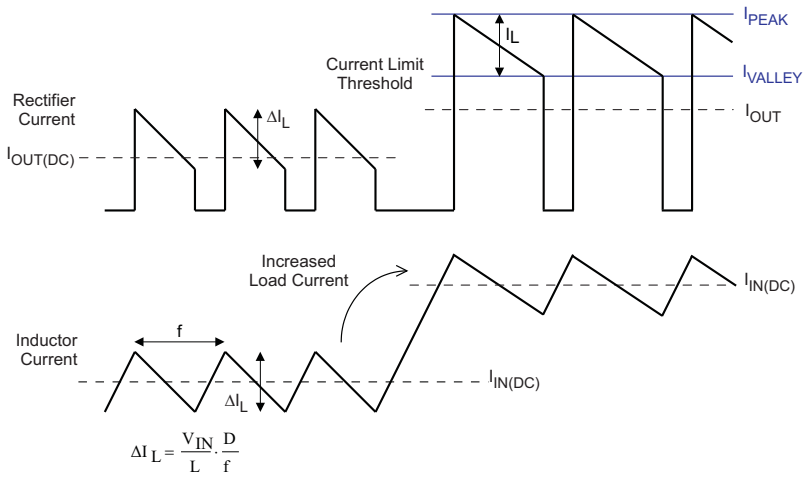



**Figure 19. Inductor/Rectifier Currents in Current Limit Operation (DC/DC Boost Mode)**

During pass-through mode, the TPS6128xD device is short-circuit protected by a very fast current limit detection scheme. If the current in the bypass FET exceeds approximately 7.5Amps a fault is declared and the device cycles through a start-up procedure.

## Device Functional Modes (continued)

### 9.4.5 Start-Up and Shutdown Mode

The TPS6128xD automatically powers-up as soon as the input voltage is applied. The device has an internal soft-start circuit that limits the inrush current during start-up. The first phase in the start-up procedure is to bias the output node close to the input level (so called pre-charge phase).

In this operating mode, the device limits its output current to ca. 500mA. Should the output voltage not have reached the input level within a maximum duration of 750µs, the device automatically increases its pre-charge current to ca. 2000mA. If the output voltage still fails to reach its target after 1.5ms, a fault condition is declared. After waiting 1ms, a restart is attempted.

When output voltage being close to Vout, the device enters into boost startup mode (for Auto Mode only). The device provides a reduced current limit of ~1.25A (I2C programable for TPS61280D to set it back to normal current limit) when the output voltage is below pre-set voltage to avoid the high inrush current from battery.

During start-up, it is recommended to keep DC load current draw below 250mA.

The TPS6128xD device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110°C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10°C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit condition.

When the EN and nBYP pins are set high, the device enters normal operation (that is, automatic dc/dc boost, pass-through mode) and ensures that the output voltage remains above a pre-defined threshold (that is, 3.3 V).

Setting the EN pin low (nBYP = 1) forces the TPS6128xD device in shutdown mode with a current consumption of <8.5 µA typical. In this mode, the output of the converter is regulated to a minimum level so as to limit the input-to-output voltage difference to less than 3.6 V (typical). The device is capable of sinking up to 10 mA output current and prohibits reverse current flow from the output to the input. For proper operation, the EN pin must be terminated and must not be left floating.

Changing operating mode from auto mode (EN = nBYP = 1) to low $I_Q$ Pass-through mode (EN = nBYP = 0) with device pins EN and nBYP can either be done controlling EN and nBYP pins from same control signal (delay between signal < 60ns) or first switching in forced pass-through mode (EN = 1, nBYP = 0) followed by switching to low $I_Q$ Pass-through mode (EN = nBYP = 0).

The TPS6128xD device also features the possibility of shutting the converter output for a short period of time, either via the nRST/nFAULT (GPIO). Pulling this input low initiates a reset of the converter's output. The sequence is falling edge-triggered and consists of a discharge phase (down to ca. 600 mV or lower) of the capacitance located at the converter's output followed by a start-up phase.

**Table 2. Mode of Operation**

| EN Input | nBYP Input | Device State |
|---|---|---|
| 0 | 0 | The device is shut down in pass-through mode featuring a shutdown current down to ca. 3µA typ.<br>The load current capability is limited (up to ca. 250mA). |
| 0 | 1 | The device is shut down and the output voltage is reduced to a minimum value (VIN - VOUT ≤ 3.6V).<br>The device shutdown current is approximately 8.5µA typ. |
| 1 | 0 | The device is active in forced pass-through mode.<br>The device supply current is approximately 15µA typ. from the battery. The device is short circuit protected by a current limit of ca.7300mA. |
| 1 | 1 | The device is active in auto mode (dc/dc boost, pass-through).<br>The device supply current is approximately 50µA typ. from the battery. |

### 9.4.6 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. The I2C control interface and the output stage of the converter are disabled once the falling $V_{IN}$ trips the under-voltage lockout threshold $V_{UVLO}$ (2 V typical). The device starts operation once the rising $V_{IN}$ trips $V_{UVLO}$ threshold plus its hysteresis of 100 mV at typ. 2.1 V.

### 9.4.7 Thermal Shutdown

As soon as the junction temperature, $T_J$, exceeds 160°C (typ.) the device goes into thermal shutdown. In this mode the bypass, high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continuous the operation.

### 9.4.8 Fault State and Power-Good

The TPS6128xD enters the fault state under any of the followings conditions:

- The output voltage fails to achieve the required level during a start-up phase.
- The output voltage falls out of regulation (in pre-charge mode).
- The device has entered thermal shutdown.

Once a fault is triggered, the regulator stops operating and disconnects the load. After waiting 1ms, the device attempts to restart. The TPS61280D device can be configured to signal a fault condition by pulling the open-drain GPIO pin (nFAULT) low for a short period of time. The nFAULT output provides a falling edge triggered interrupt signal to the host. To ensure proper operation, the GPIO port needs to be pull high quick enough, that is, faster than ca. 200ns. To do so, it is recommended to use a GPIO pull-up resistor in the range of 1kΩ to 10kΩ.

The TPS6128xD (simple logic I/F version) device only provide a power-good output (PG) for signaling the system when the regulator has successfully completed start-up and no faults have occurred. Power-good also functions as an early warning flag for excessive die temperature and overload conditions.

- PG is asserted high when the start-up sequence is successfully completed.
- PG is pulled low when the output voltage falls approximately 10% below its regulation level or the die temperature exceeds 115°C. PG is re-asserted high when the device cools below ca. 100°C.
- Any fault condition causes PG to be de-asserted.
- PG is pulled high when the device is operating in forced pass-through mode (that is, nBYP = L).
- PG is pulled high when the device is in shutdown mode.

## 9.5 Programming

### 9.5.1 Serial Interface Description (TPS61280D)

I²C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

The TPS6128xD device works as a *slave* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), fast mode plus (1 Mbps) and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1V.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode. The TPS6128xD device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7bit address is defined as ‘111 0101’.

It is recommended that the I2C masters initiates a STOP condition on the I2C bus after the initial power up of SDA and SCL pull-up voltages to ensure reset of the TPS6128xD I2C engine.

### 9.5.2 Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 20. All I²C-compatible devices should recognize a start condition.

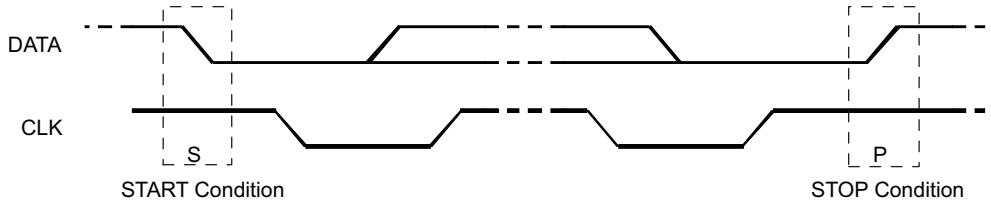



**Figure 20. START and STOP Conditions**

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 21). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 22) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

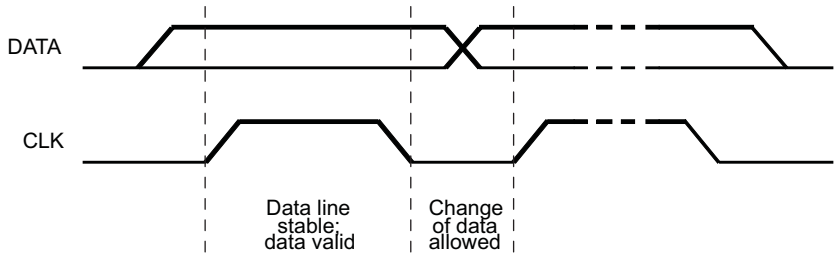



**Figure 21. Bit Transfer on the Serial Interface**

## Programming (continued)

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 20). This releases the bus and stops the communication link with the addressed slave. All $I^2C$ compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

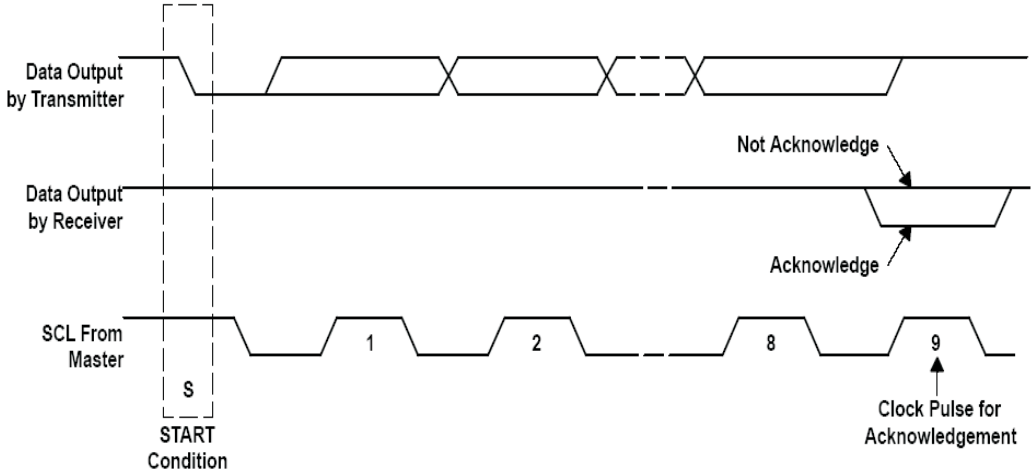



**Figure 22. Acknowledge on the $I^2C$ Bus**

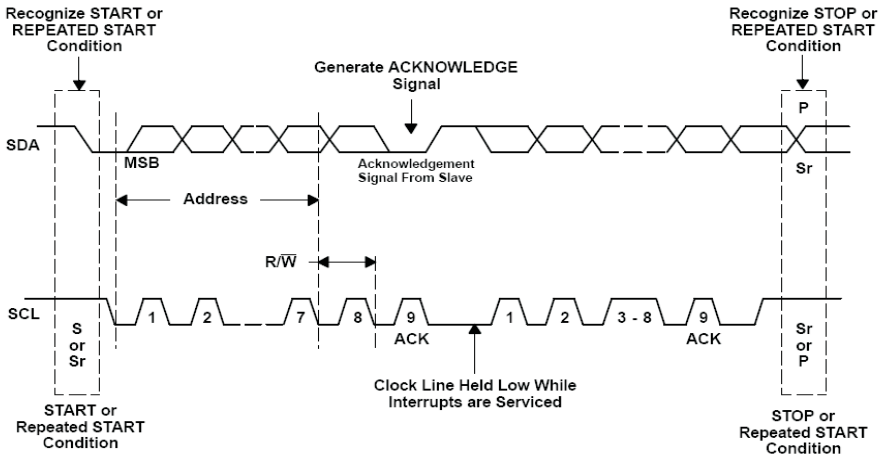



**Figure 23. Bus Protocol**

## Programming (continued)

### 9.5.3 HS-Mode Protocol

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

### 9.5.4 TPS6128xD I²C Update Sequence

The TPS6128xD requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6128xD device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS6128xD. TPS6128xD performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

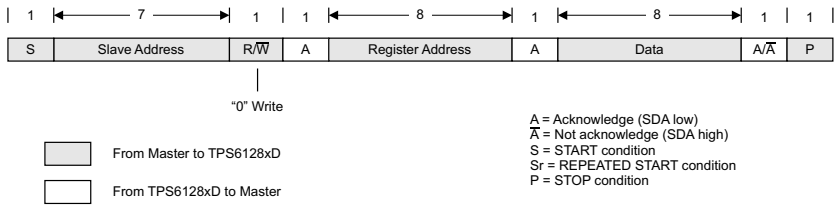



**Figure 24. : "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes**

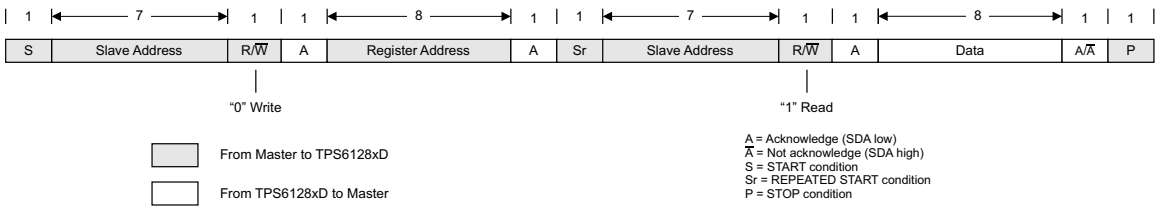



**Figure 25. "Read" Data Transfer Format in Standard-, Fast, Fast-Plus Modes**

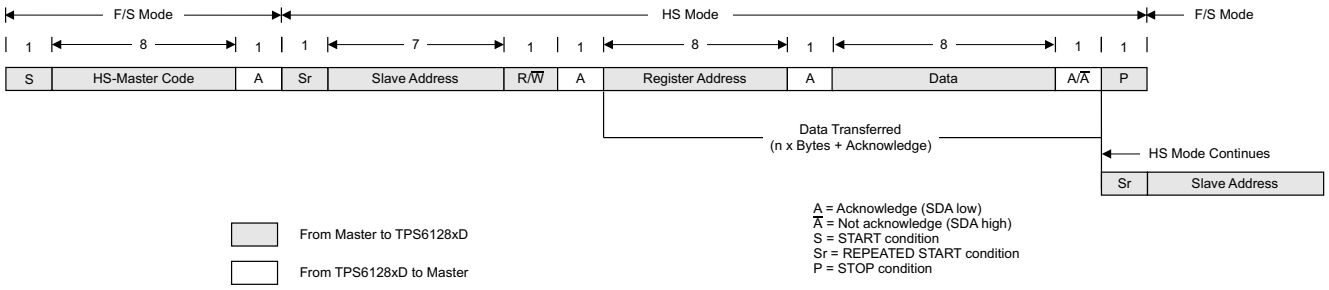



**Figure 26. Data Transfer Format in H/S-Mode**

## 9.6 Register Maps

### 9.6.1 Slave Address Byte

| MSB | | | | | | LSB |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | A1 | A0 |

The slave address byte is the first byte received following the START condition from the master device.

### 9.6.2 Register Address Byte

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 |

Following the successful acknowledgment of the slave address, the bus master will send a byte to the TPS6128xD, which will contain the address of the register to be accessed.

### 9.6.3 $I^2C$ Registers, $E^2PROM$, Write Protect

Configuration parameters can be changed by writing the desired values to the appropriate $I^2C$ register(s). The $I^2C$ registers are volatile and their contents are lost when power is removed from the device. By writing to the E2PROMCTRL Register [reset = 0xFF], it is possible to store the active configuration in non-volatile $E^2PROM$; during power-up, the contents of the $E^2PROM$ are copied into the $I^2C$ registers and used to configure the device.

**NOTE**

An active high Write Protect (WP) bit prevents the configuration parameters from being changed by accident. Once the $E^2PROM$ memory has been programmed with Write Protect (WP) bit set, its content will be locked and can not be reprogrammed any more.

Configuration parameters can be read from the $I^2C$ register(s) or $E^2PROM$ registers at any time (the WP bit has no effect on read operations).

### 9.6.4 $E^2PROM$ Configuration Parameters

Table 3 shows the memory map of the configuration parameters.

**Table 3. Configuration Memory Map**

| Register Address | Register Name | Factory Default | Description |
|---|---|---|---|
| 01h | CONFIG Register [reset = 0x01] | xxh | Sets miscellaneous configuration bits |
| 02h | VOUTFLOORSET Register [reset = 0x02] | xxh | Sets the floor output voltage threshold boost / pass-through mode change (VSEL = L) |
| 03h | VOUTROOFSET Register [reset = 0x03] | xxh | Sets the roof output voltage threshold boost / pass-through mode change (VSEL = H) |
| 04h | ILIMSET Register [reset = 0x04] | xxh | Sets the average input current limit in dc/dc boost mode |
| 05h | Status Register [reset = 0x05] | xxh | Returns status flags |
| FFh | E2PROMCTRL Register [reset = 0xFF] | 00h | Controls whether read and write operations access $I^2C$ or $E^2PROM$ registers |

The following procedure details how to save the content of all $I^2C$ registers to the $E^2PROM$ non-volatile configuration memory.

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (for example EAh)
3. TPS6128xD acknowledges (SDA low)
4. Bus master sends address of E2PROMCTRL Register [reset = 0xFF] (FFh)
5. TPS6128xD acknowledges (SDA low)
6. Bus master sends data to be written to the Control Register (C0h)
7. TPS6128xD acknowledges (SDA low)
8. Bus master sends STOP condition


**Figure 27. Saving Contents of all $I^2C$ Registers to $E^2PROM$**

### 9.6.5 CONFIG Register [reset = 0x01]

Memory location: 0x01

**Figure 28. CONFIG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESET | ENABLE | | RESERVED | GPIOCFG | SSFM | MODE_CTRL | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Stored in $E^2$ | | | | | | | |
| N | Y | Y | N | Y | Y | Y | Y |

**Table 4. CONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESET | R/W | 0 | Device reset bit.<br>0: Normal operation. or line breaks<br>1: Default values are set to all internal registers. The device operation is cycled (ON-OFF-ON), that is, the converter is disabled for a short period of time and the output is reset. |
| 6:5 | ENABLE | R/W | 0 | Device enable bits.<br>00: Device operation follows hardware control signal (refer to Table 2).<br>01: Device operates in auto transition mode (dc/dc boost, bypass) regardless of the nBYP control signal (EN = 1).<br>10: Device is forced in pass-through mode regardless of the nBYP control signal (EN = 1).<br>11: Device is in shutdown mode. The output voltage is reduced to a minimum value (VIN - VOUT ≤ 3.6V) regardless of the nBYP control signal (EN = 1). |
| 4 | RESERVED | R/W | 0 | Reserved bit.<br>This bits is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned. |
| 3 | GPIOCFG | R/W | 0 | GPIO port configuration bit.<br>0: GPIO port is configured to support manual reset input (nRST) and interrupt generation output (nFAULT).<br>1: GPIO port is configured as a device mode selection input. |
| 2 | SSFM | R/W | 0 | Spread modulation control.<br>0: Spread spectrum modulation is disabled.<br>1: Spread spectrum modulation is enabled in PWM mode |
| 1:0 | MODE_CTRL | R/W | 1 | Device mode of operation bits.<br>00: Device operation follows hardware control signal (GPIO must be configured as mode selection input).<br>01: PFM with automatic transition into PWM operation.<br>10: Forced PWM operation.<br>11: PFM with automatic transition into PWM operation (VSEL = L), forced PWM operation (VSEL = H). |

### 9.6.6 VOUTFLOORSET Register [reset = 0x02]

Memory location: 0x02

**Figure 29. VOUTFLOORSET Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | VOUTFLOOR_TH | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Stored in $E^2$ | | | | | | | |
| N | N | N | Y | Y | Y | Y | Y |

**Table 5. VOUTFLOORSET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R/W | 0 | Reserved bit.<br>This bits is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned. |
| 4 | VOUTFLOOR_TH | R/W | 0 | Output voltage threshold, dc/dc boost / pass-through mode change.<br>00000: 2.850V<br>00001: 2.900V<br>00010: 2.950V<br>00011: 3.000V<br>00100: 3.050V<br>00101: 3.100V<br>00110: 3.150V<br>00111: 3.200V<br>01000: 3.250V<br>01001: 3.300V<br>01010: 3.350V<br>01011: 3.400V<br>01100: 3.450V<br>01101: 3.500V<br>01110: 3.550V<br>01111: 3.600V<br>10000: 3.650V<br>10001: 3.700V<br>10010: 3.750V<br>10011: 3.800V<br>10100: 3.850V<br>10101: 3.900V<br>10110: 3.950V<br>10111: 4.000V<br>11000: 4.050V<br>11001: 4.100V<br>11010: 4.150V<br>11011: 4.200V<br>11100: 4.250V<br>11101: 4.300V<br>11110: 4.350V<br>11111: 4.400V |
| 3 | | R/W | 0 | |
| 2 | | R/W | 1 | |
| 1 | | R/W | 1 | |
| 0 | | R/W | 0 | |

### 9.6.7 VOUTROOFSET Register [reset = 0x03]

Memory location: 0x03

**Figure 30. VOUTROOFSET Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | VOUTROOF_TH | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Stored in $E^2$ | | | | | | | |
| N | N | N | Y | Y | Y | Y | Y |

**Table 6. VOUTROOFSET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R/W | 0 | you can use Para elements with role attributes set for IP-XACT or line breaks<br>You cannot use "morerows" in these tables, see wiki for more information 'Register Guidelines' |
| 4 | VOUTROOF_TH | R/W | 0 | Output voltage threshold, dc/dc boost / pass-through mode change.<br>00000: 2.850V 10000: 3.650V<br>00001: 2.900V 10001: 3.700V<br>00010: 2.950V 10010: 3.750V<br>00011: 3.000V 10011: 3.800V<br>00100: 3.050V 10100: 3.850V<br>00101: 3.100V 10101: 3.900V<br>00110: 3.150V 10110: 3.950V<br>00111: 3.200V 10111: 4.000V<br>01000: 3.250V 11000: 4.050V<br>01001: 3.300V 11001: 4.100V<br>01010: 3.350V 11010: 4.150V<br>01011: 3.400V 11011: 4.200V<br>01100: 3.450V 11100: 4.250V<br>01101: 3.500V 11101: 4.300V<br>01110: 3.550V 11110: 4.350V<br>01111: 3.600V 11111: 4.400V |
| 3 | | R/W | 1 | |
| 2 | | R/W | 0 | |
| 1 | | R/W | 1 | |
| 0 | | R/W | 0 | |

### 9.6.8 ILIMSET Register [reset = 0x04]

Memory location: 0x04

**Figure 31. ILIMSET Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | ILIM OFF | Soft-start | ILIM | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Stored in $E^2$ | | | | | | | |
| N | N | N | Y | Y | Y | Y | Y |

**Table 7. ILIMSET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | RESERVED | R/W | 0 | Reserved bit.<br>This bits is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned. |
| 5 | ILIM OFF | R/W | 0 | Enable/Disable Current Limit<br>0 : Current Limit Enabled<br>1 : Current Limit Disabled |
| 4 | Soft-start | R/W | 1 | Soft-start selection bit.<br>0: DC/DC boost soft-start current is limited per ILIM bit settings<br>1: DC/DC boost soft-start current is limited to ca. 1250mA inductor valley current |
| 3 | ILIM | R/W | 1 | Inductor valley current limit in dc/dc boost mode (COUTRNG bit = 0)(1).<br>1000: 1500mA<br>1001: 2000mA<br>1010: 2500mA<br>1011: 3000mA<br>1100: 3500mA<br>1101: 4000mA<br>1110: 4500mA<br>1111: 5000mA |
| 2 | | R/W | 0 | |
| 1 | | R/W | 1 | |
| 0 | | R/W | 1 | |

(1) Refer to Start-Up and Shutdown Mode Mode section for additional information.

### 9.6.9 Status Register [reset = 0x05]

Memory location: 0x05

**Figure 32. Status Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TSD | HOTDIE | DCDCMODE | OPMODE | ILIMPT | ILIMBST | FAULT | PGOOD |
| R | R | R | R | R | R | R | R |
| Stored in $E^2$ | | | | | | | |
| N | N | N | N | N | N | N | N |

**Table 8. Status Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | TSD | R | 0 | Thermal shutdown status bit.<br>0: Normal operation.<br>1: Thermal shutdown tripped. This flag is reset after readout. |
| 6 | HOTDIE | R | 0 | Instantaneous die temperature bit.<br>0: $T_J$ < 115ºC.<br>1: $T_J$ > 115ºC. |
| 5 | DCDCMODE | R | 0 | DC/DC mode of operation status bit.<br>1: Device operates in PFM mode.<br>0: Device operates in PWM mode. |
| 4 | OPMODE | R | 0 | Device mode of operation status bit.<br>0: Device operates in pass-through mode.<br>1: Device operates in dc/dc mode. |
| 3 | ILIMPT | R | 0 | Current limit status bit (pass-through mode).<br>0: Normal operation.<br>1: Indicates that the bypass FET current limit has triggered. This flag is reset after readout. |
| 2 | ILIMBST | R | 0 | Current limit status bit (dc/dc boost mode).<br>0: Normal operation.<br>1: Indicates that the average input current limit has triggered for 1.5ms in dc/dc boost mode. This flag is reset after readout. |
| 1 | FAULT | R | 0 | FAULT status bit.<br>0: Normal operation.<br>1: Indicates that a fault condition has occurred. This flag is reset after readout. |
| 0 | PGOOD | R | 0 | Power Good status bit.<br>0: Indicates the output voltage is out of regulation.<br>1: Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in pass-through mode. |

### 9.6.10 E2PROMCTRL Register [reset = 0xFF]

Memory location: 0xFF

**Figure 33. E2PROMCTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| WEN | WP | ISE2PROMWP | RESERVED | | | | |
| R/W | R/W | R | R/W | R/W | R/W | R/W | R/W |
| Stored in $E^2$ | | | | | | | |
| N | Y | N | N | N | N | N | N |

**Table 9. E2PROMCTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | WEN | R/W | 0 | $E^2$PROM Write Enable bit.<br>0: No operation.<br>1: Forces the contents of selected $I^2C$ register bits to be copied into $E^2$PROM, thereby making them the default values during power-up. When the contents of all the $I^2C$ register bits have been written to the $E^2$PROM, the device automatically resets this bit. |
| 6 | WP | R/W | 0 | $E^2$PROM Write Protect bit.<br>0: Normal operation.<br>1: Forces the $E^2$PROM content to be locked following a write sequence (WEN = 1). This protects the $E^2$PROM content from undesirable write actions making it virus safe. This process is non reversible. |
| 5 | ISE2PROMWP | R | 0 | $E^2$PROM Write Protect Status bit.<br>0: $E^2$PROM content is not write protected. $E^2$PROM content can still be updated.<br>1: $E^2$PROM content is write protected. $E^2$PROM content is permanently locked. |
| 4:0 | RESERVED | R/W | 0 | Reserved bit.<br>This bits is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned. |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The devices are step up dc/dc converters with true bypass function integrated. They are typically used as preregulators with input voltage ranges from 2.3V to 4.8V, extend the battery run time and overcome input current and input voltage limitations of the system being powered.

While the input voltage higher than boost/bypass threshold, the high-efficient integrated pass-through path connects the battery to the powered system directly.

If the input voltage becomes lower than boost/bypass threshold, the device seamlessly transitions into boost mode operation with a maximum available output current of 3 A.

The following design procedure can be used to select component values for the TPS61281D and TPS61282D (also applicable for TPS61280D just by $I^2C$ program).

## 10.2 Typical Application

### 10.2.1 TPS61281D with 2.5V-4.35 $V_{IN}$, 1500 mA Output Current (TPS61280D with default $I^2C$ Configuration)

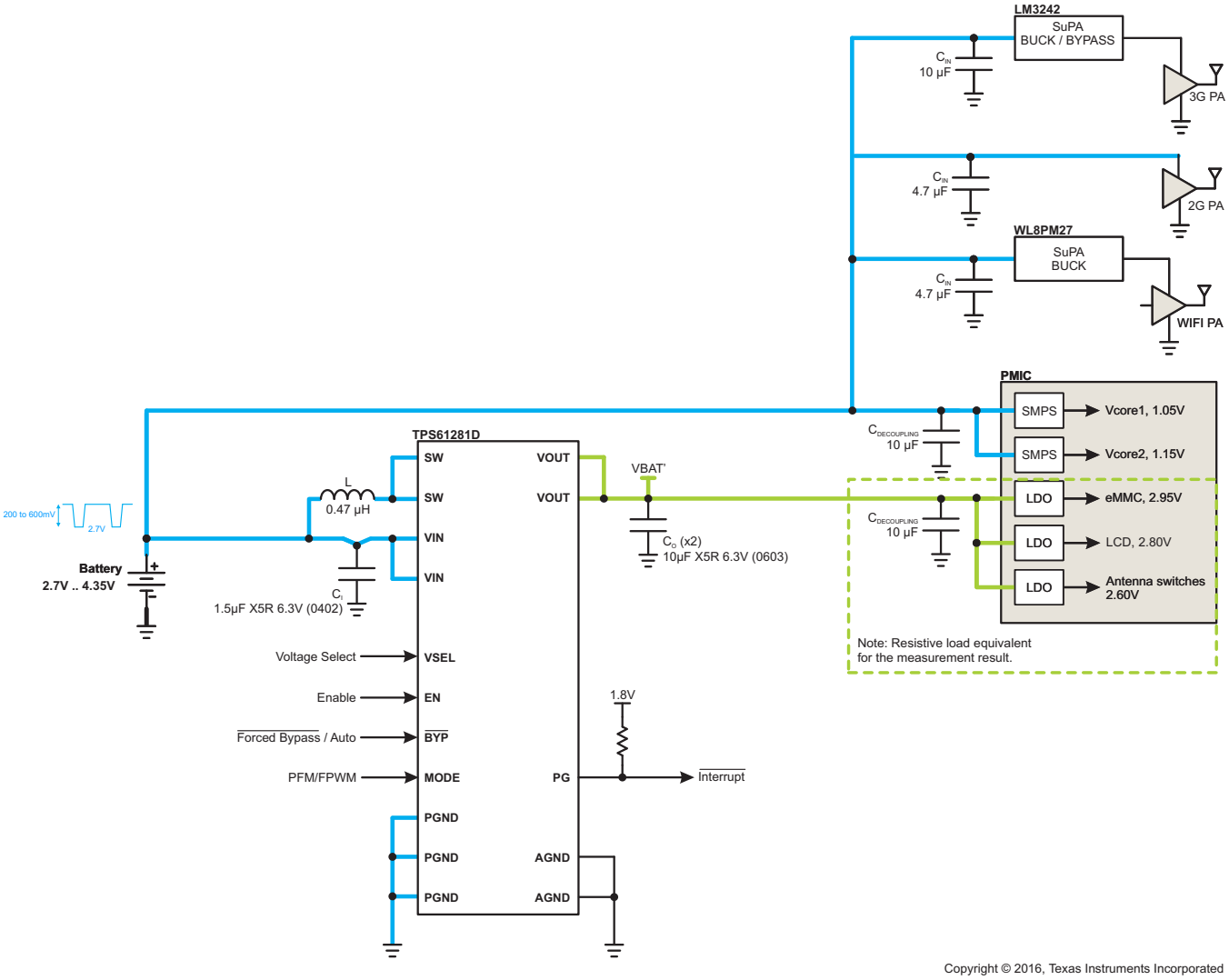





**Figure 34. TPS61281D Application Circuit with 1500mA Output Current**

#### *10.2.1.1 Design Requirement*

**Table 10. Design Parameters**

| REFERENCE | DESCRIPTION | SAMPLE VALUES |
|---|---|---|
| $V_{IN}$ | Input voltage range | 2.5V-4.35V |
| $V_{OUT}$ | Output voltage range at $V_{SEL}$ = Low | $V_{OUT}$ = 3.15 V if $V_{IN} \leq$ 3.15 V, $V_{OUT} = V_{IN}$ if $V_{IN}$ > 3.15 V |
| $V_{OUT}$ | Output voltage range $V_{SEL}$ = High | $V_{OUT}$= 3.35 V if $V_{IN} \leq$ 3.35 V, $V_{OUT} = V_{IN}$ if $V_{IN}$ > 3.35 V |
| $I_{OUT}$ | Output current | 1500mA |

### 10.2.1.2 Detailed Design Parameters

#### 10.2.1.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor are required. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages and can be estimated using Equation 8.

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \quad \text{with} \quad D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{8}$$

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce it's reliability.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. The inductor DC current rating should be greater than the maximum input average current, refer to Equation 9 and the *Current Limit Operation* section for more details.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \times I_{OUT} \tag{9}$$

The TPS6128xD series of step-up converters have been optimized to operate with a effective inductance in the range of 200 nH to 800 nH. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions. For more details, see the *Checking Loop Stability* section.

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$ , and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

For good efficiency, the inductor DC resistance should be less than 30 mΩ. The following inductor series from different suppliers have been used with the TPS6128xD converters.

**Table 11. List of Inductors**

| SERIES | DIMENSIONS (in mm) | DC INPUT CURRENT LIMIT SETTING |
|---|---|---|
| DFE252010C | 2.5 x 2.0 x 1.0 max. height | ≤3000 mA |
| DFE252012C | 2.5 x 2.0 x 1.2 max. height | ≤3500 mA |
| DFR252010C | 2.5 x 2.0 x 1.0 max. height | ≤3000 mA |
| DFE252012C | 2.5 x 2.0 x 1.2 max. height | ≤3500 mA |
| DFE252012P | 2.5 x 2.0 x 1.2 max. height | ≤3500 mA |
| DFE201610C | 2.0 x 1.6 x 1.0 max. height | ≤2000 mA |
| DFE201612C | 2.0 x 1.6 x 1.2 max. height | ≤3000 mA |
| DFE201612P | 2.0 x 1.6 x 1.2 max. height | ≤3000 mA |

#### 10.2.1.2.2 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the $V_{OUT}$ and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 10 can be used.

$$C_{MIN} = \frac{I_{OUT} \text{ x } (V_{OUT} - V_{IN})}{f \text{ x } \Delta V \text{ x } V_{OUT}} \quad (10)$$

where

- f is the switching frequency which is 2.3 MHz (typ.) and ΔV is the maximum allowed output ripple.

With a chosen ripple voltage of 20 mV, a minimum effective capacitance of 10 µF is needed. The total ripple is larger due to the ESR and ESL of the output capacitor. This additional component of the ripple can be calculated using Equation 11

$$\Delta V_{OUT(ESR)} = ESR \text{ x } \left( \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} \right) \quad (11)$$

$$\Delta V_{OUT(ESL)} = ESL \text{ x } \left( \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} - I_{OUT} \right) \text{ x } \frac{1}{t_{SW(RISE)}} \quad (12)$$

$$\Delta V_{OUT(ESL)} = ESL \text{ x } \left( \frac{I_{OUT}}{1 - D} - \frac{\Delta I_L}{2} - I_{OUT} \right) \text{ x } \frac{1}{t_{SW(FALL)}}$$

where

- $I_{OUT}$ = output current of the application
- D = duty cycle
- $\Delta I_L$ = inductor ripple current
- $t_{SW(RISE)}$ = switch node rise time
- $t_{SW(FALL)}$ = switch node fall time
- ESR = equivalent series resistance of the used output capacitor
- ESL = equivalent series inductance of the used output capacitor (13)

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

In applications featuring high (pulsed) load currents (e.g. ≥ 2 Amps), it is recommended to run the converter with a reasonable amount of effective output capacitance and low-ESL device, for instance x2 22 µF X5R 6.3V (0603) MLCC capacitors connected in parallel with a 1 µF X5R 6.3 V (0306-2T) MLCC LL capacitor.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and it's effective capacitance. For instance, a 10 µF X5R 6.3 V (0603) MLCC capacitor would typically show an effective capacitance of less than 5 µF (under 3.5 V bias condition, high temperature).

For RF Power Amplifier applications, the output capacitor loading is combined between the dc/dc converter and the RF Power Amplifier (x2 10 µF X5R 6.3 V (0603) + PA input cap 4.7 µF X5R 6.3 V (0402)) are recommended.

High values of output capacitance are mainly achieved by putting capacitors in parallel. This reduces the overall series resistance (ESR) to very low values. This results in almost no voltage ripple at the output and therefore the regulation circuit has no voltage drop to react on. Nevertheless, for accurate output voltage regulation even with low ESR, the regulation loop can switch to a pure comparator regulation scheme.

#### 10.2.1.2.3 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 4.7-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between $C_I$ and the power source lead to reduce ringing than can occur between the inductance of the power source leads and $C_I$.

#### 10.2.1.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, $I_L$
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. $V_{OUT}$ immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{(LOAD)}$ begins to charge or discharge $C_{OUT}$ generating a feedback error signal used by the regulator to return $V_{OUT}$ to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, $V_{OUT}$ can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (that is, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

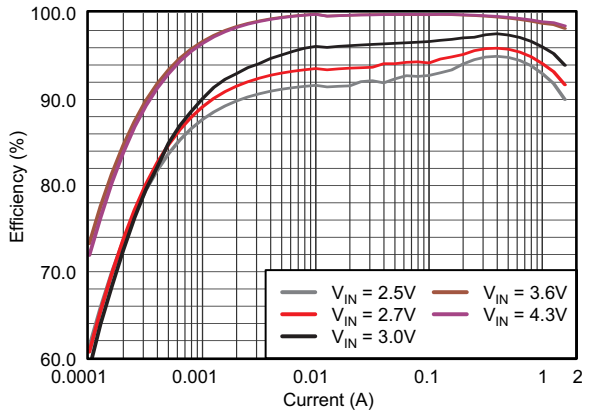
The TPS6128xD series of step-up converters have been optimized to operate with a effective inductance in the range of 200 nH to 800 nH and with output capacitors in the range of 8 µF to 100 µF. The internal compensation is optimized for an output filter of L = 0.5 µH and $C_O$ = 15 µF.

**Table 12. Component List**

| REFERENCE | DESCRIPTION | PART NUMBER, MANUFACTURER(1) |
|---|---|---|
| $C_{IN}$ | 1.5µF, 6.3V, 0402, X5R ceramic | GRM155R60J155ME80D |
| $C_{OUT}$ | 2 x 10µF, 6.3V, 0603, X5R ceramic | 2 x GRM188R60J106ME84 |
| L | 470nH, 47mΩ, 2.5mm x 2.0mm x 1.2mm | DFE252012CR470 |

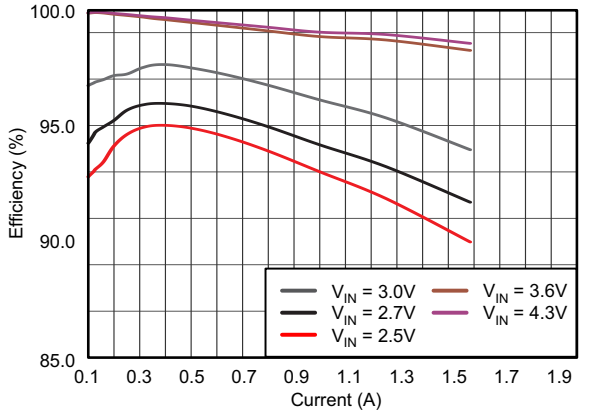
(1) See *Third-Party Products Disclaimer*

### 10.2.1.3 Application Performance Curves



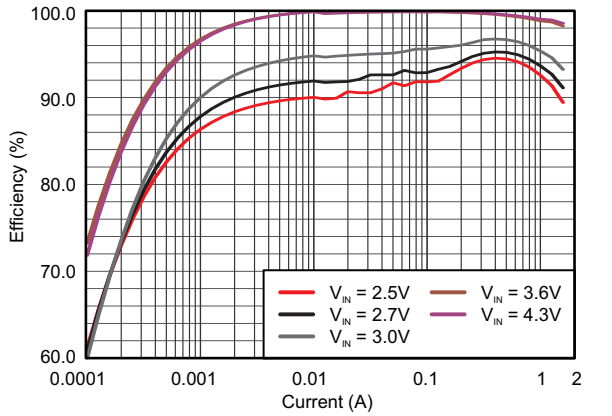

$V_{OUT}$ = 3.15 V VSEL = Low Mode = Low

**Figure 35. TPS61281D Efficiency vs Output Current**



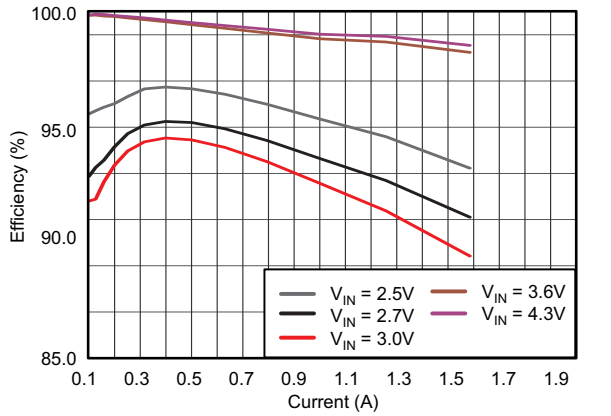

$V_{OUT}$ = 3.15 V VSEL = Low Mode = Low

**Figure 36. TPS61281D Efficiency vs Output Current**



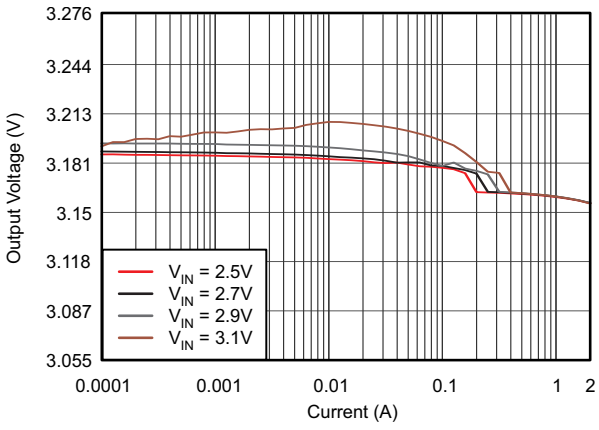

$V_{OUT}$ = 3.35 V VSEL = High Mode = Low

**Figure 37. TPS61281D Efficiency vs Output Current**



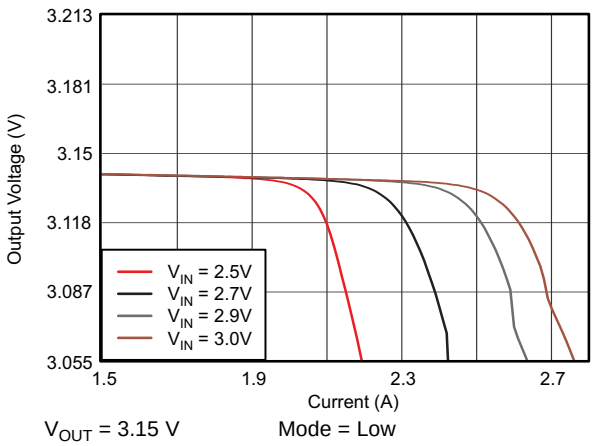

$V_{OUT}$ = 3.35 V VSEL = High Mode = Low

**Figure 38. TPS61281D Efficiency vs Output Current**



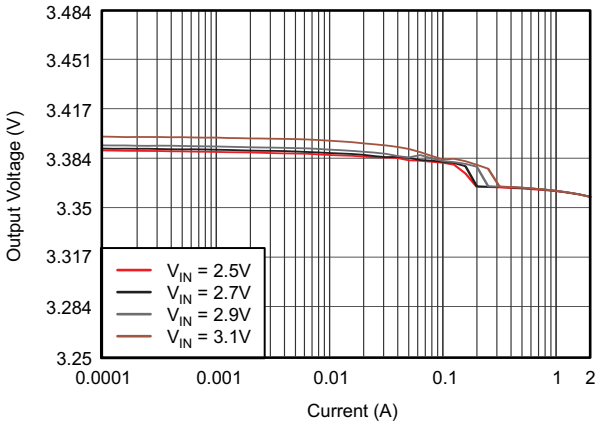

$V_{OUT}$ = 3.15 V Mode = Low

**Figure 39. TPS61281D DC Output Voltage vs Output Current**



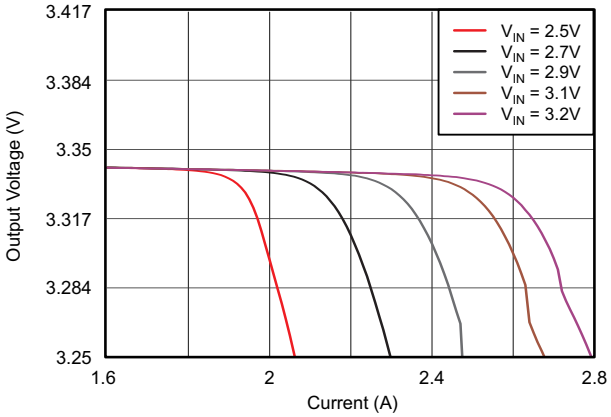

$V_{OUT}$ = 3.15 V Mode = Low

**Figure 40. TPS61281D DC Output Voltage vs Output Current**



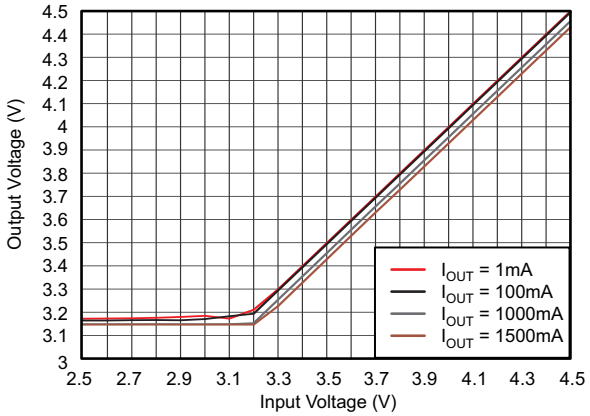

$V_{OUT}$ = 3.35 V Mode = Low

**Figure 41. TPS61281D DC Output Voltage vs Output Current**



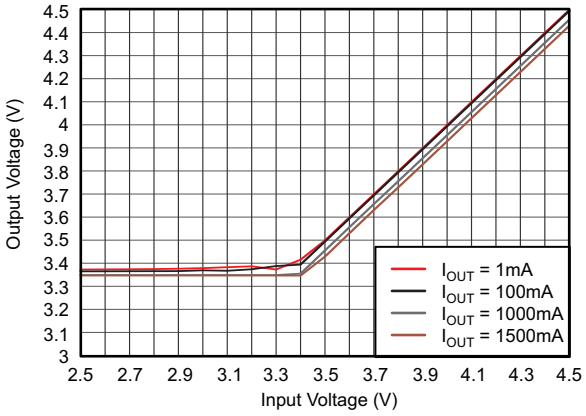

$V_{OUT}$ = 3.35 V Mode = Low

**Figure 42. TPS61281D DC Output Voltage vs Output Current**



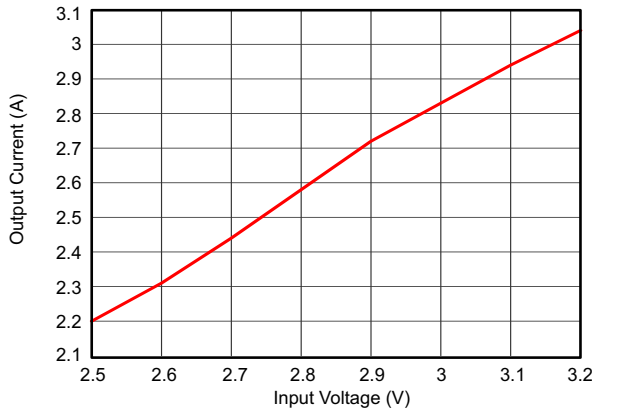

$V_{OUT}$ = 3.15 V VSEL = Low

**Figure 43. TPS61281D DC Output Voltage vs Input Voltage**




$V_{OUT}$ = 3.35 V VSEL = High Mode = Low

**Figure 44. TPS61281D DC Output Voltage vs Input Voltage**




$V_{OUT}$ = 3.35 V $T_A$ = 85°C Mode = Low

**Figure 45. TPS61281D Maximum Output Current vs Input Voltage**

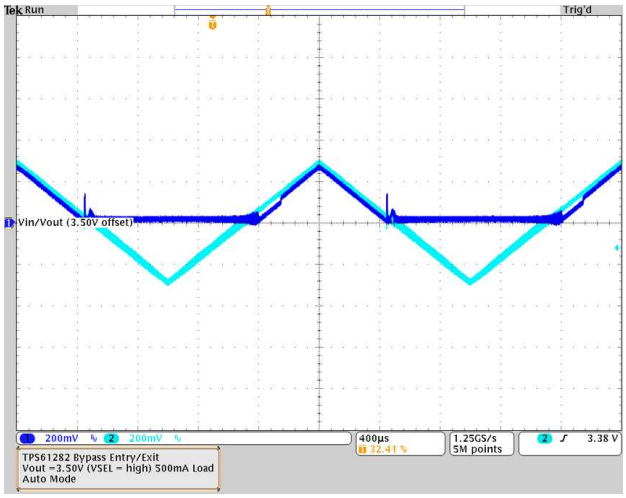



**Figure 46. Boost to Pass-Through Mode Exit / Entry**

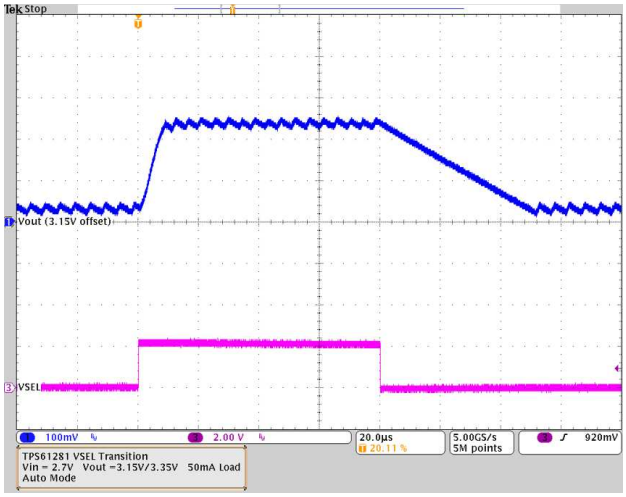



**Figure 47. TPS61281D Dynamic Voltage Management (VSEL) Load Current 50 mA**

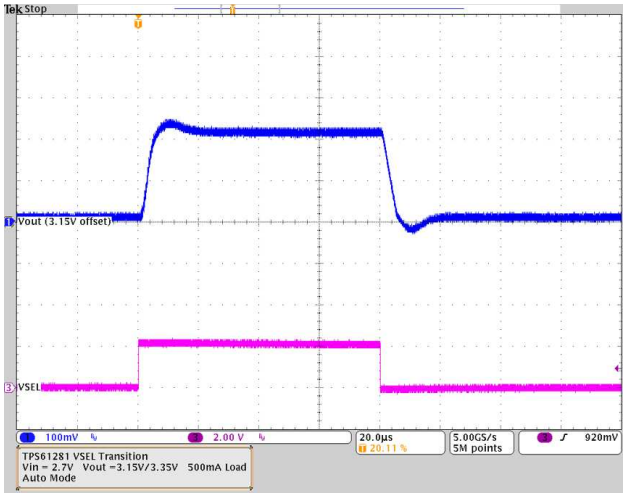



**Figure 48. TPS61281D Dynamic Voltage Management (VSEL) Load Current 500 mA**

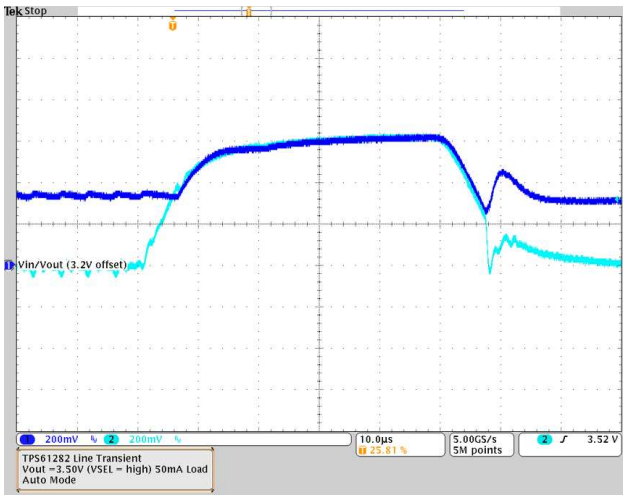



**Figure 49. TPS61281D Forced Pass-Through to Boost Mode Transition**

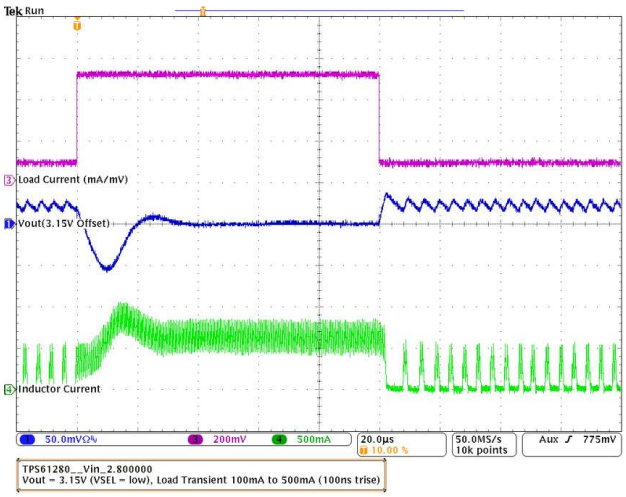



**Figure 50. TPS61280D, 81A Load Transient Response In PFM/PWM Operation**

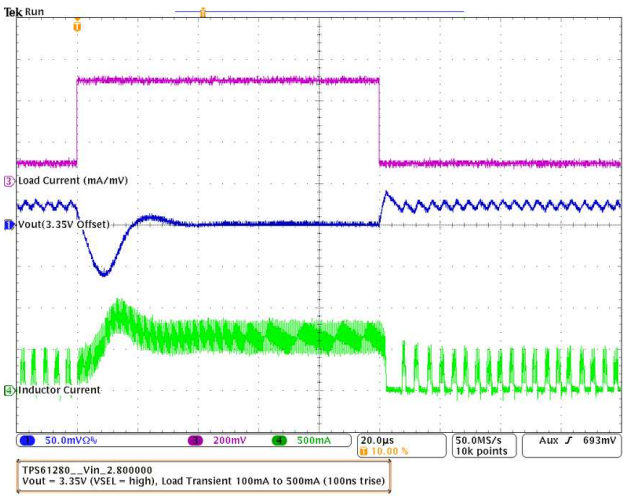



**Figure 51. TPS61280D, 81A Load Transient Response In PFM/PWM Operation**

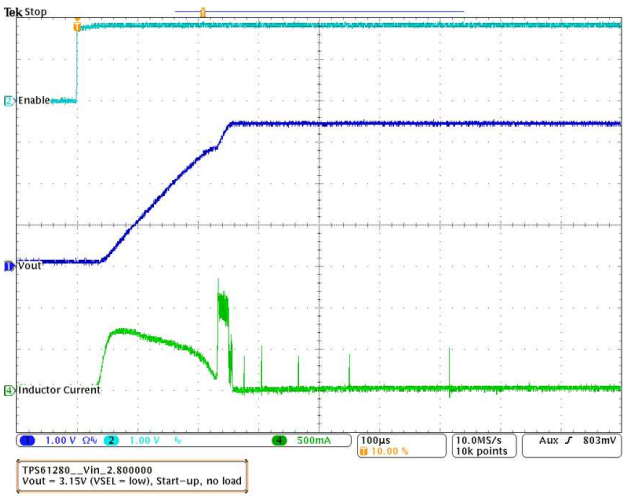



**Figure 52. Start-Up at No Load**

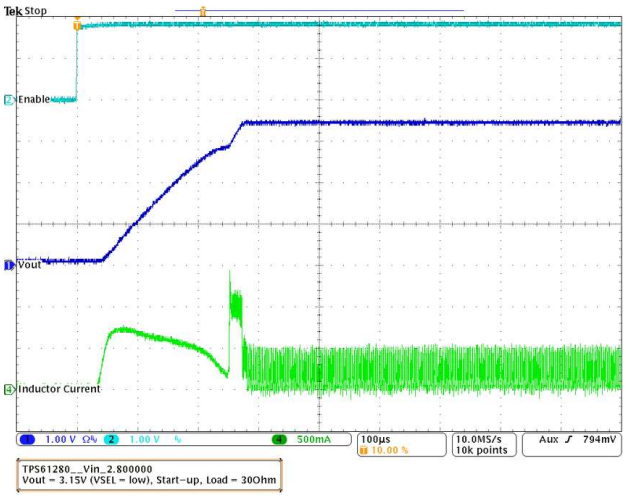



**Figure 53. Start-Up at 30-Ω Load**

### 10.2.2 TPS61282D with 2.5V-4.35 $V_{IN}$, 2000 mA Output Current (TPS61280D with $I^2C$ Programmable)

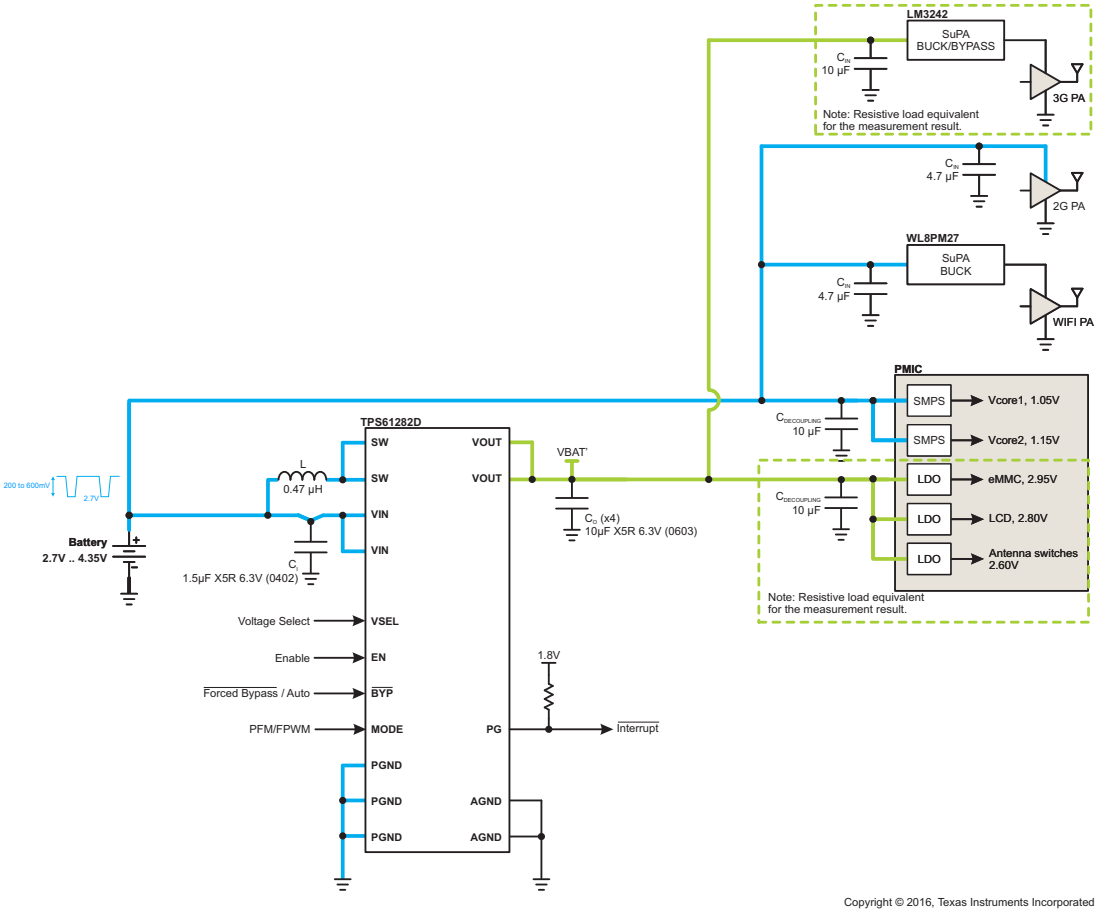



**Figure 54. TPS61282D Application Circuit with 2000 mA Output Current**

#### *10.2.2.1 Design Requirements*

**Table 13. Design Parameters**

| REFERENCE | DESCRIPTION | PART NUMBER, MANUFACTURER |
|---|---|---|
| $V_{IN}$ | Input voltage range | 2.5 V to 4.35 V |
| $V_{OUT}$ | Output voltage range at $V_{SEL}$=Low | $V_{OUT}$ = 3.3 V if $V_{IN} \le 3.3$ V, $V_{OUT}$= $V_{IN}$ if $V_{IN} > 3.3$ V |
| $V_{OUT}$ | Output voltage range $V_{SEL}$=High | $V_{OUT}$ = 3.5 V if $V_{IN} \le 3.5$ V, $V_{OUT}$= $V_{IN}$ if $V_{IN} > 3.5$ V |
| $I_{OUT}$ | Output Current | 2000 mA |

**Table 14. Component List**

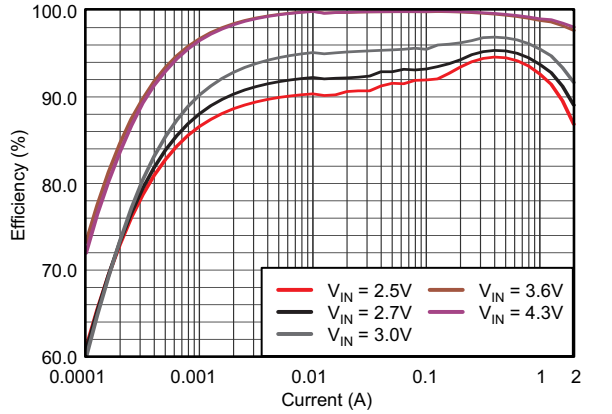
| REFERENCE | DESCRIPTION | PART NUMBER, MANUFACTURER(1) |
|---|---|---|
| $C_I$ | 1.5 µF, 6.3 V, 0402, X5R ceramic | GRM155R60J155ME80D |
| $C_O$ | 4 x 10 µF, 6.3 V, 0603, X5R ceramic | 4 x GRM188R60J106ME84 |
| L | 470 nH, 47 mΩ, 2.5 mm x 2.0 mm x 1.2 mm | DFE252012CR470 |

(1) See *Third-Party Products Disclaimer*

#### *10.2.2.2 Detailed Design Procedures*

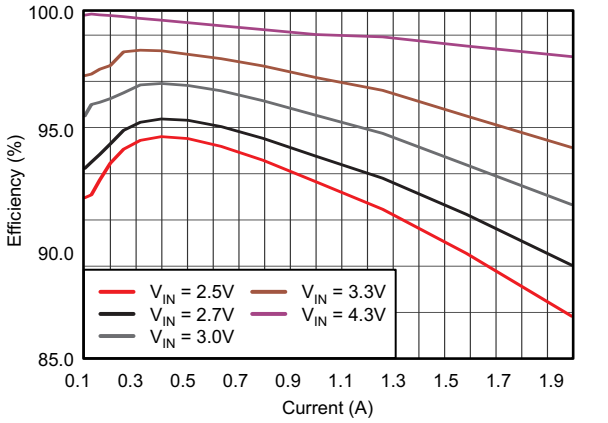
See *TPS61281D with 2.5V-4.35 $V_{IN}$, 1500 mA Output Current (TPS61280D with default $I^2C$ Configuration)* for all Detailed Design Procedures.

### 10.2.2.3 Application Performance Curves



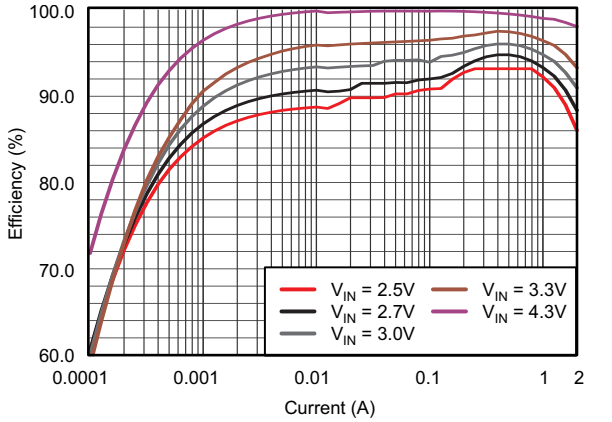

$V_{OUT}$ = 3.3 V VSEL = Low Mode = Low

**Figure 55. TPS61282D Efficiency vs Output Current**



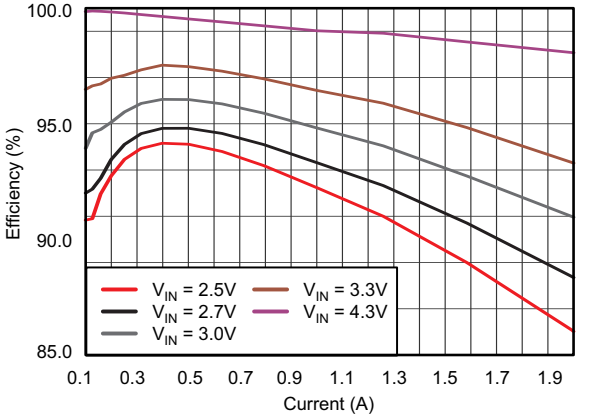

$V_{OUT}$ = 3.3 V VSEL = Low Mode = Low

**Figure 56. TPS61282D Efficiency vs Output Current**



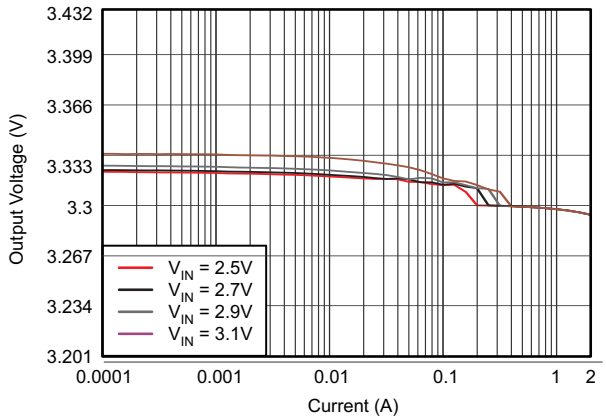

$V_{OUT}$ = 3.5 V VSEL = High Mode = Low

**Figure 57. TPS61282D Efficiency vs Output Current**



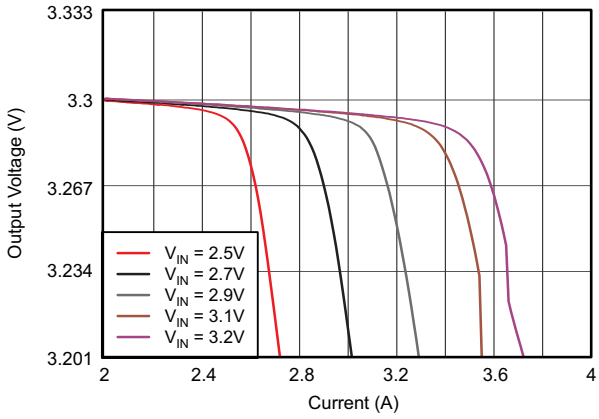

$V_{OUT}$ = 3.5 V VSEL = High Mode = Low

**Figure 58. TPS61282D Efficiency vs Output Current**




$V_{OUT}$ = 3.3 V Mode = Low

**Figure 59. TPS61282D DC Output Voltage vs Output Current**




$V_{OUT}$ = 3.3 V Mode = Low

**Figure 60. TPS61282D DC Output Voltage vs Output Current**

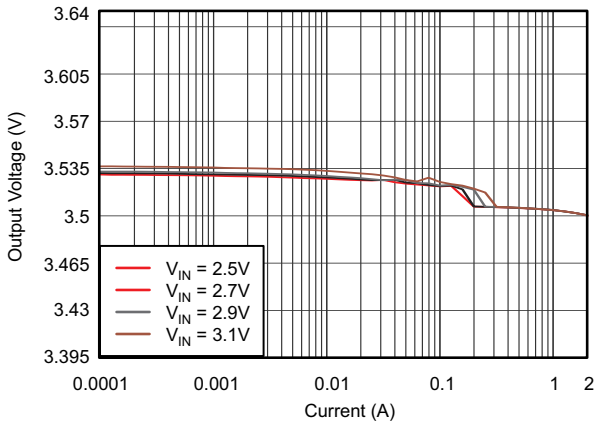



**Figure 61. TPS61282D DC Output Voltage vs Output Current**

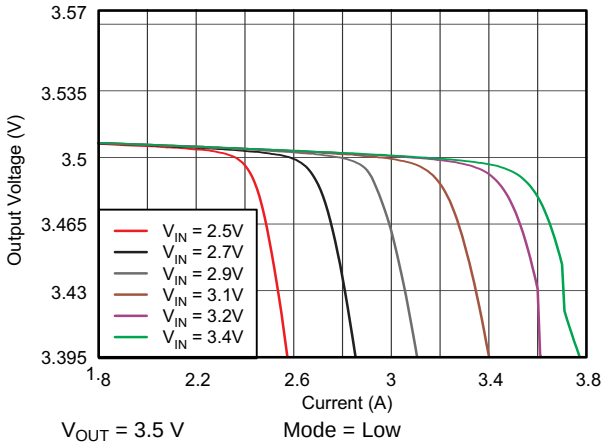



**Figure 62. TPS61282D DC Output Voltage vs Output Current**

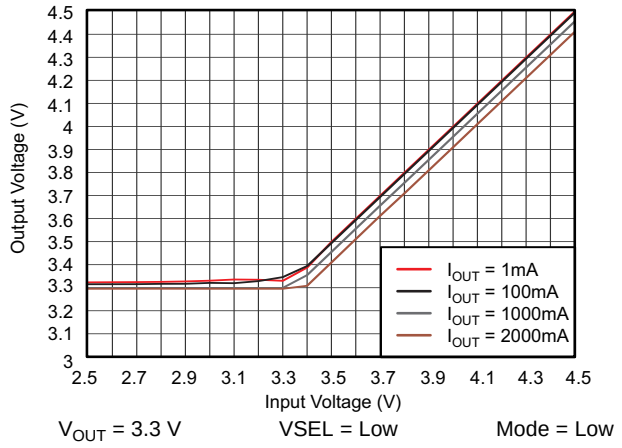



**Figure 63. TPS61282D DC Output Voltage vs Input Voltage**

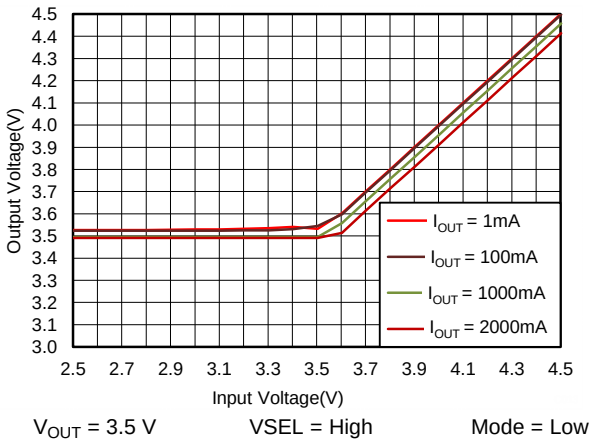



**Figure 64. TPS61282D DC Output Voltage vs Input Voltage**

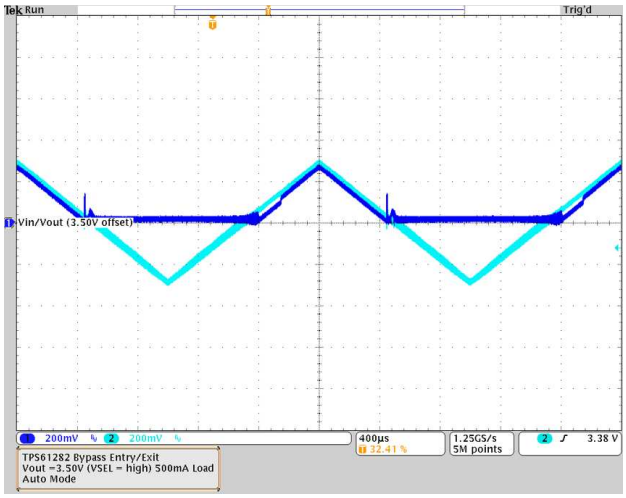



**Figure 65. Boost to Pass-Through Mode Exit / Entry**

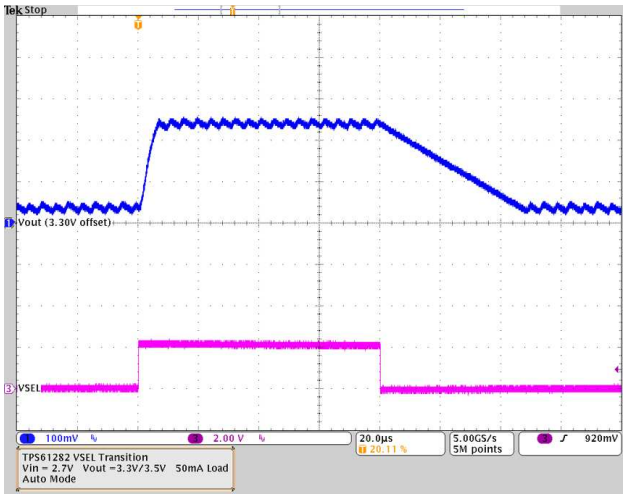



**Figure 66. TPS61282D Dynamic Voltage Management (VSEL) Load Current 50mA**

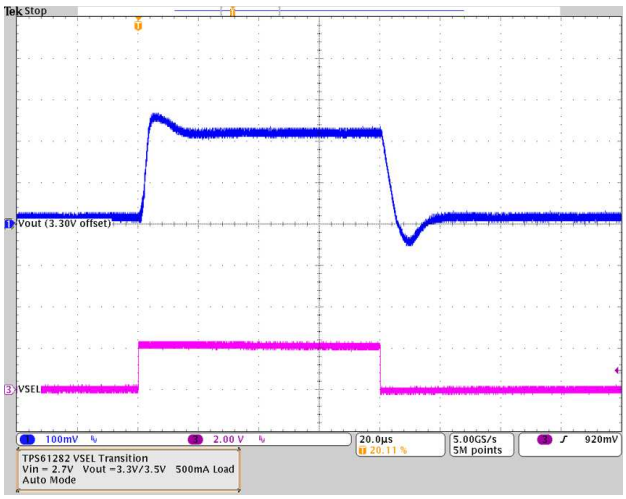



**Figure 67. TPS61282D Dynamic Voltage Management (VSEL) Load Current 500mA**

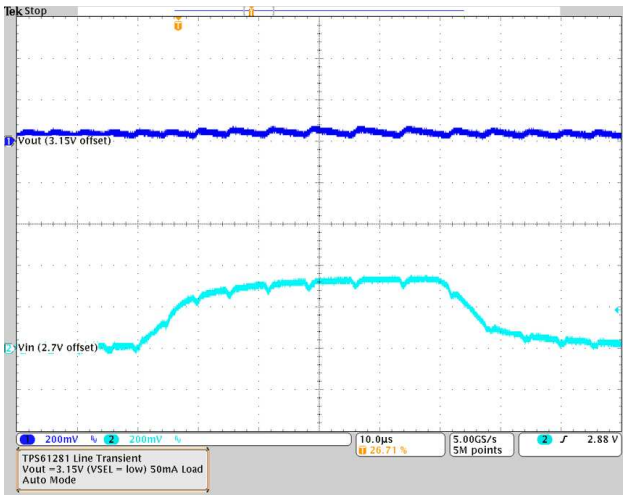



**Figure 68. TPS61282D Line Transient**

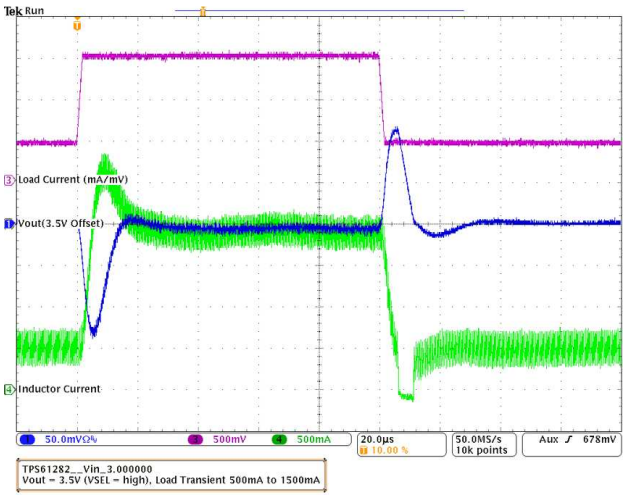



**Figure 69. TPS61282D Load Transient Response In PWM Operation**

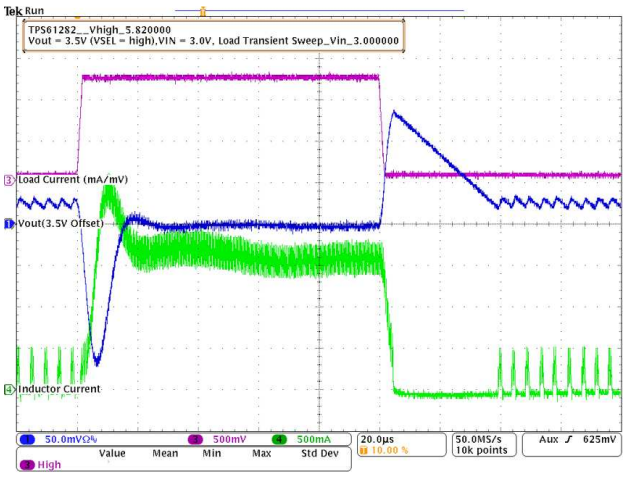



**Figure 70. TPS61282D Load Transient Response In PFM/PWM Operation**

# 11 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.3 V and 4.8 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS61280D, TPS61281D or TPS61282D converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 μF is a typical choice.

# 12 Layout

## 12.1 Layout Guidelines

- For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies.
- If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.
- Therefore, use wide and short traces for the main current path and for the power ground tracks.
- To minimize voltage spikes at the converter's output:
  - Place the output capacitor(s) as close as possible to GND and $V_{OUT}$, as shown in Figure 71.
  - The input capacitor and inductor should also be placed as close as possible to the IC.
  - Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise.
  - Connect these ground nodes at any place close to the ground pins of the IC.
  - Junction-to-ambient thermal resistance is highly application and board-layout dependent.
  - It is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill available PWB surface area and tied to internal layers with a cluster of thermal vias.

## 12.2 Layout Example

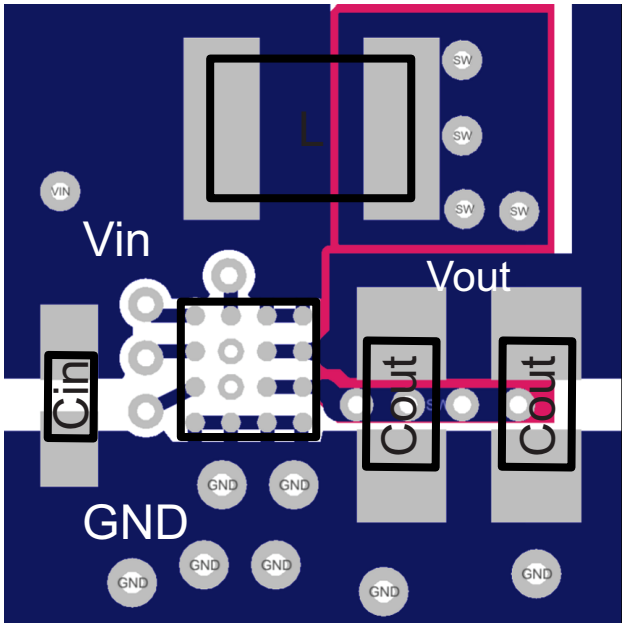



**Figure 71. Suggested Layout (Top)**

## 12.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and solution size. Due to integration and miniaturization, junction temperature can increase significantly which could lead to bad application behaviors (that is, premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The device operating junction temperature ($T_J$) should be kept below 125°C.

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Third-Party Products Disclaimer

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## 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.4 Trademarks

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$I^2C$ is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

## 13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 14.1 Package Summary

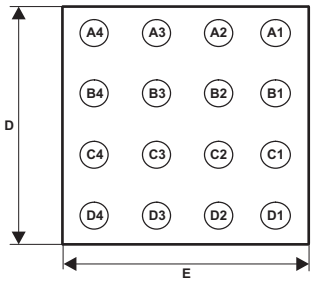



**Figure 72. Chip Scale Package (Bottom View)**


**Figure 73. Chip Scale Package (Top View)**

Code:

- YM — Year Month date code
- LLLL — Lot trace code
- S — Assembly site code

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61280DYFFR | ACTIVE | DSBGA | YFF | 16 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 61280D | Samples |
| TPS61280DYFFT | ACTIVE | DSBGA | YFF | 16 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 61280D | Samples |
| TPS61281DYFFR | ACTIVE | DSBGA | YFF | 16 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 61281D | Samples |
| TPS61281DYFFT | ACTIVE | DSBGA | YFF | 16 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 61281D | Samples |
| TPS61282DYFFR | ACTIVE | DSBGA | YFF | 16 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 61282D | Samples |
| TPS61282DYFFT | ACTIVE | DSBGA | YFF | 16 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 61282D | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

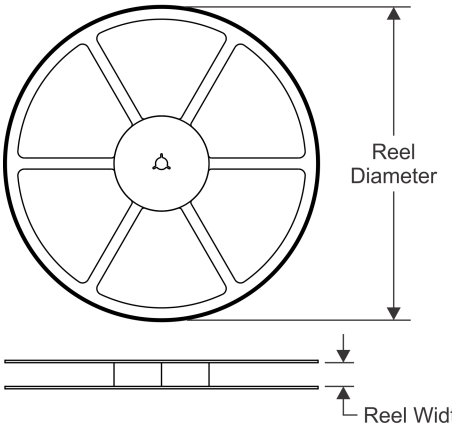
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

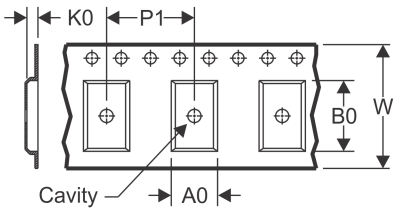
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

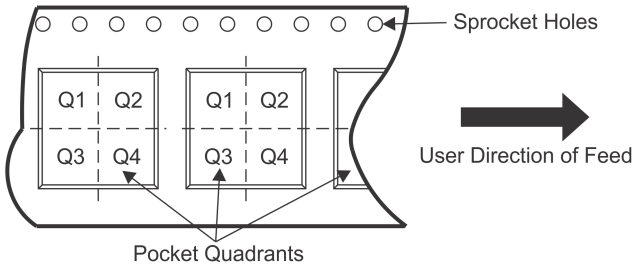



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

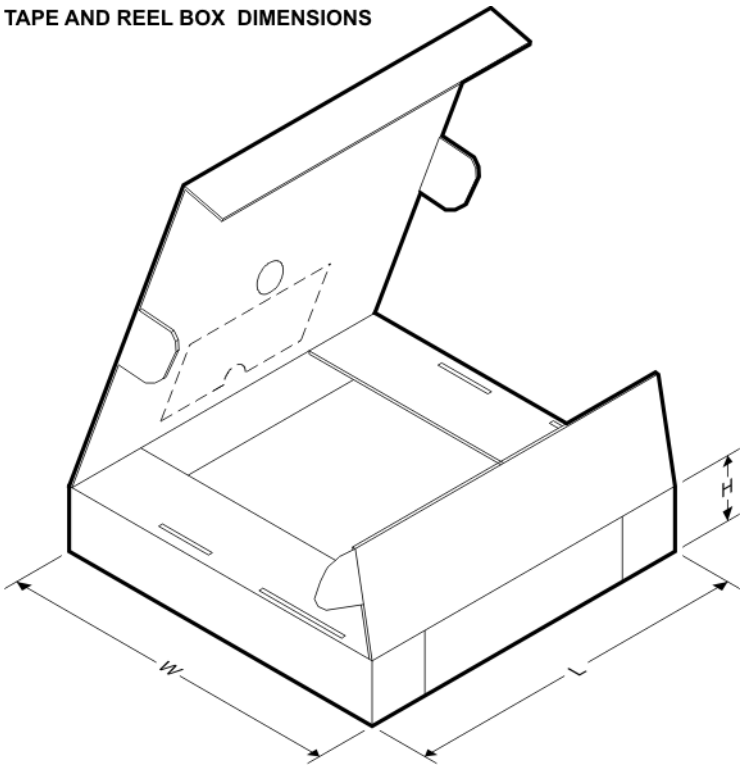
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61280DYFFR | DSBGA | YFF | 16 | 3000 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61280DYFFT | DSBGA | YFF | 16 | 250 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61281DYFFR | DSBGA | YFF | 16 | 3000 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61281DYFFT | DSBGA | YFF | 16 | 250 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61282DYFFR | DSBGA | YFF | 16 | 3000 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS61282DYFFT | DSBGA | YFF | 16 | 250 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

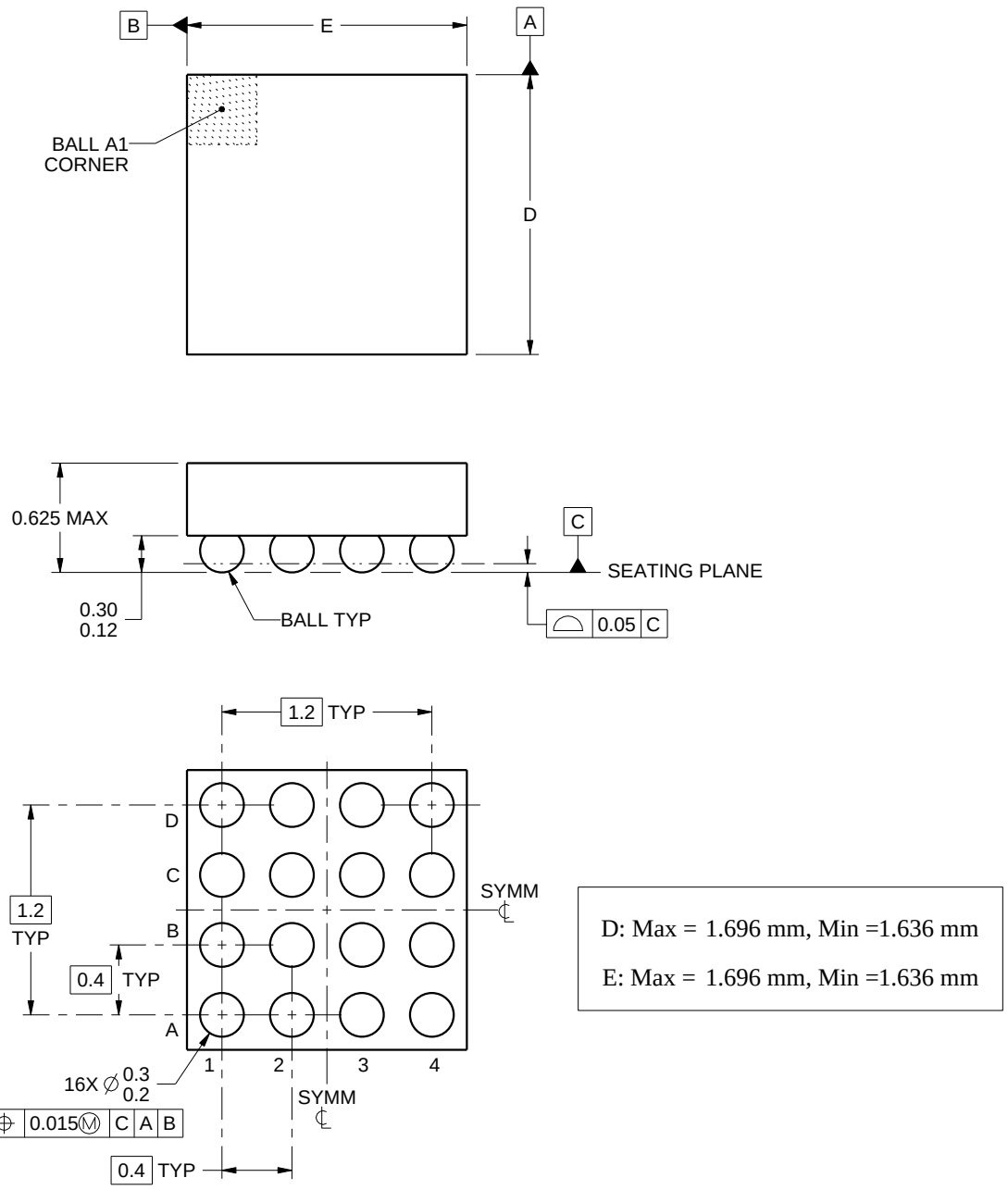
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS61280DYFFR | DSBGA | YFF | 16 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS61280DYFFT | DSBGA | YFF | 16 | 250 | 182.0 | 182.0 | 20.0 |
| TPS61281DYFFR | DSBGA | YFF | 16 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS61281DYFFT | DSBGA | YFF | 16 | 250 | 182.0 | 182.0 | 20.0 |
| TPS61282DYFFR | DSBGA | YFF | 16 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS61282DYFFT | DSBGA | YFF | 16 | 250 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## YFF0016

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY




4219386/A 05/2016

NOTES:

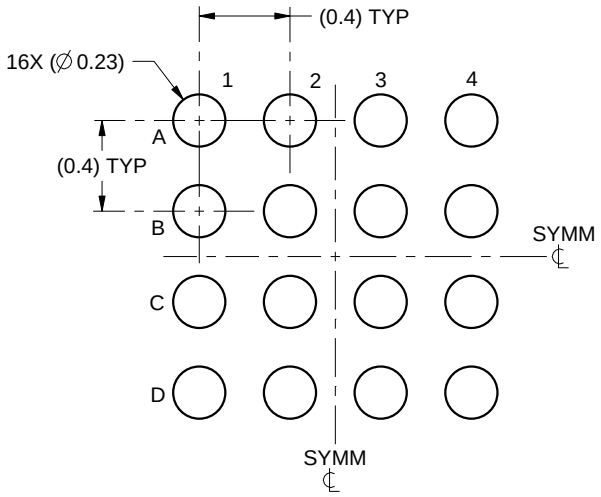
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

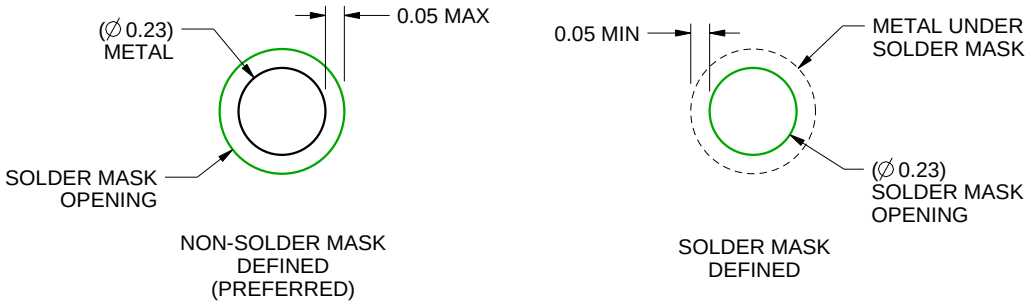
## YFF0016

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
SCALE:30X




SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

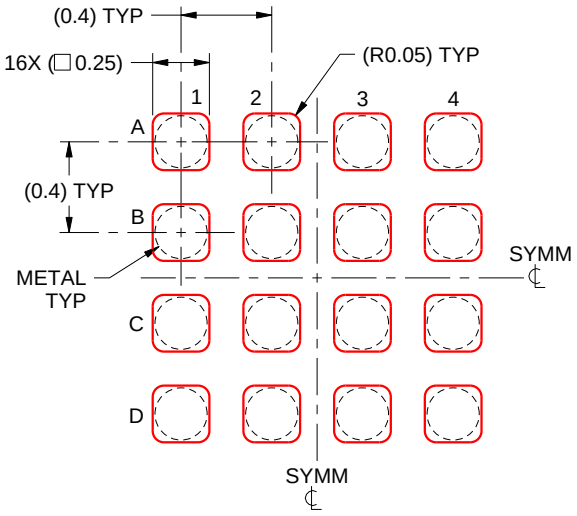
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YFF0016

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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