TPD3S0x4 Current Limit Switch and D+/D– ESD Protection for USB Host Ports

1 Features

- Continuous Current Ratings of 0.5 A and 1.5 A
- Fixed, Constant Current Limits of 0.85 A and 2.15 A (Typ)
- Fast Overcurrent Response – 2 µs
- Integrated Output Discharge
- Reverse Current Blocking
- Short-Circuit Protection
- Over Temperature Protection With Auto-Restart
- Built-In Soft Start
- Ambient Temperature Range: –40°C to 85°C
- Product Regulatory Compliance
  - UL Recognized Component (UL 2367, Standard for Solid State Overcurrent Protectors)
  - CB File No. E169910 to IEC 60950-1, Information Technology Equipment
- IEC 61000-4-2 Level 4 ESD Protection (External Pins)
  - ±12-kV Contact Discharge (IEC 61000-4-2)
  - ±15-kV Air Gap Discharge (IEC 61000-4-2)

2 Applications

- End Equipment:
  - Electronic Point of Sale (ESOP)
  - USB Hubs
  - Laptops, Desktops
  - High-Definition Digital TVs
  - Set-Top Boxes
- Interfaces:
  - USB Ports
  - 5-V Power Rails

3 Description

The TPD3S0x4s are integrated devices that feature a current-limited load switch and a two-channel transient voltage suppressor (TVS) based electrostatic discharge (ESD) protection diode array for USB interfaces.

The TPD3S0x4 devices are intended for applications such as USB where heavy capacitive loads and short-circuits are likely to be encountered; TPD3S0x4s provide short-circuit protection and overcurrent protection. The TPD3S0x4s limit the output current to a safe level by operating in constant current mode when the output load exceeds the current limit threshold. The fast overload response eases the burden on the main 5-V power supply by quickly regulating the power when the output is shorted. The rise and fall times for the current limit switch are controlled to minimize current surges when turning the device on and off.

The TPD3S014 and TPD3S044 will allow 0.5 A and 1.5 A of continuous current, respectively. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard.

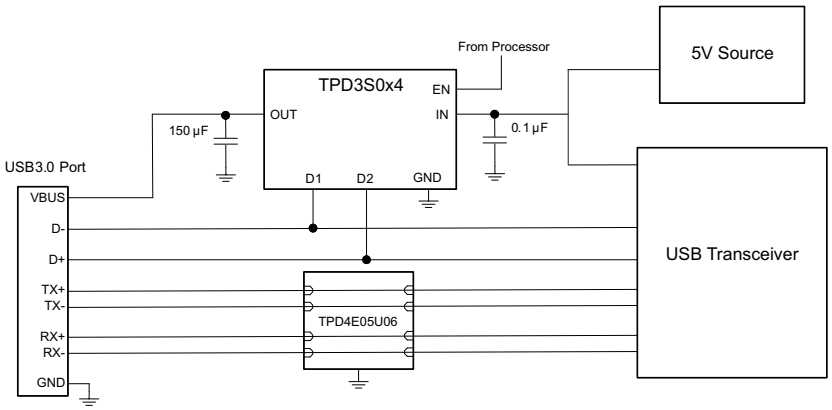
The high level of integration, combined with its easy-to-route DBV package, allows this device to provide great circuit protection for USB interfaces in applications like laptops, high-definition digital TVs, set-top boxes, and electronic point of sale equipment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3S0x4	DBV (6)	2.90 mm × 2.80 mm × 1.45 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2015) to Revision B — **Page**

- Added electronic point of sale to applications ... 1
- Added package height ... 1
- Added EN values to *Design Requirements* ... 16
- Added *Implementing Active Low Logic* section to show using EN as active low ... 17
- Moved *Power Dissipation and Junction Temperature* to the *Layout* section ... 21
- Added *Community Resources* ... 23

Changes from Original (October 2014) to Revision A — **Page**

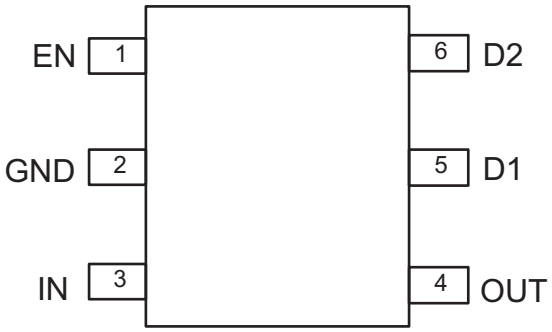
- Updated document to full version datasheet. ... 1

5 Device Comparison Table

PART NUMBER	MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE	PACKAGED DEVICE AND MARKING SOT23-6 (DBV)
TPD3S014	0.5 A	Y	High	SII
TPD3S044	1.5 A	Y	High	SIJ

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
D1	5	USB data+ or USB data–
D2	6	
EN	1	Enable input, logic high turns on power switch
GND	2	Ground
IN	3	Input voltage and power-switch drain; Connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	4	Power-switch output, connect to load

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage(3)	V_{IN}	–0.3	6	V
	V_{OUT}	–0.3	6	
	EN	–0.3	6	
	D1	–0.3	6	
	D2	–0.3	6	
Voltage from V_{IN} to V_{OUT}		–6	6	V
Junction temperature, T_J		Internally limited		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.
(3) See the *Input and Output Capacitance* section.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±500	
		IEC 61000-4-2 contact discharge(3)	V_{OUT}, Dx pins	±12000	
		IEC 61000-4-2 air-gap discharge(3)	V_{OUT}, Dx pins	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.
(3) V_{OUT} was tested on a PCB with input and output bypassing capacitors of 0.1 µF and 120 µF, respectively.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5		5.5	V
V_{EN}	Input voltage, EN	0		5.5	V
V_{IH}	High-level Input voltage, EN	2			V
V_{IL}	Low-level Input voltage, EN			0.7	V
C_{IN}	Input decoupling capacitance, IN to GND	0.1			µF
I_{OUT}(1)	Continuous output current (TPD3S014)			0.5	A
	Continuous output current (TPD3S044)			1.5	
T_J	Operating junction temperature	–40		125	°C

(1) Package and current ratings may require an ambient temperature derating of 85°C

7.4 Thermal Information

THERMAL METRIC[1][2]		TPD3S0x4 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W
$R_{\theta JA}$(Custom)	See the *Power Dissipation and Junction Temperature* section	120.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) See *Device Comparison Table*.

7.5 Electrical Characteristics: $T_J = T_A = 25°C$

Unless otherwise noted: V_{IN} = 5 V, $V_{EN} = V_{IN}$, I_{OUT} = 0 A. See *Device Comparison Table* for the rated current of each part number. Parametrics over a wider operational range are shown in the second *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C* table.

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Input – Output resistance	TPD3S014		97	110	mΩ
		TPD3S014: –40°C ≤ (T_J, T_A) ≤ 85°C		96	130	
		TPD3S044		74	91	
		TPD3S044: –40°C ≤ (T_J, T_A) ≤ 85°C		74	106	
CURRENT LIMIT						
I_{OS}[2]	Current limit, see Figure 27	TPD3S014	0.67	0.85	1.01	A
		TPD3S044	1.70	2.15	2.50	
SUPPLY CURRENT						
I_{SD}	Supply current, switch disabled	I_{OUT} = 0A		0.02	1	µA
		–40°C ≤ (T_J, T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A			2	
I_{SE}	Supply current, switch enabled	I_{OUT} = 0A		66	74	µA
		–40°C ≤ (T_J, T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A			85	
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V, Measure I_{VOUT}		0.2	1	µA
		–40°C ≤ (T_J, T_A) ≤ 85°C, V_{OUT} = 5 V, V_{IN} = 0 V, measure IV_{OUT}			5	
OUTPUT DISCHARGE						
R_{PD}	Output pull-down resistance[3]	$V_{IN} = V_{OUT}$ = 5 V, disabled	400	456	600	Ω
ESD PROTECTION						
ΔC_{IO}	Differential capacitance between the D1, D2 lines	f = 1 MHz, V_{IO} = 2.5 V		0.02		pF
C_{IO}	(D1, D2 to GND)	f = 1 MHz, V_{IO} = 2.5 V		1.4		pF
R_{DYN}	Dynamic on-resistance D1, D2 IEC clamps[4]	Dx to GND		0.2		Ω
		GND to Dx				

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See *Current Limit* for explanation of this parameter.
(3) These Parameters are provided for reference only, and do not constitute a part of TI's published device specifications for purposes of TI's product warranty.
(4) RDYN was extracted using the least squares first of the TLP characteristics between I = 20 A and I = 30 A.

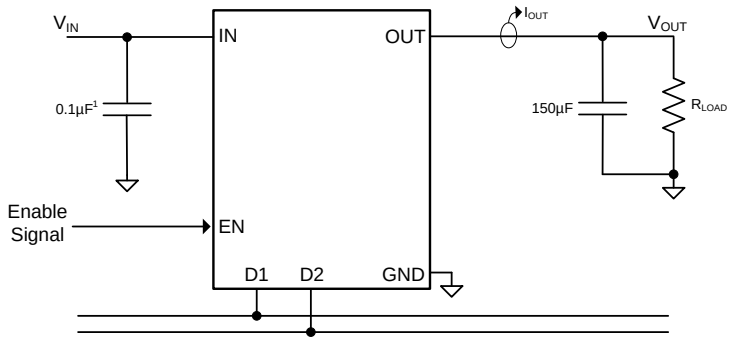
7.6 Electrical Characteristics: –40°C ≤ T_J ≤ 125°C

Unless otherwise noted: 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, I_{OUT} = 0 A, typical values are at 5 V and 25°C. See the *Device Comparison Table* for the rated current of each part number.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Input – output resistance	TPD3S014		97	154	mΩ
		TPD3S044		74	121	
ENABLE INPUT (EN)						
	Threshold	Input rising	1	1.45	2	V
	Hysteresis			0.13		V
	Leakage current	V_{EN} = 0 V	–1	0	1	µA
t_{ON}	Turn on time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↑ See Figure 26	1	1.6	2.2	ms
t_{OFF}	Turn off time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↓ See Figure 26	1.7	2.1	2.7	ms
t_R	Rise time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V, See Figure 25	0.4	0.64	0.9	ms
t_F	Fall time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V, See Figure 25	0.25	0.4	0.8	ms
CURRENT LIMIT						
I_{OS}(2)	Current limit, see Figure 27	TPD3S014	0.65	0.85	1.05	A
		TPD3S044	1.60	2.15	2.70	
t_{IOS}	Short-circuit response time(3)	V_{IN} = 5 V (see Figure 27) One Half full load → R_{SHORT} = 50 mΩ Measure from application to when current falls below 120% of final value		2		µs
SUPPLY CURRENT						
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A		0.02	10	µA
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A		66	94	µA
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, Measure I_{VOUT}		0.2	20	µA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Rising threshold	V_{IN}↑	3.5	3.77	4	V
	Hysteresis	V_{IN}↓		0.14		V
OUTPUT DISCHARGE						
R_{PD}	Output pull-down resistance	V_{IN} = 4 V, V_{OUT} = 5 V, Disabled	350	545	1200	Ω
		V_{IN} = 5 V, V_{OUT} = 5 V, Disabled	300	456	800	
THERMAL SHUTDOWN						
T_{SHDN}	Rising threshold (T_J)	In current limit	135			°C
		Not in current limit	155			
	Hysteresis(3)			20		°C
ESD PROTECTION						
I_I	Input leakage current (D1, D2)	V_I = 3.3 V		0.02	1	µA
V_D	Diode forward voltage (D1, D2); Lower clamp diode	I_O = 8 mA			0.95	V
V_{BR}	Breakdown voltage (D1, D2)	I_{BR} = 1 mA	6			V

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See *Current Limit* section for explanation of this parameter.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Typical Characteristics



(1) During the short applied tests, 300µF is used because of the use of an external supply.

Figure 1. Test Circuit for System Operation in Typical Characteristics

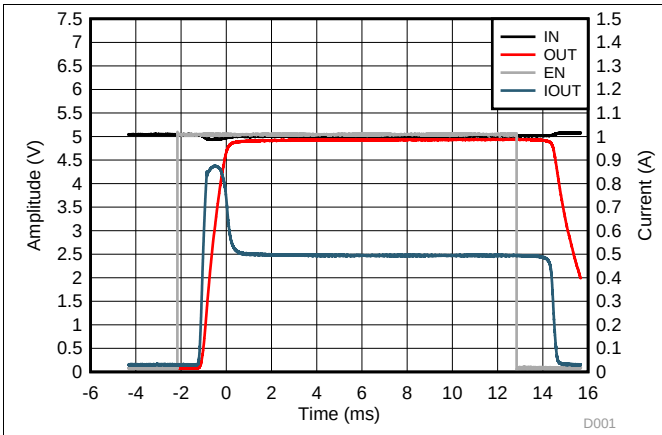


Figure 2. TPD3S014 Turn ON into 10 Ω

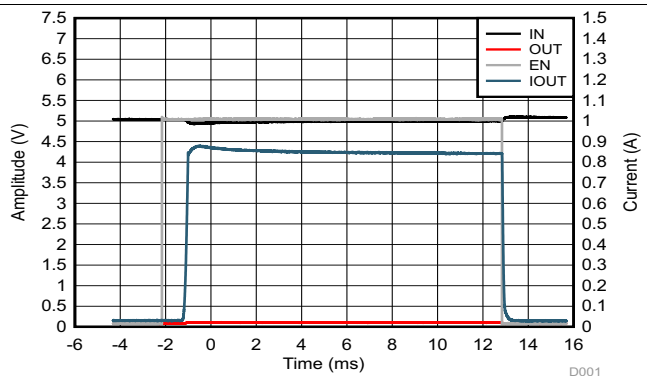


Figure 3. TPD3S014 Enable into Short

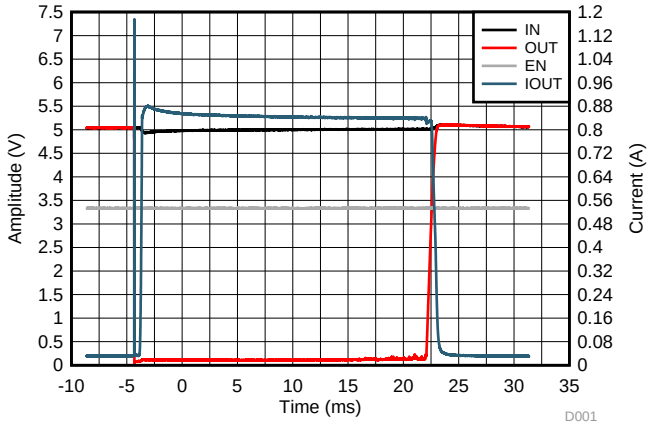


Figure 4. TPD3S014 Pulsed Output Short

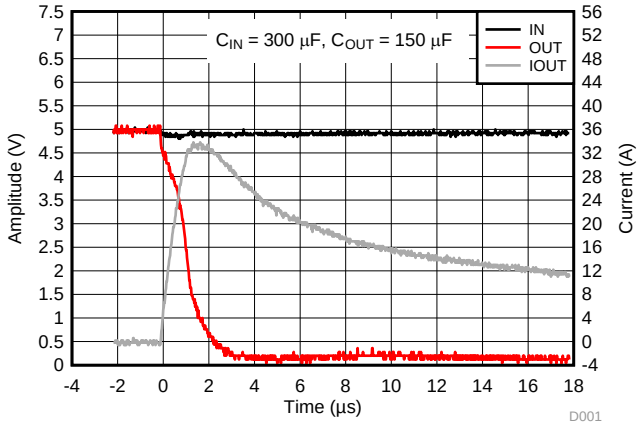


Figure 5. TPD3S014 Short Applied

Typical Characteristics (continued)

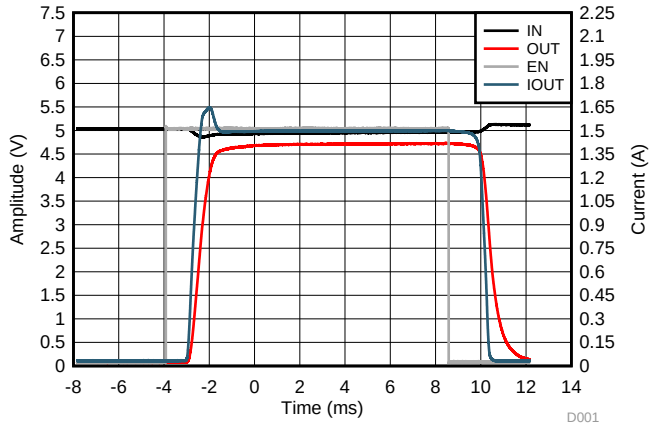


Figure 6. TPD3S044 Turn-On into 3.3 Ω

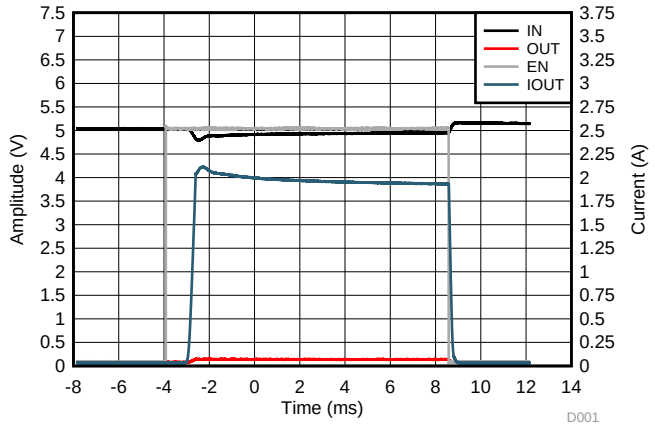


Figure 7. TPD3S044 Enable into Short

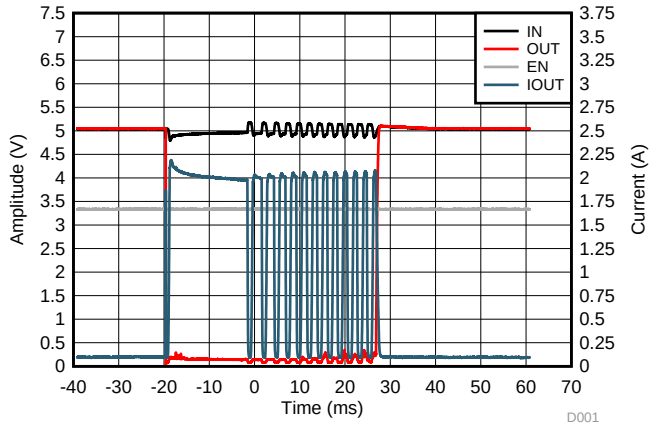


Figure 8. TPD3S044 Pulsed Output Short

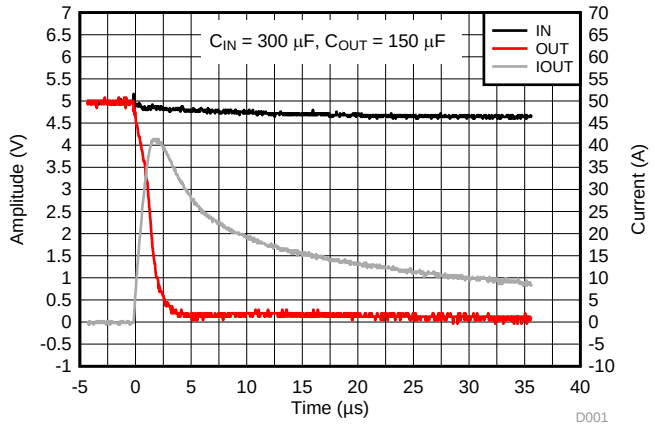


Figure 9. TPD3S044 Short Applied

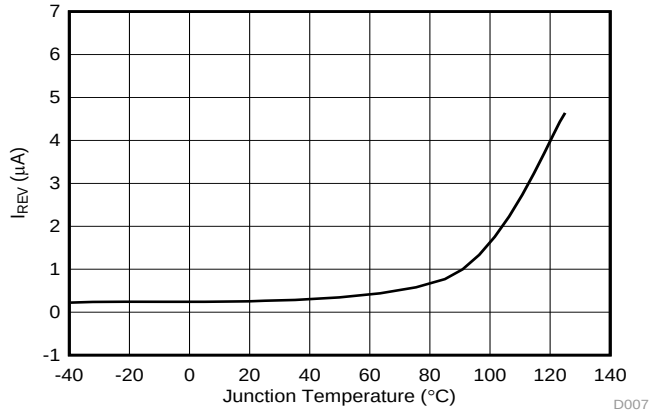


Figure 10. Reverse Leakage Current (I_{REV}) vs Temperature

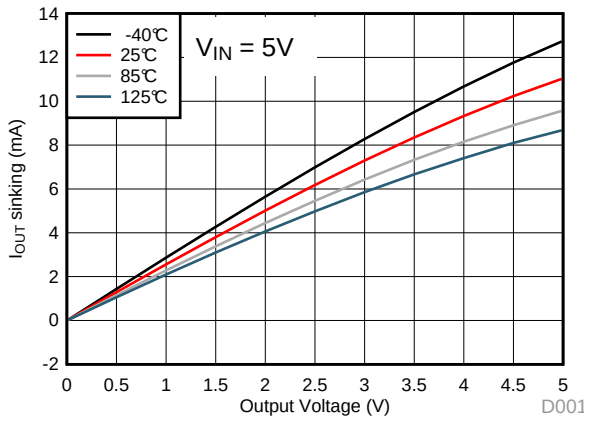


Figure 11. Output Discharge Current vs Output Voltage

Typical Characteristics (continued)

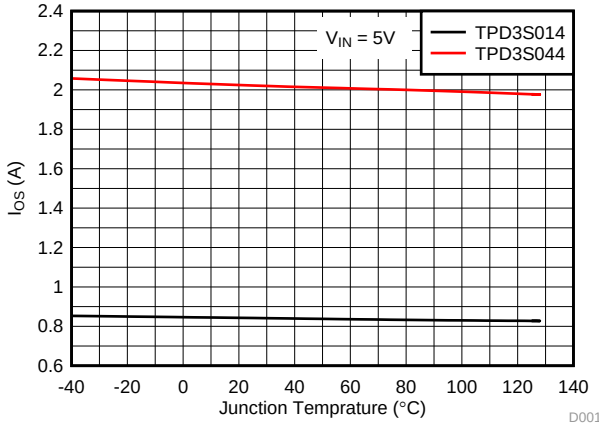


Figure 12. Short Circuit Current (I_{OS}) vs Temperature

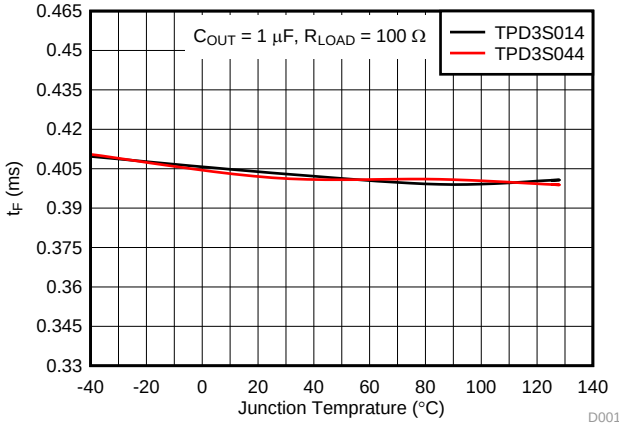


Figure 13. Output Fall Time (t_F) vs Temperature

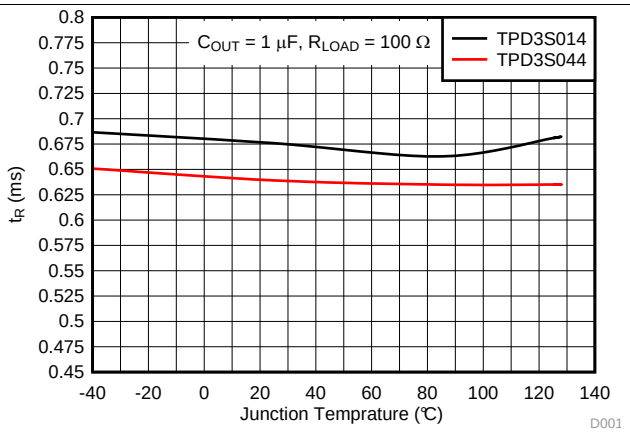


Figure 14. Output Rise Time (t_R) vs Temperature

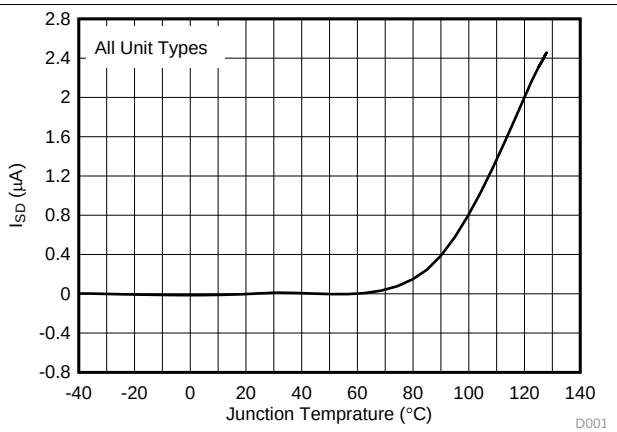


Figure 15. Disabled Supply Current (I_{SD}) vs Temperature

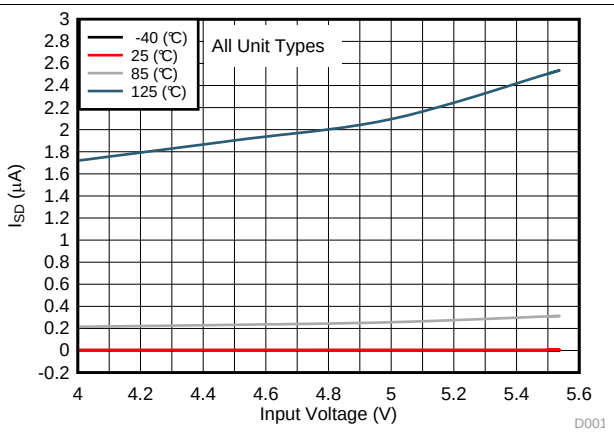


Figure 16. Disabled Supply Current (I_{SD}) vs Input Voltage

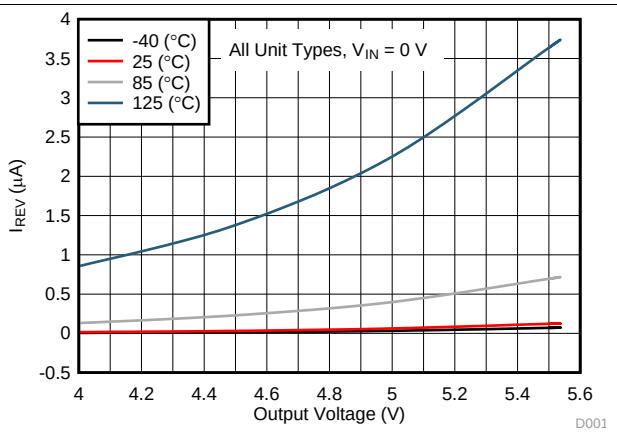


Figure 17. Reverse Leakage Current (I_{REV}) vs Output Voltage

Typical Characteristics (continued)

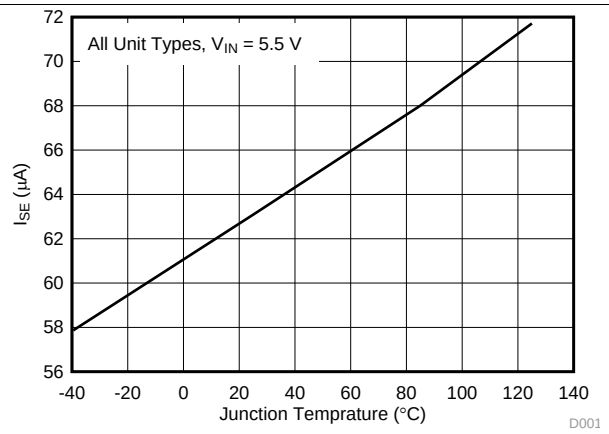


Figure 18. Enabled Supply Current (I_{SE}) vs Temperature

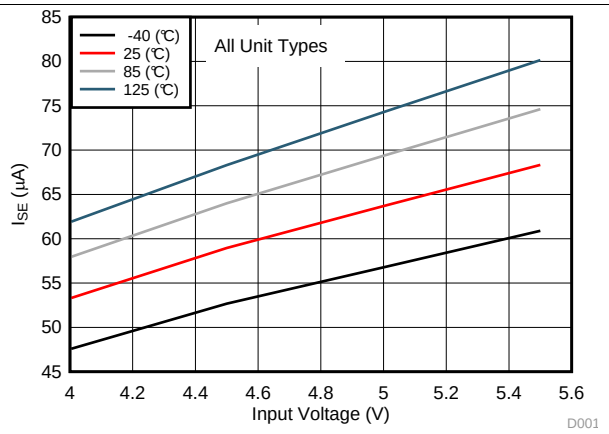


Figure 19. Enabled Supply Current (I_{SE}) vs Input Voltage

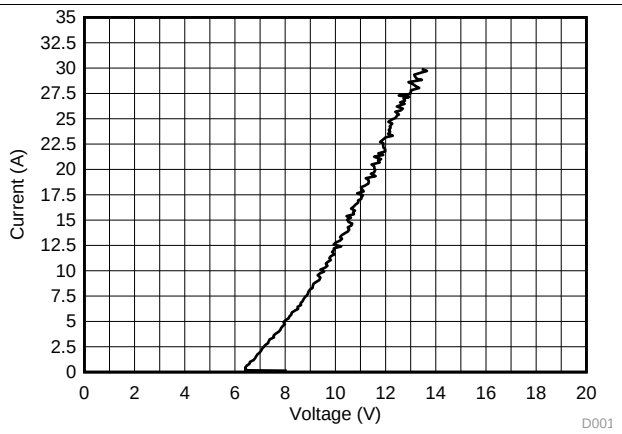


Figure 20. TPD3S044 D1/D2 Positive TLP Curve

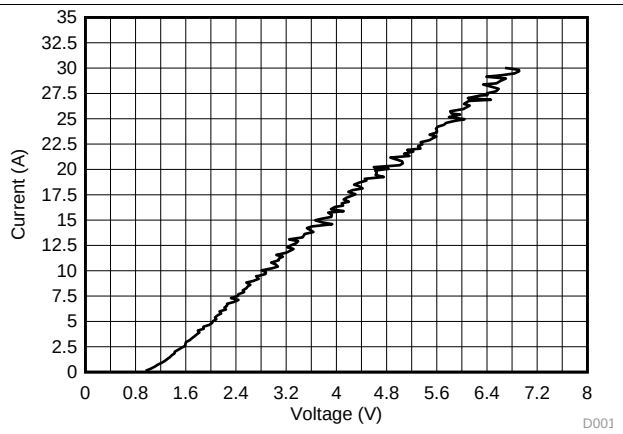


Figure 21. TPD3S044 D1/D2 Negative TLP Curve

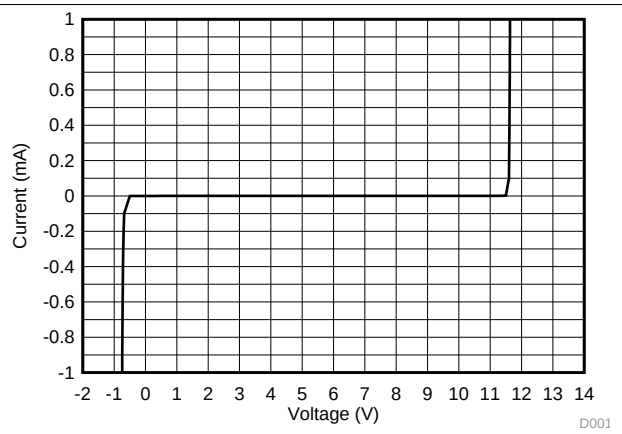


Figure 22. D1/D2 I-V Curve

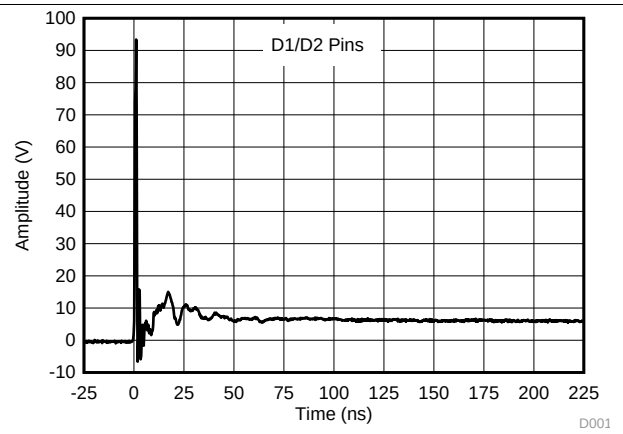


Figure 23. D1/D2 IEC61000-4-2 +8-kV Contact

Typical Characteristics (continued)

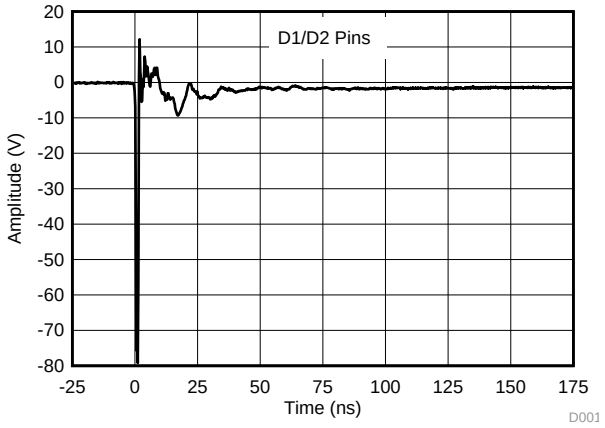


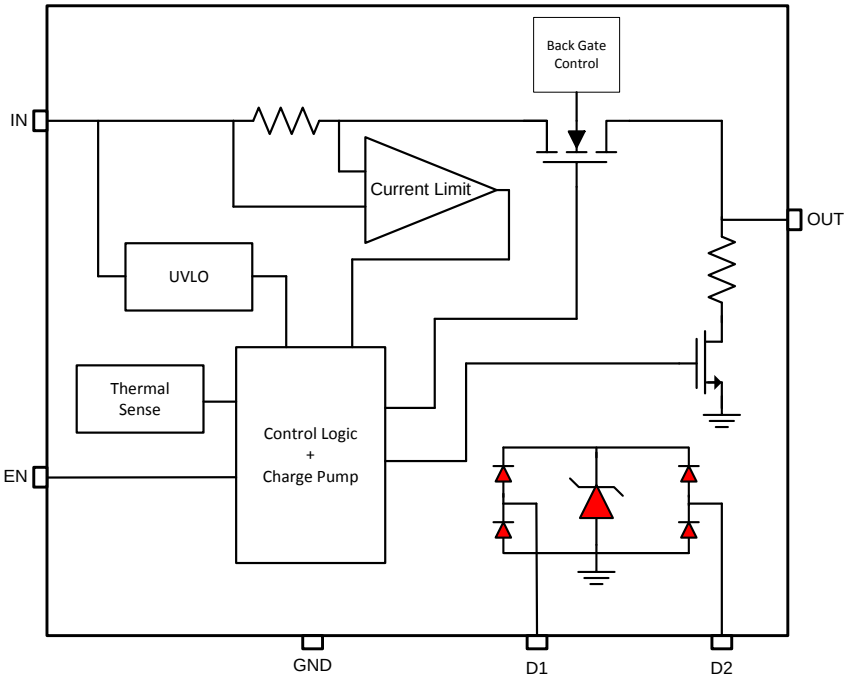
Figure 24. D1/D2 IEC61000-4-2 –8-kV Contact

8 Detailed Description

8.1 Overview

The TPD3S0x4 are highly integrated devices that feature a current limited load switch and a two-channel TVS based ESD protection diode array for USB interfaces. The TPD3S014 and TPD3S044 provide 0.5 A and 1.5 A, respectively, of continuous load current in 5-V circuits. These parts use N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. It is designed for applications where short circuits or heavy capacitive loads will be encountered. Device features include enable, reverse blocking when disabled, output discharge pull-down, overcurrent protection, and overtemperature protection. Finally, with two channels of TVS ESD protection diodes integrated, TPD3S0x4s provide system level ESD protection to all the pins of the USB port.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The UVLO circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

8.3.2 Enable

The logic enable input (EN) controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPD3S0x4s are disabled. The enable input is compatible with both TTL and CMOS logic levels.

The turn on and turn off times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPD3S0x4s and the external loading (especially capacitance). TPD3S0x4s fall time is controlled by the loading (R and C), and the output discharge (R_{PD}). An output load consisting of only a resistor will experience a fall time set by the TPD3S0x4s. An output load with parallel R and C elements will experience a fall time determined by the (R × C) time constant if it is longer than the TPD3S0x4's t_F. See Figure 25 and Figure 26 for a pictural description of t_R, t_F, t_{ON}, and t_{OFF}. The enable should not be left open; it may be tied to VIN.

Feature Description (continued)

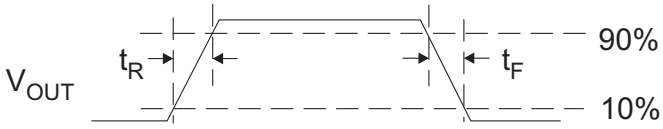


Figure 25. Power-On and Power-Off Timing

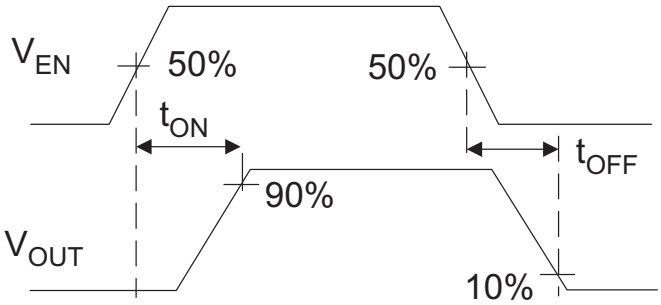


Figure 26. Enable Timing, Active-High Enable

8.3.3 Internal Charge Pump

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch will block current from OUT to IN when turned off by the UVLO or disabled.

8.3.4 Current Limit

The TPD3S0x4s respond to overloads by limiting output current to the static current-limit (IOS) levels shown in the *Electrical Characteristics: $T_J = T_A = 25°C$* table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by ($I_{OS} \times R_{LOAD}$). Two possible overload conditions can occur.

The first overload condition occurs when either:

1. The input voltage is first applied, enable is true, and a short circuit is present (load which draws $I_{OUT} > I_{OS}$) or
2. The input voltage is present and the TPD3S0x4s are enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPD3S0x4s ramp the output current to IOS. The TPD3S0x4s will limit the current to IOS until the overload condition is removed or the device begins to thermal cycle. The device subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} (Figure 27 and Figure 28) when the specified overload (per Electrical Characteristics table) is applied. The response speed and shape will vary with the overload level, input circuit, and rate of application. The current-limit response will vary between simply settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPD3S0x4s will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

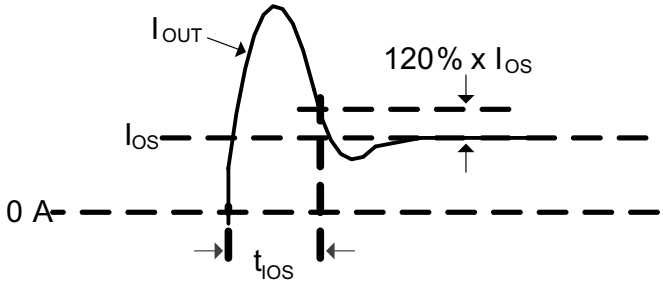


Figure 27. Output Short Circuit Parameters

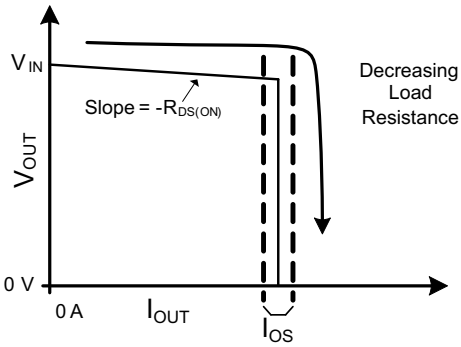


Figure 28. Output Characteristic Showing Current Limit

Feature Description (continued)

The TPD3S0x4s thermal cycle if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) × I_{OS}] driving the junction temperature up. The devices turn off when the junction temperature exceeds 135°C (min) while in current limit. The devices remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products similar to the TPD3S0x4s. Many older designs have an output I vs V characteristic similar to the plot labeled "Current Limit with Peaking" in Figure 29. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPD3S0x4 parts do not present noticeable peaking in the current limit, corresponding to the characteristic labeled "Flat Current Limit" in Figure 29. This is why the I_{OC} parameter is not present in the *Electrical Characteristics* tables.

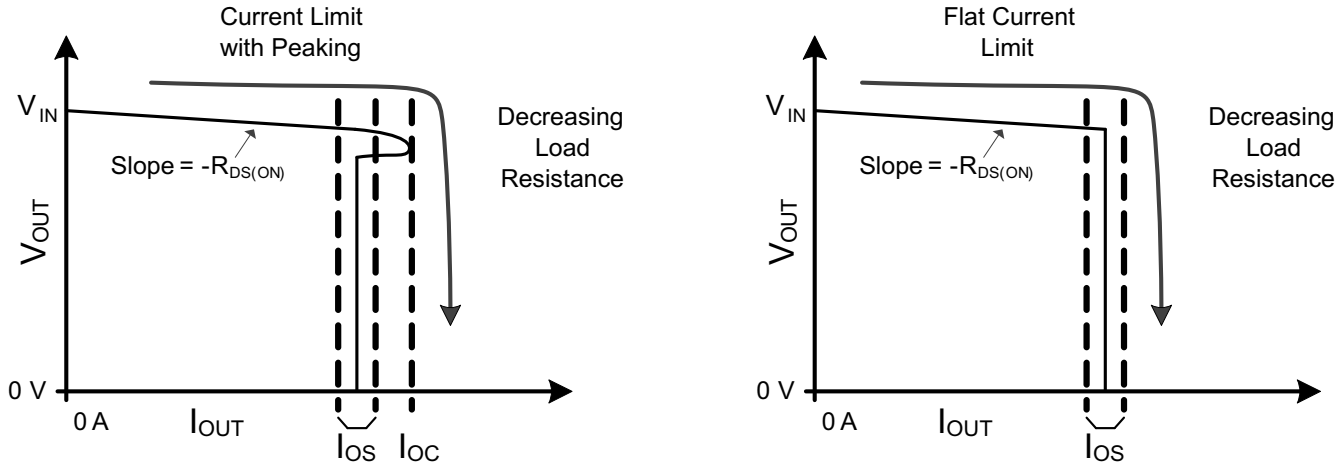


Figure 29. Current Limit Profiles

8.3.5 Output Discharge

A 470-Ω (typical) output discharge resistance will dissipate stored charge and leakage current on OUT when the TPD3S0x4s are in UVLO or disabled. The pull-down circuit will lose bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V.

8.3.6 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1 µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits such as the TPD3S0x4s will have the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turn on). Theoretically, the peak voltage is 2 times the applied. The second cause is due to the abrupt reduction of output short circuit current when the TPD3S0x4s turn off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPD3S0x4s outputs are shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current-limit speed of the TPD3S0x4s to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 to 22 µF adjacent to the TPD3S0x4s inputs aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

Feature Description (continued)

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPD3S0x4s have abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120 µF minimum output capacitance is required. Typically a 150-µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, a minimum of 10-µF ceramic capacitance on the output is recommended. The voltage undershoot should be controlled to less than 1.5 V for 10 µs.

8.4 Device Functional Modes

8.4.1 Operation With V_{IN} < 4 V (Minimum V_{IN})

These devices operate with input voltages above 4 V. The maximum UVLO voltage on IN is 4 V and the devices will operate at input voltages above 4 V. Any voltage below 4 V may not work with these devices. The minimum UVLO is 3.5 V, so some devices may work between 3.5 V and 4 V. At input voltages below the actual UVLO voltage, these devices will not operate.

8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.45 V typical and 2 V maximum. With EN held below that voltage the device is disabled and the load switch will be open. The IC quiescent current is reduced in this state. When the EN pin is above its rising edge threshold and the input voltage on the IN pin is above its UVLO threshold, the device becomes active. The load switch is closed, and the current limit feature is enabled. The output voltage on OUT will ramp up with the soft start value T_{ON} in order to prevent large inrush current surges on V_{BUS} due to a heavy capacitive load. When EN voltage is lowered below is falling edge threshold, the device output voltage will also ramp down with soft turn off value T_{OFF} to prevent large inductive voltages being presented to the system in the case a large load current is following through the device.

8.4.3 Operation of Level 4 IEC61000-4-2 ESD Protection

Regardless of which functional mode the devices are in, TPD3S0x4 will provide Level 4 IEC61000-4-2 ESD Protection on the pins of the USB connector.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TPD3S0x4 are devices that feature a current limited load switch and a two-channel TVS based ESD protection diode array. They are typically used to provide a complete protection solution for USB host ports. USB host ports are required by the USB specification to provide a current limit on the VBUS path in order to protect the system from overcurrent conditions on the port that could lead to system damage and user injury. Additionally, USB ports typically require system level IEC ESD protection due to direct end-user interaction. The following design procedure can be used to determine how to properly implement TPD3S0x4s in your systems to provide a complete, one-chip solution for your USB ports.

9.2 Typical Applications

9.2.1 USB2.0 Application

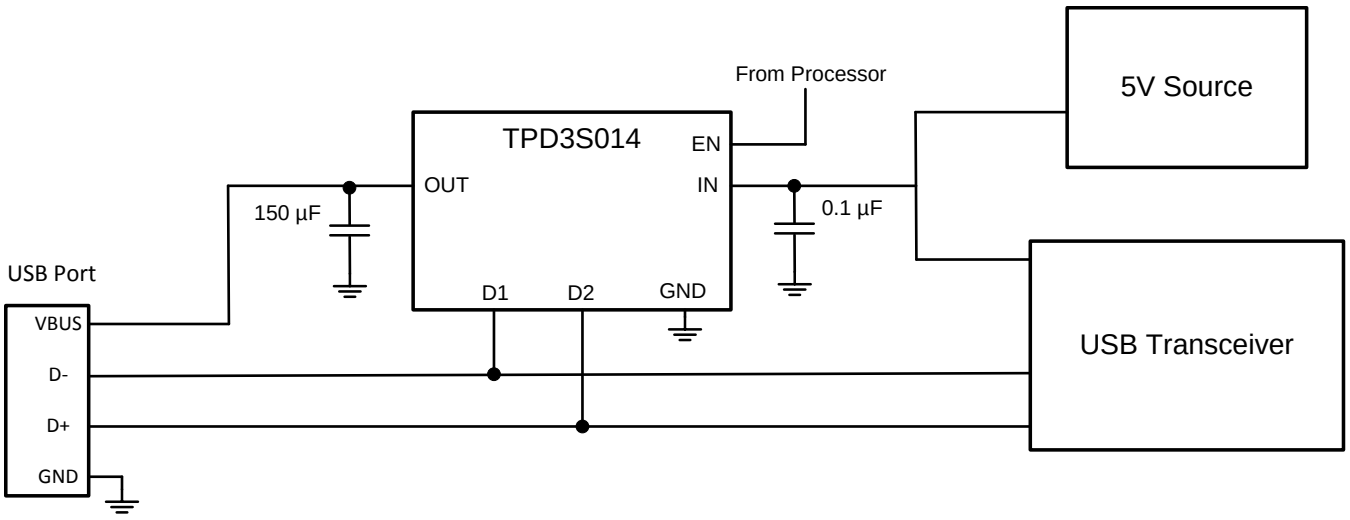


Figure 30. USB2.0 Application Schematic

9.2.1.1 Design Requirements

For this design example, use the following as the system parameters.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
USB port type	Standard downstream port
Signal voltage range on V_{BUS}	0 V to 5.25 V
Current range on V_{BUS}	0 mA to 500 mA
Drive EN low (disabled)	0 V to 0.7 V(1)
Drive EN high (enabled)	2 V to 5.5 V(1)
Maximum voltage droop allowed on adjacent USB port	330 mV
Maximum data rate	480 Mbps

(1) If active low logic is desired, see the *Implementing Active Low Logic* section.

9.2.1.2 Detailed Design Procedure

To properly implement your USB port with TPD3S0x4s, the first step is to determine what type of USB port you are implementing in your system, whether it be a Standard Downstream Port (SDP), Charging Downstream Port (CDP), or Dedicated Charging Port (DCP); this will inform you what your maximum continuous operating current will be on VBUS. In our example, we are implementing an SDP port, so the maximum continuous current allowed to be pulled by a device is 500mA. Therefore, we need to choose a current limit switch that is 5.25V tolerant, can handle 500mA continuous DC current, and has a current limit point is above 500 mA so it will not current limit during normal operation. TPD3S014 is therefore the best choice for this application, as it has these features, and in fact was specifically designed for this application.

The next decision point is choosing your input and output capacitors for your current limit switch. A minimum of 0.1 µF is always recommended on the IN pin. For the OUT pin on VBUS, USB standard requires a minimum of 120 µF; typically a 150 µF capacitor is used. The purpose of the capacitance requirement on the VBUS line in the USB specification is to prevent the adjacent USB port's VBUS voltage from dropping more than 330 mV during a hot-plug or fault occurrence on the VBUS pin of one USB port. Hot-plugs and fault conditions on one USB port should not disturb the normal operation of an adjacent USB port; therefore, it is possible to use an output capacitance lower than 120 µF if your system is able to keep voltage droops on adjacent USB ports less than or equal to 330 mV. For example, if the DC/DC powering VBUS has a fast transient response, 120 µF may not be required.

If your USB port is powered from a shared system 5V rail, a system designer may desire to use an input capacitor larger than 0.1 µF on the IN pin. This is largely dependent on your PCB layout and parasitics, as well as your maximum tolerated voltage droop on the shared rail during transients. For more information on choosing input and output capacitors, see *Input and Output Capacitance*.

The EN pin controls the on and off state of the device, and typically is connected to the system processor for power sequencing. However, the EN pin can also be shorted to the IN pin to always have the TPD3S014 on when 5-V power supply on; this also saves a GPIO pin on your processor.

For a USB port with High-Speed 480Mbps operation, low capacitance TVS ESD protection diodes are required to protect the D+ and D- lines in the event of system level ESD event. TPD3S014 has 2-channels of low capacitance TVS ESD protection diodes integrated. When placed near the USB connector, TPD3S014 offers little or no signal distortion during normal operation. TPD3S014 also ensures that the core system circuitry is protected in the event of an ESD strike. PCB layout is critical when implementing TVS ESD protection diodes in your system; please read the *Layout* section for proper guidelines on routing your USB lines with TPD3S014.

9.2.1.3 Implementing Active Low Logic

For active low logic, a transistor can be used with the TPD3S014 EN Pin.

Using an nFET transistor, when the Processor sends a low signal, the transistor is switched off, and V_{LOGIC} pulls up EN through R_1. When the Processor sends a “high” signal, the nFET is switched on and sinks current from the EN Pin and R_1. For 5-V V_{LOGIC}, with the appropriate on-resistance (R_{ON}) value in the nFET and resistance for R_1, the V_{IL} for EN can be met. For example, with a transistor with R_{ON} of 3-Ω, a pull-up resistor as low as 11 Ω provides a logic level of 0.7 V. For power-budgeting concerns, a better choice is R_1 of 40-kΩ which provides 0.25 V for EN when the Processor asserts high, and 4.96 V when the Processor asserts low.

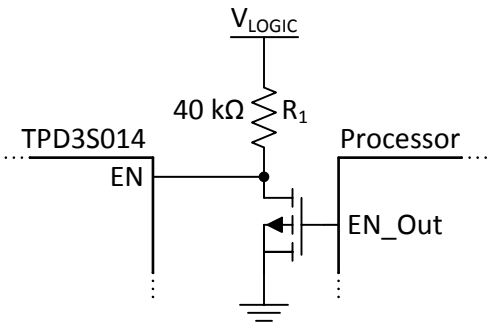


Figure 31. Implementing Active Low Logic for EN Pin

9.2.1.4 Application Curves

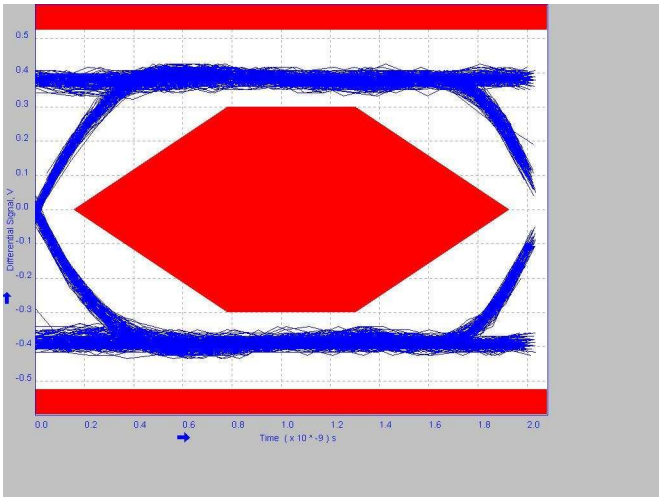


Figure 32. Eye-Diagram Without EVM

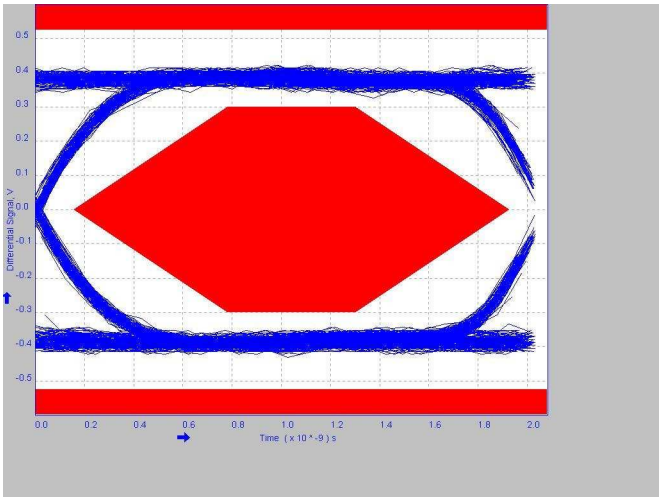


Figure 33. Eye-Diagram With EVM, Without TPD3S0x4

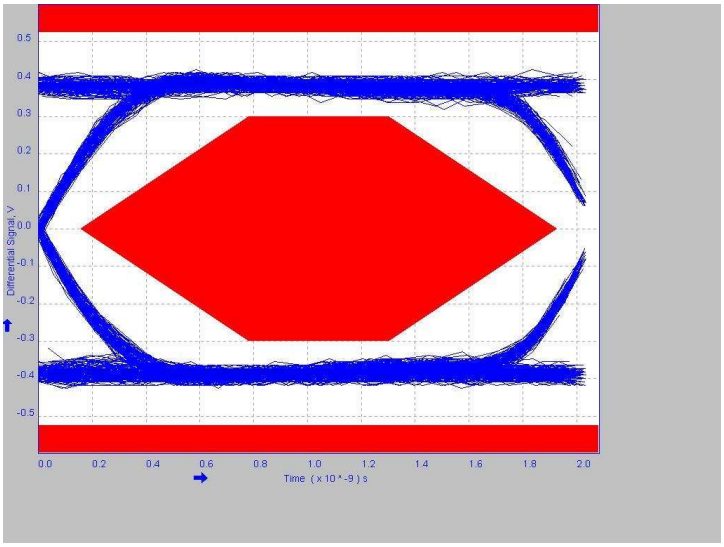


Figure 34. Eye-Diagram of TPD3S0x4 on EVM

9.2.2 USB3.0 Application

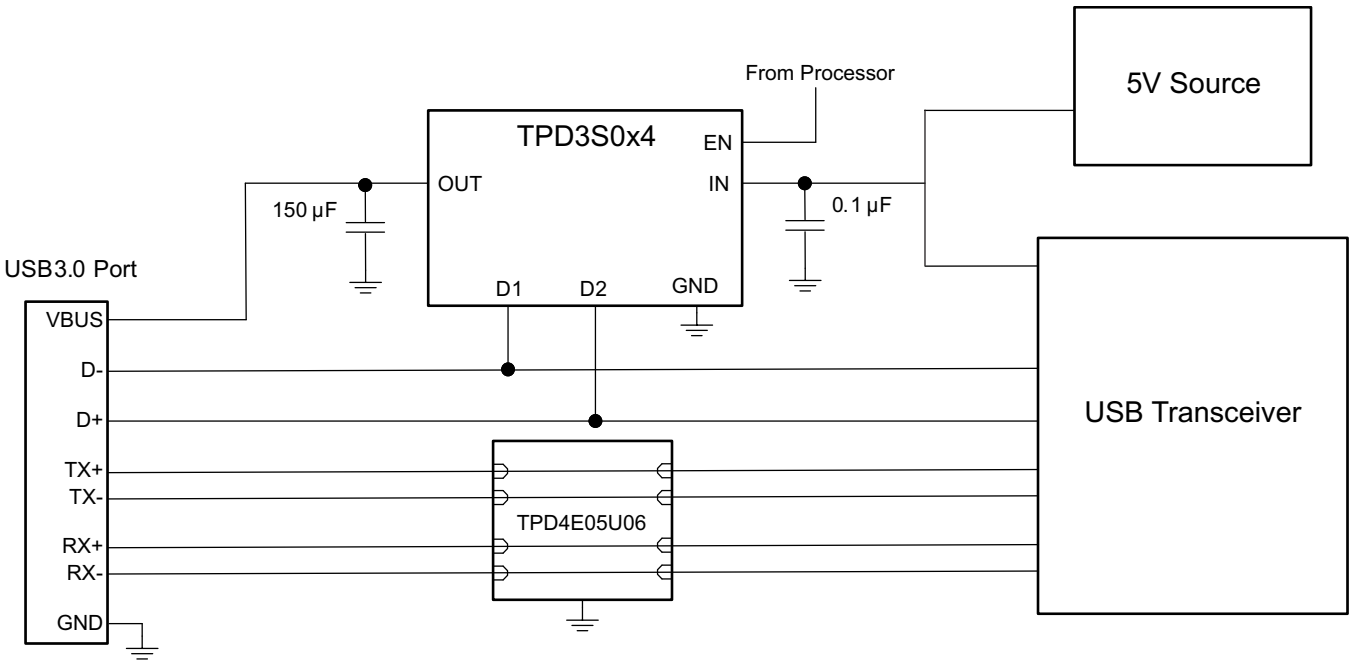


Figure 35. USB3.0 Application Schematic

9.2.2.1 Design Requirements

For this design example, use the following as the system parameters.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
USB port type	Standard downstream port
Signal voltage range on V_{BUS}	0 V to 5.25 V
Current range on V_{BUS}	0 mA to 900 mA
Maximum voltage droop allowed on adjacent USB port	330 mV
Maximum data rate D+, D- lines	480 Mbps
Maximum data rate TX±, RX± lines	5 Gbps

9.2.2.2 Detailed Design Procedure

The implementation of the USB3.0 port with TPD3S0x4s is identical to the USB2.0 port, except that in this use case we must use TPD3S044 because USB3.0 SDP has a maximum V_{BUS} current 900 mA. TPD3S014 current limit level is too low for USB3.0 operation. In addition to using TPD3S044, USB3.0 has four more Super-Speed Lines for transferring data 5 Gbps, and these lines also typically require Level 4 IEC61000-4-2 ESD Protection. With a data rate of 5 Gbps, ultra-low capacitance TVS ESD protection diodes are required to protect the TX± and RX± lines in the event of system level ESD event. TPD4E05U06 provides 4-channels of ultra-low capacitance TVS ESD protection diodes for USB3.0 Super-Speed lines, and can be coupled with TPD3S044 to provide a two-chip total protection solution for the USB3.0 host port. Please refer to the *Layout* section of the data sheet for guidelines on the PCB layout of this two-chip solution.

The rest of the design procedure is identical to the *USB2.0 Application* section, so refer to it for the rest of the design procedure.

9.2.2.3 Application Curves

See *Application Curves* for TPD3S0x4 eye-diagram performance. Refer to the TPD4E05U06 data sheet on ti.com to see its specifications and eye-diagram performance.

10 Power Supply Recommendations

These devices are designed to operate from a 5-V input voltage supply. This input should be well regulated. If the input supply is located more than a few inches away from the TPD3S0x4, additional bulk capacitance may be required in addition to the recommended minimum 0.1-µF bypass capacitor on the IN pin to keep the input rail stable during fault events.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Examples

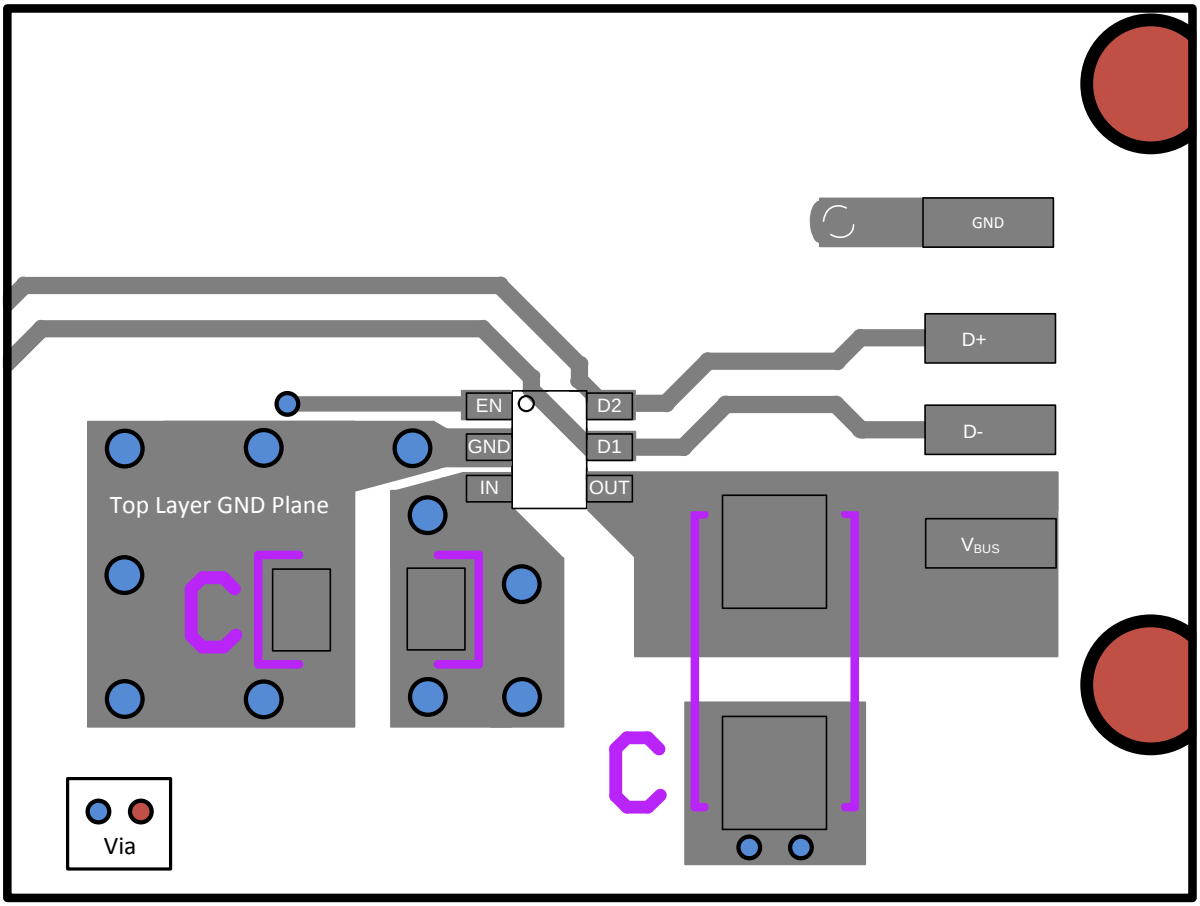


Figure 36. USB2.0 Type A TPD3S0x4 Board Layout

Layout Examples (continued)

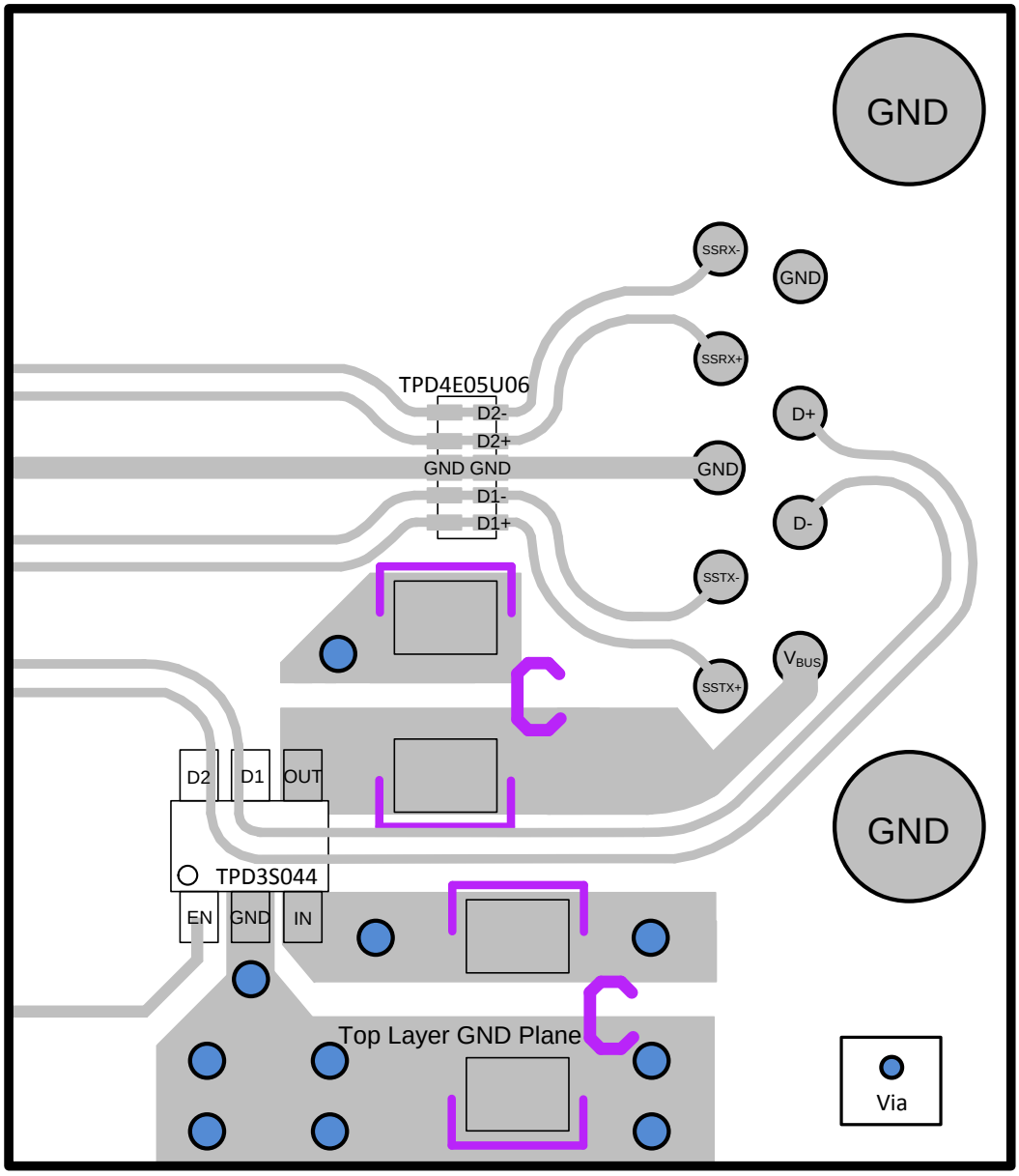


Figure 37. USB3.0 Type A TPD3S044 Board Layout

11.3 Power Dissipation and Junction Temperature

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPD3S0x4s. The system designer can control choices of the devices proximity to other power dissipating devices and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow. Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. In particular, connect the GND pin to a large ground plane for the best thermal dissipation. The following PCB layout example Figure 38 was used to determine the $R_{\theta JA}$ Custom thermal impedances noted in the *Thermal Information* table. It is based on the use of the JEDEC high-k circuit board construction with 4, 1 oz. copper weight layers (2 signal and 2 plane).

Power Dissipation and Junction Temperature (continued)

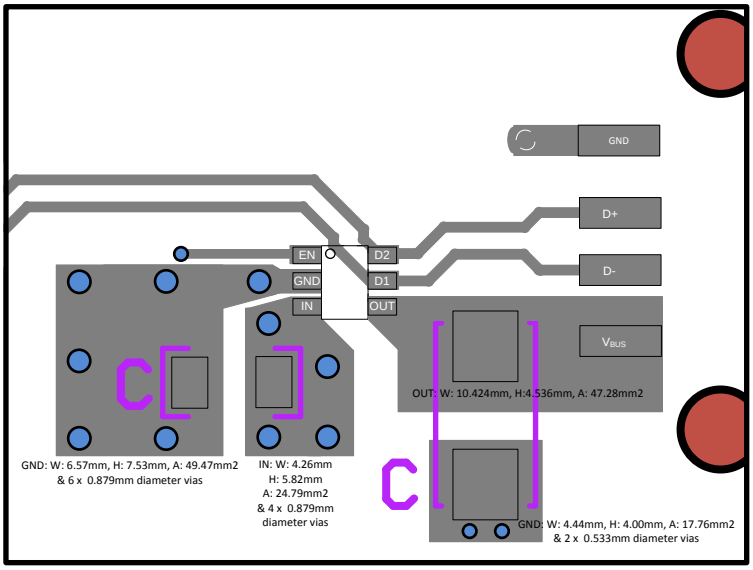


Figure 38. PCB Layout Example

The following procedure requires iteration because power loss is due to the internal MOSFET $I^2 \times R_{DS(ON)}$, and $R_{DS(ON)}$ is a function of the junction temperature. As an initial estimate, use the $R_{DS(ON)}$ at 125°C from the *Typical Characteristics*, and the preferred package thermal resistance for the preferred board construction from the *Thermal Information* table.

$$T_J = T_A + [(I_{OUT}^2 \times R_{DS(ON)}) \times R_{\theta JA}]$$

where

- I_{OUT} = Rated OUT pin current (A)
- $R_{DS(ON)}$ = Power switch on-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)
- $R_{\theta JA}$ = Thermal resistance (°C/W) (1)

If the calculated T_J is substantially different from the original assumption, estimate a new value of $R_{DS(ON)}$ using the typical characteristic plot and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction with a lower $R_{\theta JA}$. Please find the junction temperature derating curve based on the TI standard reliability duration in Figure 39.

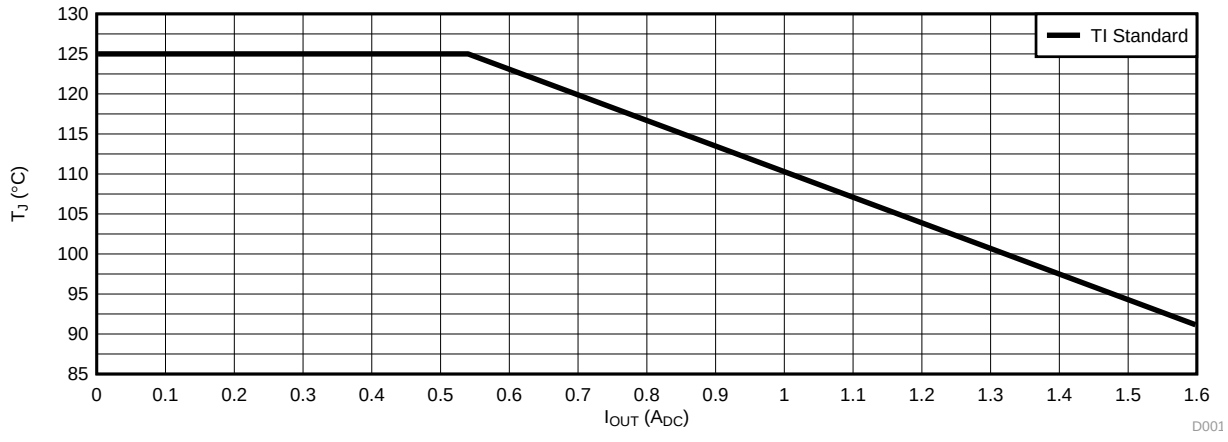


Figure 39. Junction Temperature Derating Curve

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD3S014	Click here	Click here	Click here	Click here	Click here
TPD3S044	Click here	Click here	Click here	Click here	Click here
TPD4E05U06	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3S014DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SII	Samples
TPD3S044DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SIJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD3S014 :

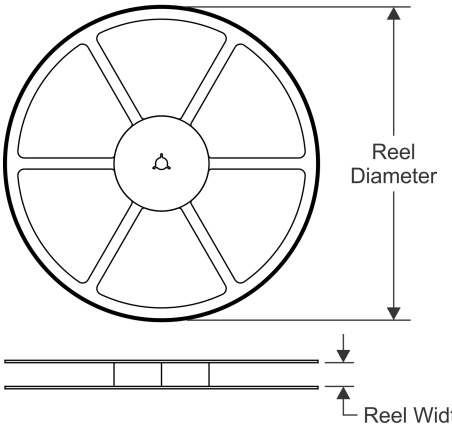
- Automotive: TPD3S014-Q1

NOTE: Qualified Version Definitions:

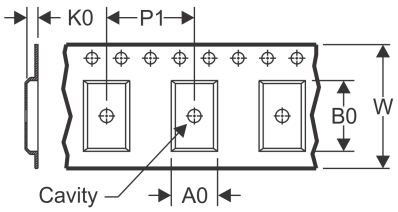
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

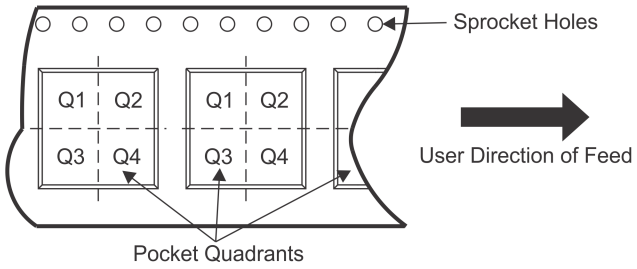


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

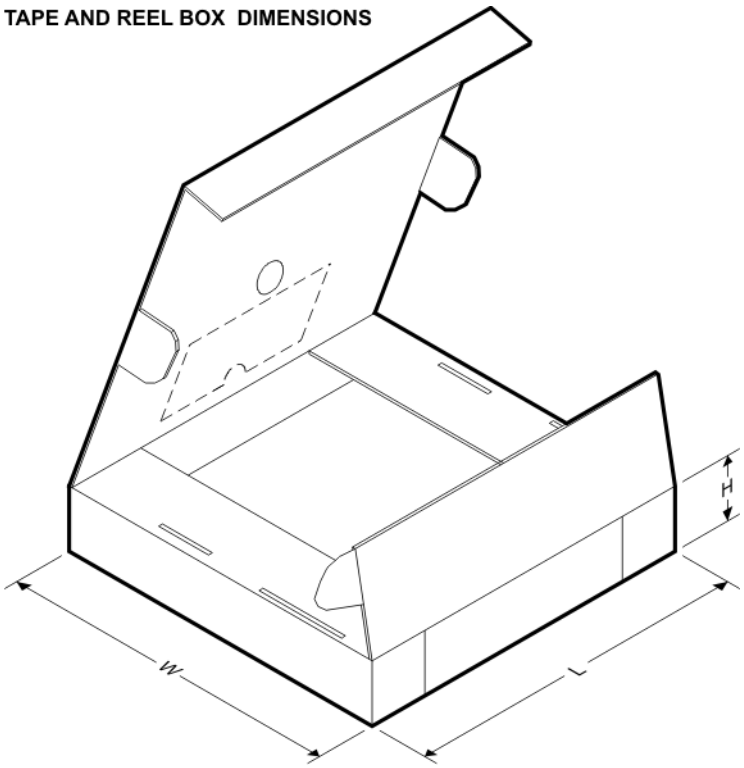
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S014DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPD3S044DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

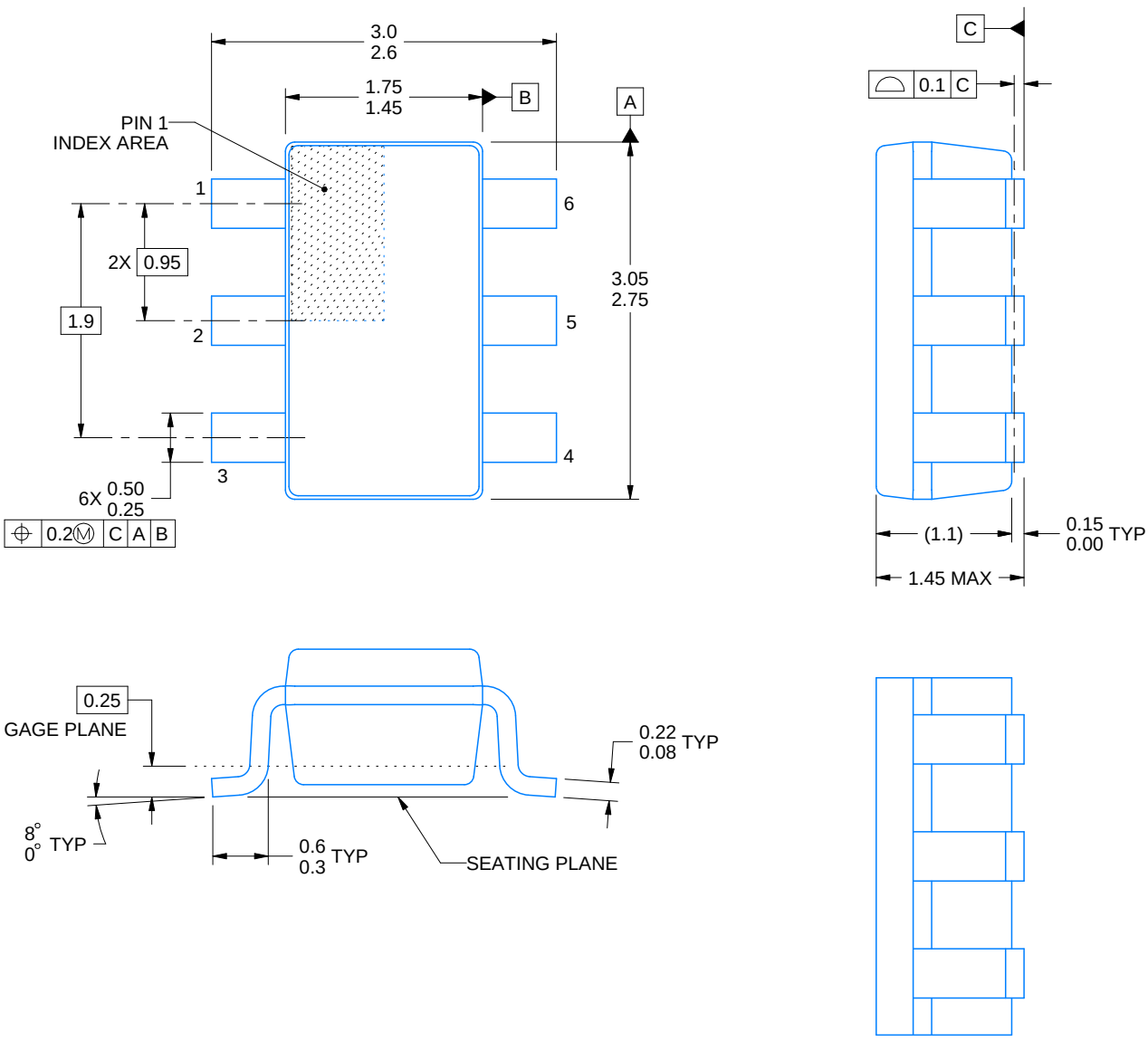
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S014DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPD3S044DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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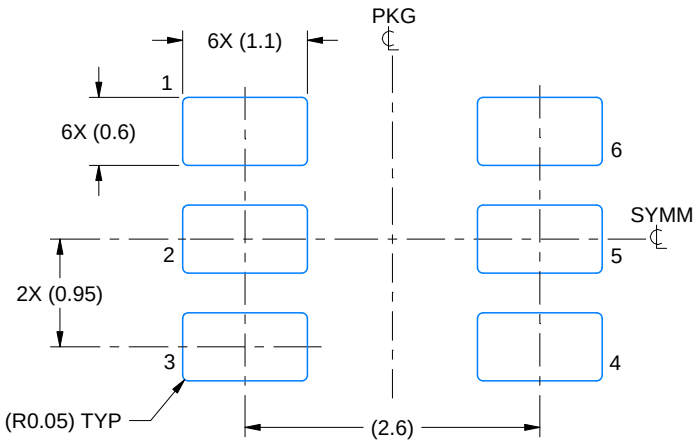
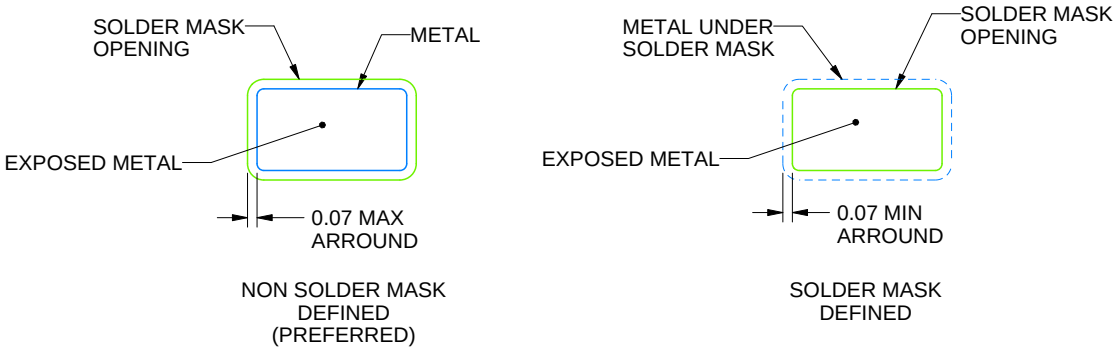
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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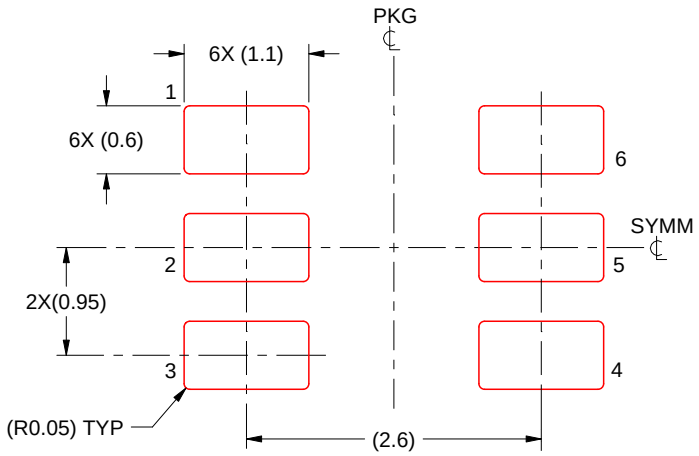
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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