8-PIN QUASI-RESONANT FLYBACK GREEN-MODE CONTROLLER

Check for Samples: UCC28600-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Green-Mode Controller With Advanced Energy Saving Features**
- **Quasi-Resonant Mode Operation for Reduced EMI and Low Switching Losses (Low Voltage Switching)**
- **Low Standby Current for System No-Load Power Consumption**
- **Low Startup Current: 25 μA Maximum**
- **Programmable Overvoltage Protection, Line and Load**
- **Internal Overtemperature Protection**
- **Current Limit Protection**
  - **Cycle-by-Cycle Power Limit**
  - **Primary-Side Overcurrent Hiccup Restart Mode**
- **1-A Sink TrueDrive™, -0.75-A Source Gate Drive Output**
- **Programmable Soft-Start**
- **Green-Mode Status Pin (PFC Disable Function)**

APPLICATIONS

- **Bias Supplies for LCD-Monitors, LCD-TV, PDP-TV, and Set Top Boxes**
- **AC/DC Adapters and Offline Battery Chargers**
- **Energy Efficient Power Supplies up to 200 W**

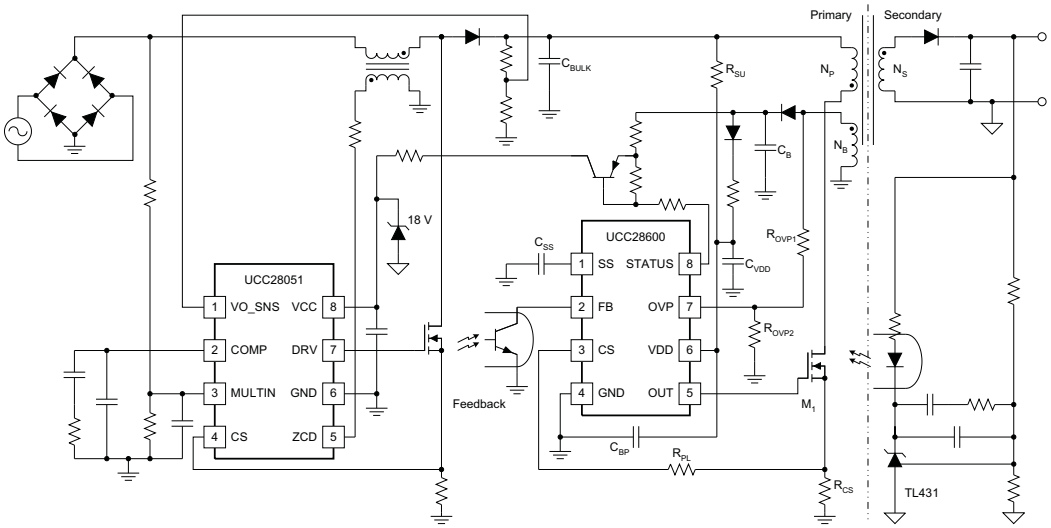
DESCRIPTION

The UCC28600-Q1 is a PWM controller with advanced energy features to meet stringent world-wide energy efficiency requirements.

UCC28600-Q1 integrates built-in advanced energy saving features with high level protection features to provide cost effective solutions for energy efficient power supplies. UCC28600-Q1 incorporates frequency fold back and green mode operation to reduce the operation frequency at light load and no load operations.

UCC28600-Q1 is offered in the 8-pin SOIC (D) package. Operating ambient temperature range is -40°C to 105°C.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TrueDrive is a trademark of Texas Instruments.

DESCRIPTION (CONT.)

The Design Calculator, (Texas Instruments Literature number SLVC104), located in the Tools and Software section of the UCC28600-Q1 product folder, provides a user-interactive iterative process for selecting recommended component values for an optimal design.

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	SOIC – D	Tape and reel	UCC28600TDRQ1	28600T

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UCC28600-Q1	UNIT
V_{DD}	Supply voltage range	I_{DD} < 20 mA	32	V
I_{DD}	Supply current		20	mA
$I_{OUT(sink)}$	Output sink current (peak)		1.2	A
$I_{OUT(source)}$	Output source current (peak)		-0.8	
	Analog inputs	FB, CS, SS	-0.3 to 6.0	V
V_{OVP}			-1.0 to 6.0	
$I_{OVP(source)}$			-1.0	mA
V_{STATUS}		V_{DD} = 0 V to 30 V	30	V
	Power dissipation	SOIC-8 package, T_A = 25°C	650	mW
T_J	Operating junction temperature range		-40 to 125	°C
T_{stg}	Storage temperature		–65 to 150	
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage			21	V
I_{OUT}	Output sink current	0			A
T_A	Ambient temperature range	-40		105	°C
T_J	Operating junction temperature range	-40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human Body Model		1500	V
Charged-Device Model		1000	
Machine Model		150	V

ELECTRICAL CHARACTERISTICS

VDD = 15 V, 0.1-µF capacitor from VDD to GND, 3.3-nF capacitor from SS to GND charged over 3.5 V, 500-Ω resistor from OVP to -0.1 V, FB = 4.8 V, STATUS = not connected, 1-nF capacitor from OUT to GND, CS = GND, T_A = -40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall						
$I_{STARTUP}$	Startup current	VDD = V_{UVLO} -0.3 V		12	25	µA
$I_{STANDBY}$	Standby current	V_{FB} = 0 V		350	550	µA
I_{DD}	Operating current	Not switching		2.5	3.5	mA
		130 kHz, QR mode		5.0	7.0	mA
	VDD clamp	FB = GND, I_{DD} = 10 mA	21	26	32	V
Undervoltage Lockout						
$VDD_{(uvlo)}$	Startup threshold		10.3	13.0	15.3	V
	Stop threshold		6.3	8	9.3	V
$\Delta VDD_{(uvlo)}$	Hysteresis		4.0	5.0	6.0	V
PWM (Ramp) (1)						
D_{MIN}	Minimum duty cycle	V_{SS} = GND, V_{FB} = 2 V			0%	
D_{MAX}	Maximum duty cycle	QR mode, f_S = max, (open loop)		99%		
Oscillator (OSC)						
$f_{QR(max)}$	Maximum QR and DCM frequency		114	130	145	kHz
$f_{QR(min)}$	Minimum QR and FFM frequency	V_{FB} = 1.3 V	32	40	48	kHz
f_{SS}	Soft start frequency	V_{SS} = 2.0 V	32	40	48	kHz
dT_S/dFB	VCO gain	T_S for 1.6 V < V_{FB} < 1.8 V	-38	-30	-22	µs/V
Feedback (FB)						
R_{FB}	Feedback pullup resistor		12	20	28	kΩ
V_{FB}	FB, no load	QR mode	3.30	4.87	6.00	V
	Green-mode ON threshold	V_{FB} threshold	0.3	0.5	0.7	V
	Green-mode OFF threshold	V_{FB} threshold	1.2	1.4	1.6	V
	Green-mode hysteresis	V_{FB} threshold	0.7	0.9	1.1	V
	FB threshold burst-ON	V_{FB} during green mode	0.3	0.5	0.7	V
	FB threshold burst-OFF	V_{FB} during green mode	0.5	0.7	0.9	V
	Burst Hysteresis	V_{FB} during green mode	0.13	0.25	0.42	V
Status						
$R_{DS(on)}$	STATUS on resistance	V_{STATUS} = 1 V	1.0	2.4	3.8	kΩ
$I_{STATUS(leakage)}$	STATUS leakage/off current	V_{FB} = 0.44 V, V_{STATUS} = 15 V	-0.1		2.0	µA

(1) R_{SCT} and C_{CST} are not connected in the circuit for maximum and minimum duty cycle tests, current sense tests and power limit tests.

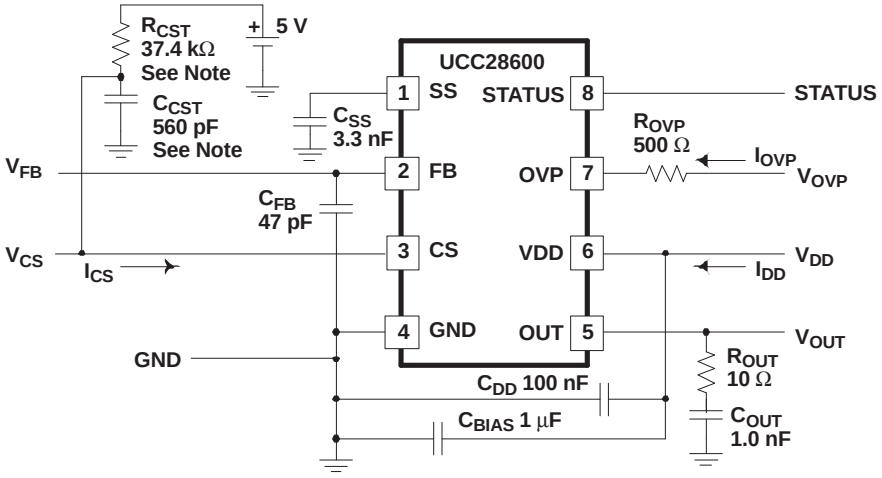
ELECTRICAL CHARACTERISTICS (continued)

VDD = 15 V, 0.1-μF capacitor from VDD to GND, 3.3-nF capacitor from SS to GND charged over 3.5 V, 500-Ω resistor from OVP to -0.1 V, FB = 4.8 V, STATUS = not connected, 1-nF capacitor from OUT to GND, CS = GND, T_A = -40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense (CS)(2)						
$A_{CS(FB)}$	Gain, FB = ΔV_{FB} / ΔV_{CS}	QR mode		2.5		V/V
	Shutdown threshold	V_{FB} = 2.4 V, V_{SS} = 0 V	1.13	1.25	1.38	V
	CS to output delay time (power limit)	CS = 1.0 V_{PULSE}	100	175	300	ns
	CS to output delay time (over current fault)	CS = 1.45 V_{PULSE}	50	100	150	
	CS discharge impedance	CS = 0.1 V, V_{SS} = 0 V	25	115	250	Ω
$V_{CS(os)}$	CS offset	SS mode, V_{SS} ≤ 2.0 V, via FB	0.35	0.40	0.45	V
Power Limit (PL)(2)						
$I_{PL(cs)}$	CS current	OVP = -300 μA	-165	-150	-135	μA
	CS working range	QR mode, peak CS voltage	0.70	0.81	0.92	V
V_{PL}	PL threshold	Peak CS voltage + CS offset	1.05	1.20	1.37	
Soft Start (SS)						
$I_{SS(chg)}$	Softstart charge current	V_{SS} = GND	-9.0	-6.0	-4.5	μA
$I_{SS(dis)}$	Softstart discharge current	V_{SS} = 0.5 V	2.0	5.0	10	mA
V_{SS}	Switching ON threshold	Output switching start	0.8	1.0	1.2	V
Overvoltage Protection (OVP)						
$I_{OVP(line)}$	Line overvoltage protection	I_{OVP} threshold, OUT = HI	-512	-450	-370	μA
$V_{OVP(on)}$	OVP voltage at OUT = HIGH	V_{FB} = 4.8 V, V_{SS} = 5.0 V, $I_{OVP(on)}$, = -300 μA	-125		-25	mV
$V_{OVP(load)}$	Load overvoltage protection	V_{OVP} threshold, OUT = LO	3.37	3.75	4.13	V
	Valley detect delay		300	550	800	ns
Thermal Protection (TSP)						
	Thermal shutdown (TSP) temperature(3)		130	140	150	°C
	Thermal shutdown hysteresis			15		
OUT						
t_{RISE}	Rise time	10% to 90% of 13 V typical out clamp		50	75	ns
t_{FALL}	Fall time			10	20	

(2) R_{SCT} and C_{CST} are not connected in the circuit for maximum and minimum duty cycle tests, current sense tests and power limit tests.
(3) Ensured by design. Not production tested.

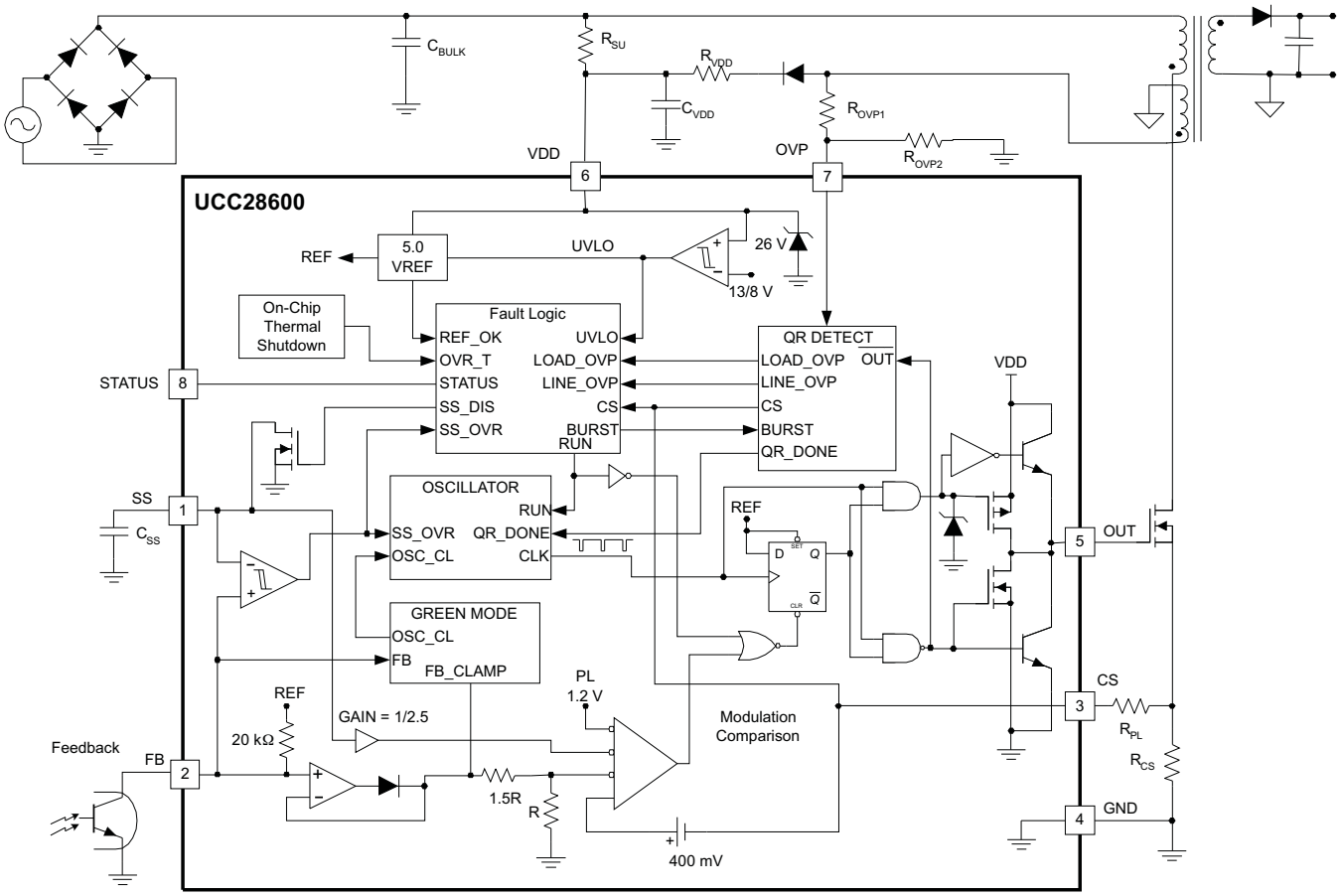
OPEN LOOP TEST CIRCUIT



NOTE

R_{CST} and C_{CST} are not connected for maximum and minimum duty cycle tests, current sense tests and power limit tests.

BLOCK DIAGRAM/TYPICAL APPLICATION



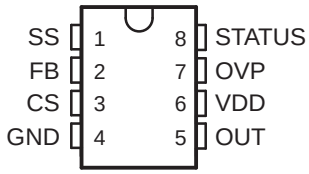
ORDERING INFORMATION

T_A	PACKAGES	PART NUMBER
-40°C to 105°C	SOIC (D)(1)	UCC28600-Q1D

(1) SOIC (D) package is available taped and reeled by adding "R" to the above part numbers. Reeled quantities for UCC28600-Q1DR is 2,500 devices per reel.

DEVICE INFORMATION

UCC28600
D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CS	3	I	Current sense input. Also programs power limit, and used to control modulation and activate overcurrent protection. The CS voltage input originates across a current sense resistor and ground. Power limit is programmed with an effective series resistance between this pin and the current sense resistor.
FB	2	I	Feedback input or control input from the optocoupler to the PWM comparator used to control the peak current in the power MOSFET. An internal 20-kΩ resistor is between this pin and the internal 5-V regulated voltage. Connect the collector of the photo-transistor of the feedback optocoupler directly to this pin; connect the emitter of the photo-transistor to GND. The voltage of this pin controls the mode of operation in one of the three modes: quasi resonant (QR), frequency foldback mode (FFM) and green mode (GM).
GND	4	-	Ground for internal circuitry. Connect a ceramic 0.1-μF bypass capacitor between VDD and GND, with the capacitor as close to these two pins as possible.
OUT	5	O	1-A sink (TrueDrive™) and 0.75-A source gate drive output. This output drives the power MOSFET and switches between GND and the lower of VDD or the 13-V internal output clamp.
OVP	7	I	Over voltage protection (OVP) input senses line-OVP, load-OVP and the resonant trough for QR turn-on. Detect line, load and resonant conditions using the primary bias winding of the transformer, adjust sensitivity with resistors connected to this pin.
SS	1	I	Soft-start programming pin. Program the soft-start rate with a capacitor to ground; the rate is determined by the capacitance and the internal soft-start charge current. Placement of the soft-start capacitor is critical and should be placed as close as possible to the SS pin and GND, keeping trace length to a minimum. All faults discharge the SS pin to GND through an internal MOSFET with an $R_{DS(on)}$ of approximately 100 Ω. The internal modulator comparator reacts to the lowest of the SS voltage, the internal FB voltage and the peak current limit.
STATUS	8	O	ACTIVE HIGH open drain signal that indicates the device has entered standby mode. This pin can be used to disable the PFC control circuit (high impedance = green mode). STATUS pin is high during UVLO, (VDD < startup threshold), and softstart, (SS < FB).
VDD	6	I	Provides power to the device. Use a ceramic 0.1-μF by-pass capacitor for high-frequency filtering of the VDD pin, as described in the GND pin description. Operating energy is usually delivered from auxiliary winding. To prevent hiccup operation during start-up, a larger energy storage cap is also needed between VDD and GND.

TERMINAL COMPONENTS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION (1) (2) (3)
CS	3	I	$R_{CS} = \frac{\left(V_{PL} - V_{CS(os)}\right)\left(I_{CS(2)} - I_{CS(1)}\right)}{I_{CS(2)}I_{P(1)} - I_{CS(1)}I_{P(2)}}$ (1) $R_{PL} = \frac{\left(V_{PL} - V_{CS(os)}\right)\left(I_{P(2)} - I_{P(1)}\right)}{I_{CS(1)}I_{P(2)} - I_{CS(2)}I_{P(1)}}$ where: • I_{P1} is the peak primary current at low line, full load (3) • I_{P2} is the peak primary current at high line, full load (3) • I_{CS1} is the power limit current that is sourced at the CS pin at low-line voltage (3) • I_{CS2} is the power limit current that is sourced at the CS pin at high-line voltage (3) • V_{PL} is the Power Limit (PL) threshold (2) • $V_{CS(os)}$ is the CS offset voltage (2)
FB	2	I	Opto-isolator collector
GND	4	-	Bypass capacitor to VDD, C_{BP} = 0.1 µF
OUT	5	O	Power MOSFET gate
OVP	7	I	$R_{OVP1} = \frac{1}{I_{OVP(line)}}\left(\frac{N_B}{N_P}V_{BULK(ov)}\right)$ $R_{OVP2} = R_{OVP1}\left[\frac{V_{OVP(load)}}{\frac{N_B}{N_S}\left(V_{OUT(shutdown)} + V_F\right) - V_{OVP(load)}}\right]$ where: • $I_{OVP(line)}$ is OVP_{line} current threshold (2) • $V_{BULK(ov)}$ is the allowed input over- voltage level (3) • $V_{OVP(load)}$ is OVP_{load} (2) • $V_{OUT(shutdown)}$ is the allowed output over-voltage level (3) • V_F is the forward voltage of the secondary rectifier • N_B is the number of turns on the bias winding (3) • N_S is the number of turns on the secondary windings (3) • N_P is the number of turns on the primary windings (3)

(1) Refer to Figure 1 for all reference designators in the Terminal Components Table.
(2) Refer to the Electrical Characteristics Table for constant parameters.
(3) Refer to the UCC28600-Q1 Design Calculator (TI Literature Number SLVC104) or laboratory measurements for currents, voltages and times in the operational circuit.

TERMINAL COMPONENTS (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION(1) (2) (3)
SS	1	I	$C_{SS} > I_{SS} \times \frac{t_{SS(min)}(\text{due power limit})}{A_{CS(FB)} \times \left(V_{PL} - V_{CS(os)}\right)}$ where $t_{SS(min)}$ is the greater of: $t_{SS(min)} = \left[\frac{-R_{LOAD(ss)}C_{OUT}}{2} \ell n\left\{1 - \frac{\left(V_{OUT} - \Delta V_{OUT(step)}\right)^2}{R_{LOAD(ss)}P_{OUT(max)limit}}\right\}\right]$ or $t_{SS(min)} = \left[\frac{C_{OUT}V_{OUT}^2}{2\,P_{LIM}}\right]$ (2) • $R_{LOAD(ss)}$ is the effective load impedance during soft-start(4) • $\Delta V_{OUT(step)}$ is the allowed change in V_{OUT} due to a load step(4) • $P_{OUT(max\ limit)}$ Programmed power limit level, in W (4) • $A_{CS(FB)}$ is the current sense gain(5) • $V_{CS(os)}$ is the CS offset voltage(5) • I_{SS} is the soft-start charging current(5) • V_{PL} is the power limit threshold(5)
STATUS	8	O	$R_{ST2} = \frac{V_{BE(off)}}{I_{STATUS(leakage)}}$ $R_{ST1} = \frac{R_{ST2} \times \left[VDD_{(uvlo-on)} - V_{BE(sat)} - R_{DS(on)} \times \left(\frac{I_{CC}}{\beta_{sat}}\right)\right] - R_{DS(on)}V_{BE(sat)}}{\left(\left(\frac{I_{CC}}{\beta_{sat}}\right) \times R_{ST2}\right) + V_{BE(sat)}}$ where: • β_{SAT} is the gain of transistor Q_{ST} in saturation • $V_{BE(sat)}$ is the base-emitter voltage of transistor Q_{ST} in saturation • $VDD_{(uvlo-on)}$ is the startup threshold(5) • I_{CC} is the collector current of Q_{ST} • $I_{STATUS(leakage)}$ is the maximum leakage/off current of the STATUS pin(5) • $V_{BE(off)}$ is the maximum allowable voltage across the base emitter junction that will not turn Q_{ST} on • $R_{DS(on)}$ is the $R_{DS(on)}$ of STATUS(5)

(4) Refer to the UCC28600-Q1 Design Calculator (TI Literature Number SLVC104) or laboratory measurements for currents, voltages and times in the operational circuit.
(5) Refer to the Electrical Characteristics Table for constant parameters.

TERMINAL COMPONENTS (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION(1) (2) (3)
VDD	6	I	C_{VDD} is the greater of: $C_{VDD} = \left[\left(I_{DD} + C_{ISS}V_{OUT(hi)}f_{QR(max)}\right)\frac{T_{BURST}}{\Delta V_{DD(burst)}}\right]$ or $C_{VDD} = \left[\left(I_{DD} + C_{ISS}V_{OUT(hi)}f_{QR(max)}\right)\frac{t_{SS}}{\Delta VDD_{(uvlo)}}\right]$ (3) $R_{VDD} = \left(\frac{\pi}{4}\right)\left(\frac{N_B}{N_P}\right)\left\{\frac{\left(V_{DS1(os)}\, f_{QR(max)}\, \sqrt{L_{LEAKAGE}\left(C_D + C_{SNUB}\right)}\right.}{I_{DD} + C_{ISS}\, V_{OUT(hi)}\, f_{QR(max)}}\right\}$ $R_{SU} = \frac{V_{BULK(min)}}{I_{STARTUP}}$ where: • I_{DD} is the operating current of the UCC28600-Q1(6) • C_{ISS} is the input capacitance of MOSFET M_1 • $V_{OUT(hi)}$ is VOH of the OUT pin, either 13 V (typ) V_{OUT} clamp or less as measured • $f_{QR(max)}$ is f_S at high line, maximum load(6) • T_{BURST} is the measured burst mode period • $\Delta VDD_{(burst)}$ is the allowed V_{DD} ripple during burst mode • $\Delta VDD_{(uvlo)}$ is the UVLO hysteresis(6) • $V_{DS1(os)}$ is the amount of drain-source overshoot voltage • $L_{LEAKAGE}$ is the leakage inductance of the primary winding • C_D is the total drain node capacitance of MOSFET M_1 • $I_{STARTUP}$ is I_{DD} start-up current of the UCC28600-Q1(6) • C_{SNUB} is the snubber capacitor value • t_{SS} is the soft start charge time(7)

(6) Refer to the Electrical Characteristics Table for constant parameters.
(7) Refer to the UCC28600-Q1 Design Calculator (TI Literature Number SLVC104) or laboratory measurements for currents, voltages and times in the operational circuit.

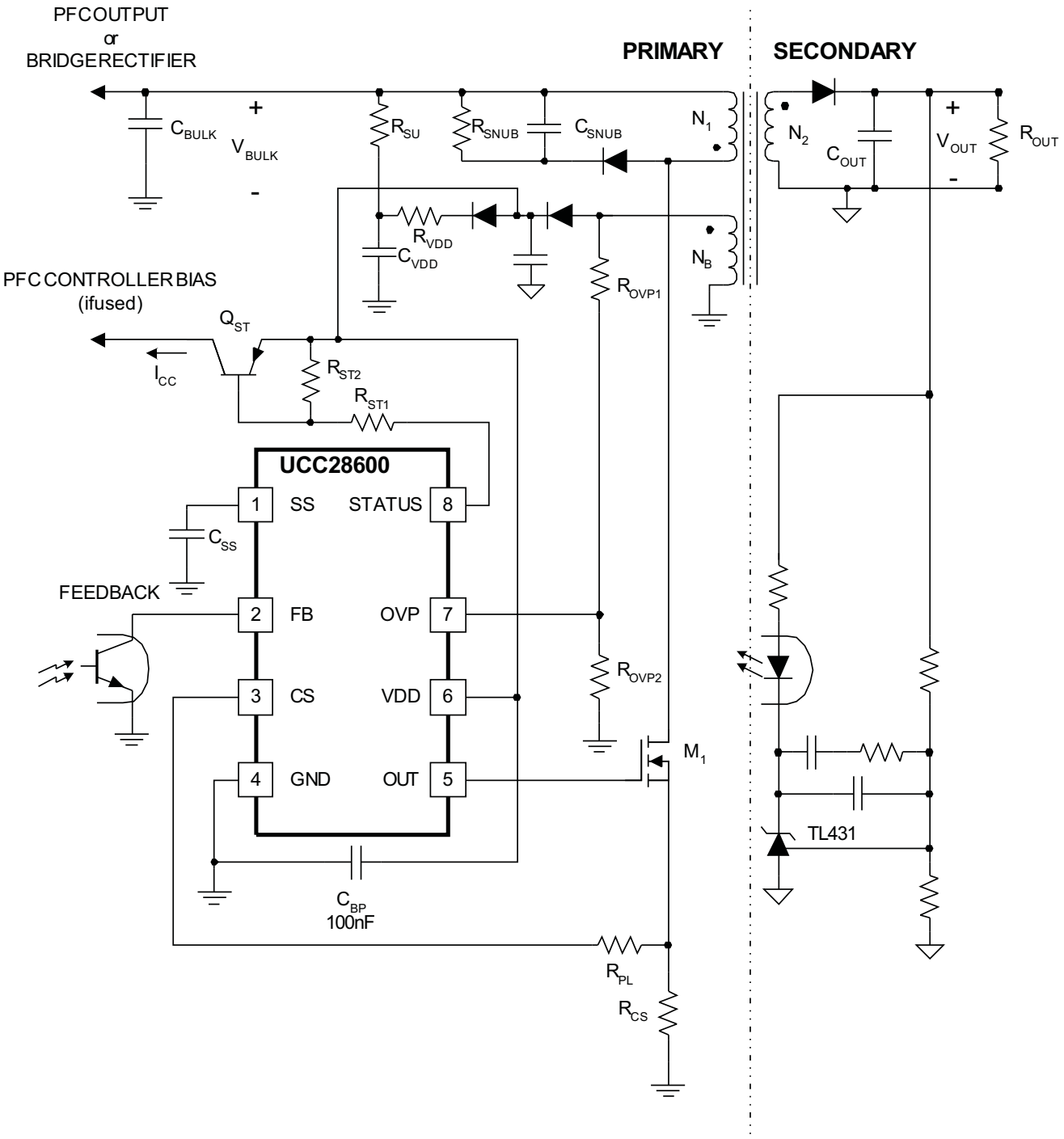


Figure 1. Pin Termination Schematic

APPLICATION INFORMATION

Functional Description

The UCC28600-Q1 is a multi-mode controller, as illustrated in Figure 3 and Figure 4. The mode of operation depends upon line and load conditions. Under all modes of operation, the UCC28600-Q1 terminates the OUT = HI signal based on the switch current. Thus, the UCC28600-Q1 always operates in current mode control so that the power MOSFET current is always limited.

Under normal operating conditions, the FB pin commands the operating mode of the UCC28600-Q1 at the voltage thresholds shown in Figure 2. Soft-start and fault responses are the exception. Soft-start mode hard-switch controls the converter at 40 kHz. The soft-start mode is latched-OFF when V_{FB} becomes less than V_{SS} for the first time after $UVLO_{ON}$. The soft-start state cannot be recovered until after passing $UVLO_{OFF}$, and then, $UVLO_{ON}$.

At normal rated operating loads (from 100% to approximately 30% full rated power) the UCC28600-Q1 controls the converter in quasi-resonant mode (QRM) or discontinuous conduction mode (DCM), where DCM operation is at the clamped maximum switching frequency (130 kHz). For loads that are between approximately 30% and 10% full rated power, the converter operates in frequency foldback mode (FFM), where the peak switch current is constant and the output voltage is regulated by modulating the switching frequency for a given and fixed V_{IN}. Effectively, operation in FFM results in the application of constant volt-seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 130 kHz to 40 kHz. For extremely light loads (below approximately 10% full rated power), the converter is controlled using bursts of 40-kHz pulses. Keep in mind that the aforementioned boundaries of steady-state operation are approximate because they are subject to converter design parameters.

Refer to the typical applications block diagram for the electrical connections to implement the features.

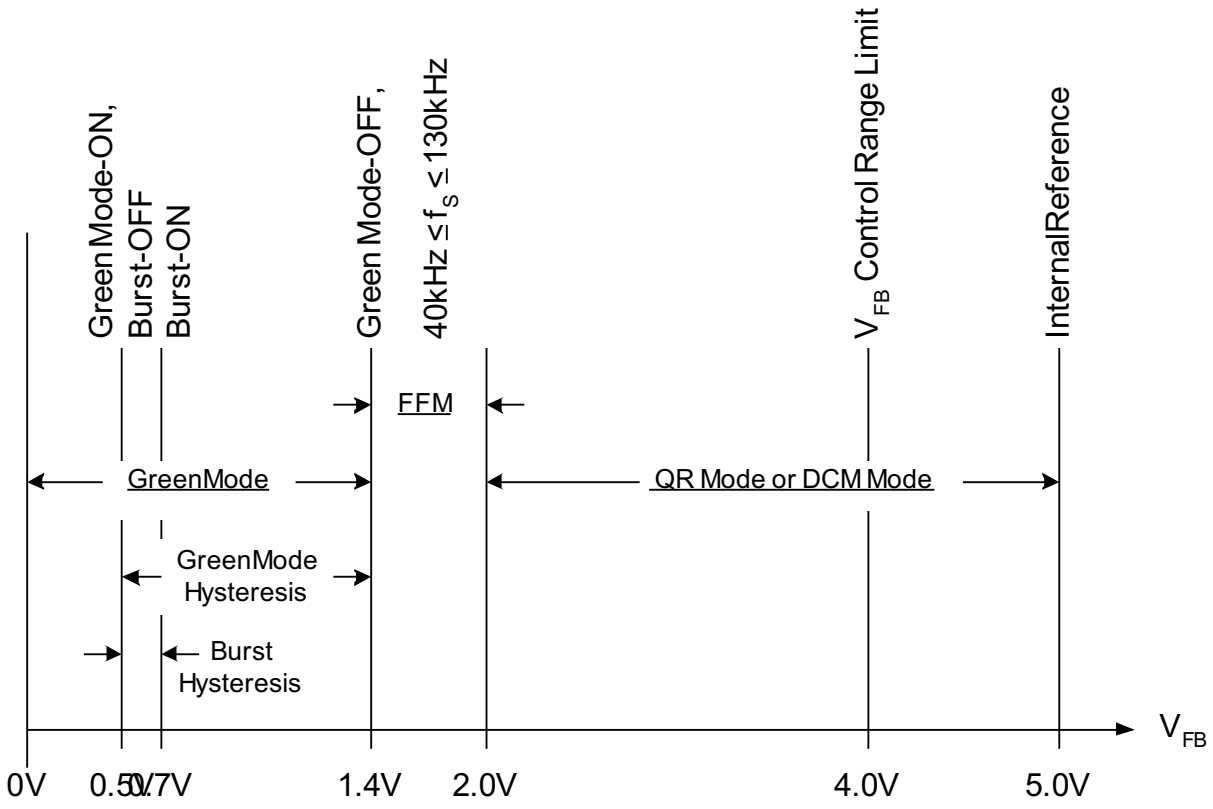


Figure 2. Mode Control with FB Pin Voltage

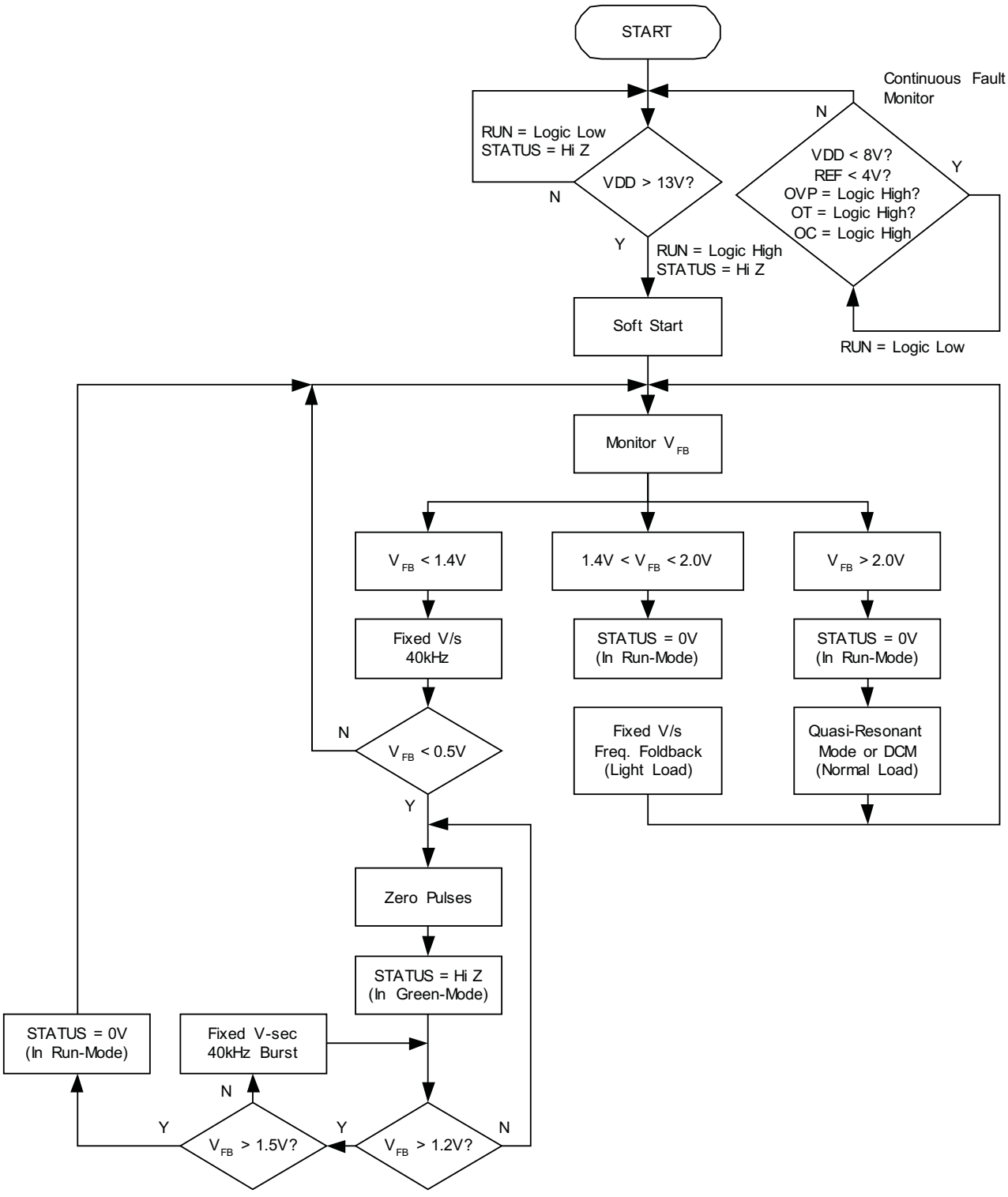


Figure 3. Control Flow Chart

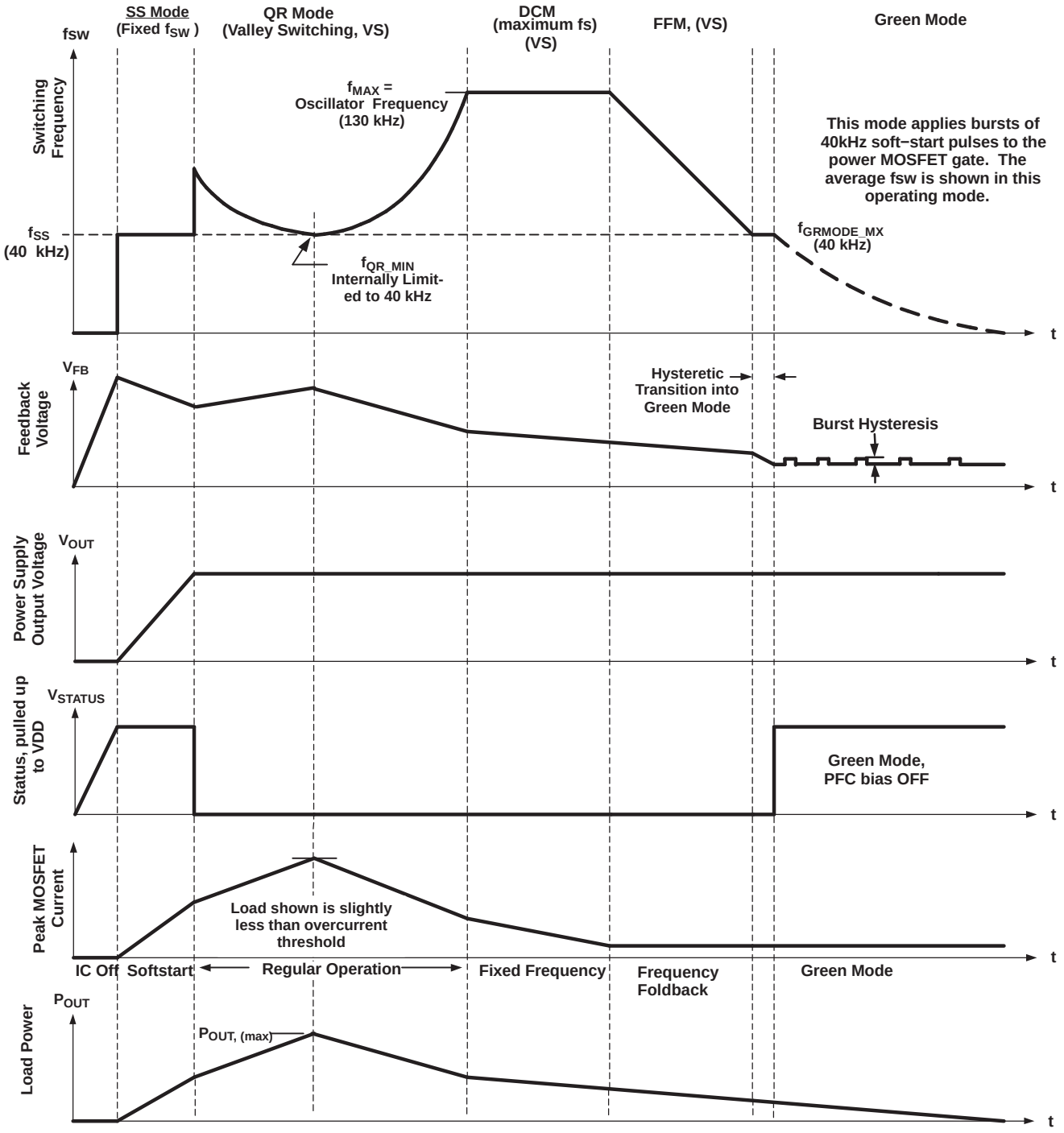


Figure 4. Operation Mode Switching Frequencies

Details of the functional boxes in the Block Diagram/Typical Application drawing are shown in Figure 5, Figure 6, Figure 7 and Figure 8. These figures conceptualize how the UCC28600-Q1 executes the command of the FB voltage to have the responses that are shown in Figure 2, Figure 3 and Figure 4. The details of the functional boxes also conceptualize the various fault detections and responses that are included in the UCC28600-Q1. During all modes of operation, this controller operates in current mode control. This allows the UCC28600-Q1 to monitor the FB voltage to determine and respond to the varying load levels such as heavy, light or ultra-light.

Quasi-resonant mode and DCM occurs for feedback voltages V_{FB} between 2.0 V and 4.0 V, respectively. In turn, the CS voltage is commanded to be between 0.4 V and 0.8 V. A cycle-by-cycle power limit imposes a fixed 0.8-V limit on the CS voltage. An overcurrent shutdown threshold in the fault logic gives added protection against high-current, slew-rate shorted winding faults, shown in Figure 8. The power limit feature in the QR DETECT circuit of Figure 7 adds an offset to the CS signal that is proportional to the line voltage. The power limit feature is programmed with R_{PL}, as shown in the typical applications diagram.

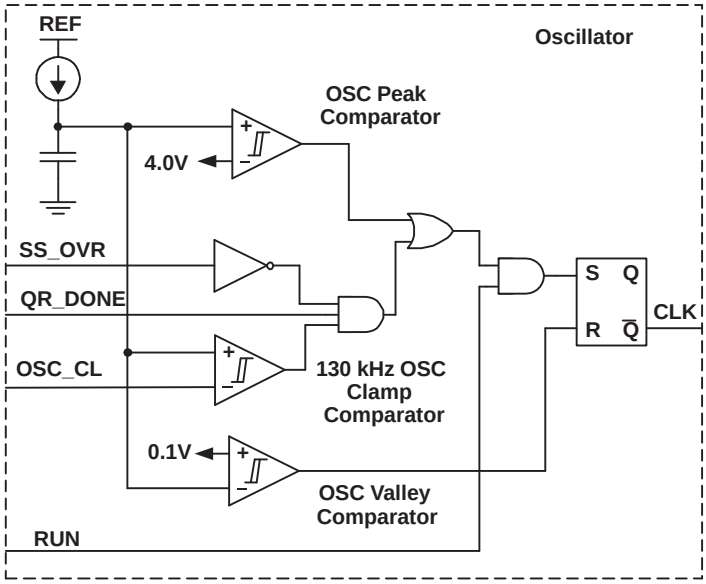


Figure 5. Oscillator Details

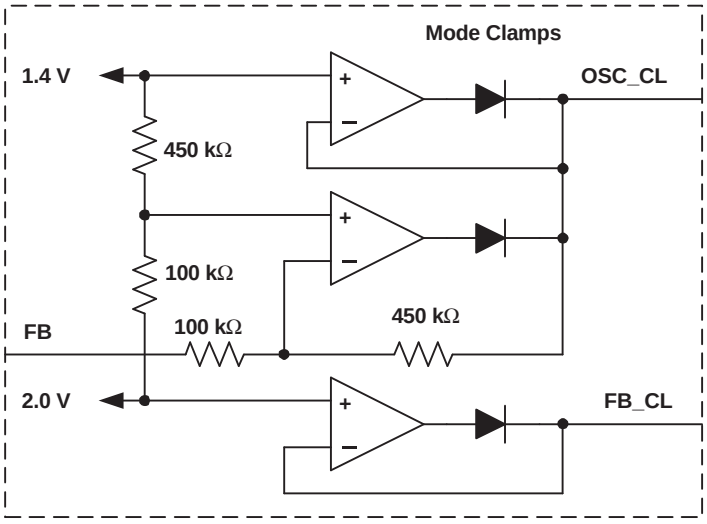


Figure 6. Mode Clamp Details

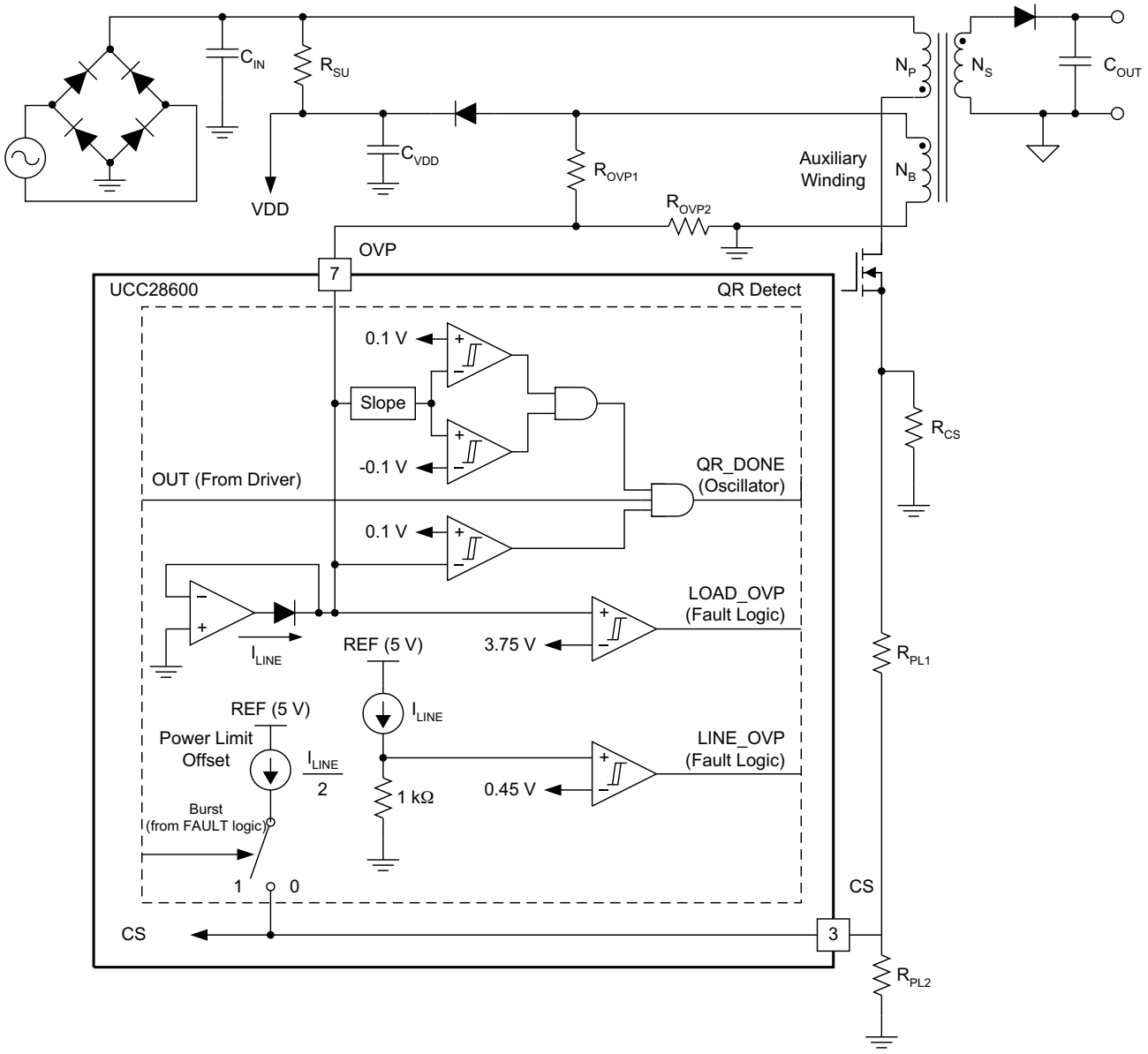


Figure 7. QR Detect Details

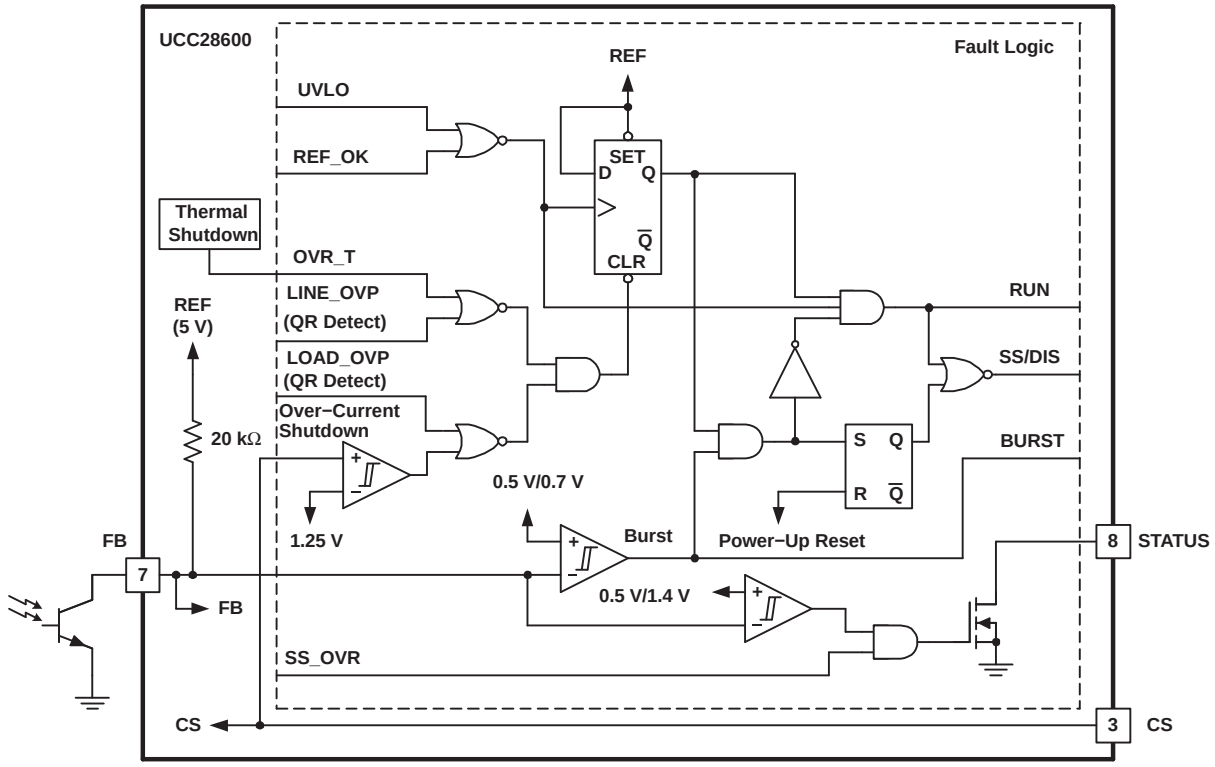


Figure 8. Fault Logic Details

Quasi-Resonant / DCM Control

Quasi-resonant (QR) and DCM operation occur for feedback voltages V_{FB} between 2.0 V and 4.0 V. In turn, the peak CS voltage is commanded to be between 0.4 V and 0.8 V. During this control mode, the rising edge of OUT always occurs at the valley of the resonant ring after demagnetization. Resonant valley switching is an integral part of QR operation. Resonant valley switching is also imposed if the system operates at the maximum switching frequency clamp. In other words, the frequency varies in DCM operation in order to have the switching event occur on the first resonant valley that occurs after a 7.7-µs (130-kHz) interval. Notice that the CS pin has an internal dependent current source, 1/2 I_{LINE}. This current source is part of the cycle-by-cycle power limit function that is discussed in the Protection Features section.

Frequency Foldback Mode Control

Frequency foldback mode uses elements of the FAULT LOGIC, shown in Figure 8 and the mode clamp circuit, shown in Figure 6. At the minimum operating frequency, the internal oscillator sawtooth waveform has a peak of 4.0 V and a valley of 0.1 V. When the FB voltage is between 2.0 V and 1.4 V, the FB_CL signal in Figure 6 commands the oscillator in a voltage controlled oscillator (VCO) mode by clamping the peak oscillator voltage. The additional clamps in the OSCILLATOR restrict VCO operation between 40 kHz and 130 kHz. The FB_CL voltage is reflected to the modulator comparator effectively clamping the reflected CS command to 0.4 V.

Green-Mode Control

Green mode uses element of the fault logic, shown in Figure 8 and the mode clamps circuit, shown in Figure 6. The OSC_CL signal clamps the Green-mode operating frequency at 40 kHz. Thus, when the FB voltage is between 1.4 V and 0.5 V, the controller is commanding an excess of energy to be transferred to the load which in turn, drives the error higher and FB lower. When FB reaches 0.5 V, OUT pulses are terminated and do not resume until FB reaches 0.7 V. In this mode, the converter operates in hysteretic control with the OUT pulse terminated at a fixed CS voltage level of 0.4 V. The power limit offset is turned OFF during Green mode and it returns to ON when FB is above 1.4 V, as depicted in Figure 8. Green mode reduces the average switching frequency in order to minimize switching losses and increase the efficiency at light load conditions.

Fault Logic

Advanced logic control coordinates the fault detections to provide proper power supply recovery. This provides the conditioning for the thermal protection. Line overvoltage protection (line OVP) and load OVP are implemented in this block. It prevents operation when the internal reference is below 4.5 V. If a fault is detected in the thermal shutdown, line OVP, load OVP, or REF, the UCC28600-Q1 undergoes a shutdown/retry cycle.

Refer to the fault logic diagram in Figure 8 and the QR detect diagram in Figure 7 to program line OVP and load OVP. To program the load OVP, select the R_{OVP1} – R_{OVP2} divider ratio to be 3.75 V at the desired output shut-down voltage. To program line OVP, select the impedance of the R_{OVP1} – R_{OVP2} combination to draw 450 μA when the V_{OVP} is 0.45 V during the ON-time of the power MOSFET at the highest allowable input voltage.

Oscillator

The oscillator, shown in Figure 5, is internally set and trimmed so it is clamped by the circuit in Figure 5 to a nominal 130-kHz maximum operating frequency. It also has a minimum frequency clamp of 40 kHz. If the FB voltage tries to drive operation to less than 40 kHz, the converter operates in green mode.

Status

The STATUS pin is an open drain output, as shown in Figure 8. The status output goes into the OFF-state when FB falls below 0.5 V and it returns to the ON-state (low impedance to GND) when FB rises above 1.4 V. This pin is used to control bias power for a PFC stage, as shown in Figure 9. Key elements for implementing this function include Q_{ST}, R_{ST1} and R_{ST2}, as shown in the figure. Resistors R_{ST1} and R_{ST2} are selected to saturate Q_{ST} when it is desirable for the PFC to be operational. During green mode, the STATUS pin becomes a high impedance and R_{ST1} causes Q_{ST} to turn-OFF, thus saving bias power. If necessary, use a zener diode and a resistor (D_{Z1} and R_{CC}) to maintain V_{CC} in the safe operating range of the PFC controller. Note the D_{VDD} - C_{VDD} combination is in addition to the standard D_{BIAS} - C_{BIAS} components. This added stage is required to isolate the STATUS circuitry from the startup resistor, R_{SU}, to ensure there is no conduction through STATUS when VDD is below the UVLO turn-on threshold.

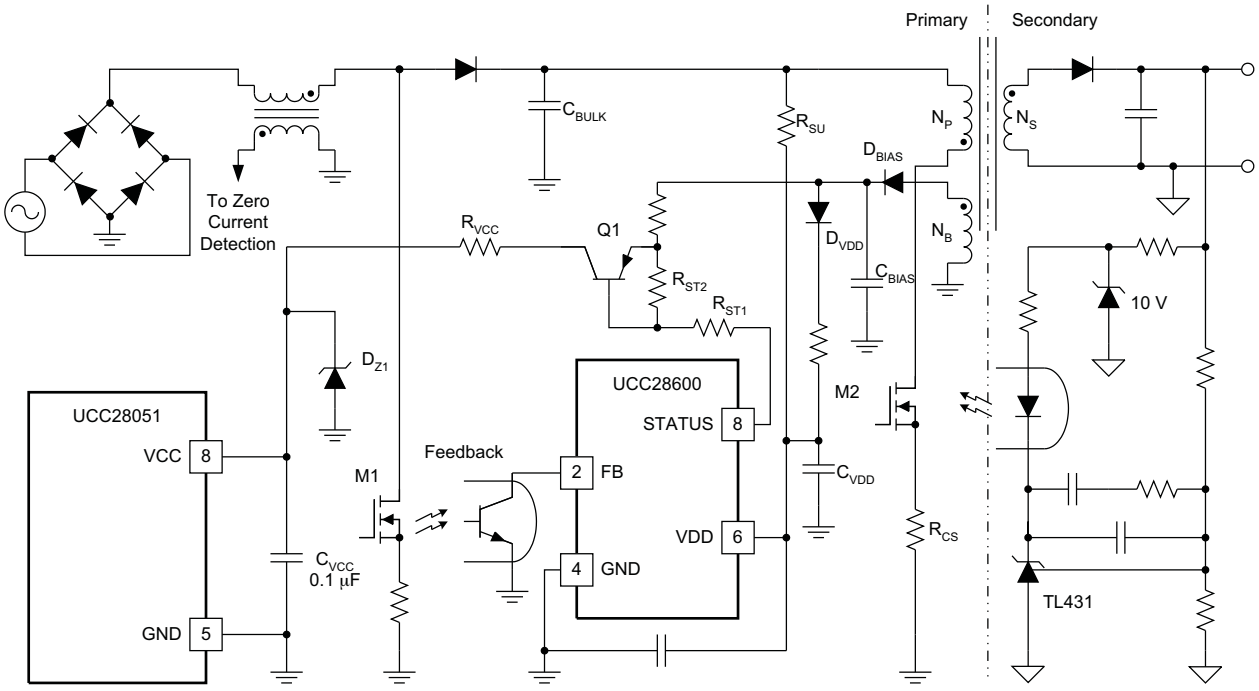


Figure 9. Using STATUS for PFC Shut-Down During Green Mode

Operating Mode Programming

Boundaries of the operating modes are programmed by the flyback transformer and the four components R_{PL}, R_{CS}, R_{OVP1} and R_{OVP2}; shown in the Block Diagram/Application drawing.

The transformer characteristics that predominantly affect the modes are the magnetizing inductance of the primary and the magnitude of the output voltage, reflected to the primary. To a lesser degree (yet significant), the boundaries are affected by the MOSFET output capacitance and transformer leakage inductance. The design procedure here is to select a magnetizing inductance and a reflected output voltage that operates at the DCM/CCM boundary at maximum load and maximum line. The actual inductance should be noticeably smaller to account for the ring between the magnetizing inductance and the total stray capacitance measured at the drain of the power MOSFET. This programs the QR/DCM boundary of operation. All other mode boundaries are preset with the thresholds in the oscillator and green-mode blocks.

The four components R_{PL}, R_{CS}, R_{OVP1} and R_{OVP2} must be programmed as a set due to the interactions of the functions. The use of the UCC28600-Q1 design calculator, TI Literature Number SLVC104, is highly recommended in order to achieve the desired results with a careful balance between the transformer parameters and the programming resistors.

Protection Features

The UCC28600-Q1 has many protection features that are found only on larger, full featured controllers. Refer to the Block Diagram/Typical Application and Figures 1, 4, 5, 6 and 7 for detailed block descriptions that show how the features are integrated into the normal control functions.

Overtemperature

Overtemperature lockout typically occurs when the substrate temperature reaches 140°C. Retry is allowed if the substrate temperature reduces by the hysteresis value. Upon an overtemperature fault, C_{SS} on softstart is discharged and STATUS is forced to a high impedance.

Cycle-by-Cycle Power Limit

The cycle terminates when the CS voltage plus the power limit offset exceeds 1.2 V.

In order to have power limited over the full line voltage range of the QR Flyback converter, the CS pin voltage must have a component that is proportional to the primary current plus a component that is proportional to the line voltage due to predictable switching frequency variations due to line voltage. At power limit, the CS pin voltage plus the internal CS offset is compared against a constant 1.2-V reference in the PWM comparator. Thus during cycle-by-cycle power limit, the peak CS voltage is typically 0.8 V.

The current that is sourced from the OVP pin (I_{LINE}) is reflected to a dependent current source of ½ I_{LINE}, that is connected to the CS pin. The power limit function can be programmed by a resistor, R_{PL}, that is between the CS pin and the current sense resistor. The current, I_{LINE}, is proportional to line voltage by the transformer turns ratio N_B/N_P and resistor R_{OVP1}. Current I_{LINE} is programmed to set the line over voltage protection. Resistor R_{PL} results in the addition of a voltage to the current sense signal that is proportional to the line voltage. The proper amount of additional voltage has the effect of limiting the power on a cycle-by-cycle basis. Note that R_{CS}, R_{PL}, R_{OVP1} and R_{OVP2} must be adjusted as a set due to the functional interactions.

Current Limit

When the primary current exceeds maximum current level which is indicated by a voltage of 1.25 V at the CS pin, the device initiates a shutdown. Retry occurs after a $UVLO_{OFF}/UVLO_{ON}$ cycle.

Over-Voltage Protection

Line and load over voltage protection is programmed with the transformer turn ratios, R_{OVP1} and R_{OVP2}. The OVP pin has a 0-V voltage source that can only source current; OVP cannot sink current.

Line over voltage protection occurs when the OVP pin is clamped at 0 V. When the bias winding is negative, during OUT = HI or portions of the resonant ring, the 0-V voltage source clamps OVP to 0 V and the current that is sourced from the OVP pin is mirrored to the Line_OVP comparator and the QR detection circuit. The Line_OVP comparator initiates a shutdown-retry sequence if OVP sources any more than 450 μA.

Load-over voltage protection occurs when the OVP pin voltage is positive. When the bias winding is positive, during demagnetization or portions of the resonant ring, the OVP pin voltage is positive. If the OVP voltage is greater than 3.75 V, the device initiates a shutdown. Retry occurs after a $UVLO_{OFF}/UVLO_{ON}$ cycle.

Undervoltage Lockout

Protection is provided to guard against operation during unfavorable bias conditions. Undervoltage lockout (UVLO) always monitors VDD to prevent operation below the UVLO threshold.

TYPICAL CHARACTERISTICS

CLAMP VOLTAGE
vs
TEMPERATURE

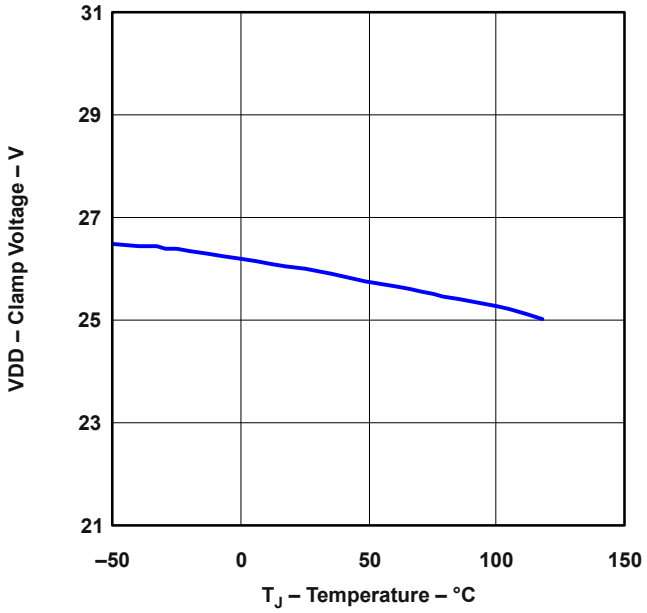


Figure 10.

SWITCHING FREQUENCY
vs
TEMPERATURE

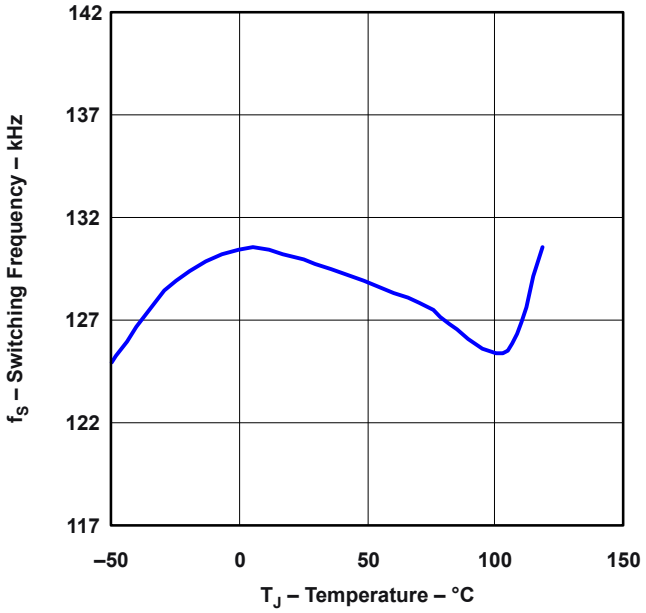


Figure 11.

PL THRESHOLD
vs
TEMPERATURE

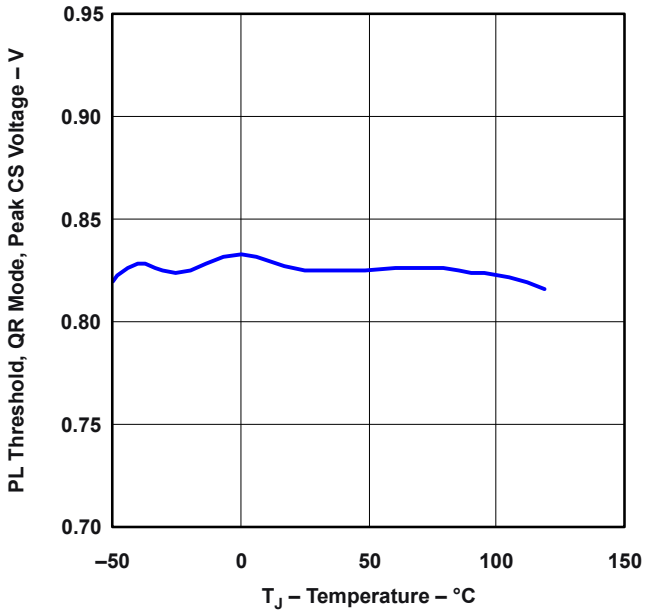


Figure 12.

OVER VOLTAGE PROTECTION THRESHOLD
vs
TEMPERATURE

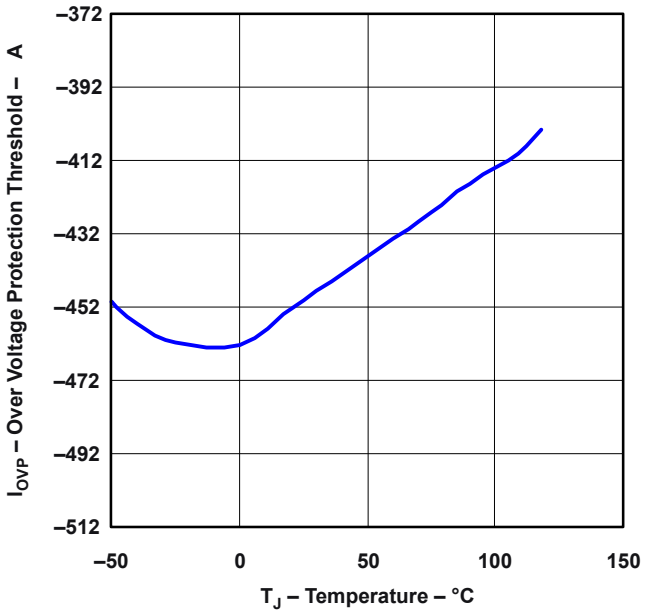


Figure 13.

PRACTICAL DESIGN NOTES

Non-Ideal Current Sense Value

Resistors R_{CS}, R_{PL}, R_{OVP1} and R_{OVP2} must be programmed as a set due to functional interactions in the converter. Often, the ideal value for R_{CS} is not available because the selection range of current sense resistors is too coarse to meet the required power limit tolerances. This issue can be solved by using the next larger available value of R_{CS} and use a resistive divider with a Thevenin resistance that is equal to the ideal R_{PL} value in order to attenuate the CS signal to its ideal value, as shown in Figure 14. The equations for modifying the circuit are:

$$R_{PL1} = R_{PL} \times \left(\frac{R_{CS}}{R_{DCS}} \right) \tag{4}$$

- R_{DCS} = ideal, but non-standard, value of current sense resistor.
- R_{PL} = previously calculated value of the power limit resistor.

$$R_{PL2} = \frac{R_{PL1}}{\left(\frac{R_{CS}}{R_{DCS}} \right) - 1} \tag{5}$$

- R_{CS} = available, standard value current sense resistor.

The board should be laid out to include R_{PL2} in order to fascillitate final optimization of the design based upon readily available components.

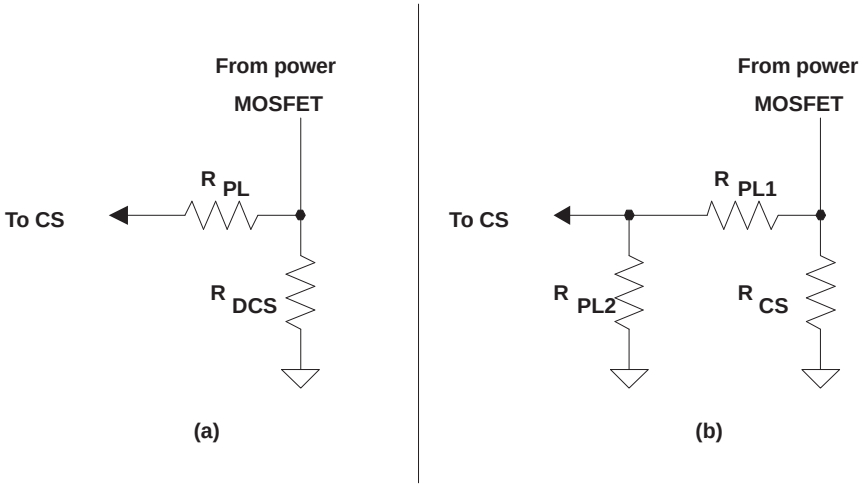


Figure 14. Modifications to Fit a Standard Current Sense Resistor Value

Snubber Damping

Resonance between the leakage inductance and the MOSFET drain capacitance can cause false load-OVP faults, in spite of the typical 2-µs delay in load-OVP detection. The bias winding is sensitive to the overshoot and ringing because it is well coupled to the primary winding. A technique to eliminate the problem is to use an R^2CD snubber instead of an RCD snubber, shown in Figure 15. A damping resistor added to the RCD snubber reduces ringing between the drain capacitor and the inductance when the snubber diode commutates OFF.

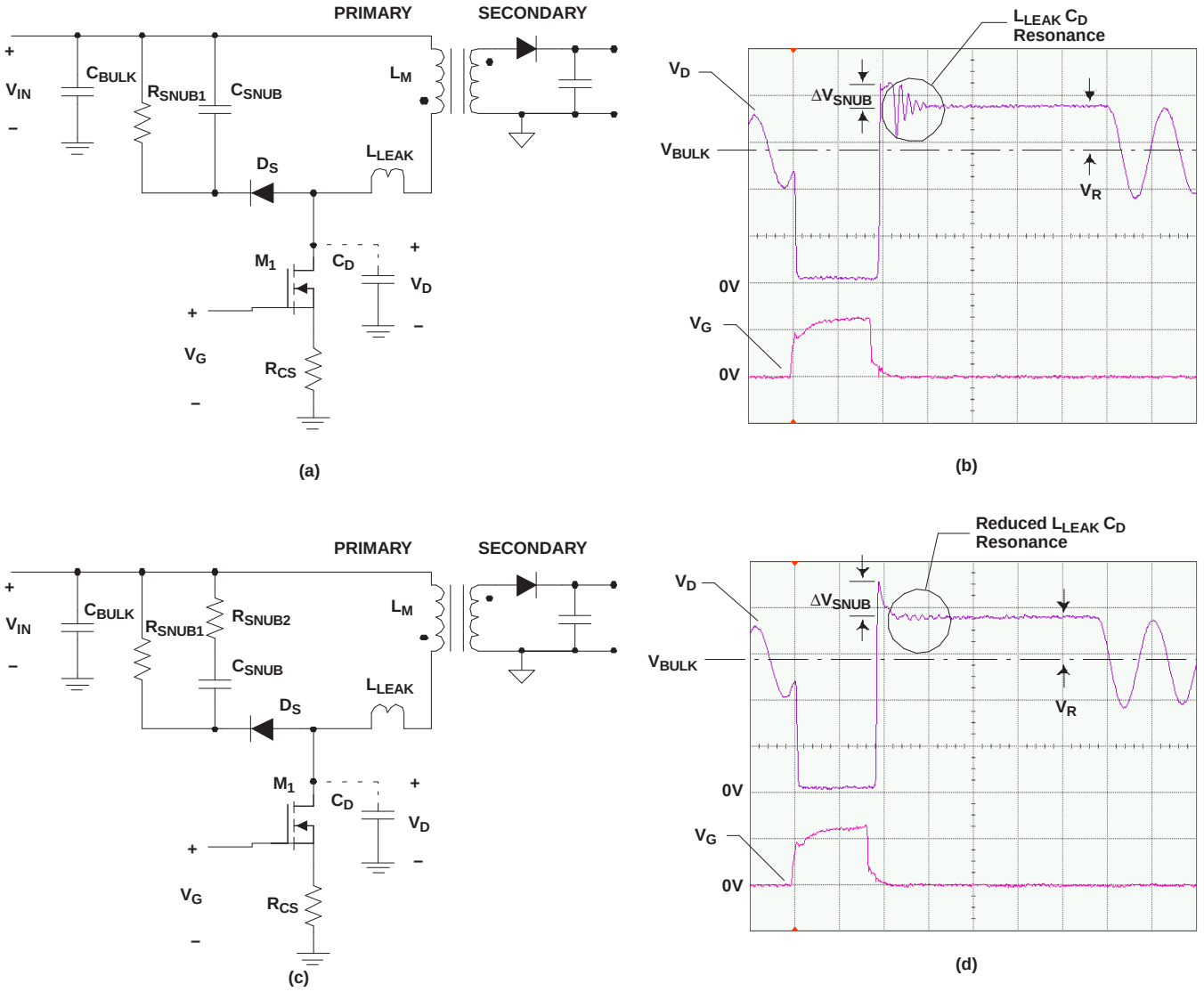


Figure 15. (a) RCD Snubber, (b) RCD Snubber Waveform, (c) R^2CD Snubber, (d) R^2CD Snubber Waveform

Begin the design of the R^2CD using the same procedure as designing an RCD snubber. Then, add the damping resistor, R_{SNUB2}. The procedure is as follows:

$$\text{Pick } \frac{\Delta V_{SNUB}}{V_R} = \text{ between 0.5 and 1} \tag{6}$$

Select a capacitor for ΔV_{SNUB}:

$$C_{SNUB} = \frac{I_{cs(peak)}{}^2 L_{LEAK}}{\left(V_R + \Delta V_{SNUB}\right)^2 - V_R{}^2} \tag{7}$$

Pick R_{SNUB} to discharge C_{SNUB}:

$$R_{SNUB1} = \left(\frac{1}{2} + \frac{V_R}{\Delta V_{SNUB}}\right)\frac{1}{C_{SNUB}}\left(\frac{1}{f_{S(max)}} - \frac{L_{LEAK} I_{CS(peak)}}{\Delta V_{SNUB}}\right) \tag{8}$$

$$P\left(R_{SNUB1}\right) = \frac{\left(V_R + \frac{\Delta V_{SNUB}}{2}\right)^2 \times \left[1 + \left(\frac{1}{3}\right) \times \left[\frac{1}{\frac{V_R}{V_{SNUB}} + \frac{1}{2}}\right]\right]^2}{R_{SNUB1}} \tag{9}$$

Pick R_{SNUB2} to dampen the L_{LEAK}-C_{SNUB} resonance with a Q that is between 1.7 and 2.2:

$$R_{SNUB2} = \frac{\Delta V_{SNUB}}{I_{CS(peak)}} \tag{10}$$

$$P\left(R_{SNUB}\right) = I_{CS(peak)}{}^2 R_{SNUB2}\left[\frac{1}{3}\frac{L_{LEAK} f_{S(max)}}{\left(V_R + \frac{\Delta V_{SNUB}}{2}\right)}\right] \tag{11}$$

For the original selection of ΔV_{SNUB},

$$Q = \sqrt{\frac{2V_R}{\Delta V_{SNUB}} + 1} \tag{12}$$

REFERENCES

1. Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature Number SLUP133
2. Datasheet, *UCC3581 Micro Power PWM Controller*, Texas Instruments Literature Number SLUS295
3. Datasheet, *UCC28051 Transition Mode PFC Controller*, Texas Instruments Literature Number SLUS515
4. UCC28600-Q1 Design Calculator, *A QR Flyback Designer.xls*, spreadsheet for Microsoft Excel 2003, Texas Instruments Literature Number SLVC104
5. Design Considerations for the UCC28600-Q1, Texas Instruments Literature Number SLUA399

RELATED PRODUCTS

- UCC28051 Transition Mode PFC Controller (SLUS515)
- UCC3581 Micro Power PWM Controller (SLUS295)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28600TDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28600T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC28600-Q1 :

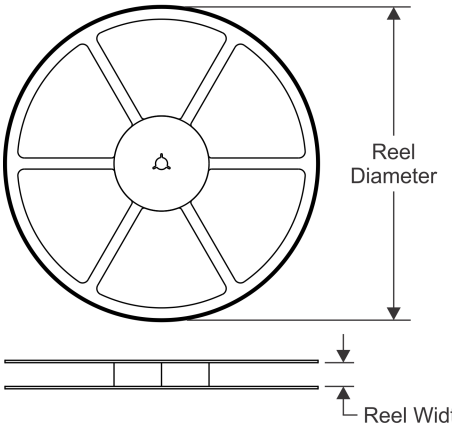
- Catalog: UCC28600

NOTE: Qualified Version Definitions:

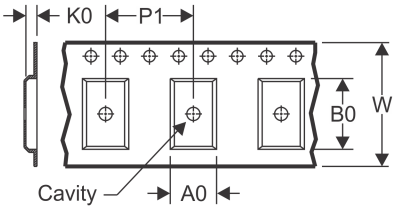
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

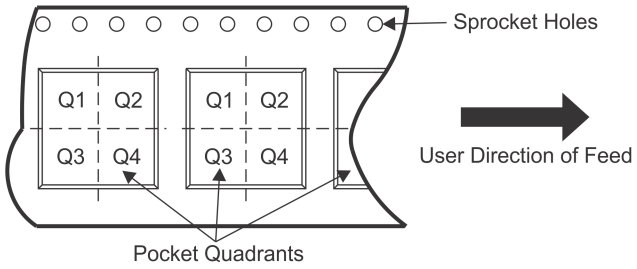


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

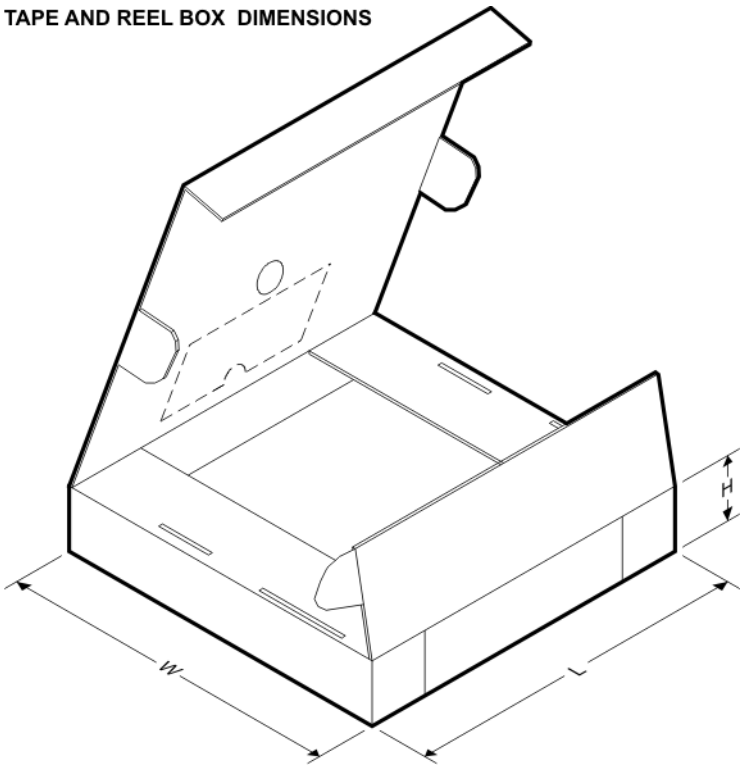
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28600TDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

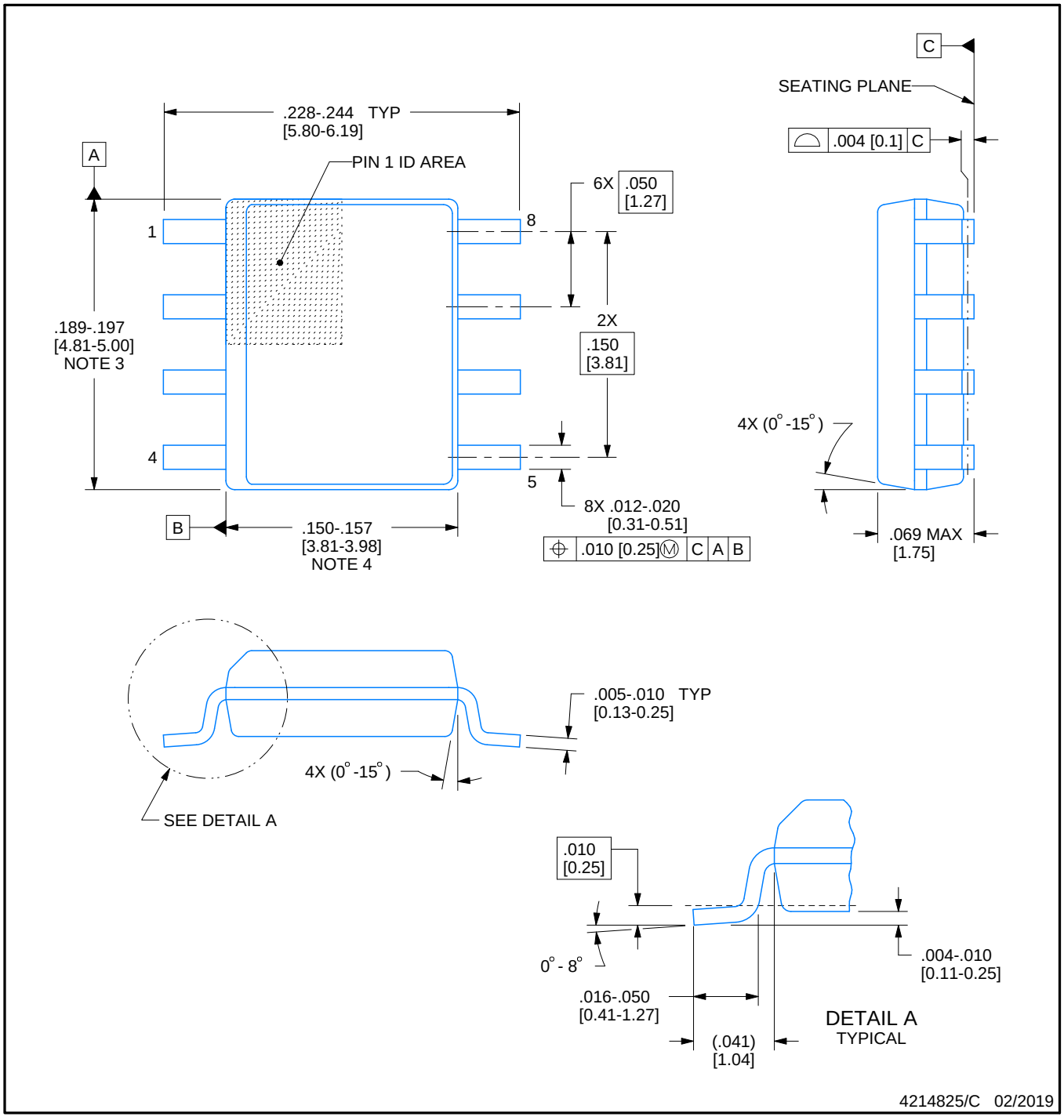
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28600TDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

PACKAGE OUTLINE

D0008A

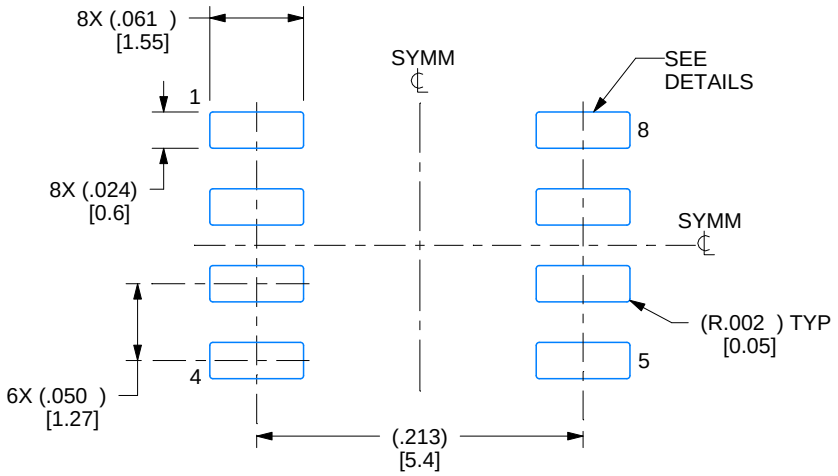
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

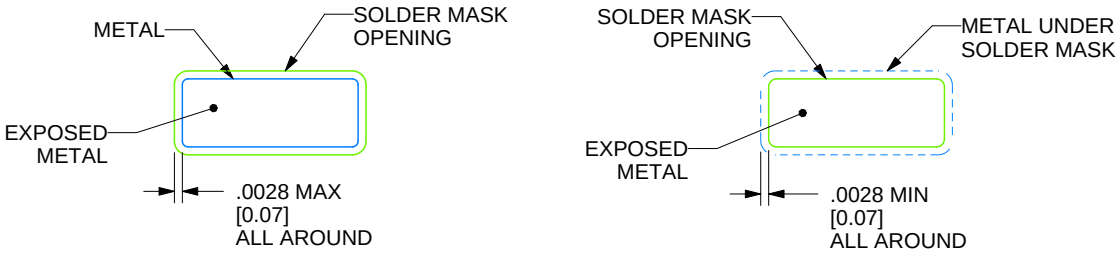


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

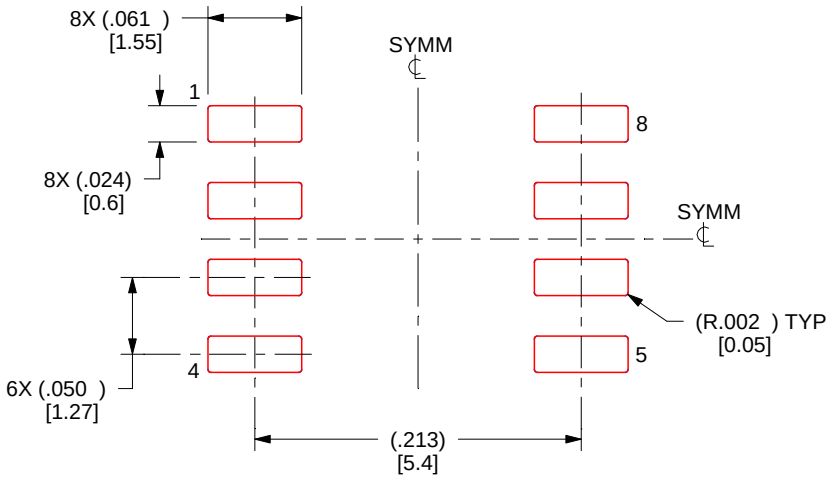
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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