TPS6242x 2.25-MHz 600-mA and 1000-mA Dual Step-Down Converter in Small 3-mm × 3-mm VSON Package

1 Features

- High Efficiency up to 95%
- V_{IN} Range from 2.5 V to 6 V
- 2.25-MHz Fixed Frequency Operation
- Output Current 600 mA and 1000 mA
- Adjustable Output Voltage from 0.6 V to V_{IN}
- Pin Selectable Output Voltage Supports Simple Dynamic Voltage Scaling
- Optional EasyScale™ One-Pin Serial Interface for Dynamic Output Voltage Adjustment
- Power-Save Mode at Light Load Currents
- 180° Out of Phase Operation
- Output Voltage Accuracy in PWM Mode ±1%
- Typical 32-μA Quiescent Current for both Converters
- 100% Duty Cycle for Lowest Dropout
- Available in a 10-Pin VSON (3 mm × 3 mm)

2 Applications

- Cell Phones, Smart-phones
- PDAs, Pocket PCs
- OMAP™ and Low Power DSP Supply
- Portable Media Players
- Digital Radios
- Digital Cameras

3 Description

The TPS6242x device is a synchronous dual step-down DC–DC converter. It provides two independent output voltage rails powered by 1-cell Li-Ion or 3-cell NiMH/NiCD batteries. The device is also suitable to operate from a standard 3.3-V or 5-V voltage rail.

With an input voltage range of 2.5 V to 6 V, the TPS6242x is ideal for battery-powered portable applications like smart phones, PDAs, and other portable equipment.

With the EasyScale™ serial interface the output voltages can be modified during operation. It therefore supports dynamic voltage scaling for low power DSP and processors.

The TPS6242x operates at 2.25-MHz fixed switching frequency and enter the power-save mode operation at light load currents to maintain high efficiency over the entire load current range. For low-noise applications the devices can be forced into fixed-frequency PWM mode by pulling the MODE/DATA pin High. In the shutdown mode, the current consumption is reduced to 1.2 μA. The device allows the use of small inductors and capacitors to achieve a small solution size.

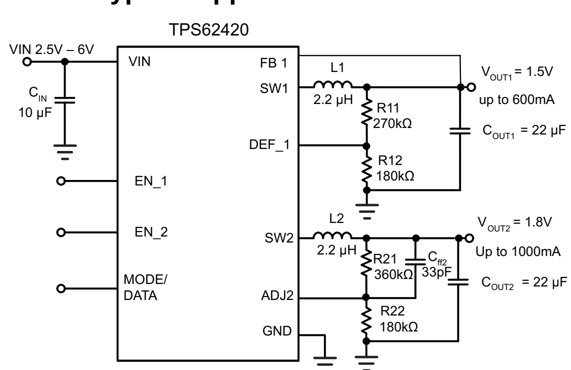
The TPS6242x operates over a free-air temperature range of –40°C to 85°C. It is available in a 10-pin leadless package (3 mm × 3 mm VSON)

Device Information(1)

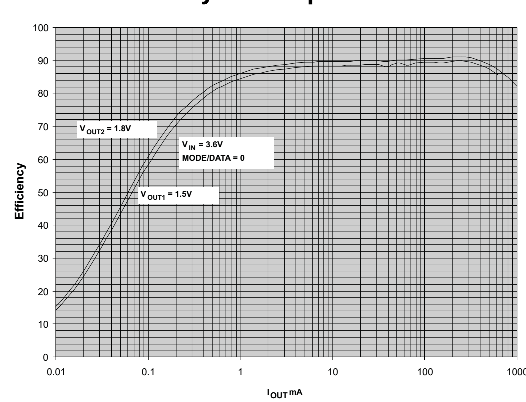
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62420 TPS62421	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2010) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

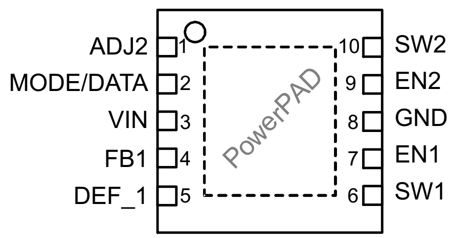
5 Device Comparison Table

PART NUMBER	DEFAULT OUTPUT VOLTAGE(1)		OUTPUT CURRENT	PACKAGE(2)	ORDERING(3)	PACKAGE MARKING
TPS62420	OUT1	Adjustable	600 mA	DRC	TPS62420DRC	BQF
	OUT2		1000 mA			
TPS62421	OUT1: DEF_1 = Low	1.2 V	600 mA		TPS62421DRC	QTQ
	OUT1: DEF_1 = High	1.8 V				
	OUT2	1.8 V	1000 mA			

(1) Contact TI for other fixed output voltage options.
(2) The DRC (VSON 10 PIN) package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.
(3) For the most current ordering information see the *Mechanical, Packaging, and Orderable Information* section or see the TI website www.ti.com.

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ2	1	I	Input to adjust output voltage of converter 2. In adjustable version (TPS62420) connect an external resistor divider between V_{OUT2}, this pin and GND to set output voltage between 0.6 V and V_{IN}. If EasyScale™ interface is used for converter 2, this pin must be directly connected to the output.
MODE/DATA	2	I	This Pin has 2 functions: 1. Operation mode selection: With low level, power-save mode is enabled where the device operates in PFM mode at light loads and enters automatically PWM mode at heavy loads. Pulling this PIN to High forces the device to operate in PWM mode over the whole load range. 2. EasyScale™ interface function: One wire serial interface to change the output voltage of both converters. The pin has an open-drain output to provide an acknowledge condition if requested. The current into the open-drain output stage may not exceed 500 µA. The interface is active if either EN1 or EN2 is High.
VIN	3	I	Supply voltage, connect to VBAT, 2.5 V to 6 V
FB1	4	I	Direct feedback voltage sense input of converter 1, connect directly to V_{OUT1}. An internal feed-forward capacitor is connected between this pin and the error amplifier. In case of fixed output voltage versions or when the interface is used, this pin is connected to an internal resistor divider network.
DEF_1	5	I/O	This pin defines the output voltage of converter 1. The pin acts in TPS62420 as an analog input for output voltage setting through external resistors. In fixed default output voltage versions this pin is a digital input to select between two fixed default output voltages, see table ordering information. In TPS62420 an external resistor network needs to be connected to this pin to adjust the default output voltage.
SW1	6	–	Switch pin of converter 1. Connected to inductor
EN1	7	I	Enable input for converter 1, active high
GND	8	I	GND for both converters, this pin should be connected with the PowerPAD
EN2	9	I/O	Enable input for converter 2, active high

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SW2	10	–	Switch pin of converter 2. Connected to inductor.
PowerPAD™	–	–	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
	Input voltage on V_{IN} [2]	–0.3	7	V
	Voltage on EN, MODE/DATA, DEF_1	–0.3	V_{IN} +0.3, ≤7	V
	Maximum current into MODE/DATA		500	µA
	Voltage on SW1, SW2	–0.3	7	V
	Voltage on ADJ2, FB1	–0.3	V_{IN} +0.3, ≤7	V
$T_{J(max)}$	Maximum junction temperature		150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage	2.5	6	V
	Output voltage range for adjustable voltage	0.6	V_{IN}	V
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS62420, TPS62421	UNIT
		DRC (VSON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 20 µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		6	V
I_Q	Operating quiescent current	One converter, I_{OUT} = 0 mA. PFM mode enabled (Mode = 0) device not switching, EN1 = 1 or EN2 = 1		19	29	µA
		Two converter, I_{OUT} = 0 mA. PFM mode enabled (Mode = 0) device not switching, EN1 = 1 and EN2 = 1		32	48	µA
		I_{OUT} = 0 mA, MODE/DATA = GND, for one converter, V_{OUT} 1.575 V(1)		23		µA
		I_{OUT} = 0 mA, MODE/DATA = V_{IN}, for one converter, V_{OUT} 1.575 V(1)		3.6		mA
I_{SD}	Shutdown current	EN1, EN2 = GND, V_{IN} = 3.6 V(2)		1.2	3	µA
		EN1, EN2 = GND, V_{IN} ramped from 0 V to 3.6 V(3)		0.1	1	
V_{UVLO}	Undervoltage lockout threshold	Falling		1.5	2.35	V
		Rising			2.4	
ENABLE EN1, EN2						
V_{IH}	High-level input voltage, EN1, EN2		1.2		V_{IN}	V
V_{IL}	Low-level input voltage, EN1, EN2		0		0.4	V
I_{IN}	Input bias current, EN1, EN2	EN1, EN2 = GND or V_{IN}		0.05	1.0	µA
DEF_1 INPUT						
V_{DEF_1H}	DEF_1 high level input voltage	DEF_1 pin is a digital input at fixed output voltage options (TPS62421)	0.9		V_{IN}	V
V_{DEF_1L}	DEF_1 low level input voltage		0		0.4	
I_{IN}	Input biasd current DEF_1	DEF_1 = GND or V_{IN}		0.01	1	µA
MODE/DATA						
V_{IH}	High-level input voltage, MODE/DATA		1.2		V_{IN}	V
V_{IL}	Low-level input voltage, MODE/DATA		0		0.4	V
I_{IN}	Input bias current, MODE/DATA	MODE/DATA = GND or V_{IN}		0.01	1	µA
V_{OH}	Acknowledge output voltage high	Open-drain, through external pullup resistor			V_{IN}	V
V_{OL}	Acknowledge output voltage low	Open-drain, sink current 500 µA	0		0.4	V
INTERFACE TIMING						
t_{Start}	Start time		2			µs
t_{H_LB}	High time low bit, logic 0 detection	Signal level on MODE/DATA pin is > 1.2 V	2		200	µs
t_{L_LB}	Low time low bit, logic 0 detection	Signal level on MODE/DATA pin < 0.4 V	2x t_{H_LB}		400	µs
t_{L_HB}	Low time high bit, logic 1 detection	Signal level on MODE/DATA pin < 0.4 V	2		200	µs
t_{H_LB}	High time high bit, logic 1 detection	Signal level on MODE/DATA pin is > 1.2 V	2x t_{L_HS}		400	µs
T_{EOS}	End of Stream	T_{EOS}	2			µs

(1) Device is switching with no load on the output, L = 3.3 µH, value includes losses of the coil
(2) These values are valid after the device has been already enabled one time (EN1 or EN2 = High) and supply voltage V_{IN} has not powered down.
(3) After the first enable, these values are valid when the device is disabled (EN1 and EN2 = Low) and supply voltage V_{IN} is powered up. The values remain valid until the device has been enabled first time (EN1 or EN2 = high).

Electrical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 20 µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ACKN}	Duration of acknowledge condition (MODE/DATE line pulled low by the device)	V_{IN} 2.5 V to 6 V	400		520	µs
t_{valACK}	Acknowledge valid time				2	µs
$t_{timeout}$	Time-out for entering power-save mode	MODE/DATA pin changes from high to low			520	µs
POWER SWITCH						
$R_{DS(ON)}$	P-channel MOSFET on-resistance, converter 1, 2	V_{IN} = V_{GS} = 3.6 V		280	620	mΩ
I_{LK_PMOS}	P-channel leakage current	V_{DS} = 6 V			1	µA
$R_{DS(ON)}$	N-channel MOSFET on-resistance converter 1, 2	V_{IN} = V_{GS} = 3.6 V		200	450	mΩ
$I_{LK\_SW1/SW2}$	Leakage current into SW1/SW2 pin	Includes N-Chanel leakage current, V_{IN} = open, V_{SW} = 6 V, EN = GND(4)		6	7.5	µA
I_{LIMF}	Forward current limit PMOS and NMOS — OUT1 600 mA	2.5 V ≤ V_{IN} ≤ 6 V	0.85	1.0	1.15	A
	Forward current limit PMOS and NMOS — OUT2 1000 mA		1.19	1.4	1.61	A
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency	2.5 V ≤ V_{IN} ≤ 6 V	2.0	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Adjustable output voltage range		0.6		V_{IN}	V
V_{ref}	Reference voltage			600		mV
$V_{OUT\ (PFM)}$	DC output voltage accuracy PFM mode, adjustable and fixed output voltage(5)	Voltage positioning active, MODE/DATA = GND, device operating in PFM mode, V_{IN} = 2.5 V to 5 V (6) (7)	–1.5%	1.01 × V_{OUT}	2.5%	
V_{OUT}		MODE/DATA = GND; device operating in PWM mode V_{IN} = 2.5 V to 6 V(7)	–1%	0%	1%	
		V_{IN} = 2.5 V to 6 V, Mode/Data = V_{IN} , Fixed PWM operation, 0 mA < I_{OUT} < I_{OUTMAX} (8)	–1%	0%	1%	
	DC output voltage load regulation	PWM operation mode			0.5	%/A
$t_{Start\ up}$	Start-up time	Activation time to start switching(9)		170		µs
t_{Ramp}	V_{OUT} Ramp UP time	Time to ramp from 5% to 95% of V_{OUT}		750		µs

(4) At pins SW1 and SW2 an internal resistor of 1 MΩ is connected to GND
(5) Output voltage specification does not include tolerance of external voltage programming resistors
(6) Configuration L typ 2.2 µH, C_{OUT} typical 20 µF, see parameter measurement information, the output voltage ripple depends on the effective capacitance of the output capacitor, larger output capacitors lead to tighter output voltage tolerance
(7) In power-save mode, PWM operation is typically entered at I_{PSM} = V_{IN}/32 Ω.
(8) For V_{OUT} > 2.2 V, V_{IN} min = V_{OUT} +0.3 V
(9) This time is valid if one converter turns from shutdown mode (EN2 = 0) to active mode (EN2 =1) and the other converter is already enabled (that is, EN1 = 1). In case both converters are turned from shutdown mode (EN1 and EN2 = Low) to active mode (EN1 and/or EN2 = 1) a value of typical 80 µs for ramp up of internal circuits needs to be added. After t_{Start} the converter starts switching and ramps V_{OUT}.

7.6 Dissipation Ratings

PACKAGE	$R_{\theta JA}$	POWER RATING FOR T_A ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C
DRC	49°C/W	2050 mW	21 mW/°C

7.7 Typical Characteristics

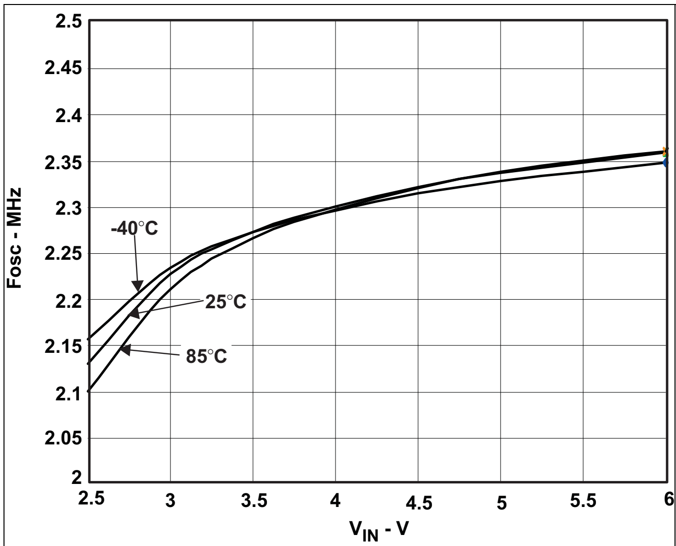


Figure 1. F_{OSC} vs V_{IN}

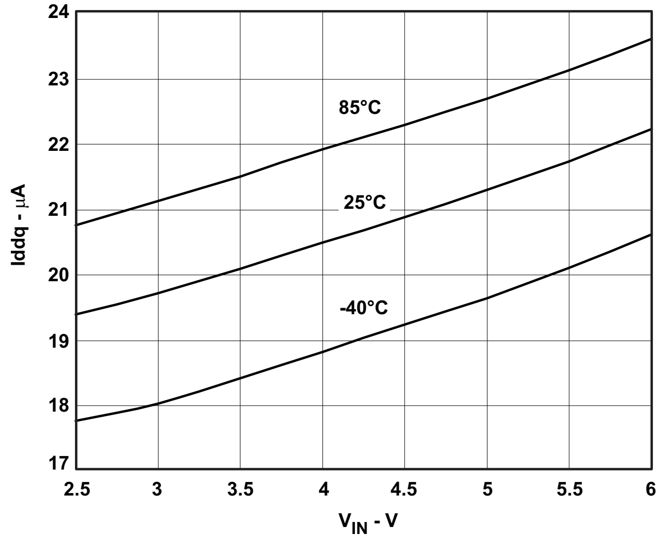


Figure 2. I_q For One Converter, Not Switching

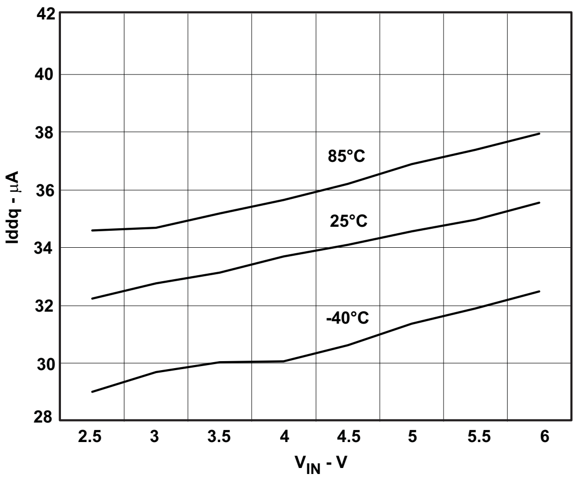


Figure 3. I_q For Both Converters, Not Switching

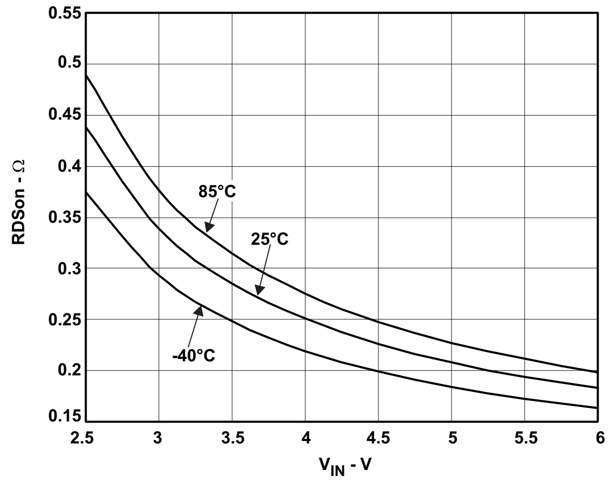


Figure 4. R_{DSON} PMOS vs V_{IN}

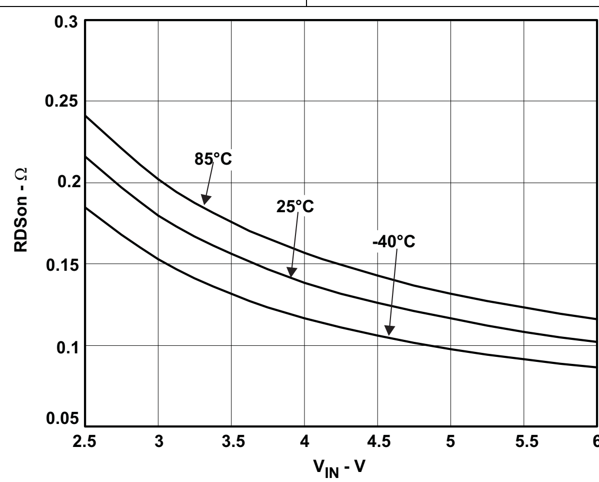


Figure 5. R_{DSON} NMOS vs V_{IN}

8 Detailed Description

8.1 Overview

The TPS6242x includes two synchronous step-down converters. The converters operate with typically 2.25-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. If power-save mode is enabled, the converters automatically enter power-save mode at light load currents and operate in pulse frequency modulation (PFM). During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

Each converter integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. If the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit. The two DC/DC converters operate synchronized to each other. A 180° phase shift between converter 1 and converter 2 decreases the input RMS current.

8.1.1 Converter 1

In the adjustable output voltage version TPS62420 the converter 1 output voltage can be set through an external resistor network on pin DEF_1, which operates as an analog input. In this case, the output voltage can be set in the range of 0.6 V to V_{IN}. The FB1 pin must be directly connected to the converter 1 output voltage V_{OUT1}. It feeds back the output voltage directly to the regulation loop.

The output voltage of converter 1 can also be changed by the EasyScale™ serial interface. This makes the device very flexible for output voltage adjustment. In this case, the device uses an internal resistor network.

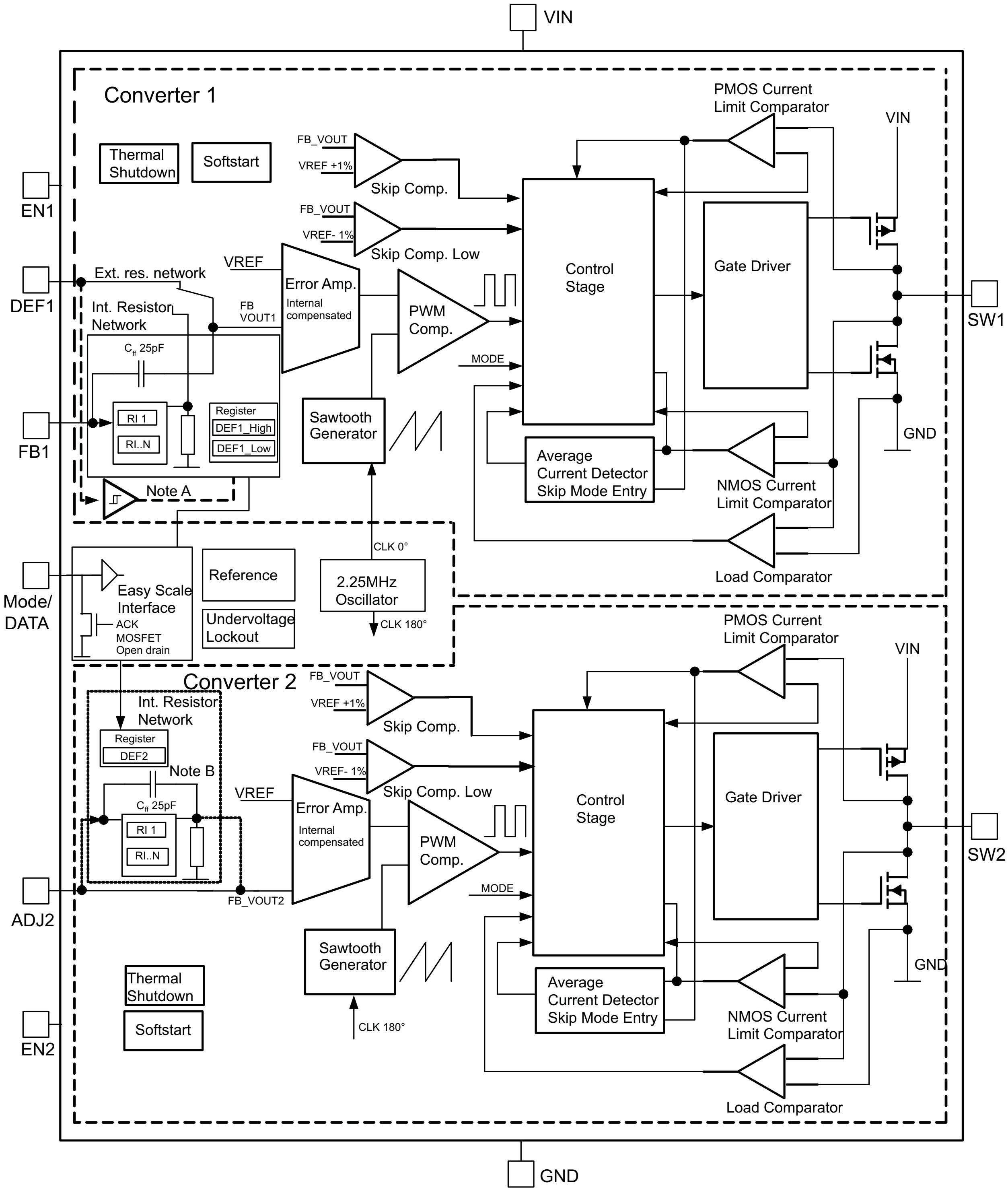
In the fixed default output voltage version like TPS62421, the DEF_1 pin is configured as a digital input. The converter 1 defaults to 1.2 V or 1.8 V depending on the level of DEF_1 pin. If DEF_1 is low the default is 1.2 V; if high, the default is 1.8 V. With the EasyScale™ interface, the output voltage for each DEF_1 pin condition (high or low) can be changed.

8.1.2 Converter 2

In the adjustable output voltage version TPS62420, the converter 2 output voltage is set by an external resistor divider connected to ADJ2 pin and uses an external feed-forward capacitor of 33 pF.

In fixed output voltage version TPS62421, the default output voltage is fixed to 1.8 V. In this case, the ADJ2 pin must be connected directly to the converter 2 output voltage V_{OUT2}. It is also possible to change the output voltage of converter 2 through the EasyScale™ interface. In this case, the ADJ2 pin must be directly connected to converter 2 output voltage V_{OUT2} and no external resistors may be connected.

8.2 Functional Block Diagram



A. In fixed output voltage version, the pin DEF_1 is connected to an internal digital input and disconnected from the error amplifier

B. To set the output voltage of converter 2 through EasyScale™ interface, ADJ2 pin must be directly connected to V_{OUT2}

8.3 Feature Description

8.3.1 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. It is activated in power-save mode operation. It provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to –2% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

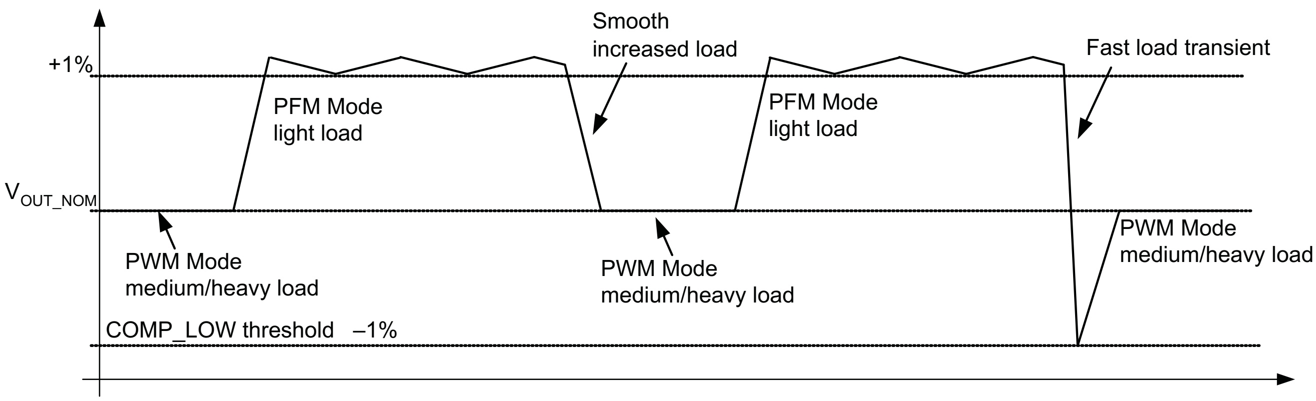


Figure 6. Dynamic Voltage Positioning

8.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the converters. The under-voltage lockout threshold is typically 1.5 V, maximum is 2.35 V. In case the default register values are overwritten by the interface, the new values in the registers REG_DEF_1_Low and REG_DEF_2 remain valid as long the supply voltage does not fall under the undervoltage lockout threshold, independent of whether the converters are disabled.

8.3.3 Mode Selection

The MODE/DATA pin allows mode selection between forced PWM mode and power-save mode for both converters. Furthermore, this pin is a multi-purpose pin and provides (besides mode selection) a one-pin interface to receive serial data from a host to set the output voltage. This is described in the section EasyScale™ interface.

Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converters operate in fixed-frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the MODE/DATA pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

In case the operation mode will be changed from forced PWM mode (MODE/DATA = High) to power-save mode Enable (MODE/DATA = 0) the power-save mode will be enabled after a delay time of typically $t_{timeout}$, which is a maximum of 520 µs.

The forced PWM mode operation is enabled immediately with pin MODE/DATA set to 1.

Feature Description (continued)

8.3.4 Enable

The device has for each converter a separate EN pin to start up each converter independently. If EN1 and EN2 are set to high, the corresponding converter starts up with soft-start.

Pulling EN1 and EN2 pin low forces the device into shutdown, with a shutdown quiescent current of typically 1.2 µA. In this mode, the P- and N-channel MOSFETs are turned-off and the entire internal control circuitry is switched off. For proper operation the EN1 and EN2 pins must be terminated and must not be left floating.

8.3.5 DEF_1 Pin Function

The DEF_1 pin is dedicated to converter 1 and makes the output voltage selection very flexible to support dynamic voltage management. Depending on the device version, this pin works either as:

1. Analog input for adjustable output voltage setting (TPS62420): Connecting an external resistor network to this pin adjusts the default output voltage to any value starting from 0.6 V to V_{IN}.

2. Digital input for fixed default output voltage selection (TPS62421): In case this pin is tied to low level, the output voltage is set according to the value in register REG_DEF_1_Low. The default voltage will be 1.2 V. If tied to high level, the output voltage is set according to the value in register REG_DEF_1_High. The default value in this case is 1.8 V. Depending on the level of pin DEF_1, it selects between the two registers REG_DEF_1_Low and REG_DEF_1_High for output voltage setting. Each register content (and therefore output voltage) can be changed individually through the EasyScale™ interface. This makes the device very flexible in terms of output voltage setting; see Table 4.

8.3.6 180° Out-of-Phase Operation

In PWM mode the converters operate with a 180° turnon phase shift of the PMOS (high side) transistors. It prevents the high-side switches of both converters to be turned on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

8.3.7 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 150°C the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again.

8.3.8 Short Circuit Protection

Both outputs are short circuit protected with maximum output current = I_{LIMF} (P-MOS and N-MOS). Once the PMOS switch reaches its current limit, it will be turned off and the NMOS turned on. The PMOS only turns on again, once the current in the NMOS decreases below the NMOS current limit.

8.4 Device Functional Modes

8.4.1 Soft-Start

The two converters have an internal soft-start circuit that limits the inrush current during start-up. During soft-start, the output voltage ramp up is controlled as shown in Figure 7.

Device Functional Modes (continued)

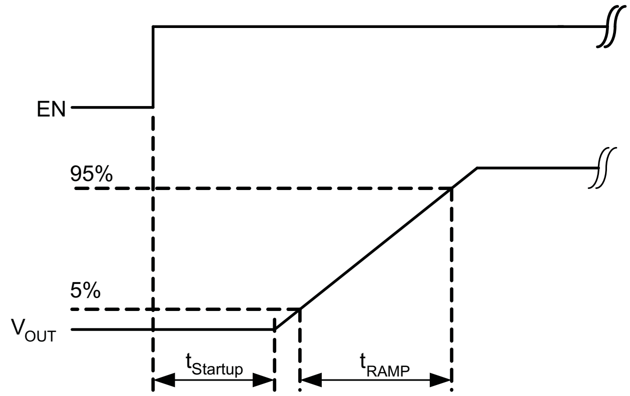


Figure 7. Soft-Start

8.4.2 100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range; that is, the minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(RDSon_{max} + R_L\right)$$

where

- $Iout_{max}$ = maximum output current plus inductor ripple current
- $RDSon_{max}$ = maximum P-channel switch RDSon
- R_L = DC resistance of the inductor
- $Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance (1)

With decreasing load current, the device automatically switches into pulse-skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically the switching losses are minimized and the device runs with a minimum quiescent current maintaining high efficiency.

8.4.3 Power-Save Mode

The power-save mode is enabled with MODE/DATA pin set to 0 for both converters. If the load current of a converter decreases, this converter will enter power-save mode operation automatically. The transition to power-save mode of a converter is independent from the operating condition of the other converter. During power-save mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage in PFM mode to typically 1.01 × V_{OUT}. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load the average inductor current is monitored. The device changes from PWM mode to power-save mode, if in PWM mode the inductor current falls below a certain threshold. The typical output current threshold depends on V_{IN} and can be calculated according to Equation 2 for each converter.

Equation 2: Average output current threshold to enter PFM mode

$$I_{OUT\_PFM\_enter} = \frac{VIN_{DCDC}}{32\ \Omega} \quad (2)$$

Equation 3: Average output current threshold to leave PFM mode

$$I_{OUT\_PFM\_leave} = \frac{VIN_{DCDC}}{24\ \Omega} \quad (3)$$

Device Functional Modes (continued)

To keep the output voltage ripple in power-save mode low, the output voltage is monitored with a single threshold comparator (skip comparator). As the output voltage falls below the skip comparator threshold (skip comp) of 1.01 × $V_{OUTnominal}$, the corresponding converter starts switching for a minimum time period of typically 1 µs and provides current to the load and the output capacitor. Therefore the output voltage increases and the device maintains switching until the output voltage trips the skip comparator threshold (skip comp) again. At this moment all switching activity is stopped and the quiescent current is reduced to minimum. The load is supplied by the output capacitor until the output voltage has dropped below the threshold again. Hereupon the device starts switching again. The power-save mode is exited and PWM mode entered in case the output current exceeds the current IOUT_PFM_leave, or if the output voltage falls below a second comparator threshold, called skip comparator low (skip comp Low) threshold. This skip comparator low threshold is set to –2% below nominal V_{out}, and enables a fast transition from power-save mode to PWM mode during a load step. In power-save mode the quiescent current is reduced typically to 19 µA for one converter and 32 µA for both converters active. This single skip comparator threshold method in power-save mode results in a very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing output capacitor values minimizes the output ripple. The power-save mode can be disabled through the MODE/DATA pin set to high. Both converters then operate in fixed PWM mode. Power-save mode enable/disable applies to both converters.

8.5 Programming

8.5.1 EasyScale™ Interface: One-Pin Serial Interface for Dynamic Output Voltage Adjustment

8.5.1.1 General

The EasyScale™ interface is a simple but very flexible one-pin interface to configure the output voltage of both DC–DC converters. The interface is based on a master-slave structure, where the master is typically a micro-controller or application processor. Figure 8 and Table 1 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 4E hex. The data byte consists of five bit for information, two address bits and the RFA bit. RFA bit set to high indicates the **R**equest **F**or **A**cknowledge condition, but the acknowledge condition is only applied if the protocol was received correctly.

The advantage of EasyScale™ interface compared to other one-pin interfaces is that its bit detection is, to a large extent, independent from the bit transmission rate. It can automatically detect bit rates from 1.7 kbps to 160 kbps. Furthermore, the interface is shared with the MODE/DATA pin and requires therefore no additional pin.

8.5.1.2 Protocol

All bits are transmitted MSB first and LSB last. Figure 9 shows the protocol without acknowledge request (bit RFA = 0), Figure 10 with acknowledge (bit RFA = 1) request.

Prior to both bytes, device address byte and data byte, a start condition needs to be applied. For this, the MODE/DATA pin needs to be pulled high for at least t_{Start} before the bit transmission starts with the falling edge. In case the MODE/DATA line was already at high level (forced PWM mode selection) no start condition need be applied prior the device address byte.

The transmission of each byte needs to be closed with an end-of-stream condition for at least T_{EOS}.

8.5.1.3 Bit Decoding

The bit detection is based on a PWM scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High Bit: $t_{High} > t_{Low}$, but with t_{High} at least 2 x t_{Low}, see Figure 11

Low Bit: $t_{Low} > t_{High}$, but with t_{Low} at least 2 x t_{High}, see Figure 11

The bit detection starts with a falling edge on the MODE/DATA pin and ends with the next falling edge. Depending on the relation between t_{Low} and t_{High} a 0 or 1 is detected.

Programming (continued)

8.5.1.4 Acknowledge

The acknowledge condition is only applied if:

- acknowledge is requested by a set RFA bit
- the transmitted device address matches with the device address of the device
- 16 bits were received correctly

In this case, the device turns on the internal ACKN-MOSFET and pulls the MODE/DATA pin low for the time t_{ACKN}, which is maximum. 520 µs. The acknowledge condition is valid after an internal delay time t_{valACK}. This means the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low during this time.

The master device can detect the acknowledge condition with its input by releasing the MODE/DATA pin after t_{valACK} and read back a 0.

In case of an invalid device address or not correctly received protocol, no acknowledge condition will be applied, thus the internal MOSFET will not be turned on and the external pullup resistor pulls MODE/DATA pin high after t_{valACK}. The MODE/DATA pin can be used again after the acknowledge condition ends.

NOTE

The acknowledge condition may only be requested in case the master device has an open-drain output.

In case of a push-pull output stage TI recommends to use a series resistor in the MODE/DATA line to limit the current to 500 µA in case of an accidentally requested acknowledge to protect the internal ACKN-MOSFET.

8.5.1.5 MODE Selection

Because of the MODE/DATA pin is used for two functions, interface and a mode selection, the device needs to determine when it has to decode the bit stream or to change the operation mode.

The device enters forced PWM mode operation immediately whenever the MODE/DATA pin turns to high level. The device stays also in forced PWM mode during the whole time of a protocol reception.

With a falling edge on the MODE/DATA pin the device starts bit decoding. If the MODE/DATA pin stays low for at least $t_{timeout}$, the device gets an internal time-out and power-save mode operation is enabled.

A protocol which is sent within this time will be ignored, because the falling edge for the mode change will be first interpreted as start of the first bit. In this case, TI recommends to send first the protocol and change at the end of the protocol to power-save mode.

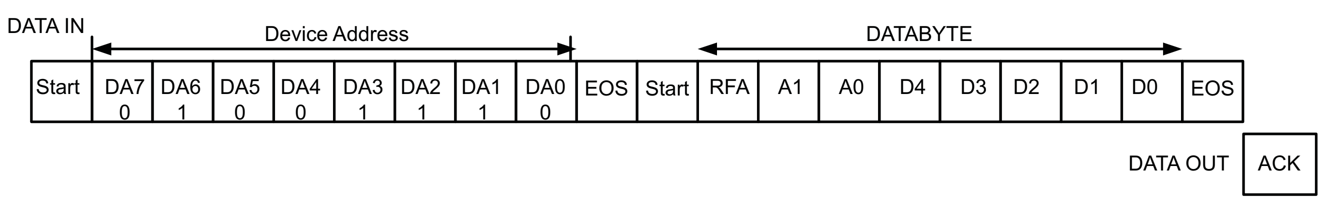


Figure 8. EasyScale™ Interface Protocol Overview

Table 1. EasyScale™ Interface Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte	7	DA7	IN	0 MSB device address
	6	DA6	IN	1
	5	DA5	IN	0
	4	DA4	IN	0

Programming (continued)

Table 1. EasyScale™ Interface Bit Description (continued)

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
4Ehex	3	DA3	IN	1
	2	DA2	IN	1
	1	DA1	IN	1
	0	DA0	IN	0 LSB device address
Data Byte	7 (MSB)	RFA	IN	Request for acknowledge, if high, acknowledge condition will applied by the device
	6	A1		Address bit 1
	5	A0		Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open-drain output, line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open-drain output stage. In case of a push-pull output stage acknowledge condition may not be requested!

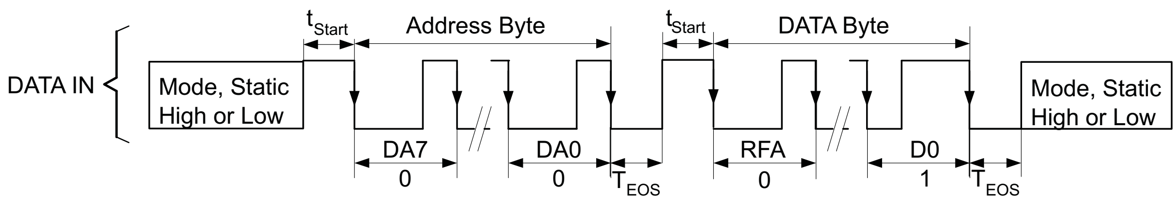


Figure 9. EasyScale™ Interface Protocol Without Acknowledge

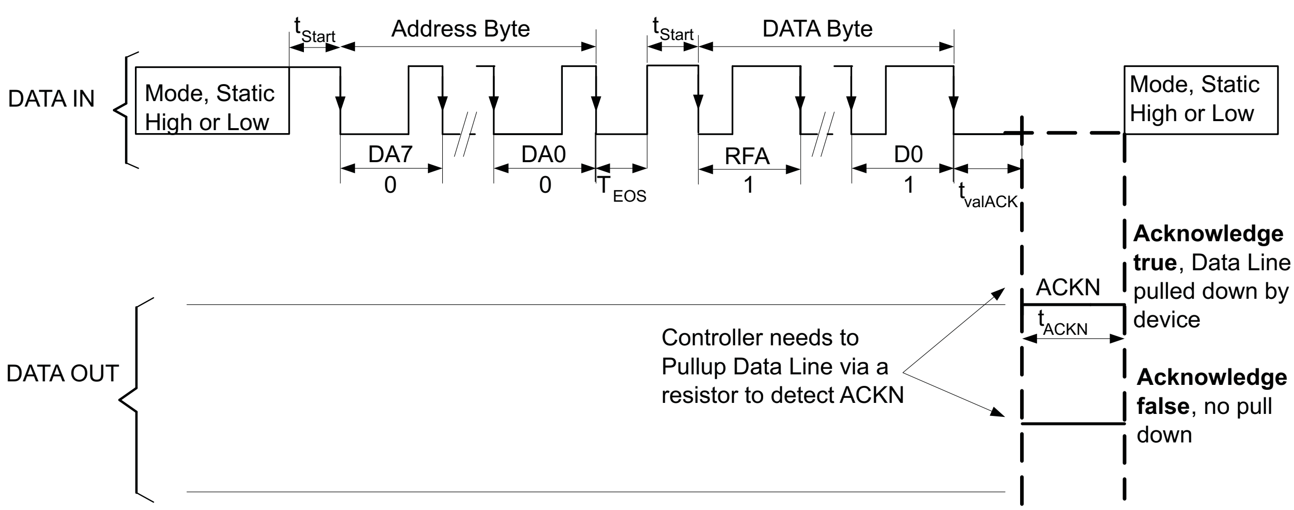


Figure 10. EasyScale™ Interface Protocol Including Acknowledge

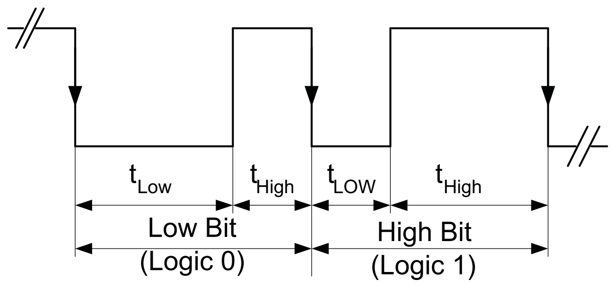


Figure 11. EasyScale™ Interface – Bit Coding

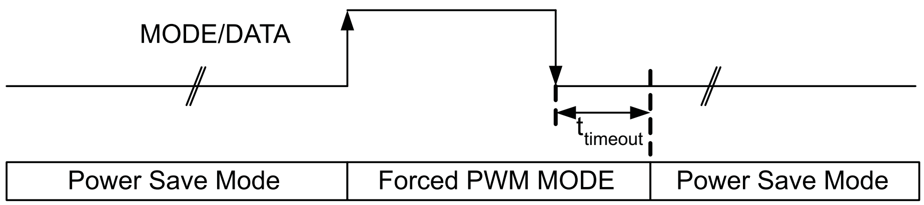


Figure 12. MODE/DATA Pin: Mode Selection

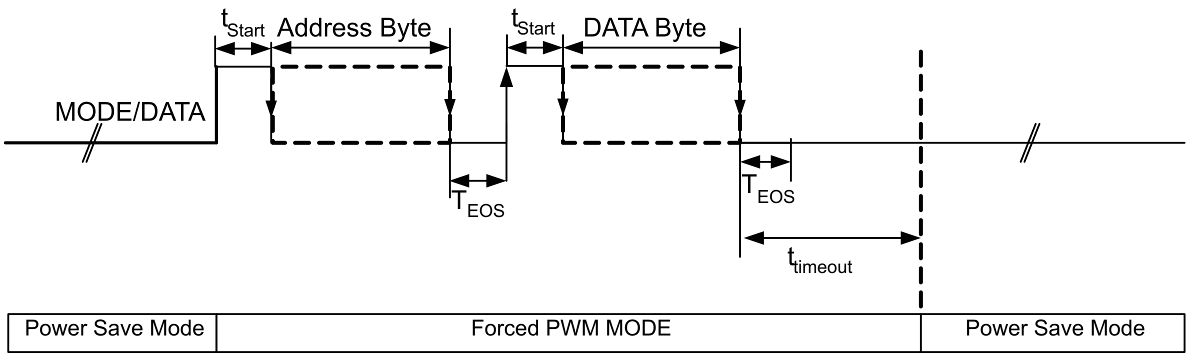


Figure 13. MODE/DATA Pin: Power-Save Mode/Interface Communication

8.6 Register Maps

Three registers with a data content of 5 bits can be addressed. With 5 bit data content, 32 different values for each register are available. Table 2 shows the addressable registers to set the output voltage when DEF_1 pin works as digital input. In this case, converter 1 has a related register for each DEF_1 pin condition, and one register for converter 2. With a high or low condition on pin DEF_1 (TPS62421) either the content of register REG_DEF_1_High/REG_DEF1_Low is selected. The output voltage of converter 1 is set according to the values in Table 4. Table 3 shows the addressable registers if DEF_1 pin acts as analog input with external resistors connected. In this case one register is available for each converter. The output voltage of converter 1 is set according to the values in Table 5. For converter 2, the available voltages are shown in Table 6. To generate these output voltages a precise internal resistor divider network is used, making external resistors unnecessary (less board space), and provides higher output voltage accuracy. The Interface is activated if at least one of the converters is enabled (EN1 or EN2 is high). After the start-up time t_{Start} (170 µs) the interface is ready for data reception.

Table 2. Addressable Registers for Fixed Output Voltage Options (Pin DEF_1 = digital input)

DEVICE	REGISTER	DESCRIPTION	DEF_1 PIN	A1	A0	D4	D3	D2	D1	D0
TPS62421	REG_DEF_1_High	Converter 1 output voltage setting for DEF_1 = High condition. The content of the register is active with DEF1_ Pin high.	high	0	1	Output voltage setting, see Table 4				
	REG_DEF_1_Low	Converter 1 output voltage setting	low	0	0	Output voltage setting, see Table 4				
	REG_DEF_2	Converter 2 output voltage	n/a	1	0	Output voltage setting, see Table 6				
		Do not use		1	1					

Table 3. Addressable Registers for Adjustable Output Voltage Devices

REGISTER	DESCRIPTION	A1	A0	D4	D3	D2	D1	D0
REG_DEF_1_High	Not available in TPS62420 adjustable version	0	1					
REG_DEF_1_Low	Converter 1 output voltage setting	0	0	TPS62420 see Table 5				
REG_DEF_2	Converter 2 output voltage	1	0	TPS62420 see Table 6, connect ADJ2 pin directly to V_{OUT2}				
	Do not use	1	1					

Table 4. Selectable Output Voltages for Converter 1, With Pin DEF_1 as Digital Input (TPS62421)

	VOLTAGE [V] REGISTER REG_DEF_1_LOW	VOLTAGE [V] REGISTER REG_DEF_1_HIGH	D4	D3	D2	D1	D0
0	0.8	0.9	0	0	0	0	0
1	0.825	0.925	0	0	0	0	1
2	0.85	0.95	0	0	0	1	0
3	0.875	0.975	0	0	0	1	1
4	0.9	1.0	0	0	1	0	0
5	0.925	1.025	0	0	1	0	1
6	0.95	1.050	0	0	1	1	0
7	0.975	1.075	0	0	1	1	1
8	1.0	1.1	**0**	**1**	**0**	**0**	**0**
9	1.025	1.125	0	1	0	0	1
10	1.050	1.150	0	1	0	1	0
11	1.075	1.175	0	1	0	1	1
12	1.1	1.2	0	1	1	0	0
13	1.125	1.225	0	1	1	0	1
14	1.150	1.25	0	1	1	1	0
15	1.175	1.275	0	1	1	1	1
16	**1.2 (default TPS62421)**	1.3	**1**	**0**	**0**	**0**	**0**
17	1.225	1.325	1	0	0	0	1
18	1.25	1.350	1	0	0	1	0
19	1.275	1.375	1	0	0	1	1
20	1.3	1.4	1	0	1	0	0
21	1.325	1.425	1	0	1	0	1
22	1.350	1.450	1	0	1	1	0
23	1.375	1.475	1	0	1	1	1
24	1.4	1.5	1	1	0	0	0
25	1.425	1.525	1	1	0	0	1
26	1.450	1.55	1	1	0	1	0
27	1.475	1.575	1	1	0	1	1
28	1.5	1.6	1	1	1	0	0
29	1.525	1.7	1	1	1	0	1
30	1.55	**1.8 (default TPS62421)**	**1**	**1**	**1**	**1**	**0**
31	1.575	1.9	1	1	1	1	1

Table 5. Selectable Output Voltages for Converter 1, With DEF1 Pin as Analog Input (TPS62420)

	TPS62420 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	D4	D3	D2	D1	D0
0	**V_{OUT1} Adjustable Output with Resistor Network on DEF_1 Pin** **0.6 V with DEF_1 pin connected to V_{OUT1}**	**0**	**0**	**0**	**0**	**0**
1	0.825	0	0	0	0	1
2	0.85	0	0	0	1	0
3	0.875	0	0	0	1	1
4	0.9	0	0	1	0	0
5	0.925	0	0	1	0	1
6	0.95	0	0	1	1	0
7	0.975	0	0	1	1	1
8	1.0	0	1	0	0	0
9	1.025	0	1	0	0	1
10	1.050	0	1	0	1	0
11	1.075	0	1	0	1	1
12	1.1	0	1	1	0	0
13	1.125	0	1	1	0	1
14	1.150	0	1	1	1	0
15	1.175	0	1	1	1	1
16	1.2	1	0	0	0	0
17	1.225	1	0	0	0	1
18	1.25	1	0	0	1	0
19	1.275	1	0	0	1	1
20	1.3	1	0	1	0	0
21	1.325	1	0	1	0	1
22	1.350	1	0	1	1	0
23	1.375	1	0	1	1	1
24	1.4	1	1	0	0	0
25	1.425	1	1	0	0	1
26	1.450	1	1	0	1	0
27	1.475	1	1	0	1	1
28	1.5	1	1	1	0	0
29	1.525	1	1	1	0	1
30	1.55	1	1	1	1	0
31	1.575	1	1	1	1	1

Table 6. Selectable Output Voltages for Converter 2, (ADJ2 Connected to V_{OUT})

	OUTPUT VOLTAGE [V] FOR REGISTER REG_DEF_2	D4	D3	D2	D1	D0
0	**V_{OUT2} Adjustable Output with Resistor Network on ADJ2 (TPS62420)**	**0**	**0**	**0**	**0**	**0**
	0.6 V with ADJ2 pin connected to V_{OUT2} (TPS62420)					
1	0.85	0	0	0	0	1
2	0.9	0	0	0	1	0
3	0.95	0	0	0	1	1
4	1.0	0	0	1	0	0
5	1.05	0	0	1	0	1
6	1.1	0	0	1	1	0
7	1.15	0	0	1	1	1
8	1.2	0	1	0	0	0
9	1.25	0	1	0	0	1
10	1.3	0	1	0	1	0
11	1.35	0	1	0	1	1
12	1.4	0	1	1	0	0
13	1.45	0	1	1	0	1
14	1.5	0	1	1	1	0
15	1.55	0	1	1	1	1
16	1.6	1	0	0	0	0
17	1.7	1	0	0	0	1
18	**1.8 (default TPS62421)**	**1**	**0**	**0**	**1**	**0**
19	1.85	1	0	0	1	1
20	2.0	1	0	1	0	0
21	2.1	1	0	1	0	1
22	2.2	1	0	1	1	0
23	2.3	1	0	1	1	1
24	2.4	1	1	0	0	0
25	2.5	1	1	0	0	1
26	2.6	1	1	0	1	0
27	2.7	1	1	0	1	1
28	2.8	1	1	1	0	0
29	2.85	1	1	1	0	1
30	3.0	1	1	1	1	0
31	3.3	1	1	1	1	1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Output Voltage Setting

9.1.1.1 Converter 1 Adjustable Default Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{11}}{R_{12}}\right) \text{ with an internal reference voltage } V_{REF} \text{ typical 0.6V} \quad (4)$$

To keep the operating current to a minimum, TI recommends selecting R_{12} within a range of 180 kΩ to 360 kΩ. The sum of R_{12} and R_{11} should not exceed ~1 MΩ. For higher output voltages than 3.3 V, TI recommends choosing lower values than 180 kΩ for R12. Route the DEF_1 line away from noise sources, such as the inductor or the SW1 line. The FB1 line needs to be directly connected to the output capacitor. An internal feed-forward capacitor is connected to this pin, therefore there is no need for an external feed-forward capacitor for converter 1.

9.1.1.2 Converter 2

The default output voltage of converter 2 can be set by an external resistor network. For converter 2 the same recommendations apply as for converter 1. In addition to that, a 33-pF external feed-forward capacitor C_{ff2} for good load transient response must be used.

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{21}}{R_{22}}\right) \text{ with an internal reference voltage } V_{REF} \text{ typical 0.6V} \quad (5)$$

Route the ADJ2 line away from noise sources, such as the inductor or the SW2 line. In case the interface is used for converter 2, connect ADJ2 pin directly to V_{OUT2}

9.2 Typical Applications

9.2.1 Typical Application Circuit 1.5-V and 2.85-V Adjustable Outputs

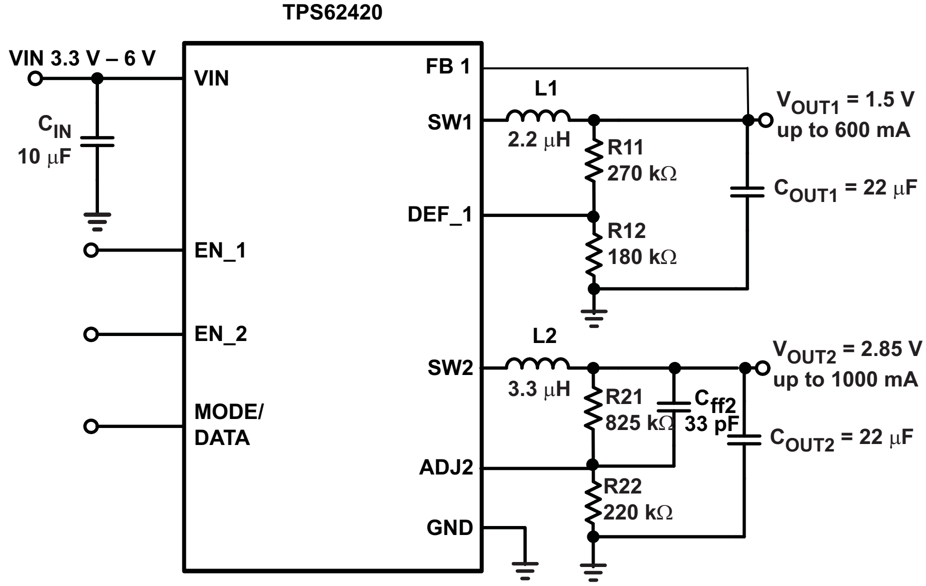


Figure 14. Typical Application Circuit 1.5-V and 2.85-V Adjustable Outputs

9.2.1.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole V_{IN}, V_{OUT} and load current range of TPS62420.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Output Filter Design (Inductor and Output Capacitor)

The device is optimized to operate with inductors of 2.2 µH to 4.7 µH and output capacitors of 10 µF to 22 µF.

For operation with a 2.2-µH inductor, a 22-µF capacitor is suggested.

9.2.1.2.1.1 Inductor Selection

The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 7. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (6)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (7)

Typical Applications (continued)

The highest inductor current will occur at maximum V_{IN}.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Refer to Table 7 and the typical applications for possible inductors.

Table 7. List of Inductors

DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
3.2 × 2.6 × 1.0	MIPW3226	FDK
3 × 3 × 0.9	LPS3010	Coilcraft
2.8 × 2.6 × 1.0	VLF3010	TDK
2.8 x 2.6 × 1.4	VLF3014	TDK
3 × 3 × 1.4	LPS3015	Coilcraft
3.9 × 3.9 × 1.7	LPS4018	Coilcraft

9.2.1.2.1.2 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the two converters allows the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage undershoots and overshoots during heavy load transients. Ceramic X7R/X5R capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. The RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \quad (9)$$

Where the highest output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents the converters operate in power-save mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. Higher output capacitors like 22-µF values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

9.2.1.2.1.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering.

9.2.1.3 Application Curves

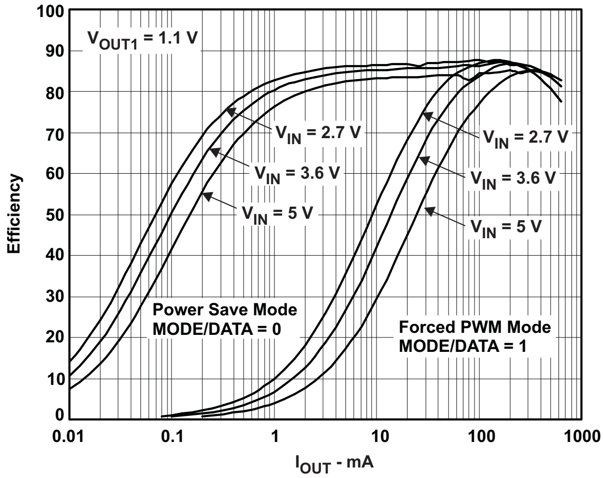


Figure 15. Efficiency V_{OUT1} = 1.1 V

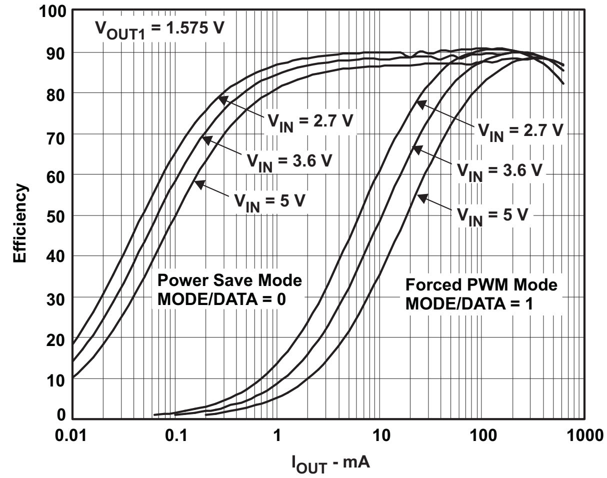


Figure 16. Efficiency V_{OUT1} = 1.575 V

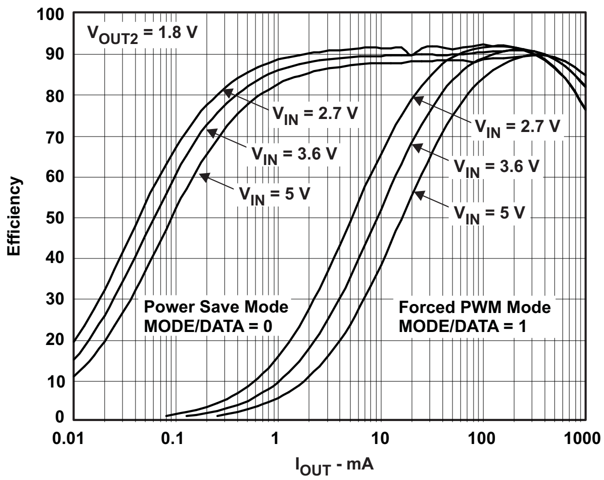


Figure 17. Efficiency V_{OUT2} = 1.8 V

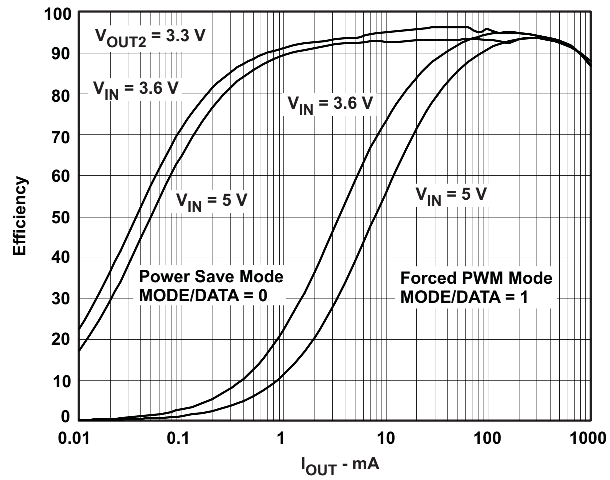


Figure 18. Efficiency V_{OUT2} = 3.3 V

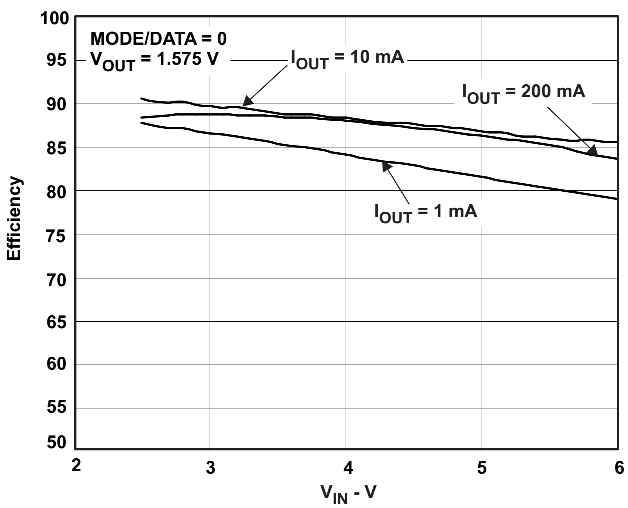


Figure 19. Efficiency vs V_{IN} , V_{OUT1} = 1.575 V

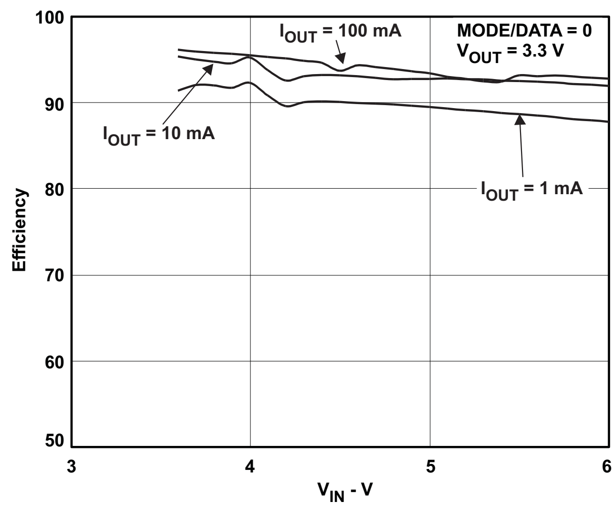


Figure 20. Efficiency vs V_{IN}, V_{OUT2} = 3.3 V

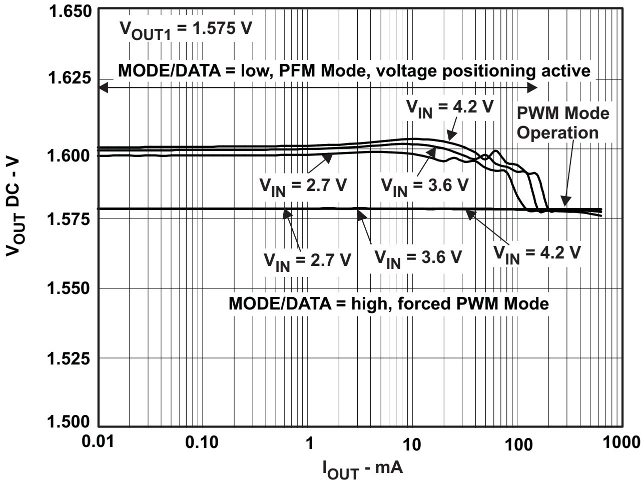


Figure 21. DC Output Accuracy V_{OUT1} = 1.575 V

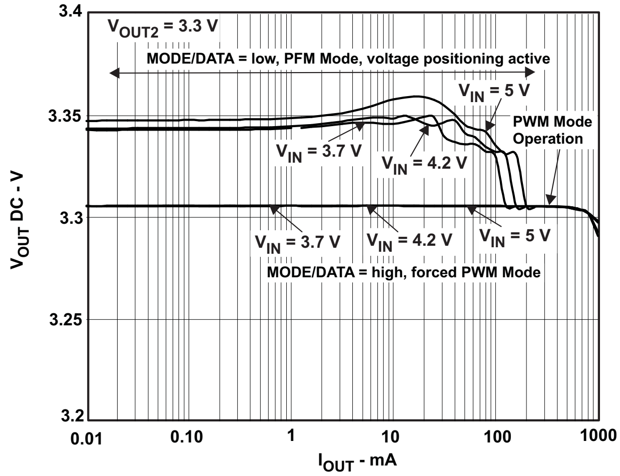


Figure 22. DC Output Accuracy V_{OUT2} = 3.3 V

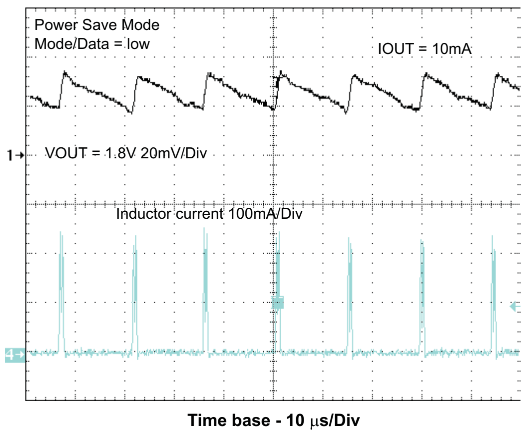


Figure 23. Light Load Output Voltage Ripple in Power-Save Mode

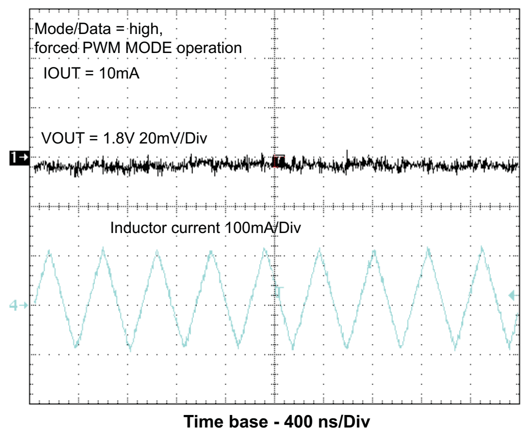


Figure 24. Output Voltage Ripple in Forced PWM Mode

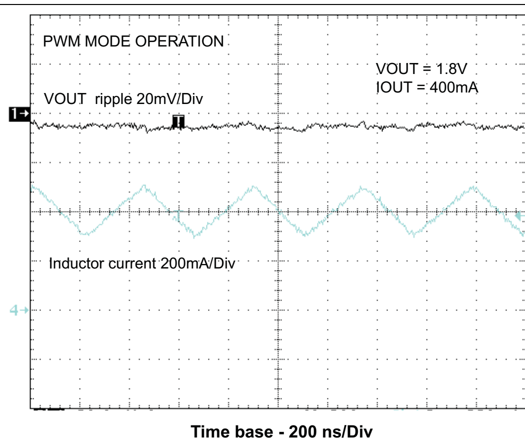


Figure 25. Output Voltage Ripple in PWM Mode

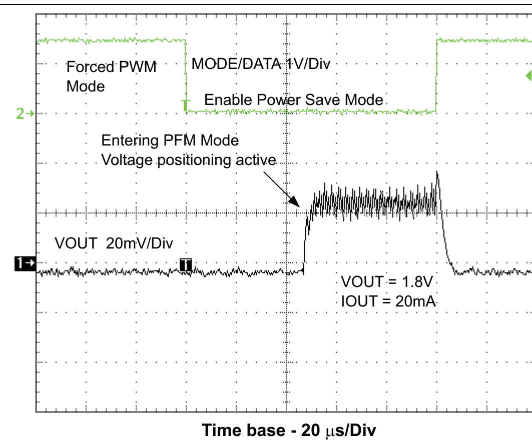
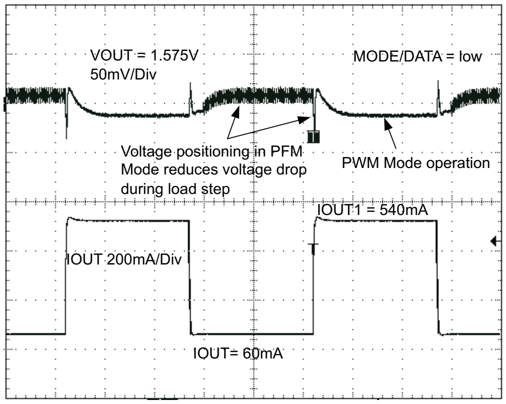
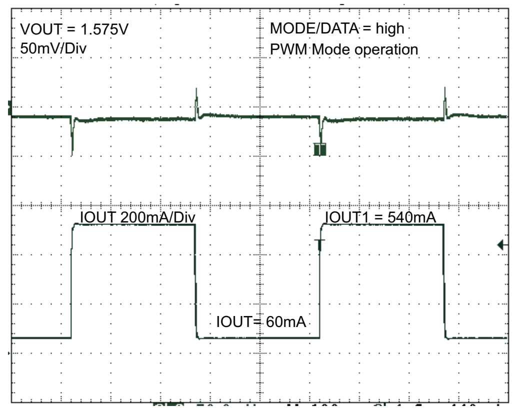


Figure 26. Forced PWM/PFM Mode Transition



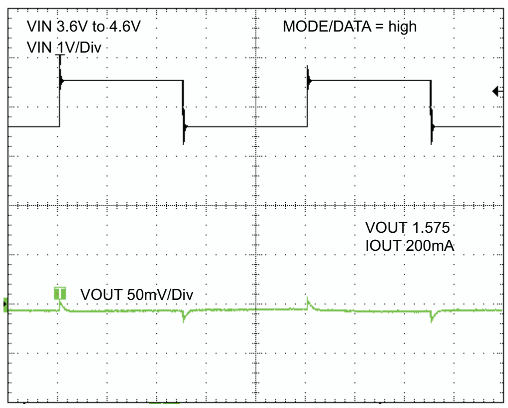
Time base - 100 µs/Div

Figure 27. Load Transient Response PFM/PWM



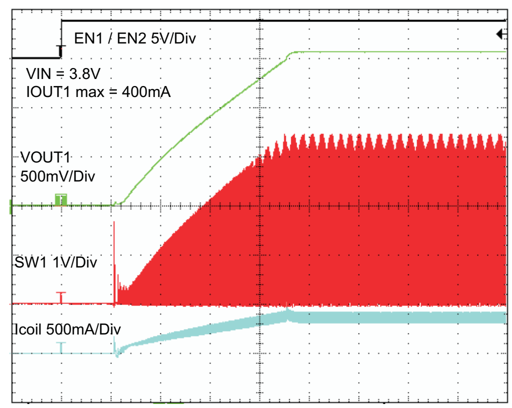
Time base - 100 µs/Div

Figure 28. Load Transient Response PWM Operation



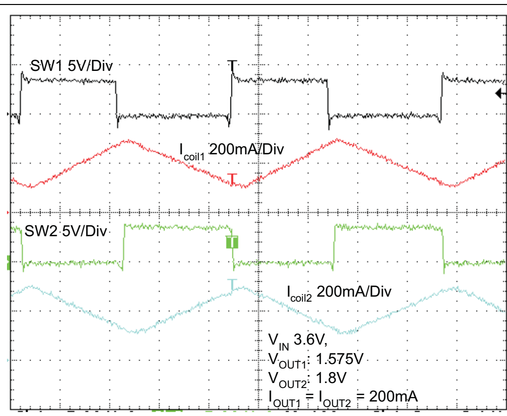
Time base - 400 µs/Div

Figure 29. Line Transient Response



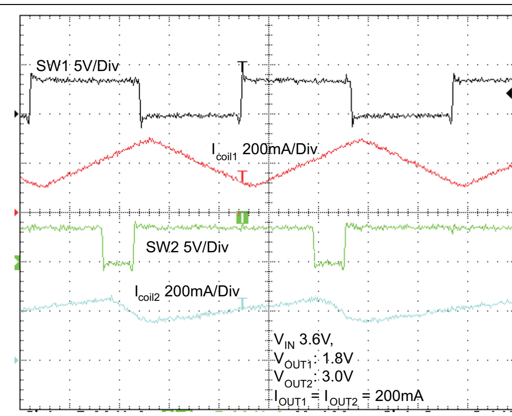
Time base - 200 µs/Div

Figure 30. Start-Up Timing One Converter



Time base - 100 ns/Div

Figure 31. Typical Operation V_{IN} = 3.6 V, V_{OUT1} = 1.575 V, V_{OUT2} = 1.8 V



Time base - 100 ns/Div

Figure 32. Typical Operation V_{IN} = 3.6 V, V_{OUT1} = 1.8 V, V_{OUT2} = 3 V

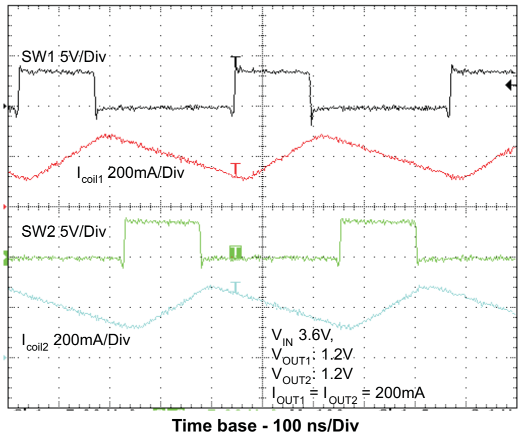


Figure 33. Typical Operation V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, V_{OUT2} = 1.2 V

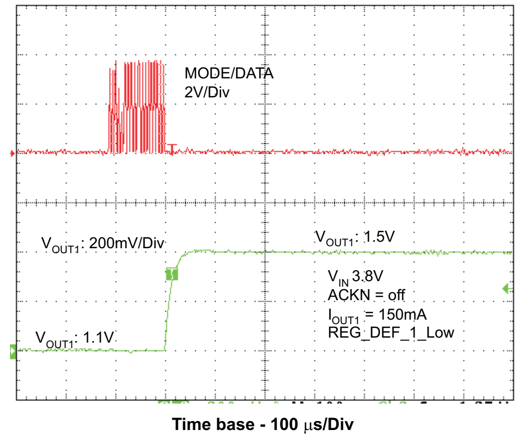


Figure 34. V_{OUT1} Change With EasyScale™ Interface

9.2.2 Typical Application Circuit TPS62421

In fixed output voltage version TPS62421, the default output voltage of converter 1 is fixed to 1.2 V or 1.8 V depending on the DEF_1 pin level. The default output voltage of converter 2 is fixed to 1.8 V. The ADJ2 pin must be connected directly to the converter 2 output voltage.

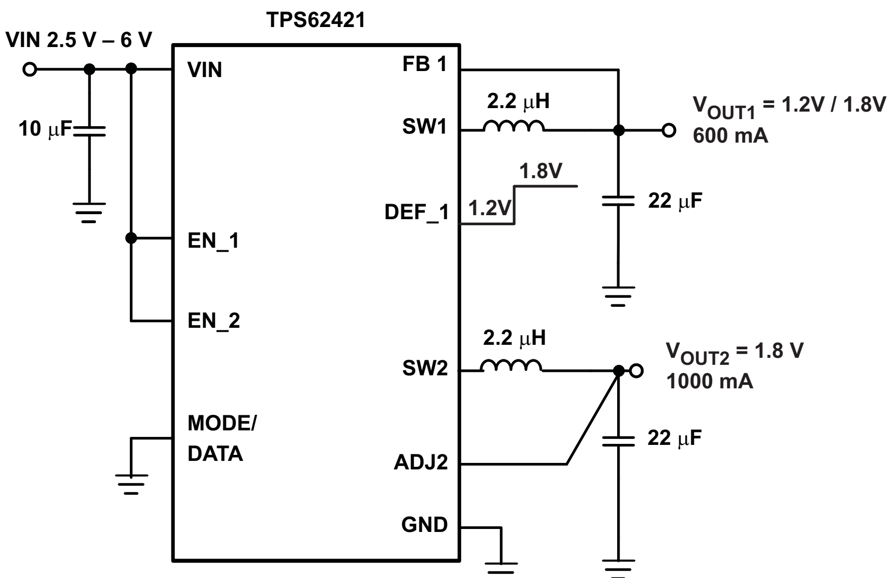


Figure 35. Typical Application Circuit TPS62421

10 Power Supply Recommendations

The TPS6242x device has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6242x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold in Figure 36.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the PowerPAD of the PCB and use this pad as a star point. For each converter use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The output voltage sense lines (FB1, ADJ2, DEF_1) should be connected right to the output capacitor and routed away from noisy components and traces (that is, SW line). If the EasyScale™ interface is operated with high transmission rates, the MODE/DATA trace must be routed away from the ADJ2 line to avoid capacitive coupling into the ADJ2 pin. A GND guard ring between the MODE/DATA pin and ADJ2 pin avoids potential noise coupling.

11.2 Layout Example

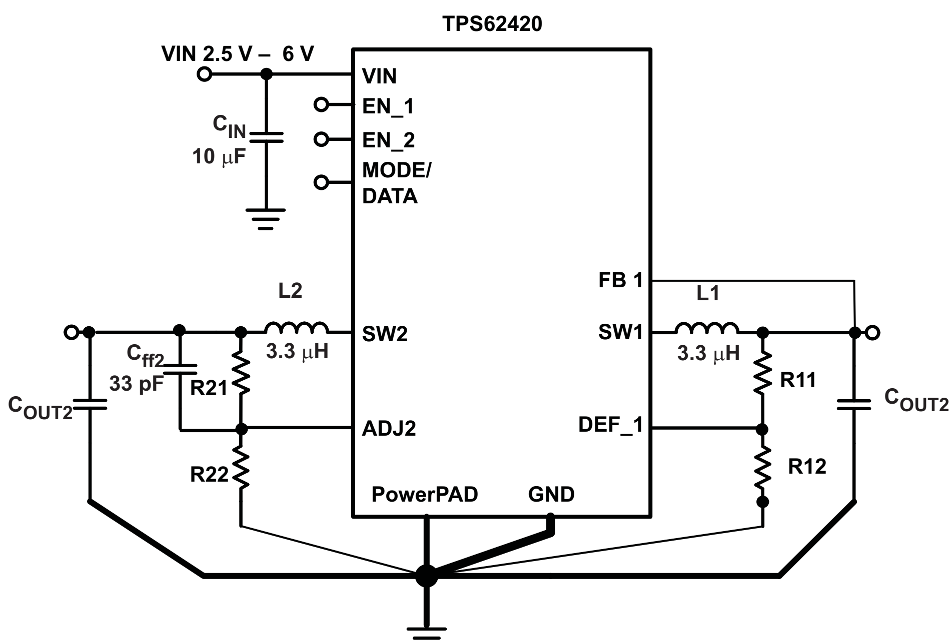


Figure 36. Layout Diagram

Layout Example (continued)

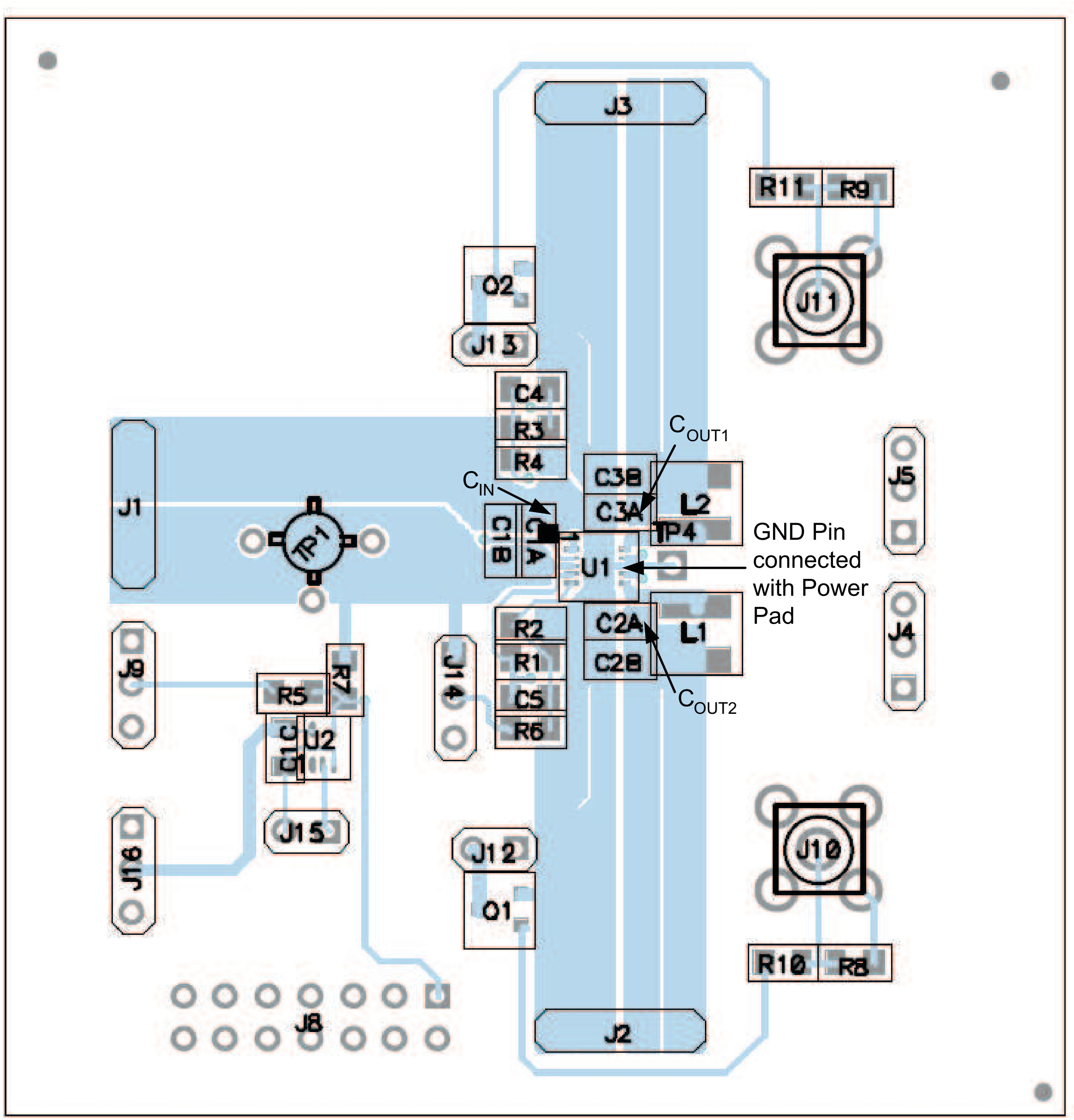


Figure 37. PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62420	Click here	Click here	Click here	Click here	Click here
TPS62421	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

EasyScale, OMAP, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62420DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQF	Samples
TPS62420DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQF	Samples
TPS62420DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQF	Samples
TPS62420DRCTG4	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQF	Samples
TPS62421DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTQ	Samples
TPS62421DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62420 :

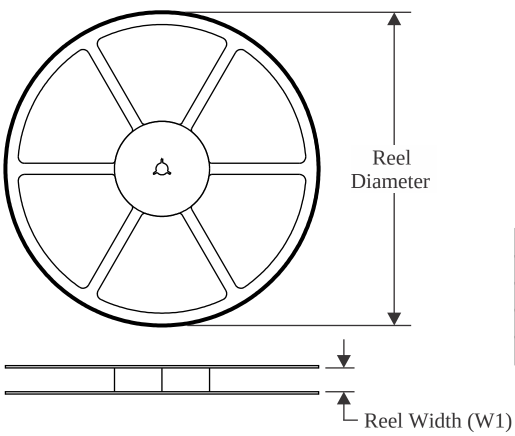
- Automotive: TPS62420-Q1

NOTE: Qualified Version Definitions:

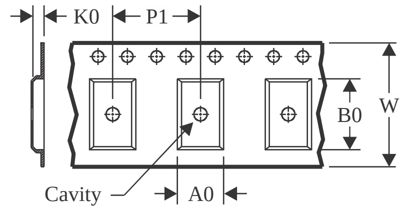
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

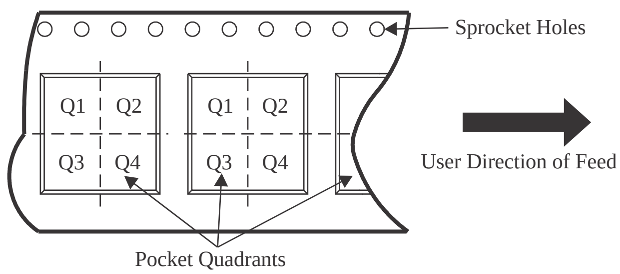


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

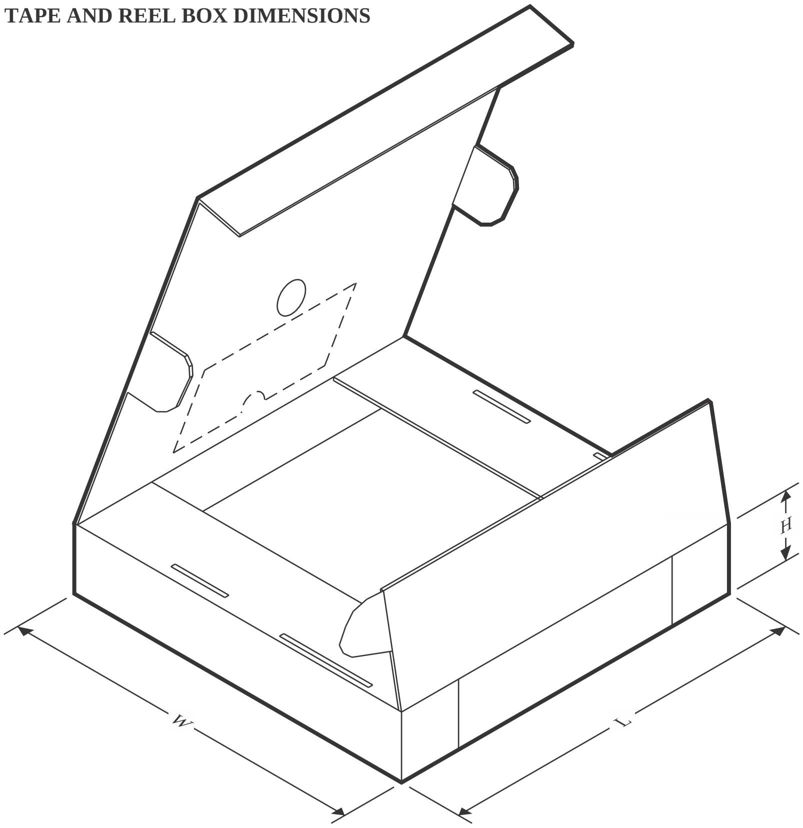
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62420DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62420DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62421DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62421DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62420DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS62420DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS62421DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TPS62421DRCT	VSON	DRC	10	250	210.0	185.0	35.0

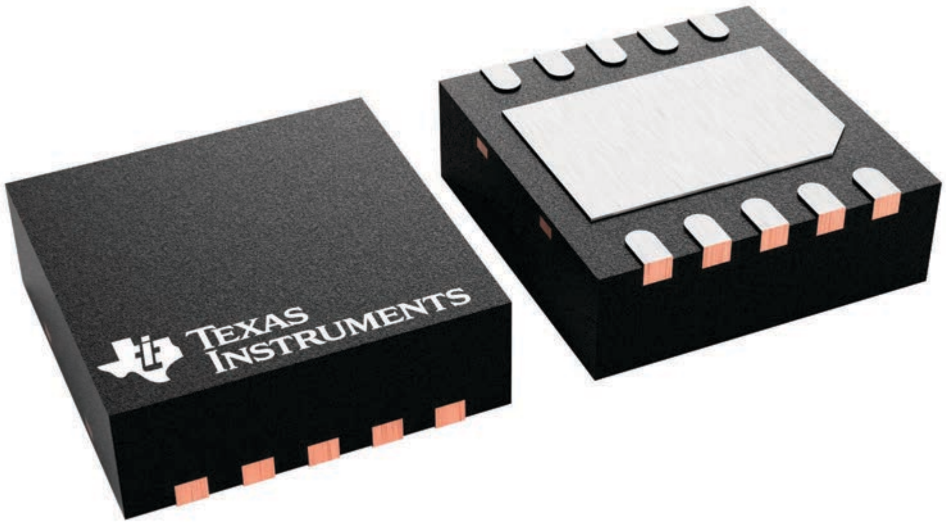
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

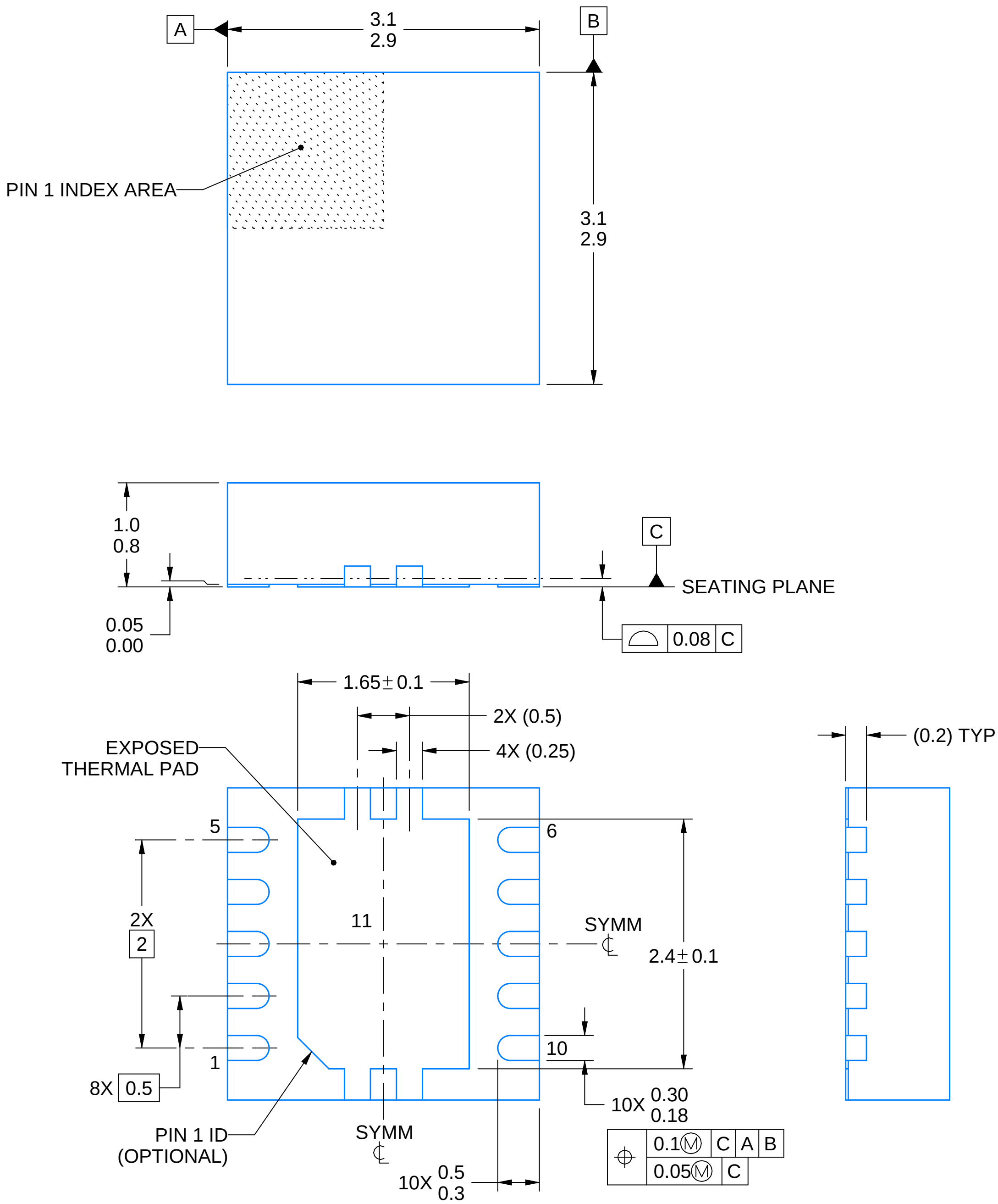
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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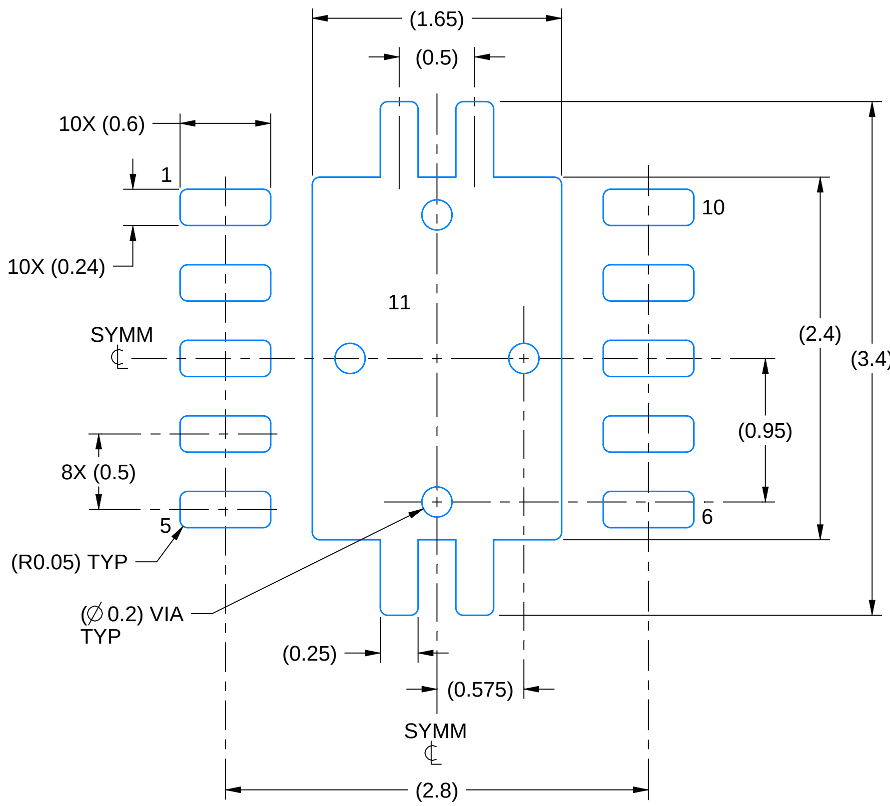
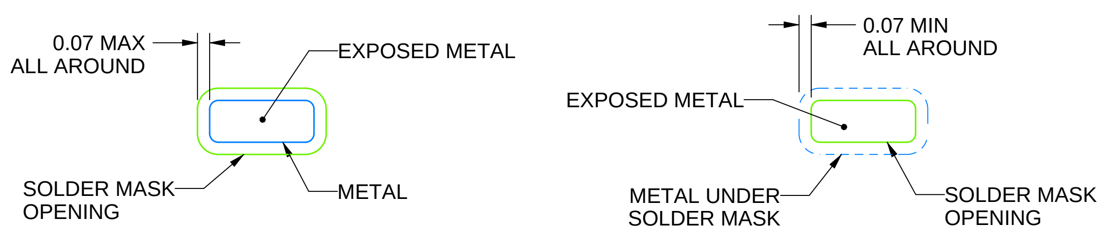
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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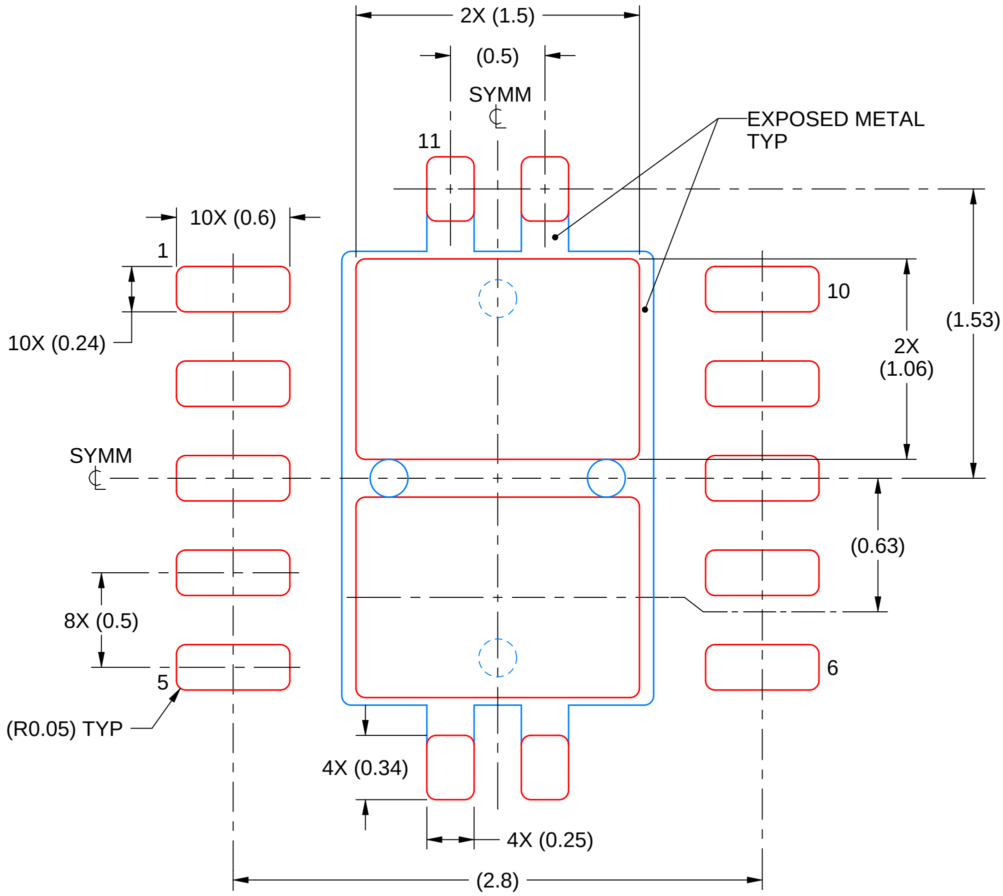
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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