ESD321 采用 0402 和 SOD-523 封装的低电容（小于 1pF）单通道 30kV ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级 ESD 保护：
  - ±30kV 接触放电
  - ±30kV 空气间隙放电
- IEC 61000-4-4 EFT 保护：
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护：
  - 6A (8μs/20μs)
- IO 电容：0.9pF（典型值）
- 直流击穿电压：4.5V（最小值）
- 低漏电流：0.1nA（典型值）
- 超低的 ESD 钳位电压：
  - 在 16A TLP 下为 6.8V（I/O 至 GND）
  - R_{DYN}：0.13Ω（I/O 至 GND）
- 工业温度范围：–40°C 至 +125°C
- 业界通用的 0402 (DFN1006P2) 和 SOD-523 封装

2 应用

- 终端设备：
  - 可穿戴设备
  - 工业和服务机器人
  - 便携式计算机和台式机
  - 手机和平板电脑
  - 机顶盒
  - DVR 和 NVR
  - 电视和监视器
  - EPOS（电子销售点）
- 接口：
  - USB 2.0/1.1
  - 通用输入/输出 (GPIO)
  - 以太网 10/100/1000Mbps
  - 按钮
  - 音频

3 说明

ESD321 是一款单向 TVS ESD 保护二极管，具有低动态电阻和低钳位电压。ESD321 的额定 ESD 冲击消散值高达 ±30kV，符合 IEC 61000-4-2 国际标准（高于 4 级）。

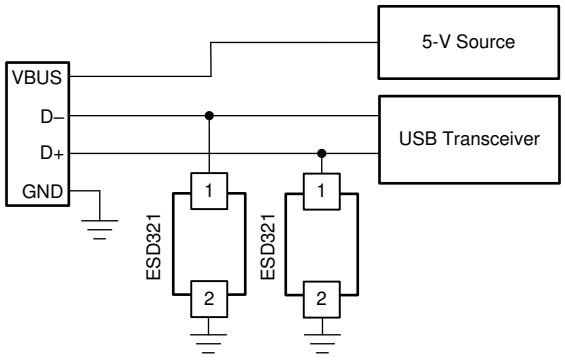
超低动态电阻 (0.13Ω) 和极低钳位电压（16A TLP 时为 6.8V）可针对瞬态事件提供系统级保护。该器件具有 0.9pF 的低 IO 电容，适合用于保护 USB 2.0 和以太网 10/100/1000Mbps 等接口。

ESD321 采用业界通用的 0402 (DPY/DFN1006P2) 和 SOD-523 (DYA) 封装。

封装信息

器件型号	封装(1)	封装尺寸(2)
ESD321	DPY（X1SON，2）	1mm × 0.6mm
	DYA（SOD-532，2）	1.6 mm × 0.8 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



USB 2.0 典型应用原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2022) to Revision B (October 2023)	Page
• 更新了*封装信息*表以包含封装尺寸	1
• Changed voltage to power in the *Surge Curve (IEC 61000-4-5, t_p=8/20 µs), I/O Pin to GND* figure	6

Changes from Revision * (July 2018) to Revision A (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 向数据表添加了 *DYA* 封装	1

5 Pin Configuration and Functions

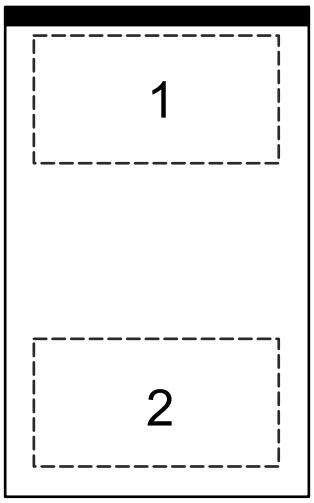


图 5-1. DPY Package, 2-Pin X1SON (Top View)

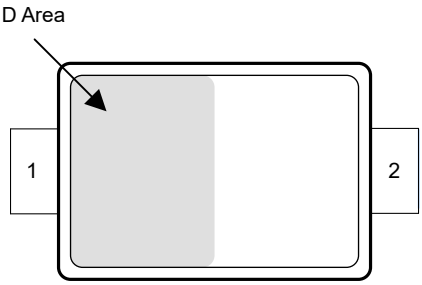


图 5-2. DYA Package, 2-Pin SOD-523 (Top View)

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DPY	DYA		
IO	1	2	I/O	ESD Protected Channel. Connect to the line being protected.
GND	2	1	GND	Connect to ground

(1) I = input, O = output, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25 °C		80	A
Surge Pulse	IEC 61000-4-5 Surge (tp 8/20 µs) Peak Power at 25 °C		40	W
	IEC 61000-4-5 Surge (tp 8/20 µs) Peak Current at 25 °C		6	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings – JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC (1)		ESD321		UNIT
		DYA (SOD-523)	DPY (X1SON)	
		2 Pins	2 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	774.7	437.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	462.3	249.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	541.1	169.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	164.4	99.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	534.6	168.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50 nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6 V	V_{IO} = 3.6 V, I/O to GND		0.1	10	nA
V_{BRF}	Breakdown voltage, I/O to GND (1)	I_{IO} = 1 mA	4.5		7.5	V
V_{FWD}	Forward Voltage, GND to I/O (1)	I_{IO} = 1 mA		0.8		V
V_{HOLD}	Holding voltage, I/O to GND (2)	I_{IO} = 1 mA		5.1		V
V_{CLAMP}	Clamping voltage	I_{PP} = 6 A (8/20 µs Surge), I/O to GND		6.3		V
		I_{PP} = 16 A (100 ns TLP), I/O to GND		6.8		V
		I_{PP} = 16 A (100 ns TLP), GND to I/O		4.7		V
R_{DYN}	Dynamic resistance	I/O to GND, 100 ns TLP, between 10 to 20 A I_{PP}		0.13		Ω
		GND to I/O , 100 ns TLP, between 10 to 20 A I_{PP}		0.2		Ω
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0 V, V_{p-p} = 30 mV, f = 1 MHz		0.9	1.1	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics

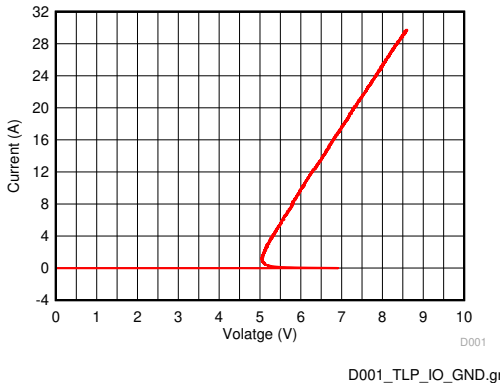


图 6-1. TLP I-V Curve, I/O Pin to GND (t_p = 100 ns)

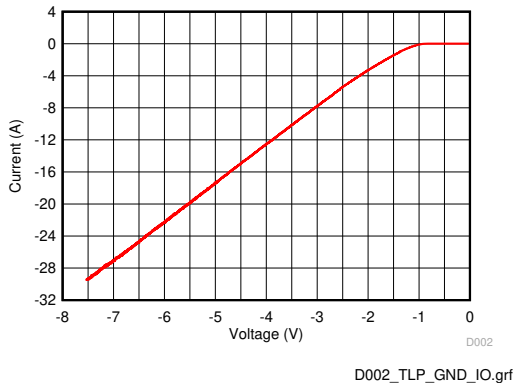


图 6-2. TLP I-V Curve, GND to I/O Pin (t_p = 100 ns)

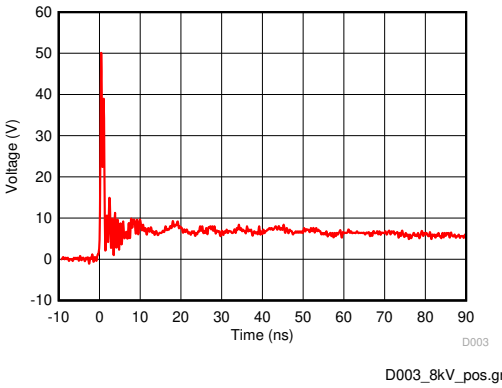


图 6-3. 8-kV IEC 61000-4-2 Clamping Voltage Waveform, I/O Pin to GND

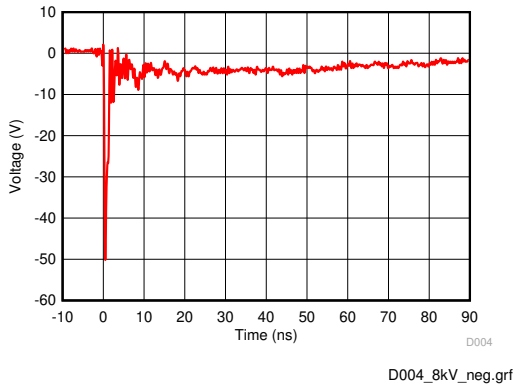


图 6-4. 8-kV IEC 61000-4-2 Clamping Voltage Waveform, GND to I/O Pin

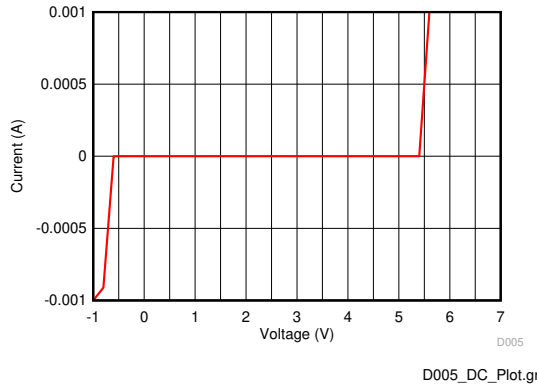


图 6-5. DC Voltage Sweep I-V Curve, I/O Pin to GND

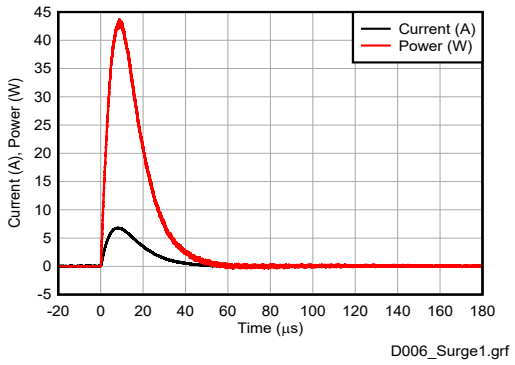


图 6-6. Surge Curve (IEC 61000-4-5, t_p=8/20 µs), I/O Pin to GND

6.7 Typical Characteristics (continued)

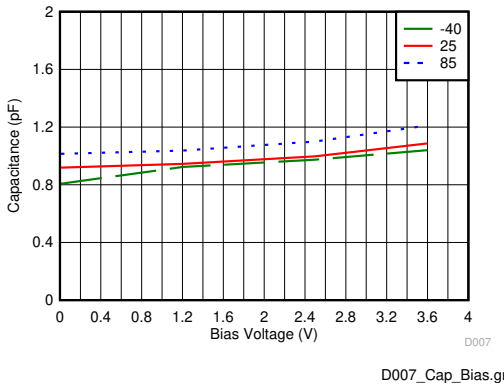


图 6-7. Capacitance vs. Bias Voltage For Different Temperatures (°C)

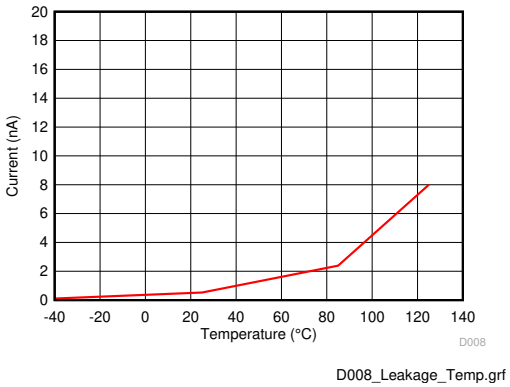


图 6-8. Leakage Current (at 3.6 V Bias) Across Temperature, I/O Pin to GND

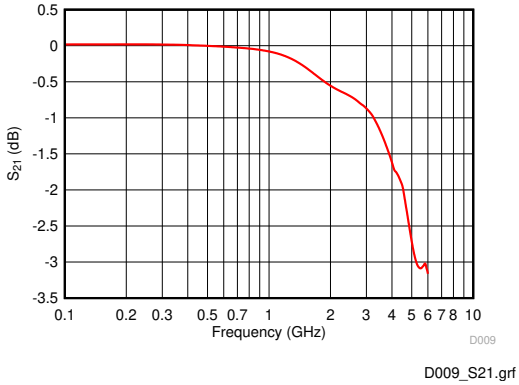


图 6-9. Insertion Loss vs. Frequency

7 Detailed Description

7.1 Overview

The ESD321 is a low capacitance uni-directional ESD Protection Diode with a low clamping voltage. This device can dissipate ESD strikes up to ±30 kV (Contact and Air) per the IEC 61000-4-2 Standard. The low clamping makes this device suitable for protecting any ESD sensitive devices.

7.2 Functional Block Diagram

7.3 Feature Description

ESD321 provides ESD protection up to ±30-kV contact and ±30-kV air gap per IEC 61000-4-2 standard. During an ESD event, ESD diode connected to the I/O pin turns on and diverts the current to ground. Additionally, ESD321 also provides protection against IEC 61000-4-5 Surge currents up to 6 A (8/20 µs waveform) and up to 80 A per IEC 61000-4-4 (5/50 ns waveform, 4 kV with 50-Ω impedance) electrical fast transient (EFT) standard. The capacitance between the I/O pin and ground is 0.9 pF (typical) and 1.1 pF (maximum). The device features a low leakage current of 0.1 nA (typical) and 50 nA (maximum, across operating temperature range) with a bias of 3.6 V. The ESD diode at the I/O pin protects the ESD-sensitive devices by clamping the voltage to a low value of 6.8 V (I_{PP} = 16 A 100 ns TLP). The layout of this device makes it simple and easy to add protection to an existing layout. The package offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The ESD321 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{FWD}. During ESD events, voltages as high as ±30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD321 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The ESD321 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

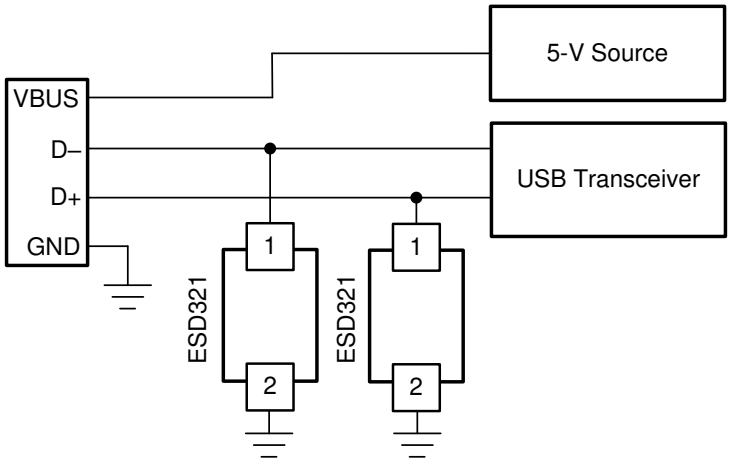


图 8-1. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two ESD321 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in 表 8-1 are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESD321 supports signal ranges between 0 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

8.2.2.2 Operating Frequency

The ESD321 has a 0.9 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

8.2.3 Application Curve

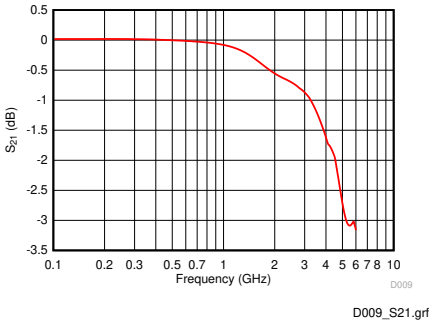


图 8-2. Insertion Loss Vs. Frequency

8.3 Power Supply Recommendations

The ESD321 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

8.4 Layout

8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

8.4.2 Layout Example

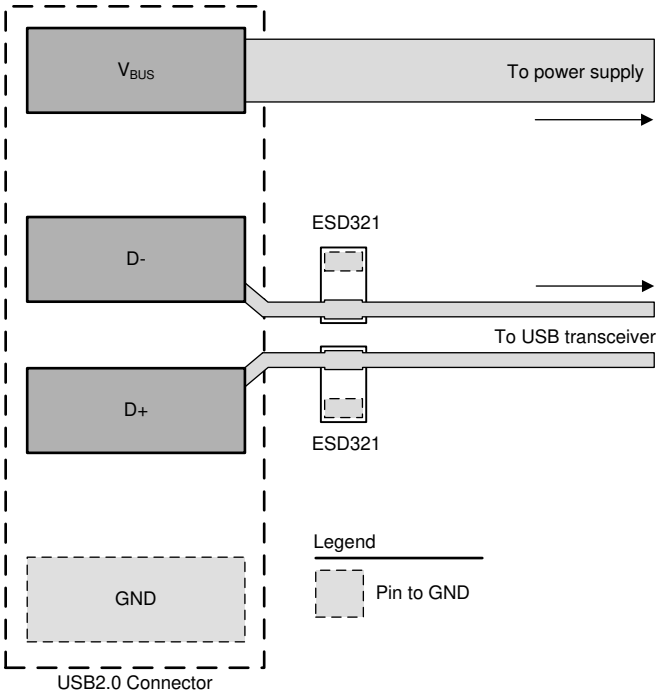


图 8-3. USB 2.0 ESD Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Generic ESD Device Evaluation Module*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD321DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A5, DD)	Samples
ESD321DYAR	ACTIVE	SOT-5X3	DYA	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	1L8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

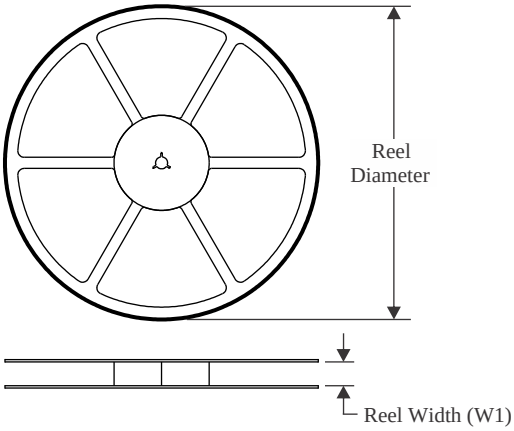
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

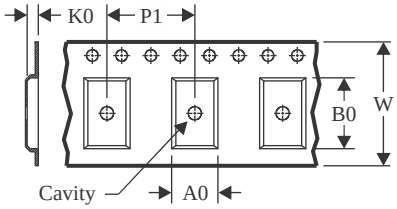
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

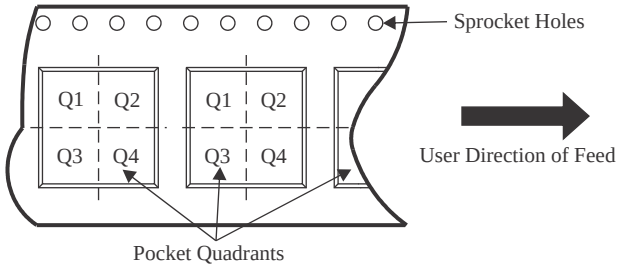


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

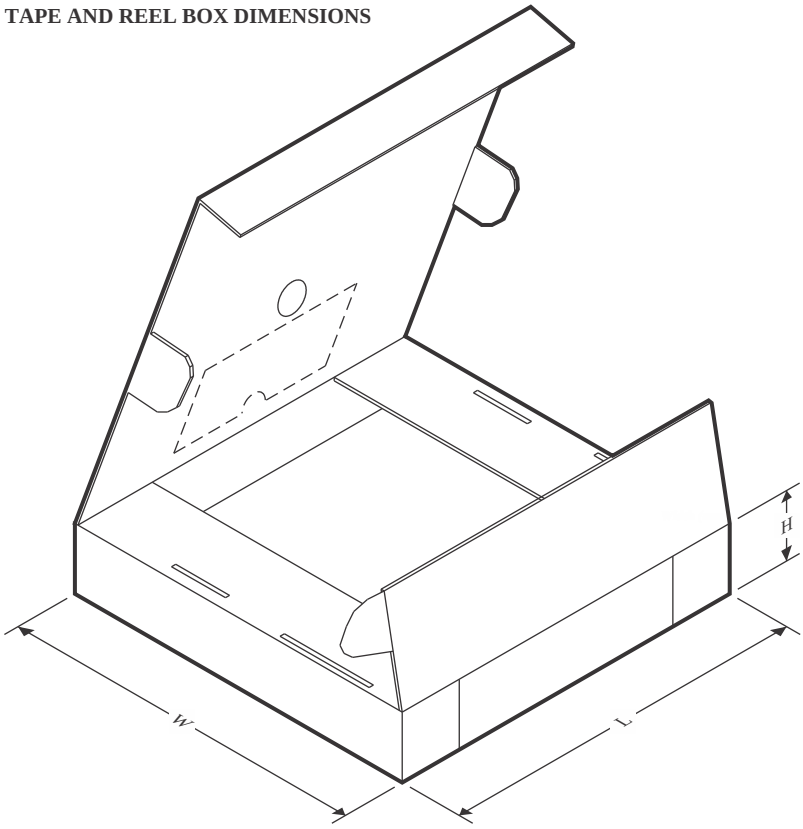
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD321DYAR	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

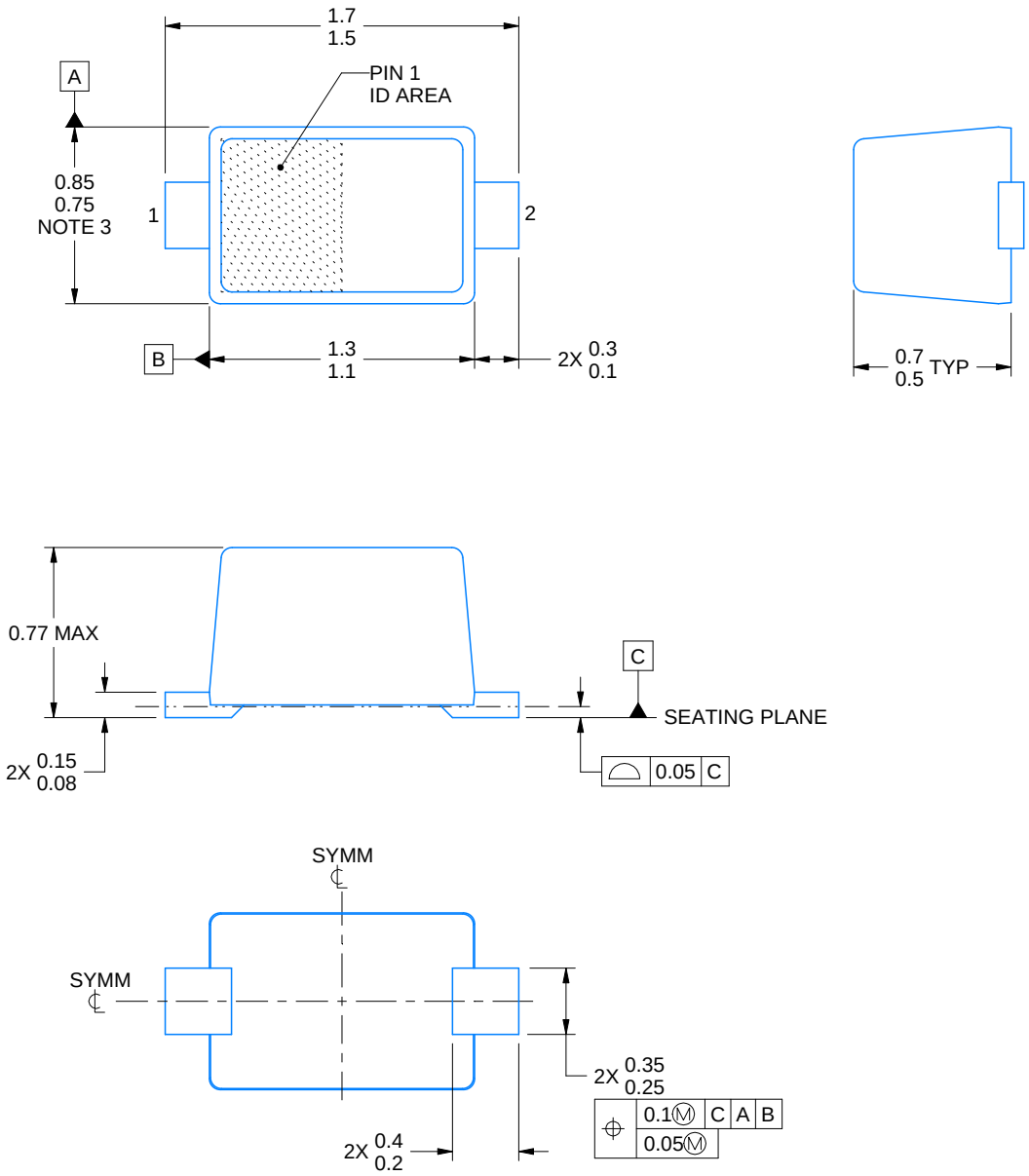
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD321DYAR	SOT-5X3	DYA	2	3000	210.0	200.0	42.0

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

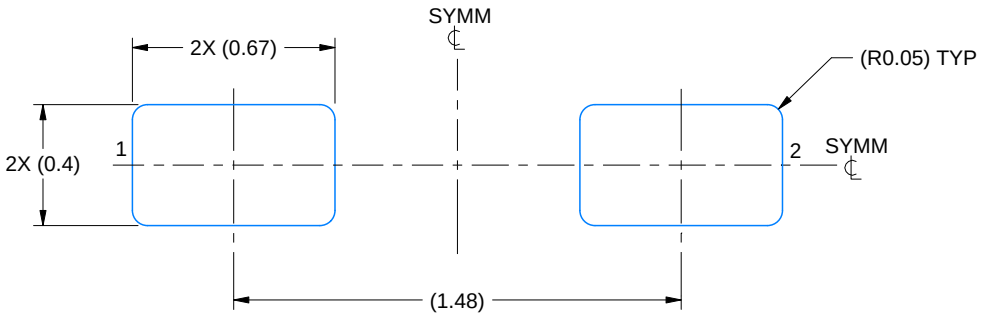
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height

EXAMPLE BOARD LAYOUT

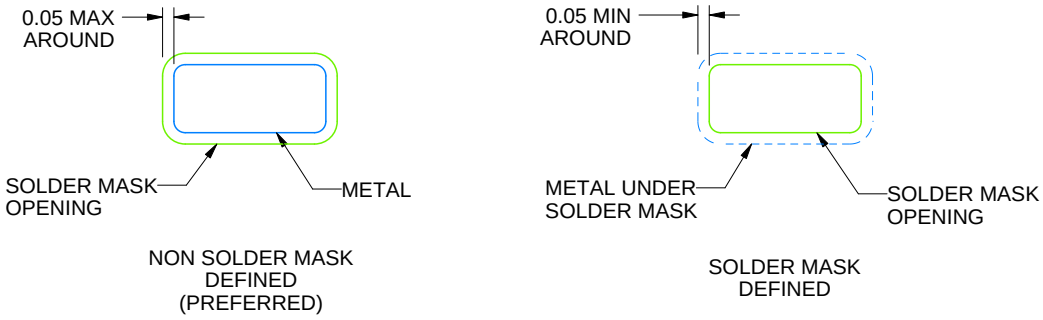
DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

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NOTES: (continued)

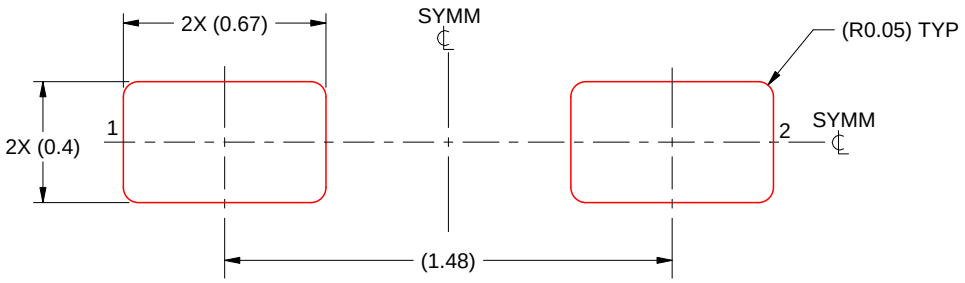
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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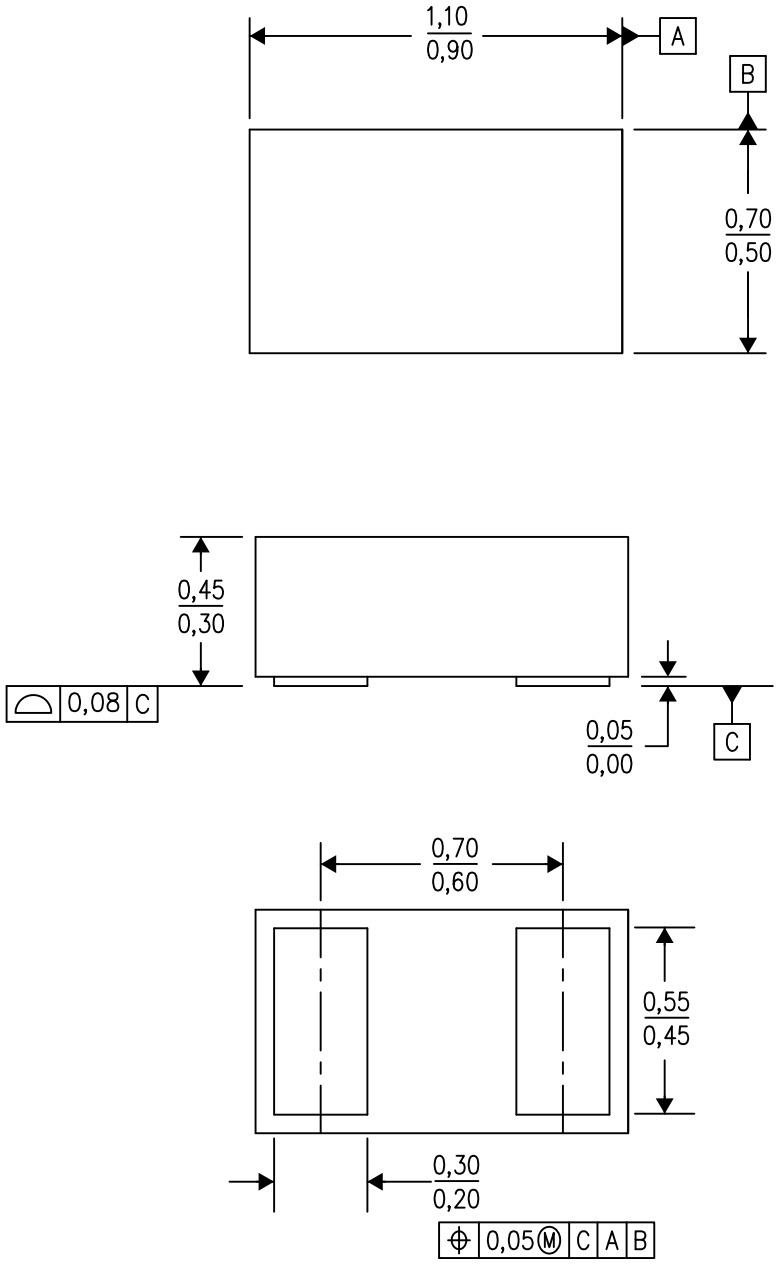
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

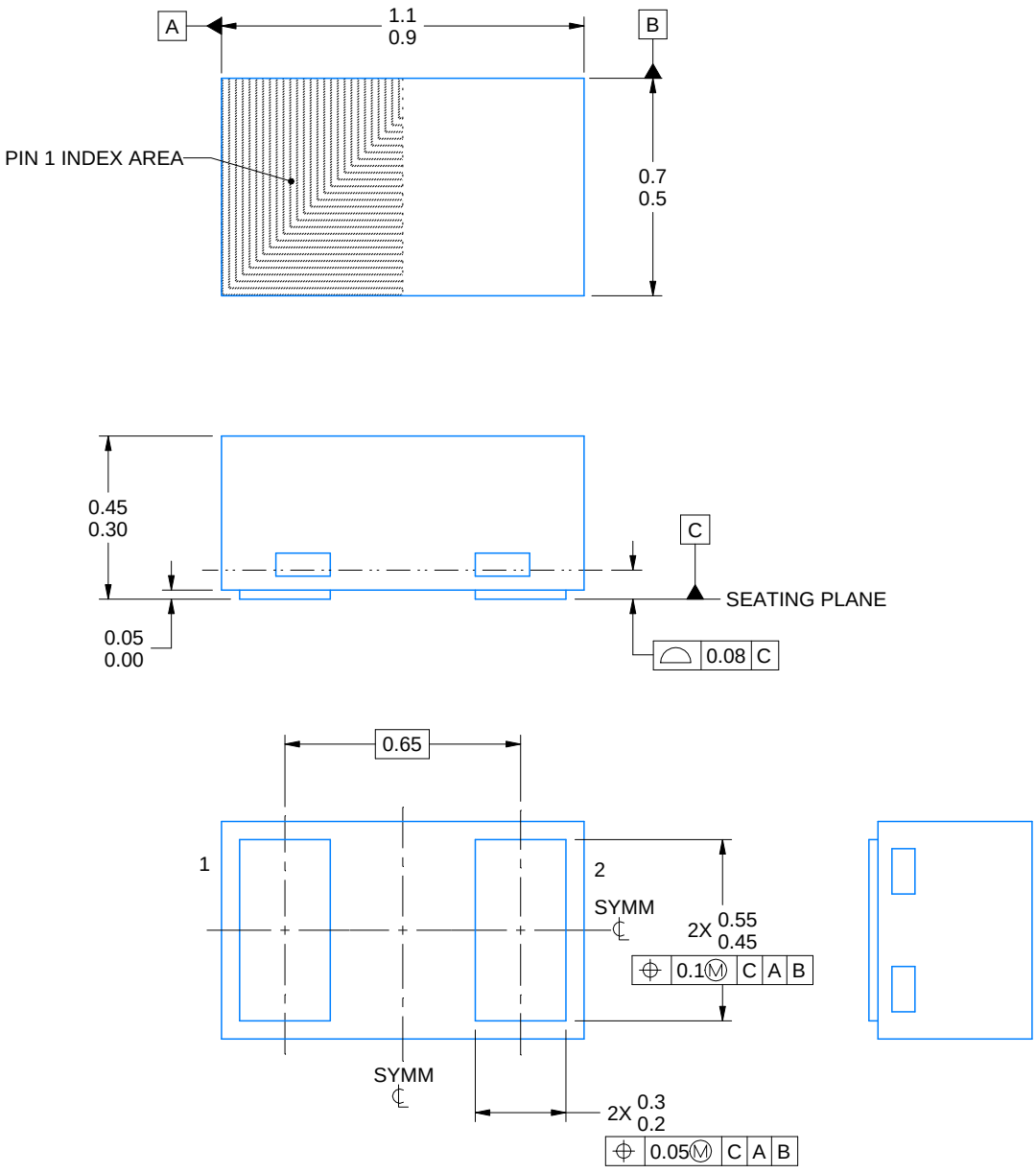
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

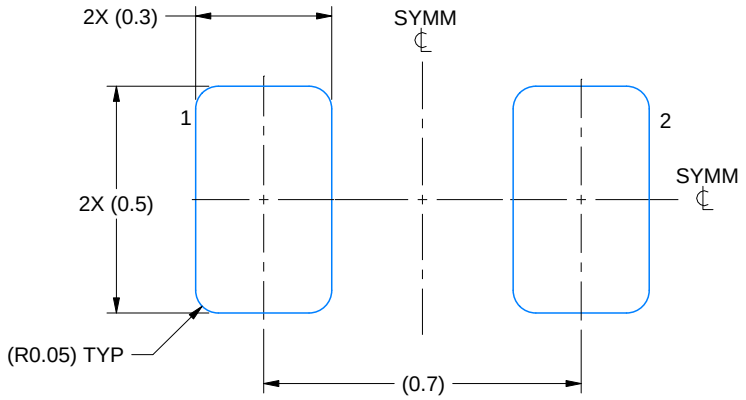
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

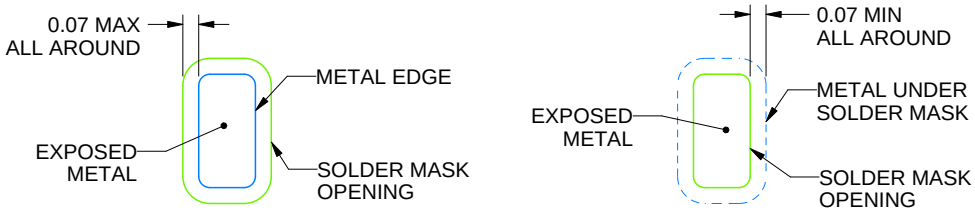
DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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NOTES: (continued)

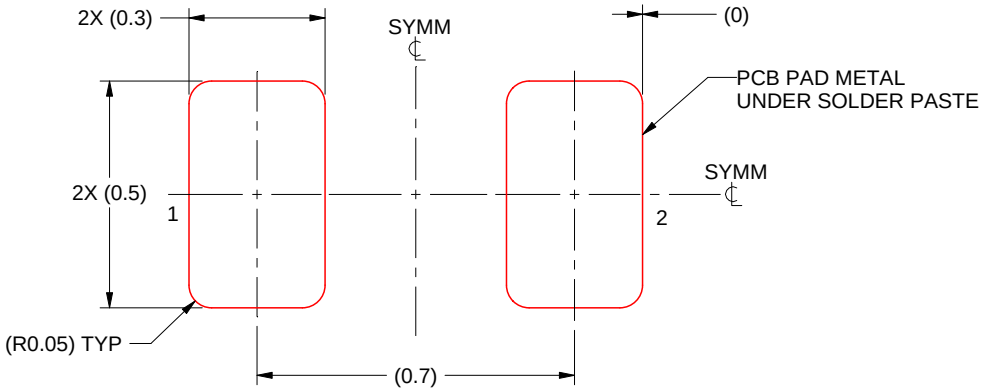
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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