TPS799 200-mA, Low-Quiescent Current, Ultralow Noise, High-PSRR Low-Dropout Linear Regulator

1 Features

- 200-mA low-dropout regulator with EN
- Multiple output voltage versions available:
  - Fixed outputs of 1.2 V to 4.5 V
  - Adjustable outputs from 1.20 V to 6.5 V
- Inrush current protection with EN toggle
- Low I_Q: 40 µA
- High PSRR:
  - 66 dB at 1 kHz
  - 51 dB at 10 kHz
- Stable with a low-ESR, 2-µF typical output capacitance
- Excellent load and line transient response
- 2% overall accuracy (load, line, and temperature)
- Very low dropout: 100 mV
- Packages:
  - 5-bump, thin, 0.97-mm × 1.34-mm DSBGA
  - 5-pin SOT-23-THIN
  - 6-pin WSON

2 Applications

- Base stations
- Smart phones
- EPOS
- Wearable electronics
- VCOs, RF
- Wireless LAN, Bluetooth®

3 Description

The TPS799 low-dropout (LDO), low-power linear regulator offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40-µA (typical) ground current.

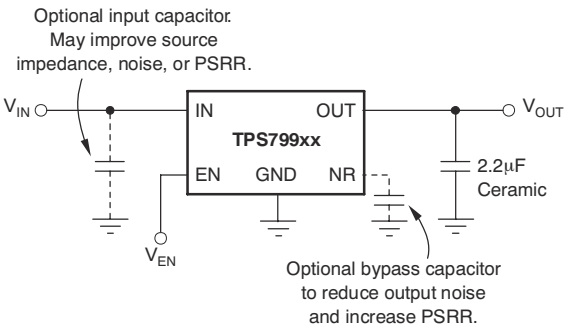
The TPS799 is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of typically 100 mV at a 200-mA output. The TPS799 uses a precision voltage reference and feedback loop to achieve an overall accuracy of 2% over all load, line, process, and temperature variations. The TPS799 features inrush current protection when the EN toggle is used to start the device, immediately clamping the current.

This device is fully specified over the temperature range of T_J = –40°C to +125°C, and is offered in a low-profile, die-sized ball grid array (DSBGA) package, making this device a good choice for wireless handsets and WLAN cards. This device is also offered in 5-pin SOT-23-THIN and 6-pin WSON packages.

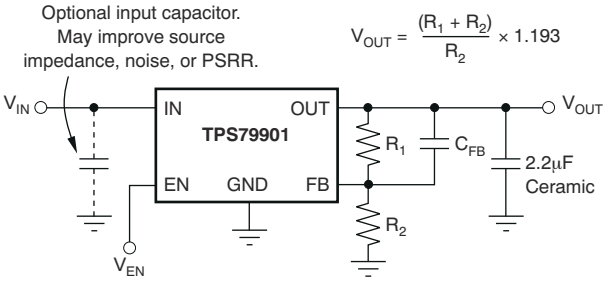
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS799	SOT-23-THIN (5)	2.90 mm × 1.60 mm
	WSON (6)	2.00 × 2.00 mm
	DSBGA (5)	1.34 mm × 0.97 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Typical Application Circuit: Fixed Voltage Versions



Typical Application Circuit: Adjustable Voltage Version

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (January 2015) to Revision L (September 2021)	Page
• Added PSRR value at 10 kHz to *Features* bullet	1
• Added missing packages to *Features* bullet	1
• Changed *SOT* to *SOT-23-THIN* and *SON* to *WSON* throughout document	1
• Changed *Applications* bullets	1
• Changed body size for DSBGA package in *Device Information* table	1
• Changed YZY package to YZU in *Pin Functions* table (typo)	3
• Added note (1) to *Recommended Operating Conditions*; moved from *Electrical Characteristics*	4
• Deleted *Input Voltage* from *Electrical Characteristics*; already shown in *Recommended Operating Conditions*	5
• Deleted *Junction Temperature* from *Electrical Characteristics*; already shown in *Recommended Operating Conditions*	5
• Changed *Do's and Don'ts* title to *What To Do and What Not To Do*	15

Changes from Revision J (August 2010) to Revision K (January 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed Features list	1
• Changed *Description* section	1
• Changed figure on front page; replaced device pinouts with application circuits	1
• Changed Pin Configuration and Functions section; updated table format, renamed pin packages	3
• Changed "free-air" to "junction" temperature in condition statement for *Absolute Maximum Ratings*	4
• Changed *free-air* to *junction* in Recommended Operating Conditions table conditions	4
• Added thermal information for additional device packages	4

5 Pin Configuration and Functions

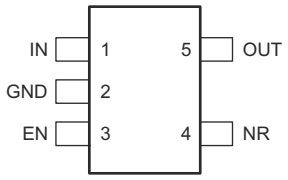


Figure 5-1. DDC Package (Fixed), 5-Pin SOT-23-THIN (Top View)

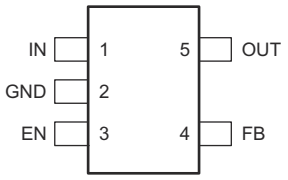


Figure 5-2. DDC Package (Adjustable), 5-Pin SOT-23-THIN (Top View)

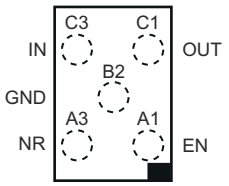


Figure 5-3. YZU Package (Fixed), 5-Pin DSBGA (Top View)

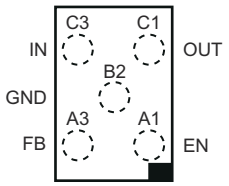


Figure 5-4. YZU Package (Adjustable), 5-Pin DSBGA (Top View)

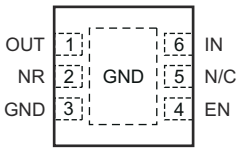


Figure 5-5. DRV Package (Fixed), 6-Pin WSON With Exposed Thermal Pad (Top View)

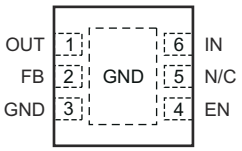


Figure 5-6. DRV Package (Adjustable), 6-Pin WSON With Exposed Thermal Pad (Top View)

Table 5-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	DDC	YZU	DRV		
IN	1	C3	6	I	Input supply.
GND	2	B2	3, Pad	—	Ground. The pad must be tied to GND.
EN	3	A1	4	I	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	A3	2	—	Fixed voltage versions only. Noise reduction; connecting this pin to an external capacitor bypasses noise generated by the internal band gap. This capacitor allows output noise to be reduced to very low levels.
FB	4	A3	2	I	Adjustable voltage version only. Feedback; this pin is the input to the control loop error amplifier, and sets the output voltage of the device.
OUT	5	C1	1	O	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance ≥ 2 µF) is required from this pin to ground.
N/C	—	—	5	—	Not internally connected. This pin must either be left open, or tied to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	7.0	V
	EN	–0.3	V_{IN} + 0.3	V
	OUT	–0.3	V_{IN} + 0.3	V
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage(1)	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	–40		125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC(1)		TPS799			UNIT
		DDC (SOT-23-THIN)	DRV (WSON)	YZU (DSBGA)	
		5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.3	74.2	143.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	58.8	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	145.9	84.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.7	54.4	84.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	7.2	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901, V_{OUT} = 3.0 V; typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Internal reference (TPS79901)			1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901)			V_{FB}		6.5 – V_{DO}	V
	Output accuracy, nominal	T_J = 25°C		–1%		1%	
	Output accuracy(1) over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V 500 µA ≤ I_{OUT} ≤ 200 mA		–2%	±1%	2%	
$\Delta V_{O(\Delta VI)}$	Line regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage(1) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	I_{OUT} = 200 mA	$V_{OUT(nom)}$ ≤ 3.3 V		100	175	mV
			$V_{OUT(nom)}$ ≥ 3.3 V		90	160	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		220	400	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1	µA
I_{FB}	Feedback pin current (TPS79901)			–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		
			f = 10 kHz		51		
			f = 100 kHz		38		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.85 V	C_{NR} = 0.01 µF		10.5 × V_{OUT}		μV_{RMS}
			C_{NR} = none		94 × V_{OUT}		
	Start-up time	V_{OUT} = 2.85 V, R_L = 14 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.001 µF		45		µs
			C_{NR} = 0.047 µF		45		
			C_{NR} = 0.01 µF		50		
			C_{NR} = none		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
UVLO	Undervoltage lockout	V_{IN} rising		1.90	2.20	2.65	V
	UVLO hysteresis	V_{IN} falling			70		mV
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		

(1) V_{DO} is not measured for devices with $V_{OUT(nom)}$ < 2.8 V because minimum V_{IN} = 2.7 V.

6.6 Typical Characteristics

at T_J= –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901, V_{OUT} = 3.0 V; typical values are at T_J = 25°C

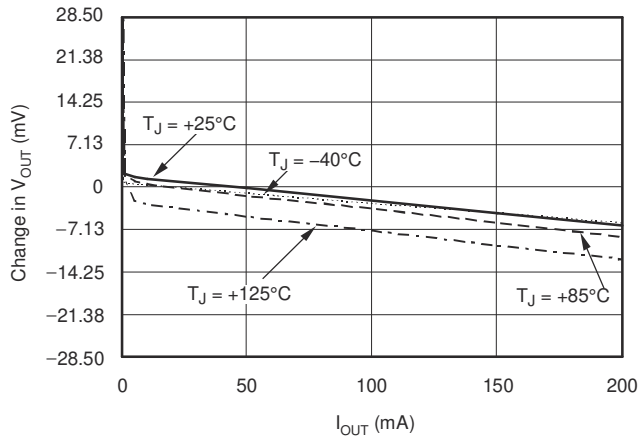


Figure 6-1. Load Regulation

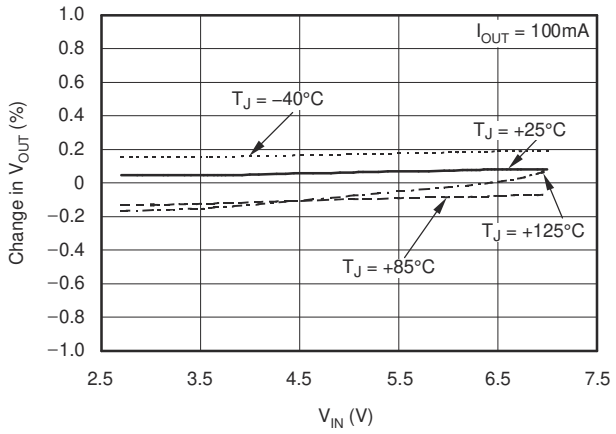


Figure 6-2. Line Regulation

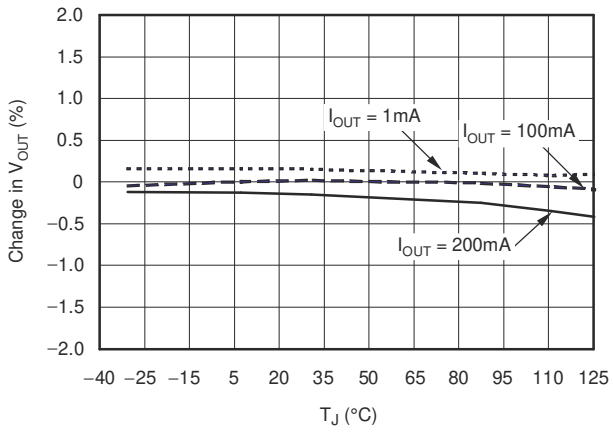


Figure 6-3. Output Voltage vs Junction Temperature

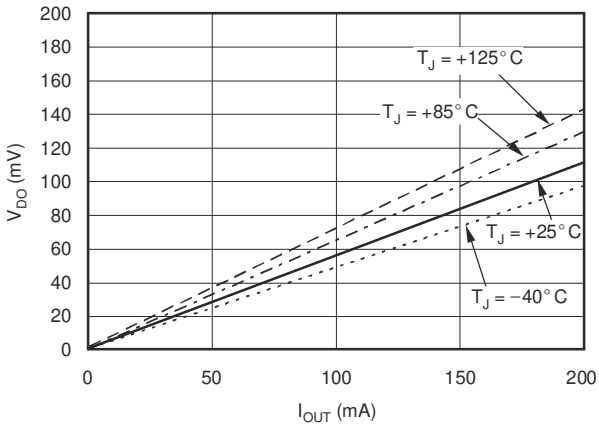


Figure 6-4. TPS799285 Dropout Voltage vs Output Current

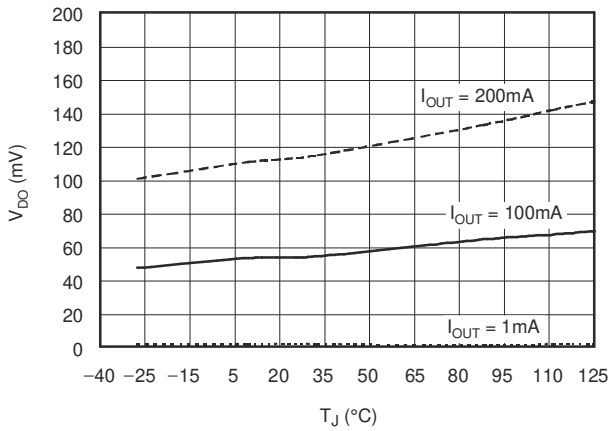


Figure 6-5. TPS799285 Dropout Voltage vs Junction Temperature

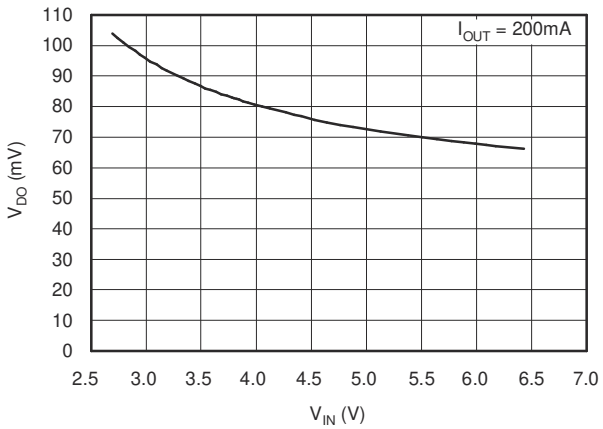


Figure 6-6. TPS79901 Dropout vs Input Voltage

6.6 Typical Characteristics (continued)

at T_J= –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901, V_{OUT} = 3.0 V; typical values are at T_J = 25°C

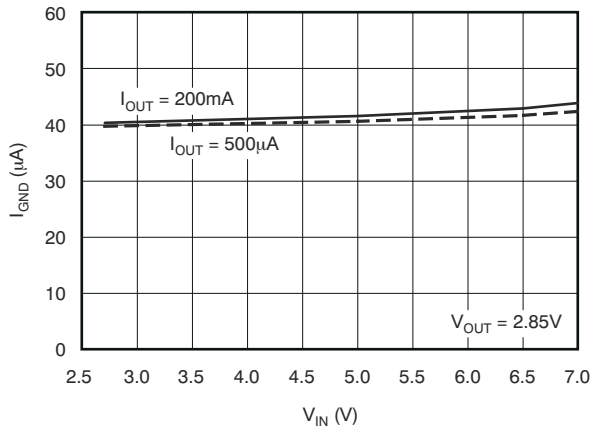


Figure 6-7. Ground Pin Current vs Input Voltage

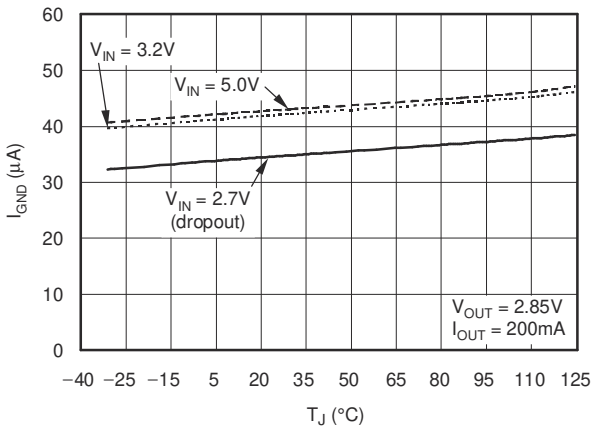


Figure 6-8. TPS799285 Ground Pin Current vs Junction Temperature

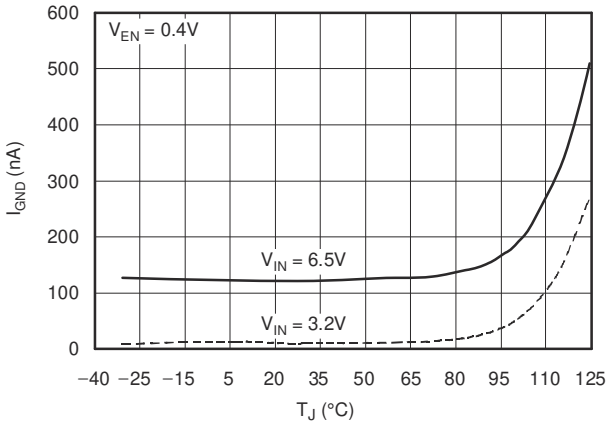
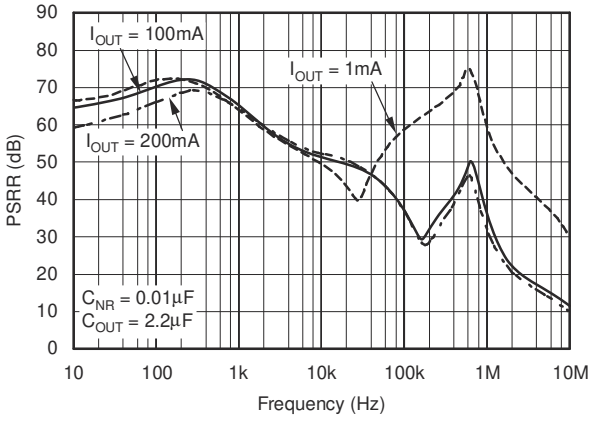
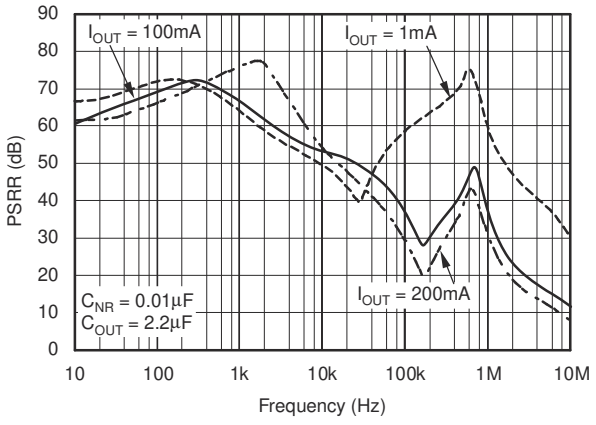


Figure 6-9. Ground Pin Current (Disabled) vs Junction Temperature



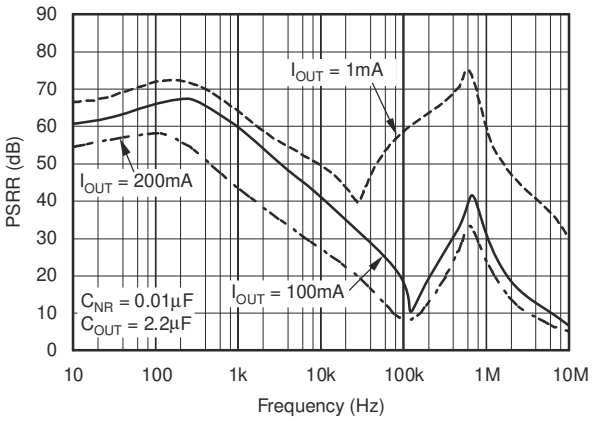
VIN – VOUT = 1.0 V

Figure 6-10. TPS799285 Power-Supply Ripple Rejection vs Frequency



VIN – VOUT = 0.5 V

Figure 6-11. TPS799285 Power-Supply Ripple Rejection vs Frequency

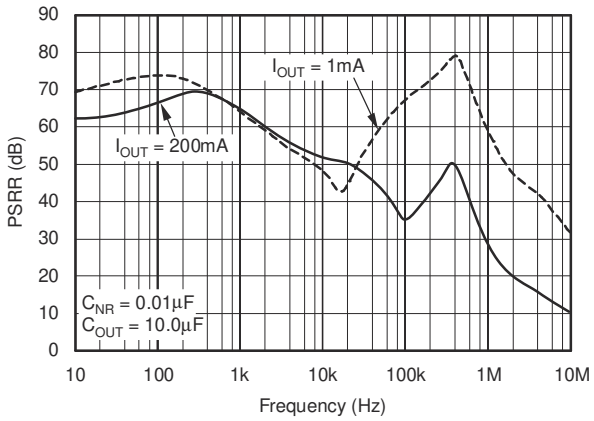


VIN – VOUT = 0.25 V

Figure 6-12. TPS799285 Power-Supply Ripple Rejection vs Frequency

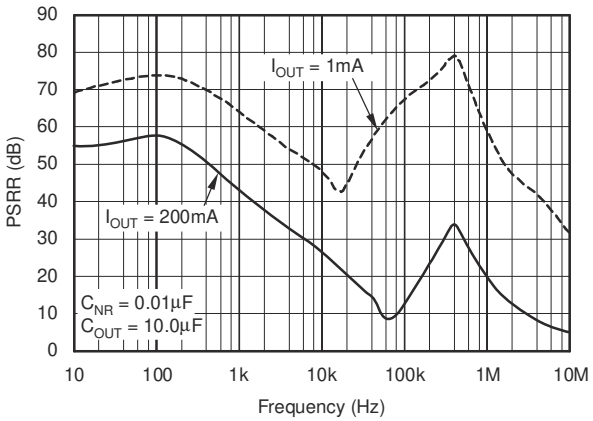
6.6 Typical Characteristics (continued)

at T_J= –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901, V_{OUT} = 3.0 V; typical values are at T_J = 25°C



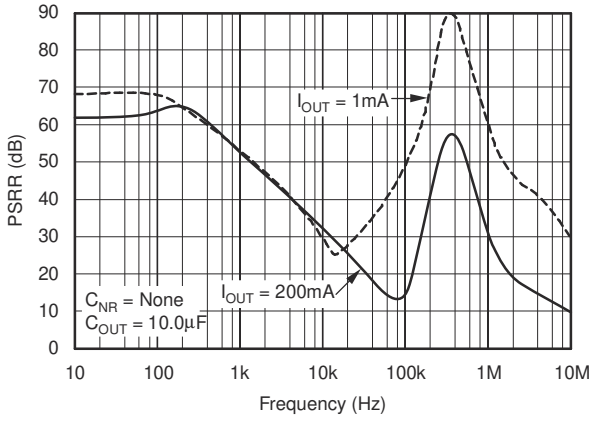
V_{IN} – V_{OUT} = 1.0 V

Figure 6-13. TPS799285 Power-Supply Ripple Rejection vs Frequency



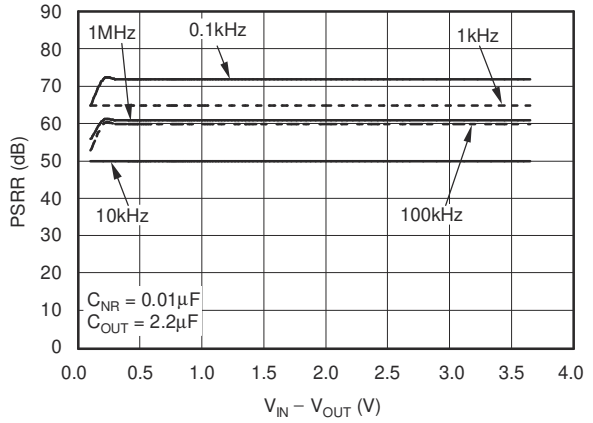
V_{IN} – V_{OUT} = 0.25 V

Figure 6-14. TPS799285 Power-Supply Ripple Rejection vs Frequency



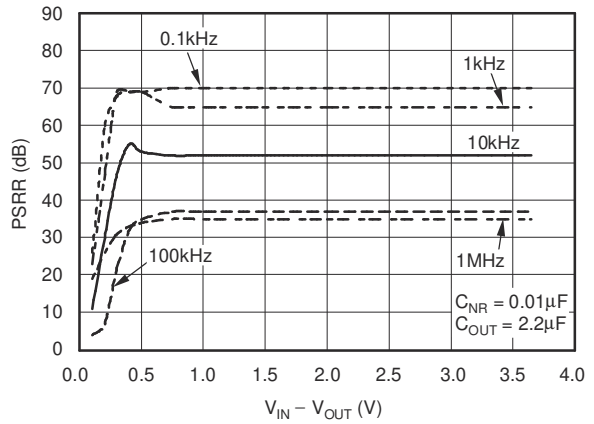
V_{IN} – V_{OUT} = 1.0 V

Figure 6-15. TPS799285 Power-Supply Ripple Rejection vs Frequency



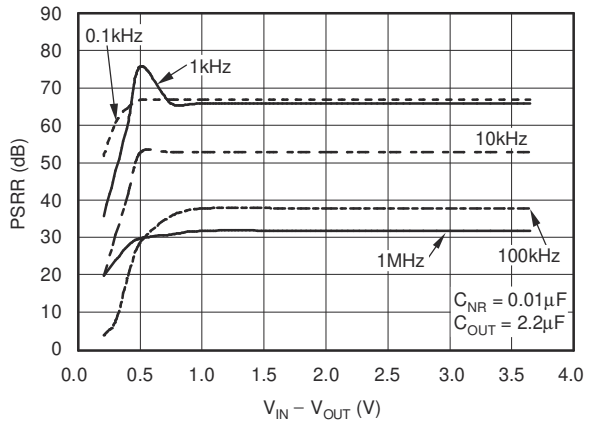
I_{OUT} = 1 mA

Figure 6-16. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}



I_{OUT} = 100 mA

Figure 6-17. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}



I_{OUT} = 200 mA

Figure 6-18. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}

6.6 Typical Characteristics (continued)

at T_J= –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901, V_{OUT} = 3.0 V; typical values are at T_J = 25°C

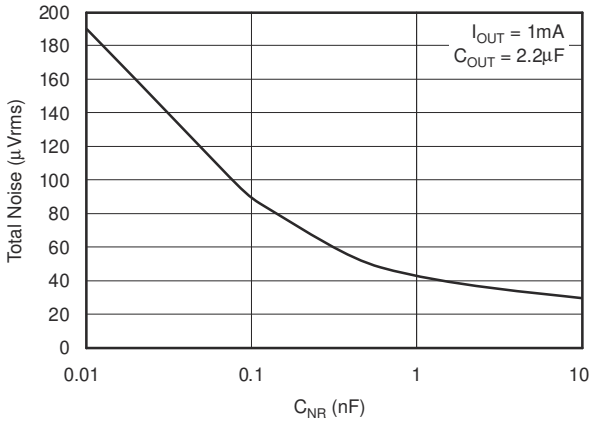


Figure 6-19. TPS799285 Total Noise vs C_{NR}

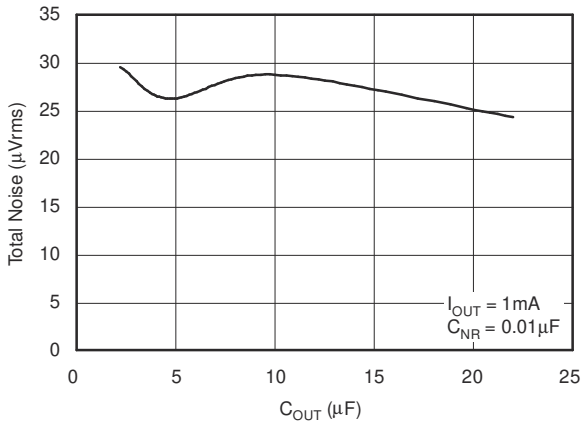


Figure 6-20. TPS799285 Total Noise vs C_{OUT}

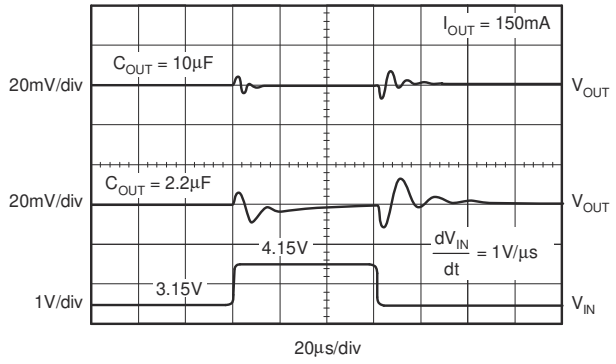


Figure 6-21. TPS799285 Line Transient Response

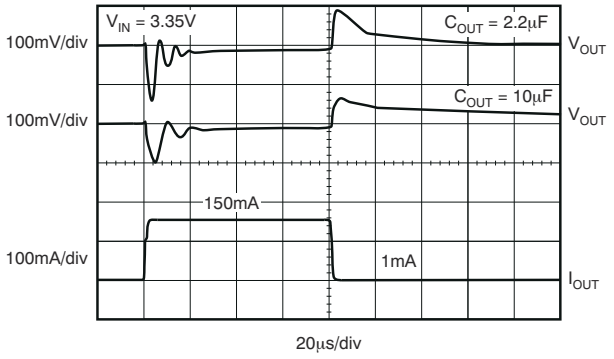


Figure 6-22. TPS799285 Load Transient Response

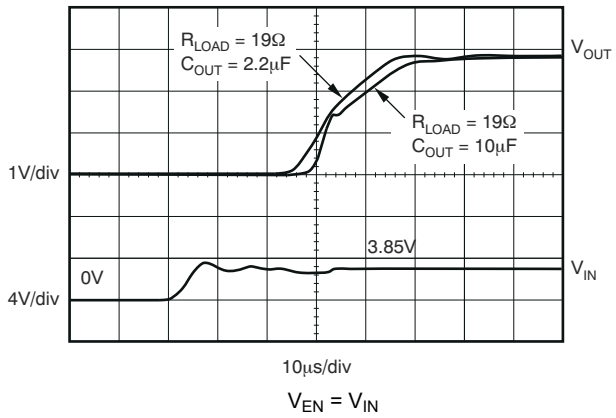


Figure 6-23. TPS799285 Turn-On Response

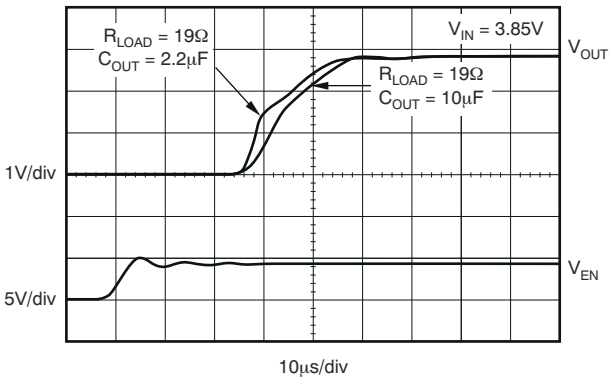


Figure 6-24. TPS799285 Enable Response

6.6 Typical Characteristics (continued)

at T_J= –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901, V_{OUT} = 3.0 V; typical values are at T_J = 25°C

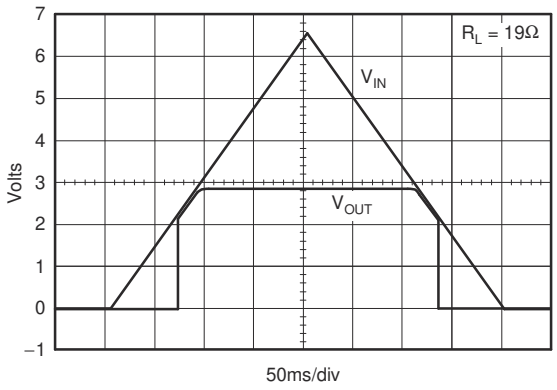


Figure 6-25. TPS799285 Power-Up and Power-Down

7 Detailed Description

7.1 Overview

The TPS799 low-dropout (LDO) regulator combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make this device an excellent choice for portable applications. This device has thermal and overcurrent protection, and is fully specified from –40°C to +125°C.

The TPS799 also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as shown in the *Functional Block Diagrams*.

7.2 Functional Block Diagrams

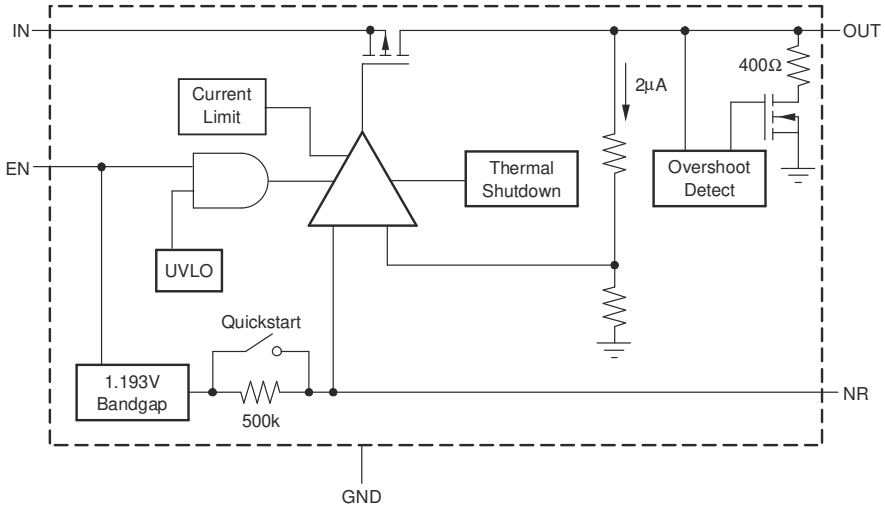


Figure 7-1. Fixed-Voltage Versions

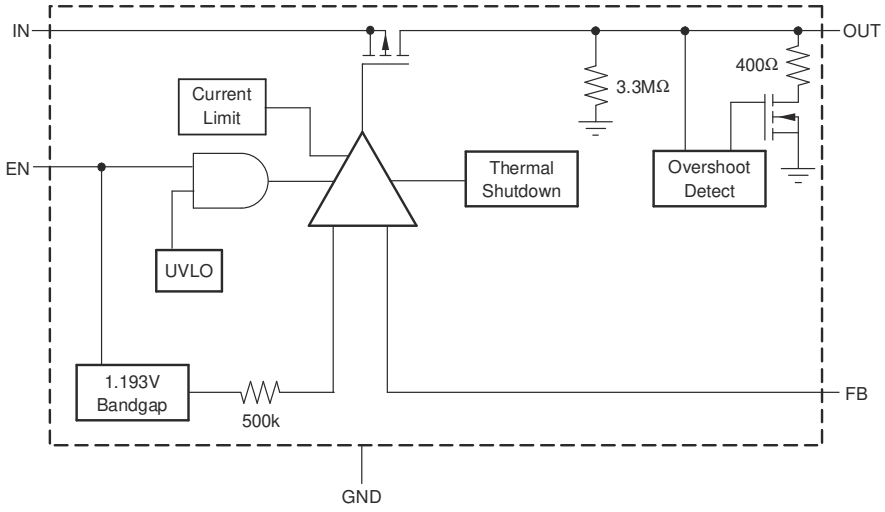


Figure 7-2. Adjustable-Voltage Versions

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS799 internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS799 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Start Up

The TPS799 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see the *Functional Block Diagrams*). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

For fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start up is somewhat slower. The start-up switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during start-up, use a 0.01-µF or smaller capacitor.

7.3.4 Undervoltage Lockout (UVLO)

The TPS799 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that undershoot transients are typically ignored on the input if these transients are less than 50 µs in duration.

7.4 Device Functional Modes

Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS799 LDO regulator provides high PSRR while maintaining ultra-low current consumption. The device also features inrush current protection and overshoot detection at the output.

8.2 Typical Application

Figure 8-1 and Figure 8-2 show the basic circuit connections.

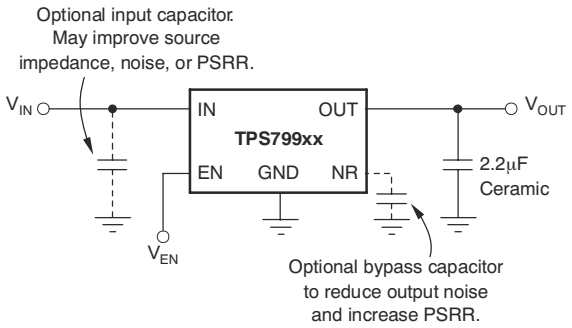


Figure 8-1. Typical Application Circuit for Fixed Voltage Versions

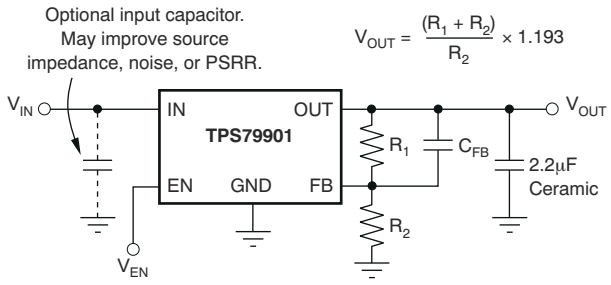


Figure 8-2. Typical Application Circuit for Adjustable Voltage Version

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS799 is designed to be stable with standard ceramic capacitors with values of 2.2 µF or greater. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1.0 Ω.

8.2.2.2 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS799, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with C_{NR} = 0.01 µF total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

8.2.2.3 Dropout Voltage

The TPS799 uses a PMOS pass transistor to achieve a low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 6-10 through Figure 6-18 in the *Typical Characteristics* section.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799 is enhanced by an active pulldown device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

8.2.2.5 Minimum Load

The TPS799 is stable with no output load. To meet the specified accuracy, a minimum load of 500 µA is required. With loads less than 500 µA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown device to turn on. The output pulldown device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 µA. In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

8.2.2.6 Feedback Capacitor Requirements (TPS79901 Only)

The feedback capacitor, C_{FB}, shown in Figure 8-2 is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Fixed voltage versions have an internal 30-pF feedback capacitor that is quick-charged at start up. The adjustable version does not have this quick-charge circuit, so use values below 5 pF to ensure fast start up; values above 47 pF can be used to implement an output

voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

8.2.3 Application Curve

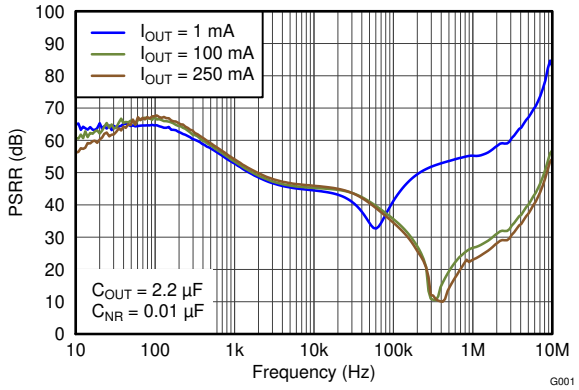


Figure 8-3. Power-Supply Rejection Ratio vs Frequency

8.3 What To Do and What Not To Do

Do place at least one 2.2-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.1.2 Thermal Information

10.1.2.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least

35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades device reliability.

10.1.2.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

10.1.2.3 Package Mounting

Solder pad footprint recommendations for the TPS799 are available from the TI's website at www.ti.com.

10.2 Layout Example

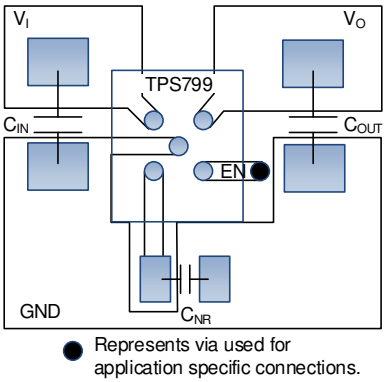


Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS799. This EVM, the TPS799 evaluation module, can be requested at the Texas Instruments web site through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS799 is available through the product folders under simulation models.

11.1.2 Device Nomenclature

Table 11-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS799**xx(x)** ***yyy z***	**xx(x)** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **yyy** is package designator. **z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *TPS799xxEVM-105* user's guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79901DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVRG4	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWT	Samples
TPS79901YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E9	Samples
TPS79901YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E9	Samples
TPS799125YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YZ	Samples
TPS799125YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YZ	Samples
TPS79912DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912DRVTG4	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCF	Samples
TPS79912YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F8	Samples
TPS79912YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F8	Samples
TPS79913DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BUJ	Samples
TPS79913DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BUJ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79913YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F9	Samples
TPS79915DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWU	Samples
TPS79915YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EA	Samples
TPS79915YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EA	Samples
TPS799185DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGP	Samples
TPS799185DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGP	Samples
TPS799185YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZA	Samples
TPS799185YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZA	Samples
TPS79918DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWV	Samples
TPS79918YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EB	Samples
TPS79918YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EB	Samples
TPS799195DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BTP	Samples
TPS799195DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BTP	Samples
TPS799195YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AO	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS799195YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AO	Samples
TPS79919YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TPS79920YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GA	Samples
TPS79921YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G7	Samples
TPS79925DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWW	Samples
TPS79925DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWW	Samples
TPS79925YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EC	Samples
TPS79925YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EC	Samples
TPS79926YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F3	Samples
TPS79926YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F3	Samples
TPS79927DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWE	Samples
TPS79927DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWE	Samples
TPS79927DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPM	Samples
TPS79927DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPM	Samples
TPS79927YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F5	Samples
TPS799285DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXY	Samples
TPS799285DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXY	Samples
TPS799285DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BST	Samples
TPS799285DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BST	Samples
TPS799285YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EE	Samples
TPS79928DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79928DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWX	Samples
TPS79928YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ED	Samples
TPS79928YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ED	Samples
TPS79930DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXZ	Samples
TPS79930YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EF	Samples
TPS79930YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EF	Samples
TPS799315DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGQ	Samples
TPS799315DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGQ	Samples
TPS799315YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GP	Samples
TPS799315YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GP	Samples
TPS79932YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(F4, FY)	Samples
TPS79933DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DDCTG4	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79933DRVRG4	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933DRVTG4	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AXX	Samples
TPS79933YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EG	Samples
TPS79933YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EG	Samples
TPS79942DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJQ	Samples
TPS79942DDCRG4	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJQ	Samples
TPS79942DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJQ	Samples
TPS79945YZUR	ACTIVE	DSBGA	YZU	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FK	Samples
TPS79945YZUT	ACTIVE	DSBGA	YZU	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS799 :

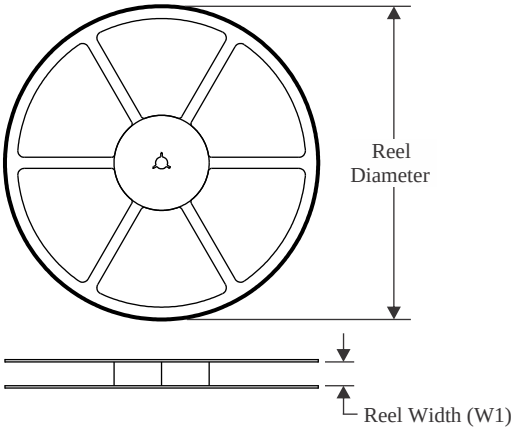
- Automotive : TPS799-Q1

NOTE: Qualified Version Definitions:

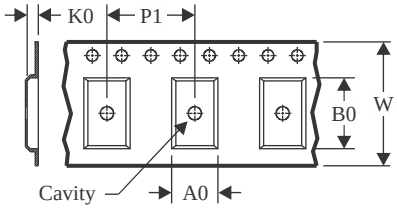
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

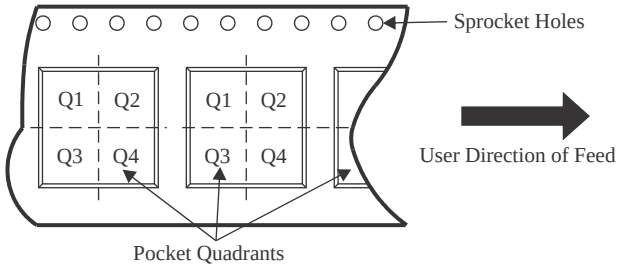


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

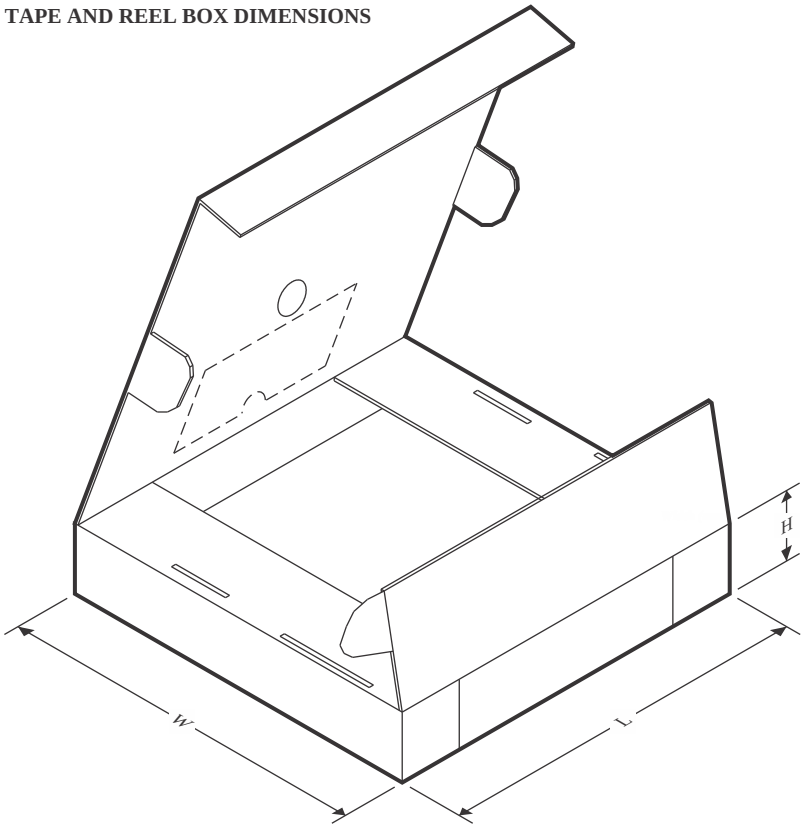
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79901DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79901DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79901DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79901DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79901YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79901YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799125YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799125YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79912DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79912DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79912DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79912DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79912YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79912YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79913DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79913DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79913YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79915DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79915YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799185DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799185DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799185YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799185YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79918DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79918DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79918DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79918DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79918YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79918YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799195DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799195DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799195YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799195YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79919YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79920YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79921YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79925DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79925DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79925YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79925YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79926YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79926YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79927DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79927DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79927YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799285DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799285DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799285DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS799285DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79928DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79928DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79928DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79928DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79928YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79928YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79930DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79930YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79930YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799315DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799315DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS799315YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS799315YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79932YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79933DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79933DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS79933DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79933YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79933YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79942DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79942DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79945YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS79945YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	183.0	183.0	20.0
TPS79901DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79901DDCT	SOT-23-THIN	DDC	5	250	183.0	183.0	20.0
TPS79901DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79901DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79901DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS79901YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79901YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS799125YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799125YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79912DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79912DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79912DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79912DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS79912YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79912YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79913DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79913DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0

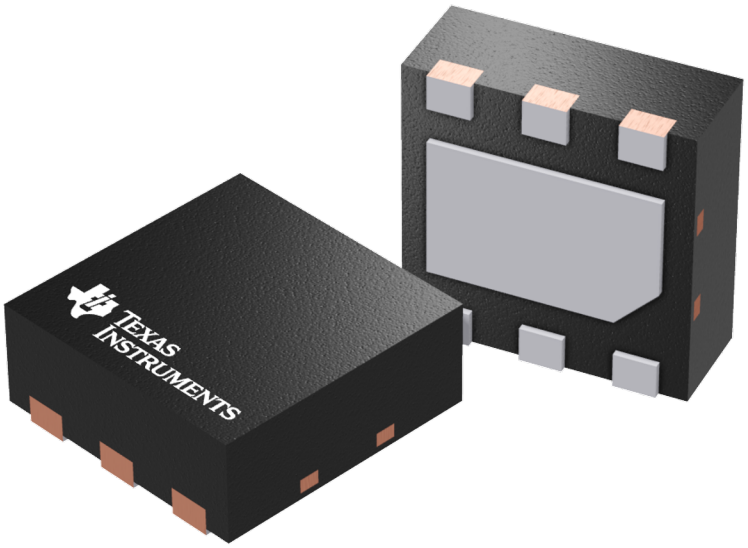
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79913YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79915DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79915DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79915YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79915YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS799185DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS799185DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS799185YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799185YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79918DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79918DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79918DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79918DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS79918YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79918YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS799195DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS799195DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS799195YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799195YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79919YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79920YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79921YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS79925DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79925DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79925YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79925YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79926YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79926YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79927DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79927DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79927DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79927DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS79927YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS799285DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS799285DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS799285DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS799285DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS79928DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79928DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79928DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79928DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS79928YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79928YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	183.0	183.0	20.0
TPS79930DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79930DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79930YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79930YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS799315DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS799315DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS799315YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS799315YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79932YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79933DDCR	SOT-23-THIN	DDC	5	3000	183.0	183.0	20.0
TPS79933DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79933DDCT	SOT-23-THIN	DDC	5	250	183.0	183.0	20.0
TPS79933DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS79933YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79933YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS79942DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79942DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS79945YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS79945YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

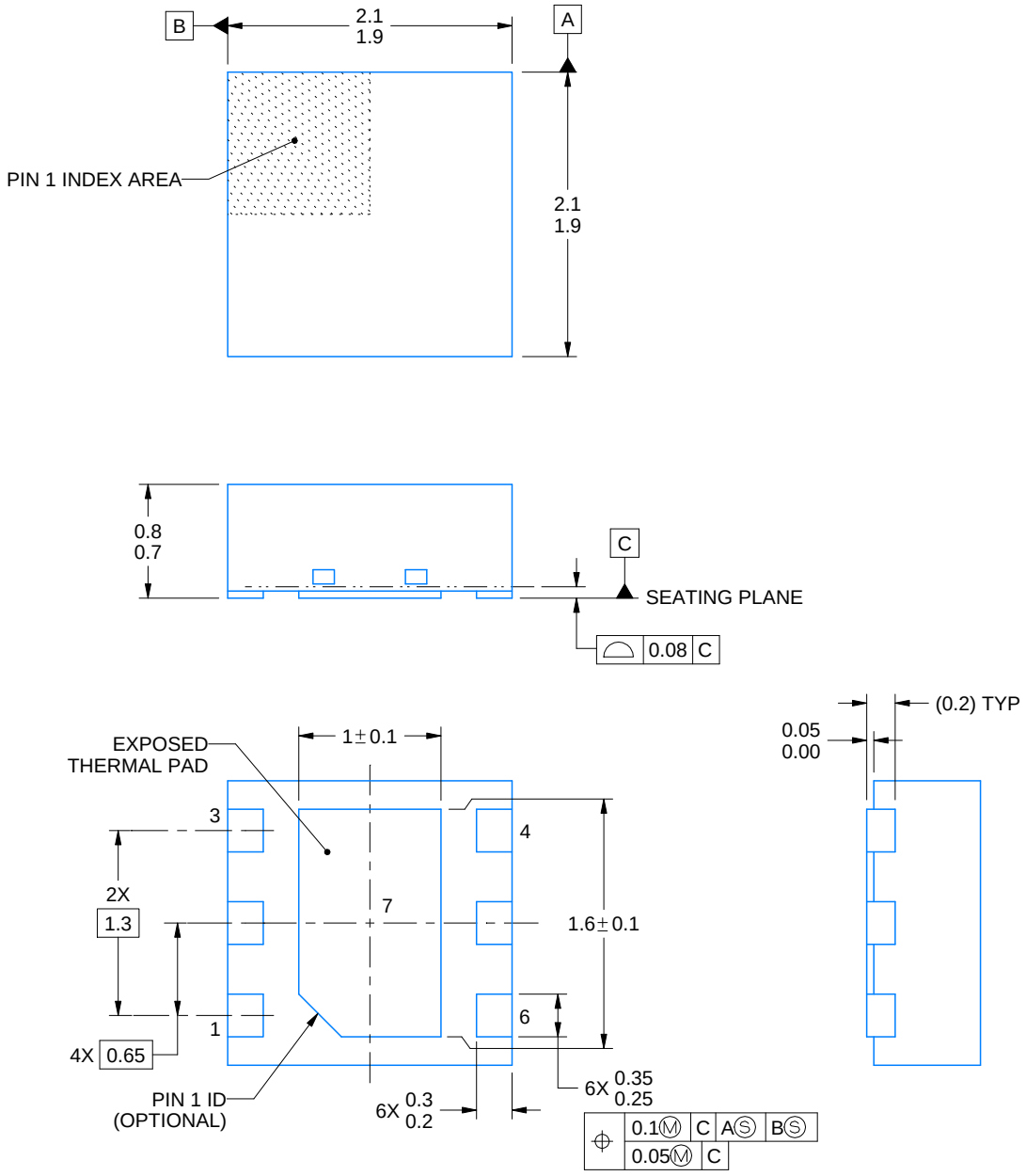
4206925/F

PACKAGE OUTLINE

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

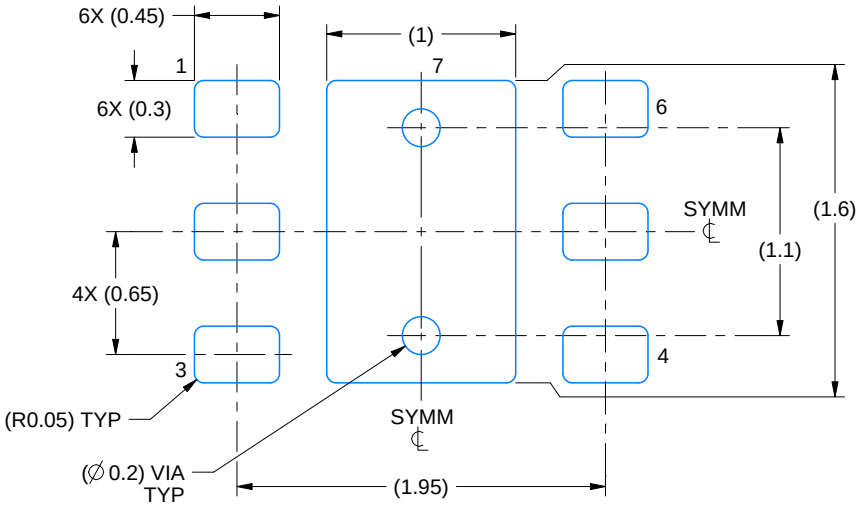
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

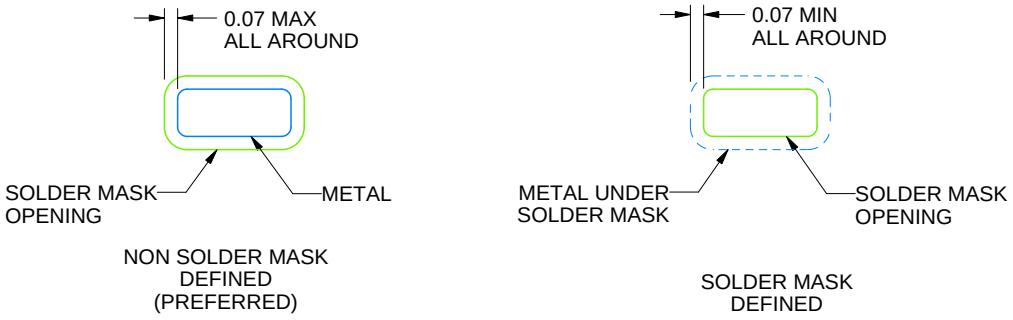
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

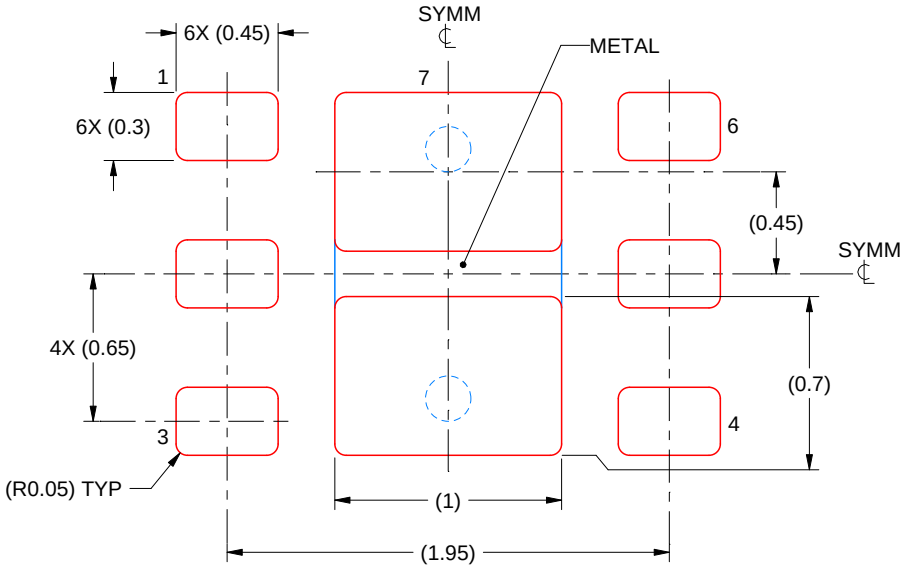
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

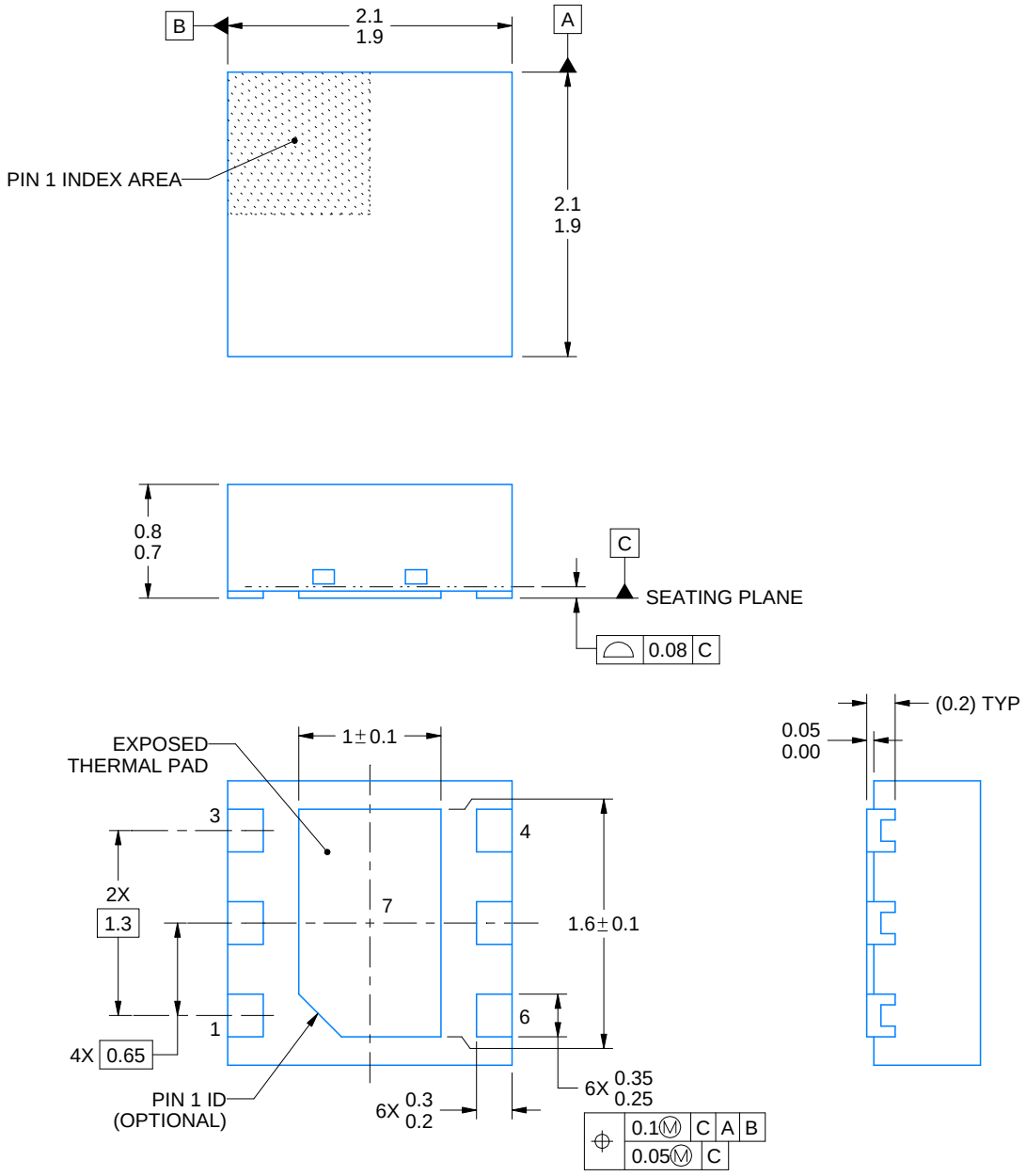
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4225563/A 12/2019

NOTES:

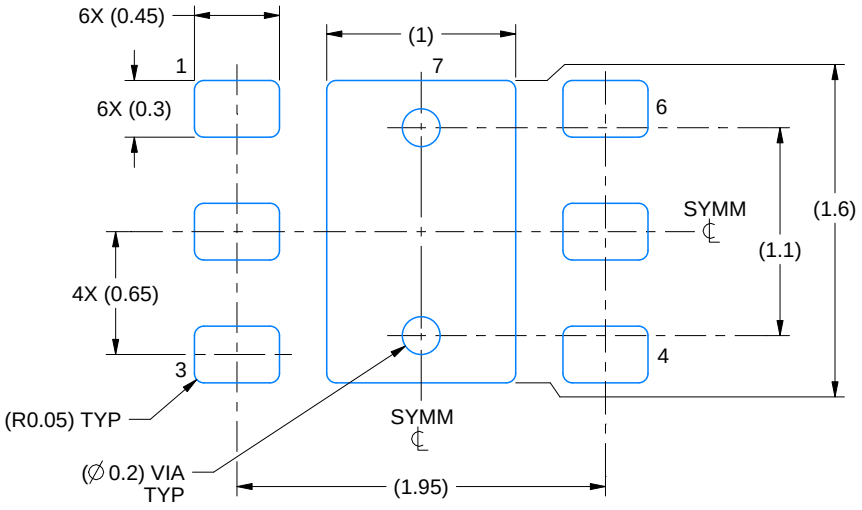
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

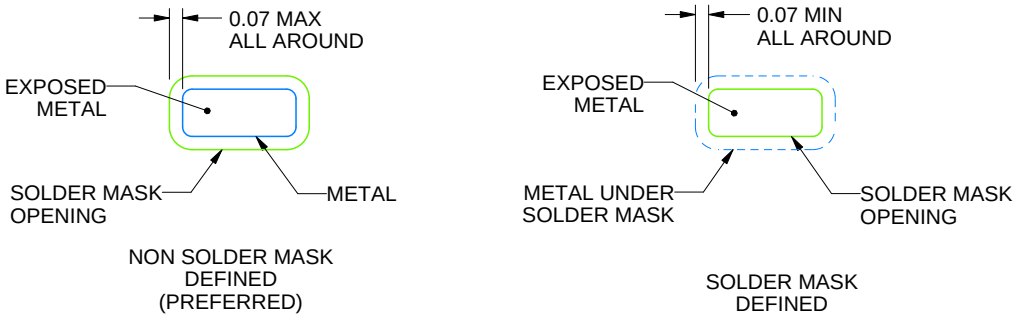
DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

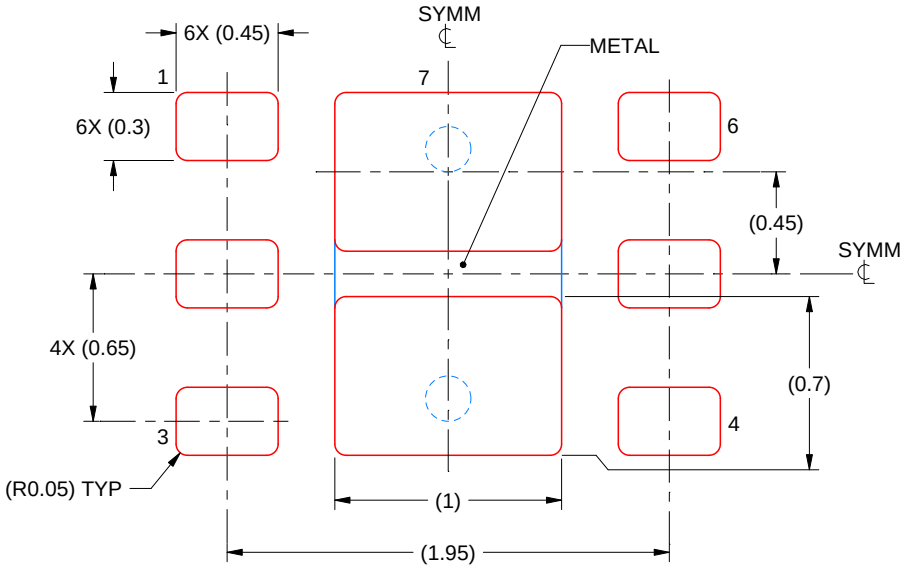


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

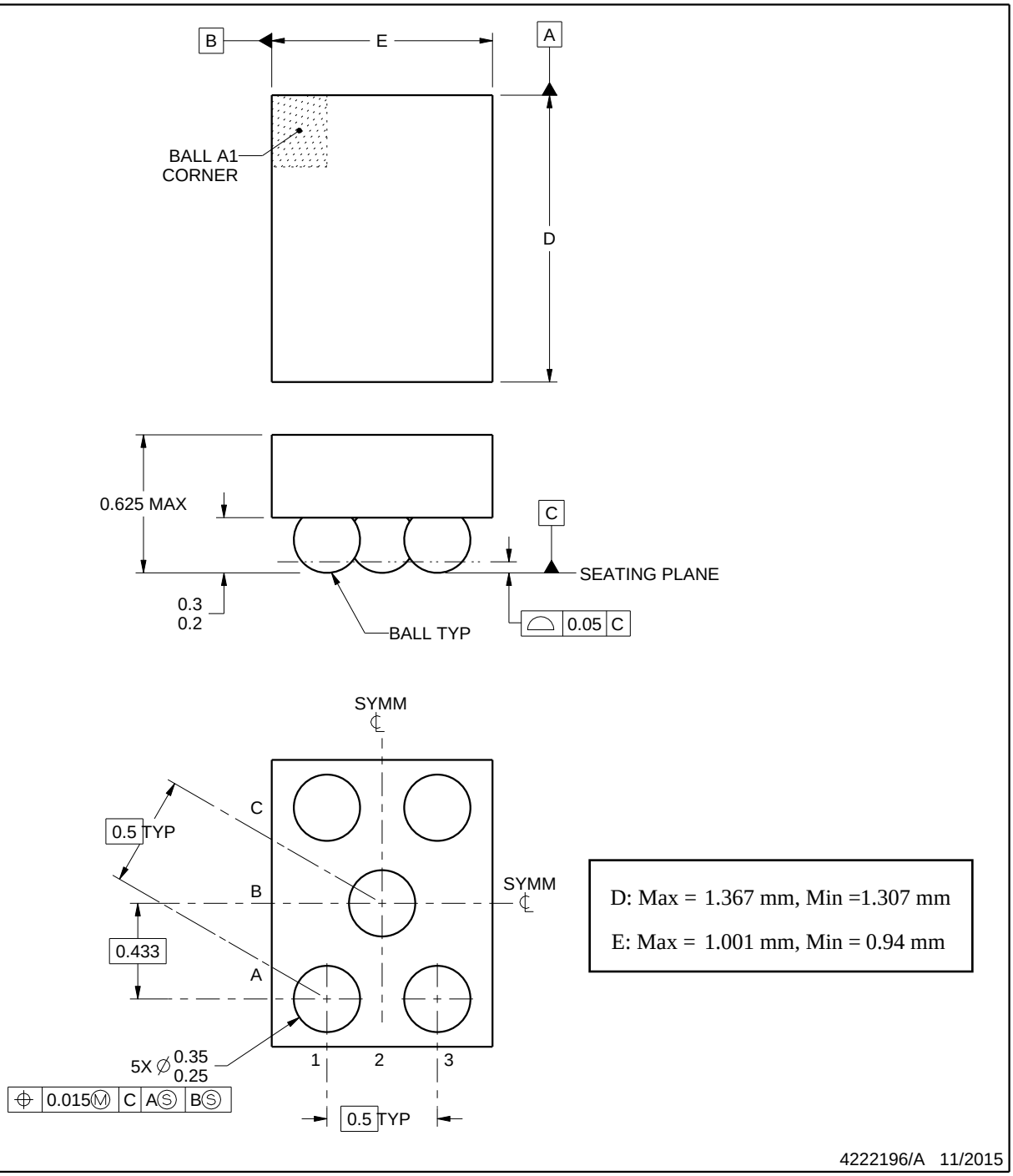
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

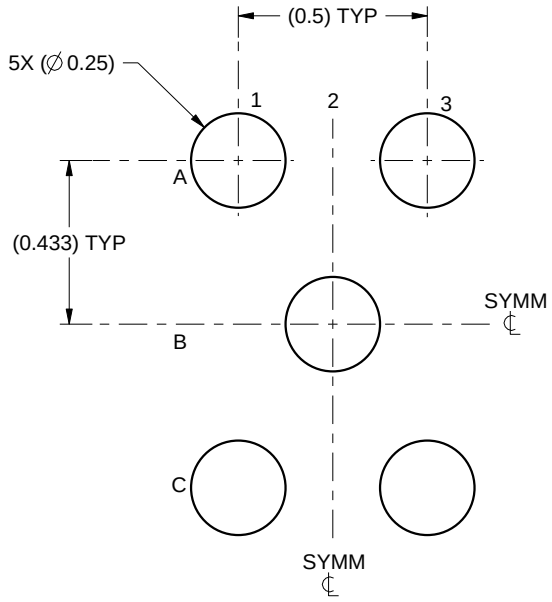
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

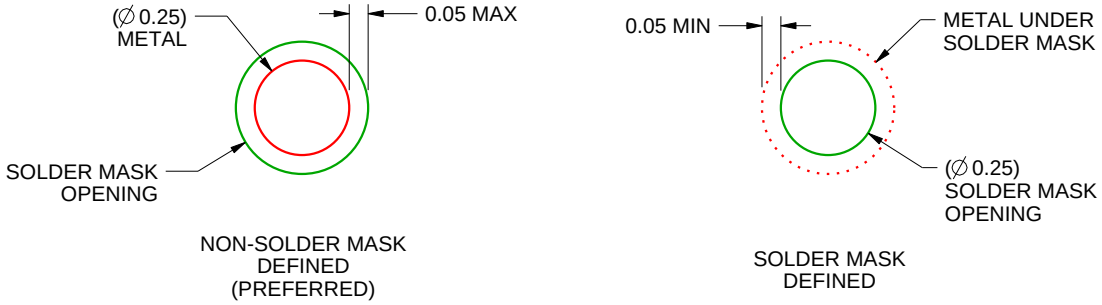
YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4222196/A 11/2015

NOTES: (continued)

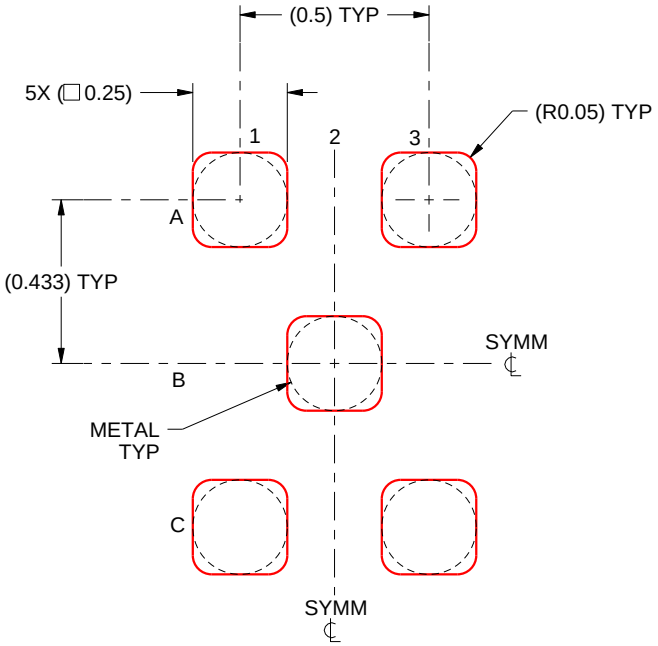
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



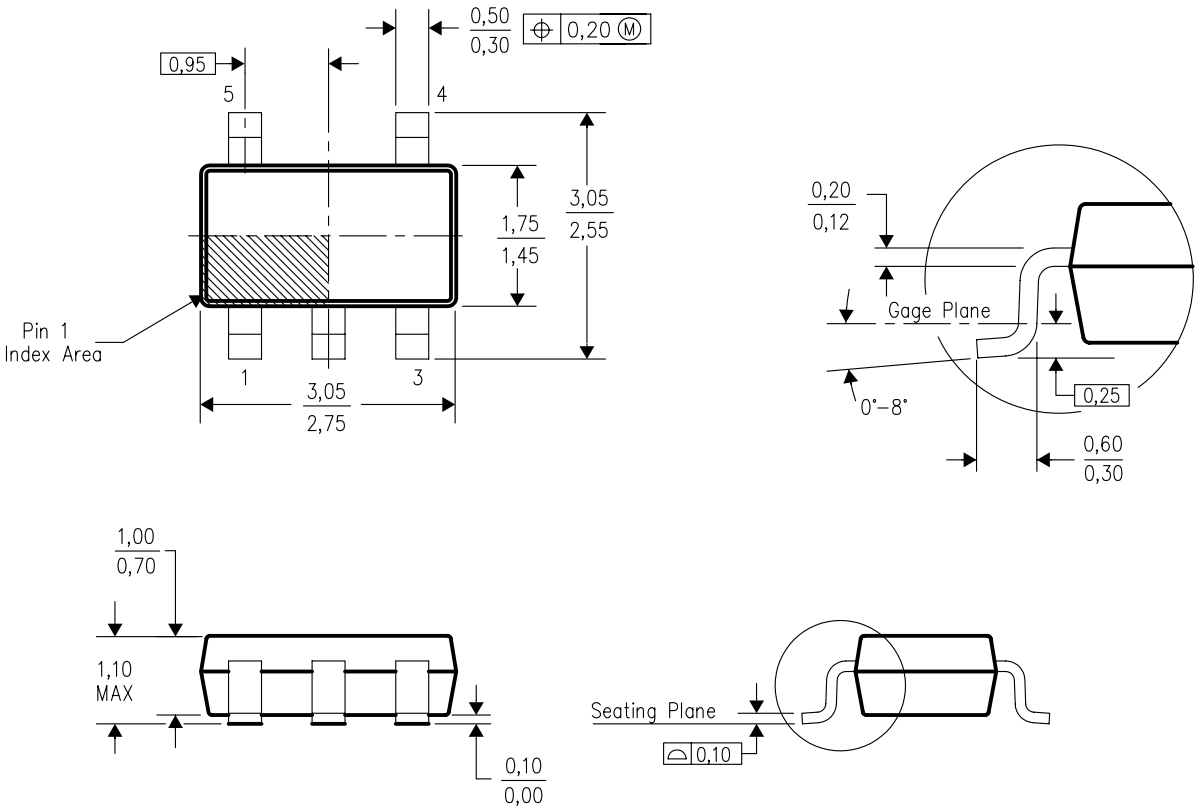
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4222196/A 11/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

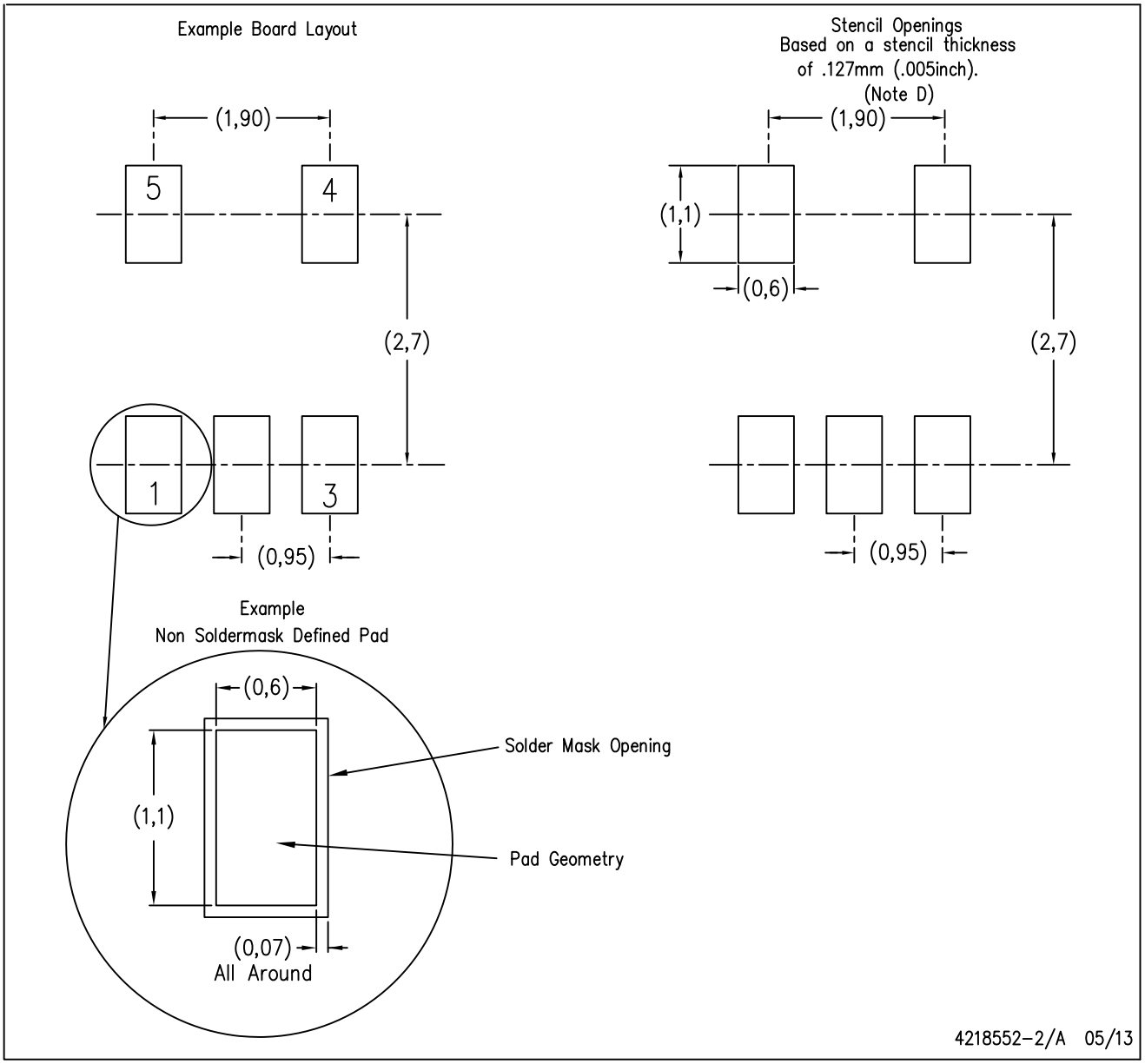
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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