BURR - BROWN®

ADS7845

TOUCH SCREEN CONTROLLER

FEATURES

- 5-WIRE TOUCH SCREEN INTERFACE
- RATIOMETRIC CONVERSION
- SINGLE SUPPLY: 2V to 5V
- UP TO 125kHz CONVERSION RATE
- SERIAL INTERFACE
- PROGRAMMABLE 8- OR 12-BIT RESOLUTION
- AUXILIARY ANALOG INPUTS
- FULL POWER-DOWN CONTROL

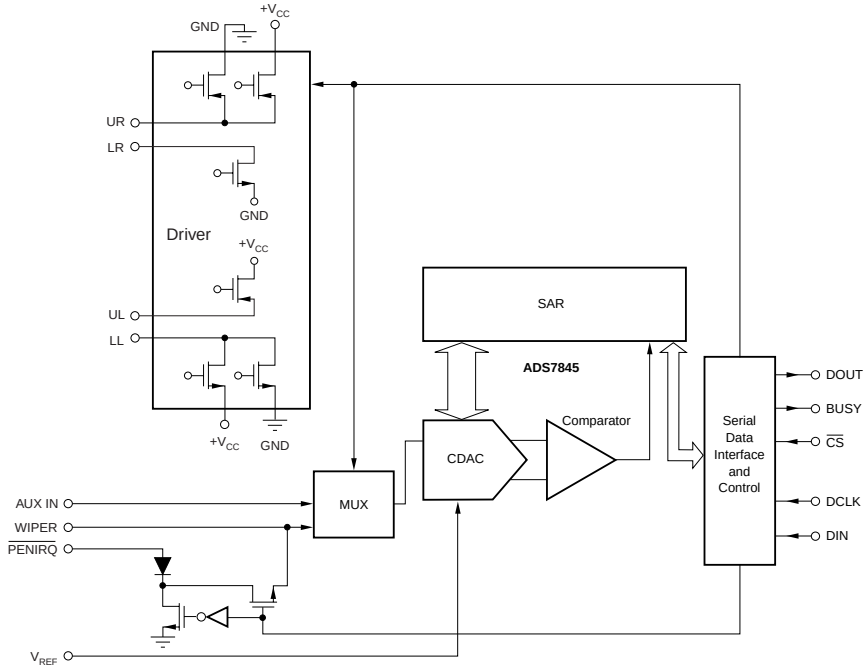
APPLICATIONS

- PERSONAL DIGITAL ASSISTANTS
- PORTABLE INSTRUMENTS
- POINT-OF-SALES TERMINALS
- PAGERS
- TOUCH-SCREEN MONITORS

DESCRIPTION

The ADS7845 is a 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface and low on-resistance switches for driving touch screens. Typical power dissipation is 750µW at a 125kHz throughput rate and a +2.7V supply. The reference voltage (V_{REF}) can be varied between 1V and $+V_{CC}$, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode which reduces typical power dissipation to under 0.5µW. The ADS7845 is guaranteed down to 2.7V operation.

Low power, high speed, and on-board switches make the ADS7845 ideal for battery-operated systems such as personal digital assistants with resistive touch screens and other portable equipment. The ADS7845 is available in a 16-lead SSOP package and is guaranteed over the –40°C to +85°C temperature range.



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SPECIFICATIONS

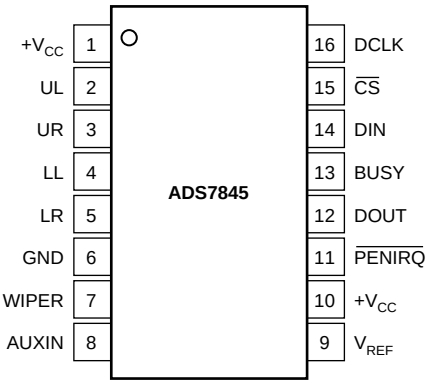
At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, f_{CLK} = 16 • f_{SAMPLE} = 2MHz, 12-bit mode, and digital inputs = GND or $+V_{CC}$, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7845E MIN	ADS7845E TYP	ADS7845E MAX	UNITS
RESOLUTION			12		Bits
ANALOG INPUT					
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	V
	Negative Input	–0.2		+0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB[1]
Offset Error				±6	LSB
Gain Error				±4	LSB
Noise			30		µVrms
Power Supply Rejection Ratio			70		dB
SAMPLING DYNAMICS					
Conversion Time				12	Clk Cycles
Acquisition Time		3			Clk Cycles
Throughput Rate				125	kHz
Multiplexer Settling Time			500		ns
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
SWITCH DRIVERS					
On-Resistance					
UL, UR			7		Ω
LL, LR			7		Ω
REFERENCE INPUT					
Range		1.0		$+V_{CC}$	V
Resistance	$\overline{CS}$ = GND or $+V_{CC}$		5		GΩ
Input Current			13	40	µA
	f_{SAMPLE} = 12.5kHz		2.5		µA
	$\overline{CS}$ = $+V_{CC}$		0.001	3	µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels, Except $\overline{PENIRQ}$					
V_{IH}	| I_{IH} | ≤ +5µA	$+V_{CC}$ • 0.7		$+V_{CC}$ +0.3	
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			V
V_{OL}	I_{OL} = 250µA			0.4	V
$\overline{PENIRQ}$					
V_{OL}	T_A = 0°C to +85°C, 100kΩ Pull-Up			0.8	V
Data Format			Straight Binary		
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$	Specified Performance[2]	2.7		5.5	V
Quiescent Current			280	650	µA
	f_{SAMPLE} = 12.5kHz		220		µA
	Shutdown Mode with			3	µA
	DCLK = DIN = $+V_{CC}$				
Power Dissipation	$+V_{CC}$ = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610µV. (2) ADS7845 will operate down to 2.0V.

PIN CONFIGURATION

Top View SSOP



PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	$+V_{CC}$	Power Supply, 2.0V to 5V.
2	UL	Upper Left Panel Driver (V_{CC} ON/OFF)
3	UR	Upper Right Panel Driver (switch between V_{CC} and GND)
4	LL	Lower Left Panel Driver (switch between GND and V_{CC})
5	LR	Lower Right Panel Driver (GND ON/OFF)
6	GND	Ground
7	WIPER	Panel Input
8	AUXIN	Auxiliary Input
9	V_{REF}	Voltage Reference Input
10	$+V_{CC}$	Power Supply, 2.0V to 5V.
11	$\overline{PENIRQ}$	Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally).
12	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
14	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
15	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
16	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

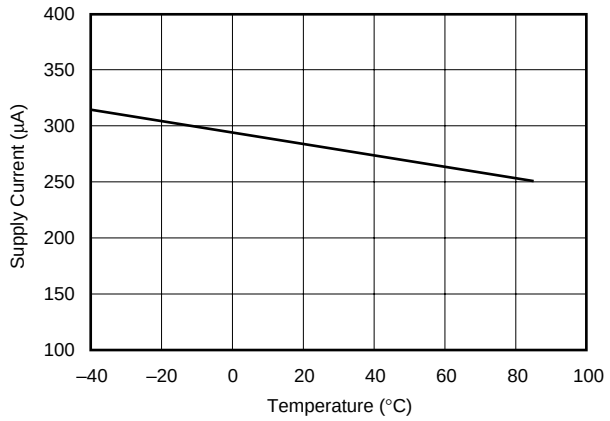
PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER(2)	TRANSPORT MEDIA
ADS7845E	±2	16-Lead SSOP	322	–40°C to +85°C	ADS7845E	Rails
"	"	"	"	"	ADS7845E/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS7845E/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

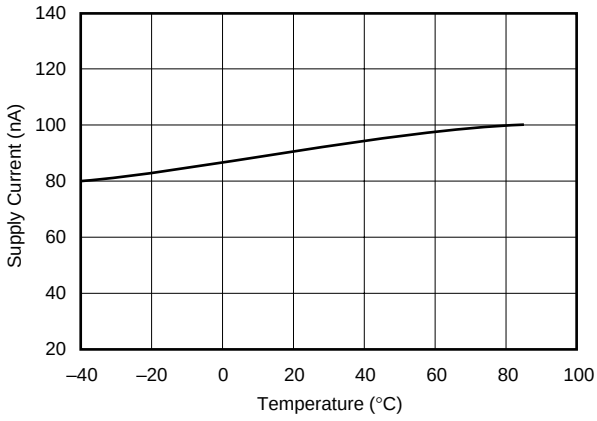
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

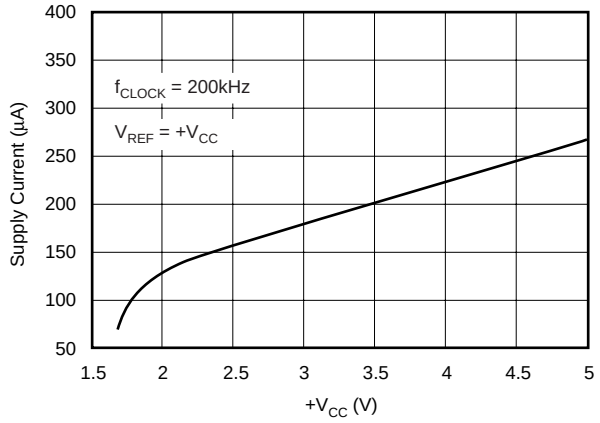
SUPPLY CURRENT vs TEMPERATURE



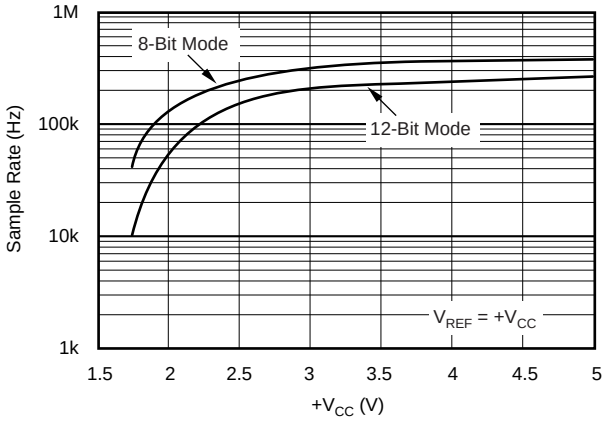
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



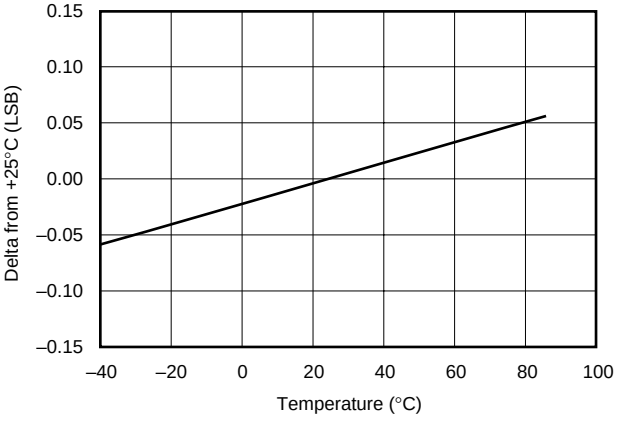
SUPPLY CURRENT vs $+V_{CC}$



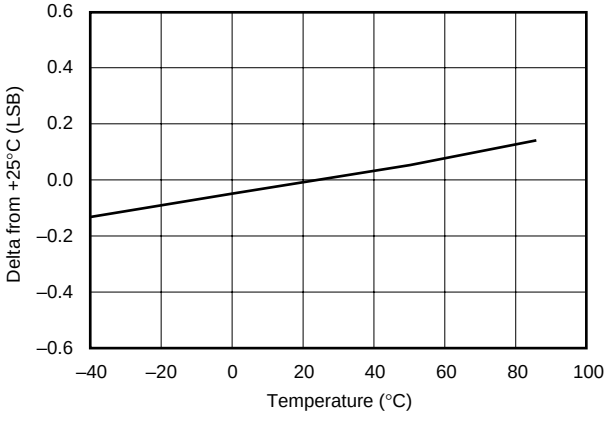
MAXIMUM SAMPLE RATE vs $+V_{CC}$



CHANGE IN GAIN vs TEMPERATURE



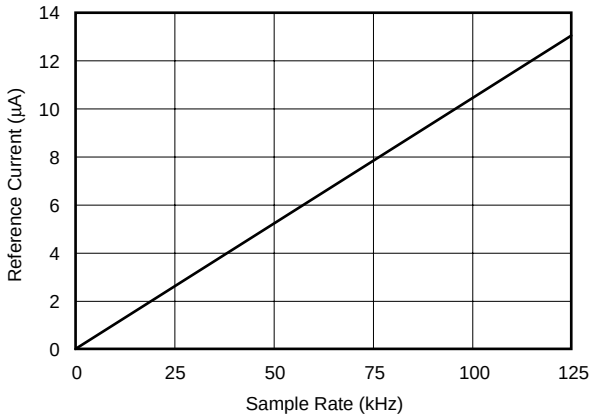
CHANGE IN OFFSET vs TEMPERATURE



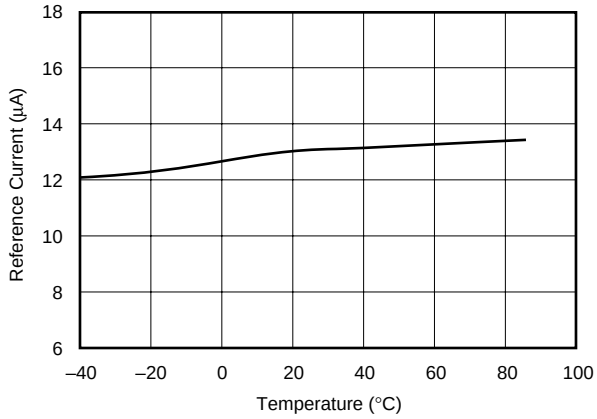
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

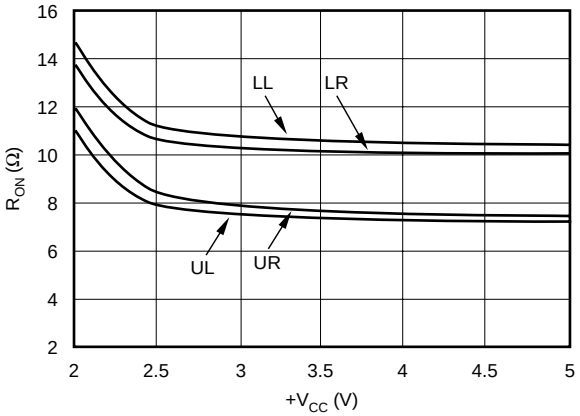
REFERENCE CURRENT vs SAMPLE RATE



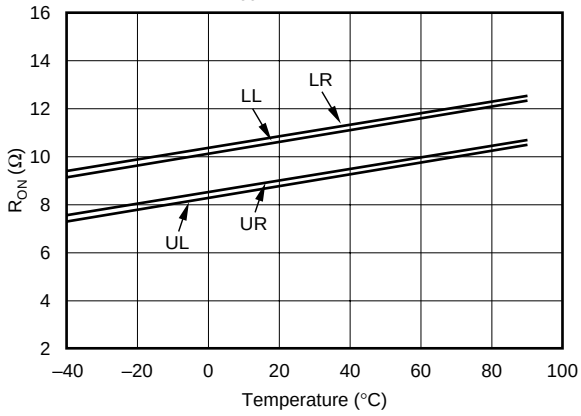
REFERENCE CURRENT vs TEMPERATURE



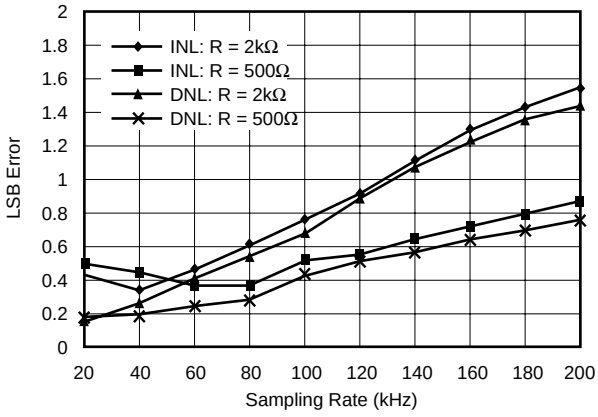
SWITCH ON RESISTANCE vs $+V_{CC}$
($X+$, $Y+$: $+V_{CC}$ to Pin; $X–$, $Y–$: Pin to GND)



SWITCH ON RESISTANCE vs TEMPERATURE
($X+$, $Y+$: $+V_{CC}$ to Pin; $X–$, $Y–$: Pin to GND)



MAXIMUM SAMPLING RATE vs R_{IN}



THEORY OF OPERATION

The ADS7845 is a classic Successive Approximation Register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7845 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.0V to 5.25V. The external reference can be any voltage between 1V and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7845.

The analog input to the converter is provided via the WIPER input. In the measurement mode, the lower right corner of the panel is connected to GND and the upper left corner is connected to V_{CC}. When the lower left corner is connected to GND and the upper right corner is connected to V_{CC}, a "Y" measurement is made. When the lower left corner is connected to V_{CC} and the upper right corner is connected to GND, a "X" measurement is made. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the switch's on-resistance error (should this be a source of error for the particular measurement).

ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the ADS7845, the differential input of the A/D converter, and the converter's differential reference. Table I and Table II show the relationship between the A2, A1, A0, and SER/$\overline{\text{DFR}}$ control bits and the configuration of the ADS7845. The control bits are provided serially via the DIN pin—see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	DRV1	DRV2	AUXIN	INTERRUPT	–IN(1)	X POSITION	Y POSITION	+REF(1)	–REF(1)
0	0	1	ON				GND	OFF	ON	$+V_{REF}$	GND
1	0	1		ON			GND	ON	OFF	$+V_{REF}$	GND
0	1	0			ON		GND	OFF	OFF	$+V_{REF}$	GND
1	1	0				DOUT	GND	OFF	OFF	$+V_{REF}$	GND

NOTE: (1) Internal node, for clarification only—not directly accessible by the user.

TABLE I. Input Configuration—Single-Ended Reference Mode (SER/$\overline{\text{DFR}}$ HIGH).

A2	A1	A0	DRV1	DRV2	AUXIN	INTERRUPT	–IN(1)	X SWITCHES	Y SWITCHES	+REF(1)	–REF(1)
0	0	1	ON				LR	OFF	ON	UL	LR
1	0	1		ON			LR	ON	OFF	UL	LR
0	1	0			ON		GND	OFF	OFF	$+V_{REF}$	GND
1	1	0				DOUT	GND	OFF	OFF	$+V_{REF}$	GND

NOTE: (1) Internal node, for clarification only—not directly accessible by the user.

TABLE II. Input Configuration—Differential Reference Mode (SER/$\overline{\text{DFR}}$ LOW).

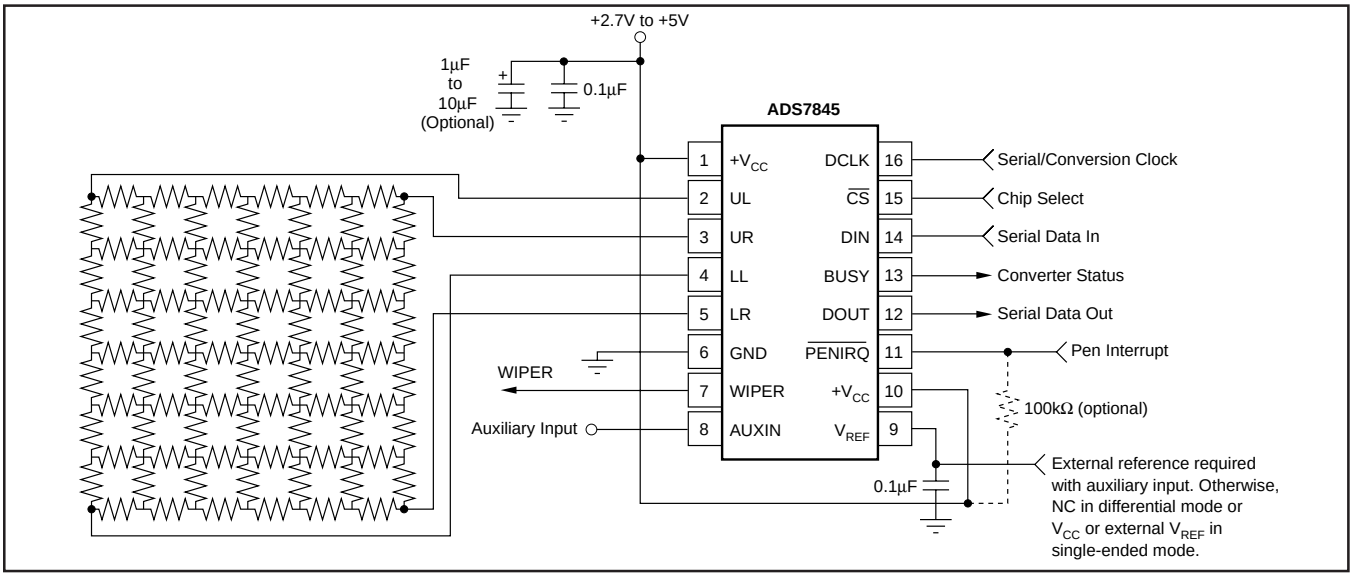


FIGURE 1. Basic Operation of the ADS7845.

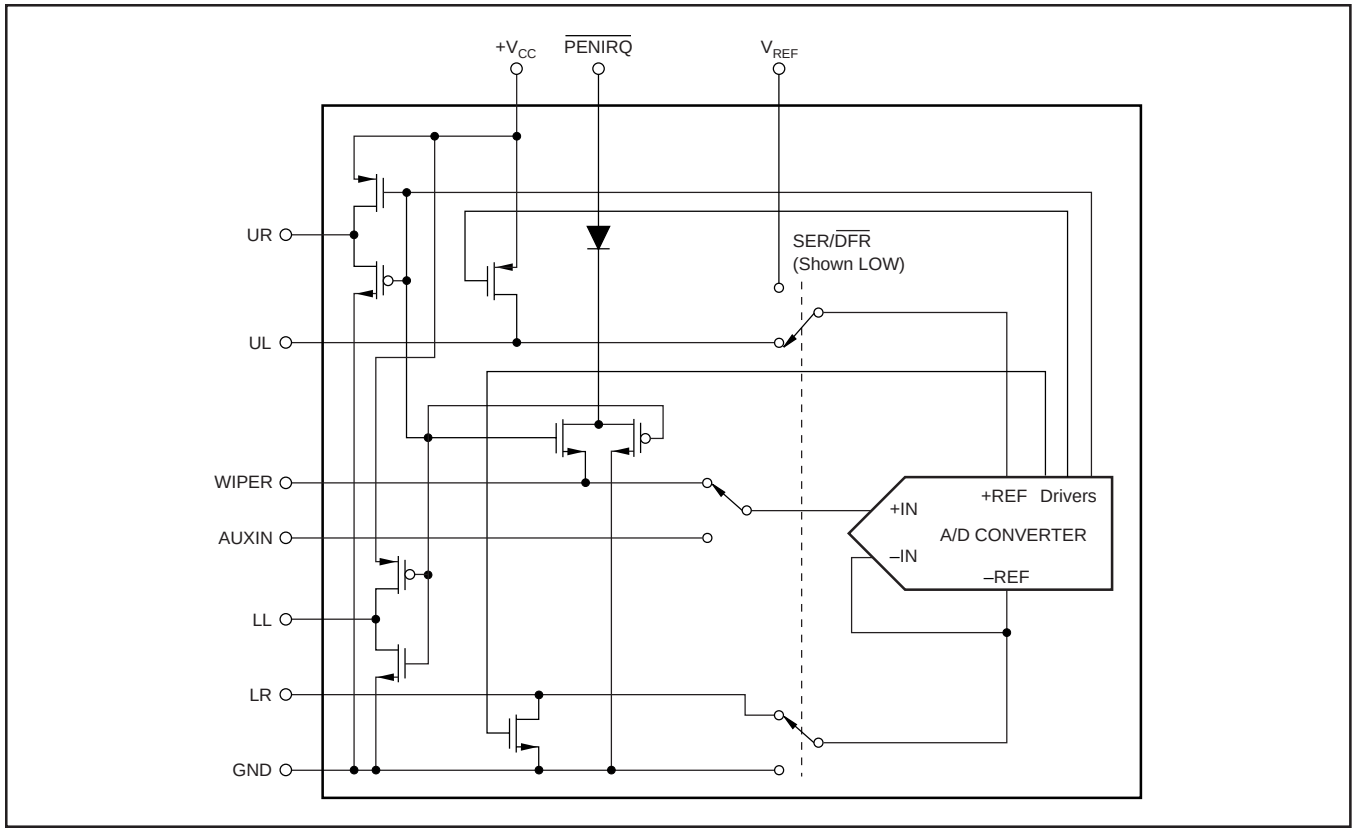


FIGURE 2. Simplified Diagram of ADS7845 Input and Panel Drivers.

REFERENCE INPUT

The voltage difference between +REF and –REF (see Figure 2) sets the analog input range. The ADS7845 will operate with a reference in the range of 1V to $+V_{CC}$. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5V reference, it will typically be 5 LSBs with a 1V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal.

The voltage into the V_{REF} input is not buffered and directly drives the capacitor digital-to-analog converter (CDAC) portion of the ADS7845. Typically, the input current is 13µA with V_{REF} = 2.5V and f_{SAMPLE} = 125kHz. This value will vary by a few microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

There is also a critical item regarding the reference when making measurements where the switch drivers are on. For this discussion, it's useful to consider the basic operation of the ADS7845 as shown in Figure 1. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made with the WIPER input to the A/D converter, turning on the UL and UR drivers to V_{CC}, grounding LL and LR, and digitizing the voltage on the WIPER (see Figure 3 for a block diagram).

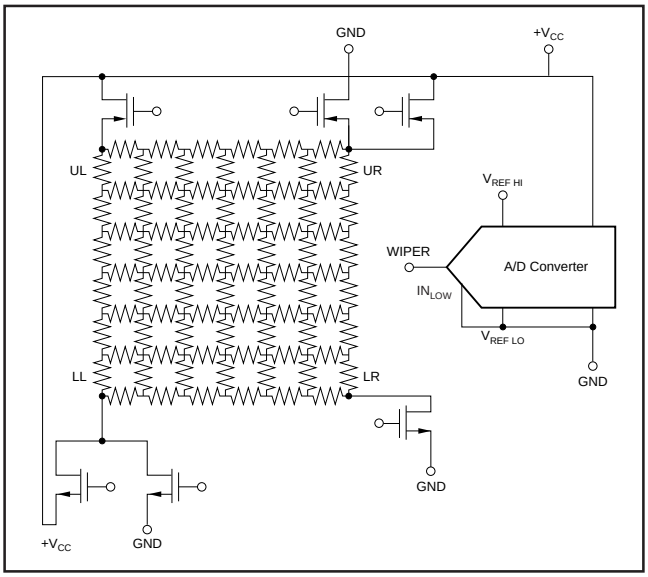


FIGURE 3. Simplified Diagram of Single-Ended Reference (SER/DFR HIGH).

Under the situation outlined so far, it would not be possible to achieve a zero volt input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

This situation can be remedied as shown in Figure 4. By setting the SER/$\overline{\text{DFR}}$ bit LOW, the +REF and –REF inputs are connected directly to Y+ and Y–. This makes the analog-to-digital conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. NOTE: There is an important consideration regarding power dissipation when using the ratiometric mode of operation. See the Power Dissipation section for more details.

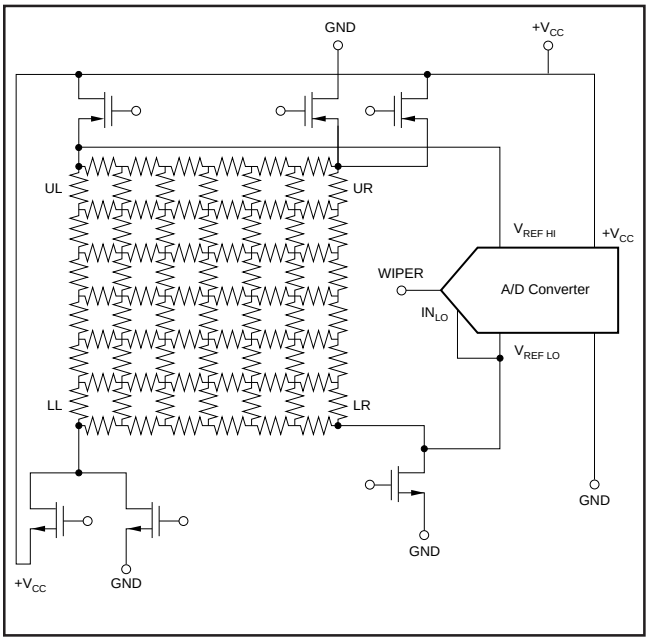


FIGURE 4. Simplified Diagram of Differential Reference (SER/$\overline{\text{DFR}}$ LOW).

As a final note about the differential reference mode, it must be used with $+V_{CC}$ as the source of the +REF voltage and cannot be used with V_{REF}. It is possible to use a high precision reference on V_{REF} and single-ended reference mode for measurements which do not need to be ratiometric. Or, in some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the ADS7845, but they might not be able to supply enough current for the external load (such as a resistive touch screen).

DIGITAL INTERFACE

Figure 5 shows the typical operation of the ADS7845's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter consists of 8 clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first 8 clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer, switches, and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the internal switches are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample/hold goes into the hold mode and the internal switches may turn off. The next 12 clock cycles accomplish the actual analog-to-digital conversion. If the conversion is ratiometric (SER/$\overline{\text{DFR}}$ LOW), the internal switches are on during the conversion. A 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

Control Byte

Also shown in Figure 5 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7845 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2 - A0) select the active panel drivers (see Tables I and II and Figure 2). The MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SER/$\overline{\text{DFR}}$ bit controls the reference mode: either single-ended (HIGH) or differential (LOW). (The differential mode is also referred to as the ratiometric conversion mode.) In

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

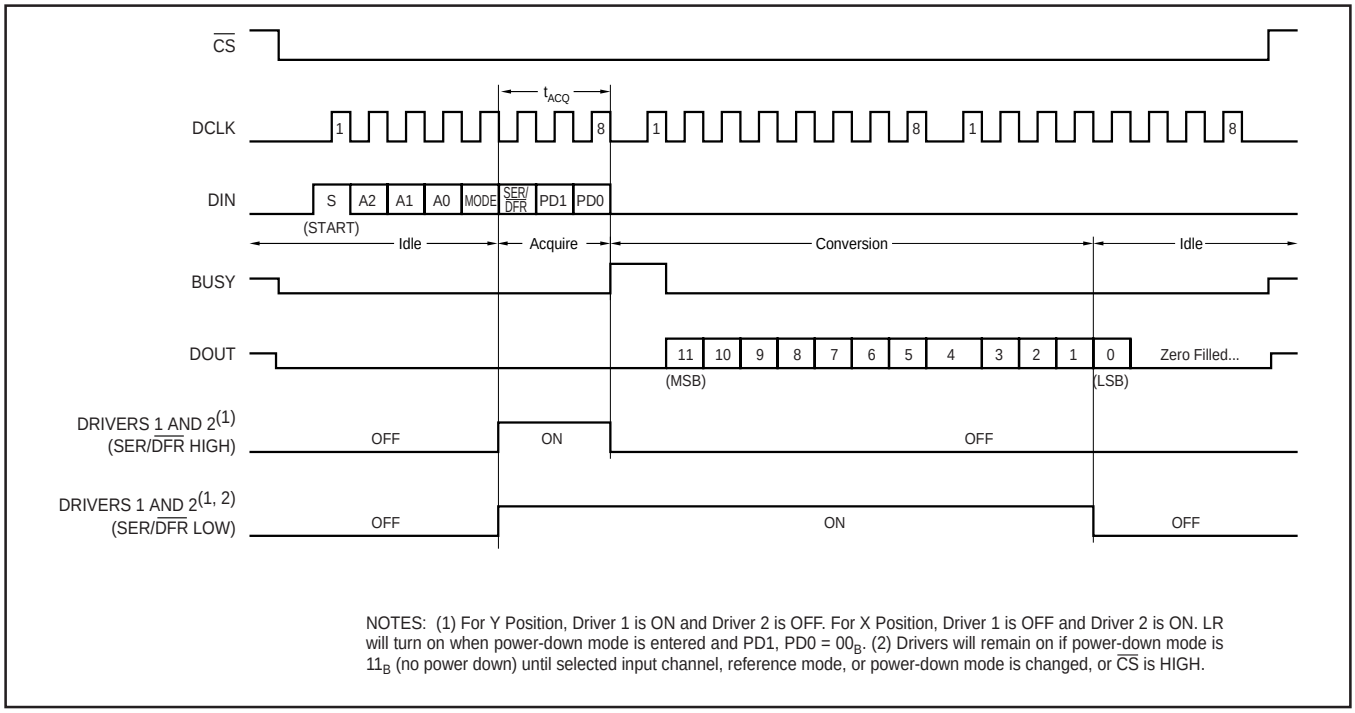
BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6 - 4	A2 - A0	Channel Select Bits. Along with the SER/$\overline{\text{DFR}}$ bit, these bits control the setting of the multiplexer input, switches, and reference inputs, as detailed in Tables I and II.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the number of bits for the following conversion: 12 bits (LOW) or 8 bits (HIGH).
2	SER/$\overline{\text{DFR}}$	Single-Ended/Differential Reference Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input, switches, and reference inputs, as detailed in Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

single-ended mode, the converter's reference voltage is always the difference between the V_{REF} and GND pins. In differential mode, the reference voltage is the difference between the currently enabled switches. See Tables I and II and Figures 2 through 4 for more information. The last two bits (PD1 - PD0) select the power- down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid. There are two power-down modes: one where $\overline{\text{PENIRQ}}$ is disabled and one where it is enabled.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-down between conversions. When each conversion is finished, the converter enters a LOW power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. The LR– switch is on while in power-down.
0	1	Disabled	Same as mode 00, except $\overline{\text{PENIRQ}}$ is disabled. The LR– switch is off while in power-down mode.
1	0	Disabled	Reserved for future use.
1	1	Disabled	No power down between conversions, device is always powered.

TABLE V. Power-Down Selection.



NOTES: (1) For Y Position, Driver 1 is ON and Driver 2 is OFF. For X Position, Driver 1 is OFF and Driver 2 is ON. LR will turn on when power-down mode is entered and PD1, PD0 = 00_B. (2) Drivers will remain on if power-down mode is 11_B (no power down) until selected input channel, reference mode, or power-down mode is changed, or $\overline{\text{CS}}$ is HIGH.

FIGURE 5. Conversion Timing, 24 Clocks per Conversion, 8-Bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

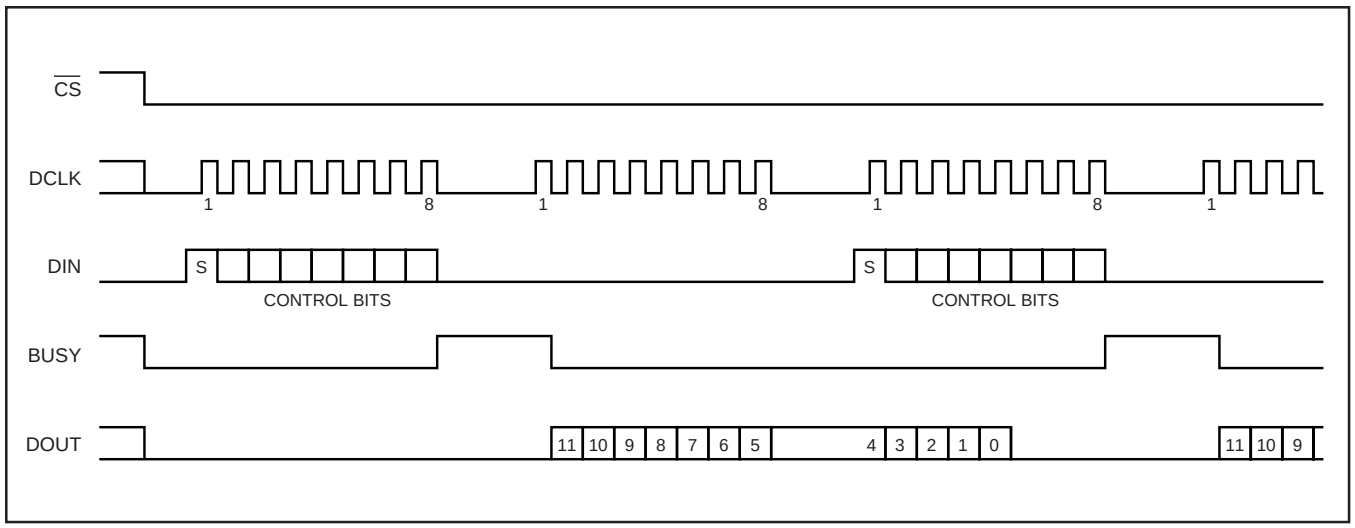


FIGURE 6. Conversion Timing, 16 Clocks per Conversion, 8-Bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

16 Clocks per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 6. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample/hold may droop enough to affect the conversion result. Note that the ADS7845 is fully powered while other serial communications are taking place during a conversion.

Digital Timing

Figure 7 and Table VI provide detailed timing for the digital interface of the ADS7845.

15 Clocks per Conversion

Figure 8 provides the fastest way to clock the ADS7845. This method will not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated Circuits (ASICs). This effectively increases the maximum conversion rate of the converter beyond the values given in the Specification table, which assume 16 clock cycles per conversion.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V and Above, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

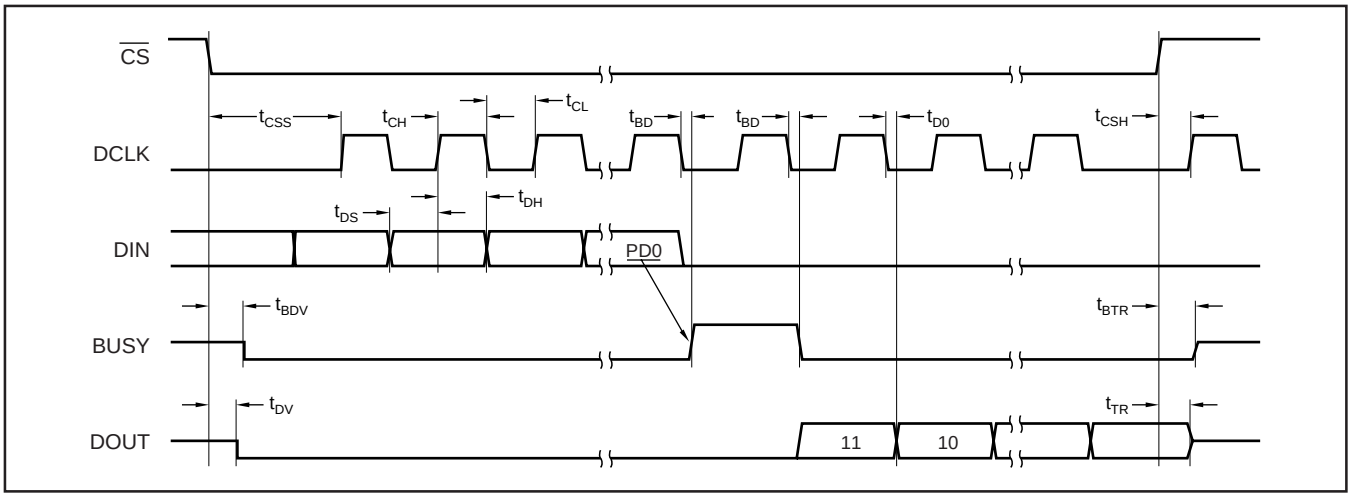


FIGURE 7. Detailed Timing Diagram.

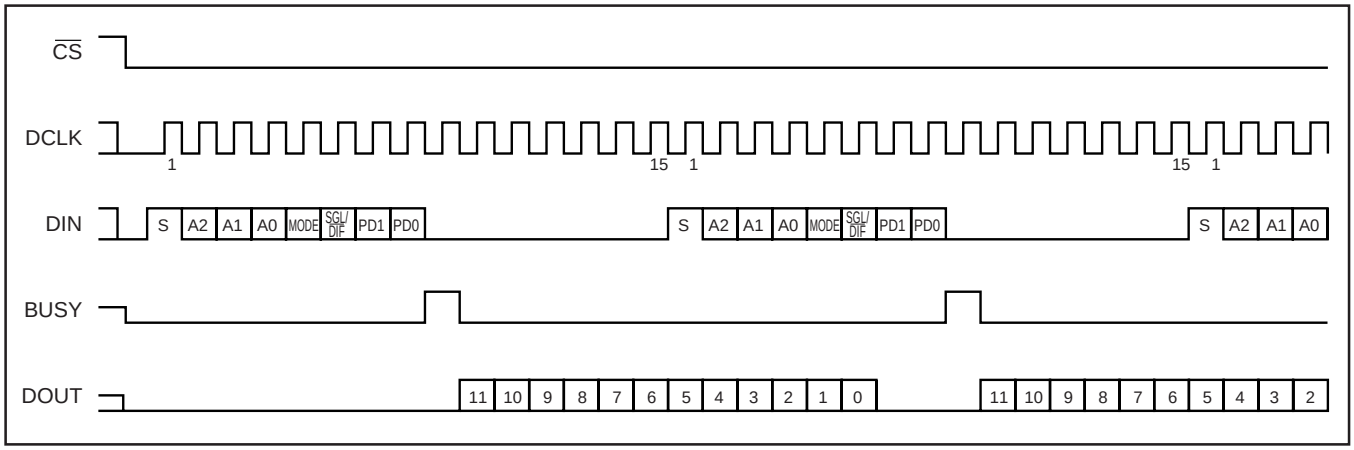
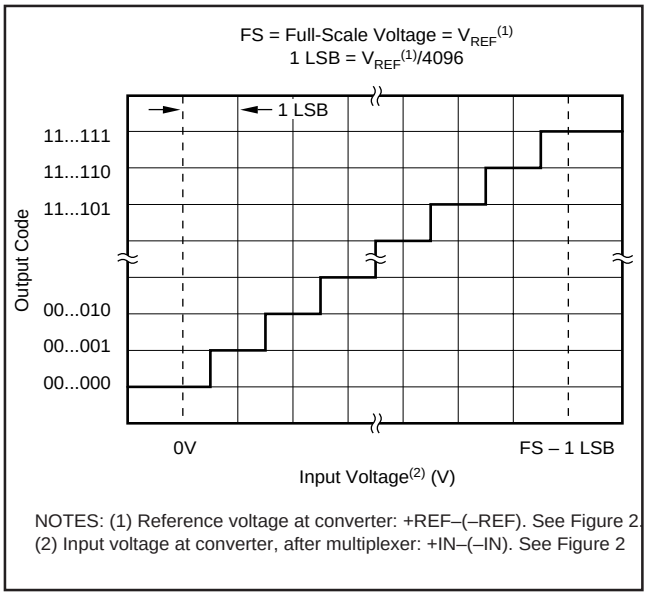


FIGURE 8. Maximum Conversion Rate, 15 Clocks per Conversion.

Data Format

The ADS7845 output data is in Straight Binary format as shown in Figure 9. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF–(–REF). See Figure 2.
(2) Input voltage at converter, after multiplexer: +IN–(–IN). See Figure 2

FIGURE 9. Ideal Input Voltages and Output Codes.

8-Bit Conversion

The ADS7845 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide 12-bit transfers or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7845 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

POWER DISSIPATION

There are two major power modes for the ADS7845: full power (PD1 - PD0 = 11_B) and auto power-down (PD1 - PD0 = 00_B). When operating at full speed and 16-clocks per conversion (as shown in Figure 6), the ADS7845 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are simply done less often, the difference between the two modes is dramatic.

Figure 10 shows the difference between reducing the DCLK frequency (“scaling” DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

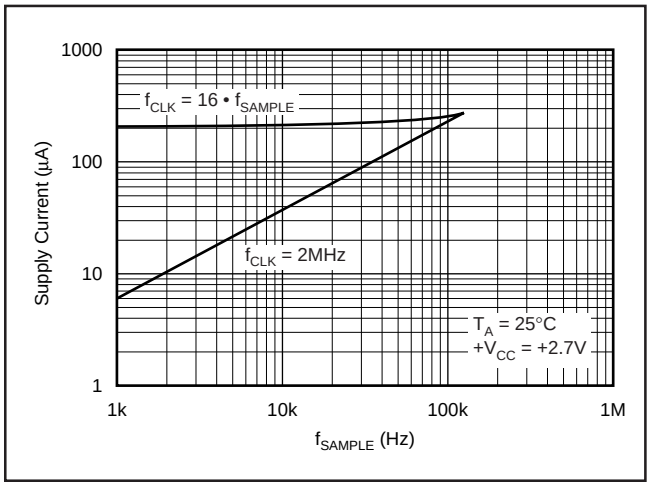


FIGURE 10. Supply Current vs Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the converter’s internal switches are on only when the analog input voltage is being acquired (see Figure 5). Thus, the external device, such as a resistive touch screen, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 5). If the conversion rate is high, this could substantially increase power dissipation.

LAYOUT

The following layout suggestions should provide the most optimum performance from the ADS7845. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly “clean” power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter’s power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the ADS7845 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an ‘n-bit’ SAR converter, there are n ‘windows’ in which

large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7845 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{CC}$ and the power supply is high.

The reference should be similarly bypassed with a 0.1µF capacitor. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation. The ADS7845 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7845 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry or battery connection point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections will be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

PENIRQ Output

The pen interrupt output function is detailed in Figure 11. By connecting a pull-up resistor to V_{CC} (typically 100kΩ), the $\overline{\text{PENIRQ}}$ output is HIGH. While in the power-down mode, with PD0 = PD1 = 0, the lower-right panel corner is connected to GND and the $\overline{\text{PENIRQ}}$ output is connected to the WIPER input. When the panel is touched, the $\overline{\text{PENIRQ}}$ output goes LOW, due to the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycles for X and Y position, the $\overline{\text{PENIRQ}}$ output diode will be internally connected to GND and the WIPER disconnected from the $\overline{\text{PENIRQ}}$ diode to eliminate any leakage current from the pull-up resistor to flow through the WIPER, thus causing no errors.

In addition, when the DIN has selected A2 = 1, A1 = 1, A0 = 0, and the ADS7845 is commanded into the power-down mode (PD0 and PD1 = 0) and $\overline{\text{CS}}$ is LOW (when $\overline{\text{CS}}$ is HI, the DOUT line is high impedance), the DOUT will be LOW (all "0"s) during no touch and HI (all "1"s) when the panel is touched. This feature eliminates the need for an additional port to detect panel touch. Since all panels have end resistance, all "0"s and all "1"s are an unused set of codes.

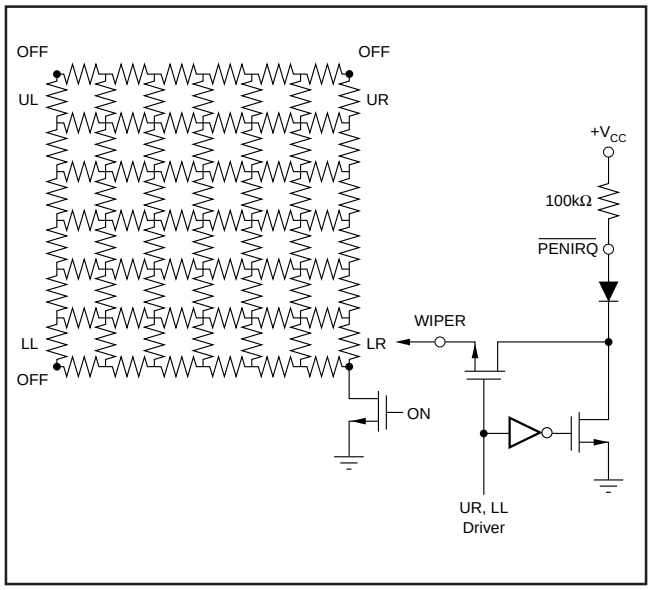


FIGURE 11. $\overline{\text{PENIRQ}}$ Functional Block Diagram.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7845E	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7845E	Samples
ADS7845E/2K5	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7845E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

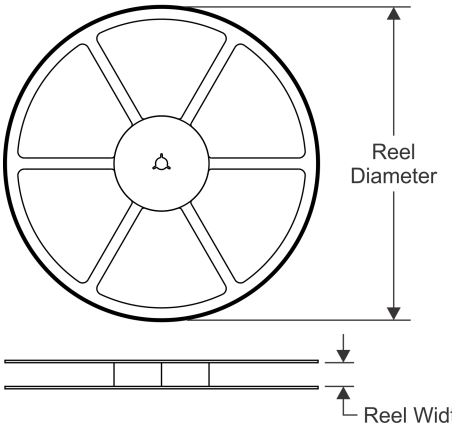
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

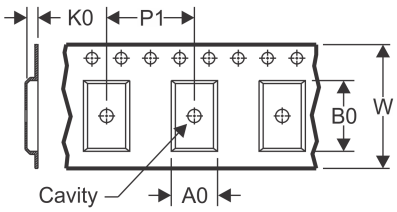
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

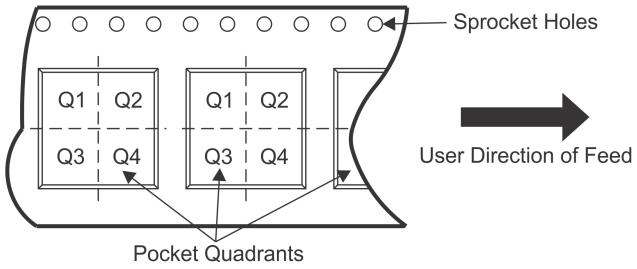


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

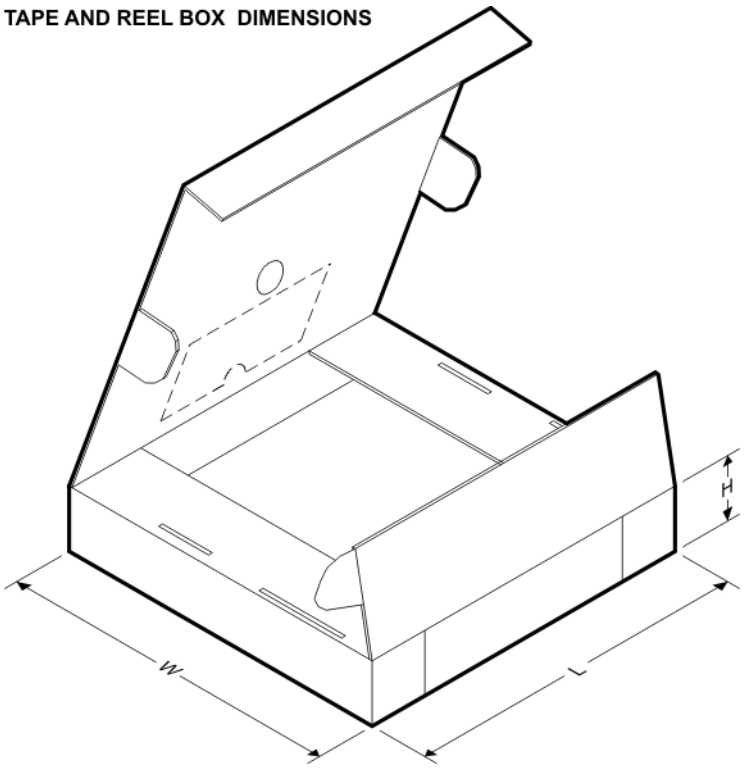
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7845E/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

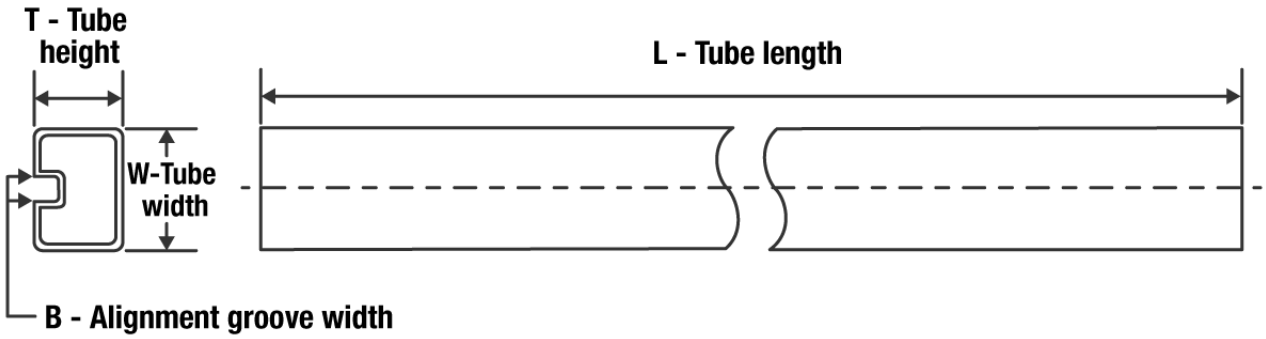
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7845E/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS7845E	DBQ	SSOP	16	75	506.6	8	3940	4.32

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