LM5060 High-Side Protection Controller With Low Quiescent Current

1 Features

- Available in Automotive Grade / AEC Q-100
- Wide operating input voltage range: 5.5 V to 65 V
- Functional safety capable
  - Documentation available to aid functional safety system design
- Less than 15-µA quiescent current in disabled mode
- Controlled output rise time for safe connection of capacitive loads
- Charge pump gate driver for external N-Channel MOSFET
- Adjustable Undervoltage Lockout (UVLO) with hysteresis
- UVLO Serves as second enable input for systems requiring safety redundancy
- Programmable fault detection delay time
- MOSFET latched off after load fault is detected
- Active low open drain POWER GOOD (nPGD) output
- Adjustable input Overvoltage Protection (OVP)
- Immediate restart after overvoltage shutdown
- 10-Lead VSSOP

2 Applications

- Automotive body electronics
- Industrial power distribution and control

3 Description

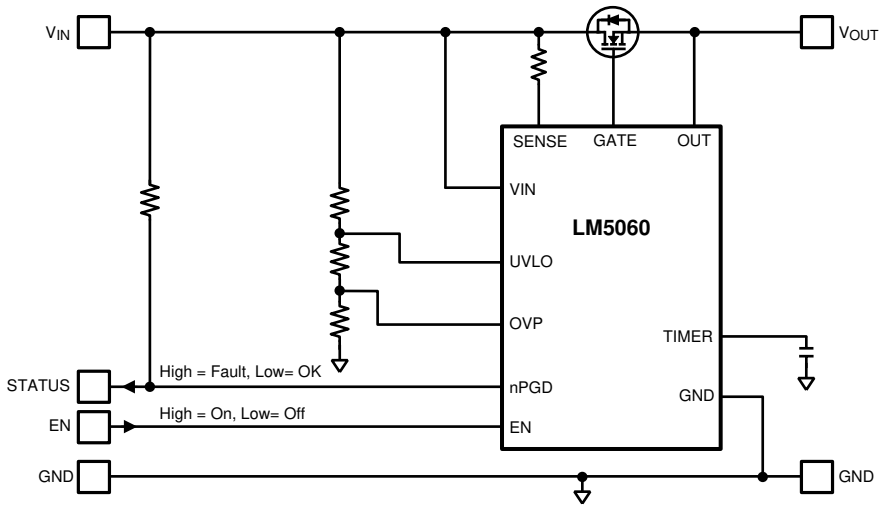
The LM5060 high-side protection controller provides intelligent control of a high-side N-channel MOSFET during normal on/off transitions and fault conditions. In-rush current is controlled by the nearly constant rise time of the output voltage. A POWER GOOD output indicates when the output voltage reaches the input voltage and the MOSFET is fully on. Input UVLO (with hysteresis) is provided as well as programmable input OVP. An enable input provides remote on or off control. The programmable UVLO input can be used as second enable input for safety redundancy. A single capacitor programs the initial start-up V_{GS} fault detection delay time, the transition V_{DS} fault detection delay time, and the continuous over-current V_{DS} fault detection delay time. When a detected fault condition persists longer than the allowed fault delay time, the MOSFET is latched off until either the enable input or the UVLO input is toggled low and then high.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5060	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2016) to Revision H — **Page**

- Added Functional safety capable link to the *Features* section ... 1
- Changed the GATE to GND Absolute Maximum from 75 V to 79 V ... 4
- Added GATE to GND to the *Recommended Operating Conditions* table ... 4

Changes from Revision F (April 2013) to Revision G — **Page**

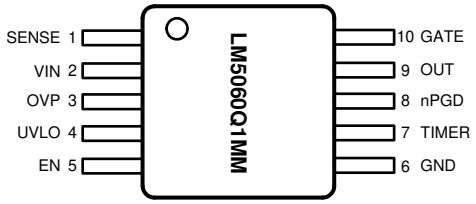
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (April 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 27

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SENSE	I	Input voltage sense: a constant current sink (16 μA typical) at the SENSE pin flows through an external resistor to set the threshold for fault detection.
2	VIN	P	Supply voltage input: the operating voltage range is 5.5 V to 65 V. The internal power-on-reset (POR) circuit typically switches to the active state when the VIN pin is greater than 5.1 V. A small ceramic bypass capacitor close to this pin is recommended to suppress noise.
3	OVP	I	Over-voltage protection comparator input: an external resistor divider from the system input voltage sets the Over-Voltage turn-off threshold. The GATE pin is pulled low when OVP exceeds the typical 2.0-V threshold, but the controller is not latched off. Normal operation resumes when the OVP pin falls below typically 1.76 V.
4	UVLO	I	Under-voltage lock-out comparator input: the UVLO pin is used as an input under-voltage lock-out by connecting this pin to a resistor divider between input supply voltage and ground. The UVLO comparator is activated when EN is high. A voltage greater than typically 1.6 V at the UVLO pin will release the pull down devices on the GATE pin and allow the output to gradually rise. A constant current sink (5.5 μA typical) is provided to ensure the UVLO pin is low in an open circuit condition.
5	EN	I	Enable input: a voltage less than 0.8 V on the EN pin switches the LM5060 to a low current shutdown state. A voltage greater than 2.0 V on the EN pin enables the internal bias circuitry and the UVLO comparator. The GATE pin pull-up bias is enabled when both EN and UVLO are in the high state. A constant current sink (6 μA typical) is provided to ensure the EN pin is low in an open circuit condition.
6	GND	–	Circuit ground
7	TIMER	I/O	Timing capacitor: an external capacitor connected to this pin sets the V_{DS} fault detection delay time. If the TIMER pin exceeds the 2.0-V threshold condition, the LM5060 will latch off the MOSFET and remain off until either the EN, UVLO or VIN (POR) input is toggled low and then high.
8	nPGD	O	Fault status: an open drain output. When the external MOSFET V_{DS} decreases such that the OUT pin voltage exceeds the SENSE pin voltage, the nPGD indicator is active (low = no fault).
9	OUT	I	Output voltage sense: connect to the output rail (external MOSFET source). Internally used to detect V_{DS} and V_{GS} conditions.
10	GATE	O	Gate drive output: connect to the external MOSFET's gate. A charge-pump driven constant current source (24 μA typical) charges the GATE pin. An internal zener clamps the GATE pin at typically 16.8 V above the OUT pin. The $\Delta V/\Delta t$ of the output voltage can be reduced by connecting a capacitor from the GATE pin to ground.

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} to GND(3)(4)	–0.3	75	V
SENSE, OUT to GND(5)	–0.3	75	V
GATE to GND(3)(5)	–0.3	79	V
EN, UVLO to GND(4)	–0.3	75	V
nPGD, OVP to GND	–0.3	75	V
TIMER to GND	–0.3	7	V
Peak reflow temperature		260	°C
Operating junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The Absolute Maximum Rating for VIN (75 V) applies only when the LM5060 is disabled.
(4) The minimum voltage of –1 V is allowed if the current is limited to below –25 mA. Also it is assumed that the negative voltage on the pins only occur during reverse battery condition when a positive supply voltage (Vin) is not applied.
(5) The minimum voltage of –25 V is allowed if the current is limited to below –25 mA. Also it is assumed that the negative voltage on the pins only occur during reverse battery condition when a positive supply voltage (VIN) is not applied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply voltage	5.5		65	V
EN	Enable voltage	0		65	V
GATE to GND		0		79	V
UVLO	Undervoltage lock-out voltage	0		65	V
nPGD	POWER GOOD off voltage	0		65	V
	POWER GOOD sink current	0		5	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM5060 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Unless otherwise stated the following conditions apply: VIN = 14 V, EN = 2.00 V, UVLO = 2.00 V, OVP = 1.50 V, and T_J = 25°C. Limits in standard type are for T_J = 25°C except where noted. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIN PIN							
I_{IN-EN}	Input current, enabled mode		T_J = 25°C		1.4		mA
			T_J = –40°C to 125°C			1.7	
I_{IN-DIS}	Input current, disabled mode	EN = 0.50 V	T_J = 25°C		9		µA
			T_J = –40°C to 125°C			15	
I_{IN-STB}	Input current, standby mode	UVLO = 0.00 V	T_J = 25°C		0.56		mA
			T_J = –40°C to 125°C			0.80	
POR_{EN}	Power on reset threshold at VIN	VIN rising	T_J = 25°C		5.1		V
			T_J = –40°C to 125°C			5.46	
POR_{EN-HYS}	POR_{EN} hysteresis	VIN falling			500		mV
OUT PIN							
I_{OUT-EN}	OUT pin bias current, enabled	OUT = VIN, normal operation	T_J = 25°C		8		µA
			T_J = –40°C to 125°C	5.0		11.0	
$I_{OUT-DIS}$	OUT pin leakage current, disabled[1]	Disabled, OUT = 0 V, SENSE = VIN			0		µA
SENSE PIN							
I_{SENSE}	Threshold programming current	SENSE pin bias current	T_J = 25°C		16		µA
			T_J = –40°C to 125°C	13.6		18.0	
V_{OFFSET}	V_{DS} comparator offset voltage	SENSE - OUT voltage for fault detection	T_J = 25°C		0		mV
			T_J = –40°C to 125°C	–7.0		7.0	
I_{RATIO}	I_{SENSE} and I_{OUT-EN} current ratio	I_{SENSE} / I_{OUT-EN}	T_J = 25°C		2.0		
			T_J = –40°C to 125°C	1.70		2.30	

(1) The GATE pin voltage is typically 12 V above the VIN pin when the LM5060 is enabled. Therefore, the Absolute Maximum Rating for VIN (75 V) applies only when the LM5060 is disabled, or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is also 75 V.

Electrical Characteristics (continued)

Unless otherwise stated the following conditions apply: VIN = 14 V, EN = 2.00 V, UVLO = 2.00 V, OVP = 1.50 V, and T_J = 25°C. Limits in standard type are for T_J = 25°C except where noted. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OVP INPUT							
OVP_{TH}	OVP threshold	OVP pin threshold voltage rising	T_J = 25°C		2.0		V
			T_J = –40°C to 125°C	1.88		2.12	
OVP_{HYS}	OVP hysteresis				240		mV
OVP_{DEL}	OVP delay time	Delay from OVP pin > OVP_{TH} to GATE low			9.6		µs
OVP_{BIAS}	OVP pin bias current	OVP = 1.9 V	T_J = 25°C		0		µA
			T_J = –40°C to 125°C			0.50	
UVLO INPUT							
$UVLO_{TH}$	UVLO threshold	UVLO pin threshold voltage rising	T_J = 25°C		1.6		V
			T_J = –40°C to 125°C	1.45		1.75	
$UVLO_{HYS}$	UVLO hysteresis		T_J = 25°C		180		mV
			T_J = –40°C to 125°C	120		230	
$UVLO_{BIAS}$	UVLO pin pull-down current		T_J = 25°C		5.5		µA
			T_J = –40°C to 125°C	3.8		7.2	
EN INPUT							
EN_{THH}	High-level input voltage		T_J = –40°C to 125°C	2.00			V
EN_{THL}	Low-level input voltage		T_J = –40°C to 125°C			0.80	V
EN_{HYS}	EN threshold hysteresis				200		mV
EN_{BIAS}	EN pin pull-down current		T_J = 25°C		6		µA
			T_J = –40°C to 125°C			8.0	
GATE CONTROL (GATE PIN)							
I_{GATE}	Gate charge (sourcing) current, on state	On-state	T_J = 25°C		24		µA
			T_J = –40°C to 125°C	17		31	
$I_{GATE-OFF}$	Gate discharge (sinking) current, off state	UVLO = 0.00 V			2.2		mA
$I_{GATE-FLT}$	Gate discharge (sinking) current, fault state	OUT < SENSE			80		mA
V_{GATE}	Gate output voltage in normal operation	GATE - VIN voltage GATE pin open	T_J = 25°C		12		V
			T_J = –40°C to 125°C	10		14	
$V_{GATE-TH}$	V_{GS} status comparator threshold voltage	GATE - OUT threshold voltage for TIMER voltage reset and TIMER current change	T_J = 25°C		5		V
			T_J = –40°C to 125°C	3.50		6.50	
$V_{GATE-CLAMP}$	Zener clamp between GATE pin and OUT pin	$I_{GATE-CLAMP}$ = 0.1 mA			16.8		V

Electrical Characteristics (continued)

Unless otherwise stated the following conditions apply: VIN = 14 V, EN = 2.00 V, UVLO = 2.00 V, OVP = 1.50 V, and T_J = 25°C. Limits in standard type are for T_J = 25°C except where noted. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TIMER (TIMER PIN)							
V_{TMRH}	Timer fault threshold	TIMER pin voltage rising			2.0		V
V_{TMRL}	Timer re-enable threshold	TIMER pin voltage falling			0.30		V
I_{TIMERH}	Timer charge current for V_{DS} fault	TIMER charge current after start-up V_{GS} = 6.5 V	T_J = 25°C		11		µA
			T_J = –40°C to 125°C	8.5		13.0	
I_{TIMERL}	Timer start-up charge current	TIMER charge current during start-up V_{GS} = 3.5 V	T_J = 25°C		6		µA
			T_J = –40°C to 125°C	4.0		7.0	
I_{TIMERR}	Timer reset discharge current	TIMER pin = 1.5 V	T_J = 25°C		6		mA
			T_J = –40°C to 125°C	4.4		8.2	
t_{FAULT}	Fault to GATE low delay	TIMER pin > 2.0 V No load on GATE pin			5		µs
POWER GOOD (nPGD PIN)							
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA	T_J = 25°C		80		mV
			T_J = –40°C to 125°C			205	
PGD_{IOH}	Off leakage current	V_{nPGD} = 10 V	T_J = 25°C		0.02		µA
			T_J = –40°C to 125°C			1.00	

6.6 Typical Characteristics

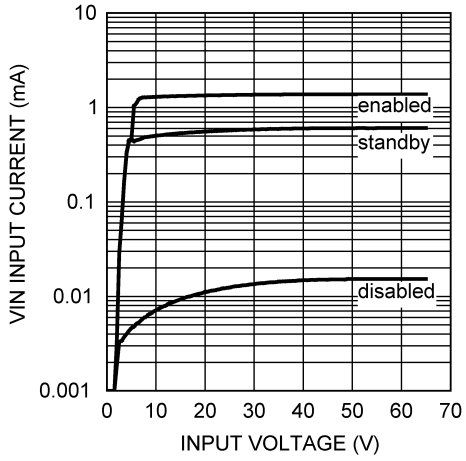


Figure 1. VIN Pin Current vs VIN Pin Voltage

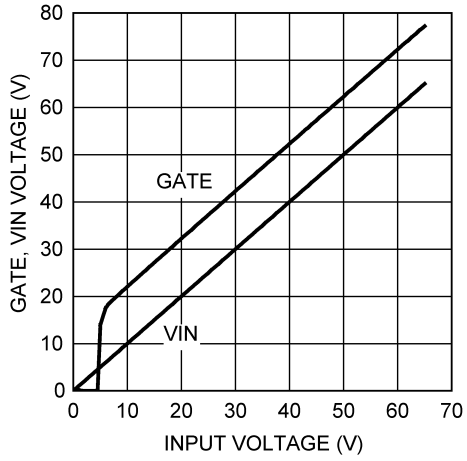


Figure 2. V_{GATE}, VIN Voltage vs Input Voltage

Typical Characteristics (continued)

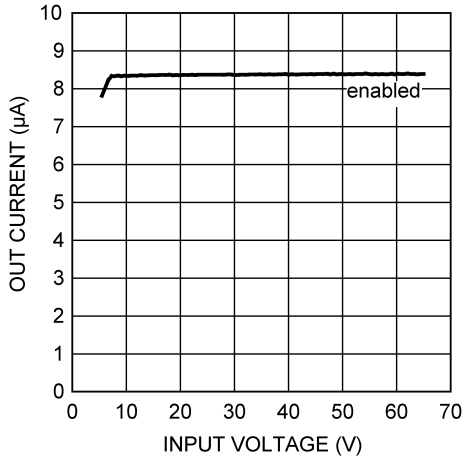


Figure 3. OUT Pin Current (I_{OUT-EN}) vs VIN Voltage

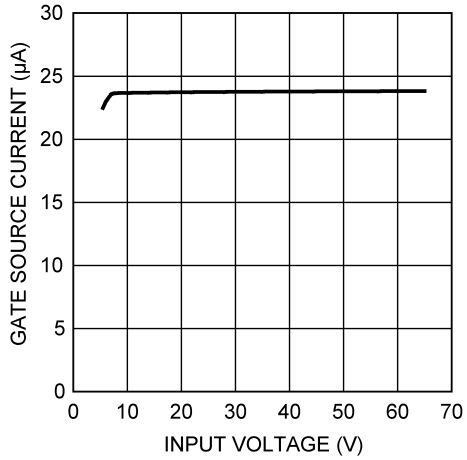


Figure 4. GATE Current (I_{GATE}) vs VIN Voltage

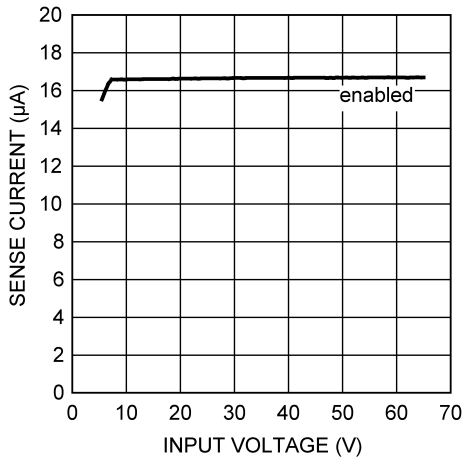


Figure 5. SENSE Current (I_{SENSE}) vs VIN Voltage

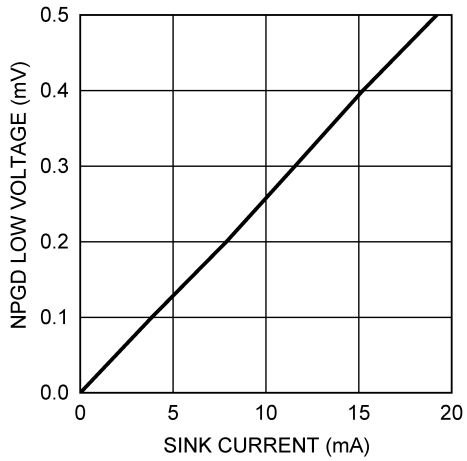


Figure 6. nPGD Low Voltage (PGD_{VOL} vs Sink Current)

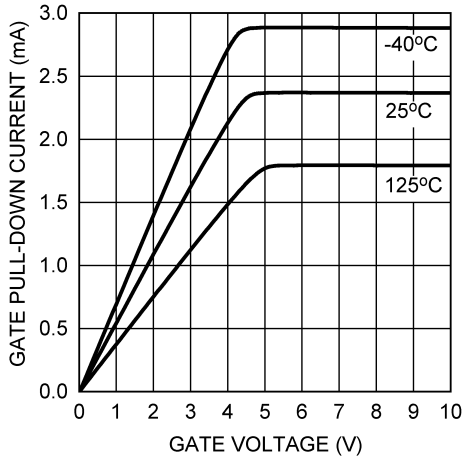


Figure 7. GATE Pull-Down Current Off ($I_{GATE-OFF}$) vs GATE Voltage

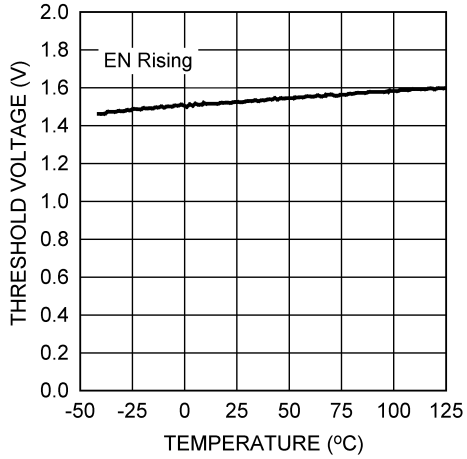


Figure 8. EN Threshold Voltage (EN_{TH}) vs Temperature

Typical Characteristics (continued)

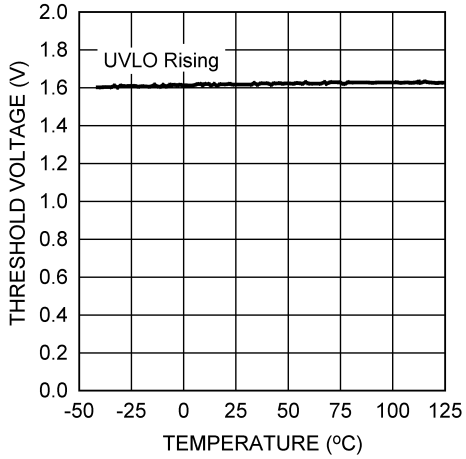


Figure 9. UVLO Threshold Voltage ($UVLO_{TH}$) vs Temperature

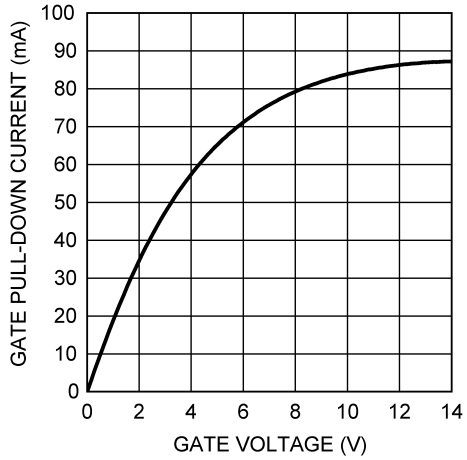


Figure 10. GATE Pull-Down Current Fault ($I_{GATE-FLT}$) vs GATE Voltage

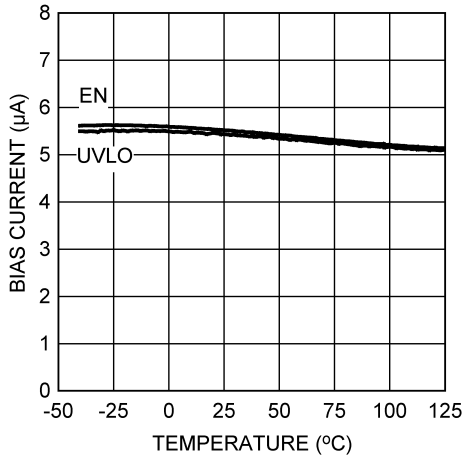


Figure 11. UVLO, EN Current vs Temperature

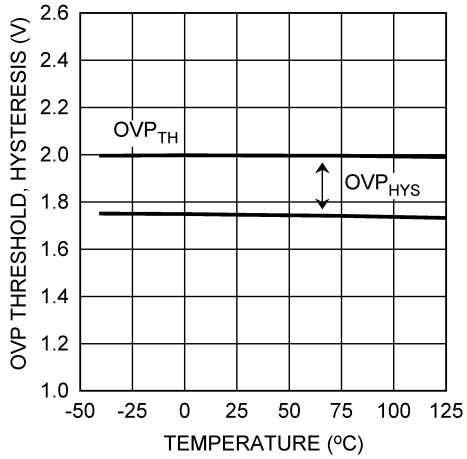


Figure 12. OVP Threshold (OVP_{TH}), Hysteresis (OVP_{HYS}) vs Temperature

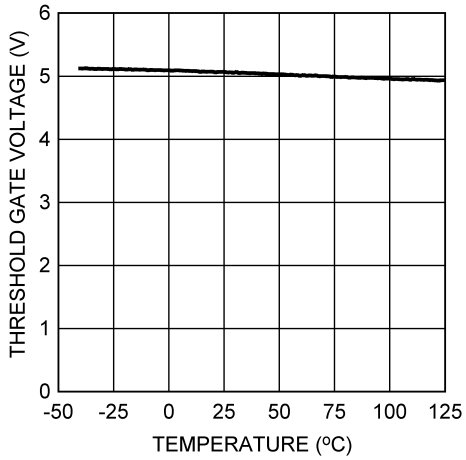


Figure 13. V_{GS} Comparator Threshold Voltage ($V_{GATE-TH}$) vs Temperature

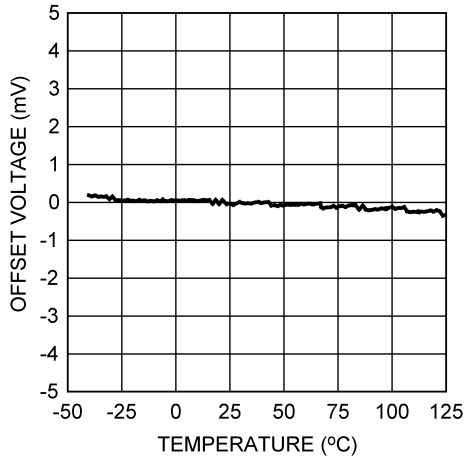


Figure 14. V_{DS} Comparator Offset Voltage (V_{OFFSET}) vs Temperature

Typical Characteristics (continued)

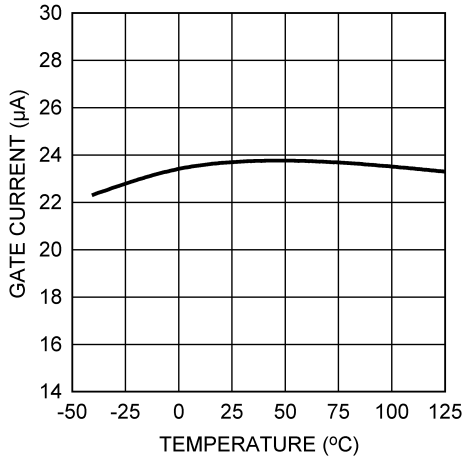


Figure 15. GATE Current (I_{GATE}) vs Temperature

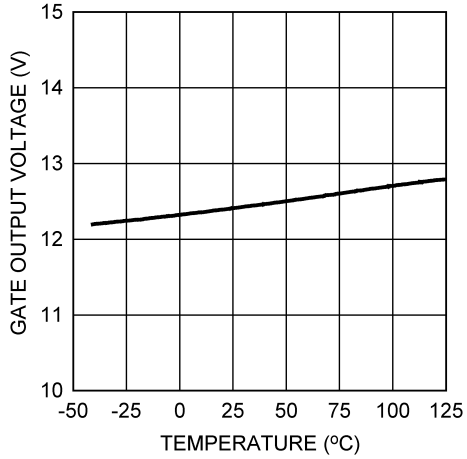


Figure 16. GATE Output Voltage (V_{GATE}) vs Temperature

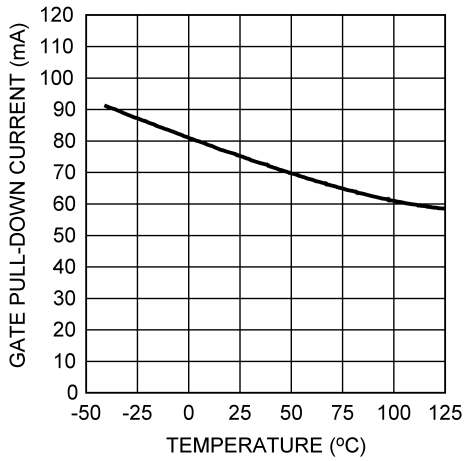


Figure 17. Gate Pull-Down Current - Fault ($I_{GATE-FLT}$) vs Temperature

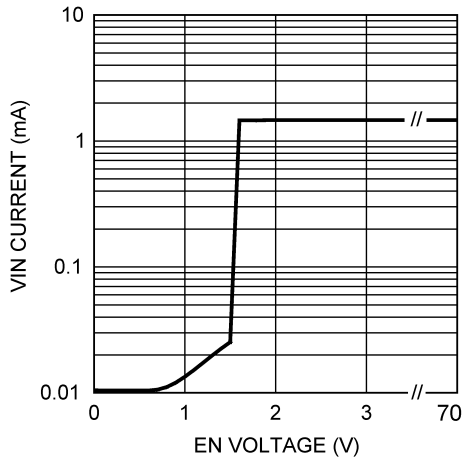


Figure 18. VIN Pin Current (I_{EN}) vs EN Voltage

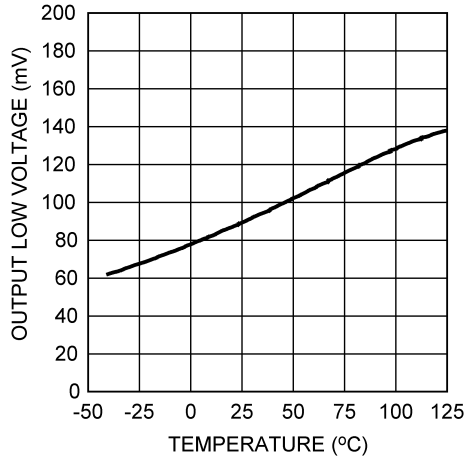


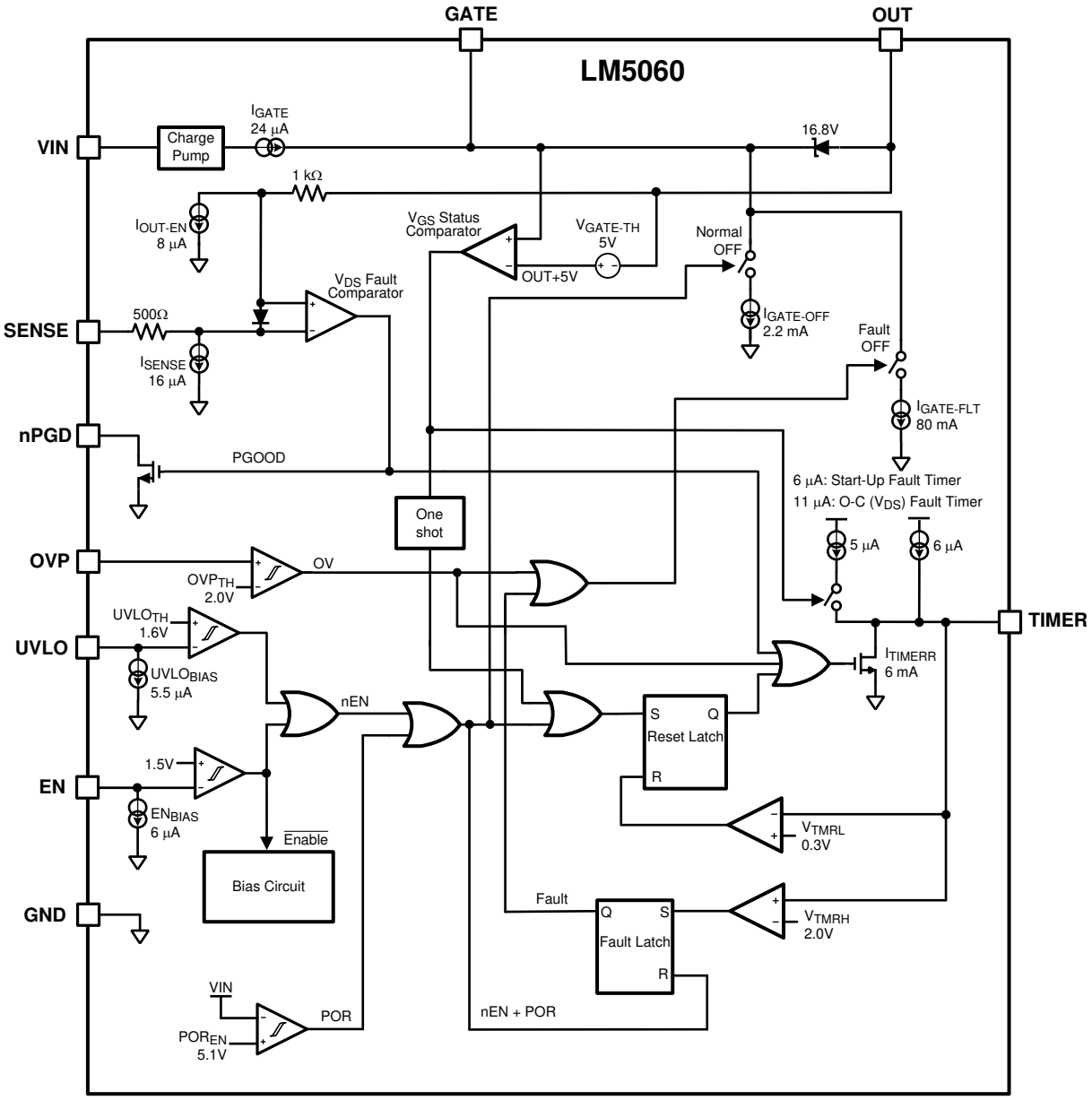
Figure 19. nPGD Low Voltage (PGD_{VOL}) vs Temperature

7 Detailed Description

7.1 Overview

The LM5060 high-side protection controller features programmable current limit, turn on voltage, fault timer, and overvoltage protection. It also has an enable input and POWER GOOD output.

7.2 Functional Block Diagram



7.3 Feature Description

The LM5060 is designed to drive an external high-side N-channel MOSFET. Over-Current protection is implemented by sensing the voltage drop across the MOSFET. When an adjustable voltage drop threshold is exceeded, and an adjustable time period has elapsed, the MOSFET is disabled. OVP and UVLO monitoring of the input line is also provided. A low state on the enable pin will turn off the N-channel MOSFET and switch the LM5060 into a very low quiescent current off state. An active low POWER GOOD output pin is provided to report the status of the N-channel MOSFET. The waiting time before the MOSFET is turned off after a fault condition is detected can be adjusted with an external timer capacitor. Since the LM5060 uses a constant current source to charge the gate of the external N-channel MOSFET, the output voltage rise time can be adjusted by adding external gate capacitance. This is useful when starting up into large capacitive loads.

7.4 Device Functional Modes

7.4.1 Power-Up Sequence

The basic application circuit is shown in Figure 20 and a normal start-up sequence is shown in Figure 21. Start-up of the LM5060 is initiated when the EN pin is above the (EN_{THH}) threshold (2.0 V). At start-up, the timer capacitor is charged with a 6-µA (typical) current source while the gate of the external N-channel MOSFET is charged through the GATE pin by a 24-µA (typical) current source.

When the gate-to-source voltage (V_{GS}) reaches the $V_{GATE-TH}$ threshold (typically 5 V) the V_{GS} sequence ends, the timer capacitor is quickly discharged to 0.3 V, and the 5-µA current source is enabled.

The timer capacitor will charge until either the V_{DS} Comparator indicates that the drain-to-source voltage (V_{DS}) has been reduced to a nominal value (i.e. no fault) or the voltage on the timer capacitor has reached the V_{TMRH} threshold (i.e. fault). The V_{DS} Comparator monitors the voltage difference between the SENSE pin and the OUT pin. The SENSE pin voltage is user programmed to be lower than the input supply voltage by selecting a suitable sense resistor value. When the OUT pin voltage exceeds the voltage at the SENSE pin, the nPGD pin is asserted low (i.e. no fault) and the timer capacitor is discharged.

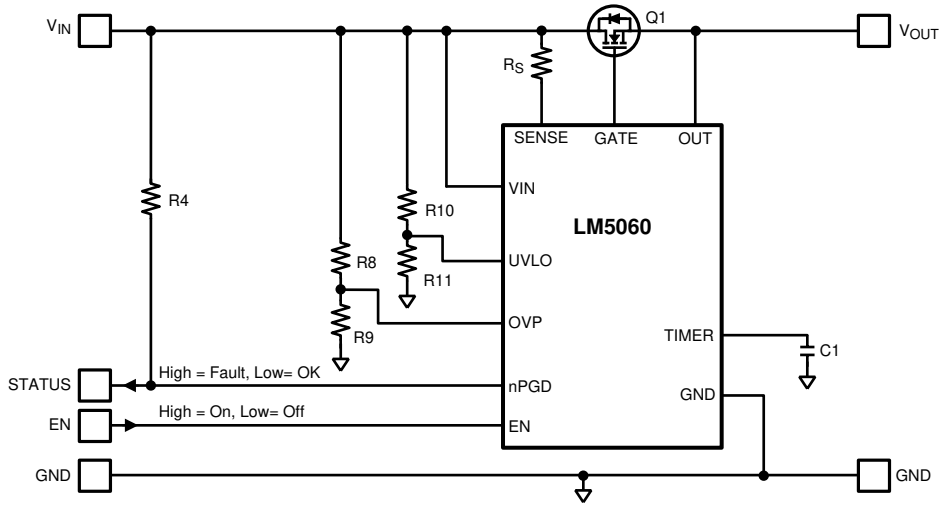


Figure 20. Basic Application Circuit

7.4.2 Status Conditions

Output responses of the LM5060 to various input conditions is shown in Table 1. The input parameters include Enable (EN), UVLO, OVP, input voltage (VIN), Start-Up Fault (V_{GS}) and Run Fault (V_{DS}) conditions. The output responses are the VIN pin current consumption, the GATE charge current, the TIMER capacitor charge (or discharge) current, the GATE discharge current if the timer capacitor voltage has reached the V_{TMRH} threshold (typically 2 V), as well as the status of nPGD.

Device Functional Modes (continued)

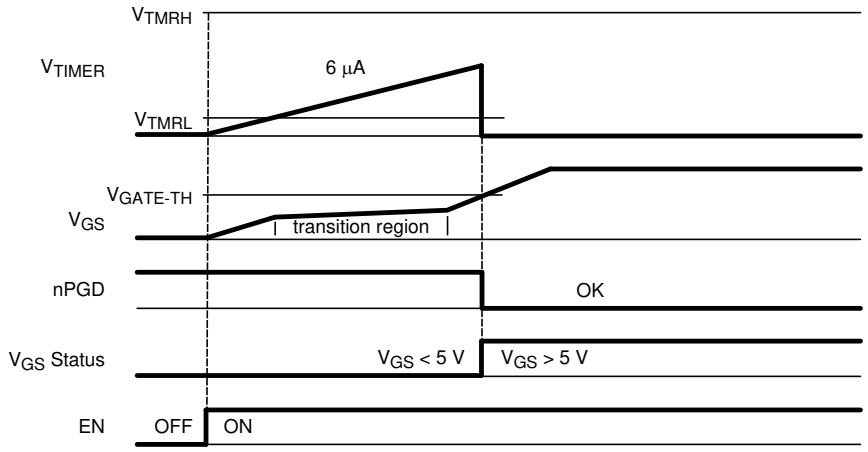


Figure 21. Voltages During Normal Start Up Sequence

Table 1. Overview of Operating Conditions

INPUTS						OUTPUTS					STATUS
EN	UVLO	OVP (typ)	VIN (typ)	SENSE-OUT	GATE -OUT	VIN Current (typ)	GATE Current (typ)	TIMER	GATE after TIMER > 2 V	nPGD	
L	L	–	>5.10 V	–	–	0.009 mA	2.2 mA sink	Low	–	–	Disabled
L	H	–	>5.10 V	–	–	0.009 mA	2.2 mA sink	Low	–	–	Disabled
H	L	<2 V	>5.10 V	SENSE>OUT	–	0.56 mA	2.2 mA sink	Low	–	H	Standby
				SENSE<OUT						L	
H	L	>2 V	>5.10 V	SENSE>OUT	–	0.56 mA	80 mA sink	Low	–	H	Standby
				SENSE<OUT						L	
H	H	<2 V	>5.10 V	SENSE>OUT	<5 V	1.4 mA	24-µA source	6-µA source	80 mA sink	H	Enabled
				SENSE<OUT				Low	–	L	
H	H	<2 V	>5.10 V	SENSE>OUT	>5 V	1.4 mA	24-µA source	11-µA source	80 mA sink	H	Enabled
				SENSE<OUT				Low	–	L	
H	H	>2 V	>5.10 V	SENSE>OUT	–	1.4 mA	80 mA sink	Low	–	H	Over-voltage
				SENSE<OUT						L	
H	H	<2 V	<5.10 V	–	–	1.4 mA	2.2 mA sink (see (1))	Low	–	H	Power on reset

(1) The 2.2 mA sink current is valid for with the VIN pin ≥ 5.1 V. When the VIN pin < 5.1 V the sink current is lower. See 'GATE Pin Off Current vs. VIN' plot in *Typical Characteristics*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Gate Control

A charge pump provides bias voltage above the input and output voltage to enhance the N-channel MOSFET gate. When the system voltage is initially applied and both EN and UVLO are above their respective thresholds, the GATE pin is charged by the 24-µA (typical) current source. During normal operating conditions, the GATE pin voltage is clamped to approximately 16.8 V above the OUT pin (i.e. V_{GS}) by an internal zener.

When either the UVLO input or the EN input is low, or when VIN is below the Power-On Reset voltage of 5.10 V (typical), the GATE pin is discharged with a 2.2 mA (typical) current sink.

When the timer capacitor is charged up to the V_{TMRH} threshold (typically 2 V) a fault condition is indicated and the gate of the external N-Channel MOSFET is discharged at a 80 mA (typical) rate. Additionally, when the OVP pin voltage is higher than the OVP_{TH} threshold (typically 2 V) a fault is indicated and the gate of the external N-Channel MOSFET is discharged at the same 80 mA (typical) rate.

8.1.2 Fault Timer

An external capacitor connected from the TIMER pin to the GND pin sets the fault detection delay time. If the voltage on the TIMER capacitor reaches the V_{TMRH} threshold (2 V typical) a fault condition is indicated. The LM5060 will latch off the MOSFET by discharging the GATE pin at a 80 mA (typical) rate, and will remain latched off until either the EN pin, the UVLO pin, or the VIN pin is toggled low and then high.

There are three relevant components to the TIMER pin's function:

1. A constant 6-µA (typical) current source driving the TIMER pin. This current source is active when EN, UVLO, and VIN are all high.
2. A second current source (5 µA typical) is activated, for a total charge current of 11 µA (typical), only when the V_{GS} sequence has completed successfully.
3. A pull-down current sink for the TIMER pin which resets the timer by discharging the timer capacitor. If EN, UVLO or VIN is low, or when OVP is high, the timer capacitor is discharged.
    a. When the V_{DS} Fault Comparator detects a fault, (SENSE pin voltage higher than OUT pin voltage) the timer capacitor pull down is disabled and the timer capacitor is allowed to charge at the 11-µA (typical) rate.

During Start-Up, the timer behaves as follows:

After applying sufficient system voltage and enabling the LM5060 by pulling the EN and UVLO pins high, the timer capacitor will be charged with a 6-µA (typical) current source. The timer capacitor is discharged when the voltage difference between the GATE pin and the OUT pin (i.e. V_{GS} of the external N-Channel MOSFET) reaches the $V_{GATE-TH}$ threshold (typically 5 V). After discharging, the timer capacitor is charged with 11 µA until either the V_{TMRH} threshold (typically 2 V) is reached, or the sensed V_{DS} voltage falls below the threshold of the V_{DS} Fault Comparator, indicating the output voltage has reached the desired steady state level. The timer capacitor voltage waveforms are illustrated in Figure 21, Figure 22, and Figure 23.

A timer capacitor is always necessary to allow some finite amount of time for the gate to charge and the output voltage to rise during startup. If an adequate timer capacitor value is not used, then the 6 µA of charge current would cause the TIMER pin voltage to reach the V_{TMRH} fault threshold (typically 2 V) prematurely and the LM5060 will latch off since a fault condition would have been indicated.

Application Information (continued)

Although not recommended, the timer function can be disabled by connecting the TIMER pin directly to GND. With this condition the TIMER pin voltage will never reach the V_{TMRH} fault threshold (2 V typical). The end result is that the fault latch-off protection is completely disabled, while the nPGD pin will continue to reflect the V_{DS} Fault Comparator output.

8.1.3 V_{GS} Considerations

The V_{GS} Status Comparator accomplishes two purposes:

1. As the gate of the external MOSFET is charged, the V_{GS} voltage transitions from cut-off, through an active region, and into the ohmic region. The LM5060 provides two fault timer modes to monitor these transitions. The TIMER pin capacitor is initially charged with a constant 6 µA (typical) until either the MOSFET V_{GS} reaches the $V_{GATE–TH}$ threshold (typically 5 V) indicating that the MOSFET channel is at least somewhat enhanced, or the voltage on the TIMER pin reaches the V_{TMRH} threshold (typically 2 V) indicating a fault condition. If the MOSFET V_{GS} reaches 5-V threshold before the TIMER pin reaches the typical 2 V timer fault threshold, the timer capacitor is then discharged to 300 mV, and then begins charging with 11-µA current source while the MOSFET transitions through the active region. The lower timer capacitor charge current during the initial start-up sequence allows more time before a fault is indicated. The turn-on time of the MOSFET will vary with input voltage, load capacitance, load resistance, as well as the MOSFET characteristics.
2. Figure 22 shows a start-up waveform with excessive gate leakage. The initial charge current on the timer capacitor is 6 µA (typical), while the simultaneous charge current to the gate is 24 µA (typical). Due to excessive gate leakage, the 24 µA is not able to charge the gate to the required typical 5 V V_{GS} threshold and the V_{DS} Fault Comparator will indicate a fault when the timer capacitor is charged to the V_{TMRH} fault threshold. When the timer capacitor voltage reaches theV_{TMRH} fault threshold (typically 2 V) the MOSFET gate is discharged at an 80 mA (typical) rate.

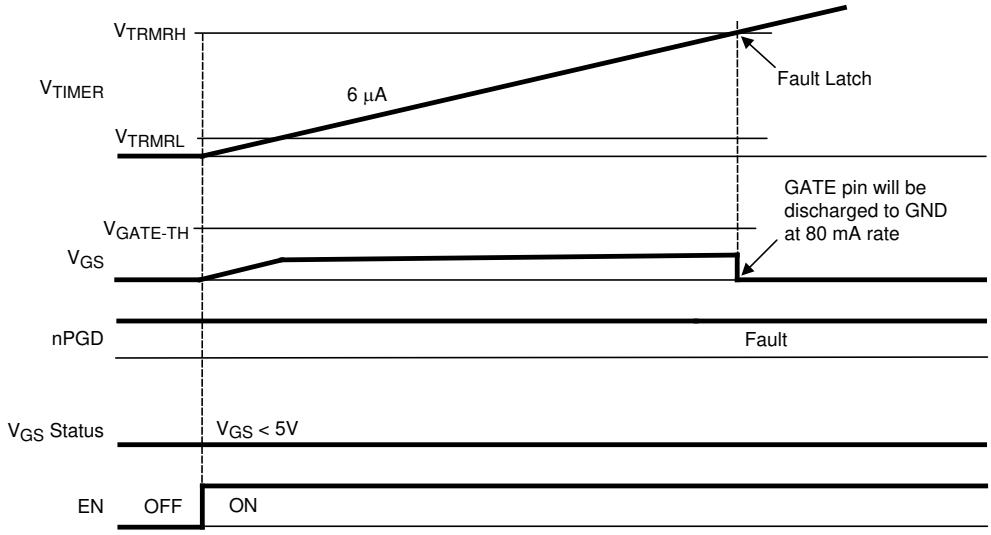


Figure 22. Voltages During Startup With V_{GS} Gate Leakage Condition

8.1.4 V_{DS} Fault Condition

The LM5060 includes a V_{DS} Fault Comparator that senses the voltage difference between the SENSE pin and the OUT pin. If the voltage at the OUT pin falls lower than the voltage at the SENSE pin, the V_{DS} Fault Comparator will trip and switch the nPGD pin to a high impedance state. It will also initiate charging of the capacitor on the TIMER pin with a 6-µA (typical) current source if V_{GS} is less than than 5-V, or a 11-µA (typical) current source if V_{GS} is higher than 5 V. If the voltage on the TIMER pin reaches the typical 2 V fault threshold, the gate of the N-Channel MOSFET is pulled low with a 80 mA (typical) sink current. Figure 23 illustrates a V_{DS} fault condition during start-up. The nPGD pin never switches low because the V_{DS} fault comparator detects excessive V_{DS} voltage throughout the entire sequence.

Application Information (continued)

8.1.5 Overcurrent Fault

The V_{DS} Fault Comparator can be used to implement an Over-Current shutdown function. The V_{DS} Fault Comparator monitors the voltage difference between the SENSE pin and the OUT pin. This is, essentially, the same voltage that is across the N-Channel MOSFET $R_{DS(ON)}$ less the threshold voltage that is set by the series resistor on the SENSE pin. The value of capacitor on the TIMER pin, the capacitor charge current (I_{TIMERH}, 11 µA typical), along with the TIMER pin fault threshold (V_{TMRH}) will determine the how long the N-Channel MOSFET will be allowed to conduct excessive current before the MOSFET is turned-off. When this delay time expires, the gate is discharged at a 80 mA rate.

The LM5060 is intended for applications where precise current sensing is not required, but some level of fault protection is needed. Examples are applications where inductance or impedance in the power path limits the current rise in a short circuit condition.

The Safe Operating Area (SOA) of the external N-Channel MOSFET should be carefully considered to ensure the peak drain-to-source current and the duration of the fault delay time is within the SOA rating of the MOSFET. Also note that the $R_{DS(ON)}$ variations of the external N-Channel MOSFET will affect the accuracy of the Over-Current detection.

8.1.6 Restart After Overcurrent Fault Event

When a V_{DS} fault condition has occurred and the TIMER pin voltage has reached 2 V, the LM5060 latches off the external MOSFET. In order to initiate a restart, either the EN pin, the VINpin, or the UVLO pin must be toggled low and then high.

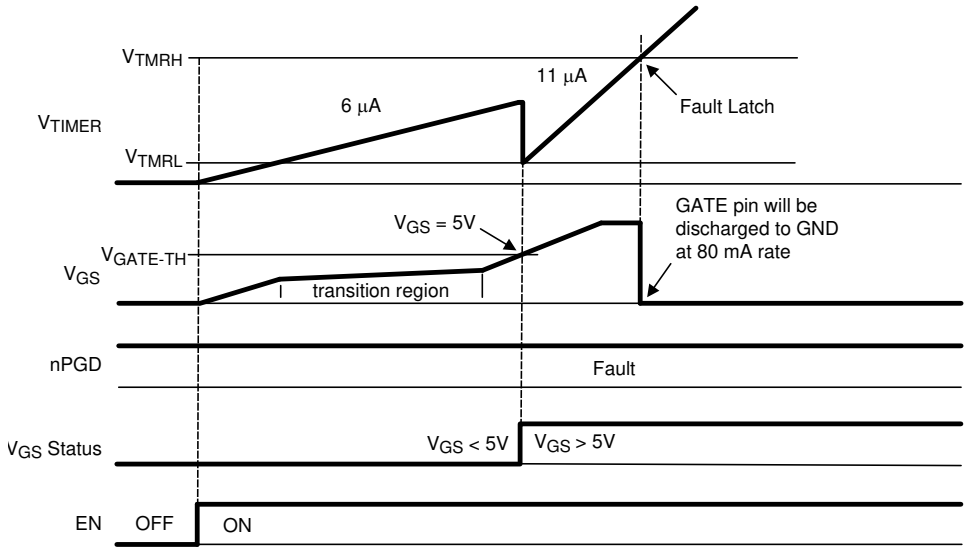


Figure 23. Voltages During Startup with V_{DS} Fault Condition

8.1.7 Enable

The LM5060 Enable pin (EN) allows for remote On/Off control. The Enable pin on/off thresholds are CMOS compatible. The external N-Channel MOSFET can be remotely switched Off by forcing the EN pin below the lower input threshold, EN_{THL} (800 mV). The external N-Channel MOSFET can be remotely switched On by forcing the EN pin above the upper input threshold, EN_{THH} (2.00 V). Figure 24 shows the threshold levels of the Enable pin.

When the EN pin is less than 0.5 V (typical) the LM5060 enters a low current (disabled) state. The current consumption of the VIN pin in this condition is 9 µA (typical).

Application Information (continued)

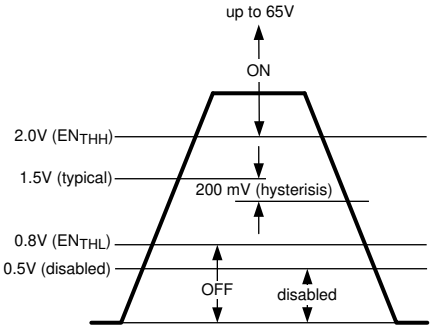


Figure 24. Enable Function Threshold Levels

8.1.8 UVLO

The UVLO function will turn off the external N-Channel MOSFET with a 2.2 mA (typical) current sink at the GATE pin. Figure 25 shows the threshold levels of the UVLO input. A resistor divider as shown in Figure 20 with R10 and R11 sets the voltage at which the UVLO function engages. The UVLO pin may also be used as a second enable pin for applications requiring a redundant, or secondary, shut-down control. Unlike the EN pin function, the UVLO function does not switch the LM5060 to the low current (disabled) state.

If the UVLO function is not needed, the UVLO pin should be connected to the VIN pin. The UVLO pin should not be left floating as the internal pull-down will keep the UVLO active.

In addition to the programmable UVLO function, an internal Power-On-Reset (POR) monitors the voltage at the VIN pin and turns the MOSFET Off when VIN falls below typically 5.10 V.

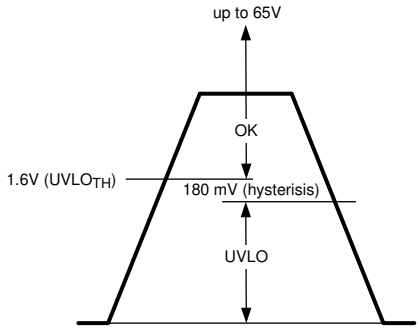


Figure 25. UVLO Threshold Levels

8.1.9 OVP

The OVP function will turn off the external N-Channel MOSFET if the OVP pin voltage is higher than the OVP_{TH} threshold (typically 2 V). A resistor divider made up with R8 and R9, shown in Figure 20, sets the OVP threshold. An internal 9.6-µs timer filters the output of the over-voltage comparator to prevent noise from triggering an OVP event. An OVP event lasting longer than typically 9.6 µs will cause the GATE pin to be discharged with an 80 mA current sink and will cause the capacitor on the TIMER pin to be discharged.

If the OVP function is not needed, the OVP pin should be connected to GND. The OVP pin should not be left floating.

Application Information (continued)

8.1.10 Restart After OVP Event

After the OVP function has been activated and the gate of the external N-Channel MOSFET has been pulled low, the OUT pin is likely to be low as well. However, an OVP condition will not cause the V_{DS} Fault Comparator to latch off of the LM5060 because the capacitor on the TIMER pin is also discharged during an OVP event. After the OVP pin falls below the lower threshold (typically 1.76 V), the LM5060 will re-start as described in the normal start-up sequence and shown in Figure 21. The EN, VIN, or UVLO pins do not need to be toggled low to high to re-enable the MOSFET after an OVP event.

8.1.11 nPGD Pin

The nPGD pin is an open drain connection that indicates when a V_{DS} fault condition has occurred. If the SENSE pin voltage is higher than the OUT pin voltage the state of the nPGD pin will be high impedance. In the typical application, as shown in Figure 20, the voltage at the nPGD pin will be high during any V_{DS} fault condition. The nPGD state is independent of the fault timer function. The resistance R4 should be selected large enough to safely limit the current into the nPGD pin. Limiting the nPGD low state current below 5 mA is recommended.

8.2 Typical Applications

Three application examples are provided. *Example Number 1: LM5060EVAL Design* illustrates the process for the LM5060EVAL in *Related Documentation*. *Example Number 2: Reverse Polarity Protection With Diodes* and *Example Number 3: Reverse Polarity Protection With Resistor* illustrate two other applications that provide additional protection features.

8.2.1 Example Number 1: LM5060EVAL Design

Figure 26 shows the schematic for the LM5060EVAL in *Related Documentation*. Design example number 1 illustrates the basic design procedure used for the evaluation module.

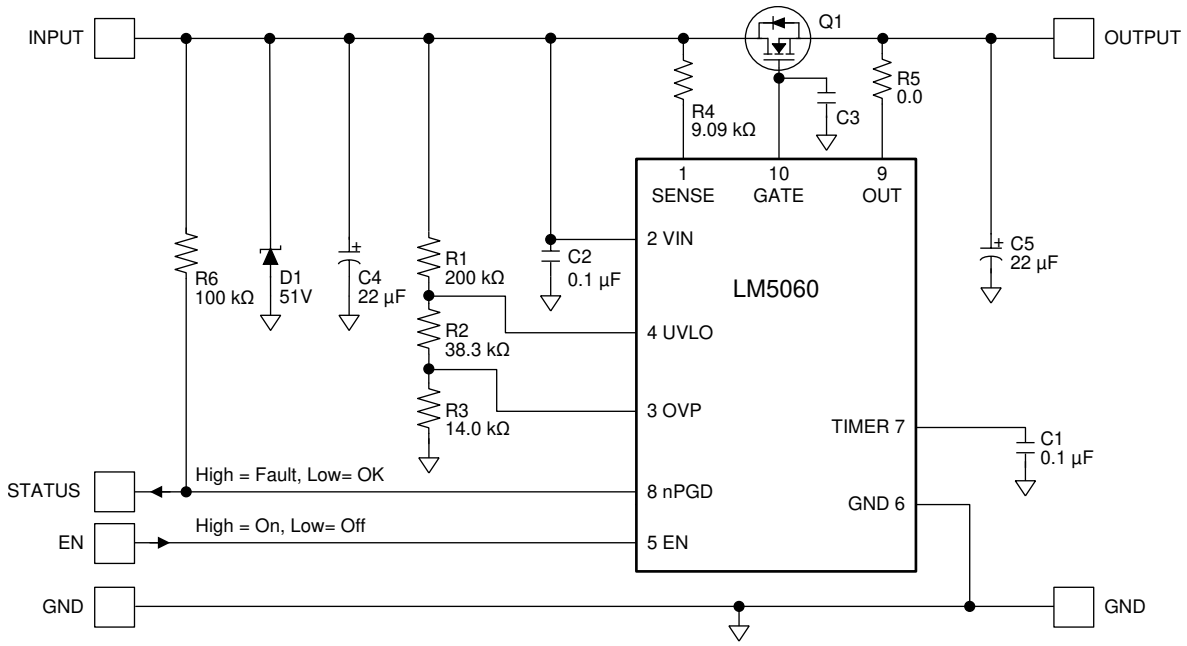


Figure 26. SNVA413 Schematic Diagram

8.2.1.1 Design Requirements

Example number 1 design requirements are shown in Table 2.

Table 2. Example Number 1 Circuit Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Maximum input voltage (OVP)	37 V
Minimum input voltage (UVLO)	9 V
Output current range	0 A to 5.0 A
Ambient temperature range	0°C to 50°C

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 V_{DS} Fault Detection and Selecting Sense Pin Resistor R_S

The LM5060 monitors the V_{DS} voltage of the external N-Channel MOSFET. The drain to source voltage threshold (V_{DSTH}), which is set with the resistor R_S, is shown in Figure 27;

$$V_{DSTH} = (R_S \times I_{SENSE}) - V_{OFFSET} \quad (1)$$

The MOSFET drain to source current threshold is:

$$I_{DSTH} = \frac{V_{DSTH}}{R_{DS(ON)}}$$

where

- $R_{DS(ON)}$ is the resistive drop of the pass element Q1 in Figure 27
- V_{OFFSET} is the offset voltage of the V_{DS} comparator
- I_{SENSE} (16 µA typical) is the threshold programming current (2)

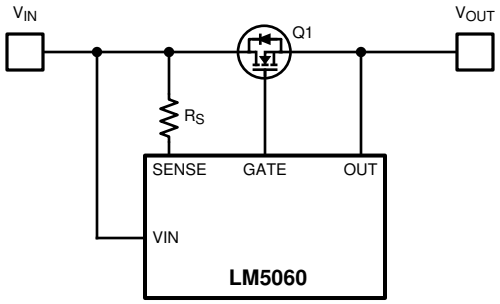


Figure 27. Setting the V_{DS} Threshold

8.2.1.2.2 Turn-On Time

To slow down the output rise time a capacitor from the GATE pin to GND may be added. The turn on time depends on the threshold level of the N-Channel MOSFET, the gate capacitance of the MOSFET as well as the optional capacitance from the GATE pin to GND. Figure 28 shows the slow down capacitor C1. Reducing the turn-on time allows the MOSFET (Q1), to slowly charge a large load capacitance. Special care must be taken to keep the MOSFET within its safe operating area. If the MOSFET turns on too slow, the peak power losses may damage the device.

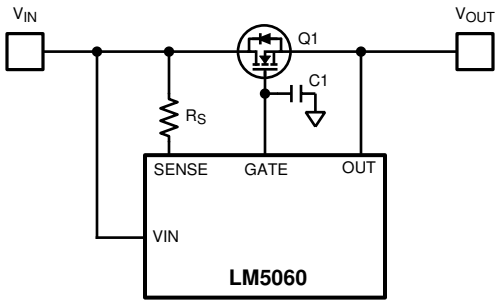


Figure 28. Turn-On Time Extension

8.2.1.2.3 Fault Detection Delay Time

To allow the gate of the MOSFET adequate time to change, and to allow the MOSFET to conduct currents beyond the protection threshold for a brief period of time, a fault delay timer function is provided. This feature is important when drive loads which require a surge of current in excess of the normal ON current upon start up, or at any point in time, such as lamps and motors. A single low leakage capacitor (C_{TIMER}) connected from the TIMER (pin 7), to ground sets the delay time interval for both the V_{GS} status detection at start-up and for the subsequent V_{DS} Over-Current fault detection.

When the LM5060 is enabled under normal operating conditions the timer capacitor will begin charging at a 6 μA (typical) rate while simultaneously charging the gate of the external MOSFET at a 24 μA (typical) rate. The gate-to-source voltage (V_{GS}) of the external MOSFET is expected to reach the 5-V (typical) threshold before the timer capacitor has charged to the V_{TMRH} threshold (2 V typical) in order to avoid being shutdown.

While V_{GS} is less than the typical 5-V threshold ($V_{GATE-TH}$), the V_{DS} start-up fault delay time is calculated from:

$$V_{DS}\ \text{Fault Delay} = \left(\frac{V_{TIMERH} \times C_{TIMER}}{I_{TIMERL}}\right)$$

where

- I_{TMRL} is typically 6 μA and V_{TMRH} is typically 2 V (3)

If the C_{TIMER} value is 68 nF (0.068μF) the V_{GS} start-up fault delay time would typically be:

V_{DS} Fault Delay = ((2 V x 0.068 μF) / 6 μA) = 23 ms (4)

When the LM5060 has successfully completed the start-up sequence by reaching a V_{GS} of 5 V within the fault delay time set by the timer capacitor (C_{TIMER}), the capacitor is quickly discharged to 300 mV (typical) and the charge current is increased to 11 μA (typical) while the gate of the external MOSFET is continued to be charge at a 24 μA (typical) rate. The external MOSFET may not be fully enhanced at this point in time and some additional time may be needed to allow the gate-to-source voltage (V_{GS}) to charge to a higher value. The drain-to-source voltage (V_{DS}) of the external MOSFET must fall below the V_{DSTH} threshold set by R_S and I_{SENSE} before the timer capacitor has charged to the V_{TMRH} threshold (2 V typical) to avoid a fault.

When V_{GS} is greater than the typical 5-V threshold ($V_{GATE-TH}$), the V_{DS} transition fault delay time is calculated from:

$$V_{DS}\ \text{Fault Delay} = \left(\frac{(V_{TIMERH} - V_{TMRL}) \times C_{TIMER}}{I_{TIMERH}}\right)$$

where

- I_{TMRH} is typically 11 μA
- V_{TMRH} is typically 2 V
- V_{TMRL} is typically 300 mV (5)

If the C_{TIMER} value is 68 nF(0.068 μF) the V_{DS} transition fault delay time would typically be:

V_{DS} Fault Delay = (((2 V–0.3 V) x 0.068 μF) / 11 μA) = 10 ms (6)

Should a subsequent load current surge trip the V_{DS} Fault Comparator, the timer capacitor discharge transistor turns OFF and the 11 μA (typical) current source begins linearly charging the timer capacitor. If the surge current, with the detected excessive V_{DS} voltage, lasts long enough for the timer capacitor to charge to the timing comparator threshold (V_{TMRH}) of typically 2 V, the LM5060 will immediately discharge the MOSFET gate and latch the MOSFET off. The V_{DS} fault delay time during an Over-Current event is calculated from:

$$V_{DS}\ \text{Fault Delay} = \left(\frac{V_{TIMERH} \times C_{TIMER}}{I_{TIMERH}} \right)$$

where

- I_{TMRH} is typically 11 μA
- V_{TMRH} is typically 2 V (7)

If the C_{TIMER} value is 68 nF(0.068 μF) the V_{DS} Over-Current fault delay time would typically be:

V_{DS} Fault Delay = ((2 V x 0.068 μF) / 11 μA) = 12 ms (8)

Since a single capacitor is used to set the delay time for multiple fault conditions, it is likely that some compromise will need to be made between a desired delay time and a practical delay time.

8.2.1.2.4 MOSFET Selection

The external MOSFET (Q1) selection should be based on the following criteria:

- The BV_{DSS} rating must be greater than the maximum system voltage (V_{IN}), plus ringing and transients which can occur at V_{IN} when the circuit is powered on or off.
- The maximum transient current rating should be based on the maximum worst case V_{DS} fault current level.
- MOSFETs with low threshold voltages offer the advantage that during turn on they are more likely to remain within their safe operating area (SOA) because the MOSFET reaches the ohmic region sooner for a given gate capacitance.
- The safe operating area (SOA) of the MOSFET device and the thermal properties should be considered relative to the maximum power dissipation possible during startup or shutdown.
- $R_{DS(ON)}$ should be sufficiently low that the power dissipation at maximum load current ($(I_{L(MAX)})^2 \times R_{DS(ON)}$) does not increase the junction temperature above the manufacturer's recommendation.
- If the device chosen for Q1 has a maximum V_{GS} rating less than 16 V, an external zener diode must be added from gate to source to limit the applied gate voltage. The external zener diode forward current rating should be at least 80 mA to conduct the full gate pull-down current during fault conditions.

8.2.1.2.5 Input and Output Capacitors

Input and output capacitors are not necessary in all applications. Any current that the external MOSFET conducts in the on-state will decrease very quickly as the MOSFET turns off. All trace inductances in the design including wires and printed circuit board traces will cause inductive voltage kicks during the fast termination of a conducting current. On the input side of the LM5060 circuit this inductive kick can cause large positive voltage spikes, while on the output side, negative voltage spikes are generated. To limit such voltage spikes, local capacitance or clamp circuits can be used. The necessary capacitor value depends on the steady state input voltage level, the level of current running through the MOSFET, the inductance of circuit board traces as well as the transition speed of the MOSFET.

Since the exact amount of trace inductance is hard to predict, careful evaluation of the circuit board is the best method to optimize the input or output capacitance or clamp circuits.

8.2.1.2.6 UVLO, OVP

The UVLO and OVP thresholds are programmed to enable the external MOSFET (Q1) when the input supply voltage is within the desired operating range. If the supply voltage is low enough that the voltage at the UVLO pin is below the UVLO threshold, Q1 is switched off by a 2.2 mA (typical) current sink at the GATE pin, denying power to the load. The UVLO threshold has approximately 180 mV of hysteresis.

If the supply voltage is high enough that the voltage at the OVP pin is above the OVP threshold, the GATE pin is pulled low with a 80 mA current sink. Hysteresis is provided for each threshold. The OVP threshold has approximately 240 mV of hysteresis.

Option A: The configuration shown in Figure 29 requires three resistors (R1, R2, and R3) to set the thresholds.

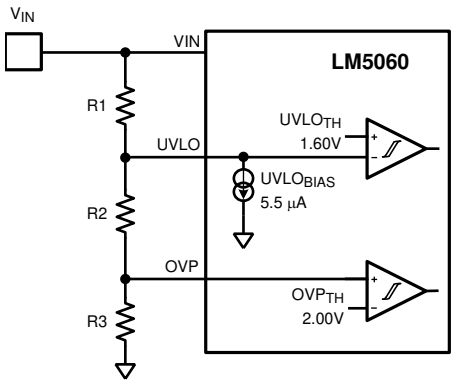


Figure 29. UVLO and OVP Thresholds Set by R1, R2 and R3

The procedure to calculate the resistor values is as follows:

1. Select R1 based on current consumption allowed in the resistor divider, including $UVLO_{BIAS}$, and consideration of noise sensitivity. A value less than 100 kΩ is recommended, with lower values providing improved immunity to variations in $ULVO_{BIAS}$.
2. Calculate R3 with the following formula:

$$R3 = \frac{\left(\frac{UVLO_{TH} \times R1}{V_{INMIN} - UVLO_{TH} - (UVLO_{BIAS} \times R1)} + R1\right)}{\left(\frac{V_{INMAX}}{OVP_{TH}} - \frac{UVLO_{BIAS} \times R1}{OVP_{TH}}\right)} \quad (9)$$

3. Calculate R2 with the following formula:

$$R2 = \frac{R3 \times V_{INMAX}}{OVP_{TH}} - R3 - R1 - \frac{UVLO_{BIAS} \times R1 \times R3}{OVP_{TH}} \quad (10)$$

V_{INMIN} is the minimum and V_{INMAX} is the maximum input voltage of the design specification. All other variables can be found in the *Electrical Characteristics* table of this document. To calculate the UVLO lower threshold including its hysteresis for falling V_{IN}, use ($UVLO_{TH}$-$UVLO_{HYS}$) instead of $UVLO_{TH}$ in the formulas above. To calculate the OVP lower threshold including hysteresis for falling V_{IN}, use (OVP_{TH}-OVP_{HYS}) instead of OVP_{TH}. With three given resistors R1, R2, and R3, the thresholds can be calculated with the formulas below:

$$V_{INMAX} = R1 \times \left(\frac{OVP_{TH}}{R3} + UVLO_{BIAS}\right) + R2 \times \frac{OVP_{TH}}{R3} + OVP_{TH}$$

$$V_{INMIN} = \left(\frac{UVLO_{TH}}{R2 + R3} + UVLO_{BIAS}\right) \times R1 + UVLO_{TH} \quad (11)$$

Also in these two formulas, the respective lower threshold value including the hysteresis is calculated by using ($UVLO_{TH}$-$UVLO_{HYS}$) instead of $UVLO_{TH}$, and (OVP_{TH}-OVP_{HYS}) instead of OVP_{TH}. The worst case thresholds, over the operating temperature range, can be calculated using the respective min and max values in bold font in the *Electrical Characteristics*.

Option B: UVLO and OVP can be independently adjusted using two resistor dividers as shown in Figure 30.

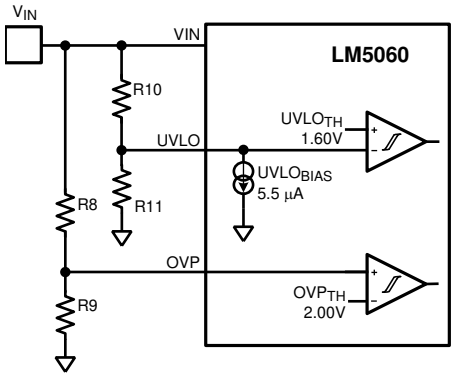


Figure 30. Programming the Thresholds with Resistors R8-R11

Choose the upper UVLO thresholds to ensure operation down to the lowest required operating input voltage (V_{INMIN}). Select R11 based on resistive divider current consumption and noise sensitivity. A value less than 100 kΩ is recommended, with lower values providing improved immunity to variations in $ULVO_{BIAS}$.

$$R10 = \frac{V_{INMIN} - UVLO_{TH}}{\left(UVLO_{BIAS} + \frac{UVLO_{TH}}{R11}\right)} \tag{12}$$

To calculate the UVLO low threshold including its hysteresis, use ($UVLO_{TH}$-$UVLO_{HYS}$) instead of $UVLO_{TH}$ in the formula above. Choose the lower OVP threshold to ensure operation up to the highest VIN voltage required (V_{INMAX}). Select R9 based on resistive divider current consumption A value less than 100 kΩ is recommended.

$$R8 = R9 \times \left(\frac{V_{INMAX} - OVP_{TH}}{OVP_{TH}}\right) \tag{13}$$

To calculate the OVP low threshold including hysteresis, use (OVP_{TH}-OVP_{HYS}) instead of OVP_{TH}. Where the R9-R11 resistor values are known, the threshold voltages are calculated from the following:

$$V_{INMAX} = OVP_{TH} + \frac{R8 \times OVP_{TH}}{R9}$$

$$V_{INMIN} = UVLO_{TH} + \left[R10 \times \left(UVLO_{BIAS} + \frac{UVLO_{TH}}{R11}\right)\right] \tag{14}$$

Also in these two formulas, the respective low value including the threshold hysteresis is calculated by using ($UVLO_{TH}$-$UVLO_{HYS}$) instead of $UVLO_{TH}$ and (OVP_{TH}-OVP_{HYS}) instead of OVP_{TH}. The worst case thresholds, over the operating temperature range, can be calculated using the respective minimum and maximum values in bold font in the *Electrical Characteristics*.

Option C: The OVP function can be disabled by grounding the OVP pin. The UVLO thresholds are set as described in Figure 30.

8.2.1.2.7 POWER GOOD Indicator

A resistor between a supply voltage and the nPGD pin limits the current into the nPGD pin in a logic low condition. A nPGD pin sink current in the range of 1 mA to 5 mA is recommended. The example in Figure 31 connects the nPGD pull-up resistor R4 to the VIN pin. Any positive supply voltage less than 65 V may be used instead of V_{IN}.

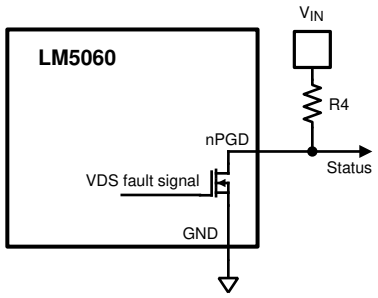


Figure 31. Circuitry at the nPGD Pin

8.2.1.2.8 Input Bypass Capacitor

Some input capacitance from the VIN pin to the GND pin may be necessary to filter noise and voltage spikes from the V_{IN} rail. If the current through Q1 in Figure 20 is very large a sudden shutdown of Q1 will cause an inductive kick across the line input and pc board trace inductance which could damage the LM5060. In order to protect the VIN pin as well as SENSE, OVP, UVLO, and nPGD pins from harm, a larger bulk capacitor from VIN to GND may be needed to reduce the amplitude of the voltage spikes. Protection diodes or surge suppressors may also be used to limit the exposure of the LM5060 pins to voltages below their maximum operating ratings.

8.2.1.2.9 Large Load Capacitance

Figure 32 shows an application with a large load capacitance C_L. Assume a worst case turn off scenario where Vin remains at the same voltage as C_L and R_L is a high impedance. The body diode of Q1 will not conduct any current and all the charge on C_L is dissipated through the LM5060 internal circuitry. The dotted line in Figure 32 shows the path of this current flow. Initially the power dissipated by the LM5060 is calculated with the formula:

$$P = I_{GATE\text{-}FLT} \times V_{OUT} \quad (15)$$

where

- $I_{GATE\text{-}FLT}$ is the sink current of the LM5060 gate control

In applications with a high input voltage and very large output capacitance, the discharge current can be limited by an additional discharge resistor R_O in series with the OUT pin as shown in Figure 33. This resistor will influence the current limit threshold, so the value of R_S will need to be readjusted.

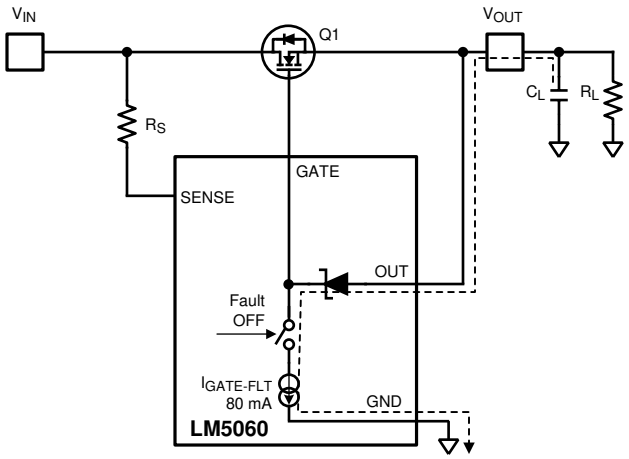


Figure 32. Discharge Path of Possible Load Capacitor

In applications exposed to reverse polarity on the input and a large load capacitance on the output, a current limiting resistor in series with the OUT pin is required to protect the LM5060 OUT pin from reverse currents exceeding 25 mA. Figure 33 shows the resistor R_O in the trace to the OUT pin.

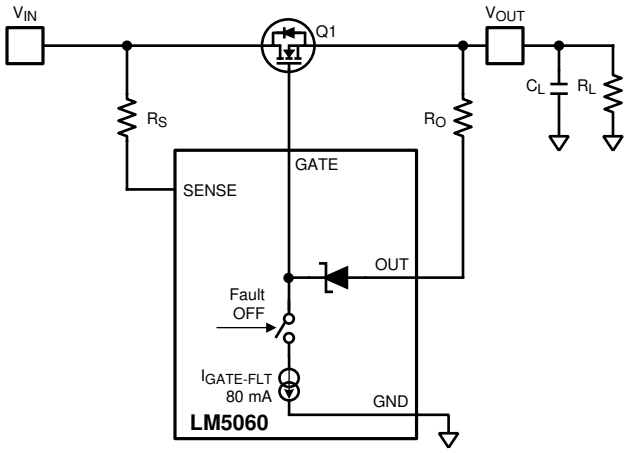


Figure 33. Current Limiting Resistor R_O for Special Cases

If a R_O resistor in the OUT path is used, the current sensing will become less accurate since R_O has some variability as well as the current into the OUT pin. The OUT pin current is specified in the *Electrical Characteristics* section as I_{OUT-EN}. A R_O resistor design compromise for protection of the OUT pin and a maintaining V_{DS} sensing accuracy can be achieved. See the *Reverse Polarity Protection With a Resistor* section for more details on how to calculate a reasonable R_O value.

8.2.1.3 Application Curves

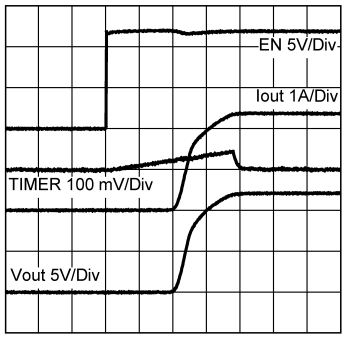


Figure 34. Start-Up Waveform

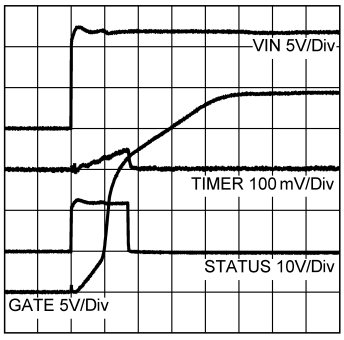


Figure 35. Start-Up Waveform

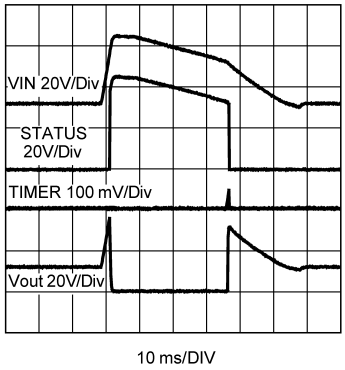


Figure 36. OVP Behavior

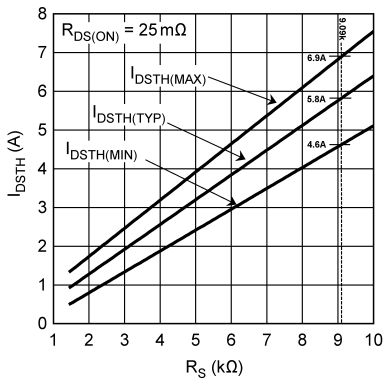


Figure 37. R_S vs I_{DSTH} for $R_{DS(ON)}$ = 25 mΩ

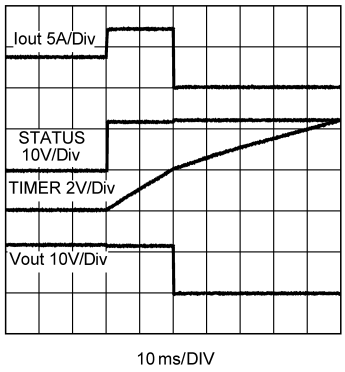


Figure 38. Fault Behavior

8.2.2 Example Number 2: Reverse Polarity Protection With Diodes

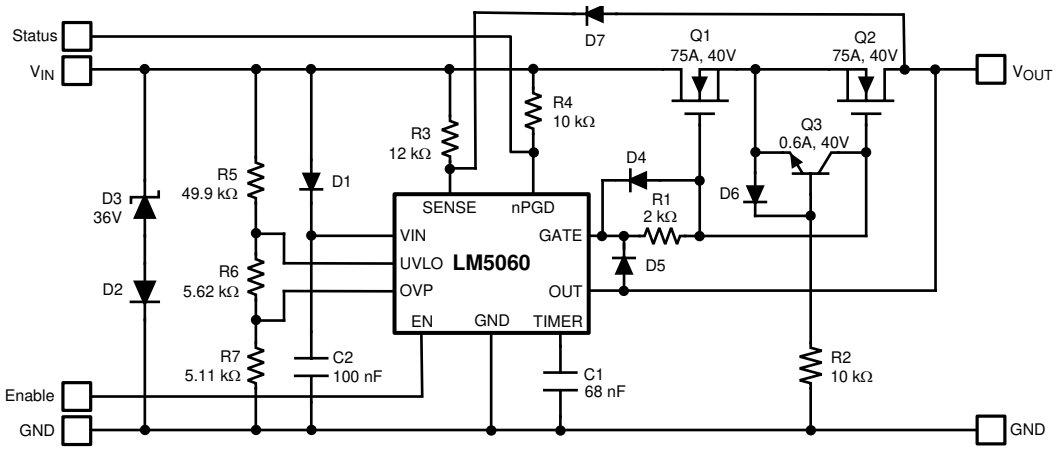


Figure 39. Application with Reverse Polarity Protection with Diodes for OUT Pin Protection

Figure 39 shows the LM5060 in an automotive application with reverse polarity protection. The second N-channel MOSFET Q2 is used to prevent the body diode of Q1 from conducting in a reverse V_{IN} polarity situation. The zener diode D3 is used to limit V_{IN} voltage transients which will occur when Q1 and Q2 are shut off quickly. In some applications the inductive kick is handled by input capacitors and D3 can be omitted. In reverse polarity protected applications, the input capacitors will see the reverse voltage. To avoid stressing input capacitors with reverse polarity, a transorb circuit implemented with D3 and D2 may be used. Diode D1 in Figure 39 protects the VIN pin in the event of reverse polarity. The resistor R1 protects the GATE pin from reverse currents exceeding 25 mA in the reverse polarity situation. This GATE resistor would slow down the shutdown of Q1 and Q2 dramatically. To prevent a slow turn off in fault conditions, D5 is added to bypass the current limiting resistor R1. When Q1 and Q2 are turned on, R1 does not cause any delay because the GATE pin is driven with a 24-µA current source. D6, Q3 and R2 protect Q2 from V_{GS} damage in the event of reverse input polarity. Diodes D5 and D7 are only necessary if the output load is highly capacitive. Such a capacitive load in combination with a high reverse polarity input voltage condition can exceed the power rating of the internal zener diode between OUT pin and GATE pin as well as the internal diode between the OUT pin and SENSE pin. External diodes D5 and D7 should be used in reverse polarity protected applications with large capacitive loads.

8.2.2.1 Design Requirements

Example number 2 design requirements are shown in Table 3.

Table 3. Example Number 2 Circuit Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Operating voltage range	9 V to 24 V
Current max	30 A
OVP setting	27 V typical
UVLO setting	9 V typical

8.2.2.2 Application Curve

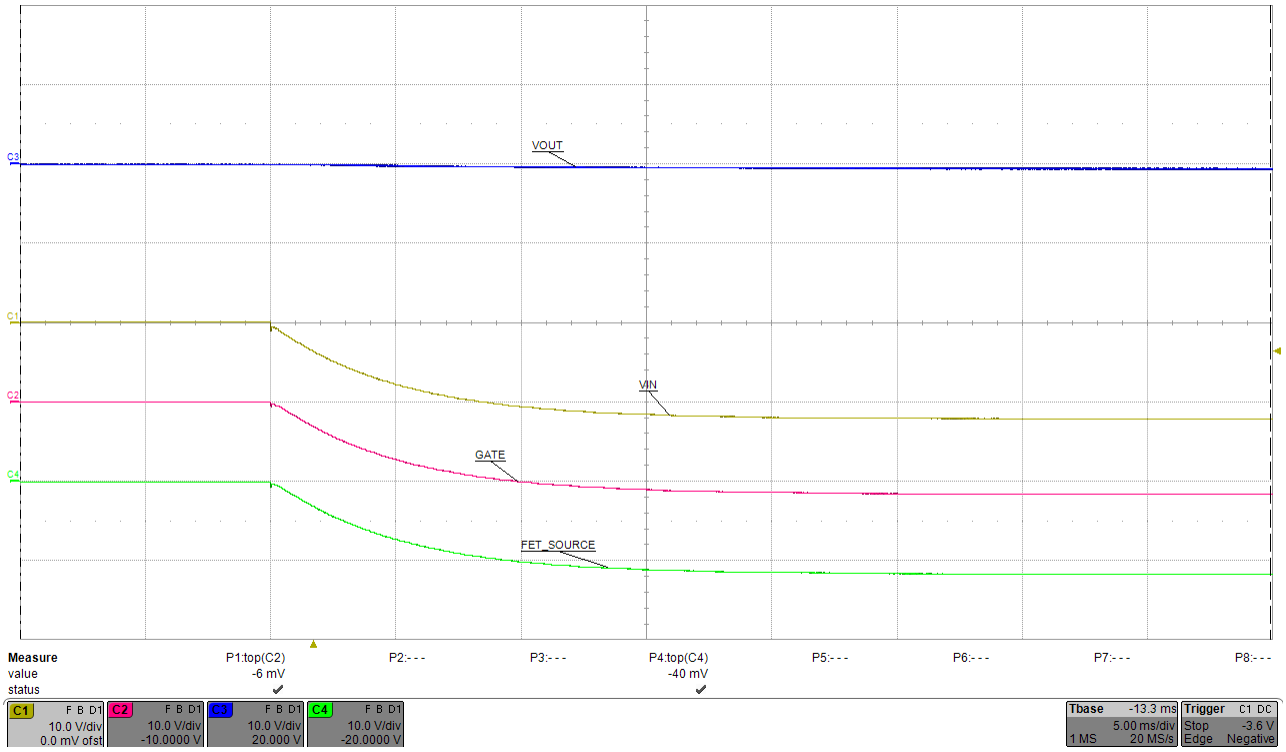


Figure 40. Reverse Input Voltage Polarity

8.2.3 Example Number 3: Reverse Polarity Protection With Resistor

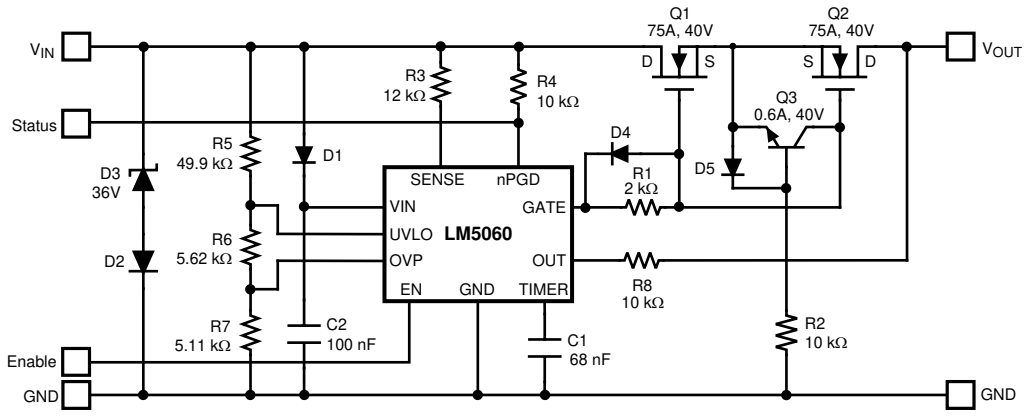


Figure 41. Application with Reverse Polarity Protection with a Resistor for OUT Pin Protection

Figure 41 shows an example circuit which is protected against reverse polarity using resistor R8 instead of the diodes D5 and D7 of Figure 39.

8.2.3.1 Design Requirements

Example number 3 design requirements are shown in Table 4.

Table 4. Example Number 3 Circuit Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Operating voltage range	9 V to 24 V
Current max	30 A
OVP setting	27 V typical
UVLO setting	9 V typical

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Reverse Polarity Protection With a Resistor

An alternative to using external diodes to protect the LM5060 OUT pin in the reverse polarity input condition is a resistor in series with the OUT pin. Adding an OUT pin resistor may require modification of the resistor in series with the SENSE pin. A resistor in series with the OUT pin will limit the current through the internal zener diode between OUT and GATE as well as through the diode between OUT and SENSE. The value of these resistors should be calculated to limit the current through the diode across the input terminals of the V_{DS} fault comparator to be no more than 4 mA. Figure 42 shows the internal circuitry relevant for calculating the values of the resistor R_O in the OUT path to limit the current into the OUT pin to 4 mA.

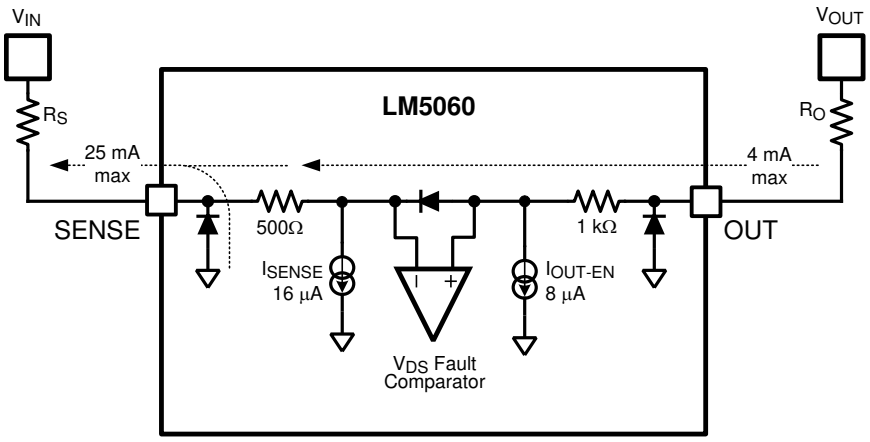


Figure 42. Current Limiting Resistor for Negative SENSE Condition

When calculating the minimum R_O resistor required to limit the current into the OUT pin, the internal current sources of 8 µA and 16 µA may be neglected. The following formulas can be used to calculate the resistor value $R_{O(MIN)}$ which is necessary to keep the I_O current to less than 4 mA.

Case A is for situations where $V_{OUT} > V_{IN}$ and reverse polarity situation is present (see Figure 42). V_{IN} is negative, but the voltage at the SENSE pin can roughly be assumed to be 0.0 V due to the internal diode from the SENSE pin to GND.

$$R_{O(MIN)} = \frac{V_{OUT} - (4\ mA \times 1.5\ k\Omega)}{4\ mA} \quad (16)$$

In this case, V_{IN} also has to be limited to a negative voltage so that reverse current through the SENSE pin does not exceed 25 mA.

$$R_{S(MIN)} = \frac{V_{IN}}{25\ mA} \quad (17)$$

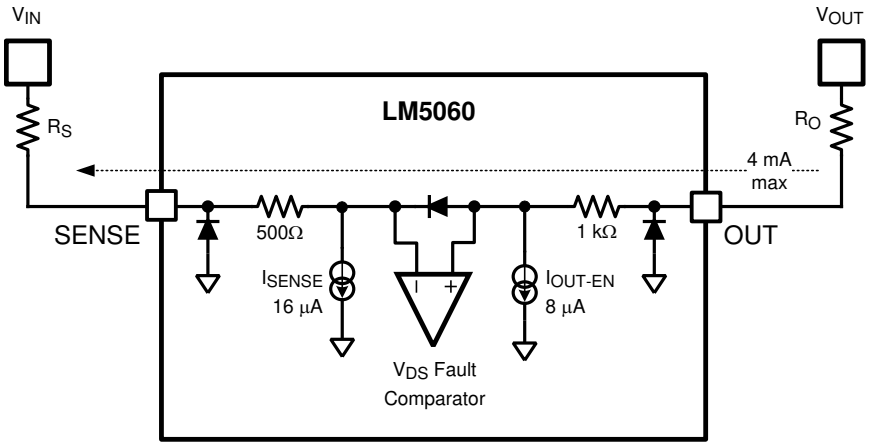


Figure 43. Current Limiting Resistor in the OUT Path for OUT > SENSE Condition

Case B is for situations where $V_{OUT} > V_{IN}$ and there is no reverse polarity situation present (see Figure 43). V_{IN} is positive and V_{OUT} is also positive, but V_{OUT} is higher than V_{IN}:

$$R_{O(MIN)} = \frac{(V_{OUT} - V_{IN})}{4\ mA} - (R_S + 1.5\ k\Omega) \quad (18)$$

In this case the voltage on the SENSE pin should not exceed 65 V.

Case C is for situations where $V_{OUT} < V_{IN}$ and both V_{IN} and V_{OUT} are positive as well. In such cases there is no risk of excessive OUT pin current. No current limiting resistors are necessary. Both the SENSE and OUT voltages should be limited to less than 65 V.

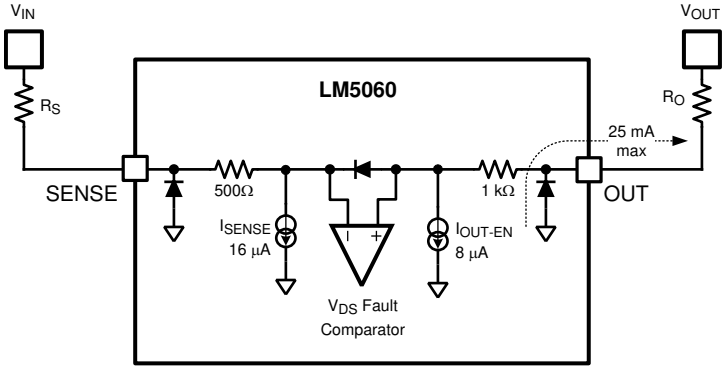


Figure 44. Current Limiting Resistor for Negative OUT Conditions

Case D for situations where $V_{OUT} < V_{IN}$, while V_{OUT} is negative and V_{IN} is positive (see Figure 44). R_O needs to be selected to protect the OUT pin from currents exceeding 25 mA.

$$R_{O(MIN)} = \frac{V_{OUT}}{25\ mA} \quad (19)$$

8.2.3.2.2 Fault Detection With R_S and R_O

Figure 41 shows an example circuit where the OUT pin is protected against a reverse battery situation with a current limiting resistor R_O. When using resistor R_O in the OUT pin path, the resistor R_S has to be selected taking the R_O resistor into account. The LM5060 monitors the V_{DS} voltage of an external N-Channel MOSFET. The V_{DS} fault detection voltage is the drain to source voltage threshold (V_{DSTH}). The formula below calculates a proper R_S resistor value for a desired V_{DSTH} taking into account the voltage drop across the R_O resistor.

$$R_S = \frac{V_{DSTH}}{I_{SENSE}} + \frac{R_O \times I_{OUT\text{-}EN}}{I_{SENSE}} - \frac{V_{OFFSET}}{I_{SENSE}} \quad (20)$$

V_{OFFSET} is the offset voltage between the SENSE pin and the OUT pin, I_{SENSE} is the threshold programming current, and I_{OUT-EN} is the OUT pin bias current. When R_S and R_O have been selected, the following formula can be used for V_{DSTH} min and max calculations:

$$V_{DSTH} = I_{SENSE} \times \left(R_S - \frac{R_O}{I_{RATIO}} \right) + V_{OFFSET} \quad (21)$$

The MOSFET drain-to-source current threshold is:

$$I_{DSTH} = \frac{V_{DSTH}}{R_{DS(ON)}}$$

where

- $R_{DS(ON)}$ is the on resistance of the pass element Q1 in Figure 20 (22)

8.2.3.3 Application Curves

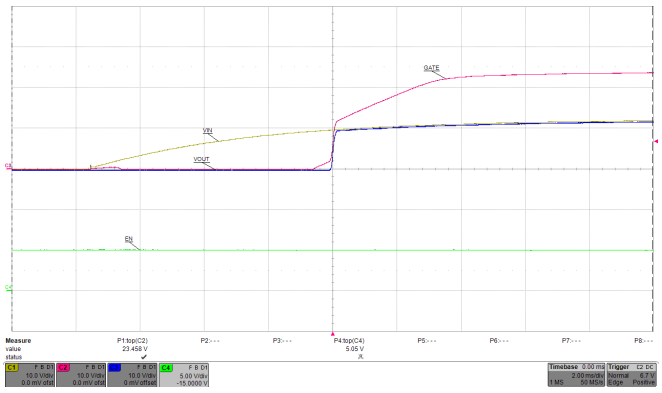


Figure 45. Startup at No Load

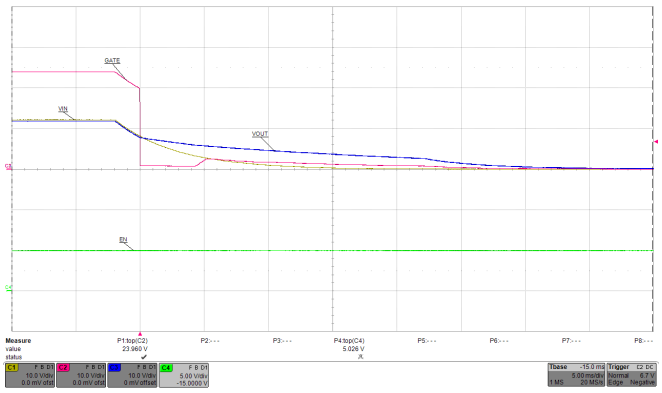


Figure 46. Shutdown

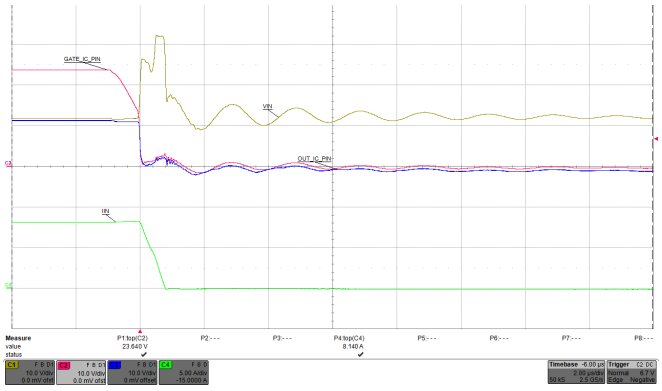


Figure 47. Overcurrent Shutdown with Gate Diode

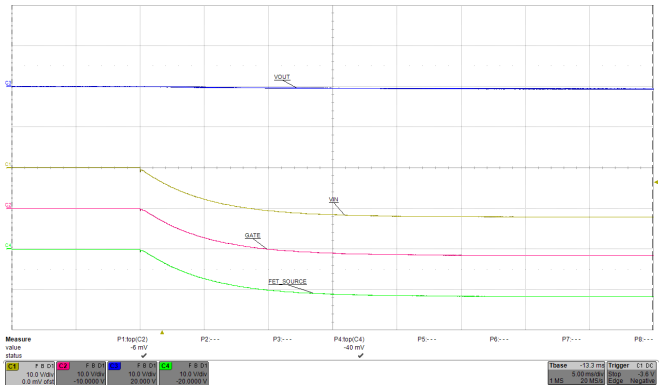


Figure 48. Reverse Input Voltage Polarity

9 Power Supply Recommendations

The recommended input power supple operating voltage range is 5.5 V to 65 V. The VIN source current rating of the power supply should be adequate to keep the LM5060 in the normal operating range during all load and line transients. Place a 10 nF or 100 nF ceramic capacitor close to the VIN pin.

10 Layout

10.1 Layout Guidelines

The component placement and layout should generally follow the example provided in Figure 49. Power from input source to load should flow in a manner similar to that shown in Figure 49 and heavy conductors for traces bearing the load current should be used. Place the VIN bypass capacitor close to pin 2. Place the TIMER capacitor close to pin 7.

10.2 Layout Example

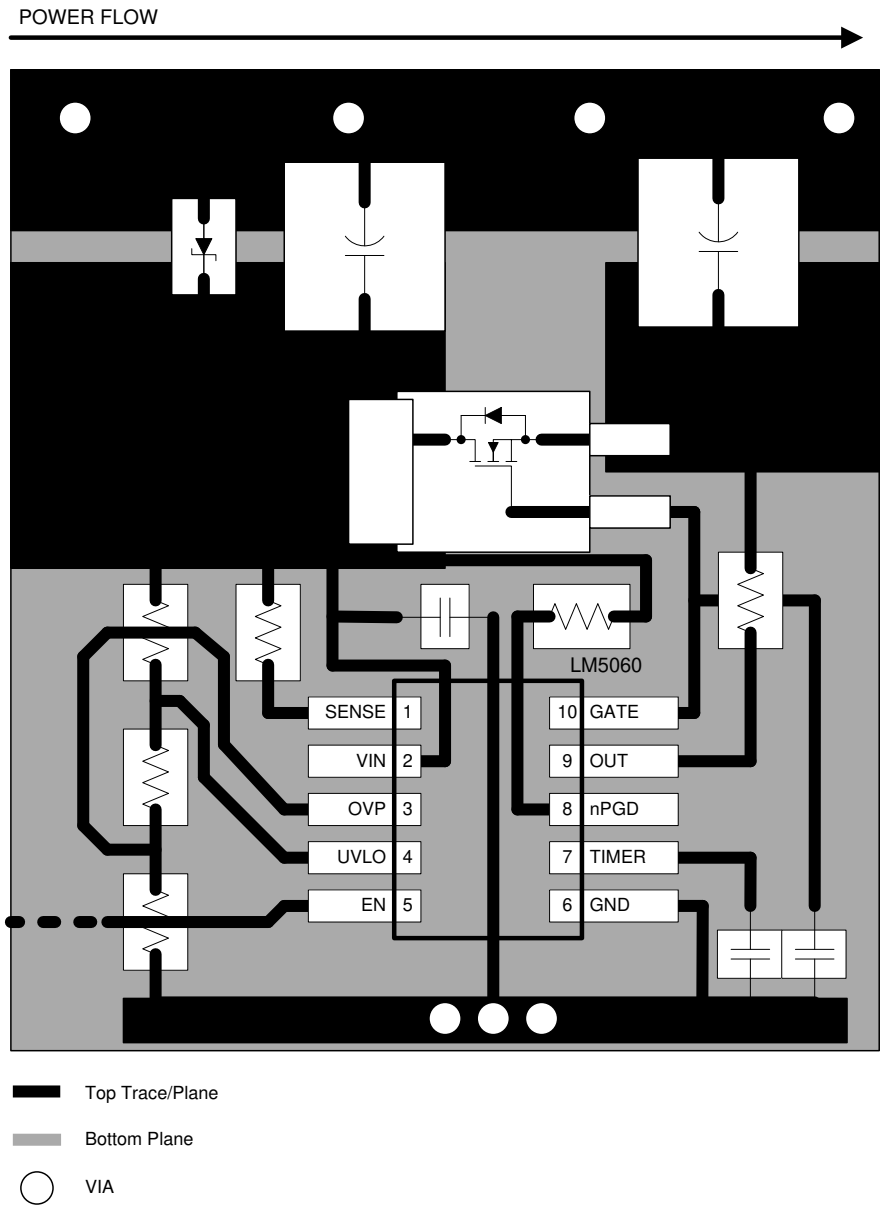


Figure 49. LM5060 Recommended Layout

10.3 Thermal Considerations

In normal operation the LM5060 dissipates very little power so that thermal design may not be very critical. The power dissipation is typically the 2 mA input current times the input voltage. If the application is driving a large capacitive load application, upon shutdown of the LM5060, the load capacitor may partially, or fully, discharge back through the LM5060 circuitry if no other loads consume the energy of the pre-charged load capacitor. One application example where energy is dissipated by the LM5060 is a motor drive application with a large capacitor load. When the LM5060 is turned off, the motor might also turn off such that total residual energy in the load capacitor is conducted through the OUT pin to ground. The power dissipated within the LM5060 is determined by the discharge current of 80 mA and the voltage on the load capacitor.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- LM5060EVAL User Guide, SNVA413

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5060MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SXAB	Samples
LM5060MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SXAB	Samples
LM5060Q1MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SZAB	Samples
LM5060Q1MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SZAB	Samples
LM5060QDGSRQ1	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1EQX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5060, LM5060-Q1 :

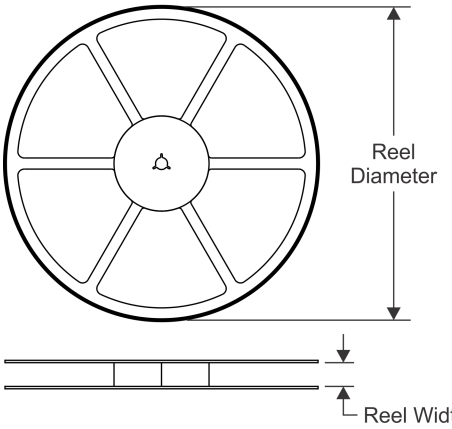
- Catalog: LM5060
- Automotive: LM5060-Q1

NOTE: Qualified Version Definitions:

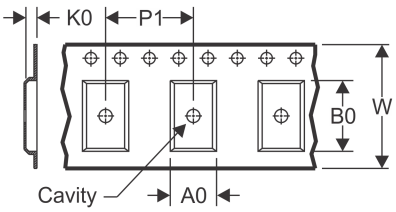
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

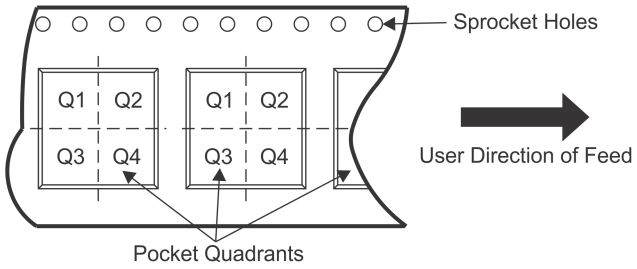


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

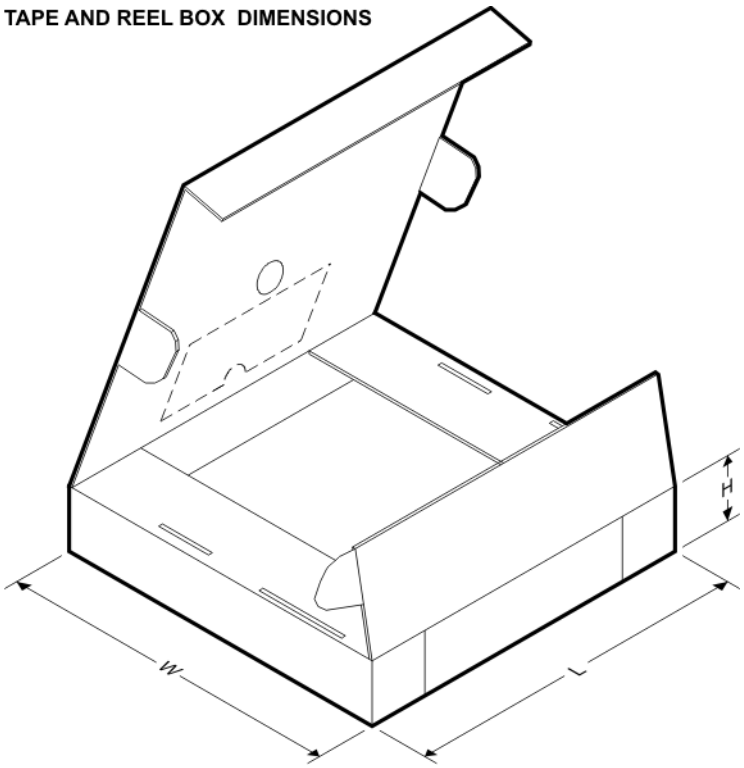
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5060MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5060MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5060Q1MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5060Q1MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5060QDGSRQ1	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

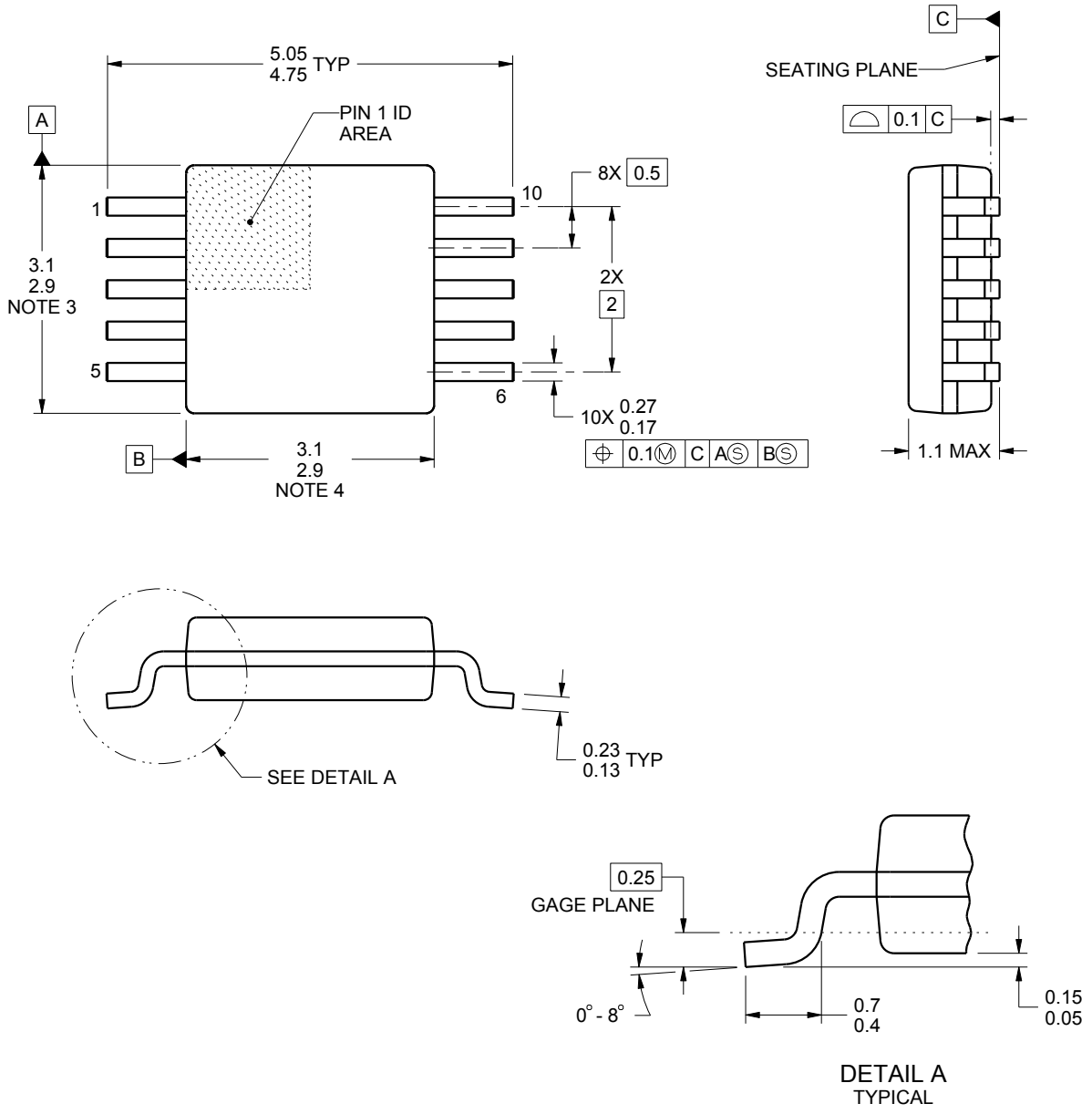
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5060MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5060MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5060Q1MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5060Q1MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5060QDGSRQ1	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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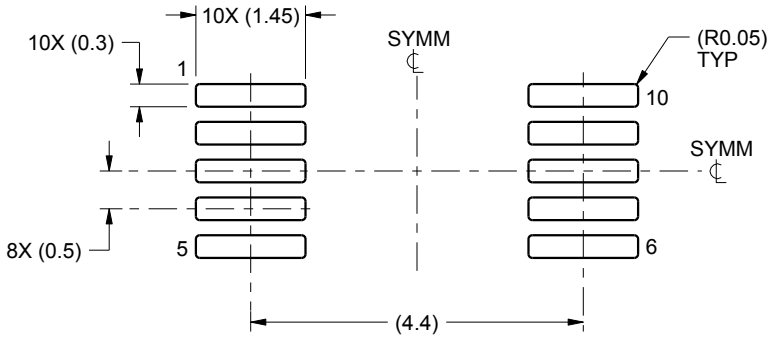
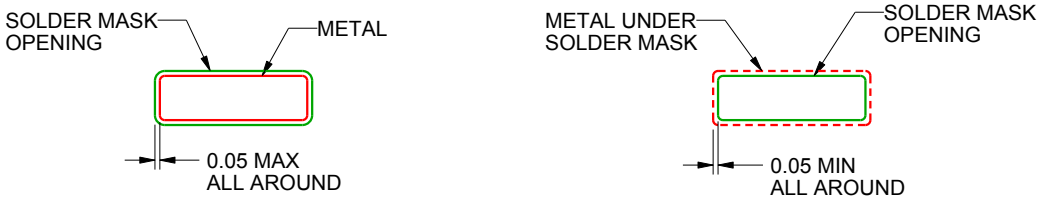
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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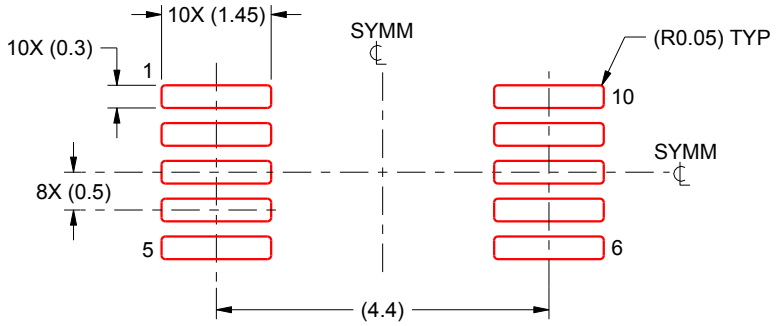
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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