TLVx314-Q1 3-MHz, low-power, internal EMI filter, RRIO, operational amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Low Offset Voltage: 0.75 mV (Typical)
- Low Input Bias Current: 1 pA (Typical)
- Wide Supply Range: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Gain Bandwidth: 3 MHz
- Low I_Q: 250 µA/Ch (Maximum)
- Low Noise: 16 nV/$\sqrt{Hz}$ at 1 kHz
- Internal RF and EMI Filter
- Number of Channels:
  - TLV314-Q1: 1
  - TLV2314-Q1: 2
  - TLV4314-Q1: 4
- Extended Temperature Range: –40°C to +125°C

2 Applications

- Low-Side Sensing
- Battery Management Systems
- Passive Safety
- Capacitive Sensing
- Fuel Pumps

3 Description

The TLVx314-Q1 family of single-, dual-, and quad-channel operational amplifiers represents a new generation of low-power, general-purpose operational amplifiers. Rail-to-rail input and output swings (RRIO), low quiescent current (150 µA typically at 5 V) combine with a wide bandwidth of 3 MHz to make this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The TLVx314-Q1 family achieves a low-input bias current of 1 pA, making it an excellent choice for high impedance sensors.

The robust design of the TLVx314-Q1 devices provides ease-of-use to the circuit designer: unity-gain stability, RRIO, capacitive loads of up to 300-pF, an integrated RF and EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and are specified over the extended industrial temperature range of –40°C to +125°C.

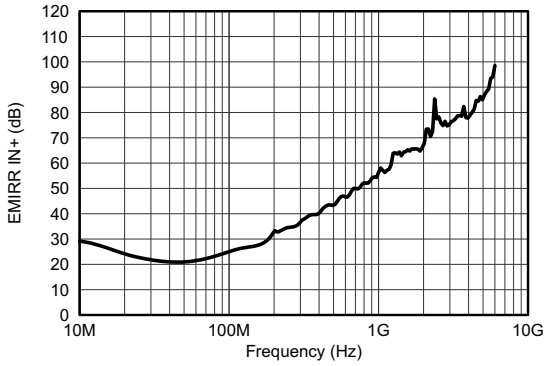
The TLV314-Q1 (single) is available in both 5-pin SC70 and SOT-23 packages. The TLV2314-Q1 (dual) is offered in 8-pin SOIC and VSSOP packages. The quad-channel TLV4314-Q1 is offered in a 14-pin TSSOP package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV314-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
TLV2314-Q1	SOIC (8)	4.90 mm × 3.91 mm
TLV4314-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

EMIRR vs Frequency



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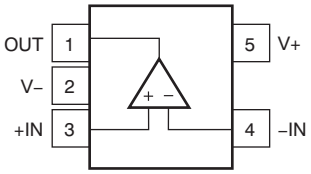
4 Revision History

Changes from Original (November 2016) to Revision A **Page**

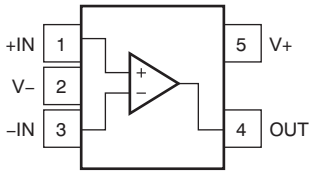
- Deleted TLV2314-Q1 Preview notation in *Device Information* ... 1
- Deleted VSSOP (8) package from *Device Information* ... 1
- Deleted VSSOP package information and preview notation for 8-Pin SOIC in *Pin Functions* ... 4
- Deleted DGK (VSSOP) thermal information ... 7

5 Pin Configuration and Functions

TLV314-Q1 DBV Package
5-Pin SOT-23
Top View



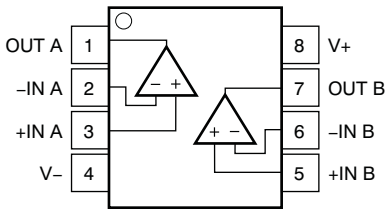
TLV314-Q1 DCK Package
5-Pin SC70
Top View



Pin Functions: TLV314-Q1

PIN			I/O	DESCRIPTION
NAME	DBV (SOT-23)	DCK (SC70)		
–IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	—	Negative (lowest) supply
V+	5	5	—	Positive (highest) supply

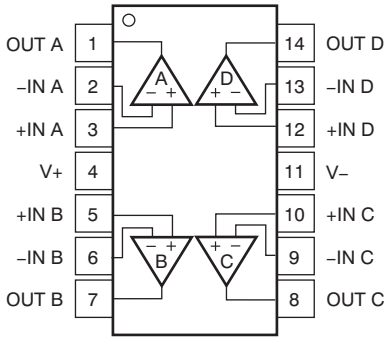
TLV2314-Q1 D Package
8-Pin SOIC
Top View



Pin Functions: TLV2314-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply

TLV4314-Q1 PW Package
14-Pin TSSOP
Top View



Pin Functions: TLV4314-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply
V+	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Supply voltage V_S= (V+) – (V–)			7	V
Signal input pins	Voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		mA
Temperature	Specified, T_A	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	1.8		5.5	V
		Dual-supply	±0.9		±2.75	
	Specified temperature range		–40		125	°C

6.4 Thermal Information: TLV314-Q1

THERMAL METRIC(1)		TLV314-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	281.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	99.1	91.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	59.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	58.8	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

6.5 Thermal Information: TLV2314-Q1

THERMAL METRIC(1)		TLV2314-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	89.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

6.6 Thermal Information: TLV4314-Q1

THERMAL METRIC(1)		TLV4314-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.2	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

6.7 Electrical Characteristics

V_S = 1.8 V to 5.5 V; at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		V_{CM} = (V_S+) – 1.3 V, T_A = 25°C		±0.75	±3	mV
dV_{OS}/dT	V_{OS} vs temperature		T_A = –40°C to +125°C		2		µV/°C
PSRR	Power-supply rejection ratio		V_{CM} = (V_S+) – 1.3 V, T_A = 25°C		±30	±135	µV/V
	Channel separation, dc		At dc, T_A = 25°C		100		dB
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = 25°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio		V_S = 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V, T_A = 25°C	72	96		dB
			V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V(2), T_A = 25°C		75		
INPUT BIAS CURRENT							
I_B	Input bias current		T_A = 25°C		±1.0		pA
I_{OS}	Input offset current		T_A = 25°C		±1.0		pA
NOISE							
	Input voltage noise (peak-to-peak)		f = 0.1 Hz to 10 Hz, T_A = 25°C		5		μV_{PP}
e_n	Input voltage noise density		f = 10 kHz, T_A = 25°C		15		nV/√Hz
			f = 1 kHz, T_A = 25°C		16		
i_n	Input current noise density		f = 1 kHz, T_A = 25°C		6		fA/√Hz
INPUT CAPACITANCE							
C_{IN}	Input capacitance	Differential	V_S = 5 V, T_A = 25°C		1		pF
		Common-mode	V_S = 5 V, T_A = 25°C		5		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		V_S = 1.8 V to 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ, T_A = 25°C	85	115		dB
			V_S = 1.8 V to 5.5 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2), T_A = 25°C	85	100		
	Phase margin		V_S = 5 V, G = 1, R_L = 10 kΩ, T_A = 25°C		65		°
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		V_S = 1.8 V, R_L = 10 kΩ, C_L = 10 pF, T_A = 25°C		2.7		MHz
			V_S = 5 V, R_L = 10 kΩ, C_L = 10 pF, T_A = 25°C		3		
SR	Slew rate(3)		V_S = 5 V, G = 1, T_A = 25°C		1.5		V/µs
t_S	Settling time		To 0.1%, V_S = 5 V, 2-V step , G = 1, T_A = 25°C		3		µs
	Overload recovery time		V_S = 5 V, V_{IN} × gain > V_S, T_A = 25°C		8		µs
THD+N	Total harmonic distortion + noise(4)		V_S = 5 V, V_O = 1 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ, T_A = 25°C		0.005%		
OUTPUT							
V_O	Voltage output swing from supply rails		V_S = 1.8 V to 5.5 V, R_L = 10 kΩ, T_A = 25°C		5	25	mV
			V_S = 1.8 V to 5.5 V, R_L = 2 kΩ, T_A = 25°C		22	45	
I_{SC}	Short-circuit current		V_S = 5 V, T_A = 25°C		±20		mA
R_O	Open-loop output impedance		V_S = 5.5 V, f = 100 Hz, T_A = 25°C		570		Ω
POWER SUPPLY							
V_S	Specified voltage range			1.8		5.5	V
I_Q	Quiescent current per amplifier, over temperature		V_S = 5 V, I_O = 0 mA, T_A = –40°C to +125°C		150	250	µA
TEMPERATURE							
	Specified range			–40		125	°C
T_{stg}	Storage range			–65		150	°C

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.
(3) Signifies the slower value of the positive or negative slew rate.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.

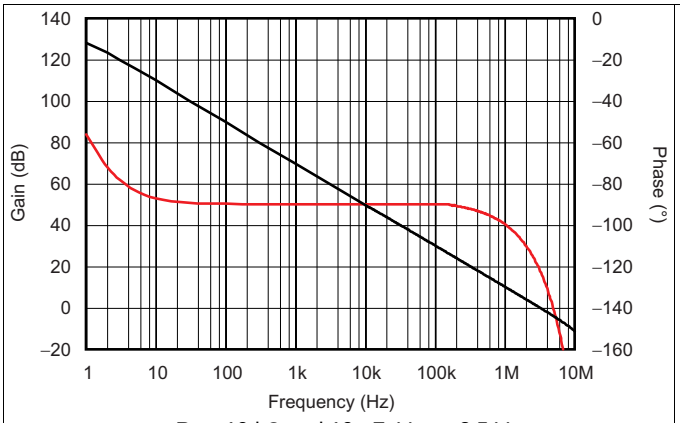
6.8 Typical Characteristics

Table 1. Table of Graphs

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	Figure 1
Quiescent Current vs Supply Voltage	Figure 2
Offset Voltage Production Distribution	Figure 3
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	Figure 4
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	Figure 5
Input Bias and Offset Current vs Temperature	Figure 6
Output Voltage Swing vs Output Current (Overtemperature)	Figure 7
Small-Signal Overshoot vs Load Capacitance	Figure 8
Small-Signal Step Response, Noninverting (1.8 V)	Figure 9
Large-Signal Step Response, Noninverting (1.8 V)	Figure 10
No Phase Reversal	Figure 11
Channel Separation vs Frequency (Dual)	Figure 12
EMIRR	Figure 13

6.9 Typical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



R_L = 10 kΩ and 10 pF, V_S = ±2.5 V

Figure 1. Open-Loop Gain and Phase vs Frequency

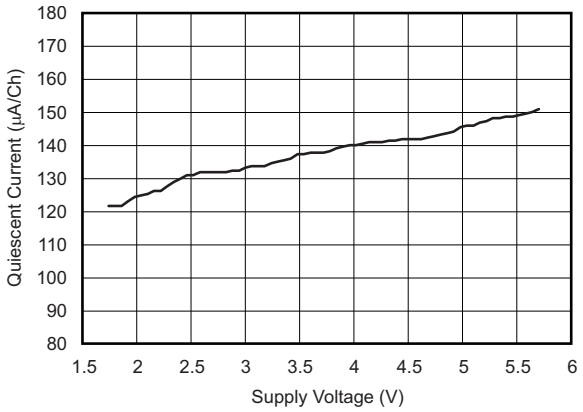


Figure 2. Quiescent Current vs Supply

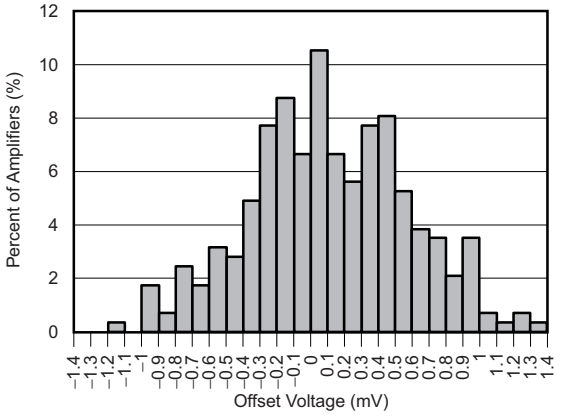
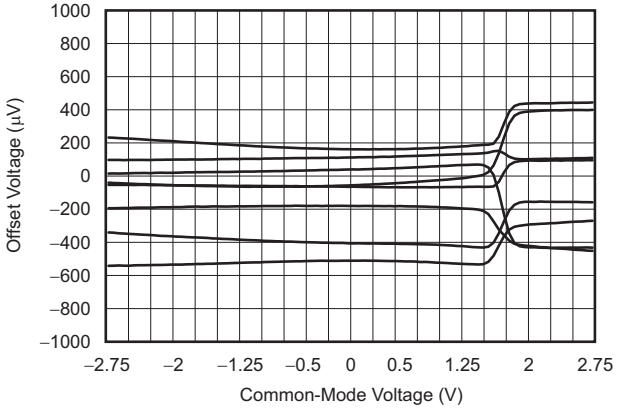


Figure 3. Offset Voltage Production Distribution



Typical units, V_S = ±2.75 V

Figure 4. Offset Voltage vs Common-Mode Voltage

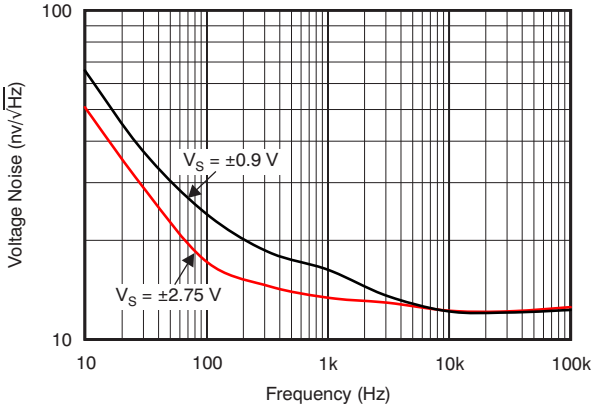


Figure 5. Input Voltage Noise Spectral Density vs Frequency

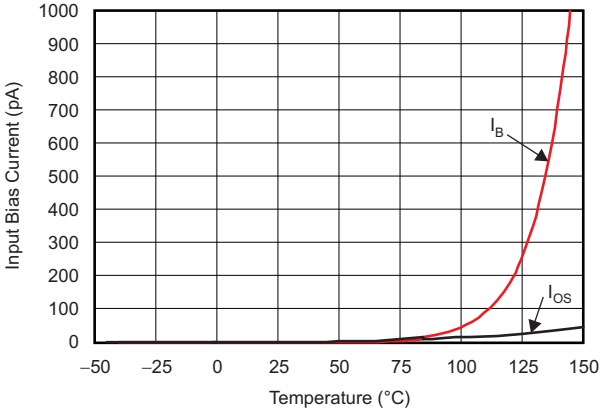
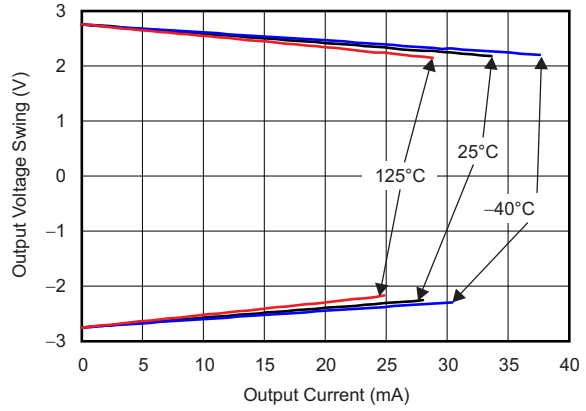


Figure 6. Input Bias and Offset Current vs Temperature

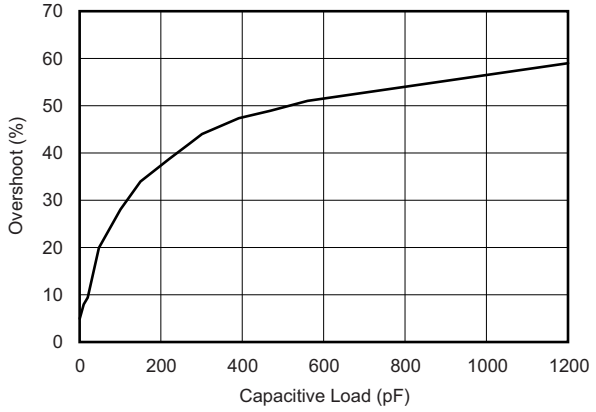
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



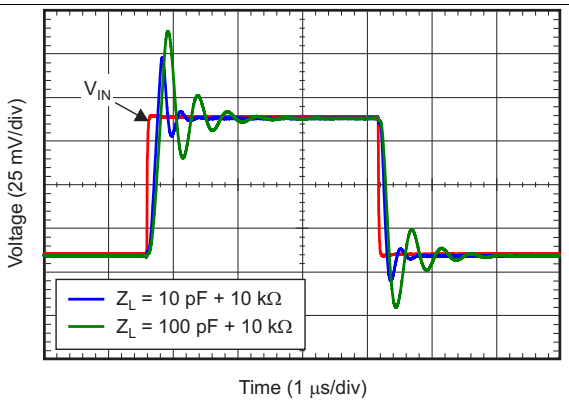
V_S = ±2.75 V

Figure 7. Output Voltage Swing vs Output Current (Overtemperature)



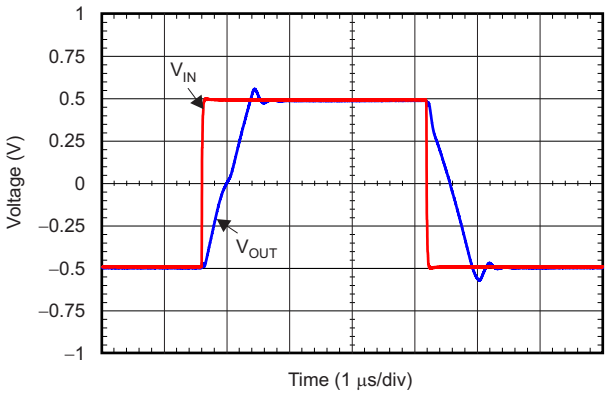
V_S = ±2.75 V Gain = 1 V/V R_L = 10 kΩ

Figure 8. Small-Signal Overshoot vs Load Capacitance



V_S = ±0.9 V Gain = 1 V/V R_F = 10 kΩ

Figure 9. Small-Signal Pulse Response (Noninverting)



V_S = ±0.9 V Gain = 1 V/V R_L = 10 kΩ

Figure 10. Large-Signal Pulse Response (Noninverting)

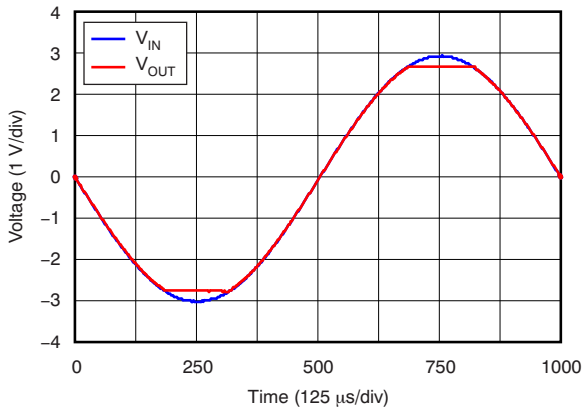
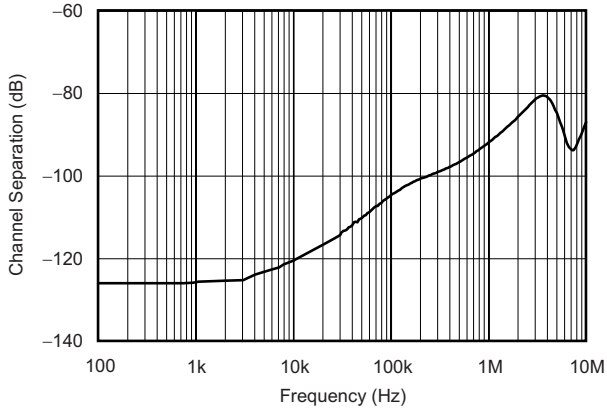


Figure 11. No Phase Reversal

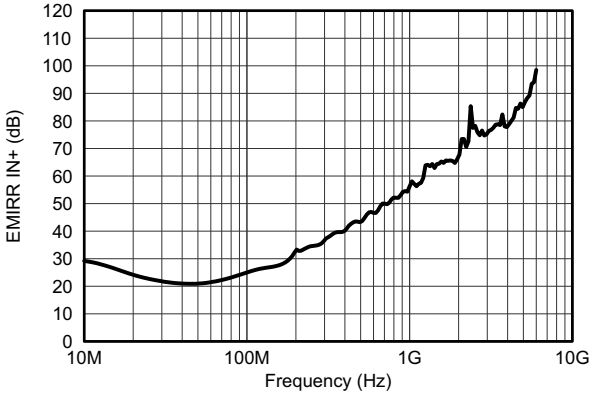


V_S = ±2.75 V

Figure 12. Channel Separation vs Frequency (TLV2314)

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



P_{RF} = –10 dBm V_S = ±2.5 V V_{CM} = 0 V

Figure 13. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency

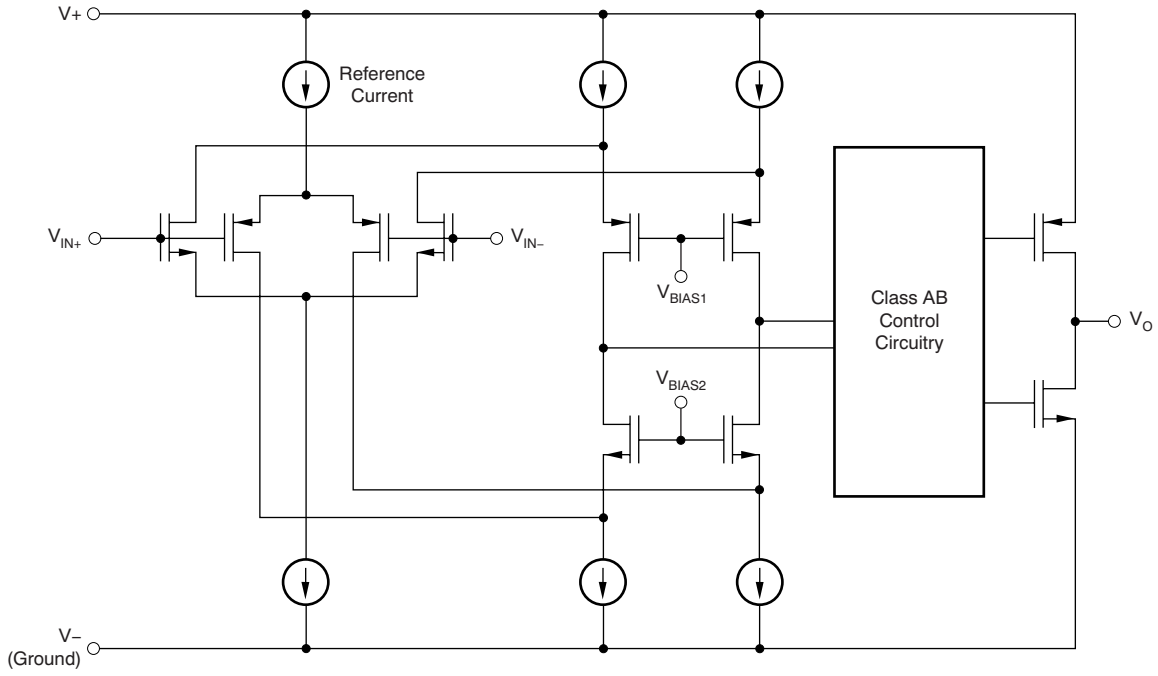
7 Detailed Description

7.1 Overview

The TLVx314-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the TLVx314-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx314-Q1 family features 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good ac performance at very-low-power consumption. DC applications are also well served with a very low input noise voltage of 14 nV / √Hz at 1 kHz, low input bias current (0.2-pA), and a typical input offset voltage of 0.5 mV.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLVx314-Q1 series of operational amplifiers is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics* section. Bypass power-supply pins with 0.01-μF ceramic capacitors.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLVx314-Q1 extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (with both stages on) ranges from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

7.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLVx314-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads up to 10-kΩ, the output typically swings to within 5 mV of either supply rail regardless of the applied power-supply voltage . Different load conditions change the ability of the amplifier to swing close to the rails, as shown in Figure 7.

7.3.4 Common-Mode Rejection Ratio (CMRR)

The CMRR for the TLVx314-Q1 is specified in several ways so the best match for a given application can be used; see the *Electrical Characteristics* table. First, the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations measured through the transition region, as shown in Figure 4.

Feature Description (continued)

7.3.5 Capacitive Load and Stability

The TLVx314-Q1 is designed for applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLVx314-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLVx314-Q1 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L capacitors with a value greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop so the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains, as shown in Figure 8.

Inserting a small resistor (typically 10-Ω to 20-Ω) can increase the capacitive load drive of the amplifier in a unity-gain configuration, as shown in Figure 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

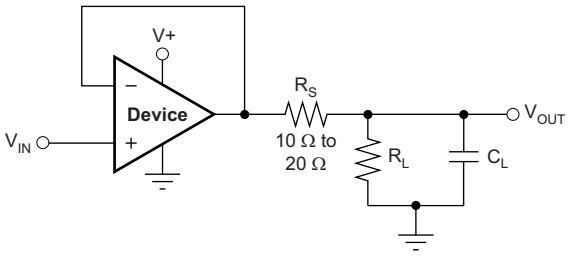


Figure 14. Improving Capacitive Load Drive

7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from the nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the signal input pins are likely to be the most susceptible. The TLVx314-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. The filter provides common-mode and differential mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared to the EMI immunity. Figure 13 illustrates the testing results on the TLVx314-Q1. For more detailed information, see *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

7.4 Device Functional Modes

The TLVx314-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLVx314-Q1 device is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the TLVx314-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx314-Q1 features a 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good ac performance at very-low-power consumption. DC applications are also well served with a very-low input noise voltage of 14 nV/√Hz at 1 kHz, low-input bias current (0.2 pA), and a typical input offset voltage of 0.5 mV.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 15. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor (R_I) and the feedback resistor (R_F).

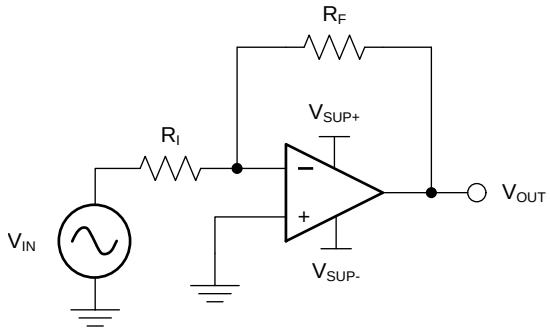


Figure 15. Application Schematic

8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Calculate the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Typical Application (continued)

When the desired gain is determined, select a value for R_I or R_F. Selecting a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (hundreds of kilohms) draw the smallest current, but generate the highest noise. Very small resistors (hundreds of ohms) generate low noise but draw high current. This example uses 10 kΩ for R_I, and R_F uses 36 kΩ. These values are calculated using Equation 3:

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

8.2.3 Application Curve

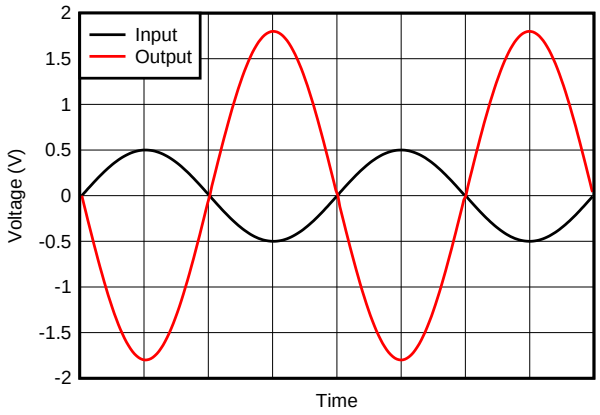


Figure 16. Inverting Amplifier Input and Output

8.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as Figure 17 shows.

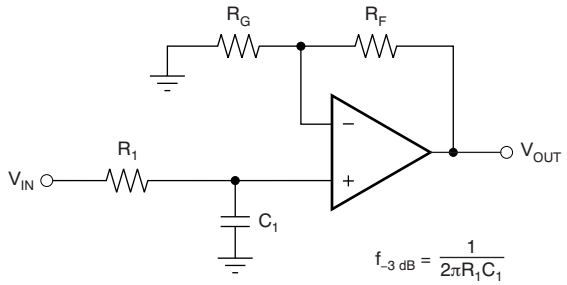


Figure 17. Single-Pole, Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as Figure 18 shows. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

System Examples (continued)

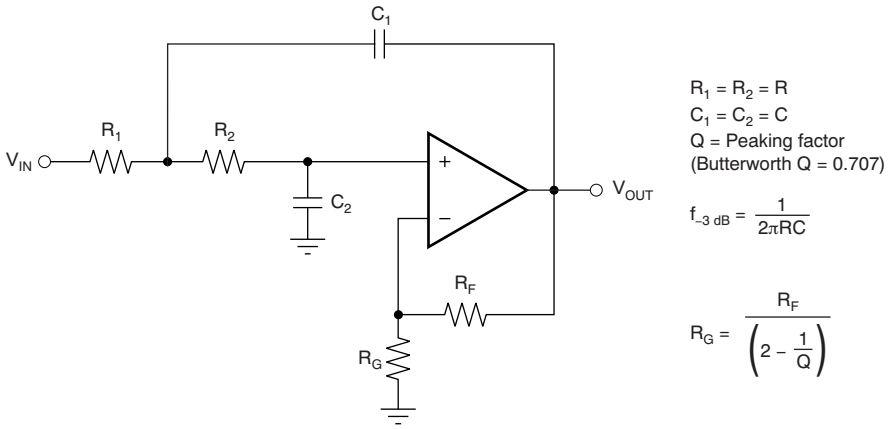


Figure 18. Two-Pole, Low-Pass, Sallen-Key Filter

9 Power Supply Recommendations

The TLVx314-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see *Layout Guidelines*.

9.1 Input and ESD Protection

The TLVx314-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the *Absolute Maximum Ratings* table. Figure 19 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input, which must be kept to a minimum in noise-sensitive applications.

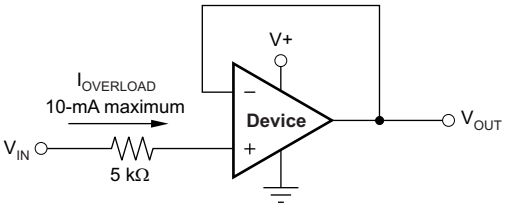


Figure 19. Input Current Protection

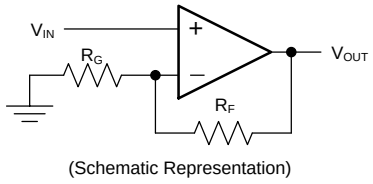
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input in order to minimize parasitic capacitance, as shown in Figure 20.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



(Schematic Representation)

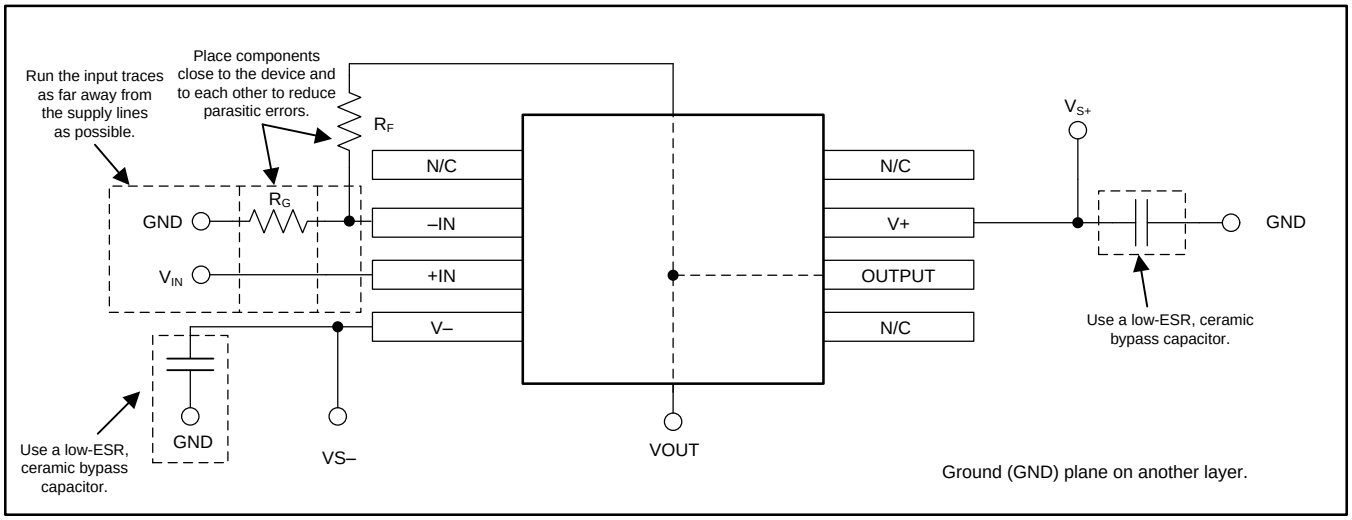


Figure 20. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers* (SBOA128).
- *Circuit Board Layout Techniques* (SLOA089).
- *QFN/SON PCB Attachment* (SLUA271).
- *Quad Flatpack No-Lead Logic Packages* (SCBA017).

11.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV314-Q1	Click here	Click here	Click here	Click here	Click here
TLV2314-Q1	Click here	Click here	Click here	Click here	Click here
TLV4314-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2314QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2314Q	Samples
TLV314QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16SD	Samples
TLV314QDBVTQ1	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16SD	Samples
TLV4314QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V4314Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2314-Q1, TLV314-Q1, TLV4314-Q1 :

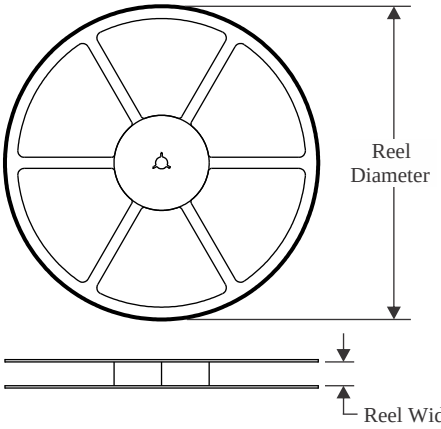
- Catalog: TLV2314, TLV314, TLV4314

NOTE: Qualified Version Definitions:

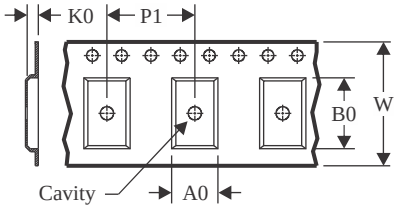
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

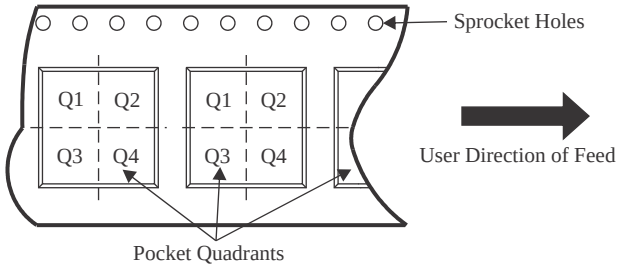


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

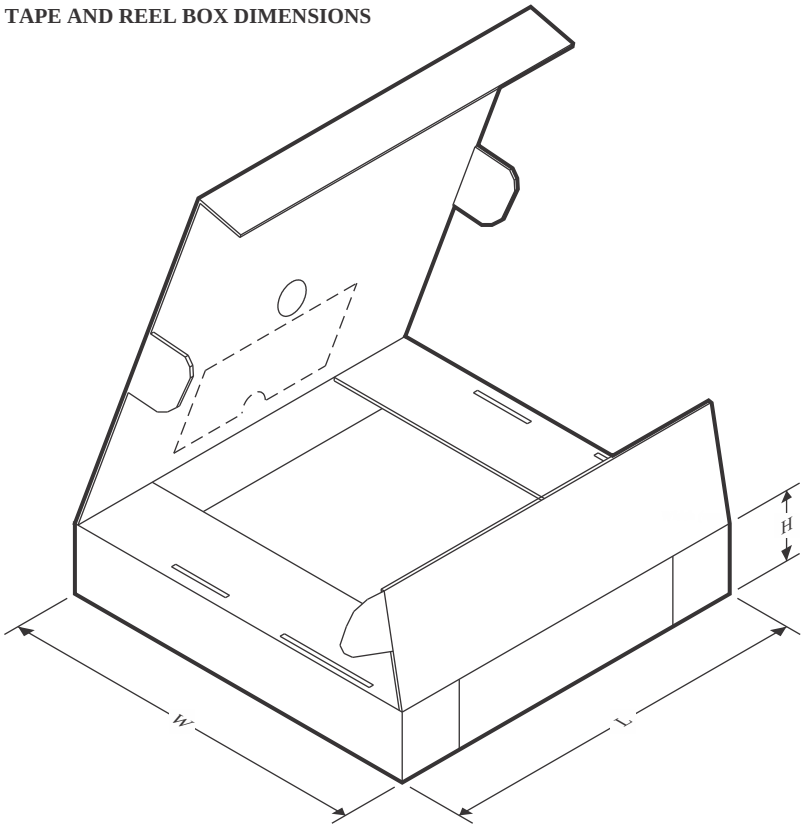
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2314QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV314QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV314QDBVTQ1	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV4314QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

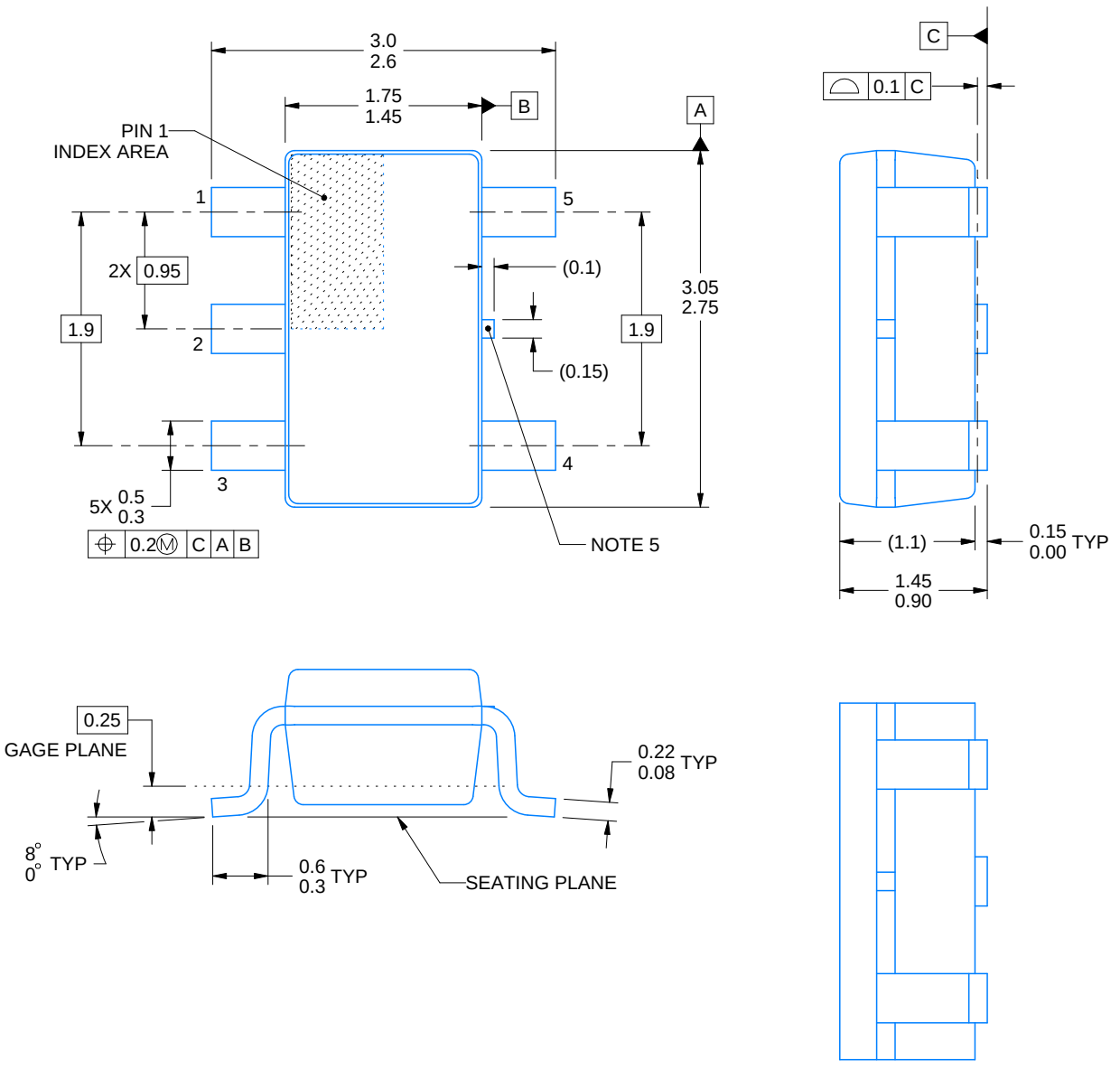
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2314QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TLV314QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV314QDBVTQ1	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV4314QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

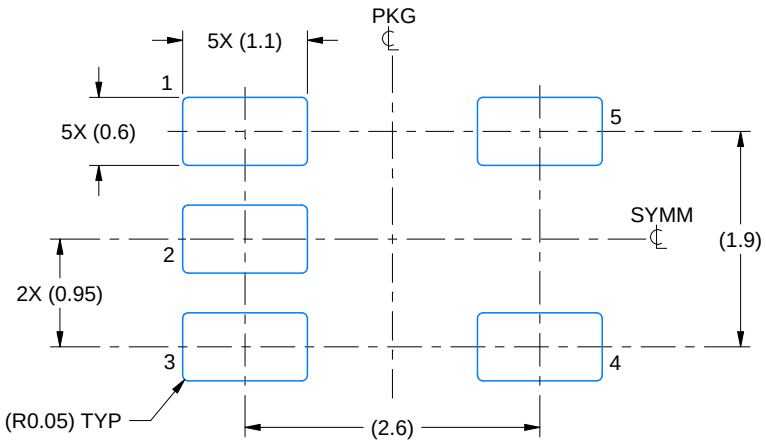


ALTERNATIVE PACKAGE SINGULATION VIEW

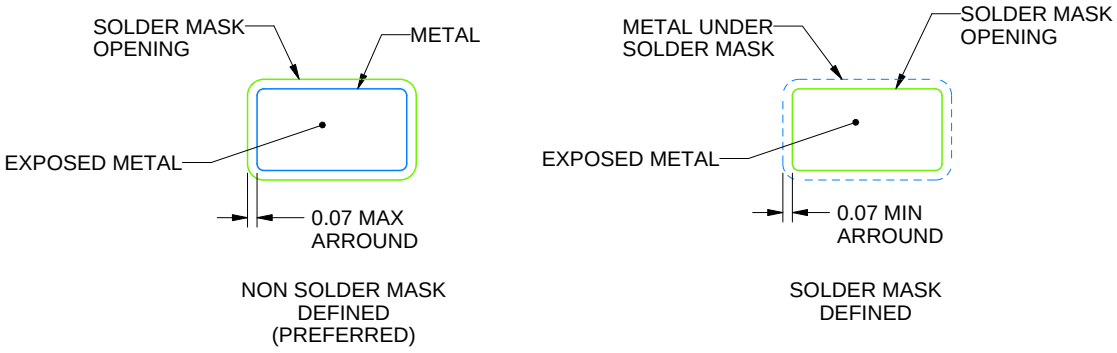
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

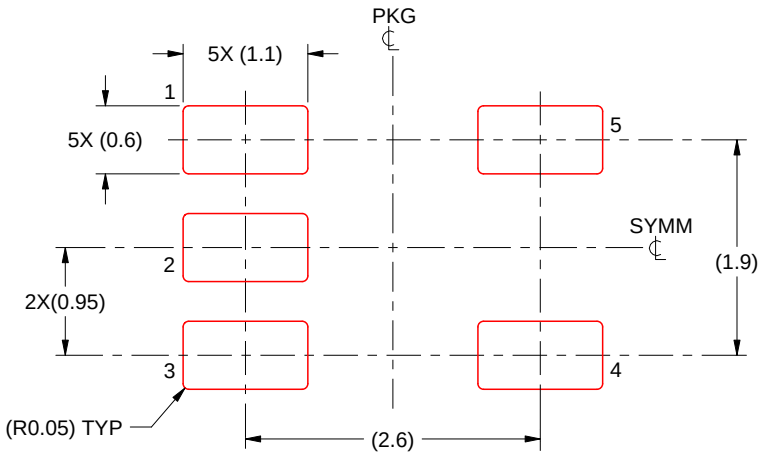


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



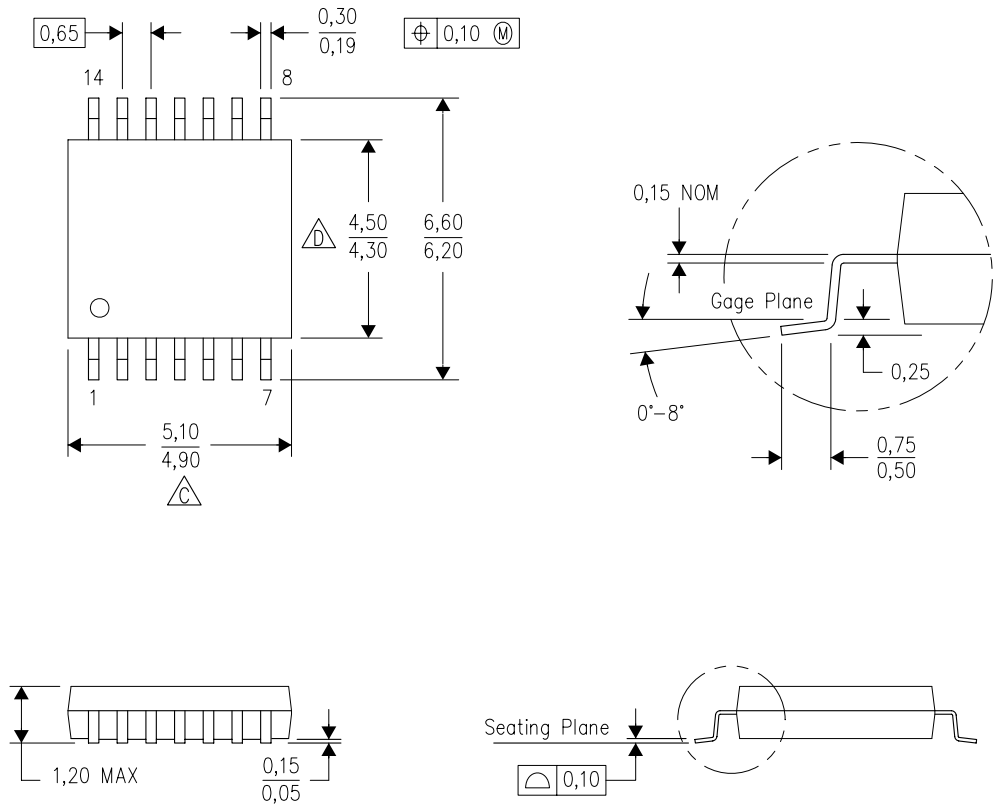
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

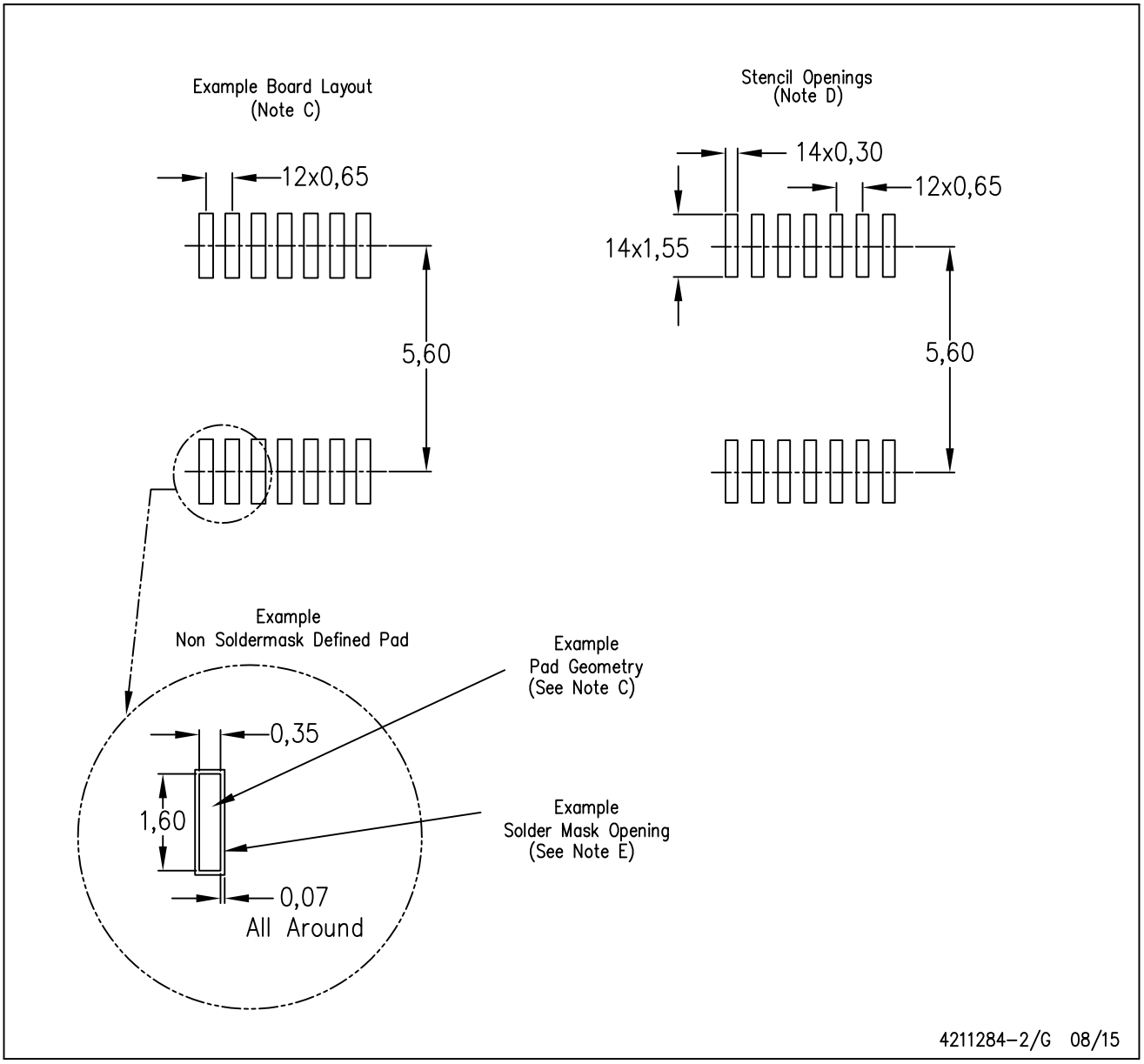
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



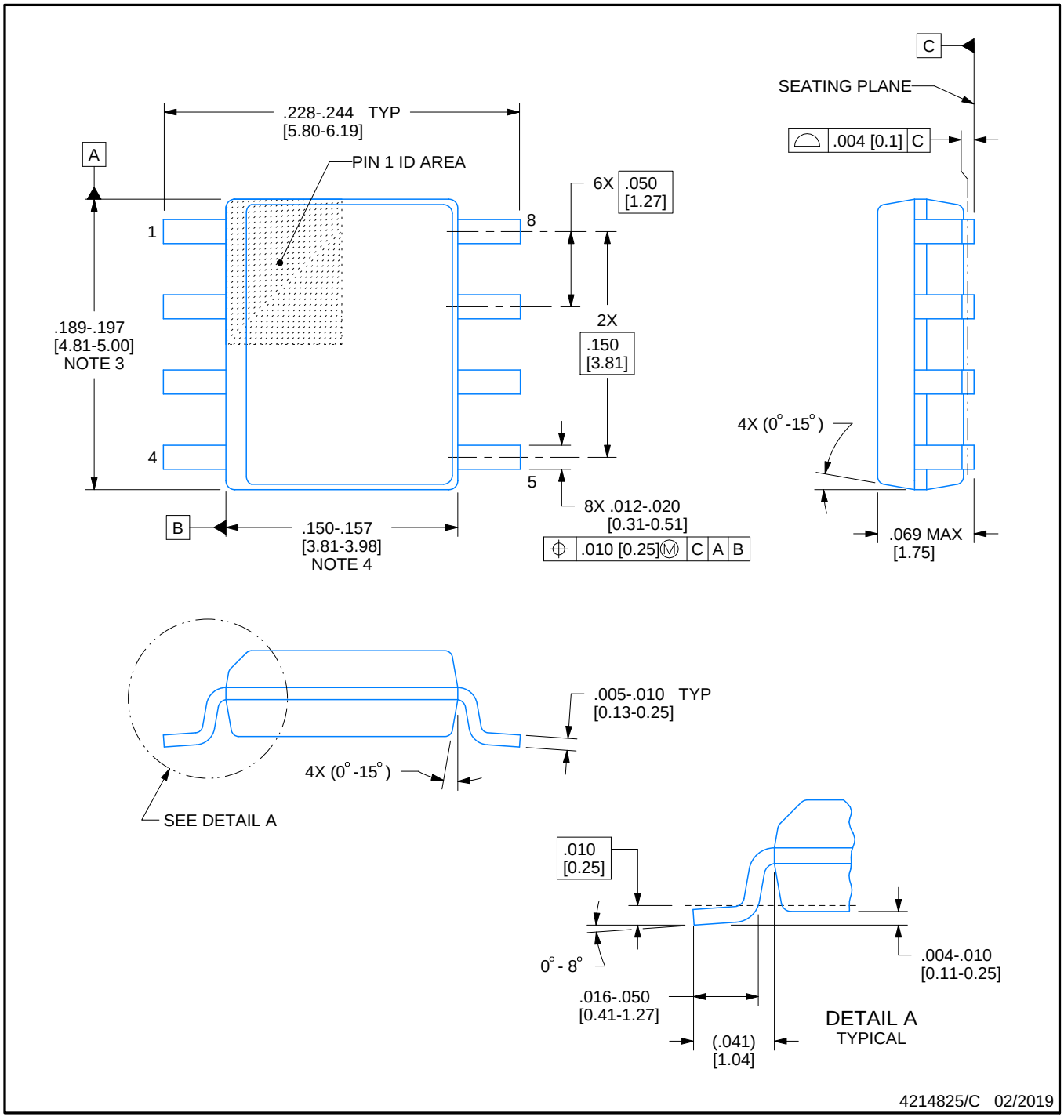
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

D0008A

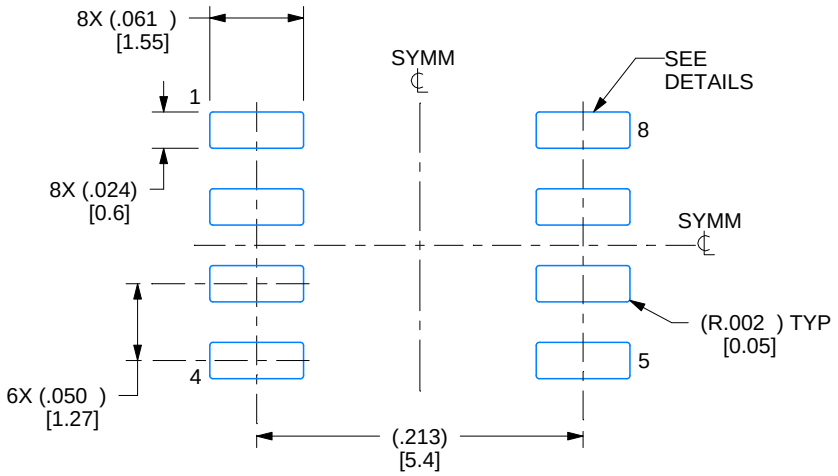
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

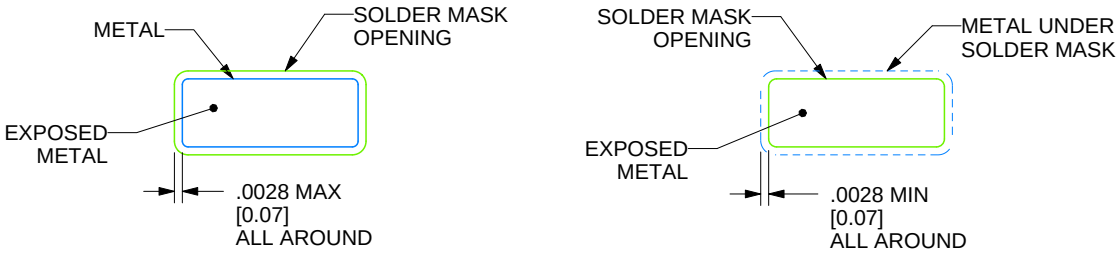


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

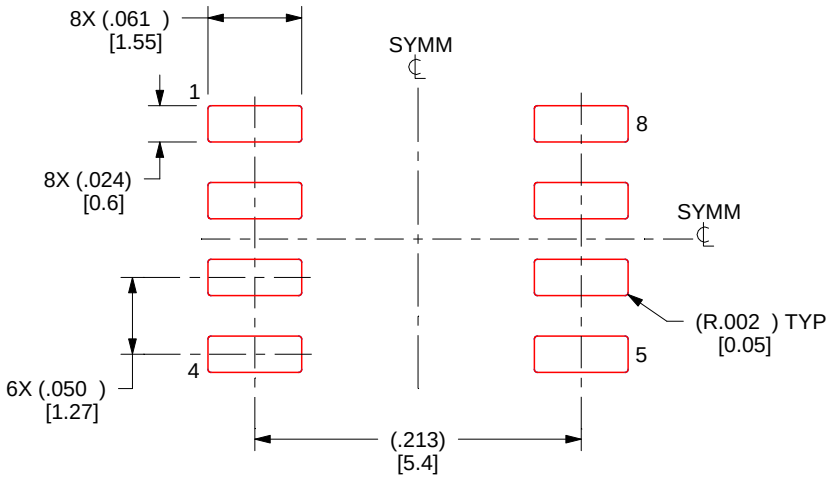
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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