36V，单电源，SOT553，通用运算放大器价值线系列

查询样品: OPA171, OPA2171, OPA4171

特性

- 电源范围：**+2.7V** 至 **+36V**，**±1.35V** 至 **±18V**
- 低噪声：**14 nV/√Hz**
- 低偏移漂移：**0.3μV/°C**（典型值）
- 已过滤的射频干扰 **(RFI)** 输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨至轨输出
- 增益带宽：**3MHz**
- 低静态电流：每个放大器 **475μA**
- 高共模抑制：**120dB**（典型值）
- 低输入偏压电流：**8pA**
- 行业标准封装：
  - **8** 引脚小外形尺寸集成电路 **(SOIC)** 封装
  - **8** 引脚微型小外形尺寸 **(MSOP)** 封装
  - **14** 引脚薄型小外形尺寸 **(TSSOP)** 封装
- *微型*封装：
  - **SOT553** 封装内为单通道
  - **VSSOP-8** 封装内为双通道

应用范围

- 电源模块内的跟踪放大器
- 商用电源
- 变频器放大器
- 桥式放大器
- 温度测量
- 应力计放大器
- 精密积分器
- 电池供电仪器
- 测试设备

产品系列

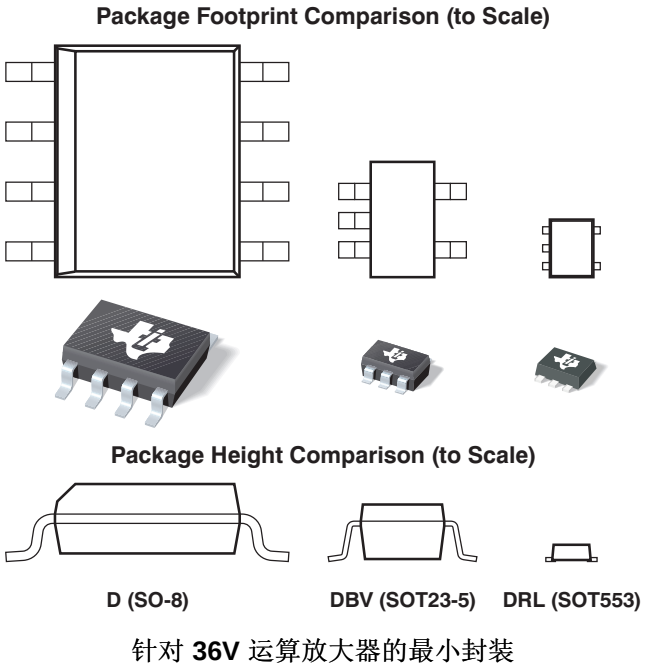
器件	封装
OPA171	**SOT553**，**SOT23-5**，小外形尺寸 **(SO)-8**
OPA2171（双通道）	**VSSOP-8**，**SO-8**，**MSOP-8**
OPA4171（四通道）	**TSSOP-14**，**SO-14**

说明

OPA171，OPA2171 和 OPA4171 (OPAx171) 是系列 36V，单电源，低噪声运算放大器，此系列运算放大器能够在 +2.7V (±1.35V) 至 +36V (±18V) 的电源范围内运行。 这个器件采用微型封装并且在保证低静态电流的情况下提供低偏移、漂移和带宽。 单通道、双通道和四通道版本均具有相同的技术规格，可最大程度地提高设计灵活性。

与大多数只有一个额定电源电压的运算放大器不同，OPAx171 的额定电压范围为 +2.7V 至 +36V。 超过电源轨的输入信号不会导致相位反转。 OPAx171 系列在电容负载高达 300pF 时保持稳定。 输入可在负电源轨以下 100mV 以及正电源轨 2V 之内正常运行。 请注意，这些器件可在正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨 2V 之内运行时性能会受到影响。

OPAx171 系列运算放大器额定运行温度范围为 -40°C 至 +125°C。



针对 **36V** 运算放大器的最小封装

这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

封装/订购信息 (1)

产品	封装-引线	封装 指示符	封装 标记	订购号	运输介质、数量
OPA171	SOT 553	DRL	DAP	OPA171AIDRLT	卷带封装，250
				OPA171AIDRLR	卷带封装，4000
	小外形尺寸晶体管封装 (SOT) 23-5	DBV	OSUI	OPA171AIDBVT	卷带封装，250
				OPA171AIDBVR	卷带封装，3000
	SO-8	D	O171A	OPA171AID	电源轨，75
				OPA171AIDR	卷带封装，2500
OPA2171	MSOP-8	DGK	OPMI	OPA2171AIDGK	电源轨，80
				OPA2171AIDGKR	卷带封装，2500
	VSSOP-8	DCU	OPOC	OPA2171AIDCUT	卷带封装，250
				OPA2171AIDCUR	卷带封装，3000
	SO-8	D	2171A	OPA2171AID	电源轨，75
				OPA2171AIDR	卷带封装，2500
OPA4171	SO-14	D	OPA4171	OPA4171AID	电源轨，50
				OPA4171AIDR	卷带封装，2500
	TSSOP-14	PW	OPA4171	OPA4171AIPW	电源轨，90
				OPA4171AIPWR	卷带封装，2000

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问www.ti.com上的器件产品文件夹。

最大绝对额定值(1)

在自然通风温度范围内运行测得，除非另有说明。

		OPAx171	单位
电源电压		±20	V
信号输入端子	电压	(V-)-0.5 至 (V+)+0.5	V
	电流	±10	mA
输出短路(2)		连续	
工作温度		-55 至 +150	°C
存储温度		-65 至 +150	°C
结温		+150	°C
ESD 额定值：	人体模型 (HBM)	4	kV
	充电器件模型 (CDM)	750	V

(1) 超过这些额定值的应力有可能造成永久损坏。 长时间处于最大绝对额定情况下会降低设备的可靠性。 这些只是应力额定值，在这些值或者任何超过那些所标明的条件下的功能运行并未注明。

(2) 短路至接地，每封装一个放大器。

电气特性

黑体字应用在额定温度范围上的限值，**T_A=-40°C 至 +125°C**。
在 T_A=+25°C 时，V_S=+2.7V 至 +36V，V_{CM}=V_{OUT}=V_S/2，并且 R_{LOAD}=10kΩ 被连接至 V_S/2，除非另外注明。

参数		测试条件	OPA171，OPA2171，OPA4171 最小值	典型值	最大值	单位
偏移电压						
输入偏移电压	V_{OS}			0.25	±1.8	mV
温度范围内				**0.3**	**±2**	**mV**
漂移	**dV_{OS}/dT**			**0.3**	**±2**	**µV/°C**
与电源的关系	**电源抑制比 (PSRR)**	**V_S=+4V 至 +36V**		**1**	**±3**	**µV/V**
通道分离，直流		DC		5		µV/V
输入偏置电流						
输入偏置电流	I_B			±8	±15	pA
在温度范围内					**±3.5**	**nA**
输入偏移电流	I_{OS}			±4		pA
在温度范围内					**±3.5**	**nA**
噪声						
输入电压噪声		f=0.1Hz 至 10Hz		3		μV_{PP}
输入电压噪声密度	e_n	f=100Hz		25		nV/√Hz
		f=1kHz		14		nV/√Hz
输入电压						
共模电压范围(1)	V_{CM}		(V-)-0.1V		(V+)-2V	V
共模抑制比	**CMRR**	**V_S=±2V，(V-)-0.1V<V_{CM} <(V+)-2V**	**90**	**104**		**dB**
		V_S=±18V，(V-)-0.1V<V_{CM}<(V+)-2V	**104**	**120**		**dB**
输入阻抗						
差分				100 || 3		MΩ || pF
共模				6 || 3		10^{12}Ω || pF
开环增益						
开环电压增益	**A_{OL}**	**V_S=+4V 至 +36V，(V-)+0.35V<V_O<(V+)-0.35V**	**110**	**130**		**dB**
频率响应						
带宽增益产品	GBP			3.0		MHz
电压转换速率	SR	G=+1		1.5		V/µs
稳定时间	t_S	到 0.1%，V_S=±18V，G=+1，10V 阶跃时的稳定时间		6		µs
		到 0.01%（12 位），V_S =±18V，G=+1，10V 阶跃时的稳定时间		10		µs
过载恢复时间		V_{IN} × 增益 > V_S		2		µs
总谐波失真+噪声	THD+N	G=+1，f=1kHz，V_O=3V_{RMS}		0.0002		%
输出的*输出*部分将自电源轨参数的电压输出摆幅改为温度范围内的电压输出摆幅						
自电源轨的电压输出摆幅	V_O	V_S=5V，R_L=10kΩ		30		mV
在温度范围内		**R_L=10kΩ，A_{OL}≥110dB**	**(V-)+0.35**		**(V+)-0.35**	**V**
短路电流	I_{SC}			+25/–35		mA
电容负载驱动	C_{LOAD}			请见 典型特点		pF
开环输出电阻	R_O	f=1MHz，I_O=0A		150		Ω
电源						
额定电压范围	V_S		+2.7		+36	V
每个放大器的静态电流	I_Q	I_O=0A		475	595	µA
温度范围内		**I_O=0A**			**650**	**µA**
温度						
额定温度			-40		+125	°C
工作范围			-55		+150	°C

(1) 输入范围可被扩展超过 (V+)-2V，最高到 V+。 附件信息请见*典型特征*和*应用信息*。

热性能信息：OPA171

热度量(1)		OPA171			单位
		D (SO)	DBV (SOT23)	DRL (SOT553)	
		8 引脚	5 引脚	5 引脚	
θ_{JA}	结到环境热阻	149.5	245.8	208.1	°C/W
$\theta_{JC(top)}$	结至芯片外壳（顶部）热阻	97.9	133.9	0.1	
θ_{JB}	结至电路板热阻	87.7	83.6	42.4	
ψ_{JT}	结至顶部的特征参数	35.5	18.2	0.5	
ψ_{JB}	结至电路板的特征参数	89.5	83.1	42.2	
$\theta_{JC(bottom)}$	结至芯片外壳（底部）热阻	不可用	不可用	不可用	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

热性能信息：OPA2171

热度量(1)		OPA2171			单位
		D (SO)	DCU (VSSOP)	DGK (MSOP)	
		8 引脚	8 引脚	8 引脚	
θ_{JA}	结到环境热阻	134.3	175.2	195.3	°C/W
$\theta_{JC(top)}$	结至芯片外壳（顶部）热阻	72.1	74.9	59.4	
θ_{JB}	结至电路板热阻	60.6	22.2	115.1	
ψ_{JT}	结至顶部的特征参数	18.2	1.6	4.7	
ψ_{JB}	结至电路板的特征参数	53.8	22.8	114.4	
$\theta_{JC(bottom)}$	结至芯片外壳（底部）热阻	不可用	不可用	不可用	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

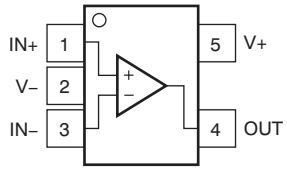
热性能信息：OPA4171

热度量(1)		OPA4171		单位
		D (SO)	PW (TSSOP)	
		14 引脚	14 引脚	
θ_{JA}	结到环境热阻	93.2	106.9	°C/W
$\theta_{JC(top)}$	结至芯片外壳（顶部）热阻	51.8	24.4	
θ_{JB}	结至电路板热阻	49.4	59.3	
ψ_{JT}	结至顶部的特征参数	13.5	0.6	
ψ_{JB}	结至电路板的特征参数	42.2	54.3	
$\theta_{JC(bottom)}$	结至芯片外壳（底部）热阻	不可用	不可用	

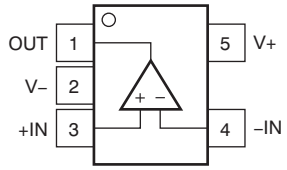
(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

引脚配置

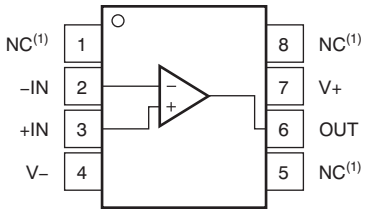
DRL 封装：OPA171
SOT-553
（顶视图）



DBV 封装：OPA171
小外形尺寸晶体管封装 (SOT) 23-5
（顶视图）

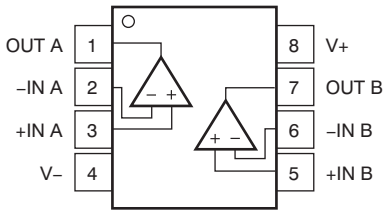


D 封装：OPA171
SO-8
（顶视图）

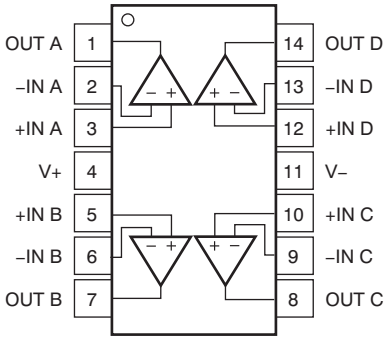


(1) 无内部连接。

D，DCU 和 DGK 封装：OPA2171
SO-8，VSSOP-8，和 MSOP-8
（顶视图）



D 和 PW 封装：OPA4171
SO-14 和 TSSOP-14
（顶视图）



典型特征

Table 1. 特征性能测量

说明	图表
偏移电压产品分布	Figure 1
偏移电压漂移分布	Figure 2
偏移电压与温度间的关系	Figure 3
偏移电压与共模电压间的关系	Figure 4
偏移电压与共模电压间的关系（前级）	Figure 5
偏移电压与电源间的关系	Figure 6
I_B 和 I_{OS}与共模电压间的关系	Figure 7
输入偏置电流与温度的关系	Figure 8
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通道分离与频率间的关系	Figure 36

典型特征

V_S=±18V，V_{CM}=V_S/2，R_{LOAD}=10kΩ 被连接至 V_S/2，和 C_L=100pF，除非另外注明。

偏移电压产品分布

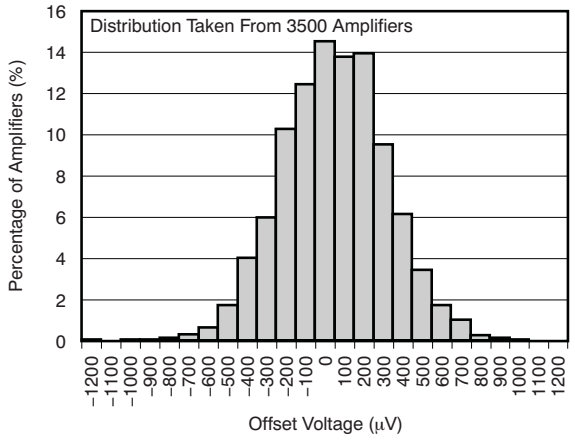


Figure 1.

偏移电压漂移分布

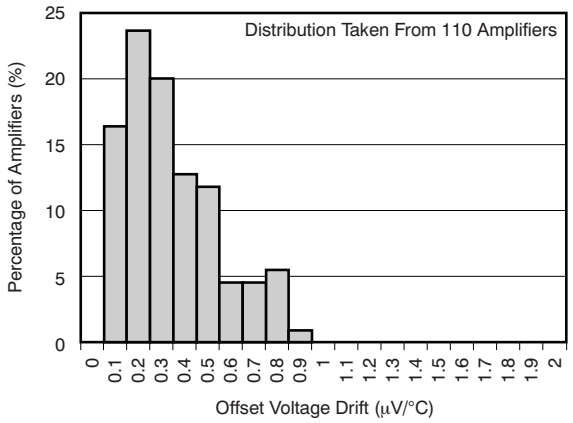


Figure 2.

偏移电压与温度间的关系

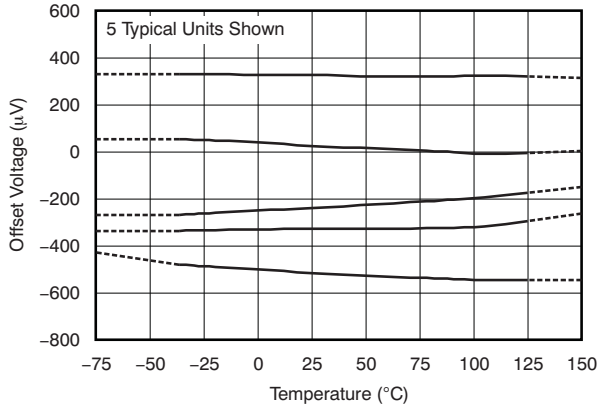


Figure 3.

偏移电压与共模电压间的关系

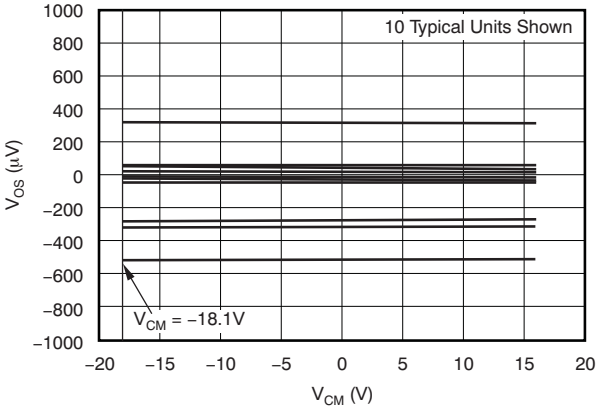


Figure 4.

偏移电压与共模电压
（前级）

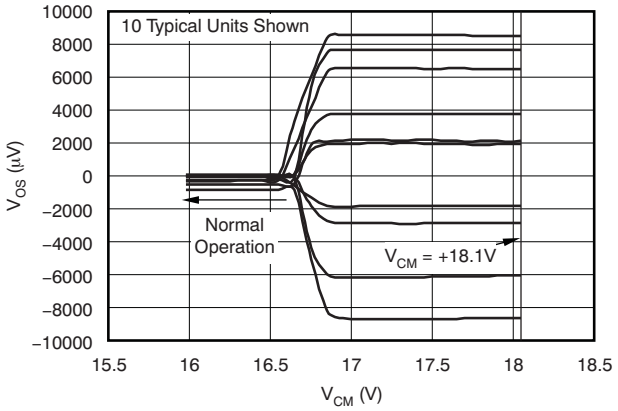


Figure 5.

偏移电压与电源间的关系

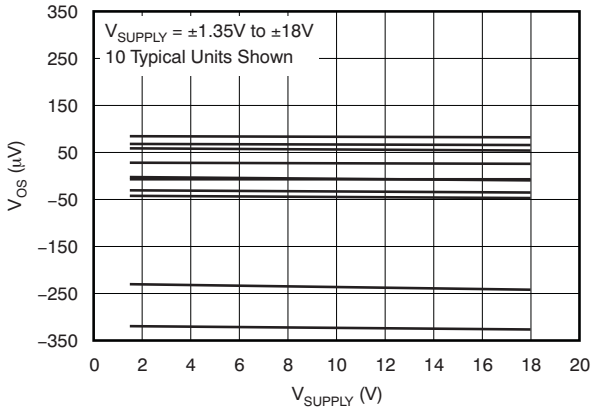


Figure 6.

典型特征 (continued)

V_S=±18V，V_{CM}=V_S/2，R_{LOAD}=10kΩ 被连接至 V_S/2，和 C_L=100pF，除非另外注明。

I_B 和 I_{OS}与共模电压间的关系

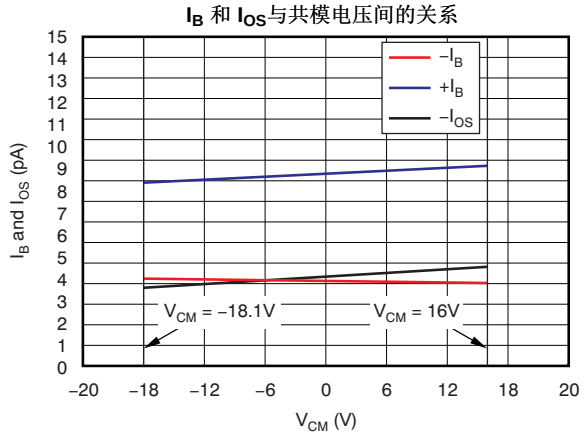


Figure 7.

输入偏置电流与温度间的关系

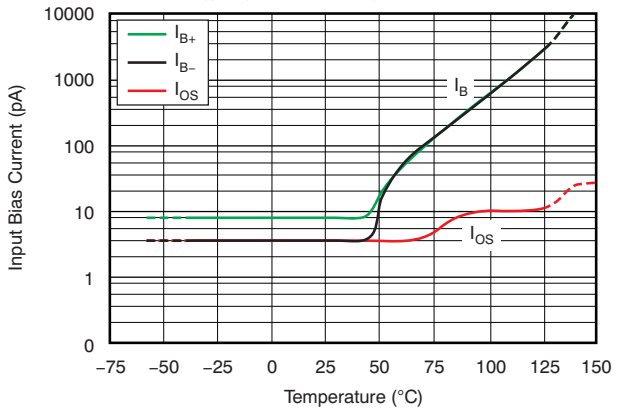


Figure 8.

输出电压摆幅与输出电流间的关系
（最大电源）

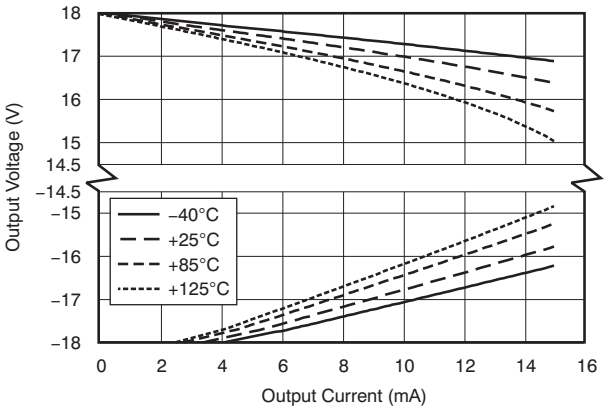


Figure 9.

CMRR 和 PSRR 与频率间的关系
（以输入为基准）

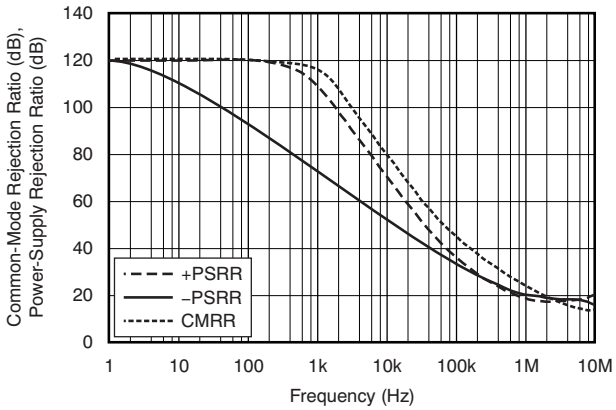


Figure 10.

CMRR 与温度间的关系

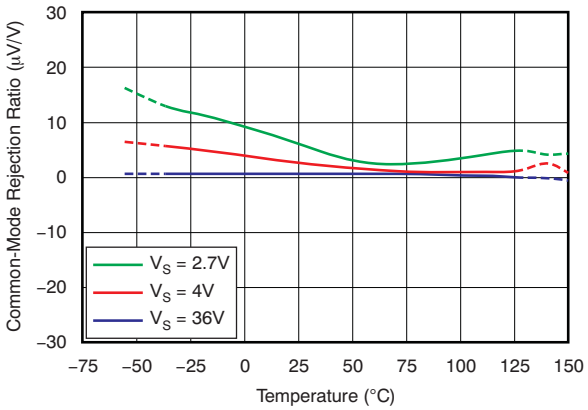


Figure 11.

PSRR 与温度间的关系

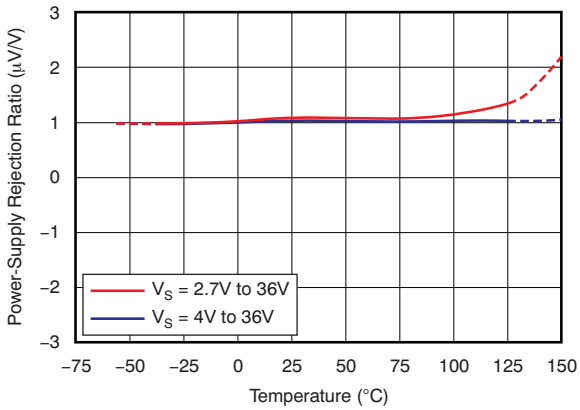


Figure 12.

典型特征 (continued)

V_S=±18V，V_{CM}=V_S/2，R_{LOAD}=10kΩ 被连接至 V_S/2，和 C_L=100pF，除非另外注明。

0.1Hz 至 10Hz 噪声

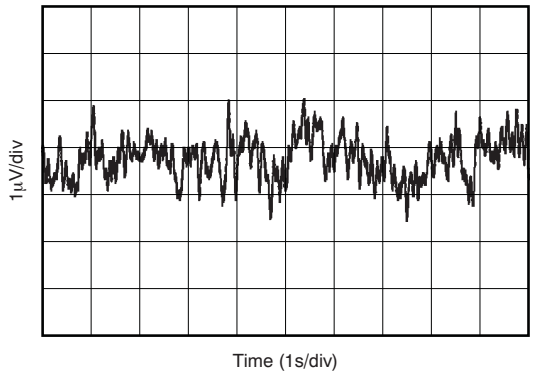


Figure 13.

输入电压噪声频谱密度与频率间的关系

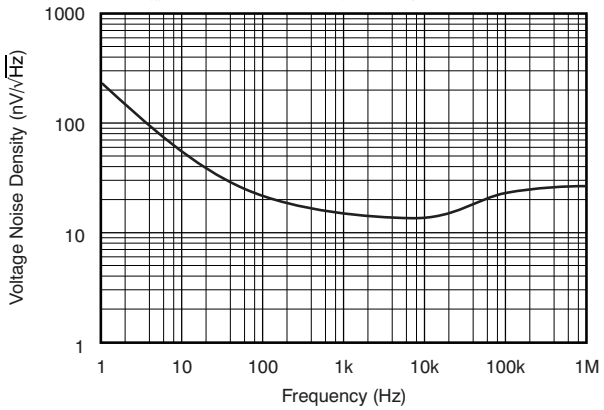


Figure 14.

THD+N 比与频率间的关系

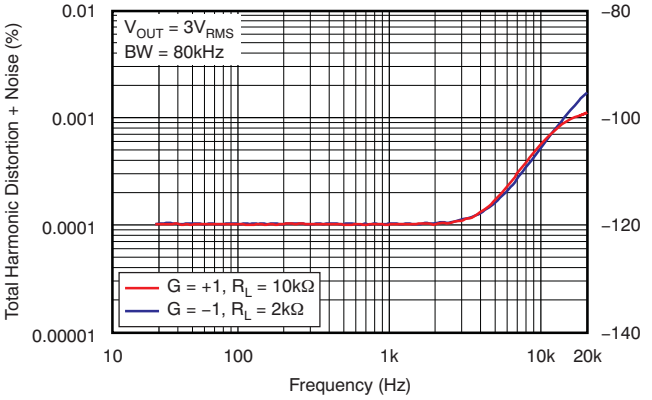


Figure 15.

THD+N 与输出摆幅间的关系

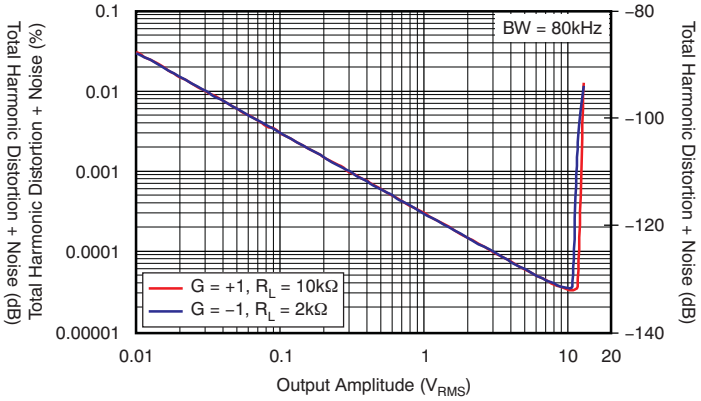


Figure 16.

静态电流与温度间的关系

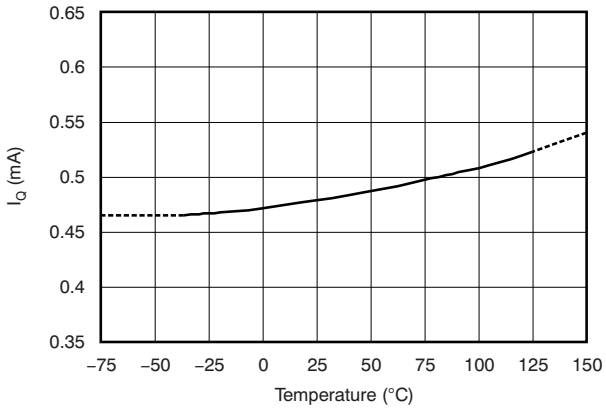


Figure 17.

静态电流与电源电压间的关系

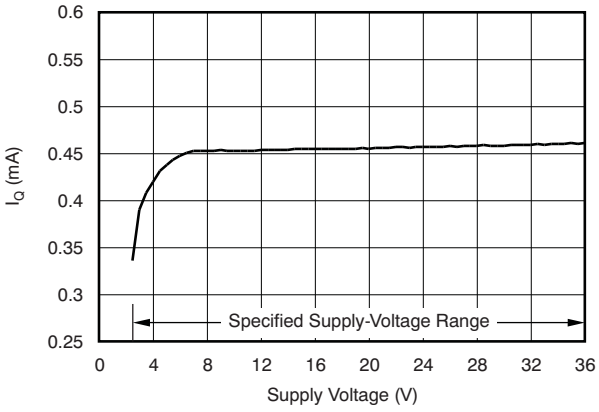


Figure 18.

典型特征 (continued)

V_S=±18V，V_{CM}=V_S/2，R_{LOAD}=10kΩ 被连接至 V_S/2，和 C_L=100pF，除非另外注明。

开环增益和相位与频率间的关系

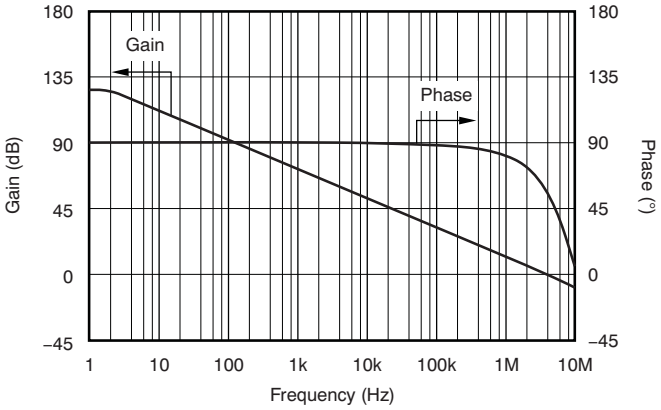


Figure 19.

闭环增益与频率间的关系

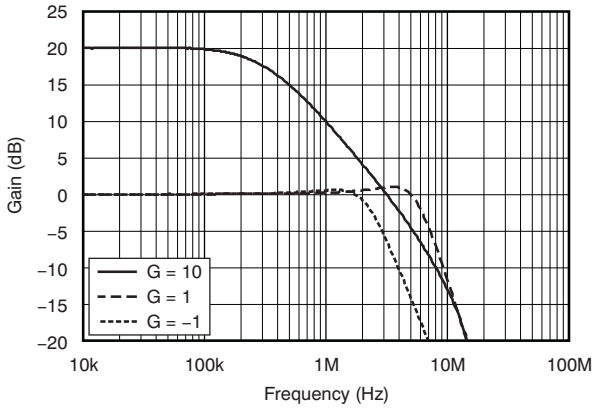


Figure 20.

开环增益与温度间的关系

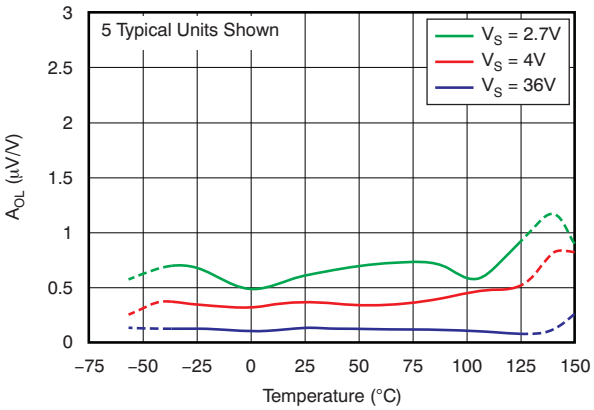


Figure 21.

开环输出阻抗与频率间的关系

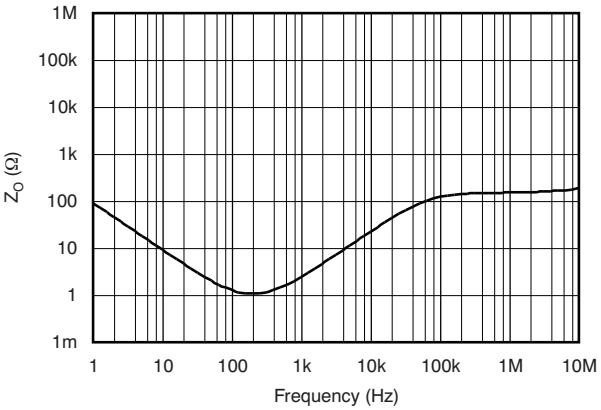


Figure 22.

小信号过冲与电容负载间的关系
（**100mV** 输出阶跃）

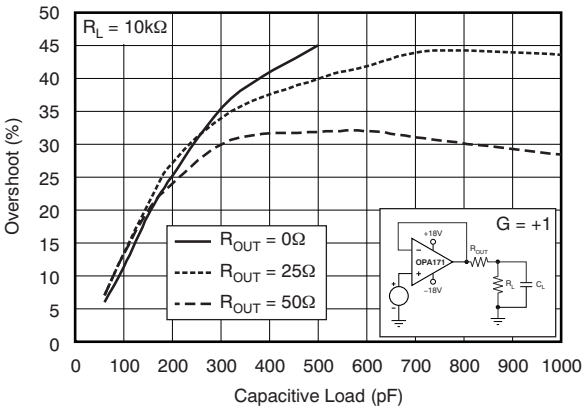


Figure 23.

小信号过冲与电容负载间的关系
（**100mV** 输出阶跃）

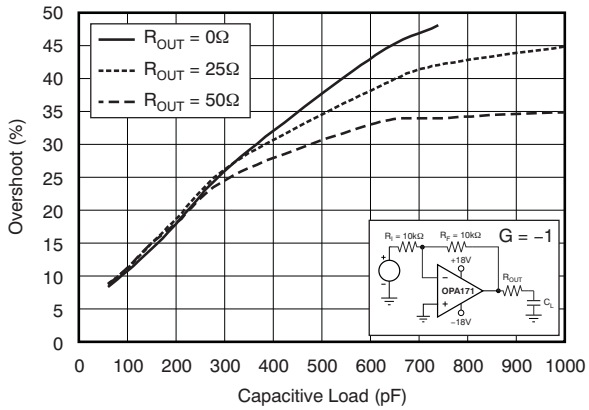


Figure 24.

典型特征 (continued)

V_S=±18V，V_{CM}=V_S/2，R_{LOAD}=10kΩ 被连接至 V_S/2，和 C_L=100pF，除非另外注明。

无相位反转

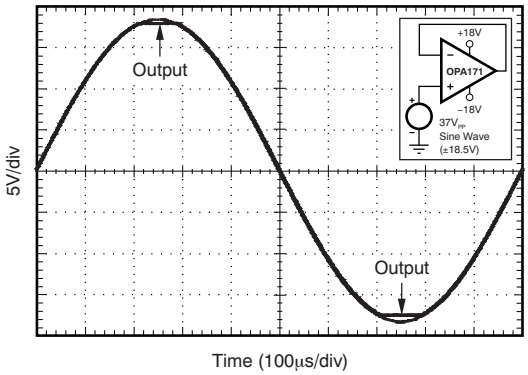


Figure 25.

正过载恢复

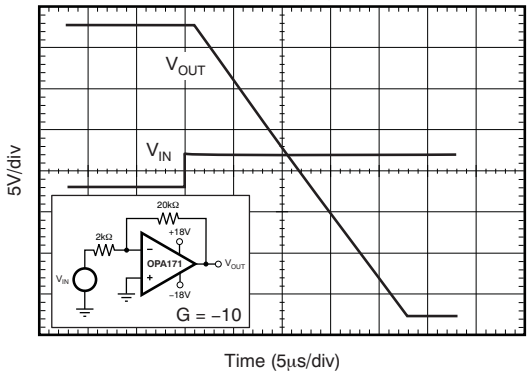


Figure 26.

负过载恢复

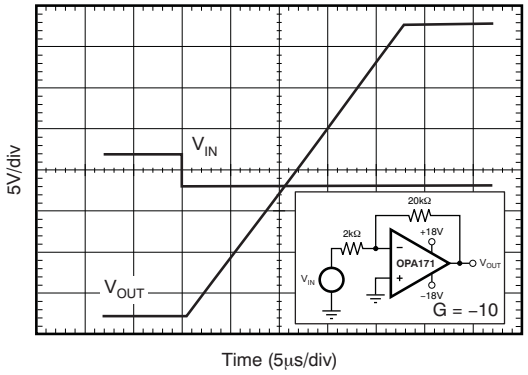


Figure 27.

小信号阶跃响应
(100mV)

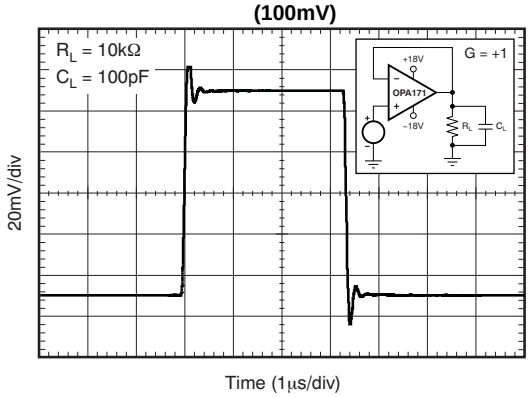


Figure 28.

小信号阶跃响应
(100mV)

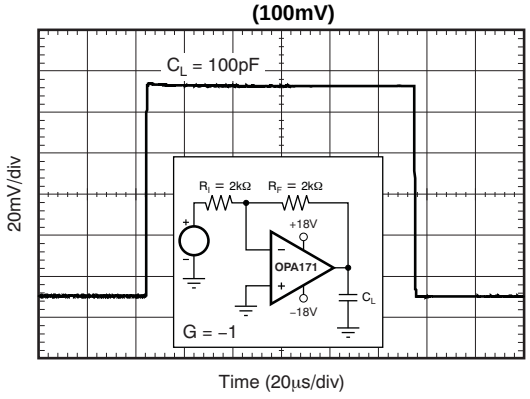


Figure 29.

大信号阶跃响应

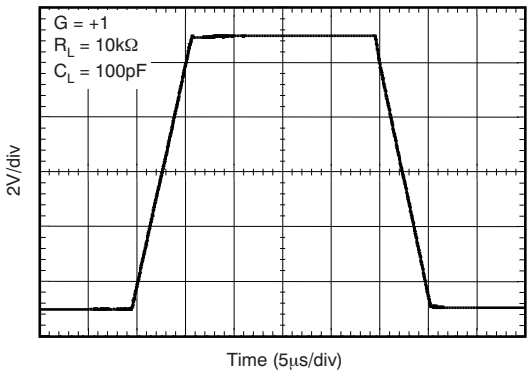


Figure 30.

典型特征 (continued)

V_S=±18V，V_{CM}=V_S/2，R_{LOAD}=10kΩ 被连接至 V_S/2，和 C_L=100pF，除非另外注明。

大信号阶跃响应

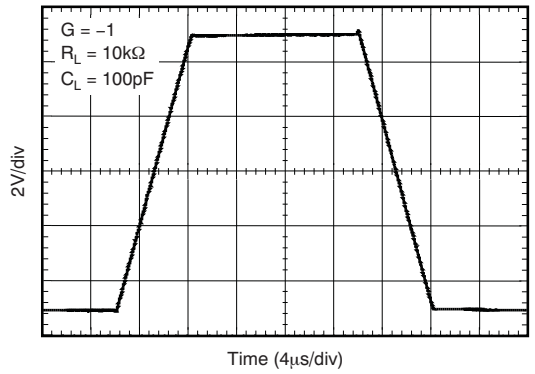


Figure 31.

大信号稳定时间
（**10V** 正阶跃）

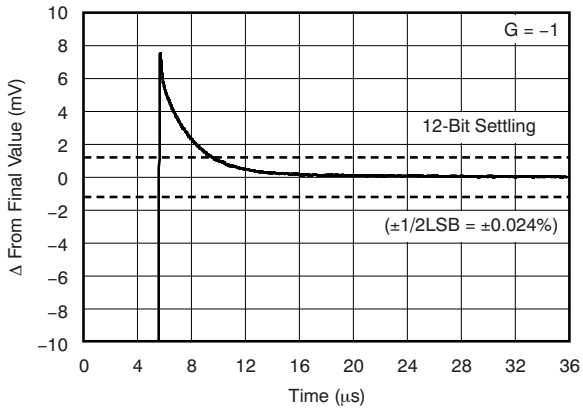


Figure 32.

大信号稳定时间
（**10V** 负阶跃）

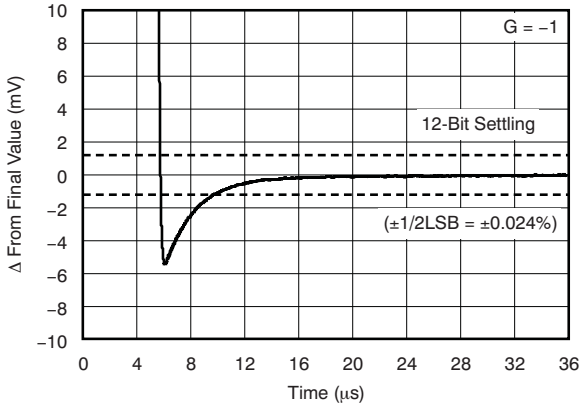


Figure 33.

短路电流与温度间的关系

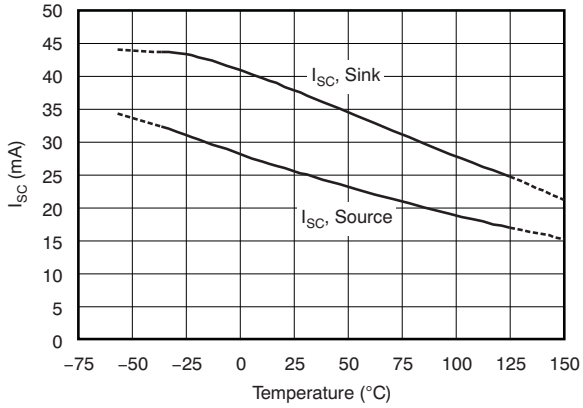


Figure 34.

最大输出电压与频率间的关系

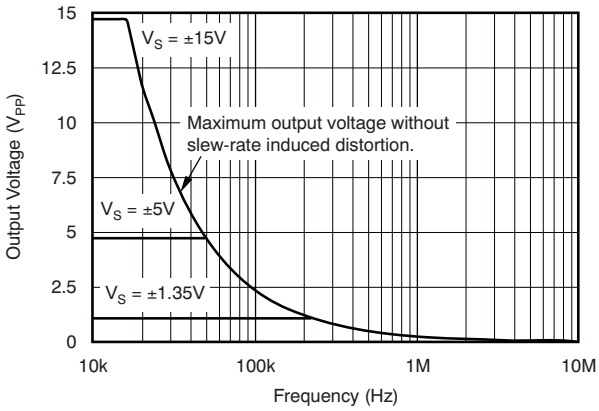


Figure 35.

通道分离与频率间的关系

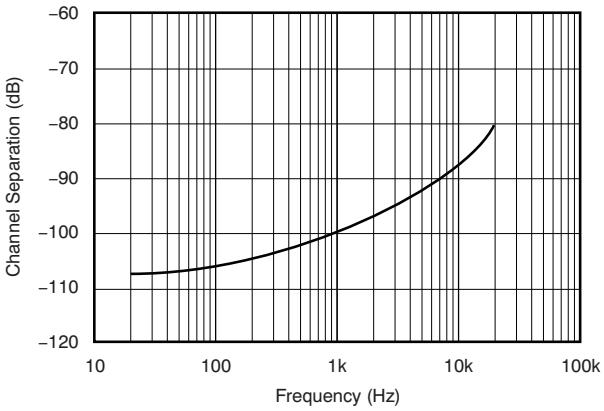


Figure 36.

应用信息

OPAx171 系列运算放大器提供较高的总体性能，从而非常适合于很多通用应用。 只有 2μV/°C 的出色偏移漂移在整个温度范围内提供极佳的稳定性。 此外，此器件提供具有高 CMRR，PSRR 和A_{OL}的极佳性能。与所有放大器一样，具有嘈杂或者高阻抗电源的应用需要放置在靠近器件引脚的去耦合电容器。 在大多数情况下，0.1μF 已足够满足需求。

工作特性

OPAx171 系列放大器额定运行电压介于 2.7V 与 36V（±1.35V 至 ±18V）之间。 大多数技术规格在 -40°C 至 +125°C 温度范围内适用。 会随工作电压或温度发生明显变化的参数显示在 典型特征中。

常用布局布线指南

为了实现器件的最佳运算性能，建议使用设计合理的印刷电路板 (PCB) 布局布线做法。 低损耗，0.1μF 旁路电容器应该被连接在每个电源引脚和接地之间，尽可能地靠近器件。 一个从 V+ 到接地的单一旁路电容器适用于单电源应用。

共模电压范围

为了实现正常运转，OPAx171 系列的输入共模电压范围向下扩展至低于负电源轨 100mV 并且在正电源轨上下 2V 之内。

这个器件可在正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨上下 2V 之内运行时性能会受到影响。 Table 2中汇总了这个范围内的典型性能。

相位反转保护

OPAx171 系列有一个内部相位反转保护。 当输入被驱动至超过其线性共模范围时，很多运算放大器表现出一个相位反转。 这个情况经常出现在输入被驱动至超过额定共模电压范围的时候，从而导致输出反向进入相对的电源轨。 OPAx171 的输入用额外的共模电压来防止相位反转。 或者，输出限制至适当的电源轨。Figure 37中显示了这个性能。

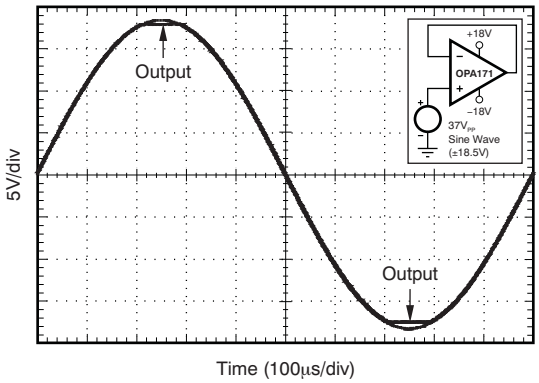


Figure 37. 无相位反转

Table 2. 无相位反转

参数	最小值	典型值	最大值	单位
输入共模电压	**(V+)-2**		**(V+)+0.1**	**V**
偏移电压		7		mV
与温度间的关系		**12**		**μV/°C**
共模抑制		65		dB
开环增益		60		dB
GBW		0.7		MHz
电压转换速率		0.7		V/μs
f=1kHz 时的噪声		30		nV/√Hz

电容负载和稳定性

已针对常见工作条件对 OPAx170 的动态特征进行了优化。 低闭环增益和高电容负载的组合减少了放大器的相位裕量并可导致增益泄漏或振荡。 因此，必须将更高的电容负载从输出上隔离开。 实现此隔离的最简单方法就是增加一个与输出串联的小电阻器（例如，等于 50Ω 的 R_{OUT}）。Figure 38和Figure 39图示了小信号过冲与电容负载间针对几个 R_{OUT}值的关系图。 此外，详细分析技巧和应用电路请参考应用期刊 AB-028 (*SBOA015*)，此文件可从 TI 网站内下载。

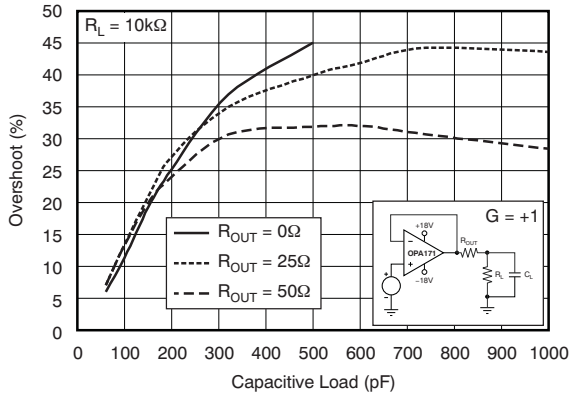


Figure 38. 小信号过冲与电容负载间的关系（**100mV** 输出阶跃）

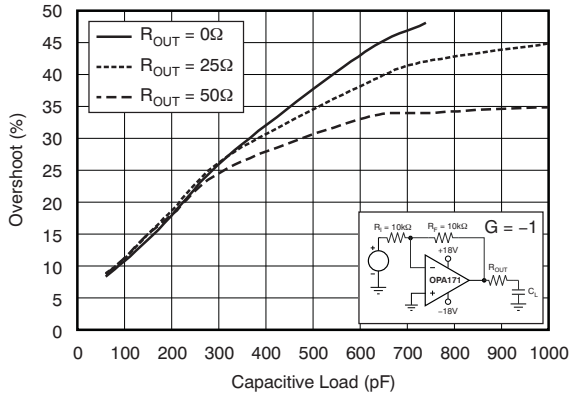


Figure 39. 小信号过冲与电容负载间的关系（**100mV** 输出阶跃）

电气过应力

设计人员经常会问到关于运算放大器耐受电气过应力的能力的问题。 这些问题往往侧重于器件输入，但是却常常涉及到电源电压引脚
。

或者甚至涉及输出引脚。 这些不同引脚功能的每一个功能具有由独特的半导体制造工艺和连接到引脚的特定电路确定的电气应力限值。 此外，这些电路有内置的内部静电放电 (ESD) 保护来在产品组装之前和组装过程中保护此电路不受意外的 ESD 事件的影响。

只要电流如 绝对最大额定值中所述被限制在 10mA，这些 ESD 保护二极管还提供电路内、输入过驱保护。Figure 40显示了一个可被添加到被驱动输入上来限制输入电流的串联输入电阻器。 这个被添加的电阻器会增加放大器输入上的热噪声，而在噪声敏感应用中需要将它的值保持在最小水平上。

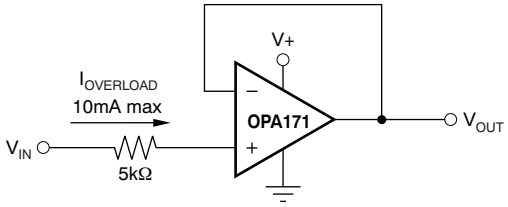


Figure 40. 输入电流保护

一个 ESD 事件产生一个持续时间短、高电压脉冲，此脉冲在它经半导体器件放电时被转变成一个持续时间短、高电流脉冲。 ESD 保护电路被设计成用来运算放大器周围的电流路径来防止其被损坏。 然后此保护电路吸收的能量以发热的形式被散发出来。

当运算放大器连接到一个电路时，ESD 保护组件将保持在未激活状态并且不会参与应用电路运行。 然而，当施加的电压超过一个指定引脚的工作电压范围时，问题情况有可能会出现。 如果这个情况出现，会存在一定的风险，某些内部 ESD 保护电路有可能被偏置而传导电流。 此类电流都由 ESD 单元产生并且很少涉及吸收器件。

如果不能确定电源对于这个电流的吸收能力，可将齐纳二极管添加到电源引脚上。 此齐纳二极管的电压是可选的，这样二极管就不会在正常运行期间打开。

然而，它的齐纳二极管电压应该足够低，这样才能使这个齐纳二极管在电源引脚电压开始上升到高于安全工作电源电压电平时导通。

修订历史记录

注意：前一修订版的页码可能与当前版本的页码不同。

Changes from Revision C (June 2011) to Revision D **Page**

- 在标题中增加了“价值线系列” 1

Changes from Revision B (November 2010) to Revision C **Page**

- 在器件图中添加了 MSOP-8 封装 1
- 在特性着重号中添加了 MSOP-8 封装 1
- 在产品系列表中添加了 MSOP-8 封装 1
- 在封装/订购信息表中增加了 MSOP-8 封装 2
- 从封装/订购信息表中的 OPA4171 封装标记中删除了后缀‘A’ 2
- 增加了自电源轨参数的电压输出摆幅行到电气特性的*输出*部分 3
- 在电气特性 3
- Updated format of thermal information tables 4
- Added MSOP-8 package to OPA2171 Thermal Information table 4
- 更新了针对 OPA2171 和 OPA4171 的引脚分配配置 5
- 已更改Figure 9 8

Changes from Revision A (November, 2010) to Revision B **Page**

- Changed 输入偏移电压技术规格 3
- Changed 输入偏移电压，在温度技术规格内 3
- Changed 每个放大器的静态电流，温度技术规格范围内 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA171AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A	Samples
OPA171AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI	Samples
OPA171AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI	Samples
OPA171AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A	Samples
OPA171AIDRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP	Samples
OPA171AIDRLT	ACTIVE	SOT-5X3	DRL	5	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP	Samples
OPA2171AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A	Samples
OPA2171AIDCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC	Samples
OPA2171AIDCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC	Samples
OPA2171AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPMI	Samples
OPA2171AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	OPMI	Samples
OPA2171AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A	Samples
OPA4171AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171	Samples
OPA4171AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171	Samples
OPA4171AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171	Samples
OPA4171AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA171, OPA2171, OPA4171 :

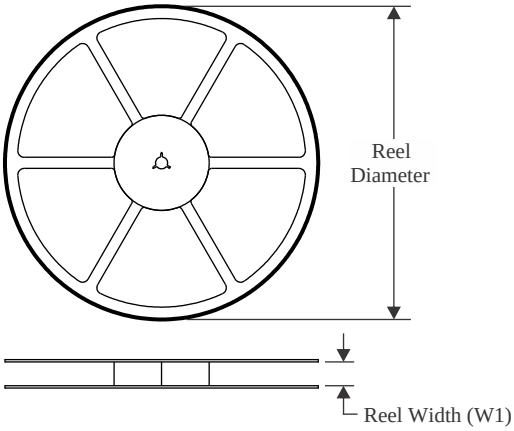
- Automotive : OPA171-Q1, OPA2171-Q1, OPA4171-Q1
- Enhanced Product : OPA2171-EP

NOTE: Qualified Version Definitions:

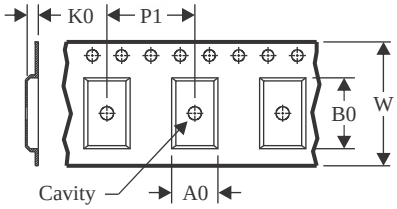
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

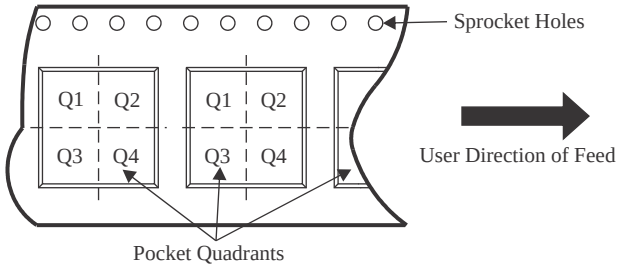


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

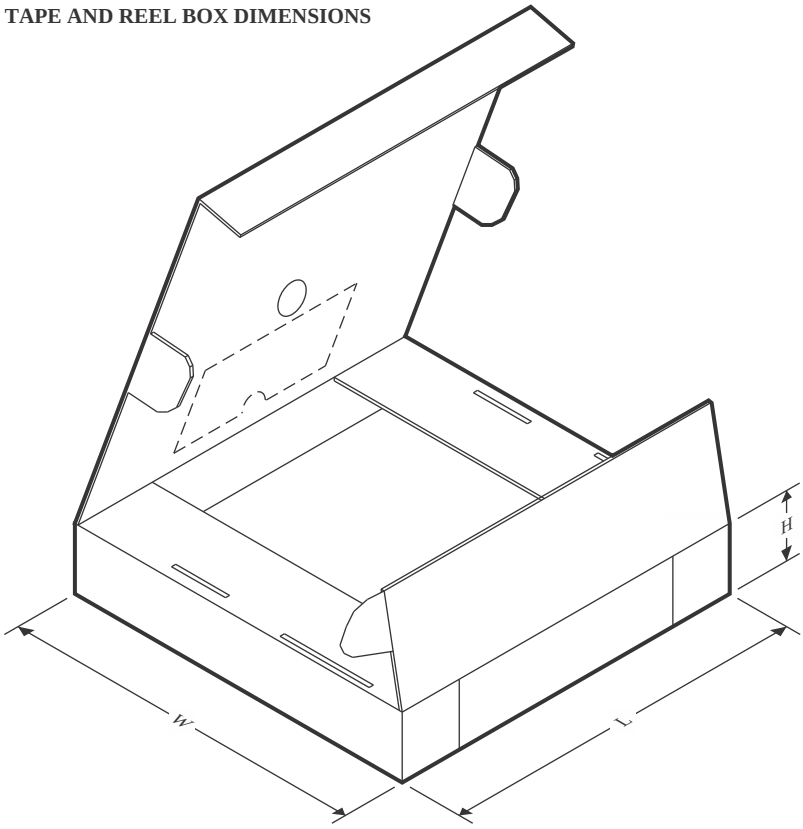
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA171AIDRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA171AIDRLT	SOT-5X3	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2171AIDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4171AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

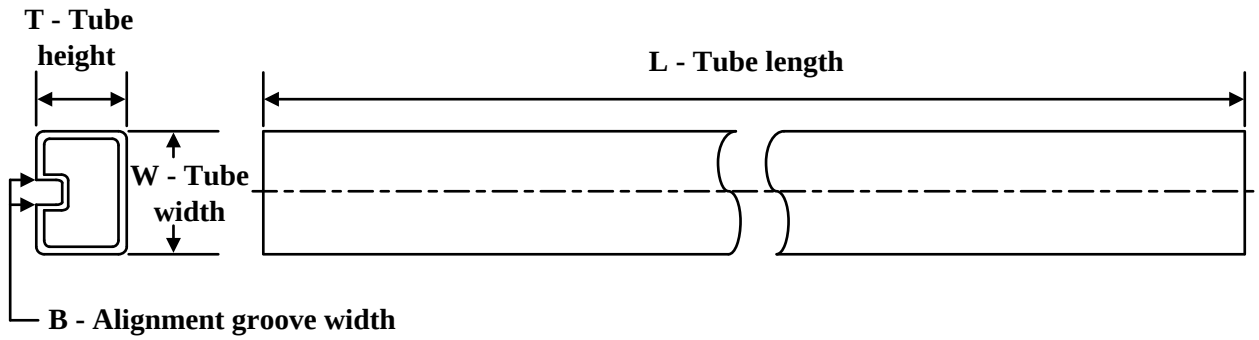
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA171AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA171AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA171AIDRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
OPA171AIDRLT	SOT-5X3	DRL	5	250	202.0	201.0	28.0
OPA2171AIDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2171AIDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2171AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2171AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4171AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4171AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

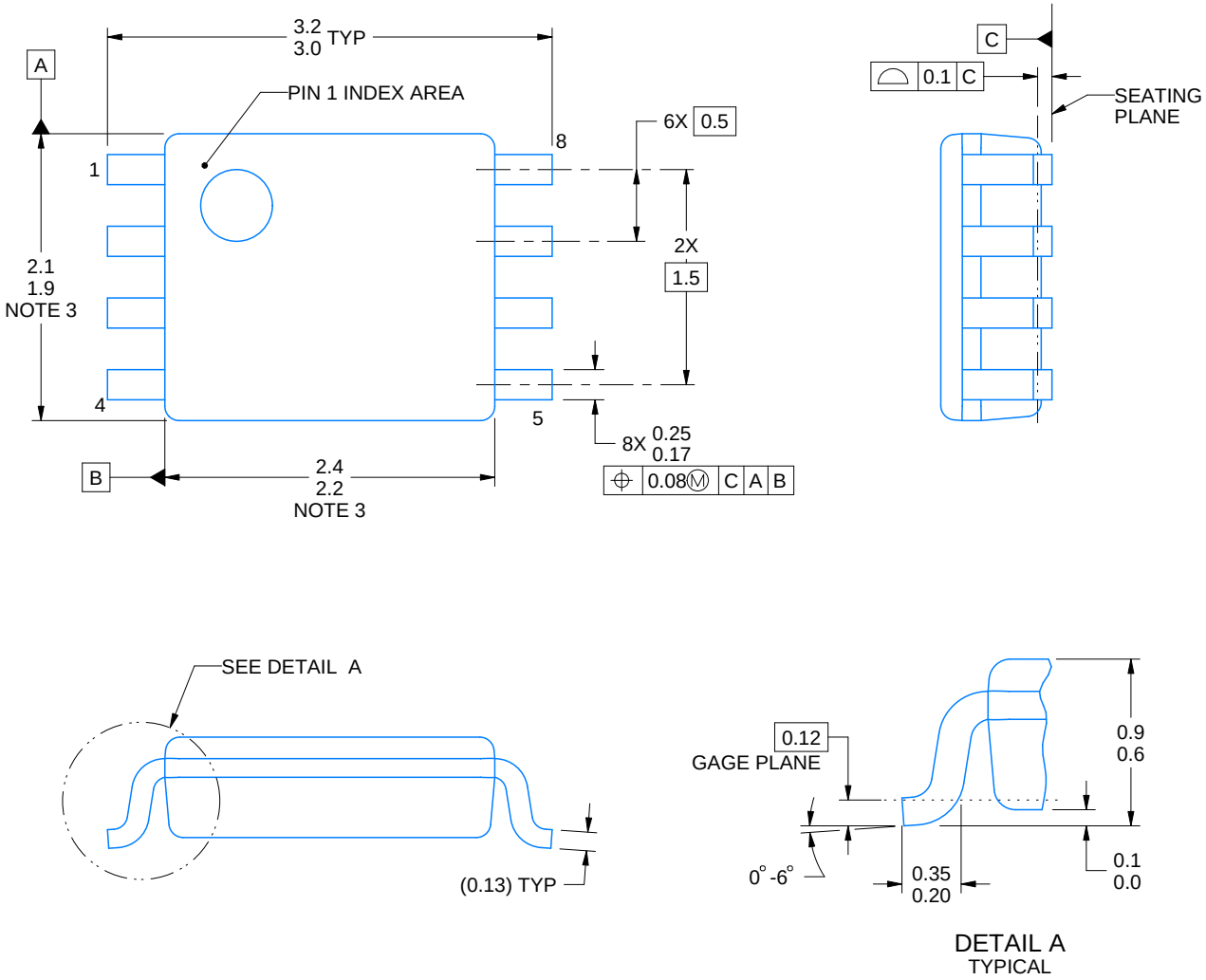
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA171AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4171AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4171AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DCU0008A

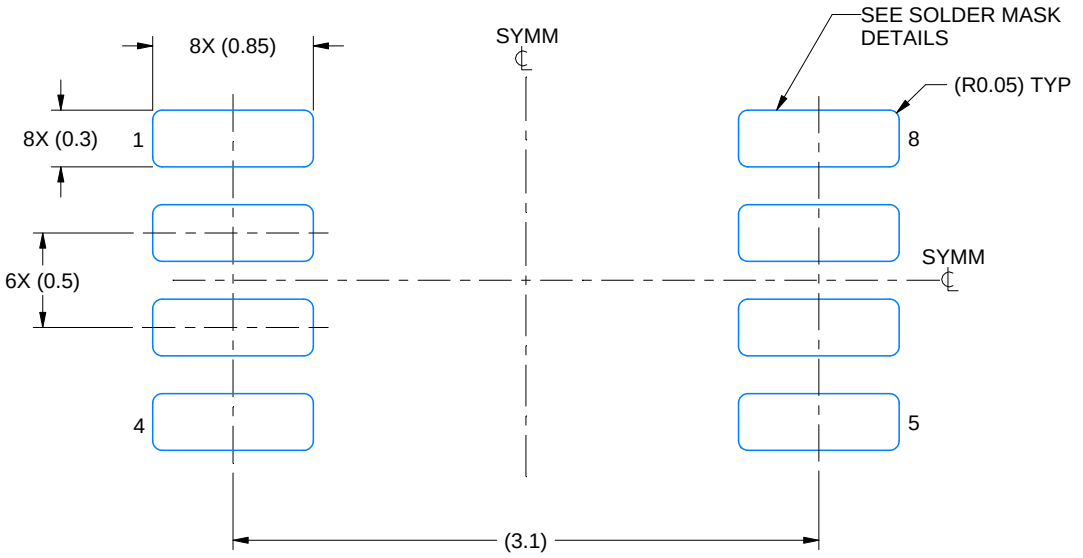
VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

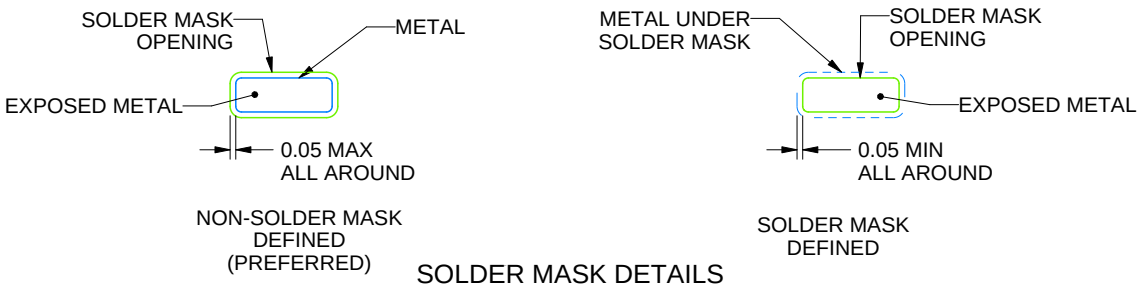


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

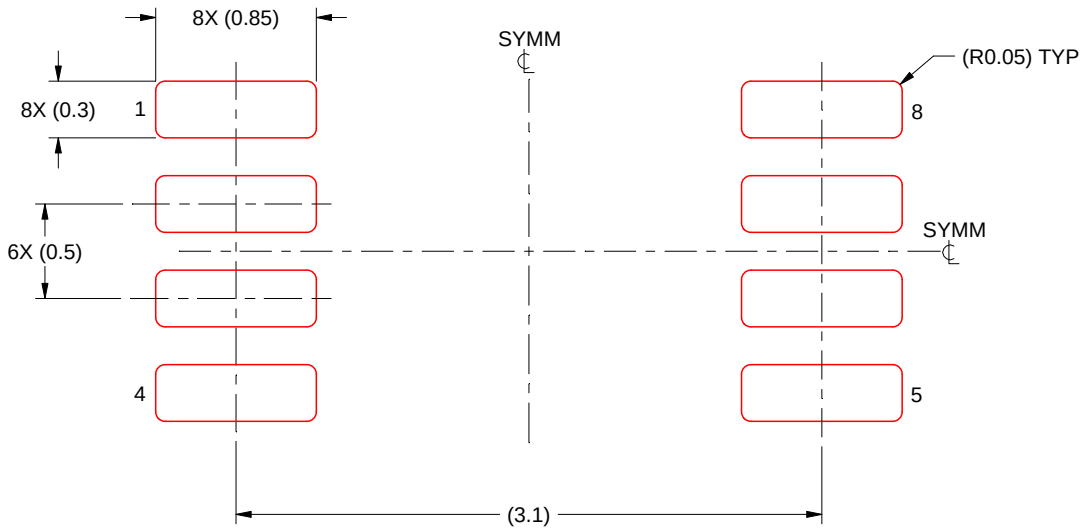
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

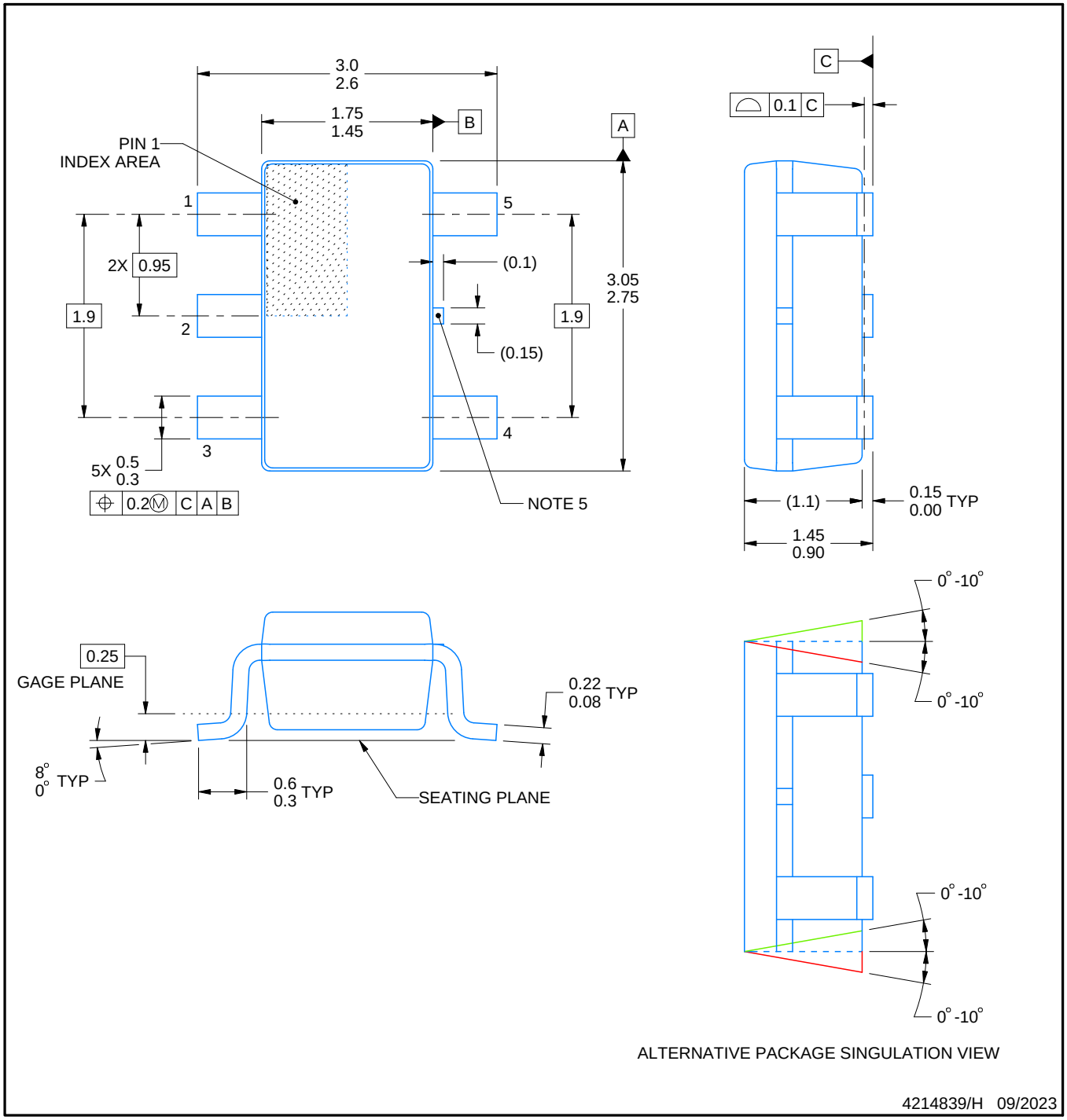
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

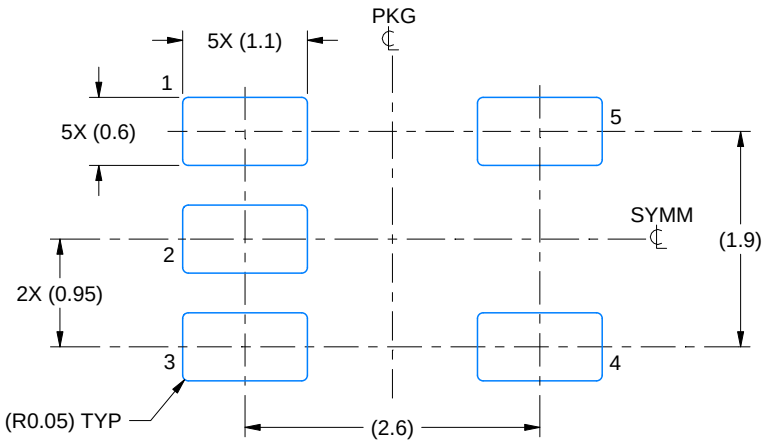


ALTERNATIVE PACKAGE SINGULATION VIEW

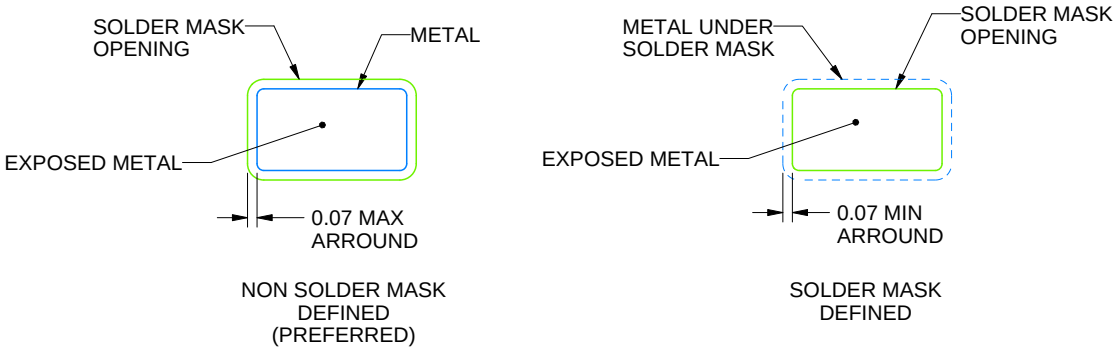
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

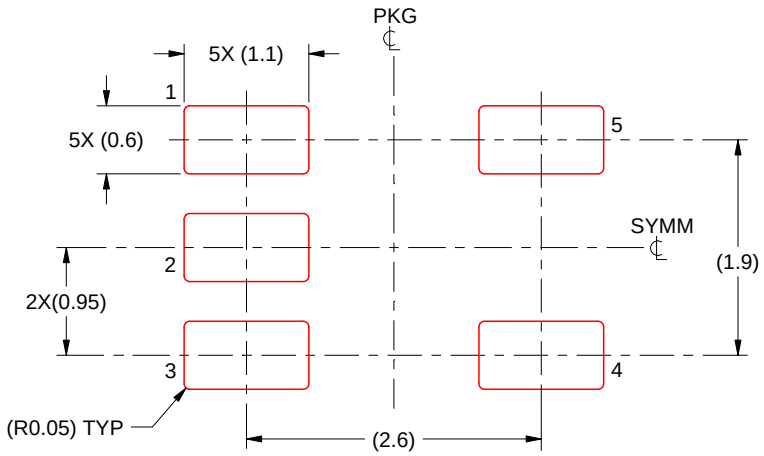


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

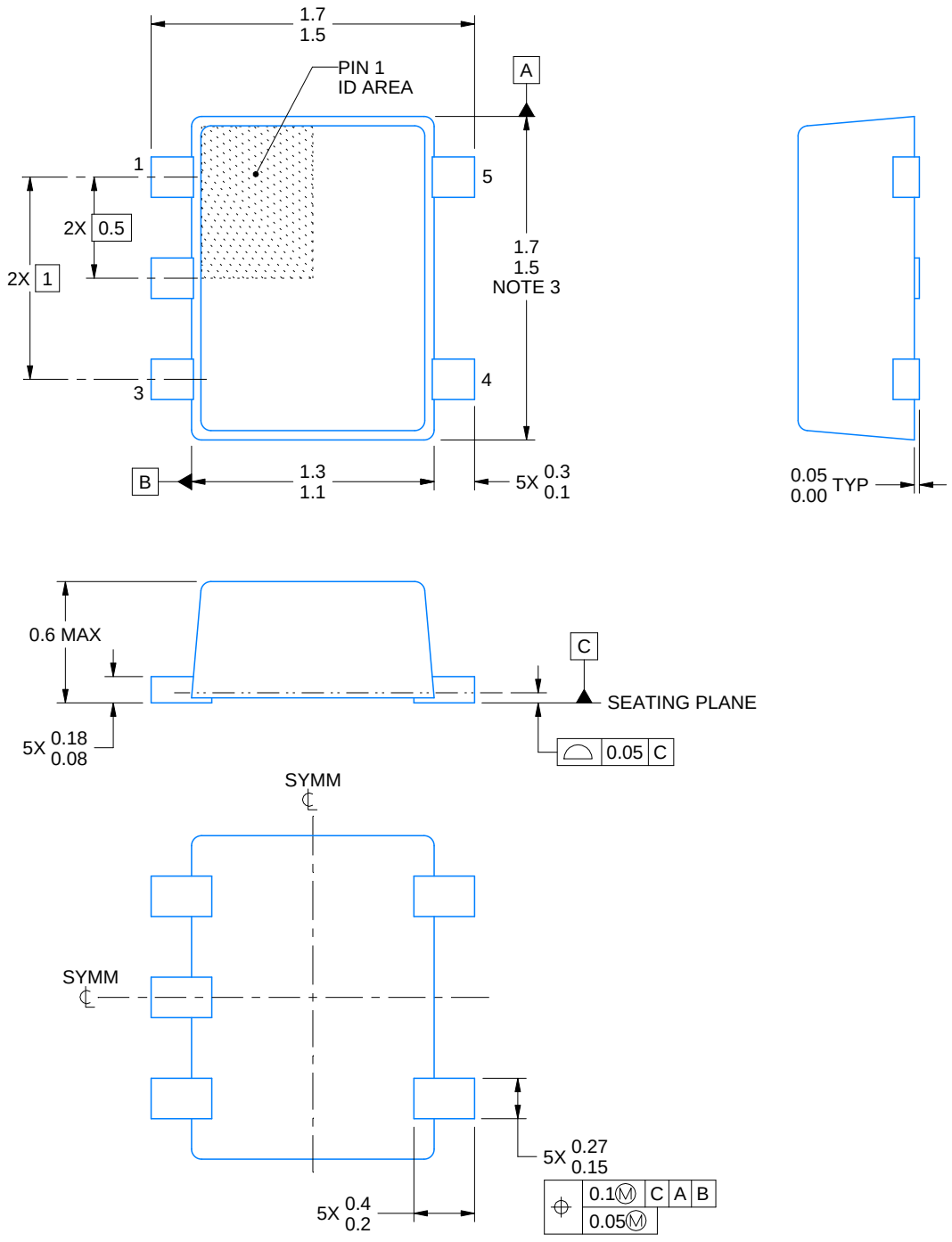
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/B 12/2020

NOTES:

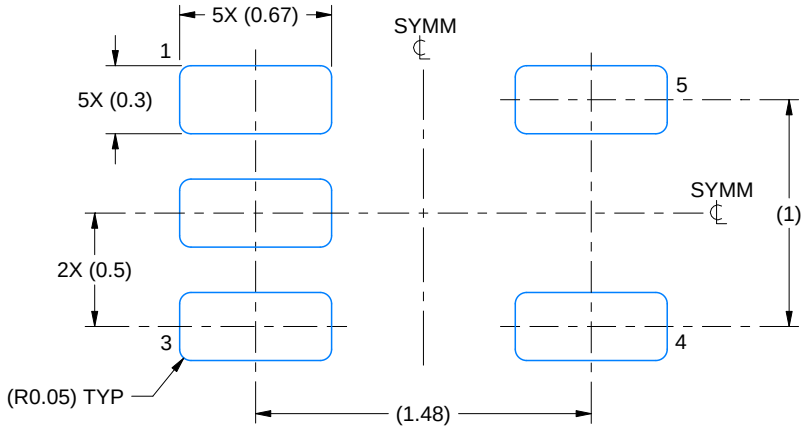
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

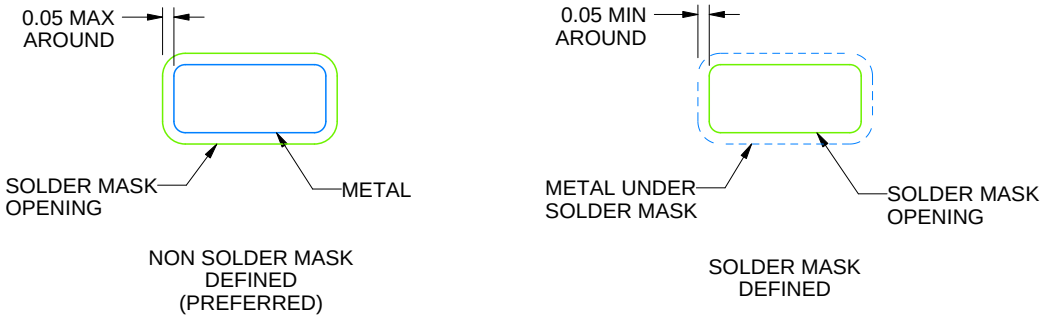
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

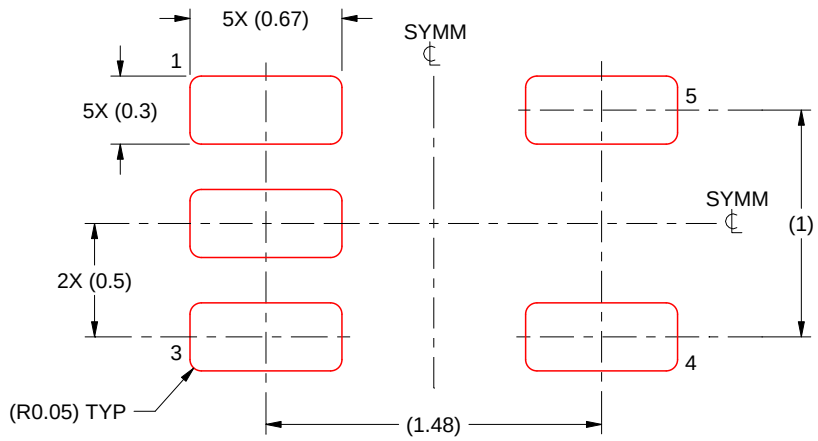
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



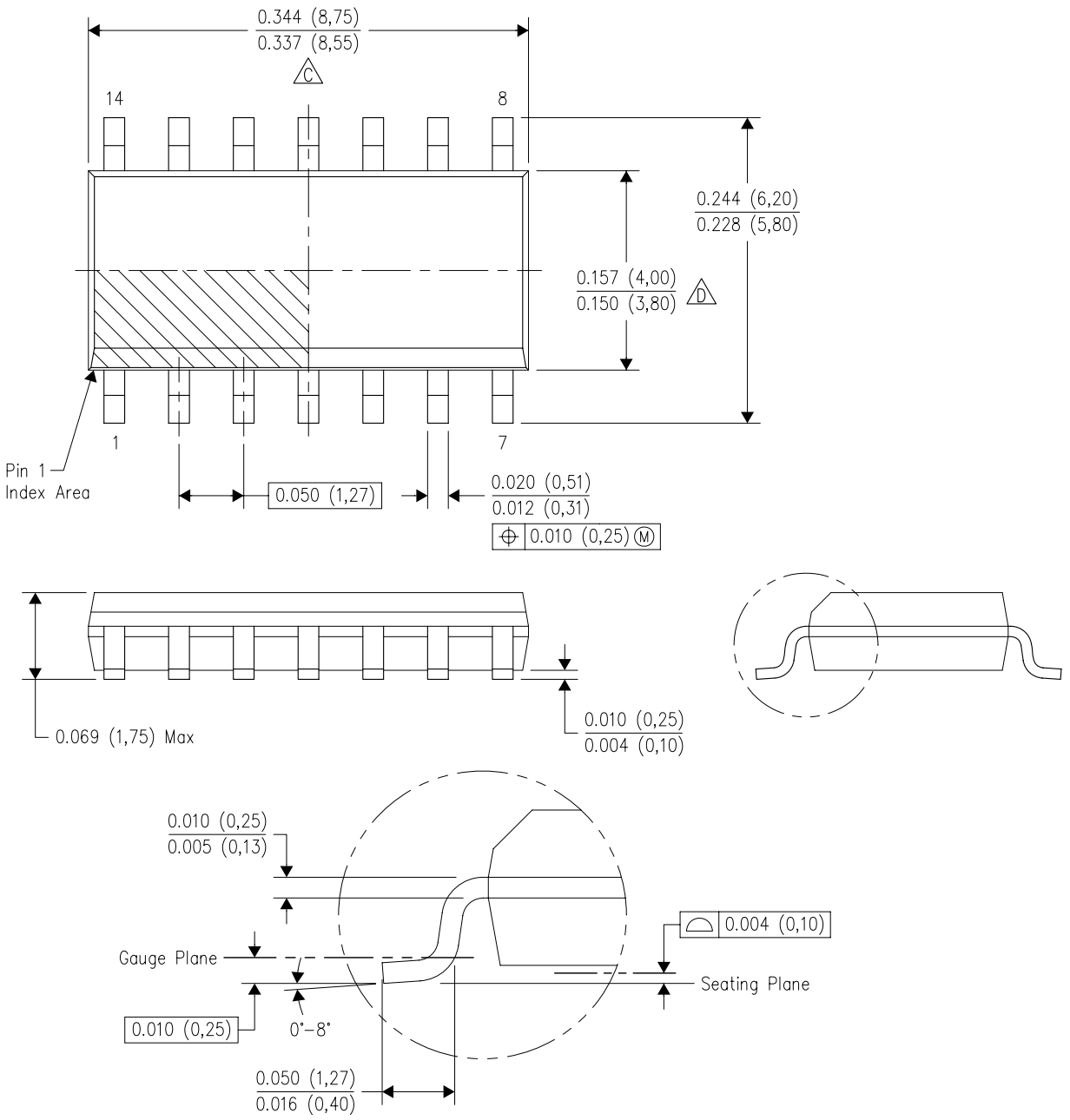
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

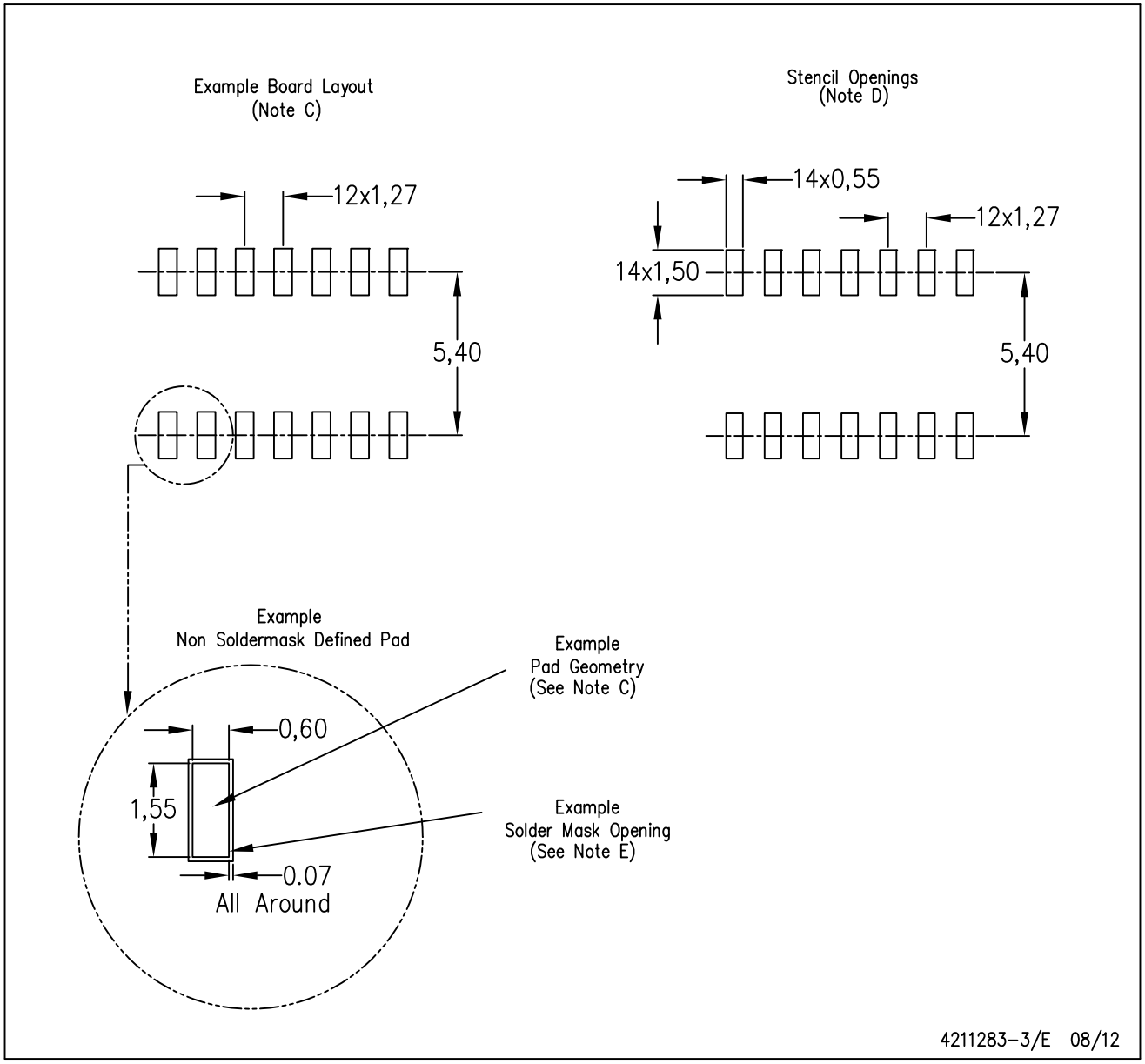
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



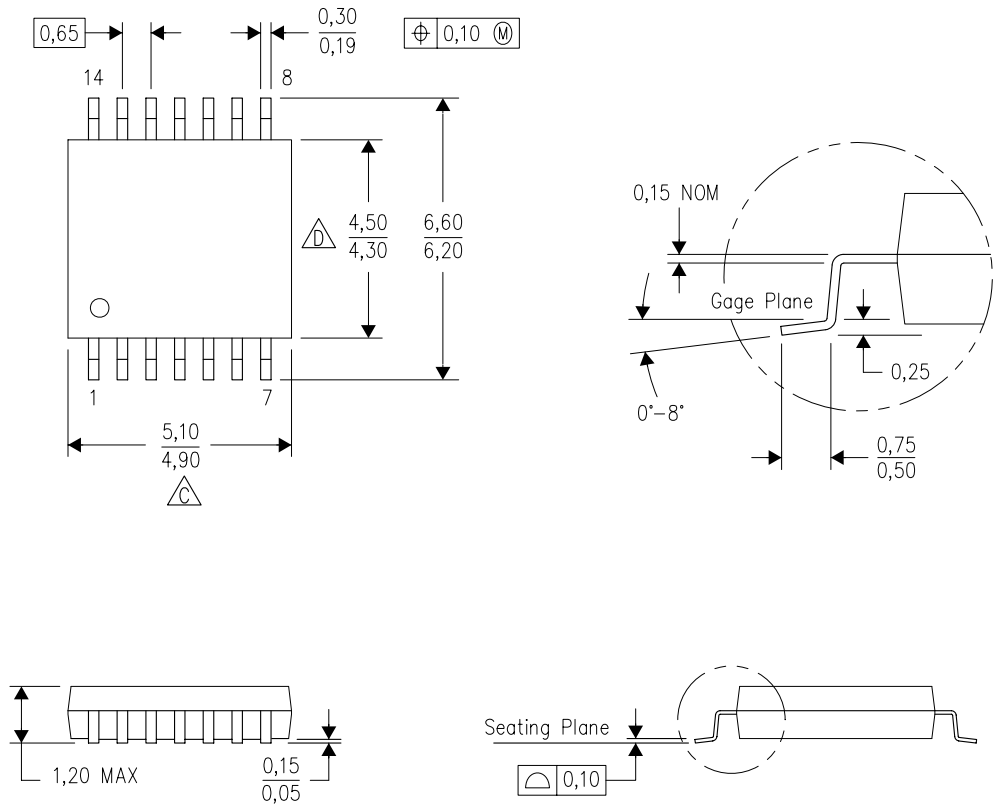
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

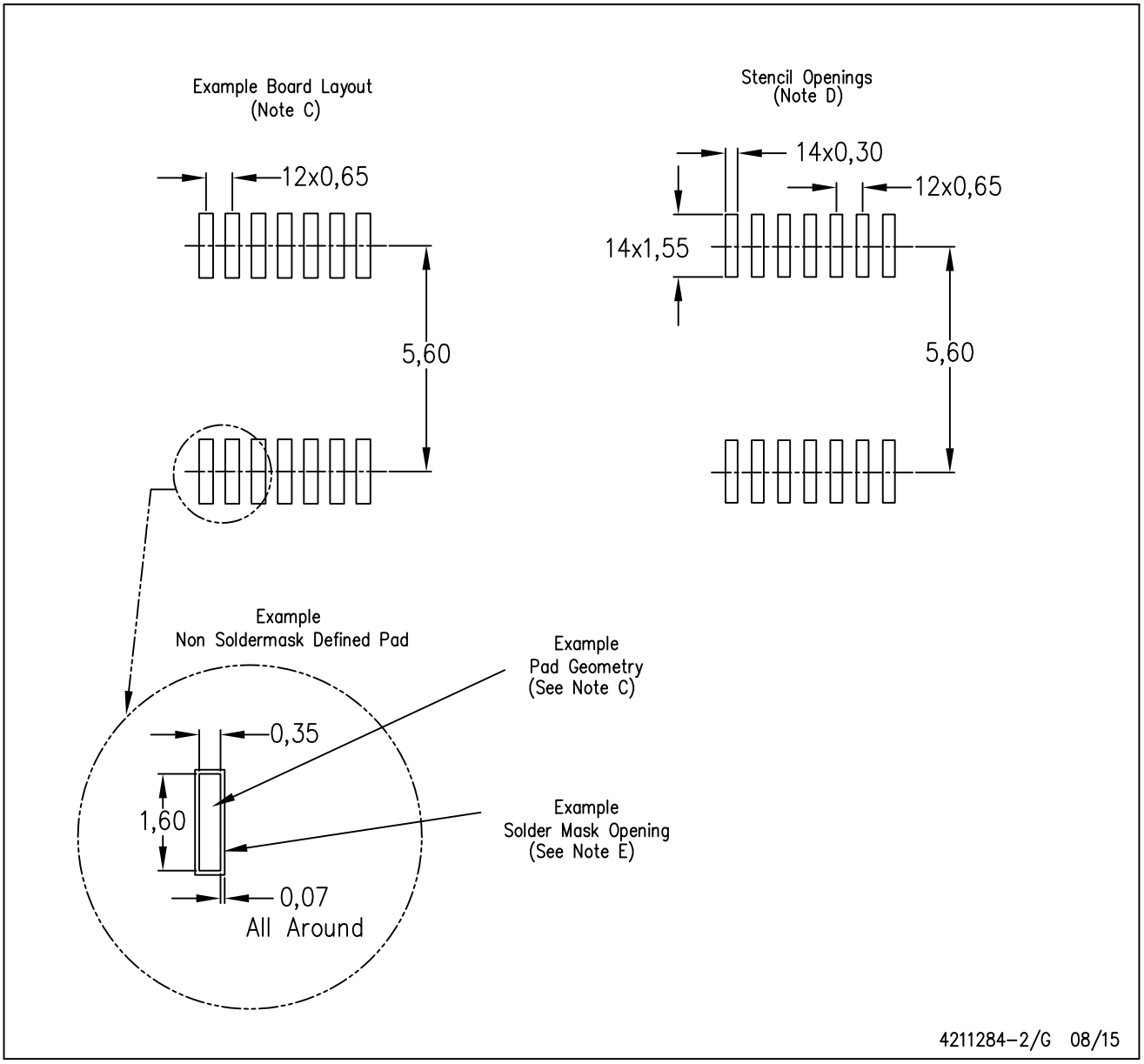
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



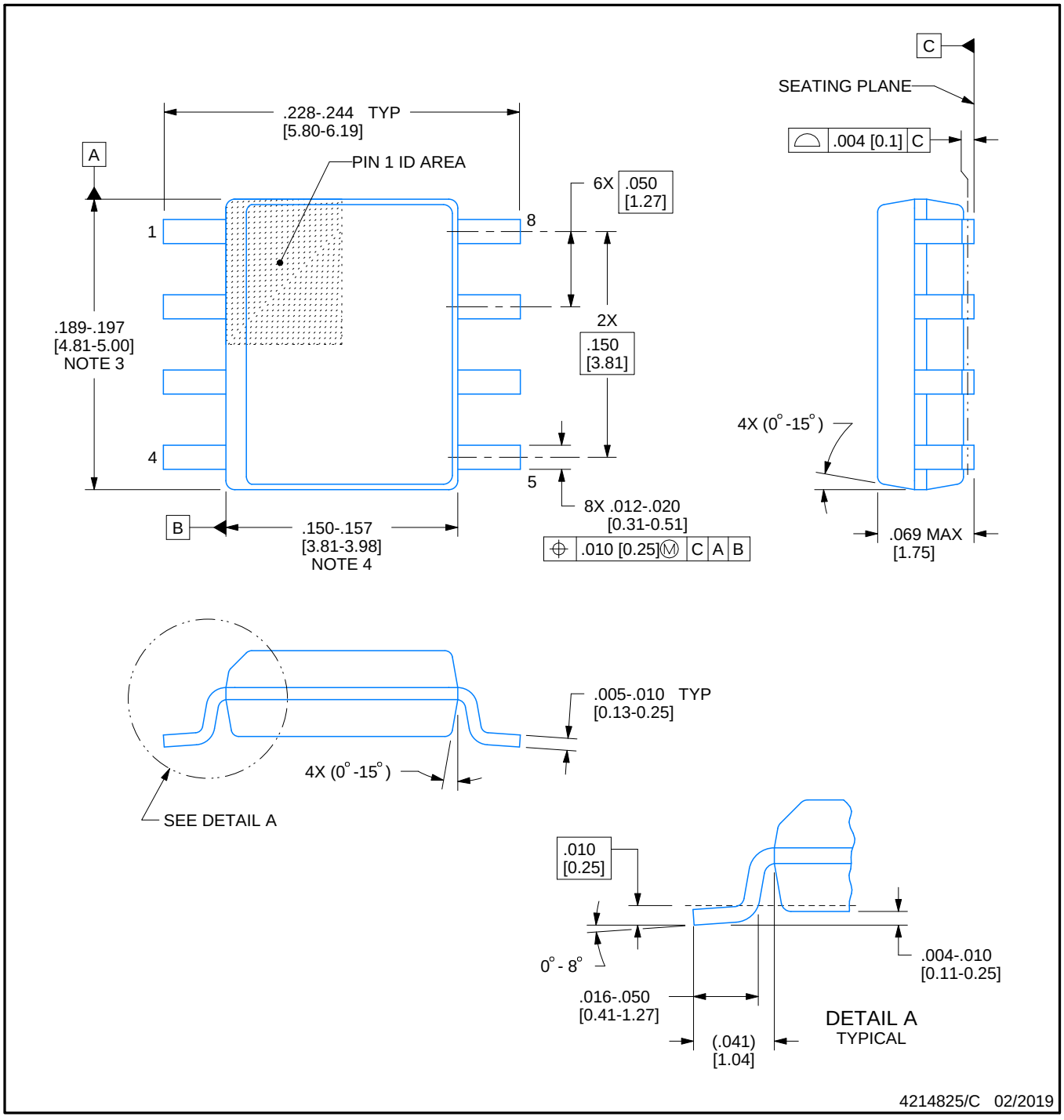
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

D0008A

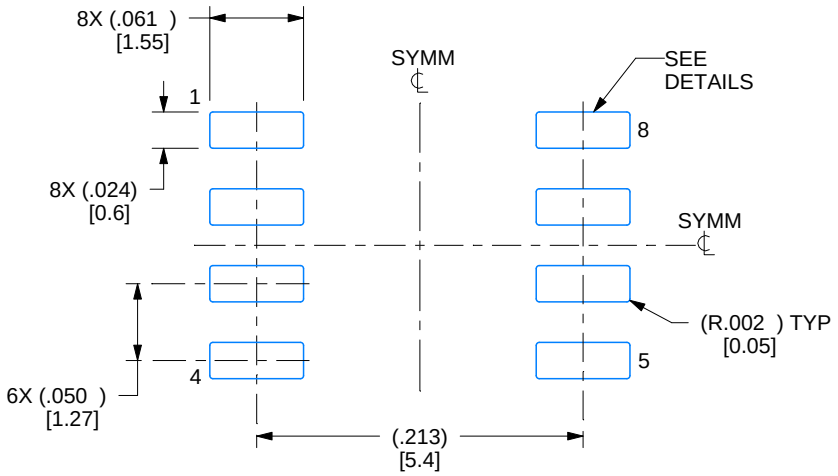
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

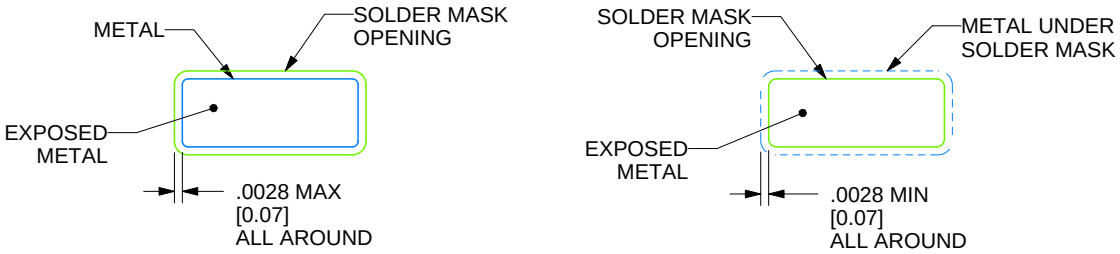


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

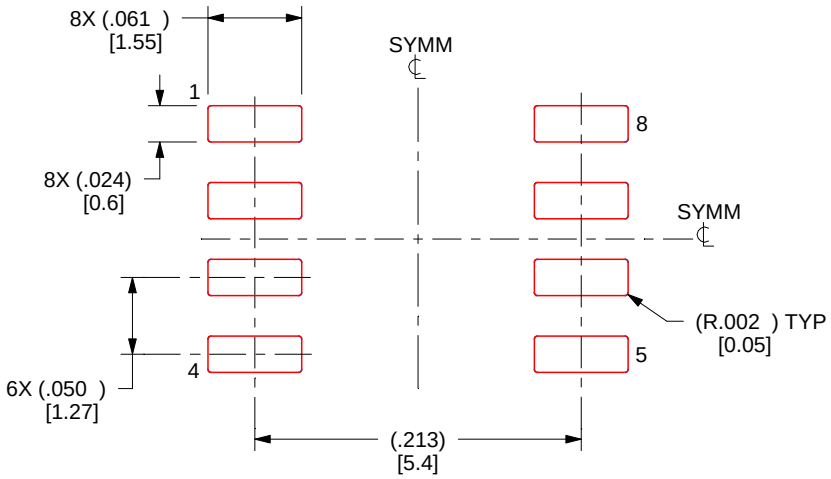
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



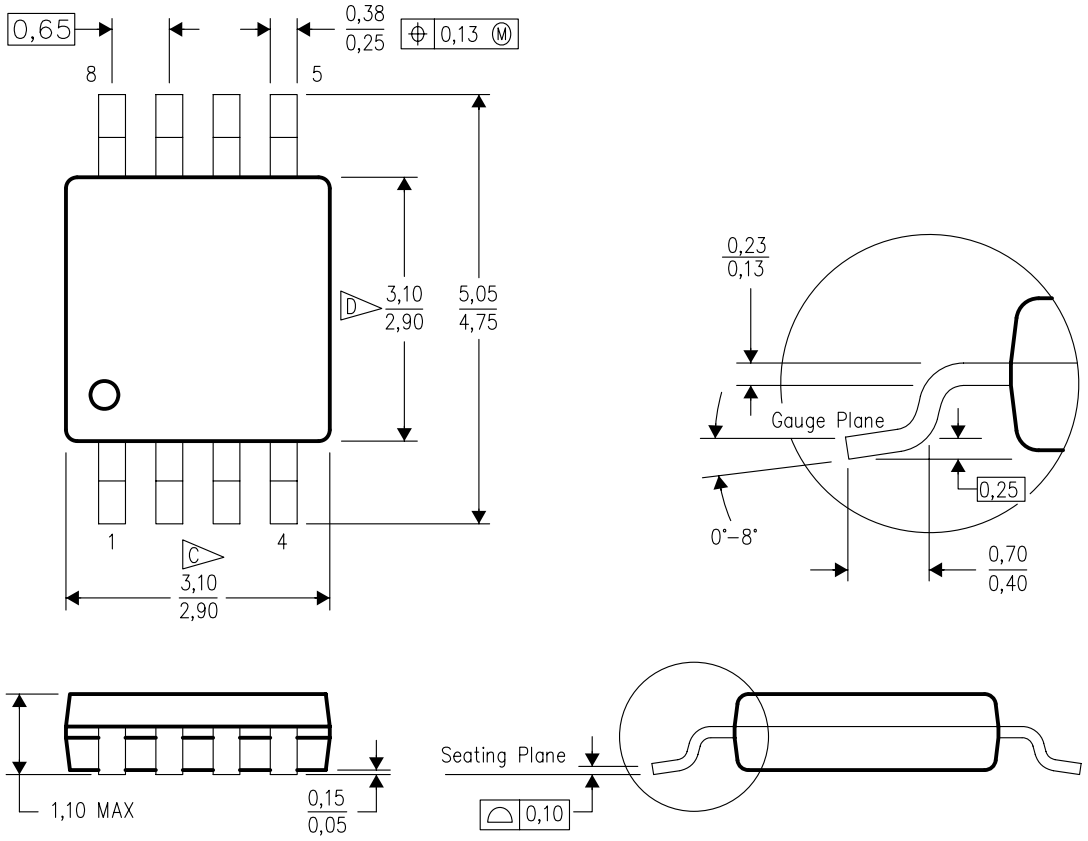
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

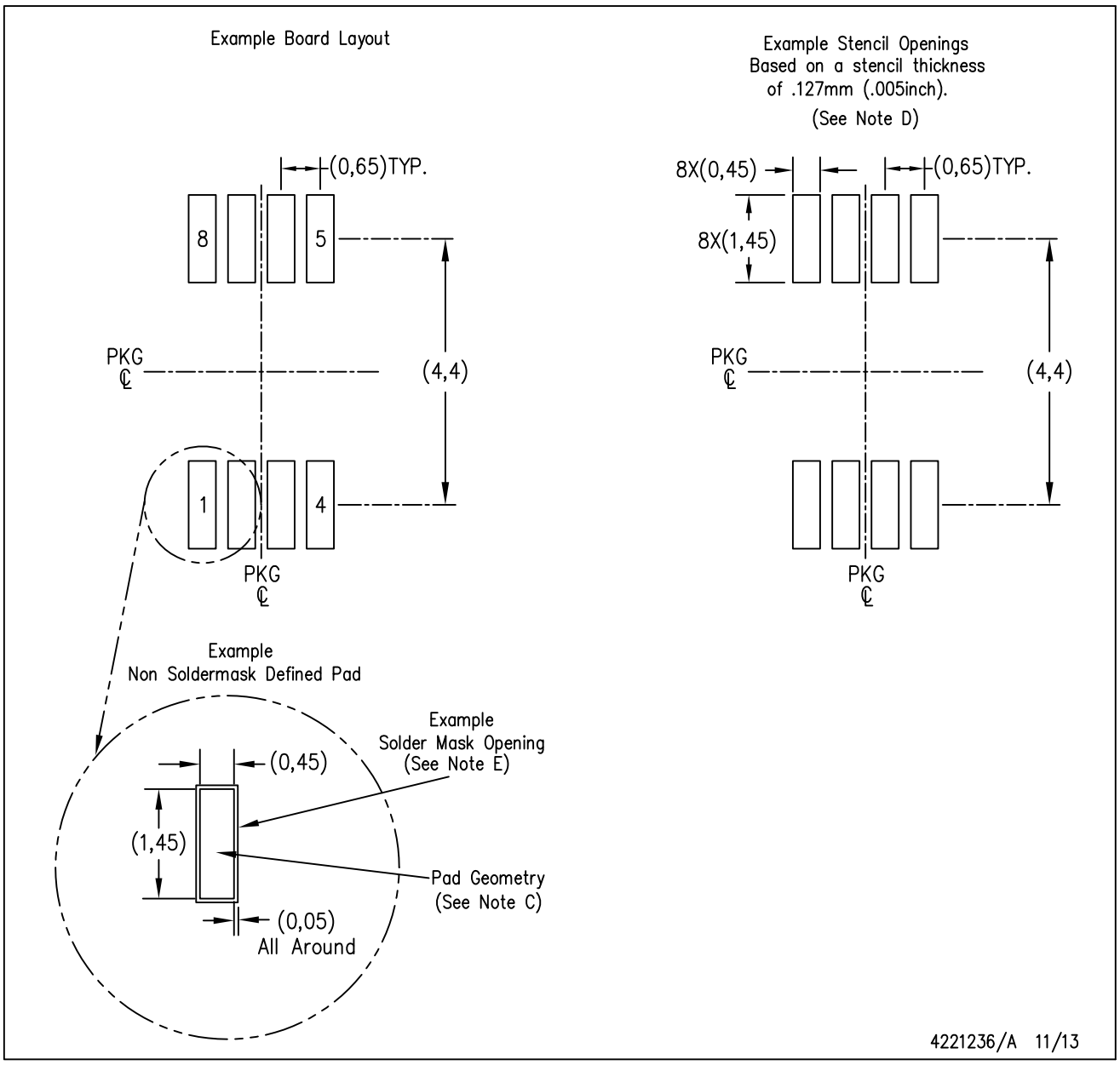
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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