16-Bit, 250kSPS, 6-Channel, Simultaneous Sampling SAR ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **Six Input Channels**
- **Fully Differential Inputs**
- **Six Independent 16-Bit ADCs**
- **4μs Total Throughput per Channel**
- **Low Power:**
  200mW in Normal Mode
  5mW in Nap Mode
  50μW in Power-Down Mode
- **TQFP-64 Package Package**

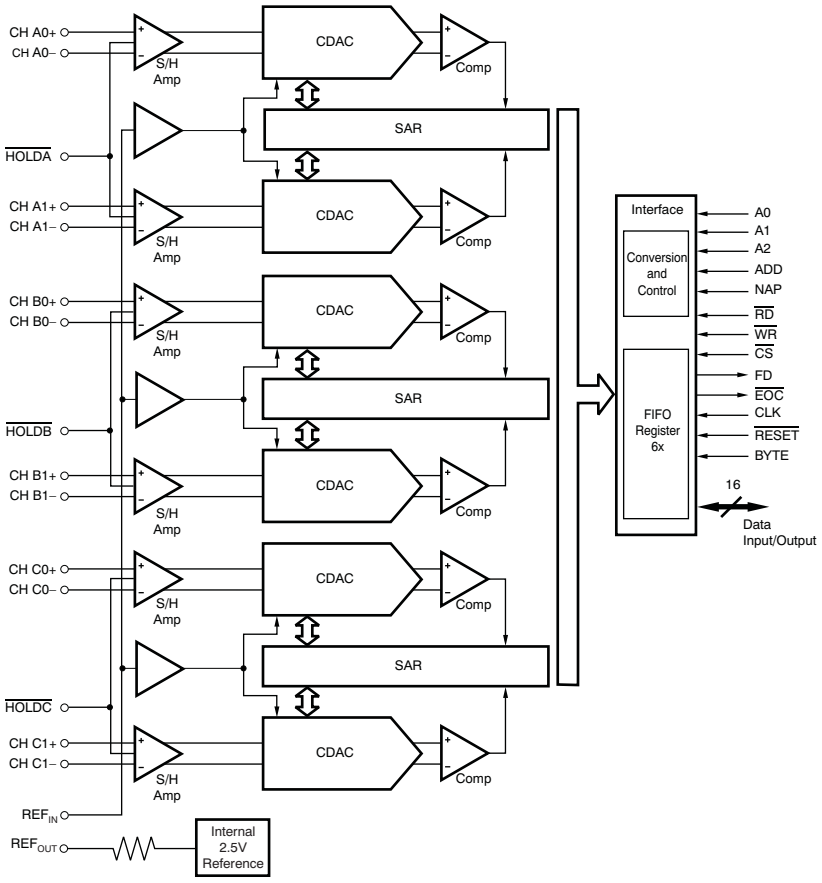
APPLICATIONS

- **Motor Control**
- **Multi-Axis Positioning Systems**
- **3-Phase Power Control**

DESCRIPTION

The ADS8365 includes six, 16-bit, 250kSPS analog-to-digital converters (ADCs) with six fully differential input channels grouped into three pairs for high-speed simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the ADC. This architecture provides excellent common-mode rejection of 80dB at 50kHz, which is important in high-noise environments.

The ADS8365 offers a flexible, high-speed parallel interface with a direct address mode, a cycle, and a FIFO mode. The output data for each channel is available as a 16-bit word.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8365	±4	14	TQFP-64	PAG	–40°C to +85°C	ADS8365AI	ADS8365IPAG	Tray, 160
							ADS8365IPAGR	Tape and Reel, 1500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	ADS8365	UNIT
Supply voltage, AGND to AV_{DD}	–0.3 to 6	V
Supply voltage, BGND to BV_{DD}	–0.3 to 6	V
Analog input voltage range	AGND – 0.3 to AV_{DD} + 0.3	V
Reference input voltage range	AGND – 0.3 to AV_{DD} + 0.3	V
Digital input voltage range	BGND – 0.3 to BV_{DD} + 0.3	V
Ground voltage differences, AGND to BGND	±0.3	V
Voltage differences, BV_{DD} to AGND	–0.3 to 6	V
Input current to any pin except supply	–20 to 20	mA
Power dissipation	See Dissipation Ratings Table	
Operating virtual junction temperature range, T_J	–40 to +150	°C
Operating free-air temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{STG}	–65 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
Low-K(1)	PAG	8.6°C/W	68.5°C/W	14.598mW/°C	1824mW	1168mW	949mW
High-K(2)	PAG	8.6°C/W	42.8°C/W	23.364mW/°C	2920mW	1869mW	1519mW

(1) The JEDEC Low K (1s) board design used to derive this data was a 3-inch x 3-inch, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC High K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes, and 2-ounce copper traces on the top and bottom of the board.

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RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD} to AGND		4.75	5	5.25	V
Supply voltage, BV_{DD} to BGND	Low-voltage levels	2.7		3.6	V
	5V logic levels	4.5	5	5.5	V
Reference input voltage		1.5	2.5	2.6	V
Operating common-mode signal, –IN		2.2	2.5	2.8	V
Analog inputs, +IN – (–IN)		0		$\pm V_{REF}$	V
Operating junction temperature range, T_J		–40		+125	°C

ELECTRICAL CHARACTERISTICS: 100kSPS

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 2MHz, and f_{SAMPLE} = 100kSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8365			UNIT
			MIN	TYP(1)	MAX	
ANALOG INPUT						
Full-scale range	FSR	+IN – (–IN)			$\pm V_{REF}$	V
Operating common-mode signal			2.2		2.8	V
Input resistance		–IN = V_{REF}		750		Ω
Input capacitance		–IN = V_{REF}		25		pF
Input leakage current		–IN = V_{REF}		±1		nA
Differential input resistance		–IN = V_{REF}		1500		Ω
Differential input capacitance		–IN = V_{REF}		15		pF
Common-mode rejection ratio	CMRR	At dc		84		dB
		V_{IN} = ±1.25V_{PP} at 50kHz		80		dB
Bandwidth	BW	FS sinewave, –3dB		10		MHz
DC ACCURACY						
Resolution				16		Bits
No missing codes	NMC		14			Bits
Integral linearity error	INL			±1.5	±4	LSB
Differential nonlinearity	DNL			±1.5		LSB
Bipolar offset error	V_{OS}			±1	±2.3	mV
Bipolar offset error match		Only pair-wise matching		0.2	1	mV
Bipolar offset error drift	TCV_{OS}			0.8		ppm/°C
Gain error	G_{ERR}	Referenced to V_{REF}		±0.05	±0.25	%FSR
Gain error match		Only pair-wise matching		0.005	0.05	%FSR
Gain error drift	TCG_{ERR}			2		ppm/°C
Noise				60		µVrms
Power-supply rejection ratio	PSRR	4.75V < AV_{DD} < 5.25V		–87		dB
SAMPLING DYNAMICS						
Conversion time per ADC	t_{CONV}	50kHz ≤ f_{CLK} ≤ 5MHz	3.2		320	µs
Acquisition time	t_{AQ}	f_{CLK} = 5MHz	800			ns
Aperture delay					5	ns
Aperture delay matching				100		ps
Aperture jitter				50		ps
Clock frequency			0.05		5	MHz

(1) All typical values are at +25°C.

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ELECTRICAL CHARACTERISTICS: 100kSPS (continued)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 2MHz, and f_{SAMPLE} = 100kSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8365 MIN	ADS8365 TYP(1)	ADS8365 MAX	UNIT
AC ACCURACY						
Total harmonic distortion	THD	V_{IN} = ±2.5V_{PP} at 50kHz		–94		dB
Spurious-free dynamic range	SFDR	V_{IN} = ±2.5V_{PP} at 50kHz		95		dB
Signal-to-noise ratio	SNR	V_{IN} = ±2.5V_{PP} at 10kHz		88		dB
Signal-to-noise + distortion	SINAD	V_{IN} = ±2.5V_{PP} at 10kHz		87		dB
Channel-to-channel isolation				95		dB
Effective number of bits	ENOB			14.3		Bits
VOLTAGE REFERENCE OUTPUT						
Reference voltage output	V_{OUT}		2.475	2.5	2.525	V
Initial accuracy					±1	%
Output voltage temperature drift	dV_{OUT}/dT			±20		ppm/°C
Output voltage noise		f = 0.1Hz to 10Hz, C_L = 10µF		40		μV_{PP}
		f = 10Hz to 10kHz, C_L = 10µF		8		µVrms
Power-supply rejection ratio	PSRR			60		dB
Output impedance	R_{OUT}			2		kΩ
Short-circuit current	I_{SC}			1.25		mA
Turn-on settling time		to 0.1% at C_L = 0pF		100		µs
VOLTAGE REFERENCE INPUT						
Reference voltage input	V_{IN}		1.5	2.5	2.6	V
Reference input resistance			100			MΩ
Reference input capacitance				5		pF
Reference input current					1	µA
DIGITAL INPUTS(2)						
Logic family				CMOS		
High-level input voltage	V_{IH}		0.7 × BV_{DD}		BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.3		0.3 × BV_{DD}	V
Input current	I_{IN}	V_I = BV_{DD} or GND			±50	nA
Input capacitance	C_I			5		pF
DIGITAL OUTPUTS(2)						
Logic family				CMOS		
High-level output voltage	V_{OH}	BV_{DD} = 4.5V, I_{OH} = –100µA	4.44			V
Low-level output voltage	V_{OL}	BV_{DD} = 4.5V, I_{OL} = 100µA			0.5	V
High-impedance state output current	I_{OZ}	$\overline{CS}$ = BV_{DD}, V_I = BV_{DD} or GND			±50	nA
Output capacitance	C_O			5		pF
Load capacitance	C_L				30	pF
DIGITAL INPUTS(3)						
Logic family				LVCMOS		
High-level input voltage	V_{IH}	BV_{DD} = 3.6V	2		BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	BV_{DD} = 2.7V	–0.3		0.8	V
Input current	I_{IN}	V_I = BV_{DD} or GND			±50	nA
Input capacitance	C_I			5		pF

(2) Applies for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(3) Applies for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

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ELECTRICAL CHARACTERISTICS: 100kSPS (continued)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 2MHz, and f_{SAMPLE} = 100kSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8365 MIN	ADS8365 TYP(1)	ADS8365 MAX	UNIT
DIGITAL OUTPUTS(4)						
Logic family				LVCMOS		
High-level output voltage	V_{OH}	BV_{DD} = 2.7V, I_{OH} = –100µA	BVDD – 0.2			V
Low-level output voltage	V_{OL}	BV_{DD} = 2.7V, I_{OL} = 100µA			0.2	V
High-impedance state output current	I_{OZ}	$\overline{CS}$ = BV_{DD}, V_I = BV_{DD} or GND			±50	nA
Output capacitance	C_O			5		pF
Load capacitance	C_L				30	pF
DATA FORMAT						
Data format		Bit DB4 = 1		Binary two's complement		
		Bit DB4 = 0		Straight binary coding		
POWER SUPPLY						
Analog supply voltage	AV_{DD}		4.75		5.25	V
Buffer I/O supply voltage	BV_{DD}	Low-voltage levels	2.7		3.6	V
		5V logic levels	4.5		5.5	V
Analog operating supply current	AI_{DD}			38	45	mA
Buffer I/O operating supply current	BI_{DD}	BV_{DD} = 3V		60	90	µA
		BV_{DD} = 5V		100	150	µA
Power dissipation		BV_{DD} = 3V		190	225	mW
		BV_{DD} = 5V		190	225	mW
		Nap mode enabled			5	mW
		Powerdown enabled			50	µW

(4) Applies for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

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ELECTRICAL CHARACTERISTICS: 250kSPS

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, and f_{SAMPLE} = 250kSPS, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS8365 MIN	ADS8365 TYP(1)	ADS8365 MAX	UNIT
ANALOG INPUT						
Full-scale range	FSR	+IN – (–IN)			$\pm V_{REF}$	V
Operating common-mode signal			2.2		2.8	V
Input resistance		–IN = V_{REF}		750		Ω
Input capacitance		–IN = V_{REF}		25		pF
Input leakage current		–IN = V_{REF}		±1		nA
Differential input resistance		–IN = V_{REF}		1500		Ω
Differential input capacitance		–IN = V_{REF}		15		pF
Common-mode rejection ratio	CMRR	At dc		84		dB
		V_{IN} = ±1.25V_{PP} at 50kHz		80		dB
Bandwidth	BW	FS sinewave, –3dB		10		MHz
DC ACCURACY						
Resolution				16		Bits
No missing codes	NMC		14			Bits
Integral linearity error	INL			±3	±8	LSB
Differential nonlinearity	DNL	Specified for 14 bit		±1.5		LSB
Bipolar offset error	V_{OS}			±1	±2.3	mV
Bipolar offset error match		Only pair-wise matching		0.2	1	mV
Bipolar offset error drift	TCV_{OS}			0.8		ppm/°C
Gain error	G_{ERR}	Referenced to V_{REF}		±0.05	±0.25	%FSR
Gain error match		Only pair-wise matching		0.005	0.05	%FSR
Gain error drift	TCG_{ERR}			2		ppm/°C
Noise				60		µVrms
Power-supply rejection ratio	PSRR	4.75V < AV_{DD} < 5.25V		–87		dB
SAMPLING DYNAMICS						
Conversion time per ADC	t_{CONV}	50kHz ≤ f_{CLK} ≤ 5MHz	3.2		320	µs
Acquisition time	t_{AQ}	f_{CLK} = 5MHz	800			ns
Throughput rate					250	kSPS
Aperture delay					5	ns
Aperture delay matching				100		ps
Aperture jitter				50		ps
Clock frequency			0.05		5	MHz
AC ACCURACY						
Total harmonic distortion	THD	V_{IN} = ±2.5V_{PP} at 50kHz		–94		dB
Spurious-free dynamic range	SFDR	V_{IN} = ±2.5V_{PP} at 50kHz		95		dB
Signal-to-noise ratio	SNR	V_{IN} = ±2.5V_{PP} at 10kHz		88		dB
Signal-to-noise + distortion	SINAD	V_{IN} = ±2.5V_{PP} at 10kHz		87		dB
Channel-to-channel isolation				95		dB
Effective number of bits	ENOB			14.3		Bits

(1) All typical values are at +25°C.

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ELECTRICAL CHARACTERISTICS: 250kSPS (continued)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, and f_{SAMPLE} = 250kSPS, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS8365 MIN	ADS8365 TYP(1)	ADS8365 MAX	UNIT
VOLTAGE REFERENCE OUTPUT						
Reference voltage output	V_{OUT}		2.475	2.5	2.525	V
Initial accuracy					±1	%
Output voltage temperature drift	dV_{OUT}/dT			±20		ppm/°C
Output voltage noise		f = 0.1Hz to 10Hz, C_L = 10µF		40		μV_{PP}
		f = 10Hz to 10kHz, C_L = 10µF		8		µVrms
Power-supply rejection ratio	PSRR			60		dB
Output impedance	R_{OUT}			2		kΩ
Short-circuit current	I_{SC}			1.25		mA
Turn-on settling time		to 0.1% at C_L = 0pF		100		µs
VOLTAGE REFERENCE INPUT						
Reference voltage input	V_{IN}		1.5	2.5	2.6	V
Reference input resistance			100			MΩ
Reference input capacitance				5		pF
Reference input current					1	µA
DIGITAL INPUTS(2)						
Logic family				CMOS		
High-level input voltage	V_{IH}		0.7 × BV_{DD}		BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.3		0.3 × BV_{DD}	V
Input current	I_{IN}	V_I = BV_{DD} or GND			±50	nA
Input capacitance	C_I			5		pF
DIGITAL OUTPUTS(2)						
Logic family				CMOS		
High-level output voltage	V_{OH}	BV_{DD} = 4.5V, I_{OH} = –100µA	4.44			V
Low-level output voltage	V_{OL}	BV_{DD} = 4.5V, I_{OL} = 100µA			0.5	V
High-impedance state output current	I_{OZ}	$\overline{CS}$ = BV_{DD}, V_I = BV_{DD} or GND			±50	nA
Output capacitance	C_O			5		pF
Load capacitance	C_L				30	pF
DIGITAL INPUTS(3)						
Logic family				LVCMOS		
High-level input voltage	V_{IH}	BV_{DD} = 3.6V	2		BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	BV_{DD} = 2.7V	–0.3		0.8	V
Input current	I_{IN}	V_I = BV_{DD} or GND			±50	nA
Input capacitance	C_I			5		pF
DIGITAL OUTPUTS(3)						
Logic family				LVCMOS		
High-level output voltage	V_{OH}	BV_{DD} = 2.7V, I_{OH} = –100µA	BVDD – 0.2			V
Low-level output voltage	V_{OL}	BV_{DD} = 2.7V, I_{OL} = 100µA			0.2	V
High-impedance state output current	I_{OZ}	$\overline{CS}$ = BV_{DD}, V_I = BV_{DD} or GND			±50	nA
Output capacitance	C_O			5		pF
Load capacitance	C_L				30	pF

(2) Applies for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(3) Applies for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

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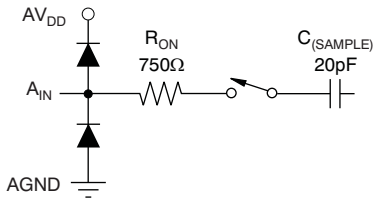
ELECTRICAL CHARACTERISTICS: 250kSPS (continued)

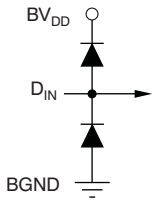
Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, and f_{SAMPLE} = 250kSPS, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS8365 MIN	ADS8365 TYP(1)	ADS8365 MAX	UNIT
DATA FORMAT						
Data format		Bit DB4 = 1	Binary two's complement			
		Bit DB4 = 0	Straight binary coding			
POWER SUPPLY						
Analog supply voltage	AV_{DD}		4.75		5.25	V
Buffer I/O supply voltage	BV_{DD}	Low-voltage levels	2.7		3.6	V
		5V logic levels	4.5		5.5	V
Analog operating supply current	AI_{DD}			40	48	mA
Buffer I/O operating supply current	BI_{DD}	BV_{DD} = 3V		150	225	µA
		BV_{DD} = 5V		250	375	µA
Power dissipation		BV_{DD} = 3V		200	240	mW
		BV_{DD} = 5V		201	241	mW
		Nap mode enabled			5	mW
		Powerdown enabled			50	µW

EQUIVALENT INPUT CIRCUIT



Equivalent Analog Input Circuit



Diode Turn-on Voltage: 0.35V

Equivalent Digital Input Circuit

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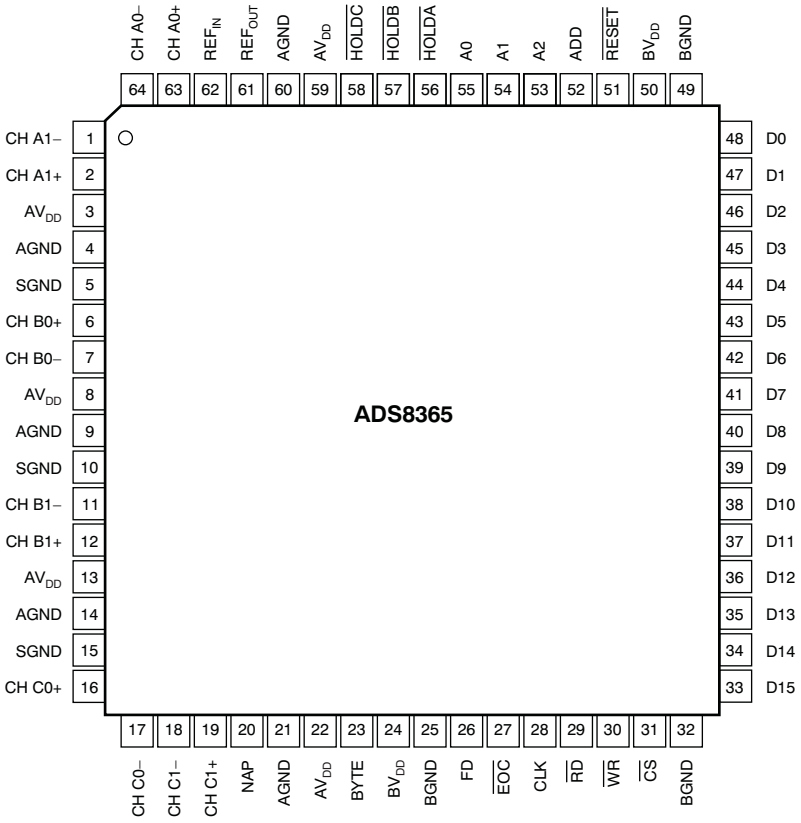
PIN CONFIGURATION

PAG PACKAGE
TQFP-64
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O[1]	DESCRIPTION
NAME	NO.		
CH A1–	1	AI	Inverting input channel A1
CH A1+	2	AI	Noninverting input channel A1
AV_{DD}	3	P	Analog power supply
AGND	4	P	Analog ground
SGND	5	P	Signal Ground
CH B0+	6	AI	Noninverting input channel B0
CH B0–	7	AI	Inverting input channel B0
AV_{DD}	8	P	Analog power supply
AGND	9	P	Analog ground
SGND	10	P	Signal ground
CH B1–	11	AI	Inverting input channel B1
CH B1+	12	AI	Noninverting input channel B1
AV_{DD}	13	P	Analog power supply
AGND	14	P	Analog ground
SGND	15	P	Signal ground
CH C0+	16	AI	Noninverting input channel C0
CH C0–	17	AI	Inverting input channel C0
CH C1–	18	AI	Inverting input channel C1

(1) AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output, and P = Power Supply Connection.

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O[1]	DESCRIPTION
NAME	NO.		
CH C1+	19	AI	Noninverting input channel C1
NAP	20	DI	Nap mode.Low level or unconnected = normal operation; high level = Nap mode.
AGND	21	P	Analog ground
AV_{DD}	22	P	+5V power supply
BYTE	23	DI	2 x 8 output capability (active high)
BV_{DD}	24	P	Power supply for digital interface from 3V to 5V
BGND	25	P	Buffer digital ground
FD	26	DO	First data (A0 data)
$\overline{EOC}$	27	DO	End of conversion (active low)
CLK	28	DI	An external CMOS compatible clock can be applied to the CLK input to synchronize the conversion process to an external source.
$\overline{RD}$	29	DI	Read (active low)
$\overline{WR}$	30	DI	Write (active low)
$\overline{CS}$	31	DI	Chip select (active low)
BGND	32	P	Buffer digital ground
D15	33	DO	Data bit 15 (MSB)
D14	34	DO	Data bit 14
D13	35	DO	Data bit 13
D12	36	DO	Data bit 12
D11	37	DO	Data bit 11
D10	38	DO	Data bit 10
D9	39	DO	Data bit 9
D8	40	DO	Data bit 8
D7	41	DIO	Data bit 7 (software input 7)
D6	42	DIO	Data bit 6 (software input 6)
D5	43	DIO	Data bit 5 (software input 5)
D4	44	DIO	Data bit 4 (software input 4)
D3	45	DIO	Data bit 3 (software input 3)
D2	46	DIO	Data bit 2 (software input 2)
D1	47	DIO	Data bit 1 (software input 1)
D0	48	DIO	Data bit 0 (software input 0) (LSB)
BGND	49	P	Buffer digital ground
BV_{DD}	50	P	Power supply for digital interface from 3V to 5V
$\overline{RESET}$	51	DI	Global reset (active low)
ADD	52	DI	Address mode select
A2	53	DI	Address line 3
A1	54	DI	Address line 2
A0	55	DI	Address line 1
$\overline{HOLDA}$	56	DI	Hold command A (active low)
$\overline{HOLDB}$	57	DI	Hold command B (active low)
$\overline{HOLDC}$	58	DI	Hold command C (active low)
AV_{DD}	59	P	Analog power supply
AGND	60	P	Analog ground
REF_{OUT}	61	AO	Reference output; attach 0.1µF and 10µF capacitors
REF_{IN}	62	AI	Reference input
CH A0+	63	AI	Noninverting input channel A0
CH A0–	64	AI	Inverting input channel A0

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TIMING INFORMATION

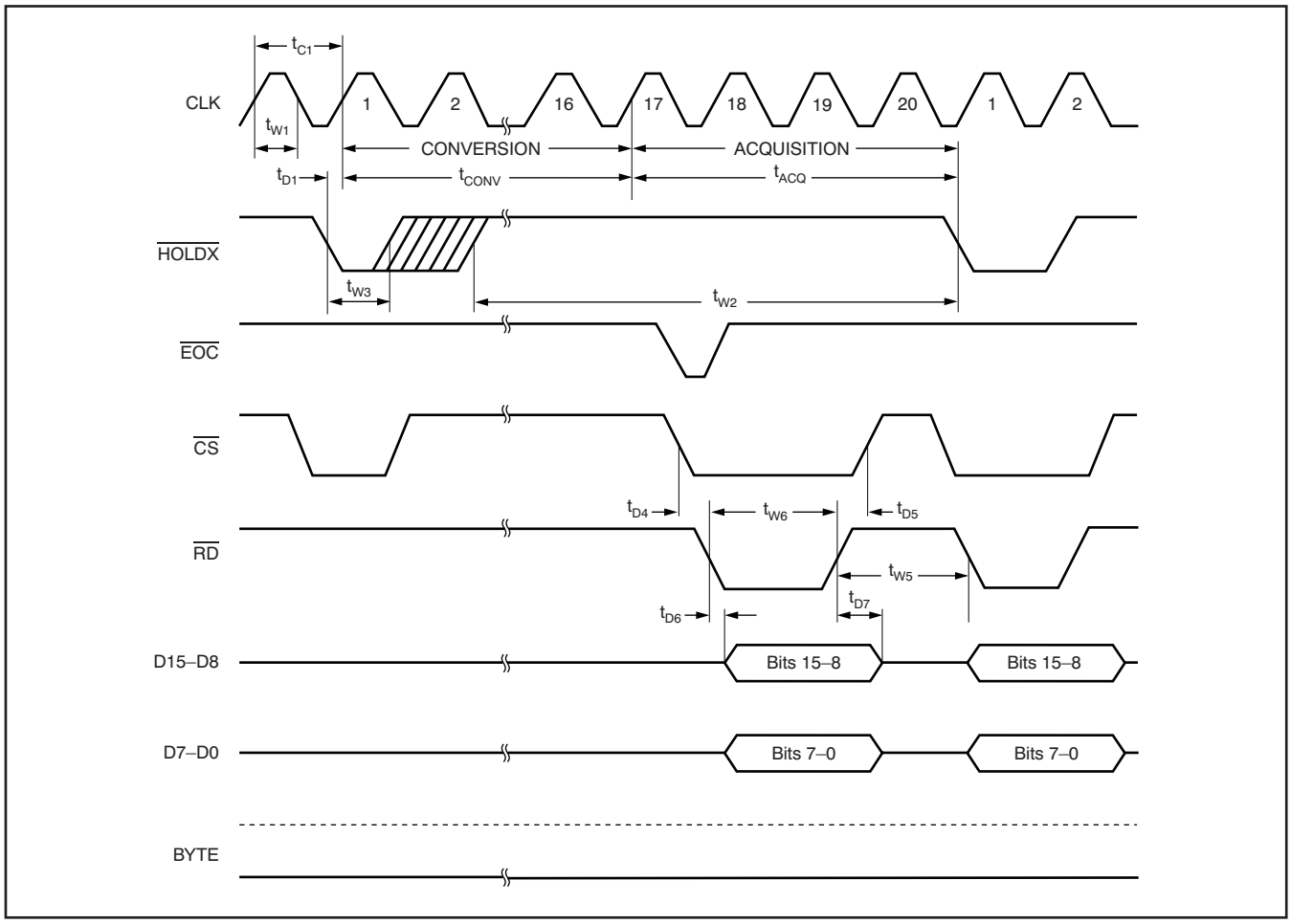

Figure 1. Read and Convert Timing

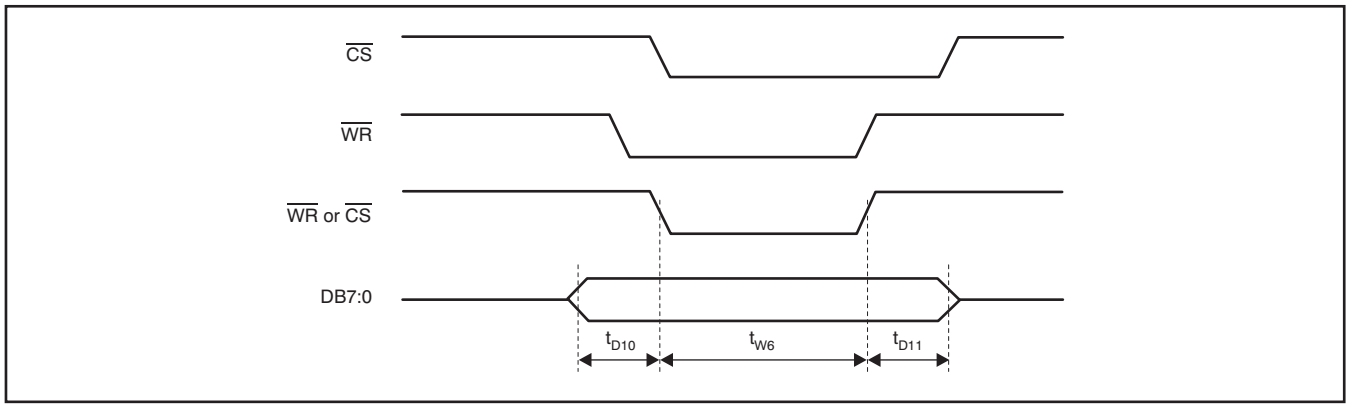

Figure 2. Write Timing

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TIMING CHARACTERISTICS(1)(2)(3)(4)

Over recommended operating free-air temperature range, T_{MIN} to T_{MAX}, AV_{DD} = 5V, REF_{IN} = REF_{OUT}, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, f_{SAMPLE} = 250kSPS, and BV_{DD} = 2.7 to 5V, unless otherwise noted,

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time				0.8	µs
t_{CONV}	Conversion time				3.2	µs
t_{C1}	Cycle time of CLK		200			ns
t_{D1}(5)	Delay time of rising edge of CLK after falling edge of $\overline{HOLDX}$		10			ns
t_{D2}	Delay time of first hold after $\overline{RESET}$	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	40			ns
t_{D4}	Delay time of falling edge of $\overline{RD}$ after falling edge of $\overline{CS}$		0			ns
t_{D5}	Delay time of rising edge of $\overline{CS}$ after rising edge of $\overline{RD}$		0			ns
t_{D6}	Delay time of data valid after falling edge of $\overline{RD}$	BV_{DD} = 5V	40			ns
		BV_{DD} = 3V	60			ns
t_{D7}	Delay time of data hold from rising edge of $\overline{RD}$	BV_{DD} = 5V	5			ns
		BV_{DD} = 3V	10			ns
t_{D8}	Delay time of $\overline{RD}$ high after $\overline{CS}$ low	BV_{DD} = 5V	50			ns
		BV_{DD} = 3V	60			ns
t_{D9}	Delay time of $\overline{RD}$ low after address setup	BV_{DD} = 5V	10			ns
		BV_{DD} = 3V	20			ns
t_{D10}	Delay time of data valid to $\overline{WR}$ low	BV_{DD} = 5V	10			ns
		BV_{DD} = 3V	20			ns
t_{D11}	Delay time of $\overline{WR}$ or $\overline{CS}$ high to data release	BV_{DD} = 5V	10			ns
		BV_{DD} = 3V	20			ns
t_{W1}	Pulse width CLK high time or low time		60			ns
t_{W2}	Pulse width of $\overline{HOLDX}$ high time to be recognized again	BV_{DD} = 5V	15			ns
		BV_{DD} = 3V	30			ns
t_{W3}	Pulse width of $\overline{HOLDX}$ low time	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	30			ns
t_{W4}	Pulse width of $\overline{RESET}$	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	40			ns
t_{W5}	Pulse width of $\overline{RD}$ high time	BV_{DD} = 5V	30			ns
		BV_{DD} = 3V	40			ns
t_{W6}	Pulse width of $\overline{RD}$ and $\overline{CS}$ both low time	BV_{DD} = 5V	50			ns
		BV_{DD} = 3V	70			ns

(1) Assured by design.
(2) All input signals are specified with rise time and fall time = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(3) See Figure 1.
(4) BYTE is asynchronous; when BYTE is 0, bits 15 to 0 appear at DB15 to DB0. When BYTE is 1, bits 15 to 8 appear on DB7 to DB0. $\overline{RD}$ may remain LOW between changes in BYTE.
(5) Only important when synchronization to clock is important.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, AV_{DD} = +5V, BV_{DD} = +3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, and f_{SAMPLE} = 250kSPS, unless otherwise noted.

INTEGRAL LINEARITY ERROR vs CODE (100kSPS)

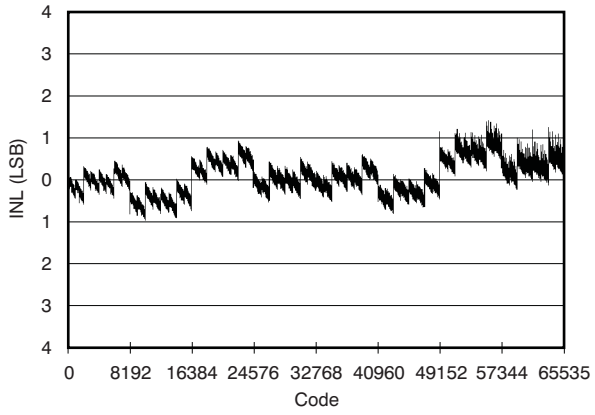

Figure 3.

DIFFERENTIAL LINEARITY ERROR vs CODE (100kSPS)

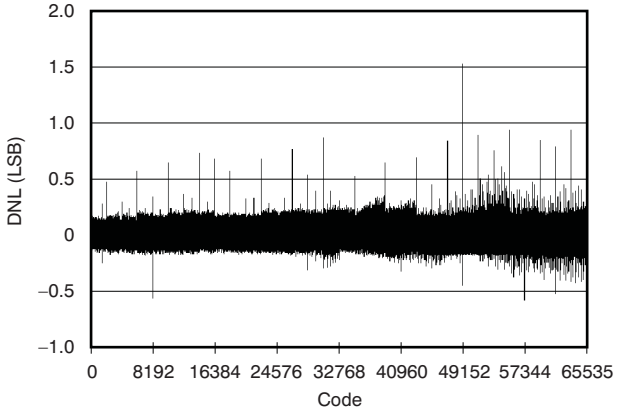

Figure 4.

MINIMUM AND MAXIMUM INL OF ALL CHANNELS vs TEMPERATURE (100kSPS)

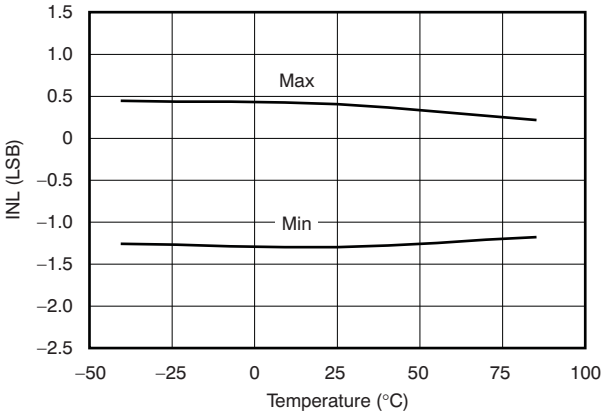

Figure 5.

MINIMUM AND MAXIMUM INL OF ALL CHANNELS vs TEMPERATURE (250kSPS)

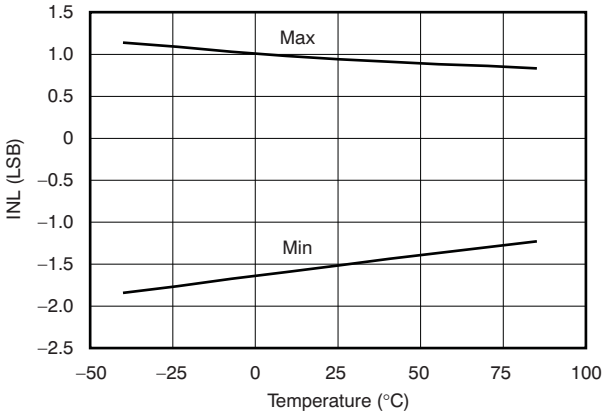

Figure 6.

MINIMUM AND MAXIMUM DNL OF ALL CHANNELS vs TEMPERATURE (100kSPS)

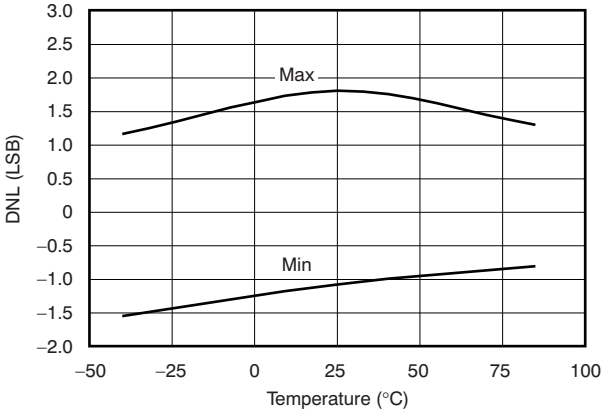

Figure 7.

MINIMUM AND MAXIMUM DNL OF ALL CHANNELS vs TEMPERATURE (250kSPS)

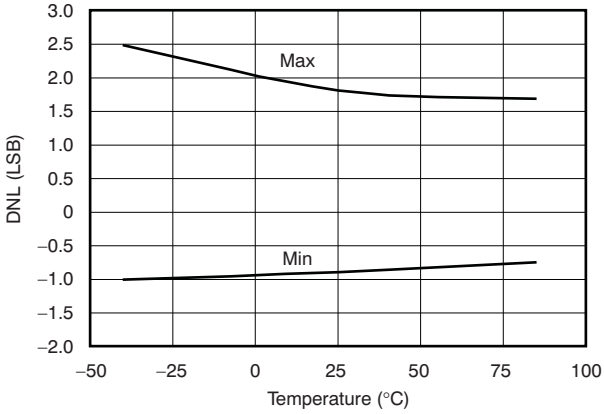

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = +5V, BV_{DD} = +3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, and f_{SAMPLE} = 250kSPS, unless otherwise noted.

FREQUENCY SPECTRUM (16384 point FFT, f_{IN} = 10kHz, –0.2dB)

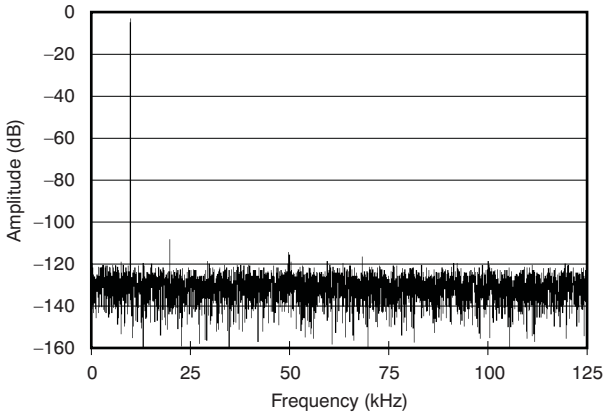

Figure 9.

FREQUENCY SPECTRUM (16384 point FFT, f_{IN} = 45kHz, –0.2dB)

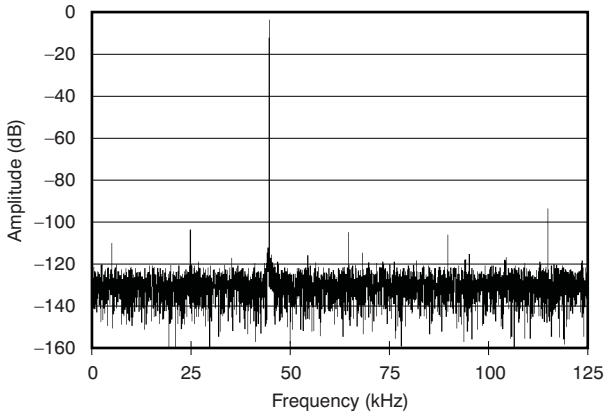

Figure 10.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY (ALL CHANNELS)

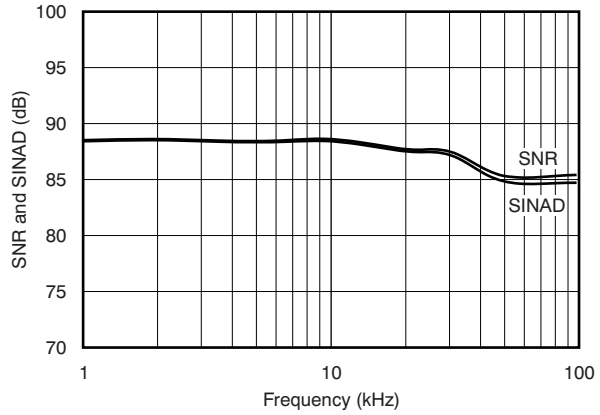

Figure 11.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY (ALL CHANNELS)

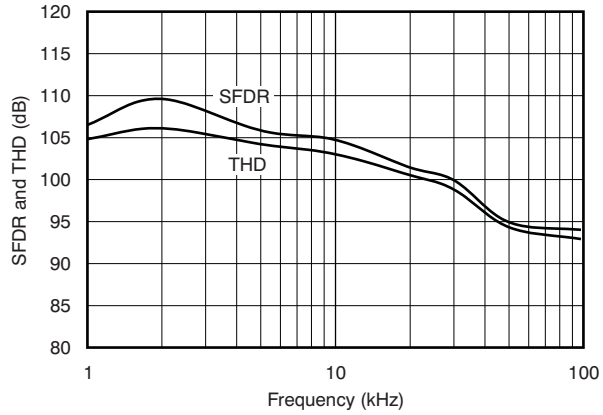

Figure 12.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE (ALL CHANNELS)

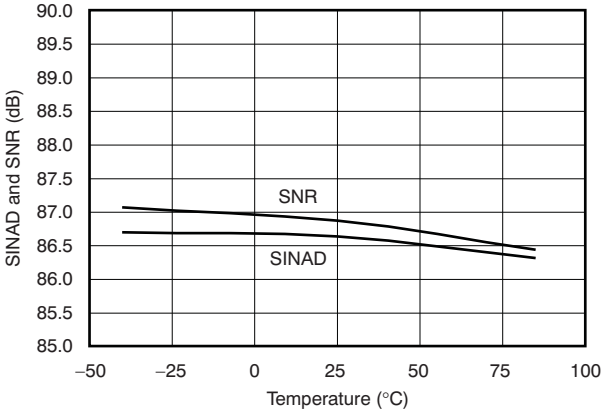

Figure 13.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE (ALL CHANNELS)

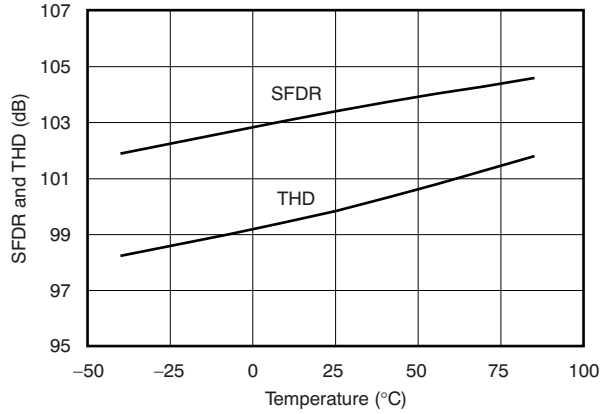

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = +5V, BV_{DD} = +3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, and f_{SAMPLE} = 250kSPS, unless otherwise noted.

OFFSET OF ALL CHANNELS vs TEMPERATURE

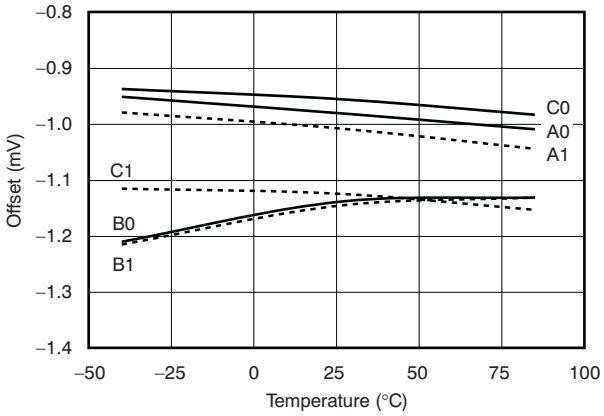

Figure 15.

OFFSET MATCHING OF CHANNEL PAIRS vs TEMPERATURE

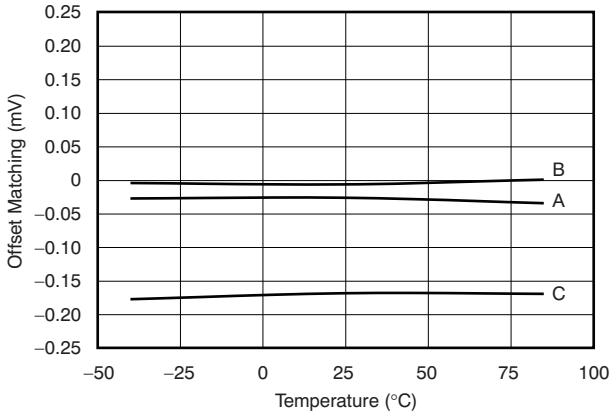

Figure 16.

GAIN ERROR OF ALL CHANNELS vs TEMPERATURE

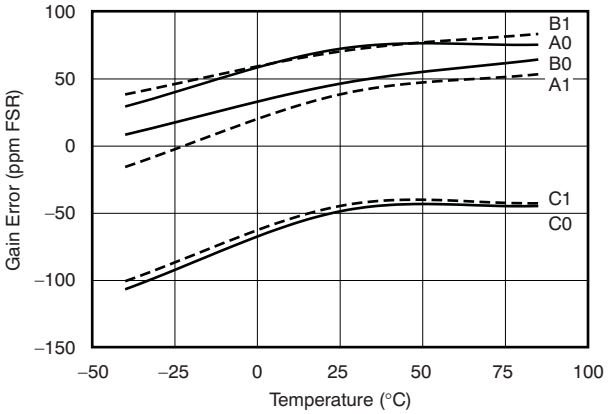

Figure 17.

GAIN-ERROR MATCHING OF CHANNEL PAIRS vs TEMPERATURE

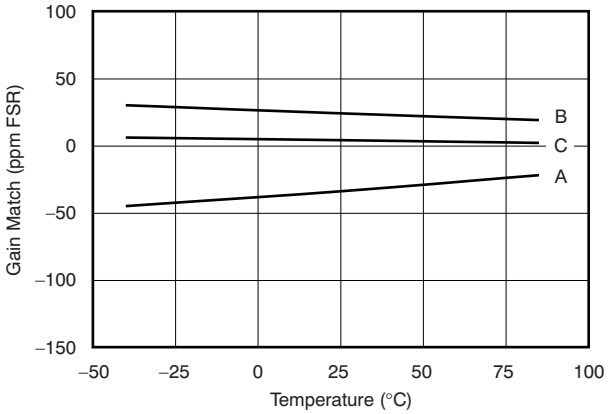

Figure 18.

REFERENCE VOLTAGE OUTPUT vs TEMPERATURE

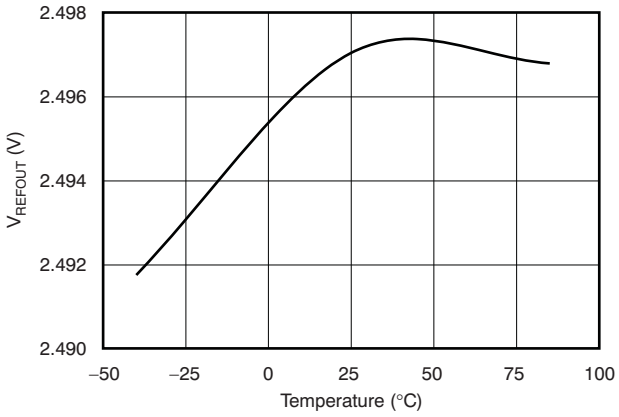

Figure 19.

ANALOG SUPPLY CURRENT vs TEMPERATURE

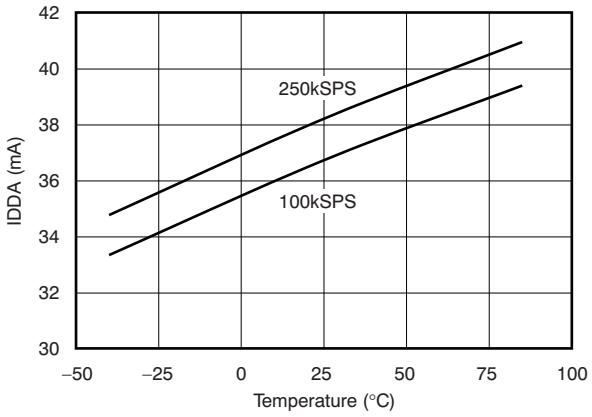

Figure 20.

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INTRODUCTION

The ADS8365 is a high-speed, low-power, six-channel simultaneous sampling and converting, 16-bit ADC that operates from a single +5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The ADS8365 contains six 4µs successive approximation ADCs, six differential sample-and-hold amplifiers, an internal +2.5V reference with REF_{IN} and REF_{OUT} pins, and a high-speed parallel interface. There are six analog inputs that are grouped into three channel pairs (A, B, and C). There are six ADCs, one for each input that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. Each pair of channels has a hold signal ($\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$) to allow simultaneous sampling on each channel pair, on four or on all six channels. The part accepts a differential analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered on the common-mode voltage (see the *Analog Input* section). The ADS8365 also accepts bipolar input ranges when a level shift circuit is used at the front end (see Figure 26).

A conversion is initiated on the ADS8365 by bringing the $\overline{HOLDX}$ pin low for a minimum of 20ns. $\overline{HOLDX}$ low places the sample-and-hold amplifiers of the X channels in the hold state simultaneously and the conversion process is started on each channel. The $\overline{EOC}$ output goes low for half a clock cycle when the conversion is latched into the output register. The data can be read from the parallel output bus following the conversion by bringing both $\overline{RD}$ and $\overline{CS}$ low. Conversion time for the ADS8365 is 3.2µs when a 5MHz external clock is used. The corresponding acquisition time is 0.8µs. To achieve the maximum output data rate (250kSPS), the read function can be performed during the next conversion. NOTE: This mode of operation is described in more detail in the *Timing and Control* section of this data sheet.

SAMPLE AND HOLD

The sample-and-hold amplifiers on the ADS8365 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 16-bit resolution. The input bandwidth of the sample-and-hold amplifiers is greater than the Nyquist rate (Nyquist = 1/2 of the sampling rate) of the ADC, even when the ADC is operated at its maximum throughput rate of 250kSPS. The typical small-signal bandwidth of the sample-and-hold amplifiers is 10MHz. Typical aperture delay time (or the time it takes for the ADS8365 to switch from the sample to the hold mode following the negative edge of the $\overline{HOLDX}$ signal) is 5ns. The average delta of repeated aperture delay values (also known as aperture jitter) is typically 50ps. These specifications reflect the ability of the ADS8365 to capture ac input signals accurately at the exact same moment in time.

REFERENCE

Under normal operation, REF_{OUT} (pin 61) can be directly connected to REF_{IN} (pin 62) to provide an internal +2.5V reference to the ADS8365. The ADS8365 can operate, however, with an external reference in the range of 1.5V to 2.6V, for a corresponding full-scale range of 3.0V to 5.2V, as long as the input does not exceed the AV_{DD} + 0.3V limit.

The reference output of the ADS8365 has an impedance of 2kΩ. The high impedance reference input can be driven directly. For an external resistive load, an additional buffer is required. A load capacitance of 0.1µF to 10µF should be applied to the reference output to minimize noise. If an external reference is used, the three input buffers provide isolation between the external reference and the CDACs. These buffers are also used to recharge all the capacitors of all CDACs during conversion.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8365: single-ended or differential, as shown in Figure 21 and Figure 22. When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode + V_{REF}) and the (common-mode $-V_{REF}$). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 23).

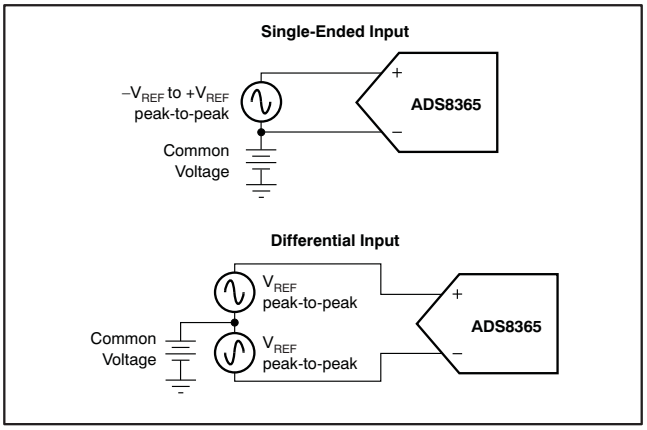

Figure 21. Methods of Driving the ADS8365 Single-Ended or Differential

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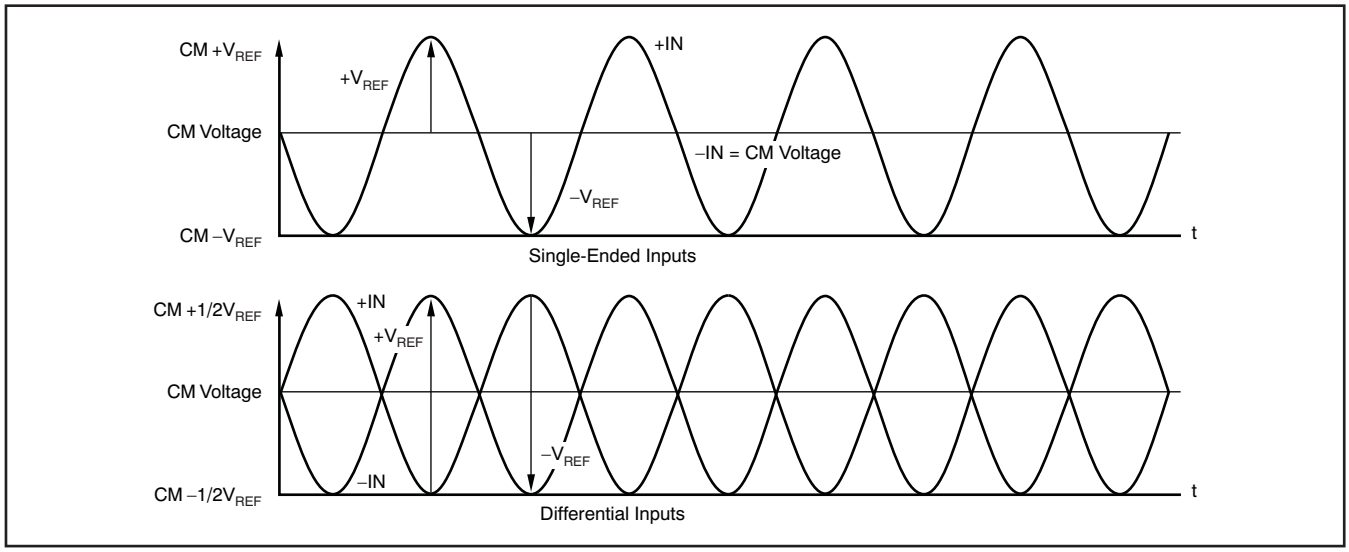

NOTES:

Common−mode voltage (Differential mode) = $\frac{(+IN) + (-IN)}{2}$. Common−mode voltage (Single−ended mode) = −IN

The maximum differential voltage between +IN and –IN of the ADS8365 is V_{REF}. See Figure 23 and Figure 24 for a further explanation of the common voltage range for single-ended and differential inputs.

Figure 22. Using the ADS8365 in the Single-Ended and Differential Input Modes

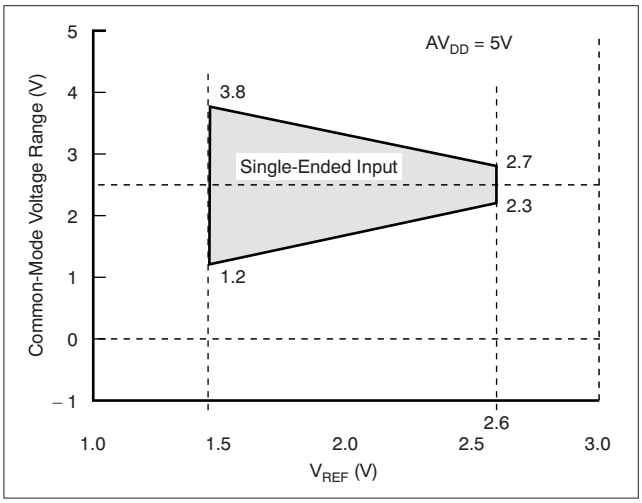

Figure 23. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}

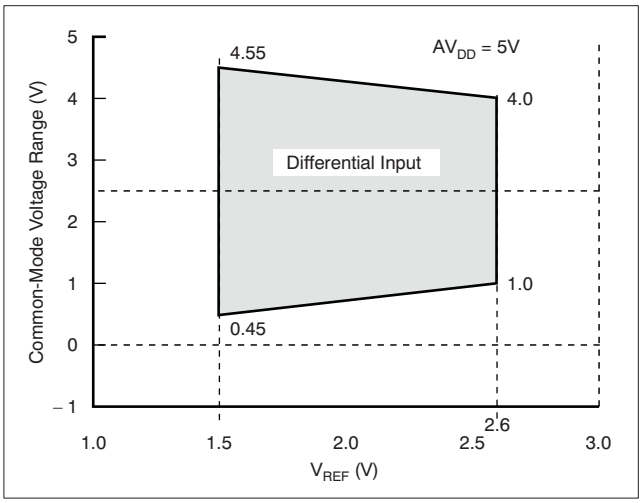

Figure 24. Differential Input: Common-Mode Voltage Range vs V_{REF}

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or: (+IN) – (–IN). The peak-to-peak amplitude of each input is $\pm 1/2V_{REF}$ around this common voltage. However, since the inputs are 180° out-of-phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs, as shown in Figure 24.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Often, a small capacitor (20pF) between the positive and negative input helps to match the impedance. Otherwise, a mismatch may result in offset error, which will change with both temperature and input voltage.

The input current on the analog inputs depends on a number of factors, such as sample rate or input

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voltage. Essentially, the current into the ADS8365 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 16-bit settling level within three clock cycles if the minimum acquisition time is used. When the converter goes into the hold mode, the input impedance is greater than 1GΩ. Care must be taken regarding the absolute analog input voltage. The +IN and –IN inputs should always remain within the range of AGND – 0.3V to AV_{DD} + 0.3V.

The OPA365 is a good choice for driving the analog inputs in a 5V, single-supply application.

TRANSITION NOISE

The transition noise of the ADS8365 itself is low, as shown in Figure 25 These histograms were generated by applying a low-noise dc input and initiating 8000 conversions. The digital output of the ADC will vary in output code due to the internal noise of the ADS8365; this feature is true for all 16-bit, successive approximation register (SAR) type ADCs. Using a histogram to plot the output codes, the distribution should appear bell-shaped, with the peak of the bell curve representing the nominal code for the input value. The ±1σ , ±2σ , and ±3σ distributions represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6, yielding the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. Remember, in order to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

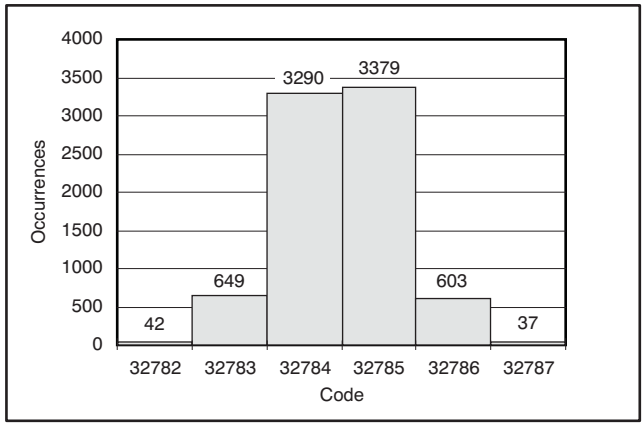
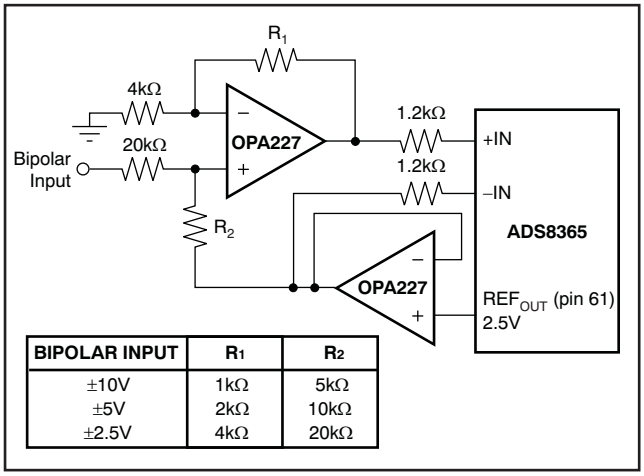


Figure 25. 8000 Conversion Histogram of a DC Input

BIPOLAR INPUTS

The differential inputs of the ADS8365 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the common-mode voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring four, high-precision external resistors, the ADS8365 can be configured to accept a bipolar input range. The conventional ±2.5V, ±5V, and ±10V input ranges could be interfaced to the ADS8365 using the resistor values shown in Figure 26.



BIPOLAR INPUT	R1	R2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

Figure 26. Level Shift Circuit for Bipolar Input Ranges

TIMING AND CONTROL

The ADS8365 uses an external clock (CLK, pin 28) that controls the conversion rate of the CDAC. With a 5MHz external clock, the ADC sampling rate is 250kSPS which corresponds to a 4µs maximum throughput time. Acquisition and conversion take a total of 20 clock cycles.

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THEORY OF OPERATION

The ADS8365 contains six 16-bit ADCs that can operate simultaneously in pairs. The three hold signals ($\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$) initiate the conversion on the specific channels. A simultaneous hold on all six channels can occur with all three hold signals strobed together. The converted values are saved in six registers. For each read operation, the ADS8365 outputs 16 bits of information (16 data or 3 channel address, data valid, and some synchronization information). The address/mode signals (A0, A1, and A2) select how the data are read from the ADS8365. These address/mode signals can define a selection of a single channel, a cycle mode that cycles through all channels, or a FIFO mode that sequences the data determined by the order of the hold signals. The FIFO mode will allow the six registers to be used by a single-channel pair; therefore, three locations for CH X0 and three locations for CH X1 can be updated before they are read from the device.

EXPLANATION OF CLOCK, $\overline{RESET}$, FD, AND $\overline{EOC}$ PINS

Clock An external clock has to be provided for the ADS8365. The maximum clock frequency is 5MHz. The minimum clock cycle is 200ns (see Figure 1, t_{C1}), and the clock has to remain high (Figure 1, t_{W1}) or low for at least 60ns.

$\overline{RESET}$ Bringing the $\overline{RESET}$ signal low will reset the ADS8365. Resetting clears the control register and all the output registers, aborts any conversion in process, and closes the sampling switches. The reset signal must stay low for at least 20ns (see Figure 27, t_{W4}). The reset signal should be back high for at least 20ns (Figure 27, t_{D2}) before starting the next conversion (negative hold edge).

$\overline{EOC}$ End of conversion goes low when new data from the internal ADC are latched into the output registers, which usually happens 16.5 clock cycles after hold initiated the conversion. It remains low for half a clock cycle. If more than one channel pair is converted simultaneously, the A-channels get stored to the registers first (16.5 clock cycles after hold), followed by the B-channels one clock cycle later, and finally the C-channels another clock cycle later. If a reading (both $\overline{RD}$ and $\overline{CS}$ are low) is in process, then the latch process is delayed until the read operation is finished.

FD First data or A0 data are high if channel A0 is chosen to be read next. In FIFO mode, the channel (X0) that is written to the FIFO first is latched into the A0 register. For example, when the FIFO is empty, FD is 0. The first result latched into the FIFO register A0 is, therefore, chosen to be read next, and FD rises. After the first channel is read (one to three read cycles, depending on BYTE and ADD), FD goes low again.

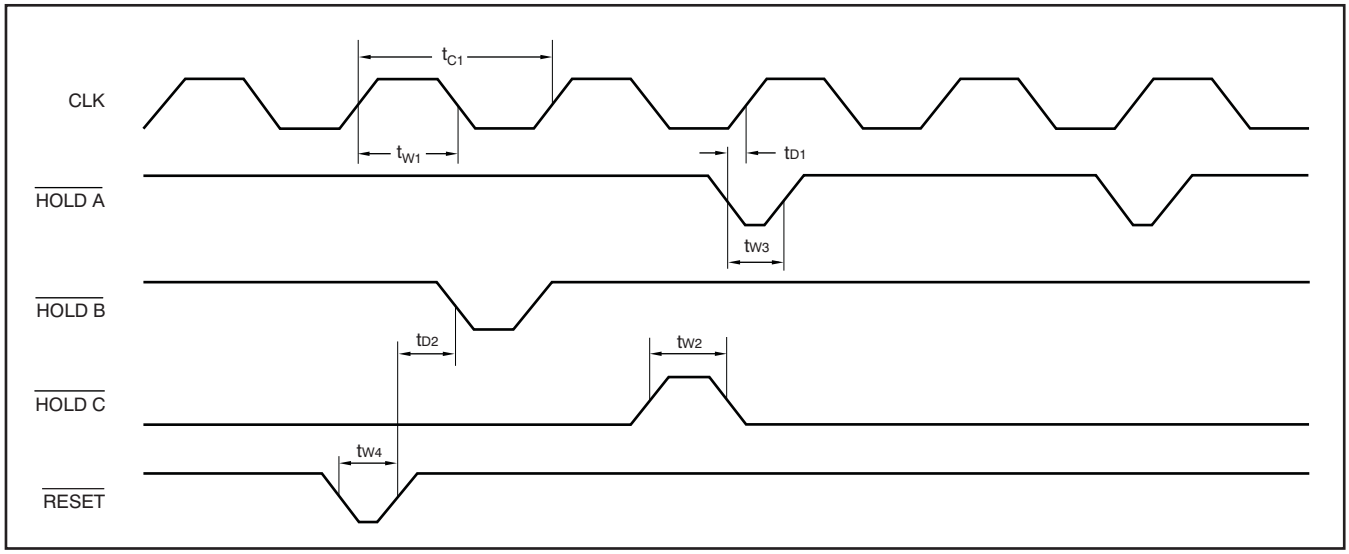

Figure 27. Start of the Conversion

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START OF A CONVERSION AND READING DATA

By bringing one, two, or all three of the $\overline{\text{HOLDX}}$ signals low, the input data of the corresponding channel X are immediately placed in the hold mode (5ns). The conversion of this channel X follows with the next rising edge of clock. If it is important to detect a hold command during a certain clock-cycle, then the falling edge of the hold signal has to occur at least 10ns before the rising edge of clock, as shown in Figure 27, t_{D1}. The hold signal can remain low without initiating a new conversion. The hold signal must be high for at least 15ns (as shown in Figure 27, t_{W2}) before it is brought low again, and hold must stay low for at least 20ns (Figure 27, t_{W3}).

Once a particular hold signal goes low, further impulses of this hold signal are ignored until the conversion is finished or the device is reset. When the conversion is finished (after 16 clock cycles) the sampling switches close and sample the selected channel. The start of the next conversion must be delayed to allow the input capacitor of the ADS8365 to be fully charged. This delay time depends on the driving amplifier, but should be at least 800ns.

The ADS8365 can also convert one channel continuously (see Figure 28). Therefore, $\overline{\text{HOLDA}}$ and $\overline{\text{HOLDC}}$ are kept high all the time. To gain acquisition time, the falling edge of $\overline{\text{HOLDB}}$ takes place just before the rising edge of clock. One conversion requires 20 clock cycles. Here, data are read after the next conversion is initiated by $\overline{\text{HOLDB}}$. To read data from channel B, A1 is set high and A2 is low. Since A0 is low during the first reading (A2 A1 A0 = 010), data B0 are put to the output. Before the second $\overline{\text{RD}}$, A0 switches high (A2 A1 A0 = 011) so that data from channel B1 are read, as shown in Table 1. However, reading data during the conversion or on a falling hold edge might cause a loss in performance.

Table 1. Address Control for $\overline{\text{RD}}$ Functions

A2	A1	A0	CHANNEL TO BE READ
0	0	0	CH A0
0	0	1	CH A1
0	1	0	CH B0
0	1	1	CH B1
1	0	0	CH C0
1	0	1	CH C1
1	1	0	Cycle mode reads registers CH A0 to CH C1 on successive transitions of the read line
1	1	1	FIFO mode

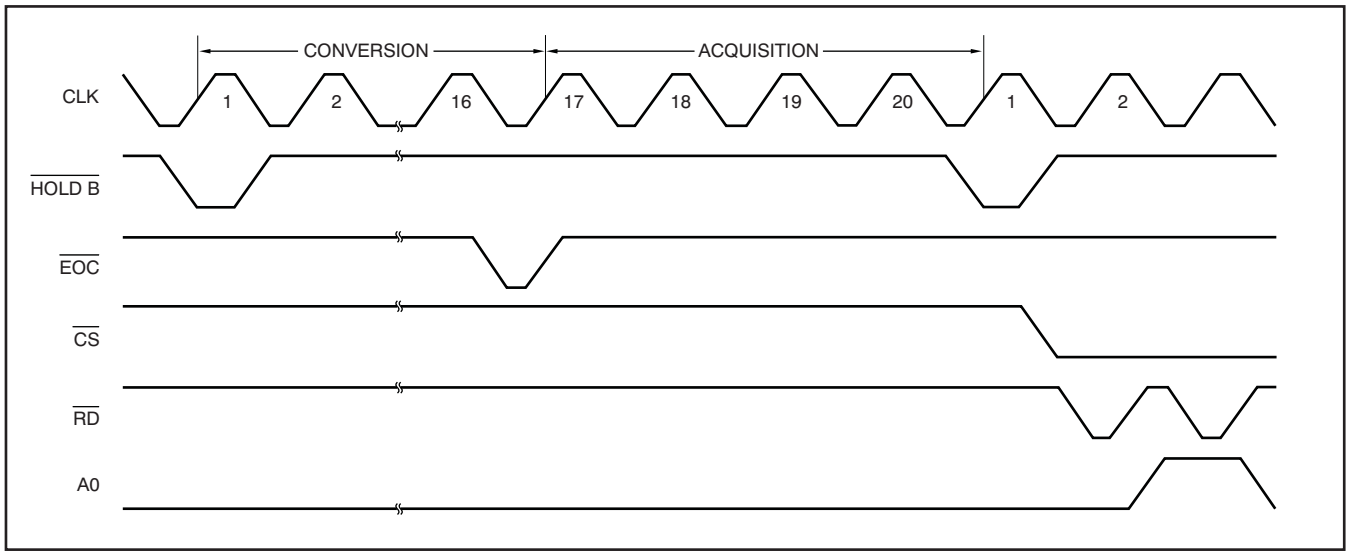

Figure 28. Timing of One Conversion Cycle

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Reading data ($\overline{RD}$ and $\overline{CS}$)

In general, the channel/data outputs are in tri-state. Both $\overline{CS}$ and $\overline{RD}$ must be low to enable these outputs. $\overline{RD}$ and $\overline{CS}$ must stay low together for at least 40ns (see Figure 1, t_{D6}) before the output data are valid. $\overline{RD}$ must remain HIGH for at least 30ns (see Figure 1, t_{W5}) before bringing it back low for a subsequent read command.

The new data are latched into its output register 16.5 clock cycles after the start of a conversion (next rising edge of clock after the falling edge of $\overline{HOLDX}$). Even if the ADS8365 is forced to wait until the read process is finished ($\overline{RD}$ signal going high) before the new data are latched into its output register, the possibility still exists that the new data was latched to the output register just before the falling edge of RD. If a read process is initiated around 16.5 clock cycles after the conversion started, $\overline{RD}$ and $\overline{CS}$ should stay low for at least 50ns (see Figure 1, t_{W6}) to get the new data stored to its register and switched to the output.

$\overline{CS}$ being low tells the ADS8365 that the bus on the board is assigned to the ADS8365. If an ADC shares a bus with digital gates, there is a possibility that digital (high-frequency) noise will be coupled into the ADC. If the bus is just used by the ADS8365, $\overline{CS}$ can be hardwired to ground. Reading data at the falling edge of one of the $\overline{HOLDX}$ signals might cause noise.

BYTE

If there is only an 8-bit bus available on a board, then BYTE can be set high (see Figure 29). In this case, the lower eight bits can be read at the output pins D15 to D8 or D7 to D0 at the first $\overline{RD}$ signal, and the higher bits after the second $\overline{RD}$ signal. If the ADS8365 is used in the cycle or the FIFO mode, then the address and data valid information is added to the data (if ADD is high). In this case, the address will be read first, then the lower eight bits, and finally the higher eight bits. If BYTE is low, then the ADS8365 operates in the 16-bit output mode. Here, data are read between pins DB15 and DB0. As long as ADD is low, with every $\overline{RD}$ impulse, data from a new channel are brought to the output. If ADD is high and the cycle or the FIFO mode is chosen; the first output word contains the address, while the second output word contains the 16-bit data.

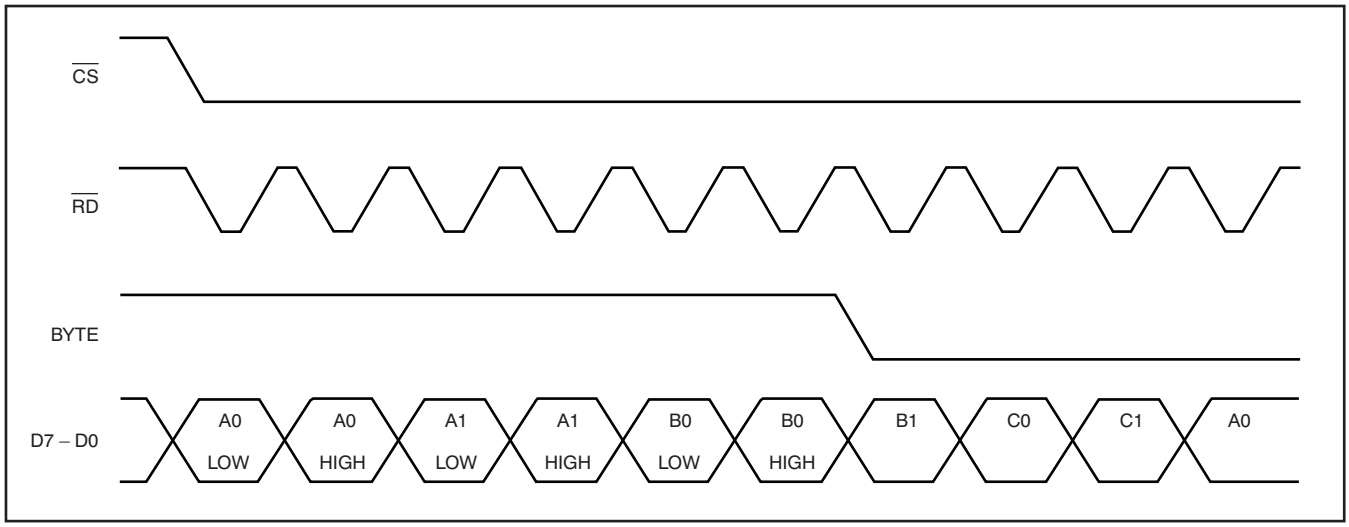

Figure 29. Reading Data in Cycling Mode

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ADD Signal

In the cycle and the FIFO mode, it might be desirable to have address information with the 16-bit output data. Therefore, ADD can be set high. In this case, two $\overline{RD}$ signals (or three readings if the part is operated with BYTE being high) are necessary to read data of one channel, while the ADS8365 provides channel information on the first $\overline{RD}$ signal (see Table 2 and Table 3).

Soft Trigger Mode

Signals NAP, ADD, A0, A1, A2, $\overline{RESET}$, $\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$ are accessible through the data bus and control word. Bits NAP, ADD, A0, A1 and A2 are in an *OR* configuration with hardware pins. When software configuration is used, these pins must be connected to ground. Conversely, the $\overline{RESET}$, $\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$ bits are in a NAND configuration with the hardware pins. When software configuration is used, these pins must be connected to BV_{DD}.

If conversion timing between ADCs is not critical, Soft Trigger mode can allow all three $\overline{HOLDX}$ signals to be triggered simultaneously. This simultaneous triggering can be done by tying all three $\overline{HOLDX}$ pins high, and issuing a write ($\overline{CS}$ and $\overline{WR}$ low) with the DB0, DB1, DB2, and DB7 bits low, and the reset bit (DB3) high. Writing a low to the reset bit (DB3) while the RESET pin is high forces a device reset, and all $\overline{HOLDX}$ signals that occur during that time are ignored.

The $\overline{HOLDX}$ signals start conversion automatically on the next clock cycle. The format of the two words that can be written to the ADS8365 are shown in Table 4.

Bits DB5 and DB4 do not have corresponding hardware pins. Bit DB5 = 1 enables Powerdown mode. Bit DB4 = 1 inverts the MSB of the output data, putting the output data in two's complement format. When DB4 is low, the data is in straight binary format.

Table 2. Overview of the Output Formats Depending on Mode When ADD = 0

ADD = 0	BYTE = 0		BYTE = 1		
A2 A1 A0	1st $\overline{RD}$	2nd $\overline{RD}$	1st $\overline{RD}$	2nd $\overline{RD}$	3rd $\overline{RD}$
000	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
001	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
010	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
011	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
100	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
101	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
110	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
111	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$

Table 3. Overview of the Output Formats Depending on Mode When ADD = 1

ADD = 1	BYTE = 0		BYTE = 1		
A2 A1 A0	1st $\overline{RD}$	2nd $\overline{RD}$	1st $\overline{RD}$	2nd $\overline{RD}$	3rd $\overline{RD}$
000	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
001	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
010	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
011	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
100	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
101	DB15...DB0	No 2nd $\overline{RD}$	DB7...DB0	DB15...DB8	No 3rd $\overline{RD}$
110	1000 0000 0000 DV A2 A1 A0	DB15...DB0	DV A2 A1 A0 DB3 DB2 DB0	DB7...DB0	DB15...DB8
111	1000 0000 0000 DV A2 A1 A0	DB15...DB0	DV A2 A1 A0 DB3 DB2 DB0	DB7...DB0	DB15...DB8

Table 4. Control Register Bits

DB7 (MSB)	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
1	NAP	PD	Invert MSB	ADD	A2	A1	A0
0	X	X	X	$\overline{RESET}$	$\overline{HOLDA}$	$\overline{HOLDB}$	$\overline{HOLDC}$

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NAP AND POWERDOWN MODE CONTROL

In order to minimize power consumption when the ADS8365 is not in use, two low-power options are available. Nap mode minimizes power without shutting down the biasing circuitry and internal reference, allowing immediate recovery after it is disabled. It can be enabled by either the NAP pin going high, or setting DB6 in the data register high. Enabling Powerdown mode results in lower power consumption than Nap mode, but requires a short recovery period after disabling. It can only be enabled by setting DB5 in the data register high.

GETTING DATA

Flexible Output Modes: A0 A1, and A2.

The ADS8365 has three different output modes that are selected with A2, A1, and A0. The A2, A1 and A0 pins are held with a transparent latch that triggers on a falling edge of the $\overline{RD}$ pin negative-ANDed with the $\overline{CS}$ pin (that is, if either $\overline{RD}$ or $\overline{CS}$ is low, the falling edge of the other will latch A0-2).

When (A2, A1, A0) = 000 to 101, a particular channel can be directly addressed (see Table 1 and Figure 30). The channel address should be set at least 10ns (see Figure 30, t_{D9}) before the falling edge of $\overline{RD}$ and should not change as long as $\overline{RD}$ is low. In this standard address mode, ADD will be ignored, but should be connected to either ground or supply.

When (A2, A1, A0) = 110, the interface is running in a cycle mode (see Figure 29). Here, data 7 down to data 0 of channel A0 is read on the first $\overline{RD}$ signal, and data 15 down to data 8 on the second as BYTE is high. Then A1 on the second $\overline{RD}$, followed by B0, B1, C0, and finally, C1 before reading A0 again. Data from channel A0 are brought to the output first after a reset signal, or after powering up the device. The third mode is a FIFO mode that is addressed with (A2, A1, A0 = 111). Data of the channel that is converted first is read first. So, if a particular channel pair is most interesting and is converted more frequently (for example, to get a history of a particular channel pair), then there are three output registers per channel available to store data.

If all the output registers are filled up with unread data and new data from an additional conversion must be latched in, then the oldest data is discarded. If a read process is going on ($\overline{RD}$ signal low) and new data must be stored, then the ADS8365 waits until the read process is finished ($\overline{RD}$ signal going high) before the new data gets latched into its output register. Again, with the ADD signal, it can be chosen whether the address should be added to the output data.

New data is always written into the next available register. At t_0 (see Figure 31), the reset deletes all the existing data. At t_1, the new data of the channels A0 and A1 are put into registers 0 and 1. At t_2, a dummy read ($\overline{RD}$ low) is performed to latch the address data correctly. At t_3, the read process of channel A0 data is finished; therefore, these data are dumped and A1 data are shifted to register 0. At t_4, new data are available, this time from channels B0, B1, C0, and C1. These data are written into the next available registers (registers 1, 2, 3, and 4).

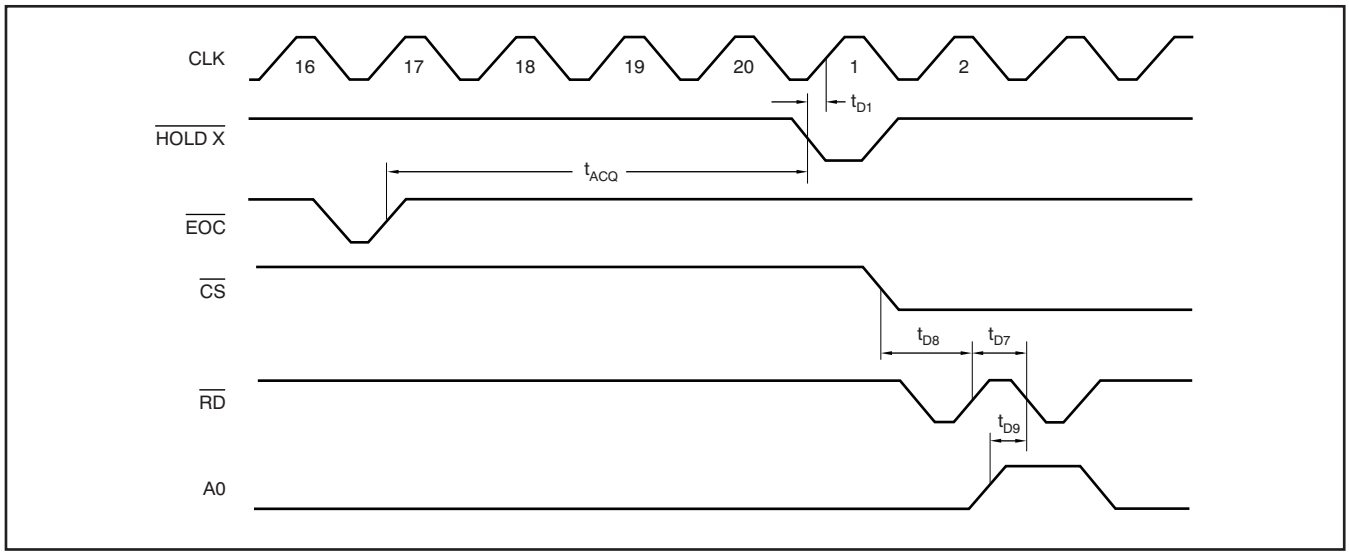

Figure 30. Timing for Reading Data

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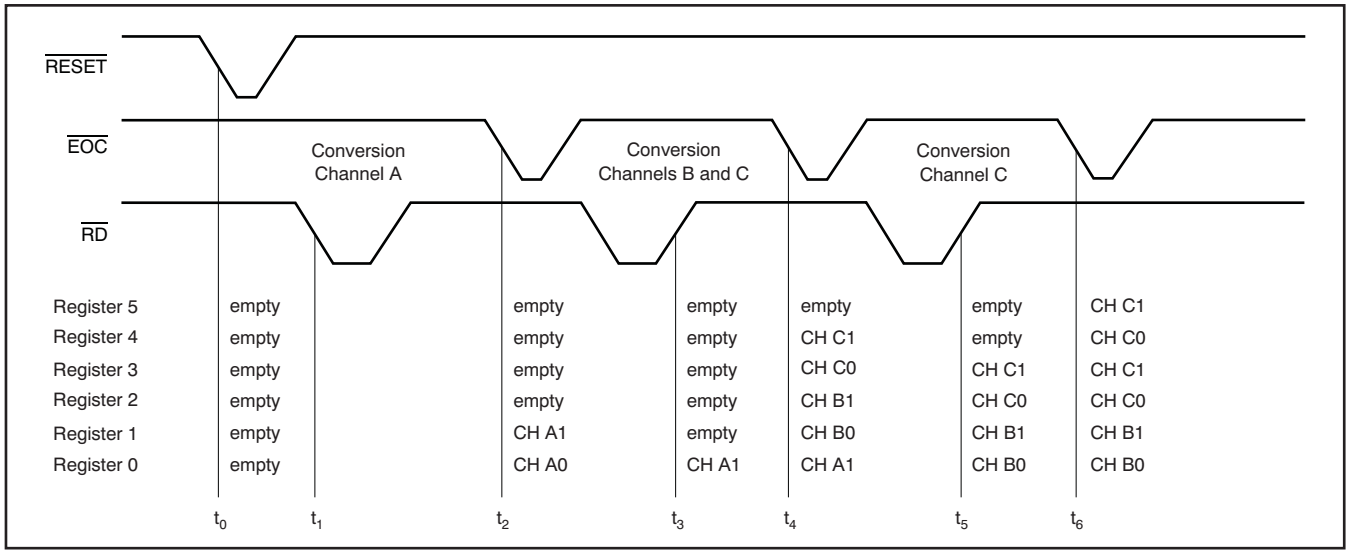

Figure 31. Functionality Diagram of the FIFO Registers

On t_5, the new read process of channel A1 data is finished. The new data of channel C0 and C1 at t_6 are put on top (registers 4 and 5).

In Cycle mode and in FIFO mode, the ADS8365 offers the ability to add the address of the channel to the output data. Since there is only a 16-bit bus available (or 8-bit bus in the case BYTE is high), an additional $\overline{RD}$ signal is necessary to get the information (see Table 2 and Table 3).

In FIFO mode, a dummy read signal ($\overline{RD}$) is required after a reset signal to set the address bits appropriately; otherwise, the first conversion will not be valid. This is only necessary in FIFO mode.

The Output Code (DB15 …DB0)

In the standard address mode (A2 A1 A0 = 000…101), the ADS8365 has a 16-bit output word on pins DB15…DB0, if BYTE = 0. If BYTE = 1, then two $\overline{RD}$ impulses are necessary to first read the lower bits, and then the higher bits on either DB7…DB0 or DB15...DB8.

If the ADS8365 operates in Cycle or in FIFO mode and ADD is set high, then the address of the channel (A2A1A0) and a data valid (DV) bit are added to the data. If BYTE = 0, then the data valid and the address of the channel is active during the first $\overline{RD}$ impulse (1000 0000 0000 DV A2 A1 A0). During the second $\overline{RD}$, the 16-bit data word can be read (DB15…DB0). If BYTE = 1, then three $\overline{RD}$ impulses are needed. On the first $\overline{RD}$ impulse, data valid, the three address bits, and data bits DB3…DB0 (DV, A2, A1, A0, DB3, DB2, DB1, DB0) are read, followed by the eight lower bits of the 16-bit data word (db7…db0), and finally the higher eight data bits (DB15…DB8). 1000 0000 0000 is added before the address in case BYTE = 0, and DB3…DB0 is added after the address if BYTE = 1. This provides the possibility to check if the counting of the $\overline{RD}$ signals inside the ADS8365 are still tracking with the external interface (see Table 2 and Table 3).

The data valid bit is useful for the FIFO mode. Valid data can simply be read until the data valid bit equals 0. The three address bits are listed in Table 5. If the FIFO is empty, 16 zeroes are loaded to the output.

Table 5. Address Bit in the Output Data

DATA FROM ...	A2	A1	A0
Channel A0	0	0	0
Channel A1	0	0	1
Channel B0	0	1	0
Channel B1	0	1	1
Channel C0	1	0	0
Channel C1	1	0	1

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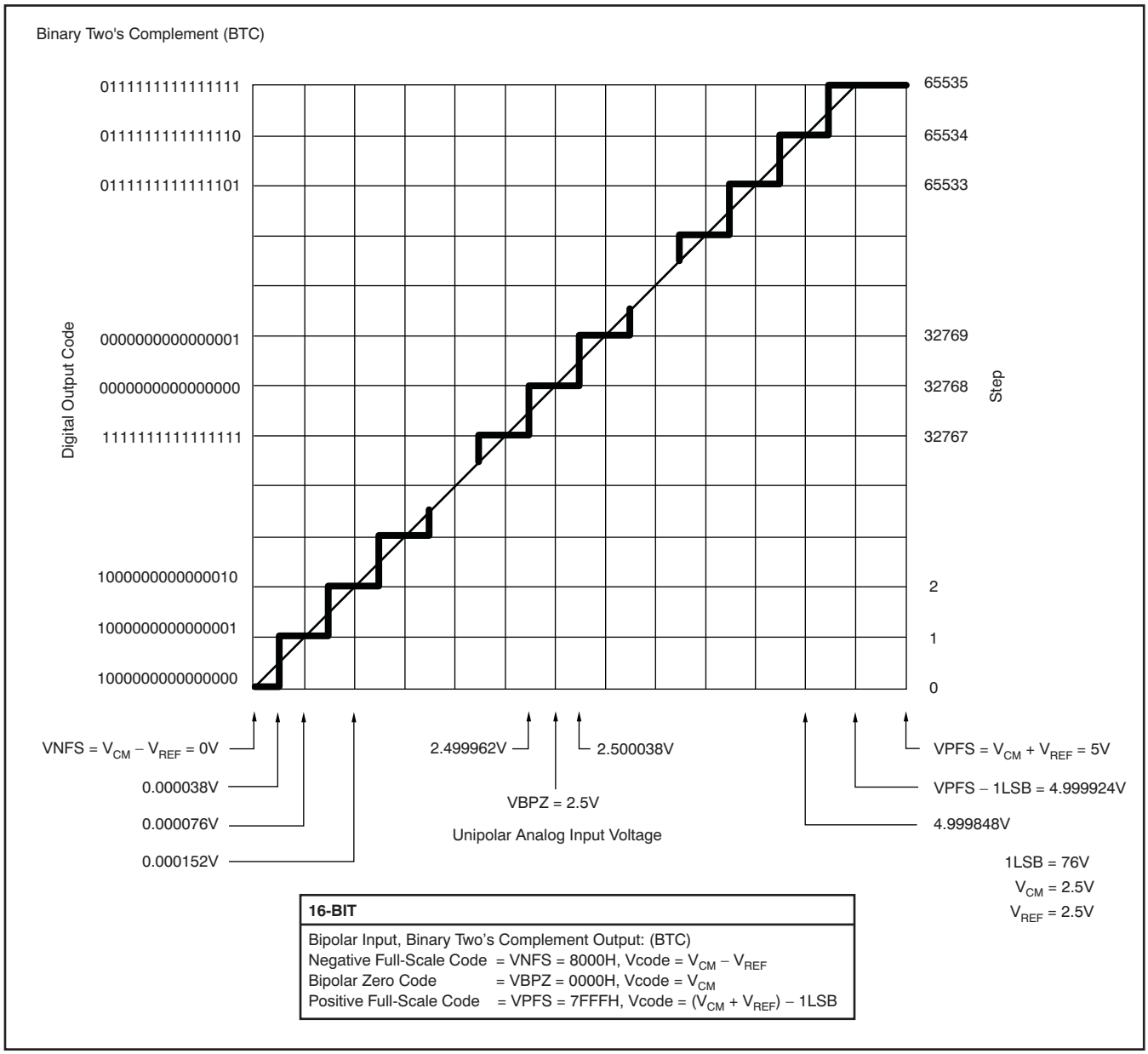

Figure 32. Ideal Conversion Characteristics (Condition: Single-Ended, V_{CM} = chXX– = 2.5V, V_{REF} = 2.5V)

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LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8365 circuitry. This recommendation is particularly true if the CLK input is approaching the maximum throughput rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLK input.

With this information in mind, power to the ADS8365 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. On average, the ADS8365 draws very little current from an external reference because the reference voltage is internally buffered. A bypass capacitor of 0.1µF and 10µF are suggested when using the internal reference (tie pin 61 directly to pin 62).

GROUNDING

The AGND pins should be connected to a clean ground point. In all cases, this point should be the analog ground. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power-supply entry point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry. Three signal ground pins (SGND) are the input signal grounds that are on the same potential as analog ground.

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APPLICATION INFORMATION

Different connection diagrams to DSPs or microcontrollers are shown in Figure 33 through Figure 39.

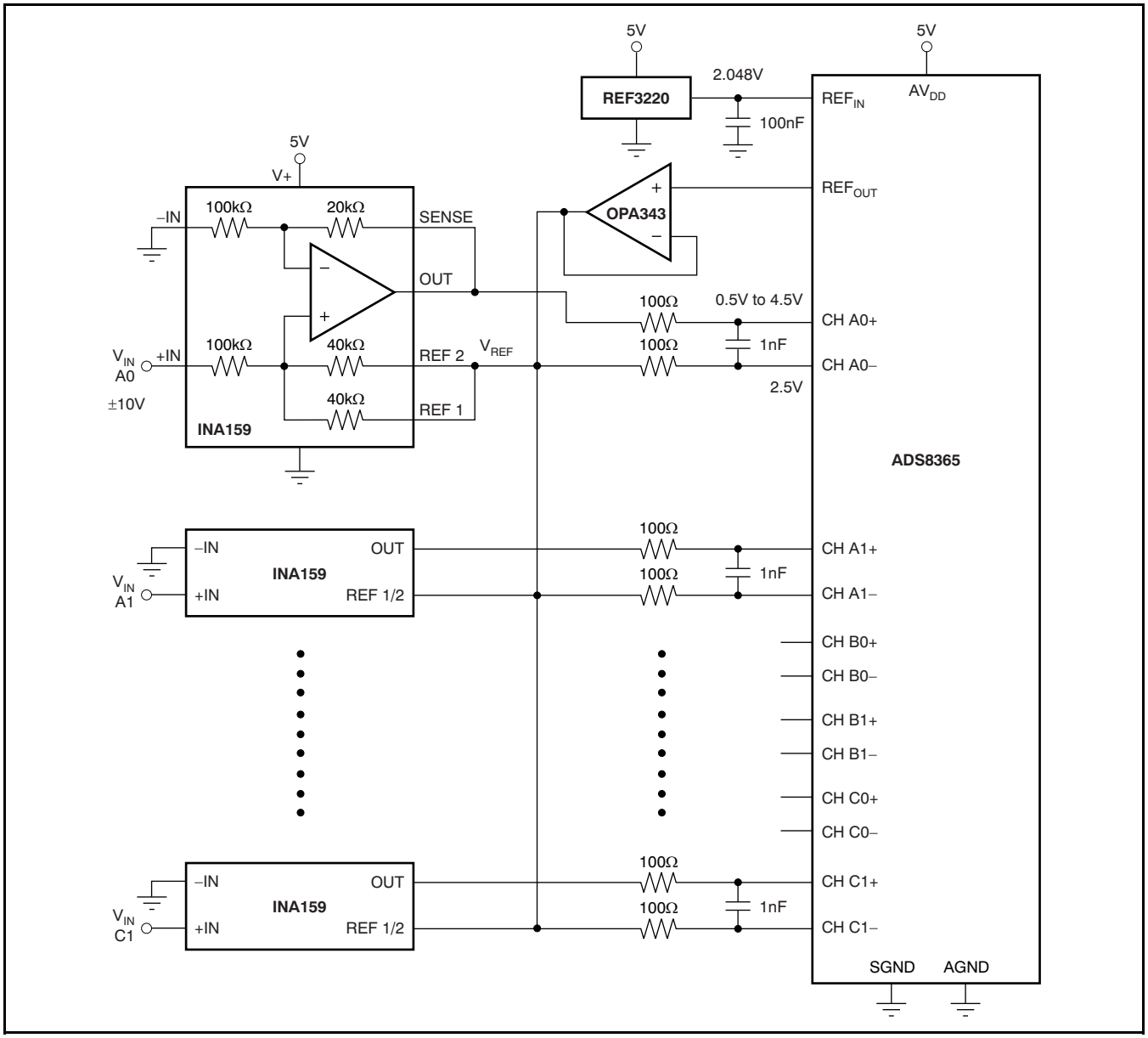

Figure 33. ±10V Input Range By Using the INA159

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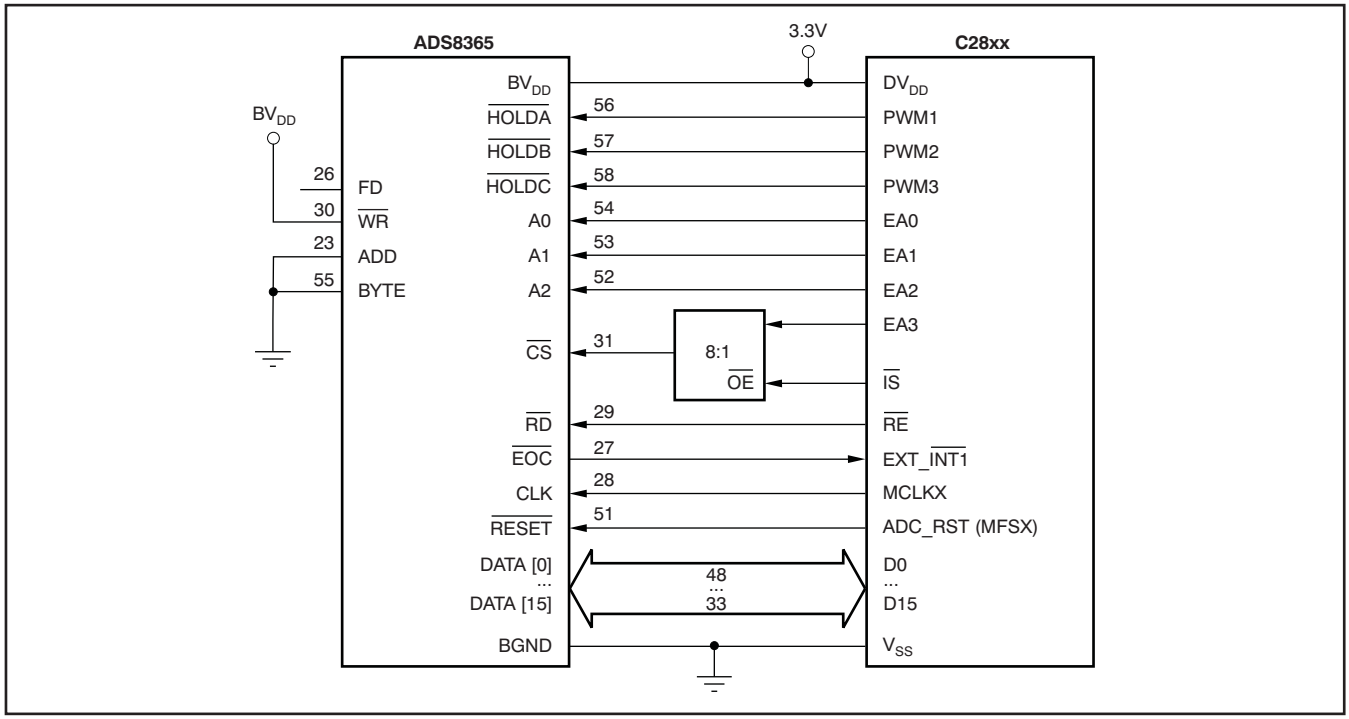

Figure 34. Typical C28xx Connection (Hardware Control)

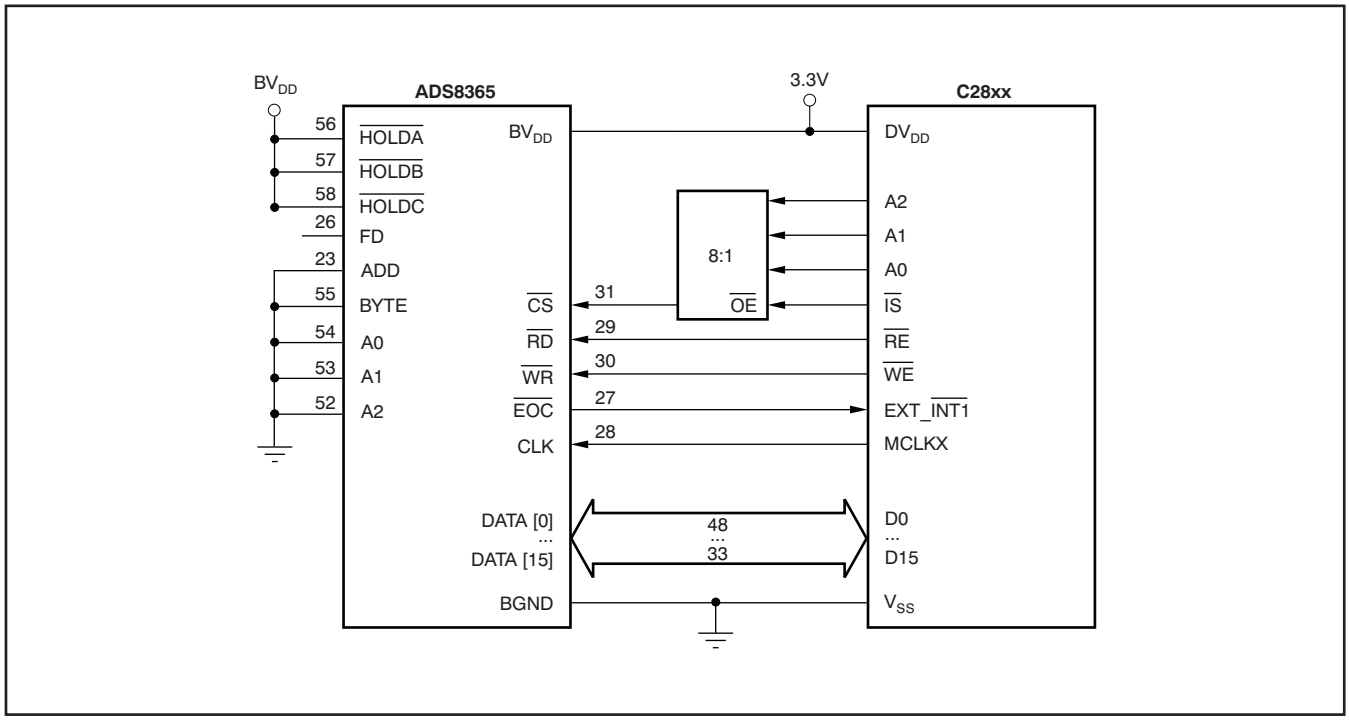

Figure 35. Typical C28xx Connection (Software Control)

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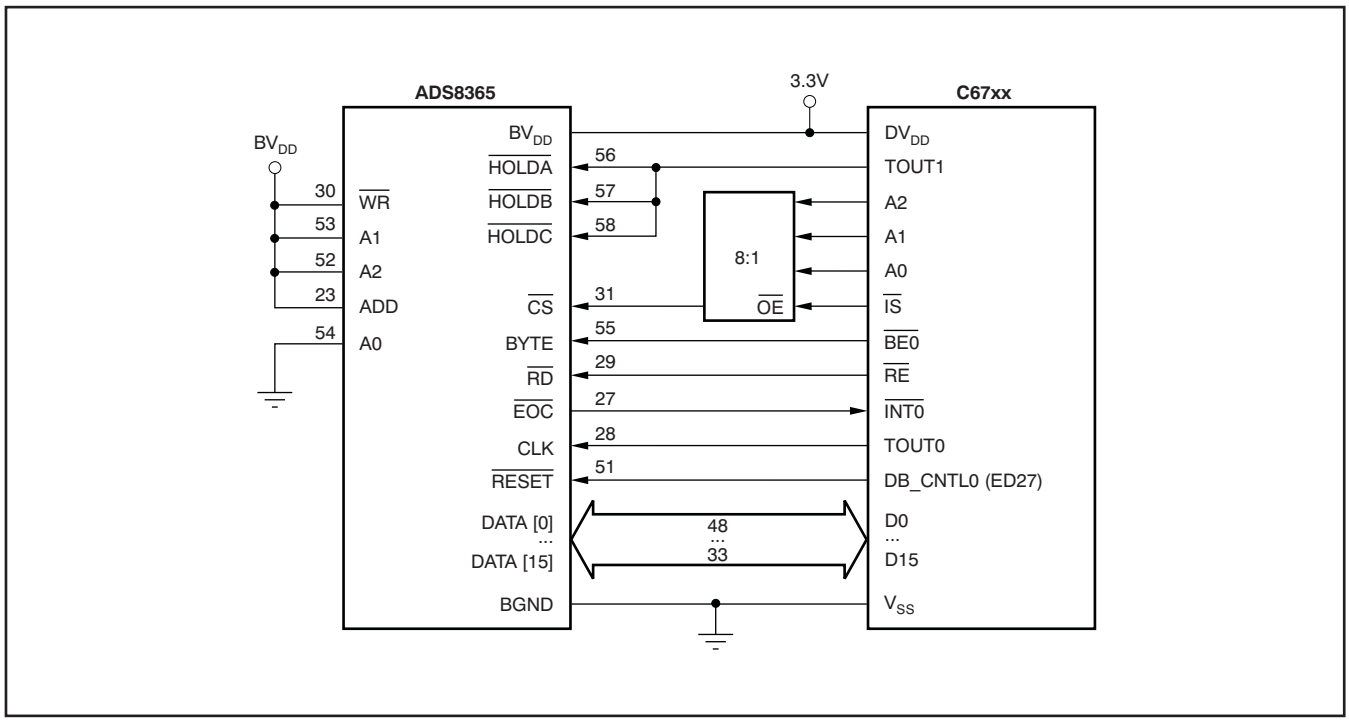

Figure 36. Typical C67xx Connection (Cycle Mode—Hardware Control)

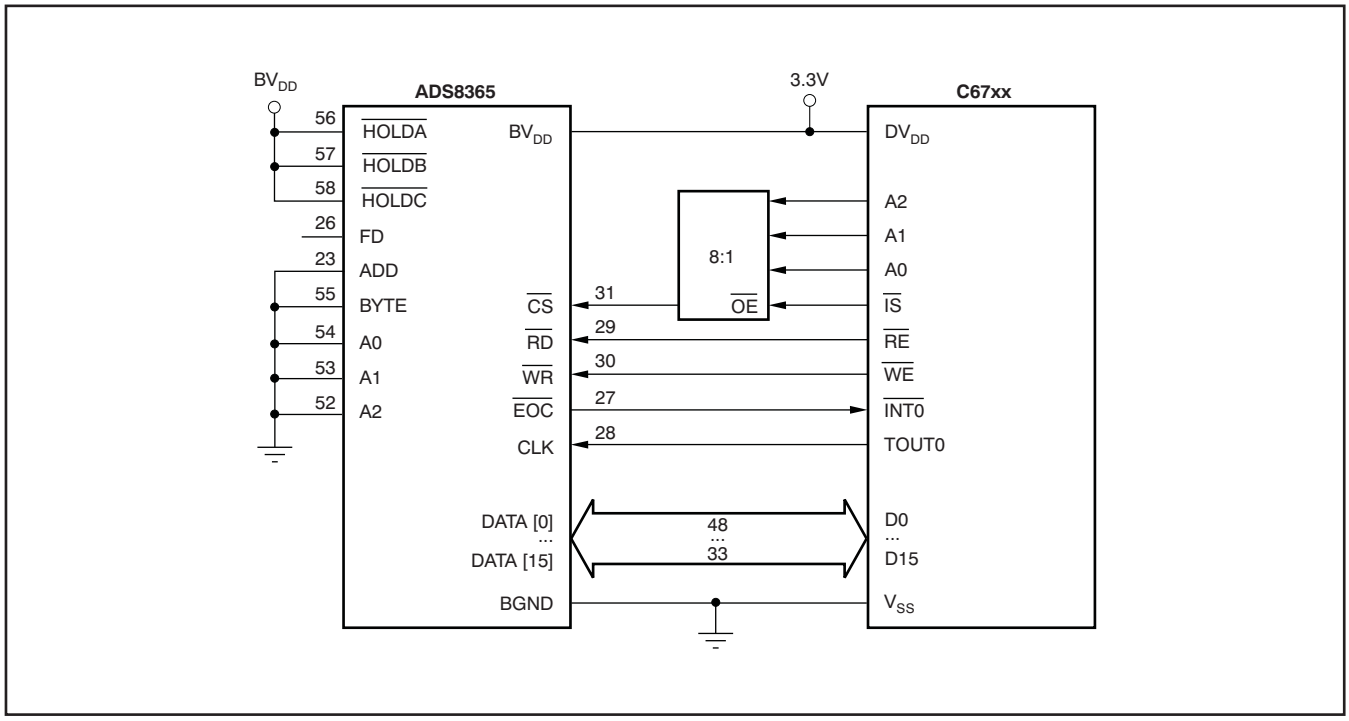

Figure 37. Typical C67xx Connection (Software Control)

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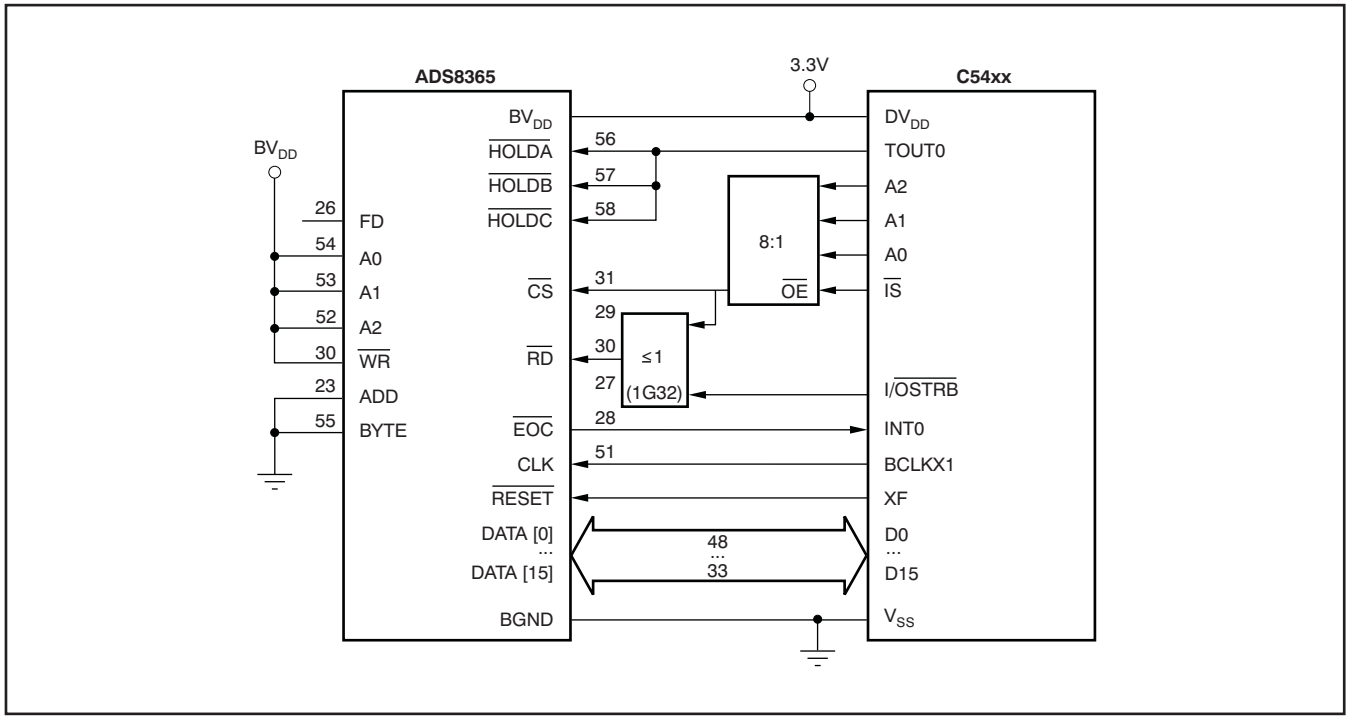

Figure 38. Typical C54xx Connection (FIFO Mode—Hardware Control)

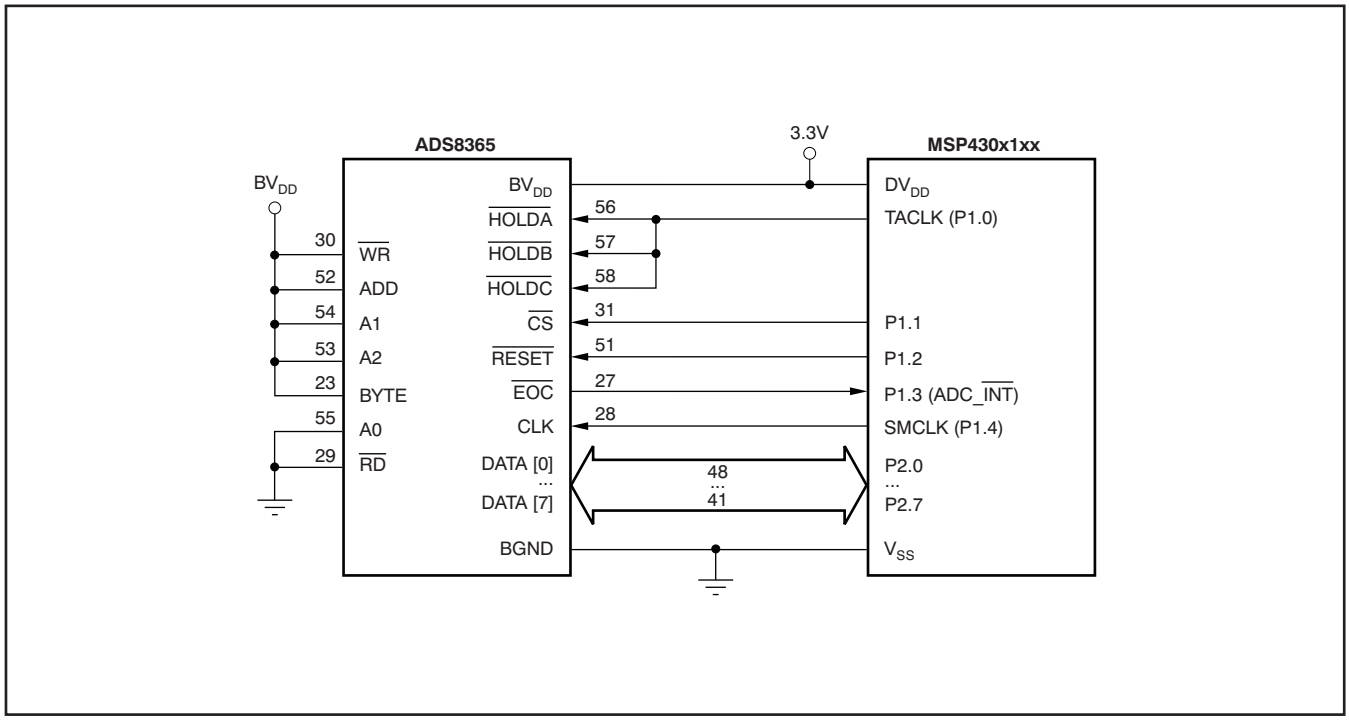

Figure 39. Typical MSP430x1xx Connection (Cycle Mode—Hardware Control)

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Part Change Notification # 20071210003

The ADS8365 device underwent a silicon change under Texas Instruments Part Change Notification (PCN) number 20071210003. Details of this change can be obtained from the Product Information Center at Texas Instruments or by contacting your local sales/distribution office. Devices with a date code of **81x** and higher are covered by this PCN.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2006) to Revision C	Page
• Added Part Change Notification information	31

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8365IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS8365AI	Samples
ADS8365IPAGG4	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS8365AI	Samples
ADS8365IPAGR	ACTIVE	TQFP	PAG	64	1500	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS8365AI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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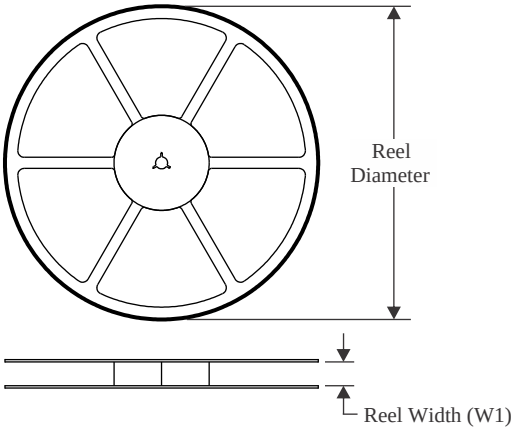
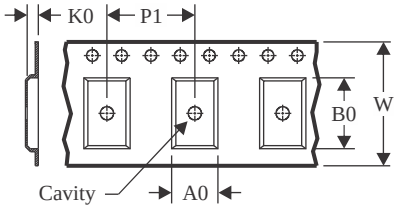
TAPE AND REEL INFORMATION

REEL DIMENSIONS

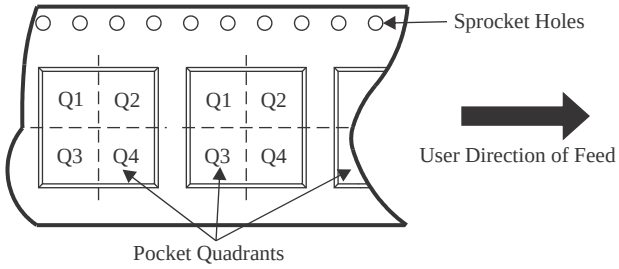


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8365IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

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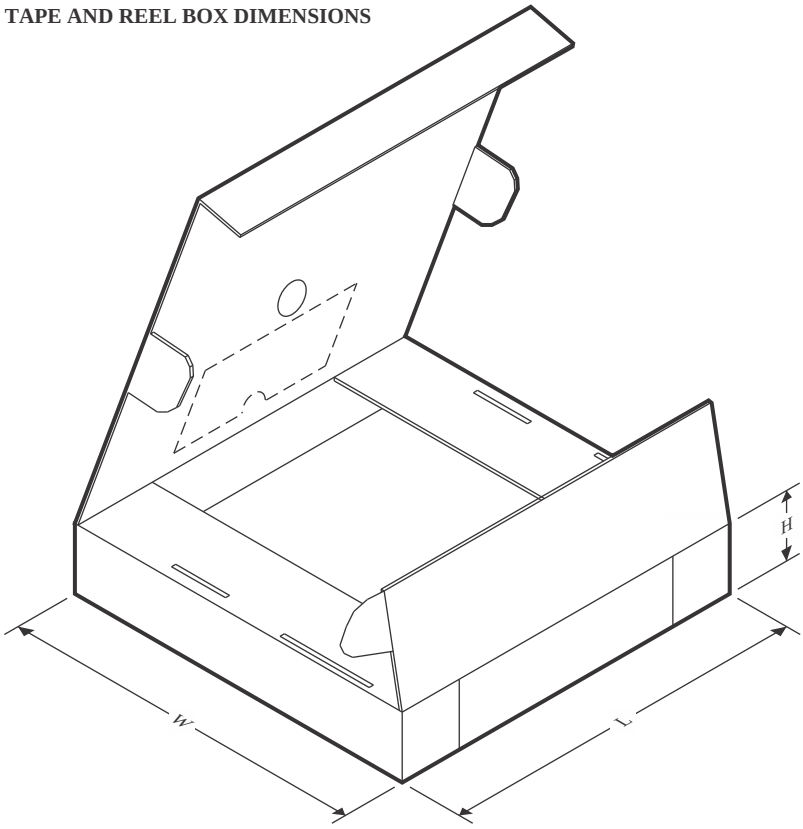
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8365IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0

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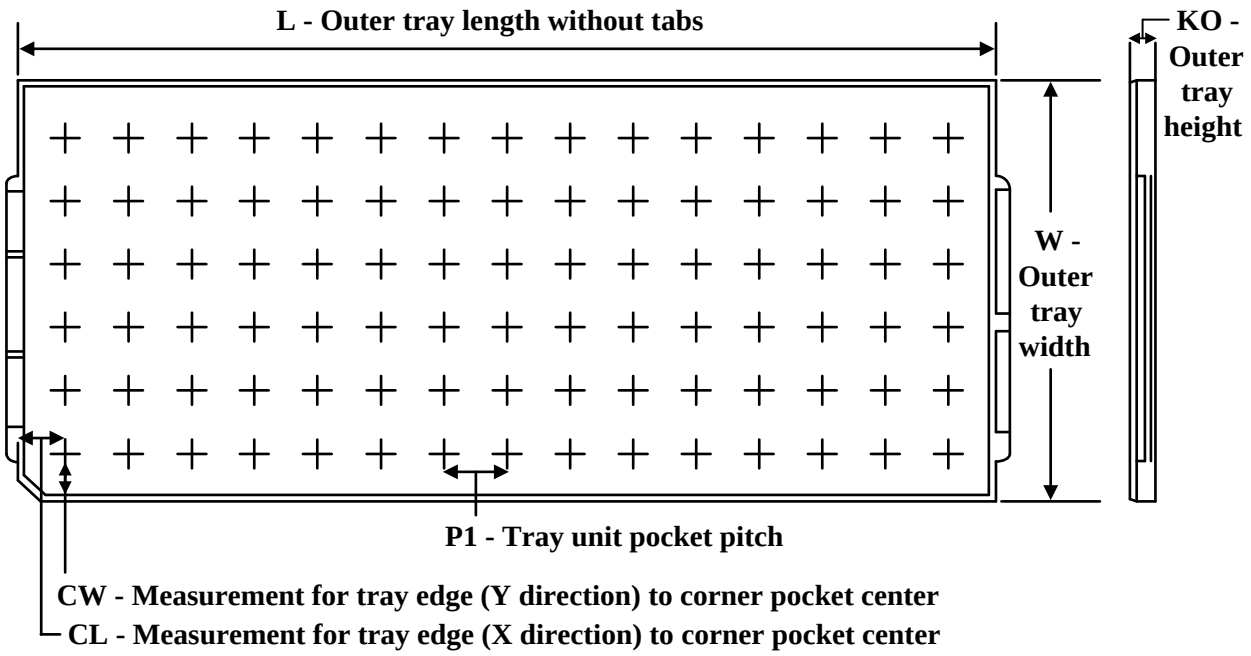
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS8365IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS8365IPAGG4	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

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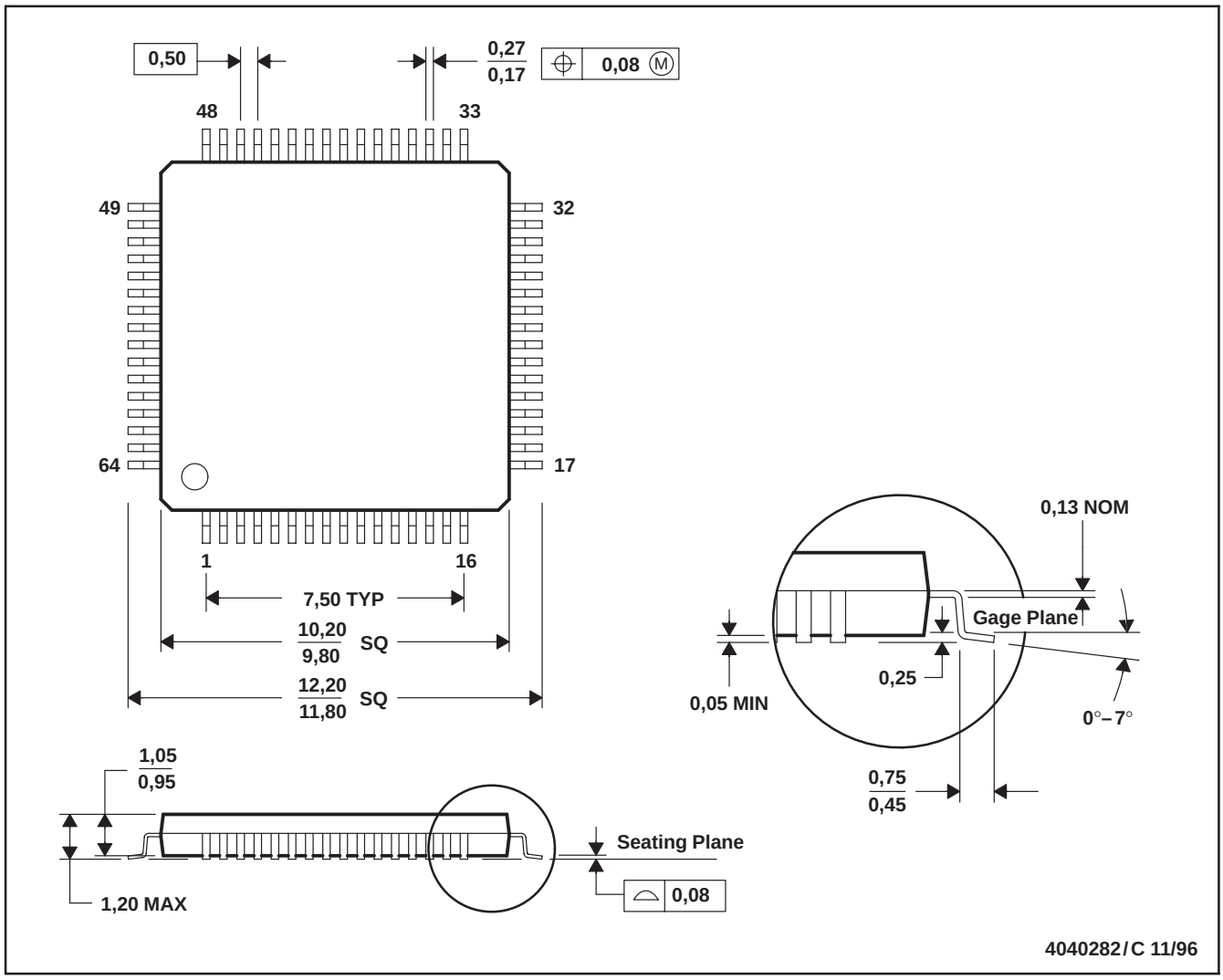
PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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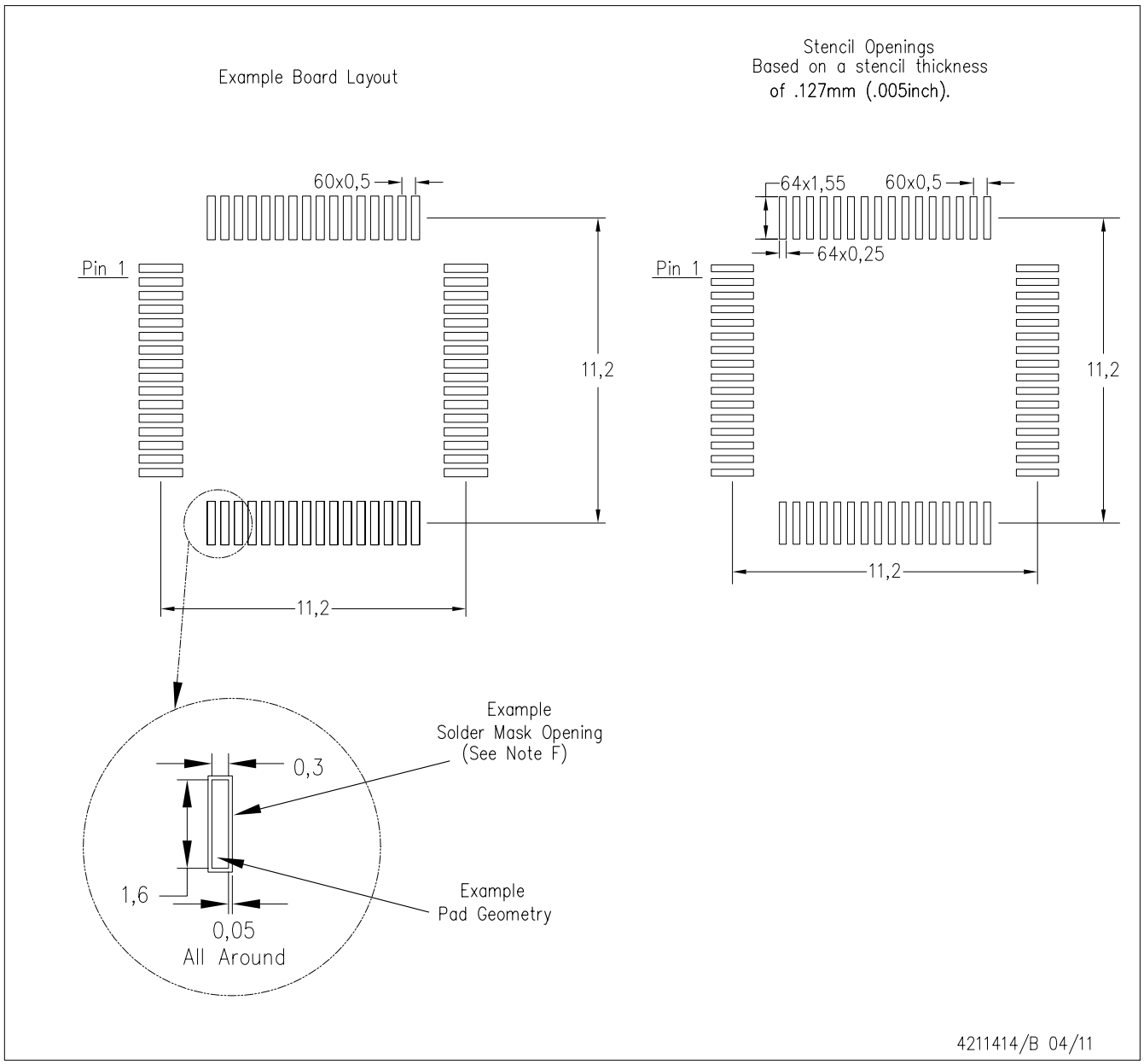
PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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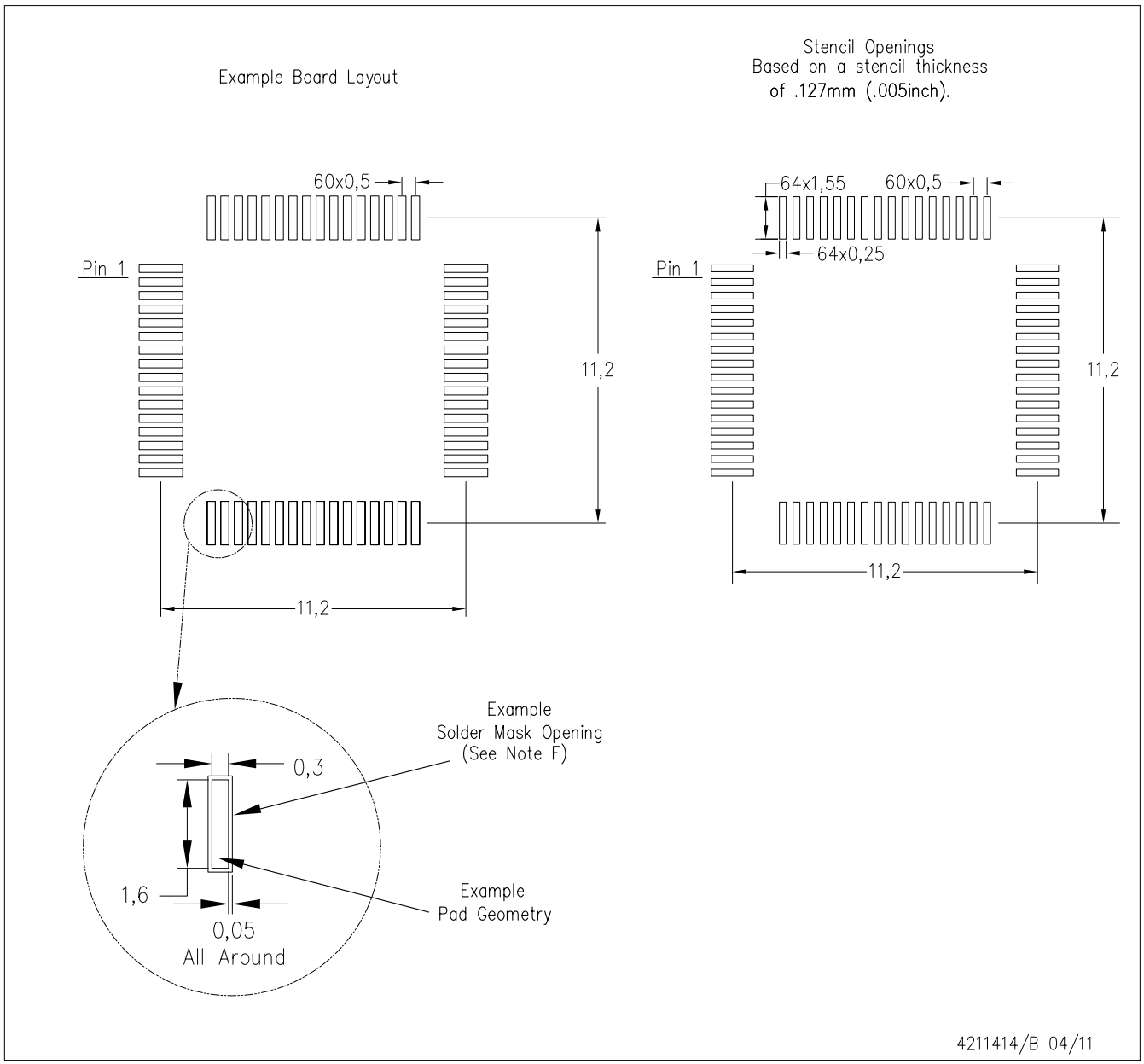
PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



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