

DRV8804 四通道串行接口低侧驱动器 IC

1 特性

- 4 通道受保护低侧驱动器
 - 四个具有过流保护的 N 沟道金属氧化物半导体场效应晶体管 (MOSFET)
 - 集成感应钳位二极管
 - 串行接口
- DW 封装：每通道最大驱动电流（25°C 时）为 1.5A（单通道开启时）/ 800mA（四通道开启时）
- PWP 封装：每通道最大驱动电流（25°C 时，适当的印刷电路板 (PCB) 散热）为 2A（单通道开启时）/ 1A（四通道开启时）
- 运行电源电压范围：8.2V 至 60V
- 耐热增强型表面贴装

2 应用

- 继电器驱动器
- 单极步进电机驱动器
- 螺线管驱动器
- 常见低侧开关 应用

3 说明

DRV8804 提供了一个具有过流保护的 4 通道低侧驱动器。它具有内置的用来钳制由电感负载生成的关闭瞬态的二极管，可被用于驱动单极步进电机、直流电机、继电器、螺线管、或者其它负载。

在小尺寸集成电路 (SOIC) (DW) 封装内，在 25°C 时，DRV8804 每通道可提供高达 1.5A（一个通道接通）或者 800mA（所有通道接通）的持续输出电流。在散热型薄型小尺寸 (HTSSOP) (PWP) 封装内，在 25°C 且具有合适的 PCB 散热的时候，它每通道能够提供高达 2A（一个通道接通）或者 1A（四个通道接通）的持续输出电流。

提供一个含串行数据输出的串行接口，此接口可被菊花链到多重器件以使用一个串行接口对这些器件进行控制。

内置的关断功能可提供过流保护、短路保护、欠压闭锁和过热保护，具体故障由故障输出引脚来指示。

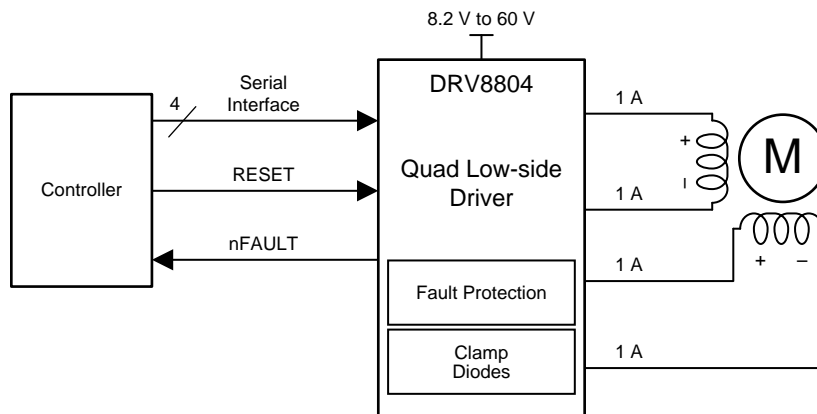
DRV8804 采用 20 引脚耐热增强型 SOIC 封装和 16 引脚 HTSSOP 封装（环境友好型：符合 RoHS 标准且无镉/无溴）。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
DRV8804	SOIC (20)	12.80mm x 7.50mm
	HTSSOP (16)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

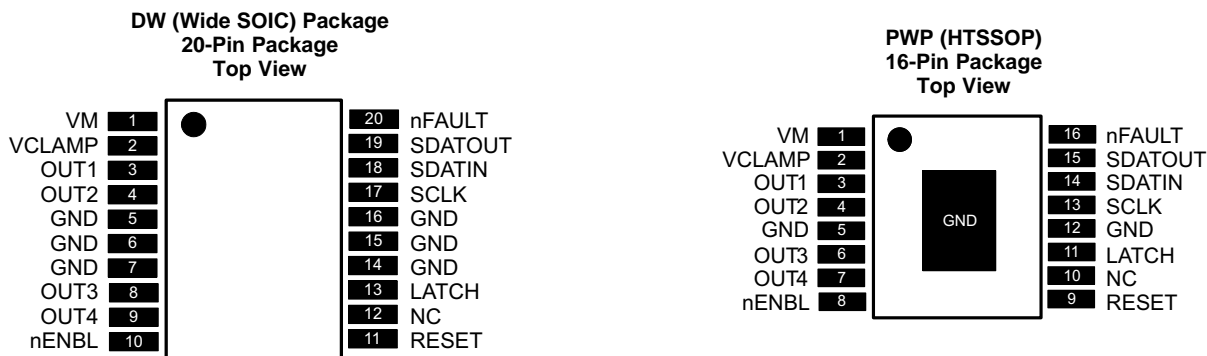
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (January 2014) to Revision F	Page
• 已更改 集流二极管至钳位二极管特性	1
• 已添加 ESD 额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	SOIC			
POWER AND GROUND				
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	—	Device ground All pins must be connected to GND.
VM	1	1	—	Device power supply Connect to motor supply (8.2 V - 60 V).
CONTROL				
LATCH	13	11	I	Latch input Rising edge latches shift register to output stage – internal pull-down
nENBL	10	8	I	Enable input Active low enables outputs – internal pull-down
RESET	11	9	I	Reset input Active-high reset input initializes internal logic – internal pull-down
SCLK	17	13	I	Serial clock Serial clock input – internal pull-down
SDATIN	18	14	I	Serial data input Serial data input – internal pull-down
SDATOUT	19	15	O	Serial data output Serial data output; push-pull structure; see serial interface section for details
STATUS				
nFAULT	20	16	OD	Fault Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT				
OUT1	3	3	O	Output 1 Connect to load 1
OUT2	4	4	O	Output 2 Connect to load 2
OUT3	8	6	O	Output 3 Connect to load 3
OUT4	9	7	O	Output 4 Connect to load 4
VCLAMP	2	2	—	Output clamp voltage Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _M	Power supply voltage	-0.3	65	V
V _{OUTx}	Output voltage	-0.3	65	V
V _{CLAMP}	Clamp voltage	-0.3	65	V
SDATOUT, nFAULT	Output current		20	mA
	Peak clamp diode current		2	A
	DC or RMS clamp diode current		1	A
	Digital input pin voltage	-0.5	7	V
SDATOUT, nFAULT	Digital output pin voltage	-0.5	7	V
	Peak motor drive output current, t < 1 μs		Internally limited	A
	Continuous total power dissipation		See Thermal Information	
T _J	Operating virtual junction temperature	-40	150	°C
T _{stg}	Storage temperature	-60	150	°C

(1) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±3000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _M	Power supply voltage	8.2		60	V
V _{CLAMP}	Output clamp voltage ⁽¹⁾	0		60	V
I _{OUT}	Continuous output current, single channel on, T _A = 25°C, SOIC package ⁽²⁾			1.5	A
	Continuous output current, four channels on, T _A = 25°C, SOIC package ⁽²⁾			0.8	
	Continuous output current, single channel on, T _A = 25°C, HTSSOP package ⁽²⁾			2	
	Continuous output current, four channels on, T _A = 25°C, HTSSOP package ⁽²⁾			1	

 (1) V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.

(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	DRV8804		UNIT	
	DW (SOIC)	PWP (HTSSOP)		
	20 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	67.7	39.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	32.9	24.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	35.4	20.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.2	0.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	34.9	20.1	°C/W

 (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

Thermal Information (continued)

THERMAL METRIC ⁽¹⁾	DRV8804		UNIT
	DW (SOIC)	PWP (HTSSOP)	
	20 PINS	16 PINS	
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	N/A	2.3	°C/W

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					
I _{VM} VM operating supply current	V _M = 24 V		1.6	2.1	mA
V _{UVLO} VM undervoltage lockout voltage	V _M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)					
V _{IL} Input low voltage			0.6	0.7	V
V _{IH} Input high voltage		2			V
V _{HYS} Input hysteresis			0.45		V
I _{IL} Input low current	V _{IN} = 0	-20		20	μA
I _{IH} Input high current	V _{IN} = 3.3 V			100	μA
R _{PD} Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)					
V _{OL} Output low voltage	I _O = 5 mA			0.5	V
I _{OH} Output high leakage current	V _O = 3.3 V			1	μA
SDATOUT OUTPUT (PUSH-PULL OUTPUT)					
V _{OL} Output low voltage	I _O = 5 mA			0.5	V
V _{OH} Output high voltage	I _O = 100 μA, V _M = 11 V - 60 V, peak			6.5	V
	I _O = 100 μA, V _M = 11 V - 60 V, steady state	3.3	4.5	5.6	
	I _O = 100 μA, V _M = 8.2 V - 11 V, steady state	2.5			
I _{SRC} Output source current	V _M = 24 V			1	mA
I _{SNK} Output sink current	V _M = 24 V			5	mA
LOW-SIDE FETS					
R _{DS(ON)} FET on resistance	V _M = 24 V, I _O = 700 mA, T _J = 25°C		0.5		Ω
	V _M = 24 V, I _O = 700 mA, T _J = 85°C		0.75	0.8	
I _{OFF} Off-state leakage current		-50		50	μA
HIGH-SIDE DIODES					
V _F Diode forward voltage	V _M = 24 V, I _O = 700 mA, T _J = 25°C		1.2		V
I _{OFF} Off-state leakage current	V _M = 24 V, T _J = 25°C	-50		50	μA
OUTPUTS					
t _R Rise time	V _M = 24 V, I _O = 700 mA, Resistive load	50		300	ns
t _F Fall time	V _M = 24 V, I _O = 700 mA, Resistive load	50		300	ns
PROTECTION CIRCUITS					
I _{OCP} Overcurrent protection trip level		2.3		3.8	A
t _{OCP} Overcurrent protection deglitch time			3.5		μs
t _{RETRY} Overcurrent protection retry time			1.2		ms
t _{TSD} Thermal shutdown temperature	Die temperature ⁽¹⁾	150	160	180	°C

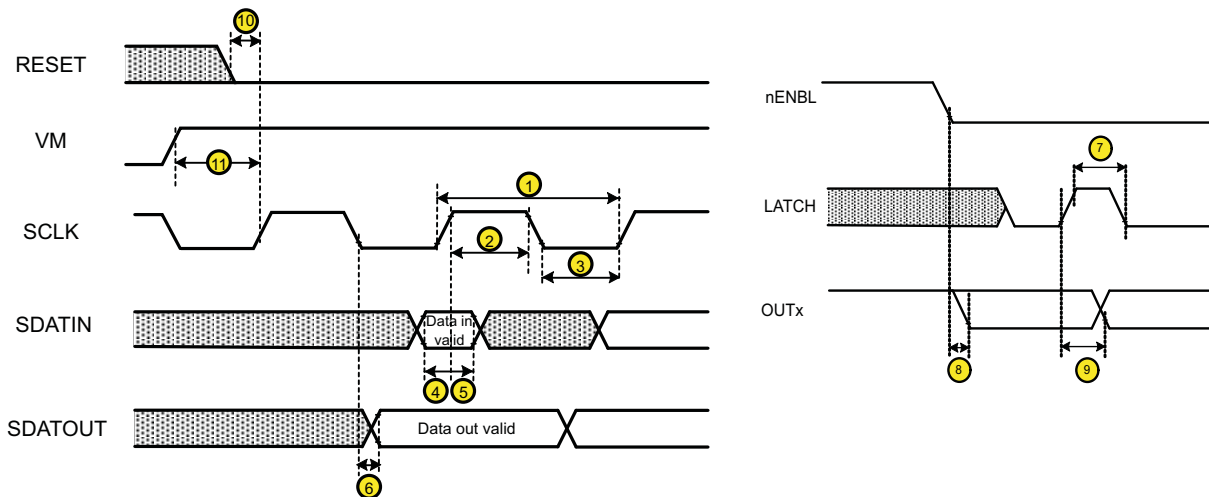
(1) Not production tested.

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
1	t_{CYC}	Clock cycle time	62			ns
2	t_{CLKH}	Clock high time	25			ns
3	t_{CLKL}	Clock low time	25			ns
4	$t_{SU(SDATIN)}$	Setup time, SDATIN to SCLK	5			ns
5	$t_{H(SDATIN)}$	Hold time, SDATIN to SCLK	1			ns
6	$t_{D(SDATOUT)}$	Delay time, SCLK to SDATOUT, no external pullup resistor, $C_{OUT} = 100 \text{ pF}$		50	100	ns
7	$t_{W(LATCH)}$	Pulse width, LATCH	200			ns
8	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		60		ns
9	$t_{D(LATCH)}$	Delay time, LATCH to output change		200		ns
—	t_{RESET}	RESET pulse width	20			μs
10	$t_{D(RESET)}$	Reset delay before clock	20			μs
11	$t_{STARTUP}$	Start-up delay VM applied before clock	55			μs

(1) Not production tested.



More than 400 ns of delay should exist between the final SCLK rising edge and the LATCH rising edge. This ensures that the last data bit is shifted into the device properly.

Figure 1. DRV8804 Timing Requirements

6.7 Typical Characteristics

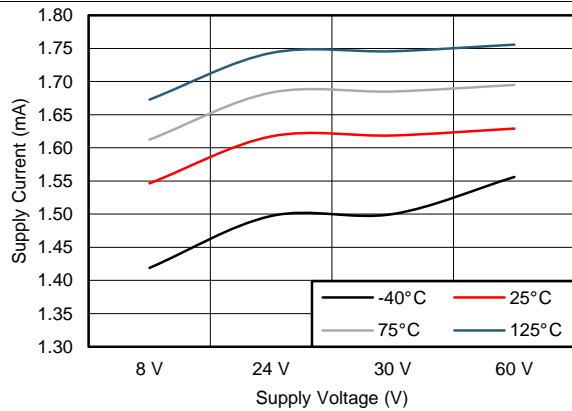


Figure 2. Supply Current over V_M

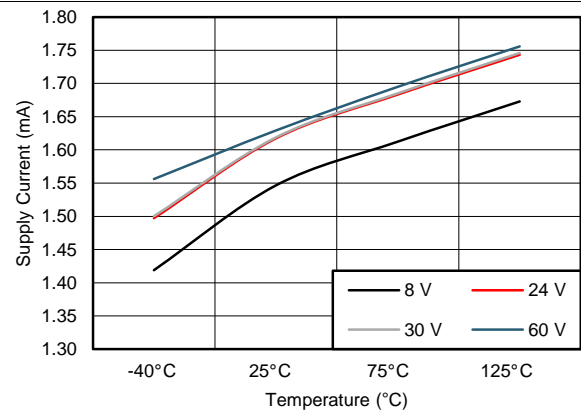


Figure 3. Supply Current Over Temperature

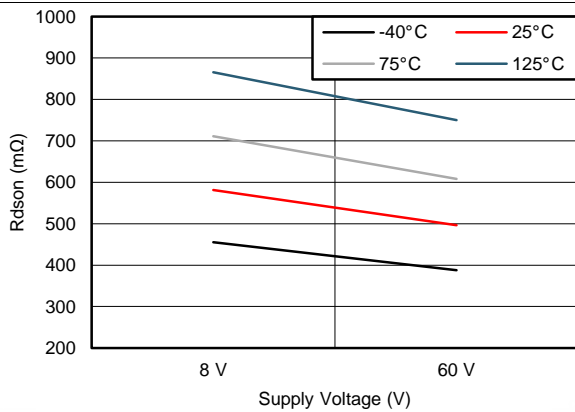


Figure 4. $R_{DS(on)}$ Over V_M

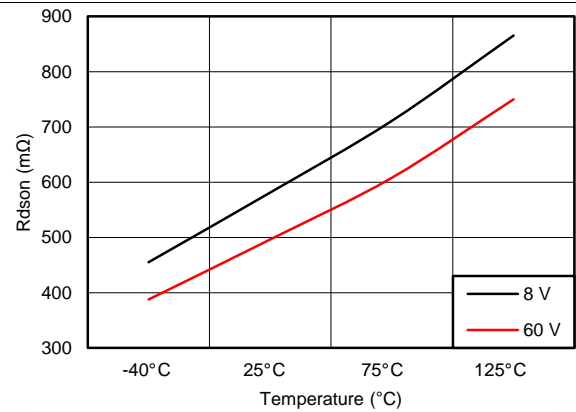


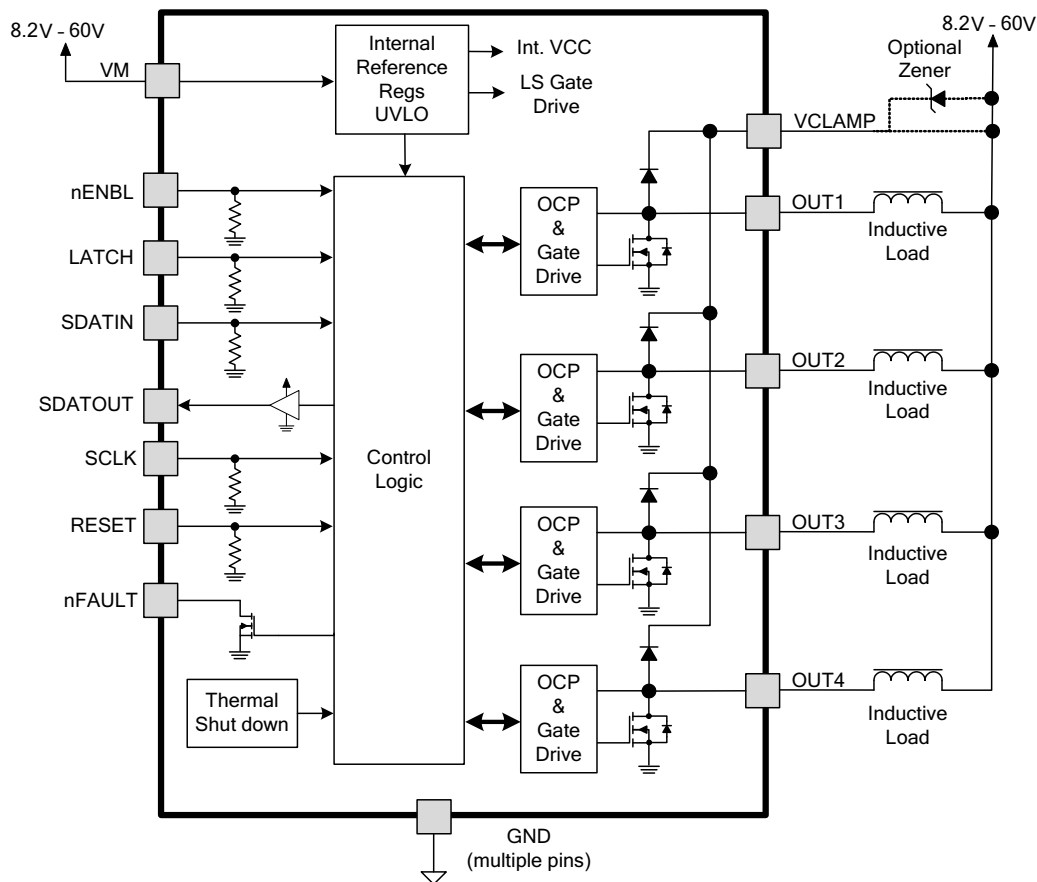
Figure 5. $R_{DS(on)}$ Over Temperature

7 Detailed Description

7.1 Overview

The DRV8804 is an integrated 4-channel low side driver solution for a low side switch application. A serial interface controls the low-side driver outputs and allows for multiple drivers to be chained together and save space on communication lines. The four low-side driver outputs consist of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 500 m Ω . A single motor supply input V_M serves as device power and is internally regulated to power the low side gate drive. The device outputs can be disabled by bringing nENBL pin logic high. This device has several safety features including integrated overcurrent protection that limits the motor current to a fixed maximum above which the device will shut down. Thermal shutdown protection enables the device to automatically shut down if the die temperature exceeds a TTSD limit and will restart once the die reaches a safe temperature. UVLO protection will disable all circuitry in the device if V_M drops below the undervoltage lockout threshold.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Drivers

The DRV8804 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a Zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

7.3.2 Serial Interface Operation

The DRV8804 is controlled with a simple serial interface. Logically, the interface is shown in Figure 6.

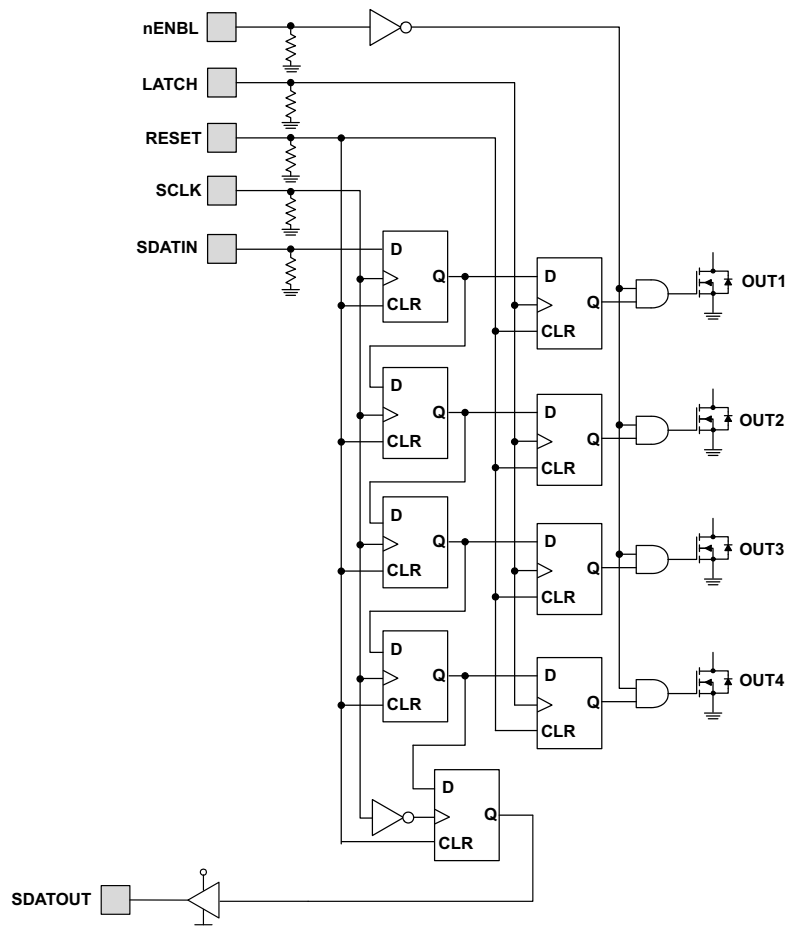


Figure 6. Serial Interface Operation

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin. Data is simultaneously shifted out of the SDATOUT pin, allowing multiple devices to be daisy-chained onto one serial port. Note that the SDATOUT pin has a push-pull driver, which can support driving another DRV8804 SDATIN pin at clock frequencies of up to 1 MHz without an external pullup. A pullup resistor can be used between SDATOUT and an external 5-V logic supply to support higher clock frequencies. TI recommends a resistor value greater than 1 kΩ. The SDATOUT pin is capable of approximately 1-mA source and 5-mA sink. To supply logic signals to a lower-voltage microcontroller, use a resistor divider from SDATOUT to GND.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

Feature Description (continued)

7.3.3 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so driving RESET at power up is not required.

7.3.4 Protection Circuits

The DRV8804 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 μs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

7.3.4.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.4.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout (UVLO) threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when V_{M} rises above the UVLO threshold.

7.4 Device Functional Modes

When the nENBL pin of the DRV8804 is pulled logic low, the open-drain FET outputs are enabled. Having the device be enabled at logic low allows for the use of long data lines in a high noise environment that do not unintentionally enable the device with coupled noise. The device will still shift data through the SDATIN / SDATOUT lines and SCLK line regardless of the state of the nENBL pin.

Once data has been moved into each of the four shift register lines the LATCH pin can be pulled high to output the state of the four shift registers. Once LATCH is pulled high the state of the four shift registers is placed in a logical AND with the inverse state of the nENBL pin. If the nENBL pin is logic low input and the LATCH pin is logic high the open-drain output of that driver channel will be turned on.

If the device detects that V_{M} has dropped below the UVLO threshold, it will immediately enter a state where all the internal logic is disabled. The device stays in a disabled state until V_{M} rises above the UVLO threshold and all internal logic is then reset. During an Overcurrent Protection (OCP) event the device removes gate drive for one t_{RETRY} interval and the nFAULT pin is driven low. The fault is cleared immediately if RESET is activated or V_{M} is removed and re-applied.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8804 can be used to drive one unipolar stepper motor.

8.2 Typical Application

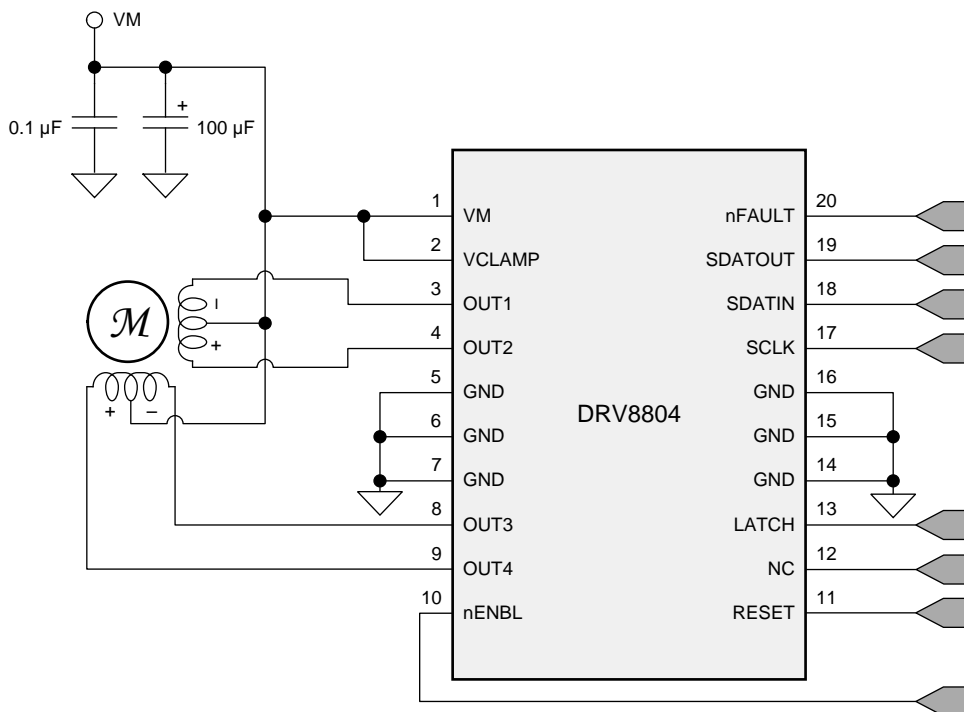


Figure 7. Typical Application Schematic

8.2.1 Design Requirements

Table 1 lists the design parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	24 V
Motor Winding Resistance	R_L	7.4 Ω /phase
Motor Full Step Angle	θ_{step}	1.8°/step
Motor Rated Current	I_{RATED}	0.75 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

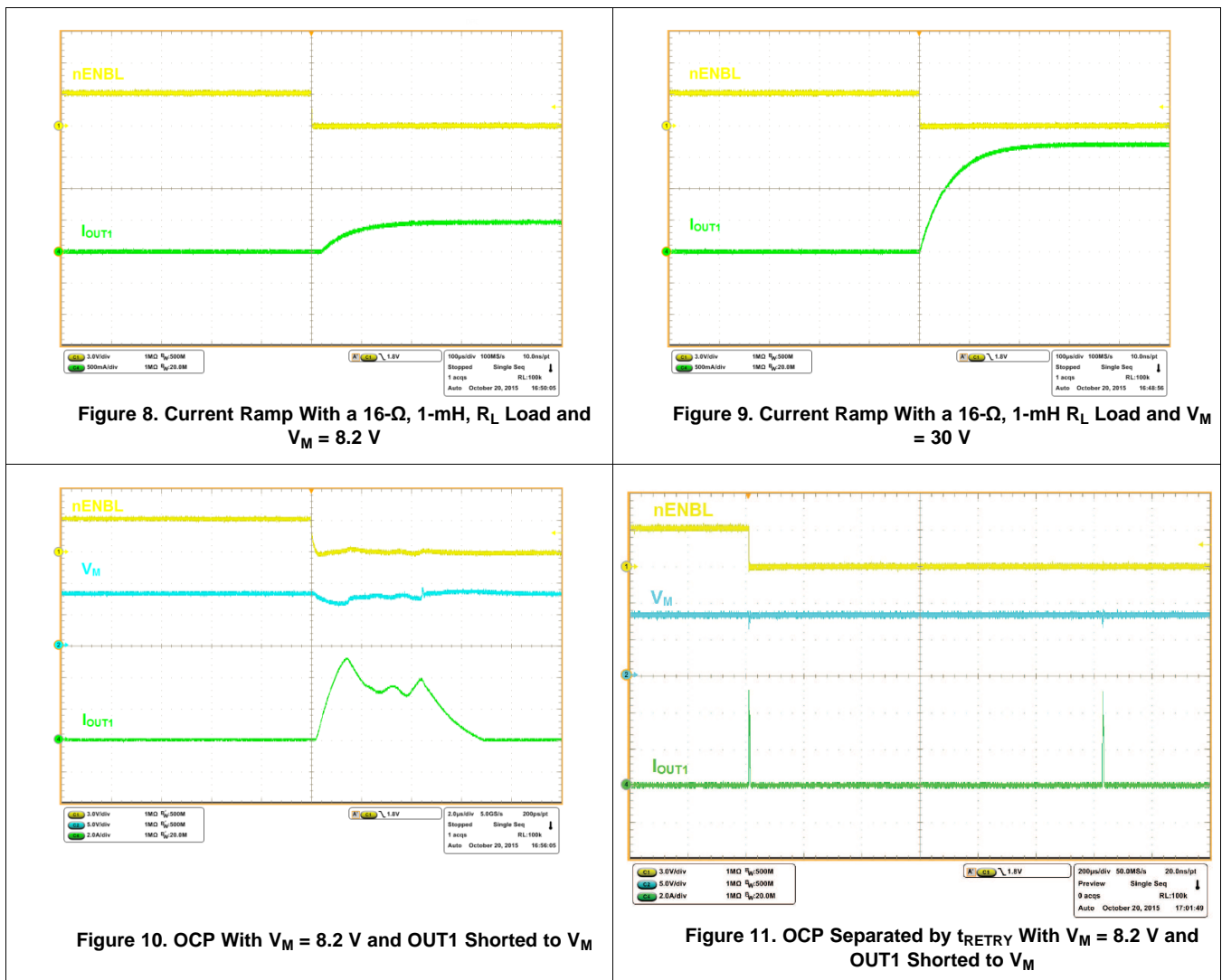
8.2.2.2 Drive Current

The current path starts from the supply V_M , moves through the inductive winding load and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

$$P = I^2 \times R_{DS(on)} \tag{1}$$

The DRV8804 has been measured to be capable of 1.5-A Single Channel or 800-mA Four Channels with the DW package and 2-A Single Channel or 1-A Four Channels with the PWP package at 25°C on standard FR-4 PCBs. The maximum RMS current will vary based on PCB design and the ambient temperature..

8.2.3 Application Curves



9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The type of motor used (Brushed DC, Brushless DC, Stepper).

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

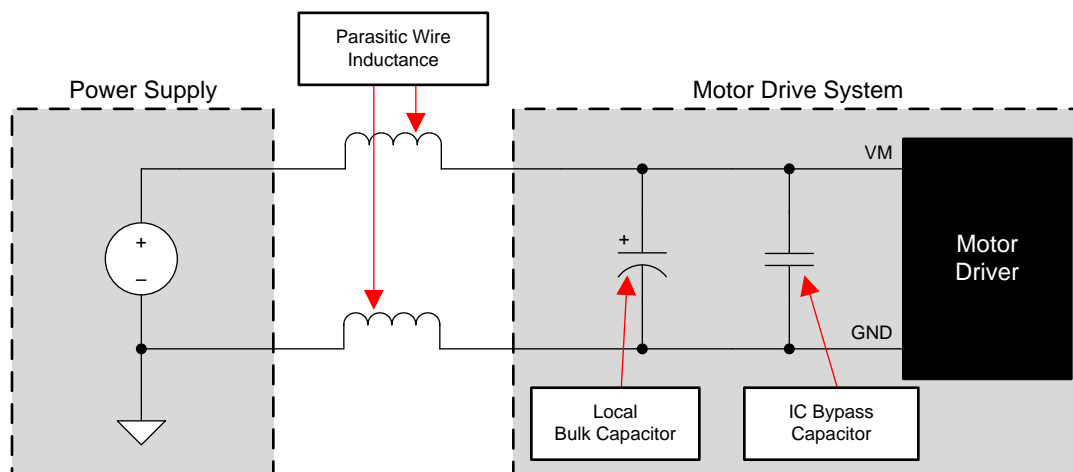


Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

- Small-value capacitors should be ceramic, and placed closely to device pins.
- The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

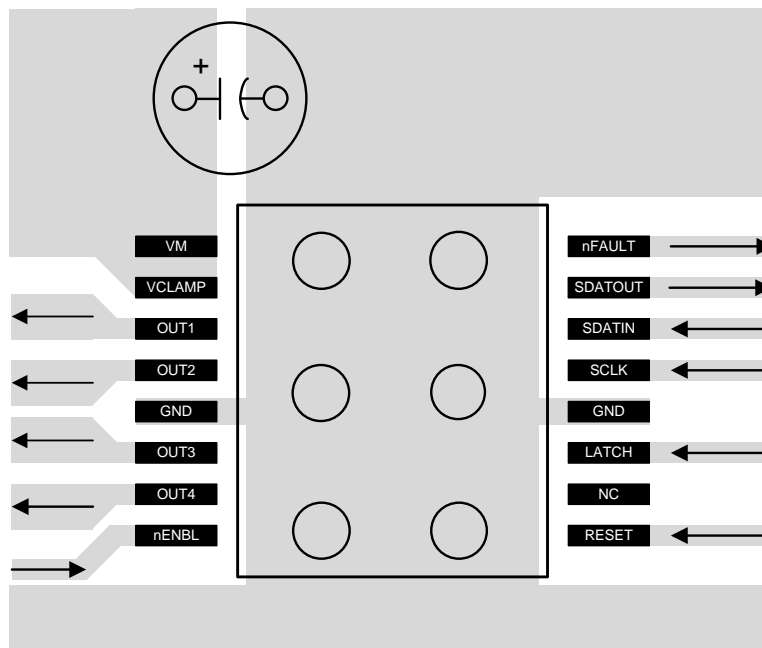


Figure 13. Layout Recommendation

10.3 Thermal Considerations

The DRV8804 has thermal shutdown (TSD) as described in [Thermal Shutdown \(TSD\)](#). If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8804 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each FET when running a static load can be roughly estimated by [Equation 2](#).

$$P = R_{DS(ON)} \cdot (I_{OUT})^2$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load

(2)

Thermal Considerations (continued)

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The DRV8804DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8804PWP package uses an HTSSOP package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see TI Application Report, *PowerPAD Thermally Enhanced Package (SLMA002)*, and TI Application Brief, *PowerPAD Made Easy (SLMA004)*, available at www.ti.com.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《PowerPAD 耐热增强型封装》， [SLMA002](#)
- 《PowerPAD 速成》， [SLMA004](#)

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8804DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8804DW	Samples
DRV8804DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8804DW	Samples
DRV8804PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804	Samples
DRV8804PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8804DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
DRV8804PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8804DWR	SOIC	DW	20	2000	367.0	367.0	45.0
DRV8804PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DRV8804DW	DW	SOIC	20	25	507	12.83	5080	6.6
DRV8804PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PWP0016J



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

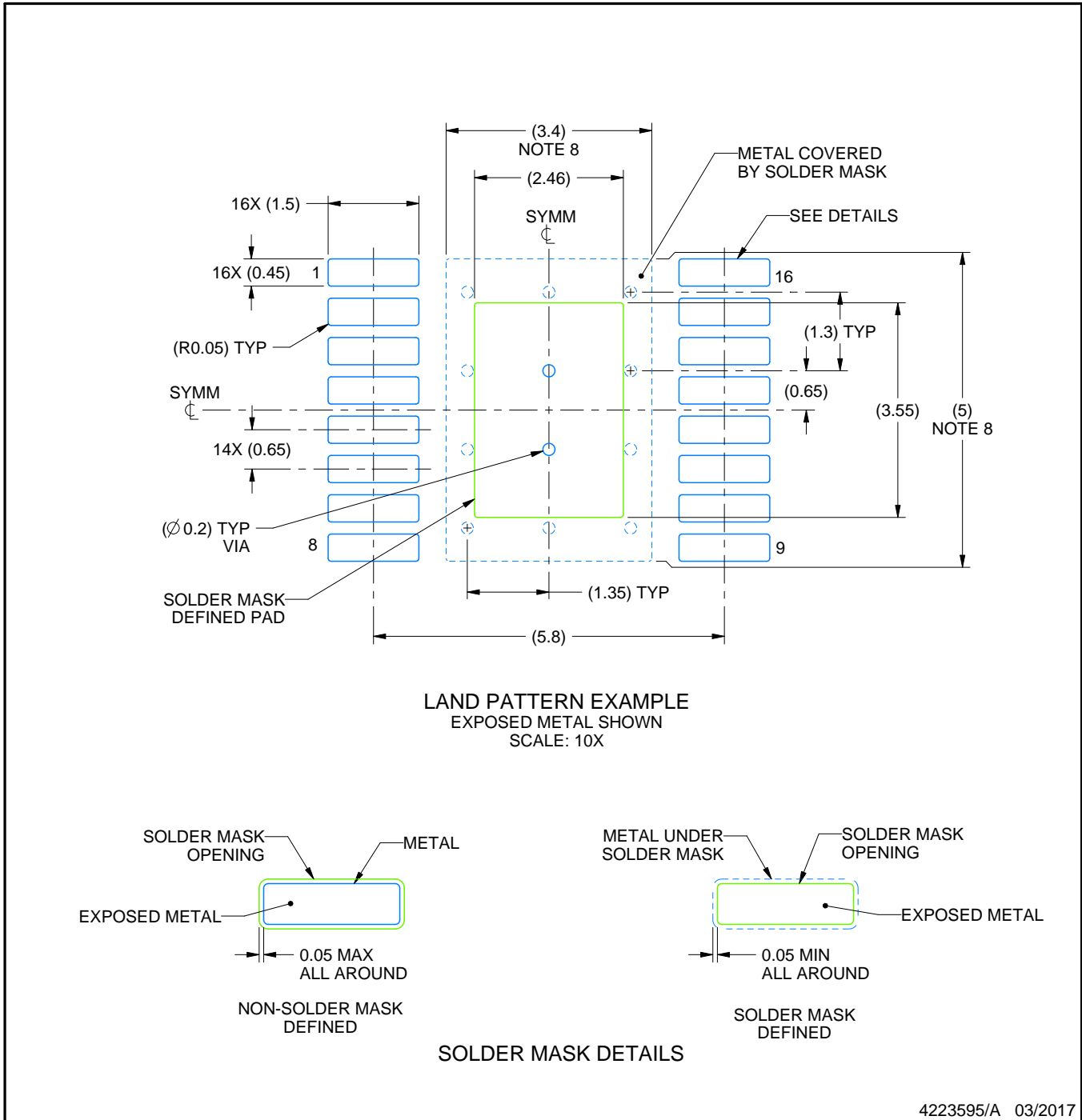


EXAMPLE BOARD LAYOUT

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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