

TL4242 500-mA, Adjustable, Constant-Current LED Driver

1 Features

- Adjustable Constant Current up to 500 mA ($\pm 5\%$)
- PWM Brightness Regulation
- Wide Input Voltage Range up to 42 V
- Low Drop Voltage
- Open-Load Detection
- Overtemperature Protection
- Short-Circuit Proof
- Reverse-Polarity Proof
- Wide Temperature Range: -40°C to 150°C

2 Applications

- Signage
- Industrial Lighting
- Printers

3 Description

The TL4242 device is an integrated, adjustable, constant-current source that can drive loads up to 500 mA. The output current level can be adjusted through an external resistor. The device is designed to supply high-power LEDs. The TL4242 is provided in the DRJ (WSON) package. Protection circuits prevent damage to the device in case of overload, short circuit, reverse polarity, and overtemperature. The connected LEDs are protected against reverse polarity as well as excess voltages up to 45 V.

The integrated PWM input of the TL4242 permits LED brightness regulation by pulse-width modulation (PWM). Due to the high input impedance of the PWM input, the LED driver can be operated as a protected high-side switch.

The TL4242 is characterized for operation from -40°C to 150°C .

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|----------|-------------------|
| TL4242 | WSON (8) | 4.00 mm x 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

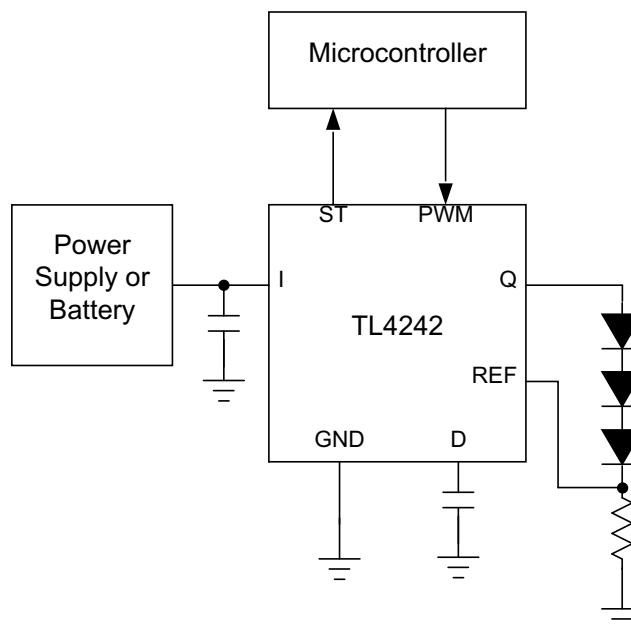


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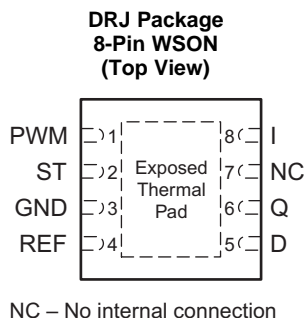
4 Revision History

Changes from Revision A (April 2011) to Revision B

Page

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. **1**

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-------------|-----|---|
| NO. | NAME | | |
| 1 | PWM | I | Pulse-width modulation input. If not used, connect to I. |
| 2 | ST | O | Status output. Open-collector output. Connect to an external pullup resistor ($R_{PULLUP} \geq 4.7 \text{ k}\Omega$). |
| 3 | GND | — | Ground |
| 4 | REF | I | Reference input. Connect to a shunt resistor. |
| 5 | D | I | Status delay. To set status reaction delay, connect to GND with a capacitor. If no delay is needed, leave open. |
| 6 | Q | O | Output |
| 7 | NC | — | No internal connection |
| 8 | I | I | Input. Connect directly to GND as close as possible to the device with a 100-nF ceramic capacitor. |
| — | Thermal Pad | — | The thermal pad must be soldered directly to the PCB. It may be connected to ground or left floating. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------|-------------------------------|-----|------|---------|----|
| V_{CC} | Supply voltage ⁽²⁾ | -42 | 45 | V | |
| V_I | Input voltage | D | -0.3 | 7 | V |
| | | PWM | -40 | 40 | |
| | | REF | -1 | 16 | |
| V_O | Output voltage | Q | -1 | 41 | V |
| | | ST | -0.3 | 40 | |
| I_O | Output current | PWM | | ± 1 | mA |
| | | REF | | ± 2 | |
| | | ST | | ± 5 | |
| T_J | Virtual-junction temperature | -40 | 150 | °C | |
| T_{stg} | Storage temperature | -50 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|-------------------------------------|--|-----|-----|------|
| V_{CC} Supply voltage | | 4.5 | 42 | V |
| V_{ST} Status (ST) output voltage | | | 16 | V |
| V_{PWM} PWM voltage | | 0 | 40 | V |
| C_D Status delay (D) capacitance | | 0 | 2.2 | μF |
| R_{REF} Reference (REF) resistor | | 0 | 10 | Ω |
| T_J Virtual-junction temperature | | -40 | 150 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TL4242 | UNIT |
|---|--|------------|------|
| | | DRJ (WSON) | |
| | | 8 PINS | |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | | 39.0 | °C/W |
| $R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance | | 31.5 | |
| $R_{\theta JB}$ Junction-to-board thermal resistance | | 15.5 | |
| Ψ_{JT} Junction-to-top characterization parameter | | 0.3 | |
| Ψ_{JB} Junction-to-board characterization parameter | | 15.6 | |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | | 1.8 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range, $V_I = 13.5$ V, $R_{REF} = 0.47$ Ω, $V_{PWM,H}$, $T_J = -40$ °C to 150°C, all voltages with respect to ground (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|------|-----|------|
| I_{qL} Supply current | $V_Q = 6.6$ V | | 12 | 22 | mA |
| I_{qOFF} Supply current, off mode | PWM = L, $T_J < 85$ °C | | 0.1 | 2 | μA |
| OUTPUT ELECTRICAL CHARACTERISTICS | | | | | |
| I_Q Output current | $V_Q - V_{REF}^{(1)} = 6.6$ V | 357 | 376 | 395 | mA |
| | $V_Q - V_{REF} = 6.6$ V, $R_{REF} = 1$ Ω | 168 | 177 | 185 | |
| | $V_Q - V_{REF} = 6.6$ V, $R_{REF} = 0.39$ Ω | 431 | 454 | 476 | |
| | $V_Q - V_{REF} = 5.4$ V to 7.8 V, $V_I = 9$ V to 16 V | 357 | 376 | 395 | |
| I_{Qmax} Output current limit | $R_{REF} = 0$ Ω | | 600 | | mA |
| V_{dr} Drop voltage | $I_Q = 300$ mA | | 0.35 | 0.7 | V |
| PWM INPUT ELECTRICAL CHARACTERISTICS | | | | | |
| $V_{PWM,H}$ High-level PWM voltage | | 2.6 | | | V |
| $V_{PWM,L}$ Low-level PWM voltage | | | | 0.7 | V |
| $I_{PWM,H}$ High-level PWM input current | $V_{PWM} = 5$ V | | 220 | 500 | μA |
| $I_{PWM,L}$ Low-level PWM input current | $V_{PWM} = 0$ V | -1 | | 1 | μA |

(1) $V_Q - V_{REF}$ equals the forward voltage sum of the connected LEDs (see [Figure 3](#)).

Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $R_{REF} = 0.47\ \Omega$, $V_{PWM,H}$, $T_J = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------------|--|-----|-----|-----|---------------|
| t_{PWN} | Delay time, turn on | 70% of I_{Qnom} , See Figure 5 | 0 | 15 | 40 | μs |
| t_{PWF} | Delay time, turn off | 30% of I_{Qnom} , See Figure 5 | 0 | 15 | 40 | μs |
| REFERENCE (REF) ELECTRICAL CHARACTERISTICS | | | | | | |
| V_{REF} | Reference voltage | $R_{REF} = 0.39\ \Omega$ to $1\ \Omega$ | 168 | 177 | 185 | mV |
| I_{REF} | Reference input current | $V_{REF} = 180\text{ mV}$ | -1 | 0.1 | 1 | μA |
| STATUS OUTPUT (ST) ELECTRICAL CHARACTERISTICS | | | | | | |
| V_{IQL} | Lower status-switching threshold | ST = L | 15 | 25 | | mV |
| V_{IQH} | Upper status-switching threshold | ST = H | | 30 | 40 | mV |
| V_{STL} | Low-level status voltage | $I_{ST} = 1.5\text{ mA}$ | | | 0.4 | V |
| I_{STLK} | Leakage current | $V_{ST} = 5\text{ V}$ | | | 5 | μA |
| STATUS DELAY (D) ELECTRICAL CHARACTERISTICS | | | | | | |
| t_{STHL} | Delay time, status reaction | $C_D = 47\text{ nF}$, ST H→L | 6 | 10 | 14 | ms |
| t_{STLH} | Delay time, status release | $C_D = 47\text{ nF}$, ST L→H | | 10 | 20 | μs |

6.6 Typical Characteristics

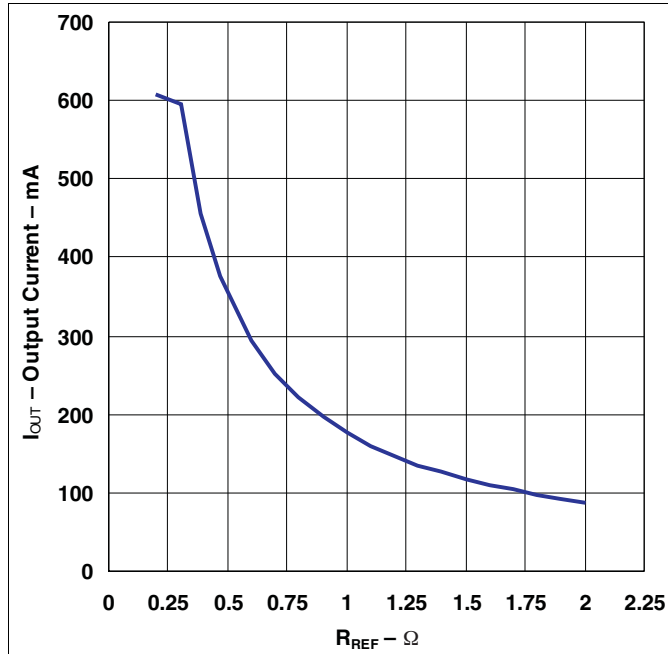


Figure 1. Output Current vs External Resistor

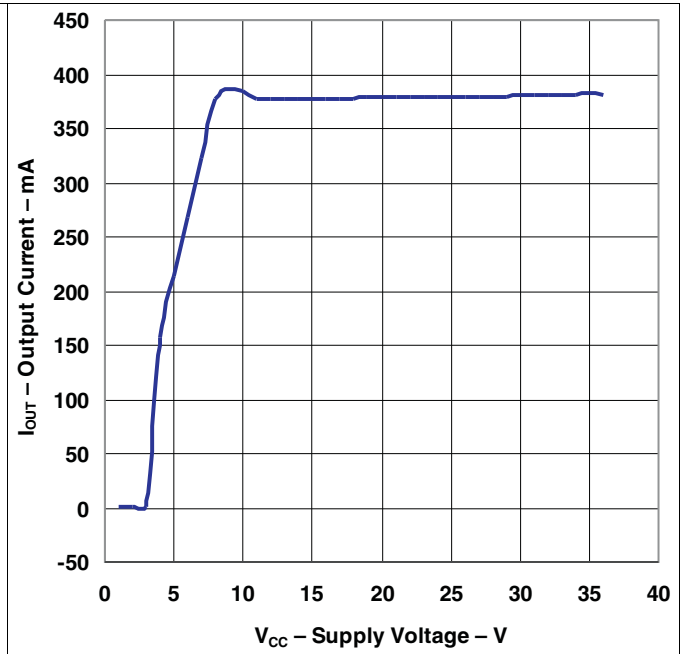


Figure 2. Output Current vs Supply Voltage

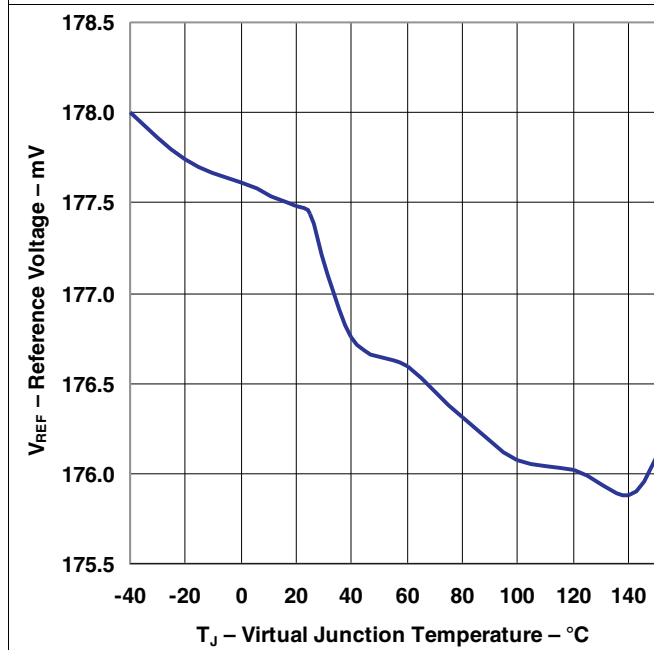


Figure 3. Reference Voltage vs Junction Temperature

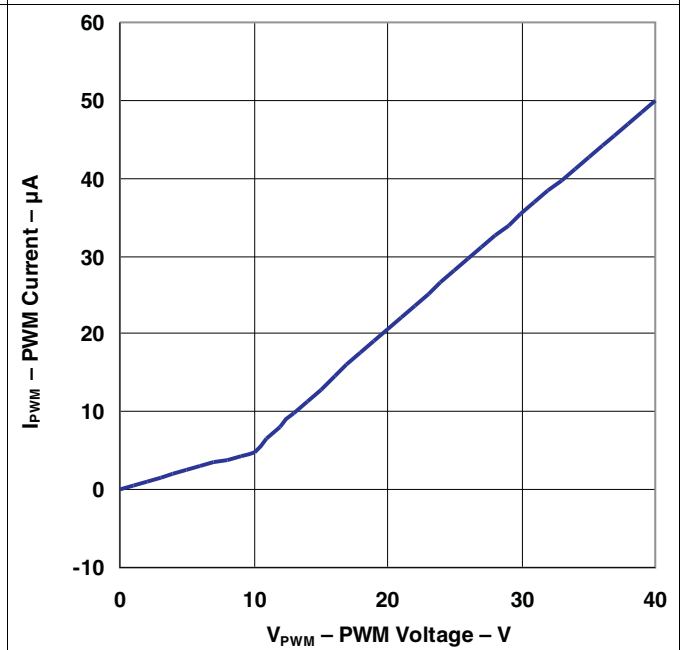


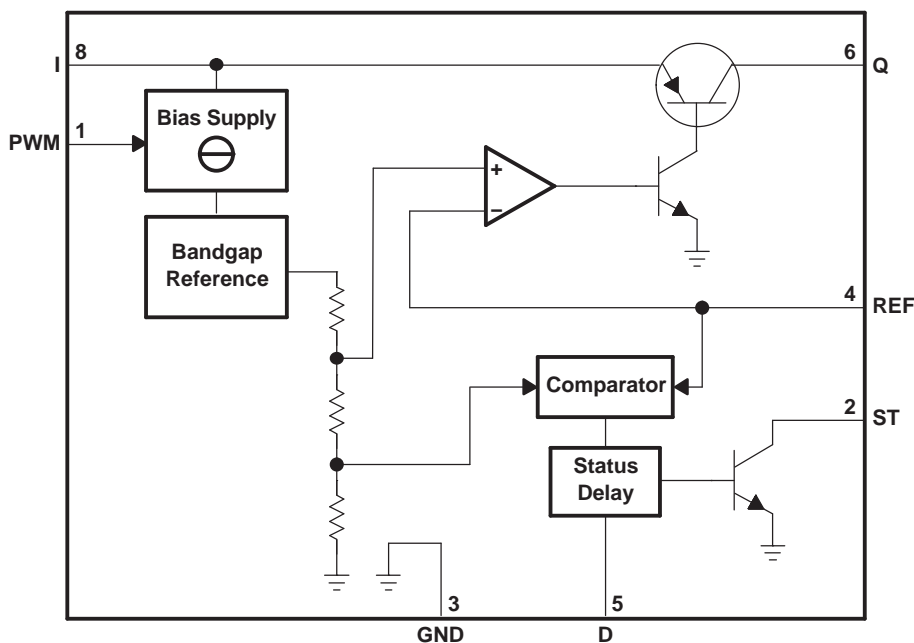
Figure 4. PWM Pin Input Current vs PWM Voltage

7 Detailed Description

7.1 Overview

The TL4242 device is an integrated, adjustable, constant-current source that can drive loads up to 500 mA. The output current level can be adjusted through an external resistor. The device is designed to supply high-power LEDs. Protection circuits prevent damage to the device in case of overload, short circuit, reverse polarity, and overtemperature. The connected LEDs are protected against reverse polarity as well as excess voltages up to 45 V. The integrated PWM input of the TL4242 permits LED brightness regulation by pulse-width modulation (PWM). Due to the high input impedance of the PWM input, the LED driver can be operated as a protected high-side switch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Input

The integrated PWM input of the TL4242 permits LED brightness regulation by pulse-width modulation (PWM). The overall LED brightness is a function of the shunt resistor, R_{REF} , and the PWM duty cycle. The PWM input can also function as a simple enable control. When the PWM input is below $V_{PWM,L}$, the device will go to a low-power consumption sleep mode. Due to the high input impedance of the PWM input, the LED driver can be operated as a protected high-side switch.

The LEDs are driven by a supply current that is adjusted by the resistor, R_{REF} , preventing brightness variations due to forward voltage spread of the LEDs. The luminosity spread arising from the LED production process can be compensated through software by an appropriate duty cycle applied to the PWM pin. Therefore, it is not necessary to select LEDs for forward voltage or luminosity classes.

7.3.2 ST Output

The status output of the LED driver (ST) detects an open-load condition, enabling supervision of correct LED operation. An LED failure is detected as a voltage drop at the shunt resistor (R_{REF}) below 25 mV (typical). In this case, the status output pin (ST) is set low after a delay time adjustable by an optional capacitor connected to pin D.

Feature Description (continued)

7.3.2.1 Function and Timing Diagram

The functionality and timing of ST and PWM are shown in [Figure 5](#). The status delay can be adjusted through the capacitor connected to pin D. Delay time scales linearly with capacitance, C_D :

$$t_{STHL,typ} = \frac{C_D}{47 \text{ nF}} \times 10 \text{ ms} \quad (1)$$

$$t_{STLH,typ} = \frac{C_D}{47 \text{ nF}} \times 10 \text{ }\mu\text{s} \quad (2)$$

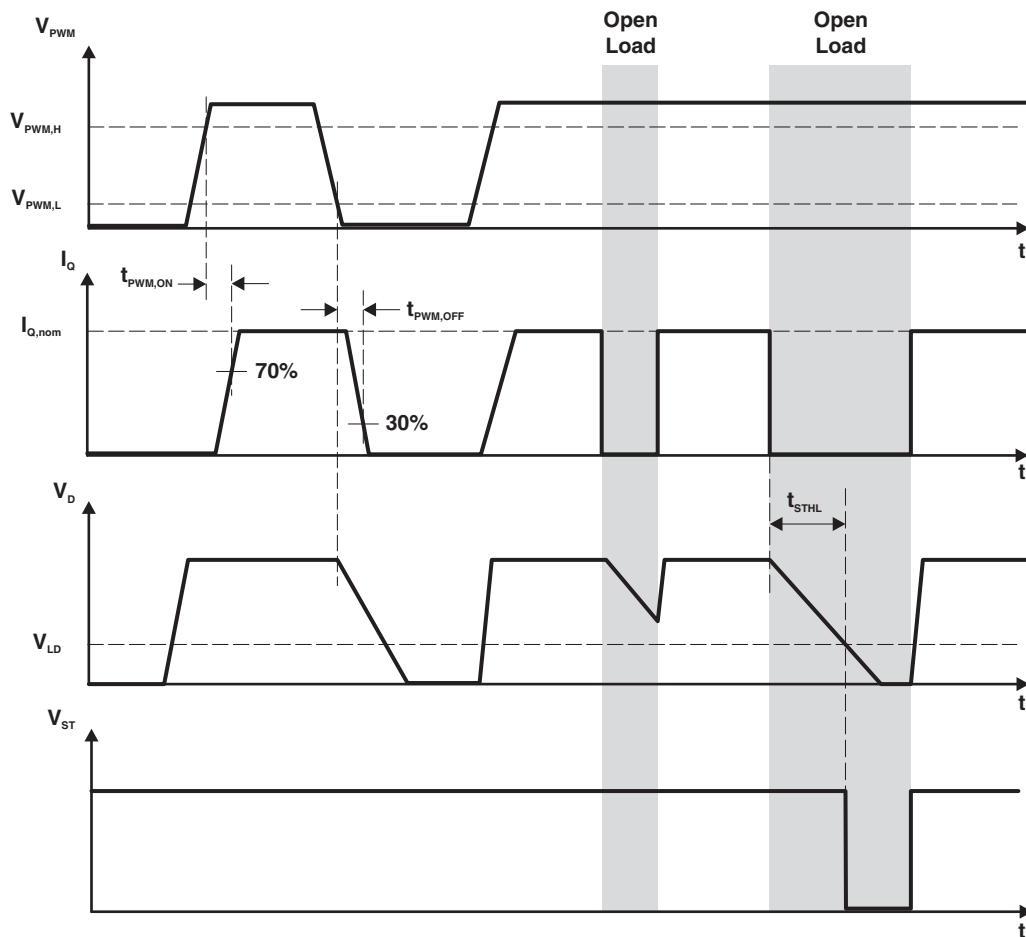


Figure 5. Function and Timing Diagram

7.4 Device Functional Modes

Table 1. Functional Modes

| V_{PWM} | DEVICE MODE |
|-----------|-------------|
| High | Active |
| Low | Sleep |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Supply Voltage

The input supply voltage calculates as the sum of the LED forward voltages, the TL4242 drop voltage, and the voltage drop across the shunt resistor, R_{REF} . The total LED forward voltage depends on the type of LED and the number of LEDs in the string. The TL4242 drop voltage must be greater than V_{dr} (typically 350 mV), but must not be too high as this could cause excessive power dissipation inside the device. The voltage drop across the shunt resistor is typically 177 mV.

8.1.2 Power Dissipation in TL4242

Power dissipation in the TL4242 will come from two sources:

- Quiescent power: (Input voltage \times Supply current)
- Power dissipation in the pass element:

$$((V_I - V_Q) \times I_Q) \quad (3)$$

The power dissipation in the pass element can be significant if the input voltage, V_I , is much higher than V_Q . The power dissipation is also dependent on the LED current. Equation 4 is an example calculation using the design parameters listed in Table 2.

Table 2. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|------------------|---------------|
| V_I | 13.5 V |
| V_Q | 7 V |
| I_Q | 0.2 A |

$$((V_I - V_Q) \times I_Q) = (13.5 - 7) \times 0.2 = 1.3 \text{ W} \quad (4)$$

In Equation 4, there is 1.3 W of power dissipation in the pass element of the TL4242. This power dissipation will cause the junction temperature of the device to increase. The increase in temperature is equal to $R_{\theta JA} \times 1.3 \text{ W}$. Please note that $R_{\theta JA}$ is dependent on the PCB layout.

8.1.3 Setting the Output Current

An external shunt resistor in the ground path of the connected LEDs is used to sense the LED current. A regulation loop holds the voltage drop at the shunt resistor at a constant level of 177 mV (typical). The constant-current level can be adjusted by selecting the shunt resistance, R_{REF} . Calculate the typical output current using the equation:

$$I_{Q,typ} = V_{REF}/R_{REF}$$

where

- V_{REF} is the reference voltage (typically 177 mV) (see [Electrical Characteristics](#)).

The equation applies for $R_{REF} = 0.39 \Omega$ to 10Ω .

The output current is shown as a function of the reference resistance in [Figure 1](#).

8.2.3 Application Curve

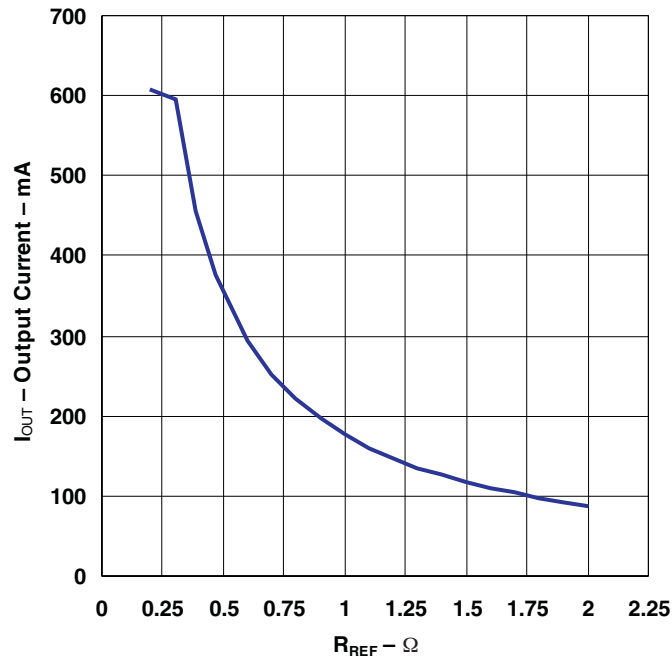


Figure 7. Output Current vs External Resistor

9 Power Supply Recommendations

The input voltage at the I pin must be greater than the sum of the LED forward voltages, the voltage drop across the TL4242 (from I to Q), and the voltage drop across the shunt resistor R_{REF} . For an example of this calculation, refer to [Typical Application](#). The input voltage should not exceed the recommended maximum operation voltage of 42 V.

10 Layout

10.1 Layout Guidelines

The REF pin should be routed directly to the shunt resistor, R_{REF} . If there is a long PCB trace between the LED string and the shunt resistor, the REF pin should connect close to the shunt resistor (rather than close to the LED string) to allow for accurate sensing across the shunt resistor.

The traces for I and Q will carry the full LED current. These traces should be the appropriate width to carry the LED current.

The exposed thermal pad on the bottom of the TL4242 should be connected to the PCB. The thermal pad helps to dissipate heat in the case of high power dissipation in the device. To further enhance the thermal performance of the device, the thermal pad can be connected by vias to the ground layer in the PCB.

10.2 Layout Example

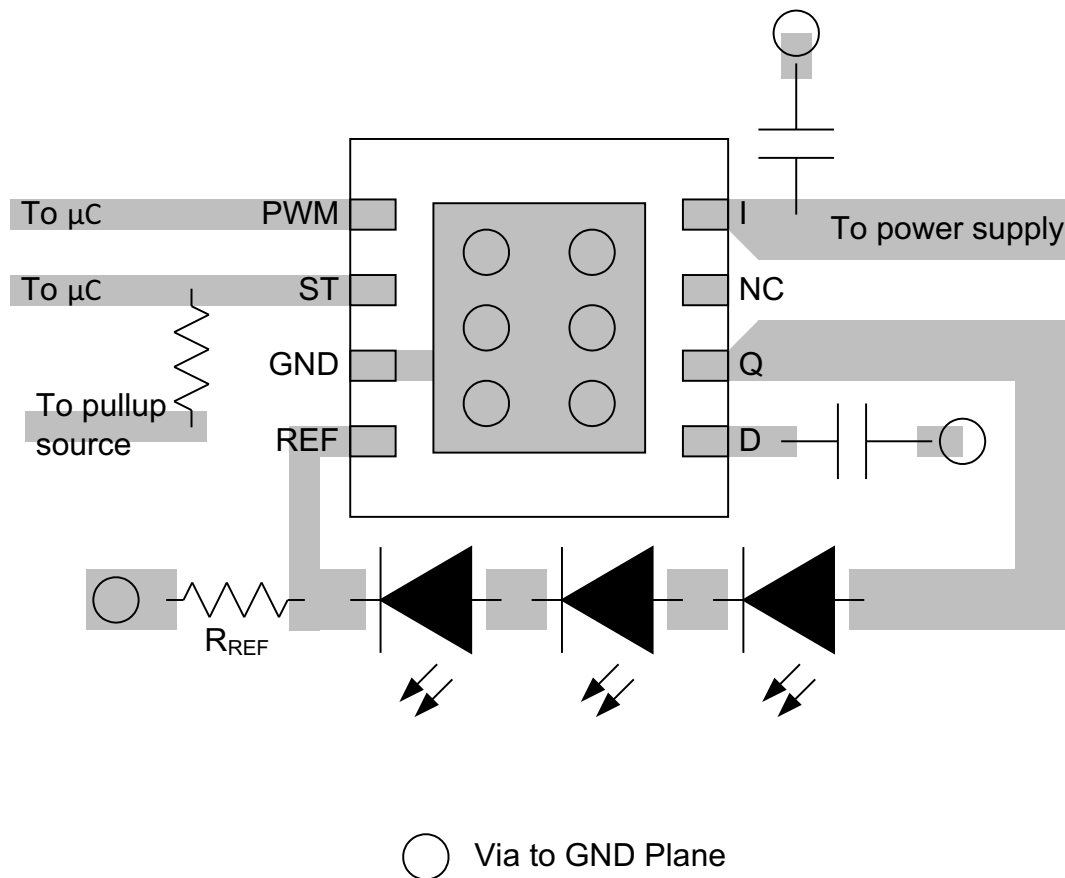


Figure 8. PCB Layout

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TL4242DRJR | ACTIVE | SON | DRJ | 8 | 3000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | T4242 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL4242 :

- Automotive: [TL4242-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL4242DRJR | SON | DRJ | 8 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

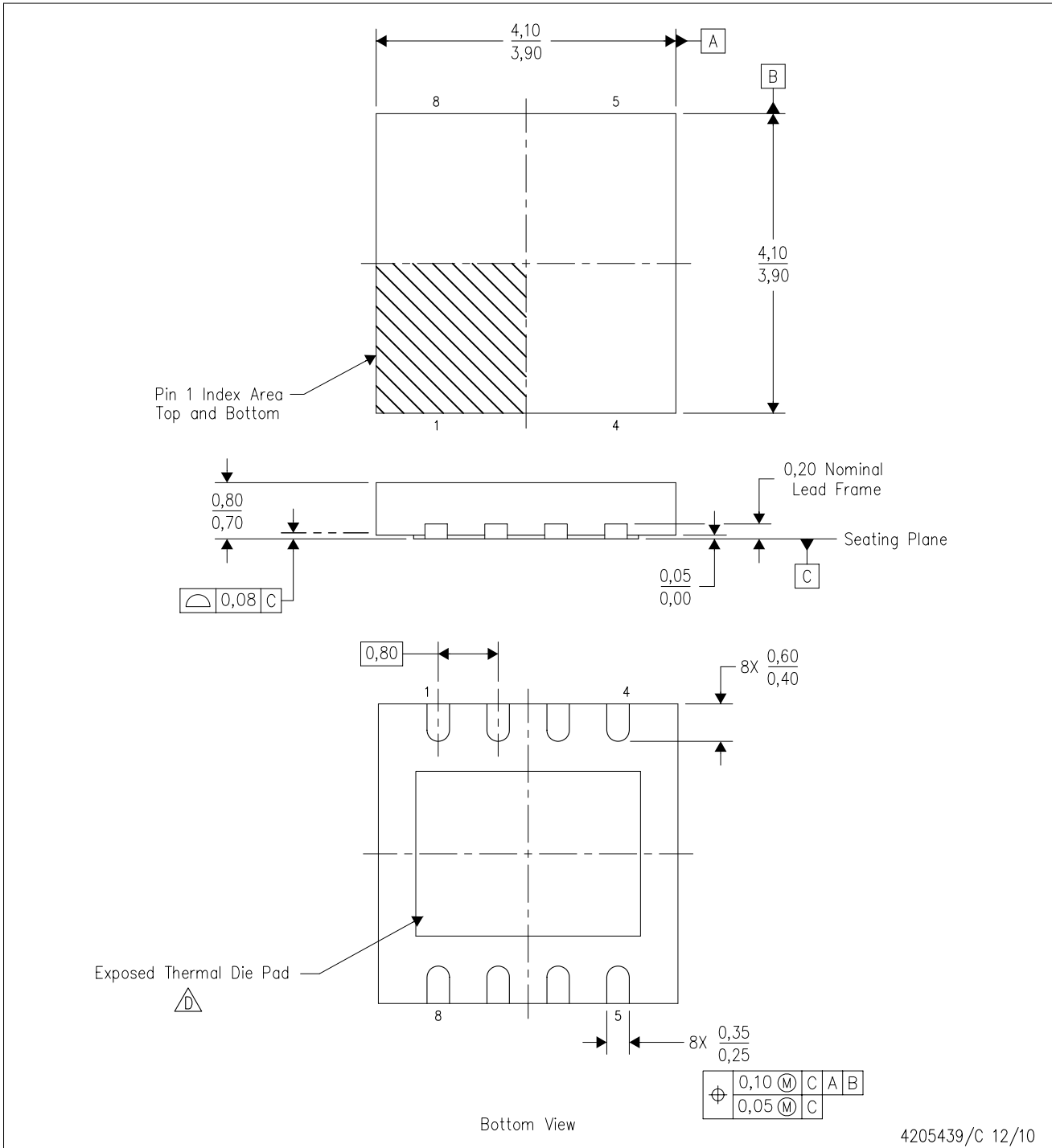


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL4242DRJR | SON | DRJ | 8 | 3000 | 356.0 | 356.0 | 35.0 |

DRJ (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4205439/C 12/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-229 variation WGGB.

THERMAL PAD MECHANICAL DATA

DRJ (S-PWSON-N8)

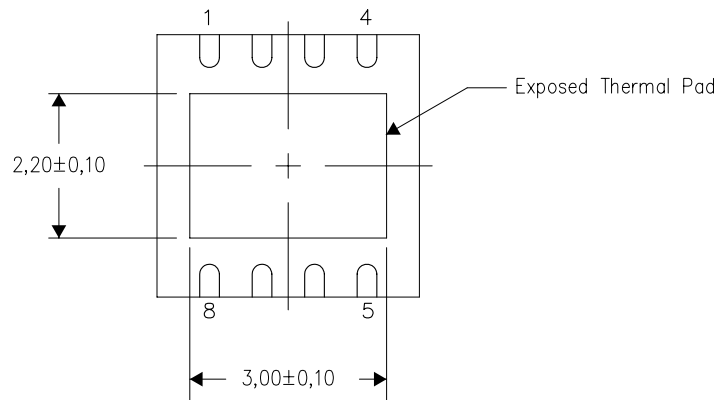
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

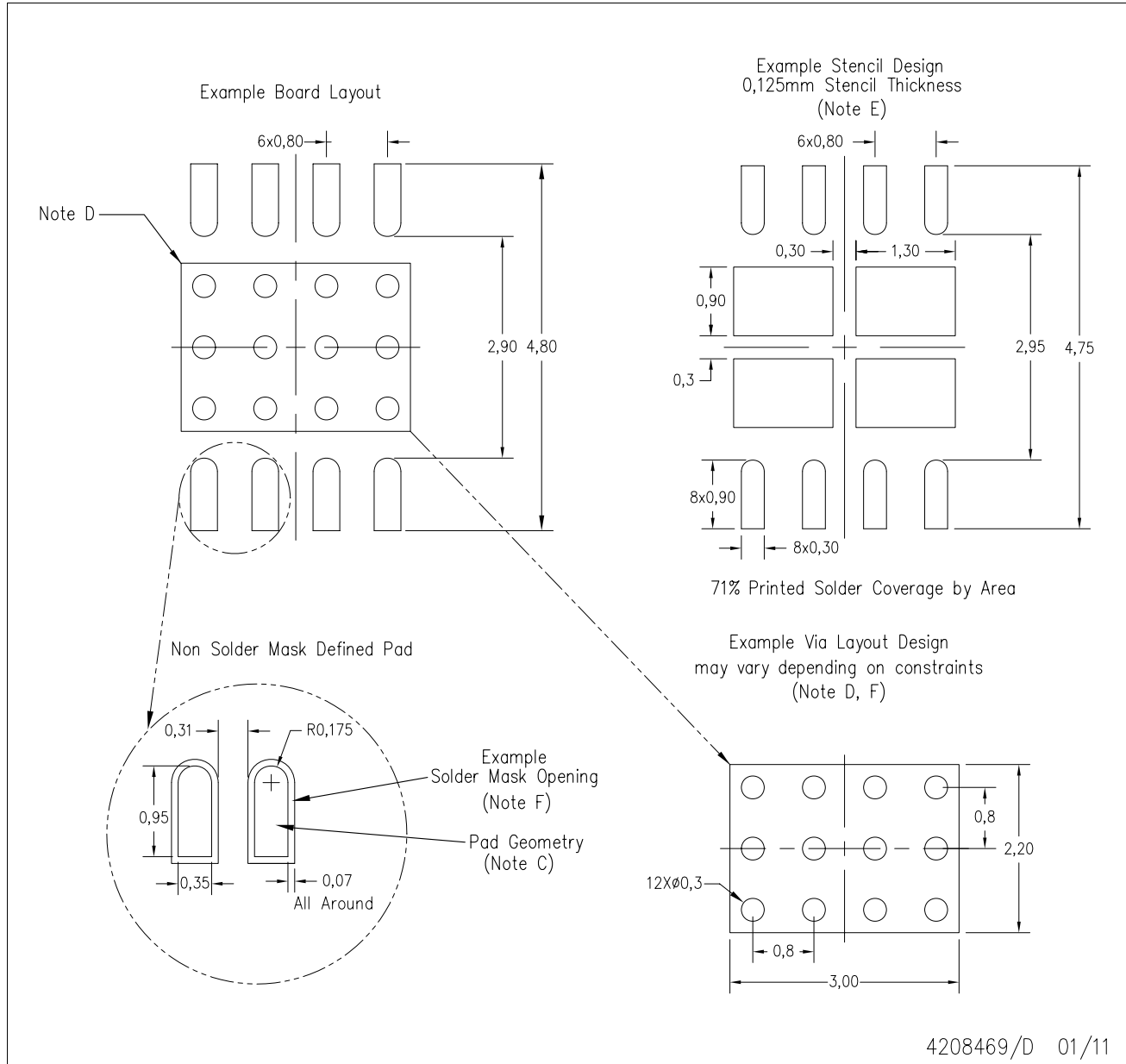
Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S-PWSON-N8)

SMALL PACKAGE OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

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