SNx5ALS176、SN75ALS176A 和 SN75ALS176B 差分总线收发器

1 特性

- 符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 的要求 [1] 以及 ITU 建议 V.11 和 X.27
- 在高达 35Mbaud 的数据速率下运行
- 提供四个偏差限制：
  - SN65ALS176：15ns
  - SN75ALS176：10ns
  - SN75ALS176A：7.5ns
  - SN75ALS176B：5ns
- 适用于嘈杂环境中长距离总线线路上的多点传输
- 低电源电流要求：30mA（最大值）
- 宽正负输入/输出总线电压范围
- 热关断保护
- 驱动器正负电流限制
- 接收器输入迟滞
- 无干扰上电和断电保护
- 接收器开路失效防护设计

2 说明

SN65ALS176 和 SN75ALS176 系列差分总线收发器旨在实现多点总线传输线路上的双向数据通信。这些器件专为平衡传输线路而设计，符合 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU 建议 V.11 和 X.27。

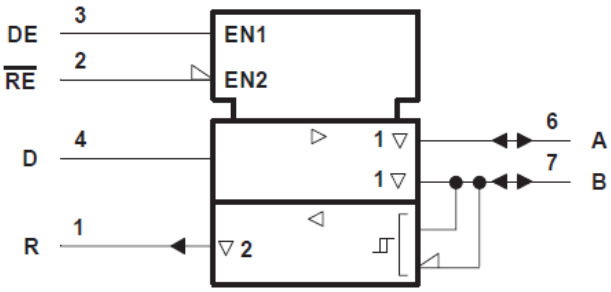
SN65ALS176 和 SN75ALS176 系列整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，这些端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。该端口具有较宽的正负共模电压范围，使得该器件适用于合用线应用。

SN65ALS176 的额定工作温度范围为 –40°C 至 85°C。SN75ALS176 系列的额定工作温度范围为 0°C 至 70°C。

封装信息

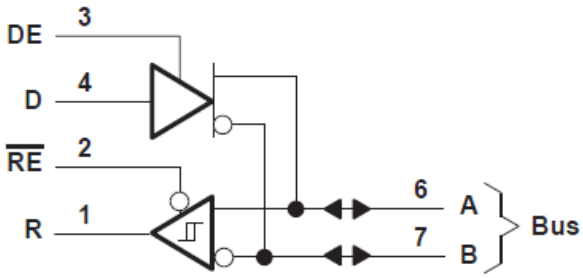
器件型号	封装(1)	封装尺寸（标称值）
SNx5ALS176	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81mm x 6.35mm
SN75ALS176A	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81mm x 6.35mm
SN75ALS176B	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81mm x 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



A. 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

逻辑符号



逻辑图（正逻辑）

[1] 这些器件符合或超出 TIA/EIA-485-A 的要求，但发生器争用测试（第 3.4.2 段）和发生器电流限制（第 3.4.3 段）除外。对于 SN75ALS176、SN75ALS176A 和 SN75ALS176B，所施加的测试电压范围为 –6V 至 8V；对于 SN65ALS180，所施加的测试电压范围为 –4V 至 8V。

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3 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (June 2000) to Revision I (January 2023)	Page
• 将文档更改为了最新 TI 格式	1
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics* graphs	9

4 Pin Configuration and Functions

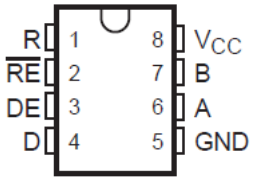


图 4-1. D or P Package (Top View)

表 4-1. Pin Functions

NO	Name	Type	Description
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	i	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V_{CC}	SUPPLY	4.75-V to 5.25-V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-7	12	V
V_I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 建议运行条件

（除非另有说明）

			最小值	标称值	最大值	单位
V_{CC}	电源电压		4.75	5	5.25	V
V_I 或 V_{IC}	任何总线端子上的输入电压（独立或共模）				12	V
					–7	
V_{IH}	高电平输入电压	D、DE 和 $\overline{RE}$	2			V
V_{IL}	低电平输入电压	D、DE 和 $\overline{RE}$			0.8	V
V_{ID}	差动输入电压(1)				±12	V
I_{OH}	高电平输出电流	驱动器			-60	mA
		接收器			–400	μA
I_{OL}	低电平输出电流	驱动器			60	mA
		接收器			8	
T_A	自然通风工作温度范围	SN65ALS176	–40		85	°C
		SN75ALS176 系列	0		70	

(1) 差分输入/输出总线电压在同相端子 A 和反相端子 B 之间测得。

5.3 Thermal Information

THERMAL METRIC(1)		P (PDIP) 8-Pins	D (SOIC) SN65 Devices 8-Pins	D (SOIC) SN75 Devices 8-Pin	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.7	62.6	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 图 6-1	½ V_{OD1} or 2(3)			V
		R_L = 54 Ω	See 图 6-1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See 图 6-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω	See 图 6-1			3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
I_O	Output current	Outputs disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I= 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current(5)	V_O = –4 V	SN65ALS176			–250	mA
		V_O = –6 V	SN75ALS176			–250	
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω loadis either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of VOD and VOC, respectively, that occur when the input is changed from one logic state to the other.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3			15	ns
$t_{sk(p)}$	Pulse skew(2)	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3			15	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-5			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.6 Switching Characteristics - Driver

SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	'ALS176	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3	3	8	13	ns
		'ALS176A				4	7	11.5	
		'ALS176B				5	8	10	
$t_{sk(p)}$	Pulse skew(2)		R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	'ALS176	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3			10	ns
		'ALS176A						7.5	
		'ALS176B						5	
$t_{t(OD)}$	Differential output transition time		R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-5		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.7 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t(R_L = 100 Ω)	V_t(R_L = 54 W)
$\|V_{OD3}\|$	None	V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	None
I_O	$\|Ix_a\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.8 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+}– $V_{IT–}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See 图 6-6	I_{OH} = –400 mA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, SeeFigure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
V_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	–15		–85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.9 Switching Characteristics - Receiver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew(2)	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	R_L = 54 Ω See 图 6-3	C_L = 50 pF,			15	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See 图 6-8		11	18	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See 图 6-8		11	18	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See 图 6-8			50	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See 图 6-8			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH}– t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.10 Switching Characteristics - Receiver

SN75ALS176,SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,	9	14	19	ns
		'ALS176A			10.5	14	18	
		'ALS176B			11.5	13	16.5	
$t_{sk(p)}$	Pulse skew(2)		V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	'ALS176	R_L = 54 Ω See 图 6-3	C_L = 50 pF,			10	ns
		'ALS176A					7.5	
		'ALS176B					5	
t_{PZH}	Output enable time to high level		C_L = 15 pF,	See 图 6-8		7	14	ns
t_{PZL}	Output enable time to low level		C_L = 15 pF,	See 图 6-8		20	35	ns
t_{PHZ}	Output disable time from high level		C_L = 15 pF,	See 图 6-8		20	35	ns
t_{PLZ}	Output disable time from low level		C_L = 15 pF,	See 图 6-8		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.11 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

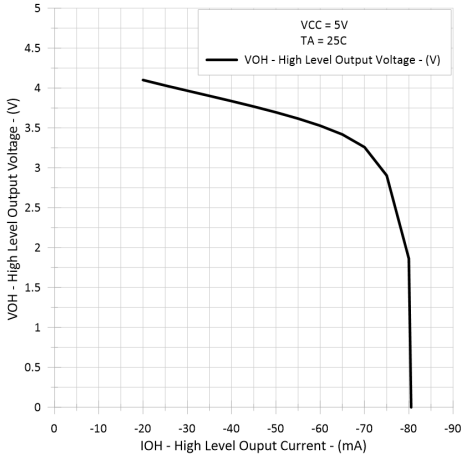


图 5-1. Driver High-LeveL Output Voltage vs High-Level Output Current

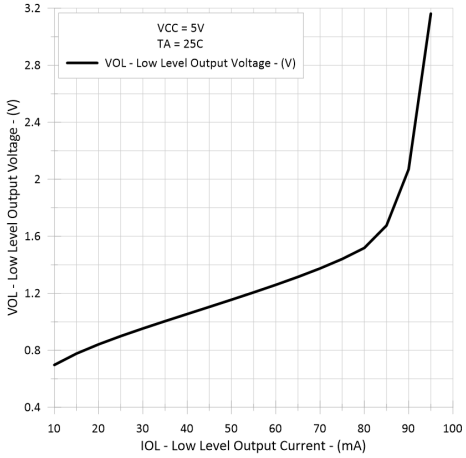


图 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

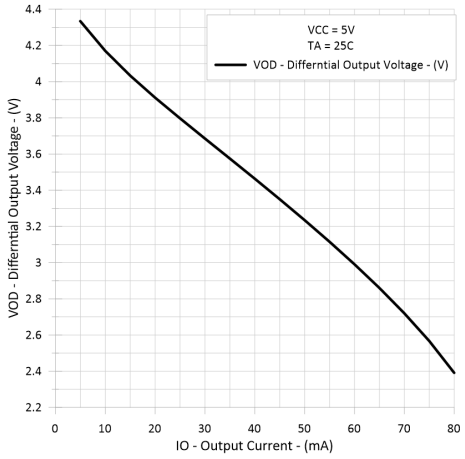


图 5-3. Driver Differential Output Voltage vs Output Current

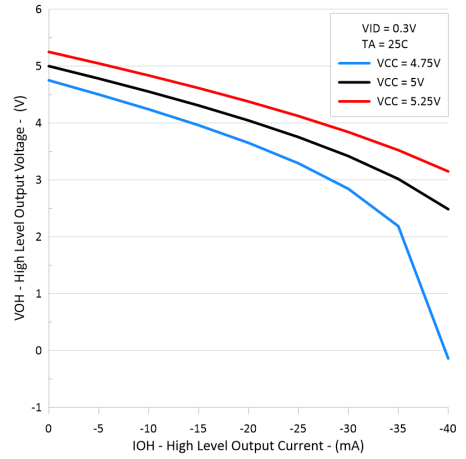


图 5-4. Receiver High-Level Output Voltage vs High-Level Output Current

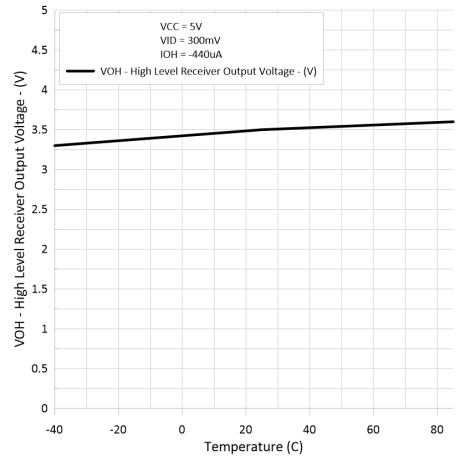


图 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature

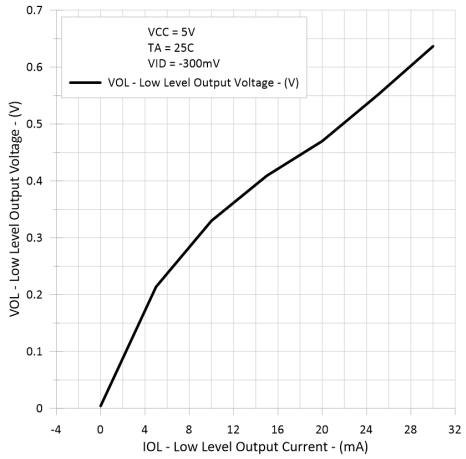


图 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

5.11 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

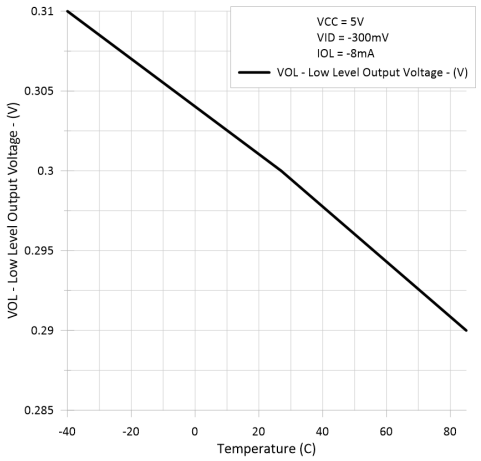


图 5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature

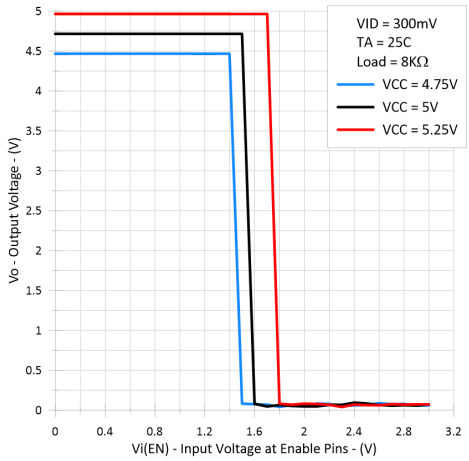


图 5-8. Receiver Output Voltage vs Enable Voltage

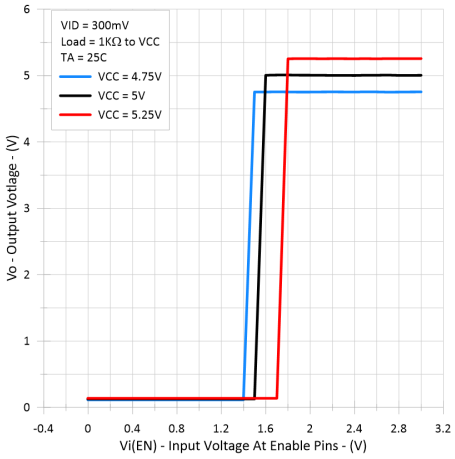


图 5-9. Receiver Output Voltage vs Enable Voltage

6 Parameter Measurement Information

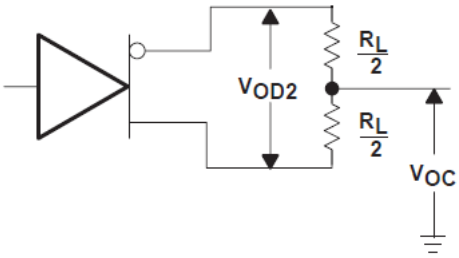


图 6-1. Driver V_{OD2} and V_{OC}

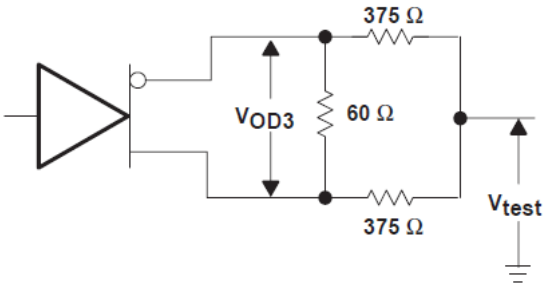
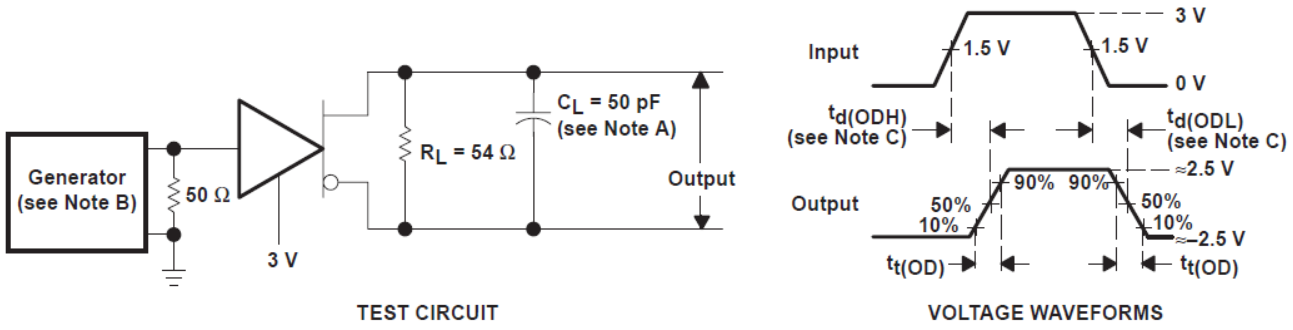
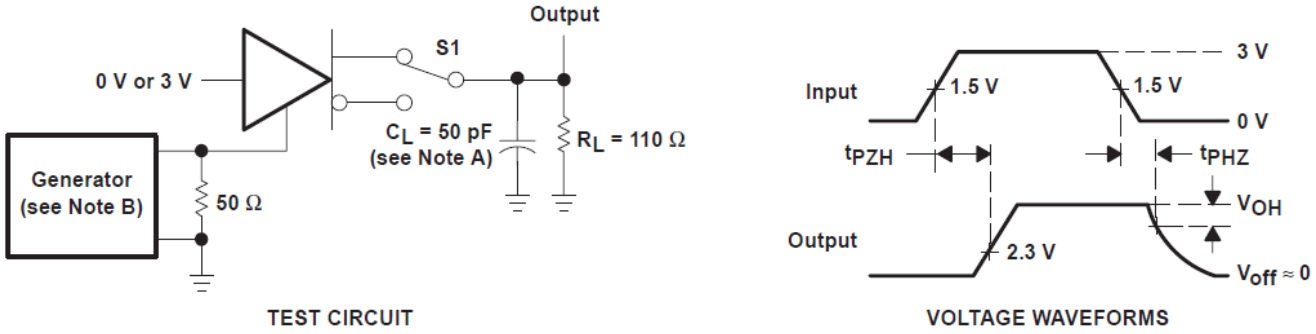


图 6-2. Driver V_{OD3}



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

图 6-3. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

图 6-4. Driver Test Circuit and Voltage Waveforms

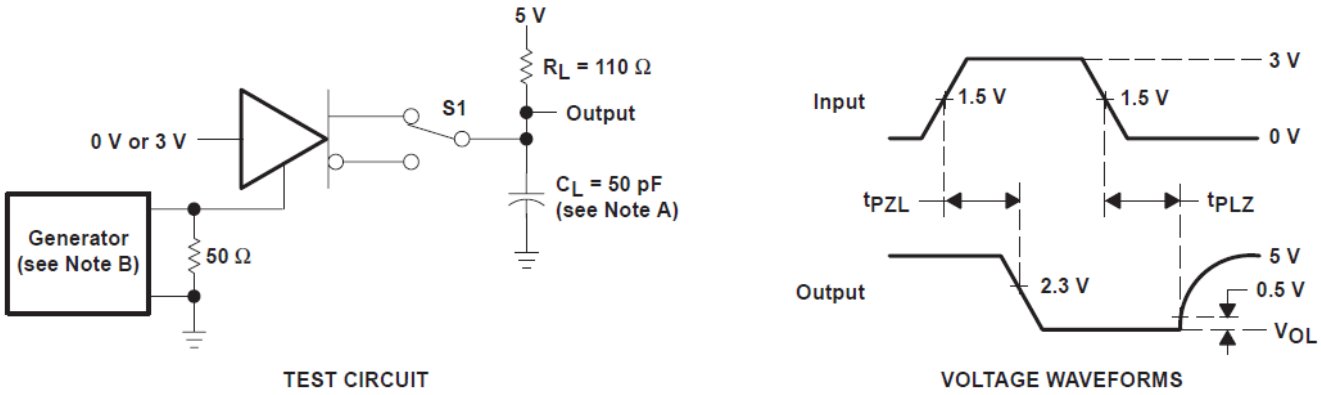


图 6-5. Driver Test Circuit and Voltage Waveforms

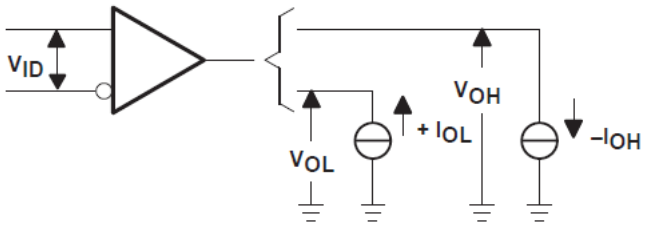
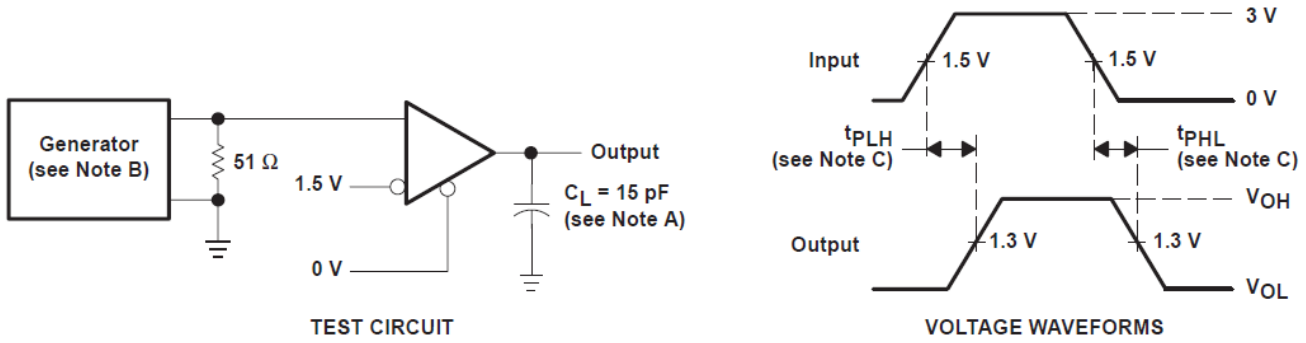


图 6-6. Receiver V_{OH} and V_{OL} Test Circuit

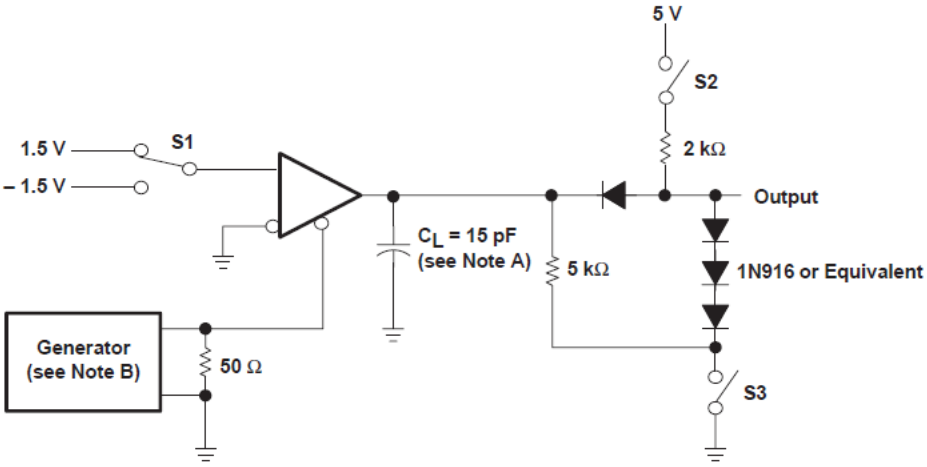


A. C_L includes probe and jig capacitance.

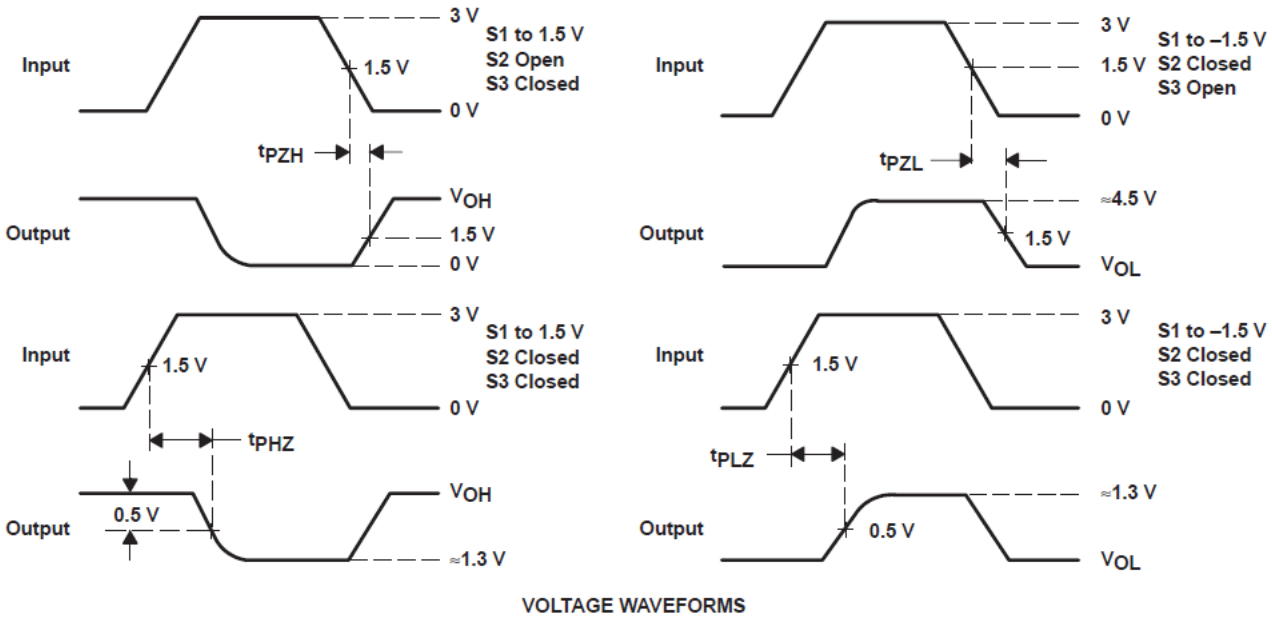
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

C. $t_{pd} = t_{PLH}$ or t_{PHL}.

图 6-7. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

图 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

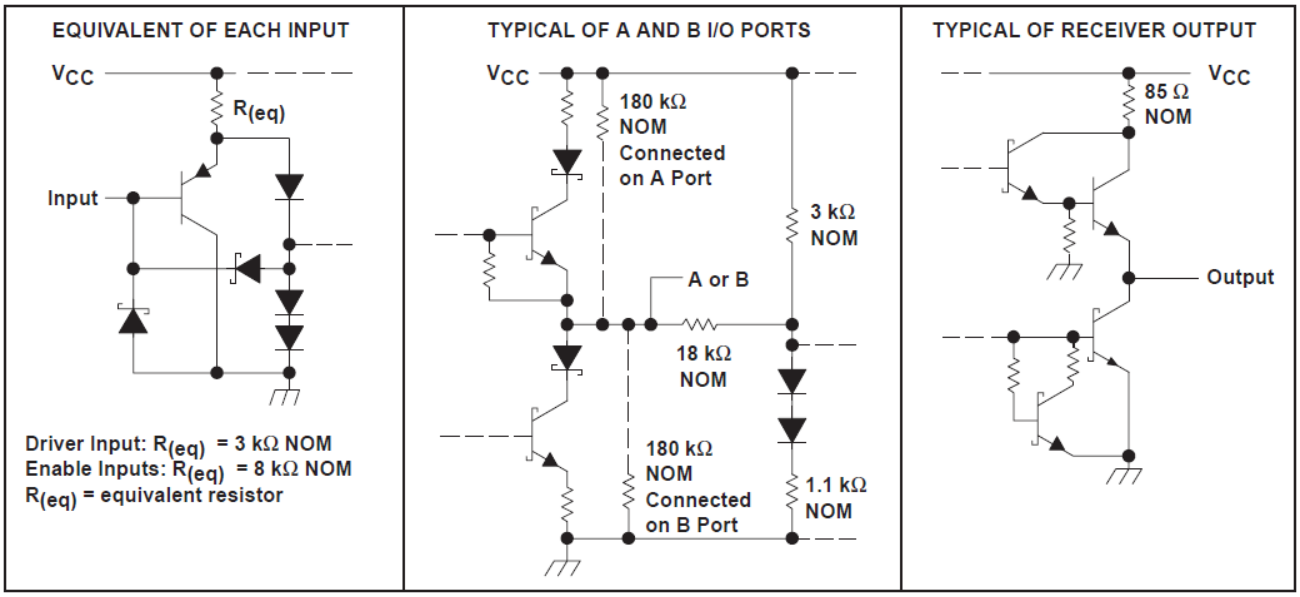


图 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Receiver(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

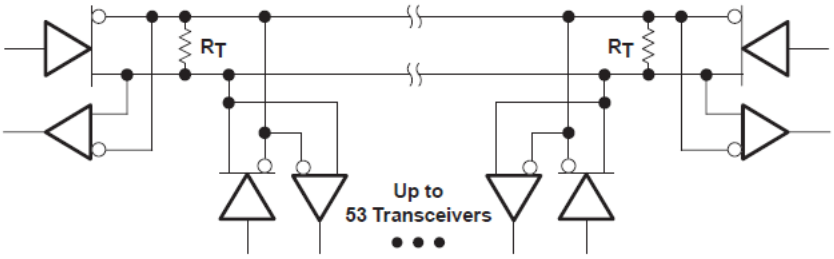
8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

8.1 Application Information

8.2 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS176D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176	
SN65ALS176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176	Samples
SN75ALS176AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A	Samples
SN75ALS176ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A	Samples
SN75ALS176ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A	Samples
SN75ALS176AP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176A	
SN75ALS176BD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176B	
SN75ALS176BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(75A176, 7A176B)	Samples
SN75ALS176BP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176B	
SN75ALS176D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75A176	
SN75ALS176DR	NRND	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75A176	
SN75ALS176P	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176	
SN75ALS176PE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

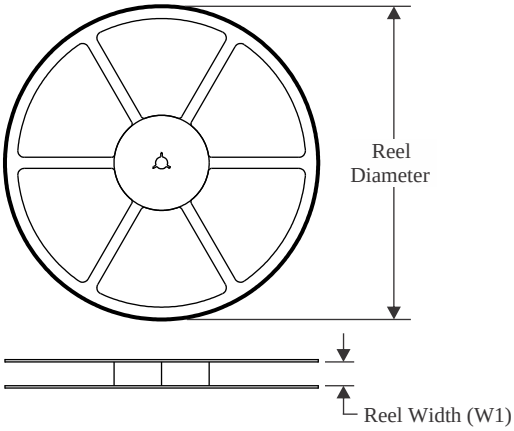
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

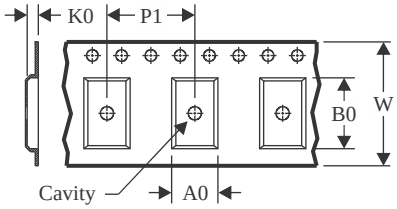
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

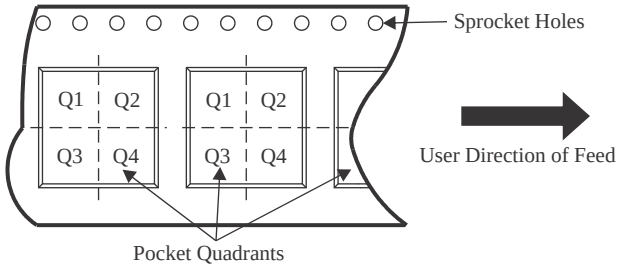


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

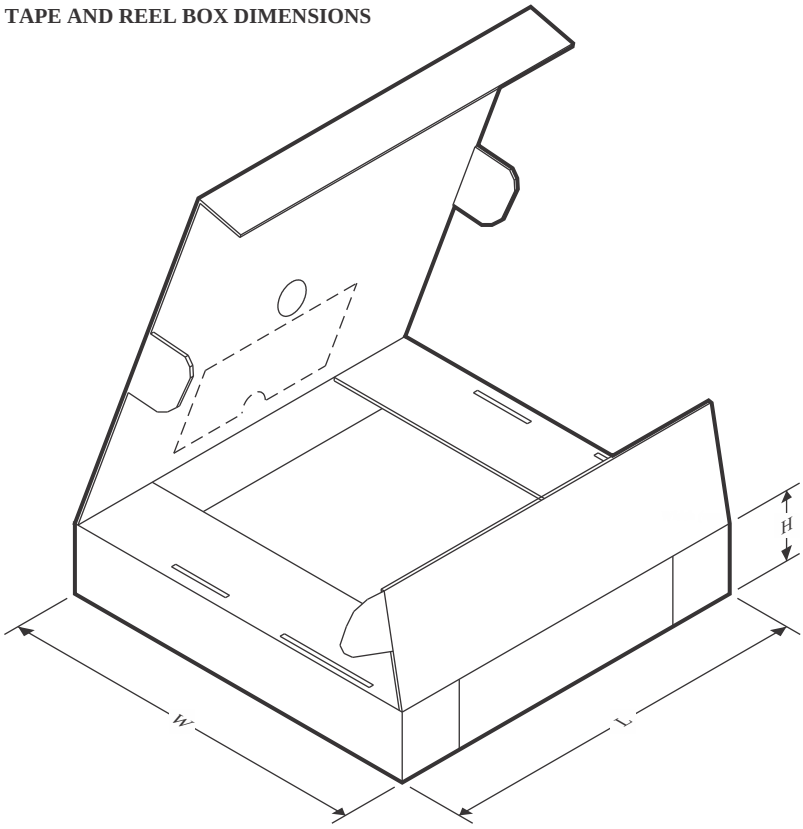
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65ALS176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

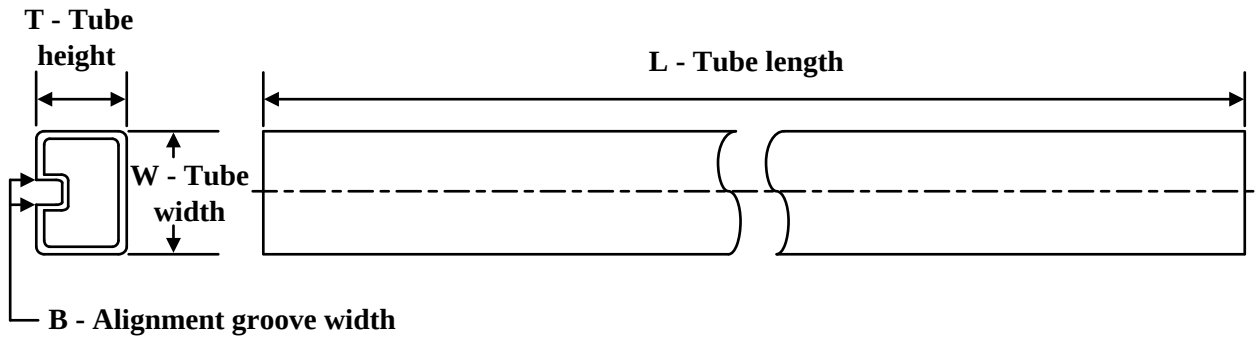
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS176DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65ALS176DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75ALS176ADR	SOIC	D	8	2500	340.5	336.1	25.0
SN75ALS176BDR	SOIC	D	8	2500	356.0	356.0	35.0
SN75ALS176BDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75ALS176DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

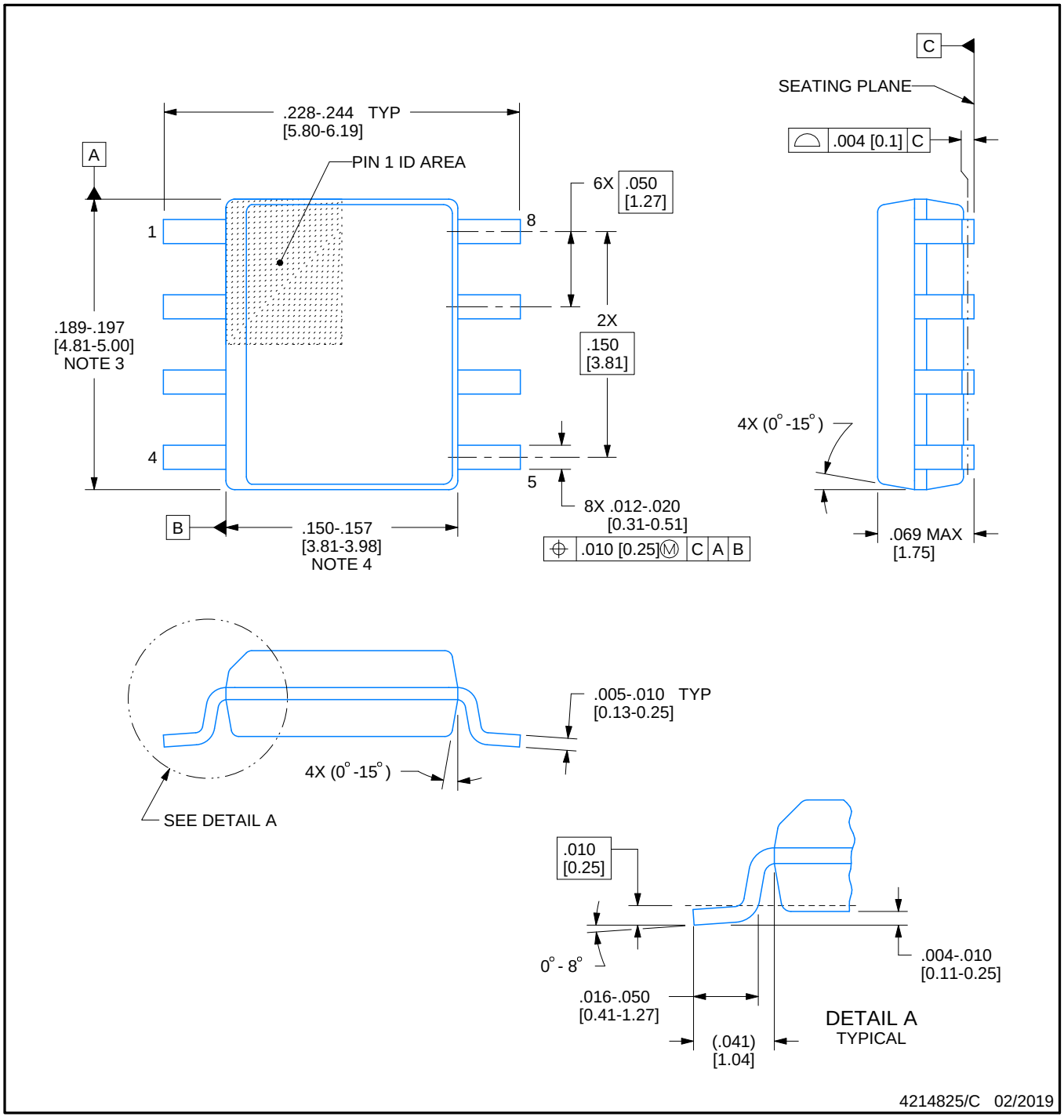
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65ALS176D	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176AD	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176BD	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176D	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176P	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176PE4	P	PDIP	8	50	506	13.97	11230	4.32

PACKAGE OUTLINE

D0008A

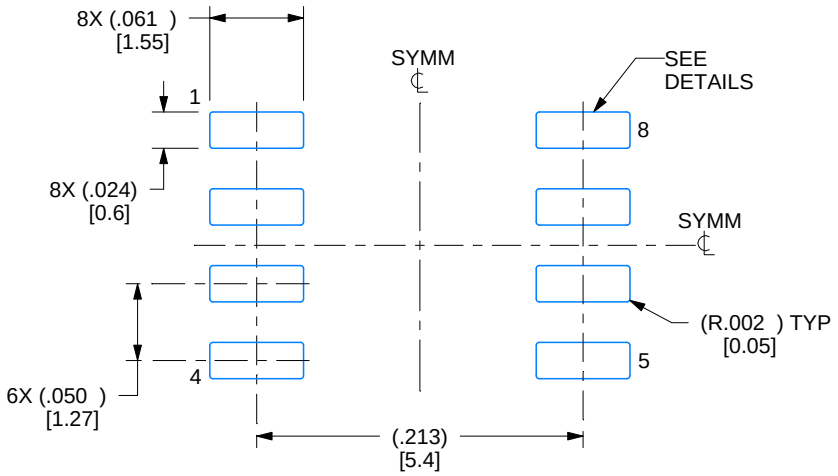
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

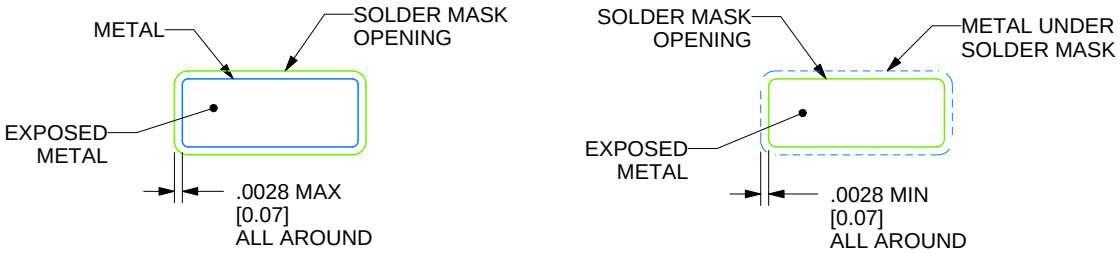


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

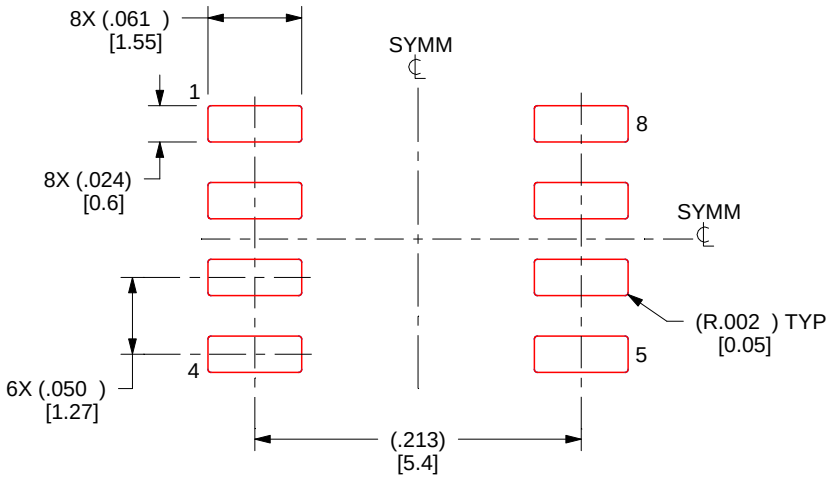
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



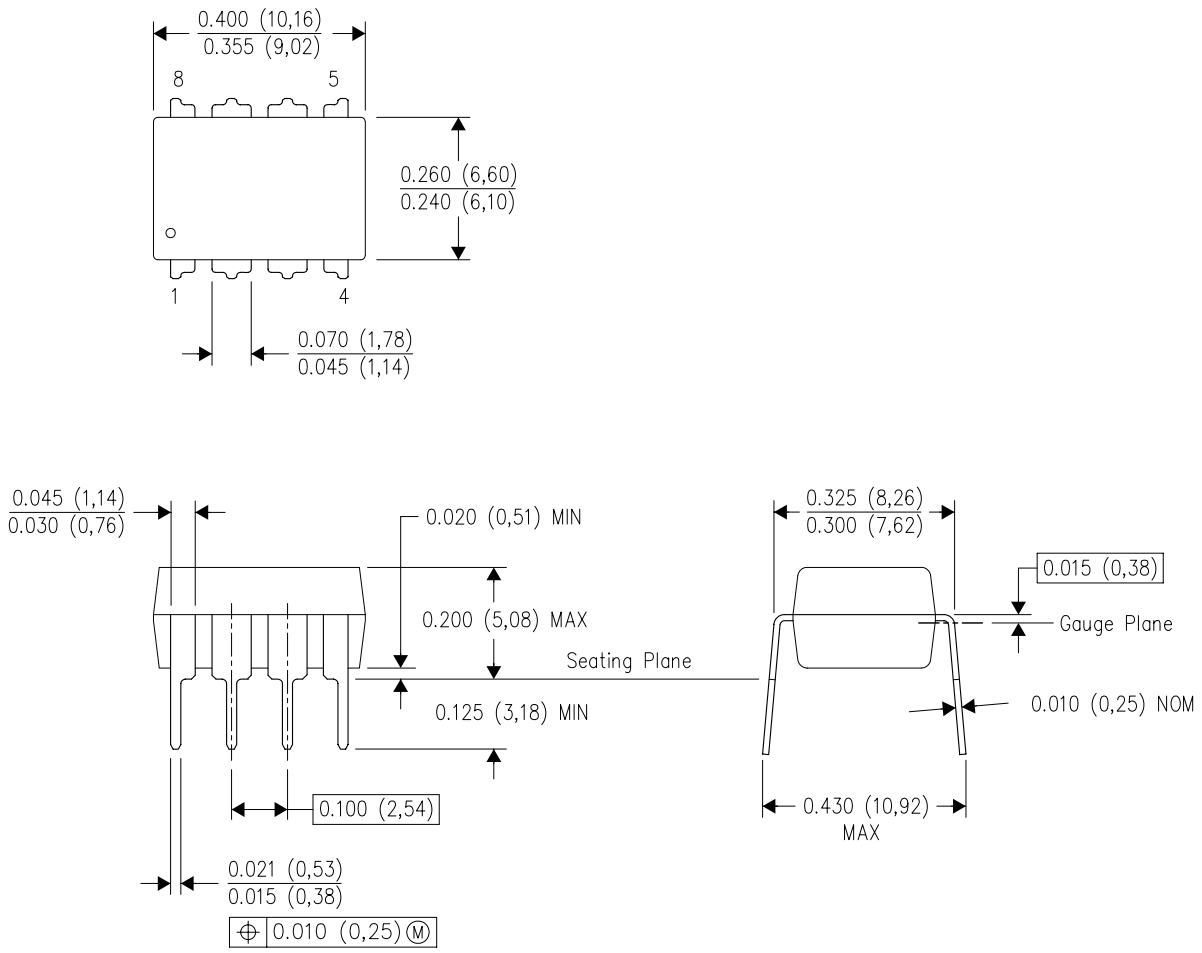
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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