# SNx4AHCT244 Octal Buffers/Drivers With 3-State Outputs

## 1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA Per JESD 17
- On products compliant to MIL-PRF-38535, All parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## 2 Applications

- Network Switches
- Power Infrastructures
- PCs and Notebooks
- Wearable Health and Fitness Devices
- Tests and Measurements

## 3 Description

These octal buffers/drivers are designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

**Package Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| SNx4AHCT244 | PDIP (20) | 25.40 mm x 6.35 mm |
| | (SOIC, 20) | 12.8 mm x 7.5 mm |
| | SOP (20) | 12.60 mm x 5.30 mm |
| | SSOP (20) | 7.50 mm x 5.30 mm |
| | TVSOP (20) | 5.00 mm x 4.40 mm |
| | TSSOP (20) | 6.50 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

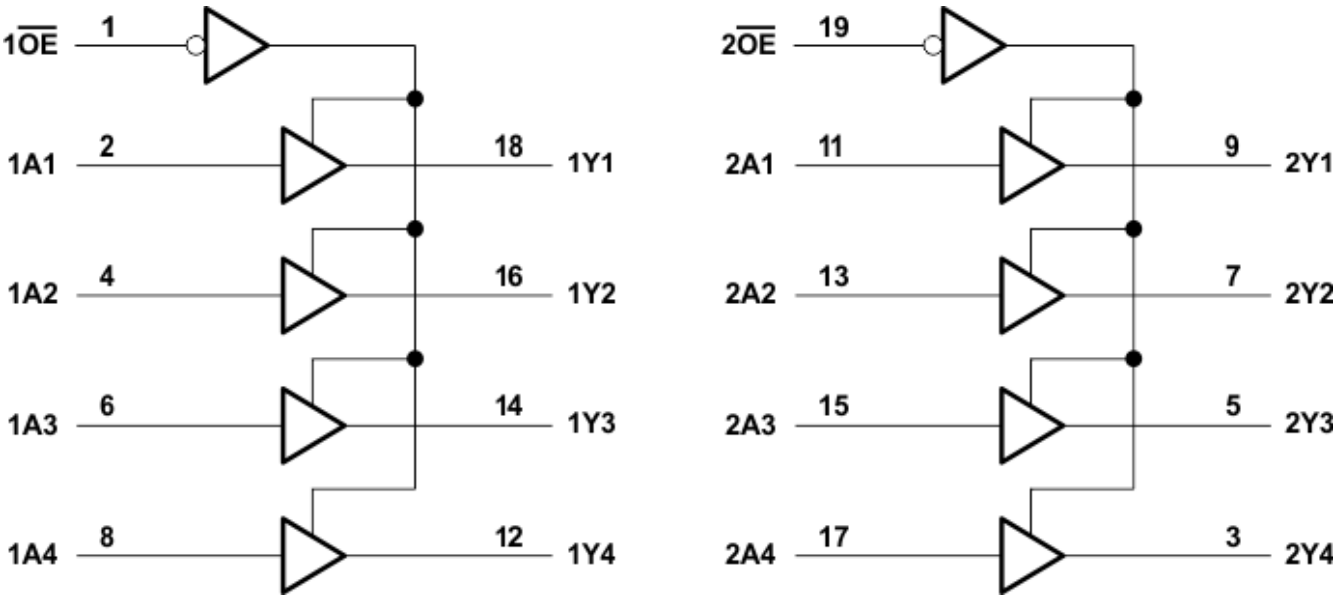



**Figure 3-1. Simplified Schematic**

## Table of Contents



## 4 Revision History

**Changes from Revision M (July 2014) to Revision N (May 2023)** **Page**

- Updated *ESD Ratings* section, *Absolute Maximum Ratings* section, and *Package Information* table....1

## 5 Pin Configuration and Functions

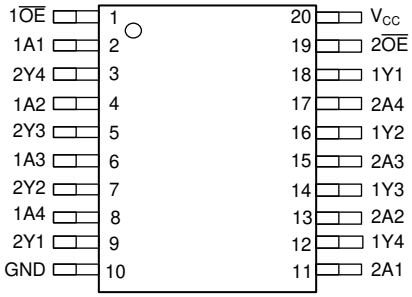



**Figure 5-1. SN54AHCT244 J or W Package; SN74AHCT244 DB, DGV, DW, N, NS, or PW Package (Top View)**

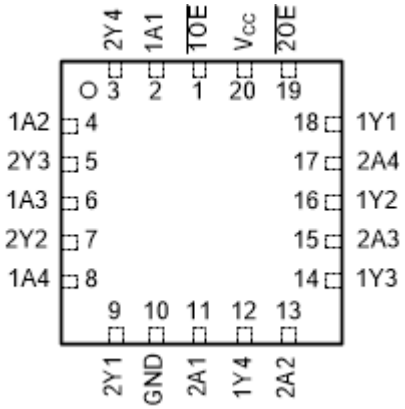



**Figure 5-2. SN54AHCT244 FK Package (Top View)**

**Table 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1 $\overline{OE}$ | I | Output Enable 1 |
| 2 | 1A1 | I | Input 1A1 |
| 3 | 2Y4 | O | Output 2Y4 |
| 4 | 1A2 | I | Input 1A2 |
| 5 | 2Y3 | O | Output 2Y3 |

**Table 5-1. Pin Functions (continued)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 6 | 1A3 | I | Input 1A3 |
| 7 | 2Y2 | O | Output 2Y2 |
| 8 | 1A4 | I | Input 1A4 |
| 9 | 2Y1 | O | Output 2Y1 |
| 10 | GND | – | Ground Pin |
| 11 | 2A1 | I | Input 2A1 |
| 12 | 1Y4 | O | Output 1Y4 |
| 13 | 2A2 | I | Input 2A2 |
| 14 | 1Y3 | O | Output 1Y3 |
| 15 | 2A3 | I | Input 2A3 |
| 16 | 1Y2 | O | Output 1Y2 |
| 17 | 2A4 | I | Input 2A4 |
| 18 | 1Y1 | O | Output 1Y1 |
| 19 | 2 $\overline{OE}$ | I | Output Enable 2 |
| 20 | VCC | – | Power Pin |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

see note 1

| | | SN54AHCT244 | | SN74AHCT244 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74AHCT244 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DB | DGV | DW | N | NS | PW | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 99.9 | 119.2 | 83.0 | 54.9 | 80.4 | 105.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 61.7 | 34.5 | 48.9 | 41.7 | 46.9 | 39.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 55.2 | 60.7 | 50.5 | 35.8 | 47.9 | 56.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 22.6 | 1.2 | 21.1 | 27.9 | 19.9 | 3.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.8 | 60.0 | 50.1 | 35.7 | 47.5 | 55.8 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT244 | | SN74AHCT244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1[1] | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $\Delta I_{CC}$ [2] | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT244 | | SN74AHCT244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.4[1] | 7.4[1] | 1[1] | 8.5[1] | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5.4[1] | 7.4[1] | 1[1] | 8.5[1] | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7.7[1] | 10.4[1] | 1[1] | 12[1] | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 7.7[1] | 10.4[1] | 1[1] | 12[1] | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5[1] | 9.4[1] | 1[1] | 10[1] | 1 | 10 | ns |
| $t_{PLZ}$ | | | | | 5[1] | 9.4[1] | 1[1] | 10[1] | 1 | 10 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.9 | 8.4 | 1 | 9.5 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 8.2 | 11.4 | 1 | 13 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8.8 | 11.4 | 1 | 13 | 1 | 13 | |

## 6.6 Switching Characteristics (continued)

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT244 | | SN74AHCT244 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1[2] | | | | 1 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 6.7 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER[1] | | SN74AHCT244 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

(1) Characteristics are for surface-mount packages only.

## 6.8 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 8.2 | pF |

## 6.9 Typical Characteristics

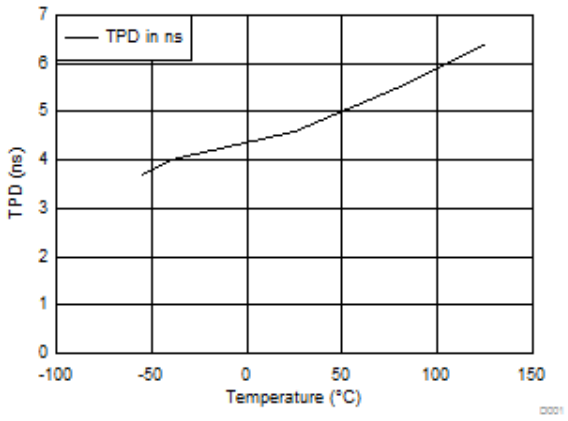
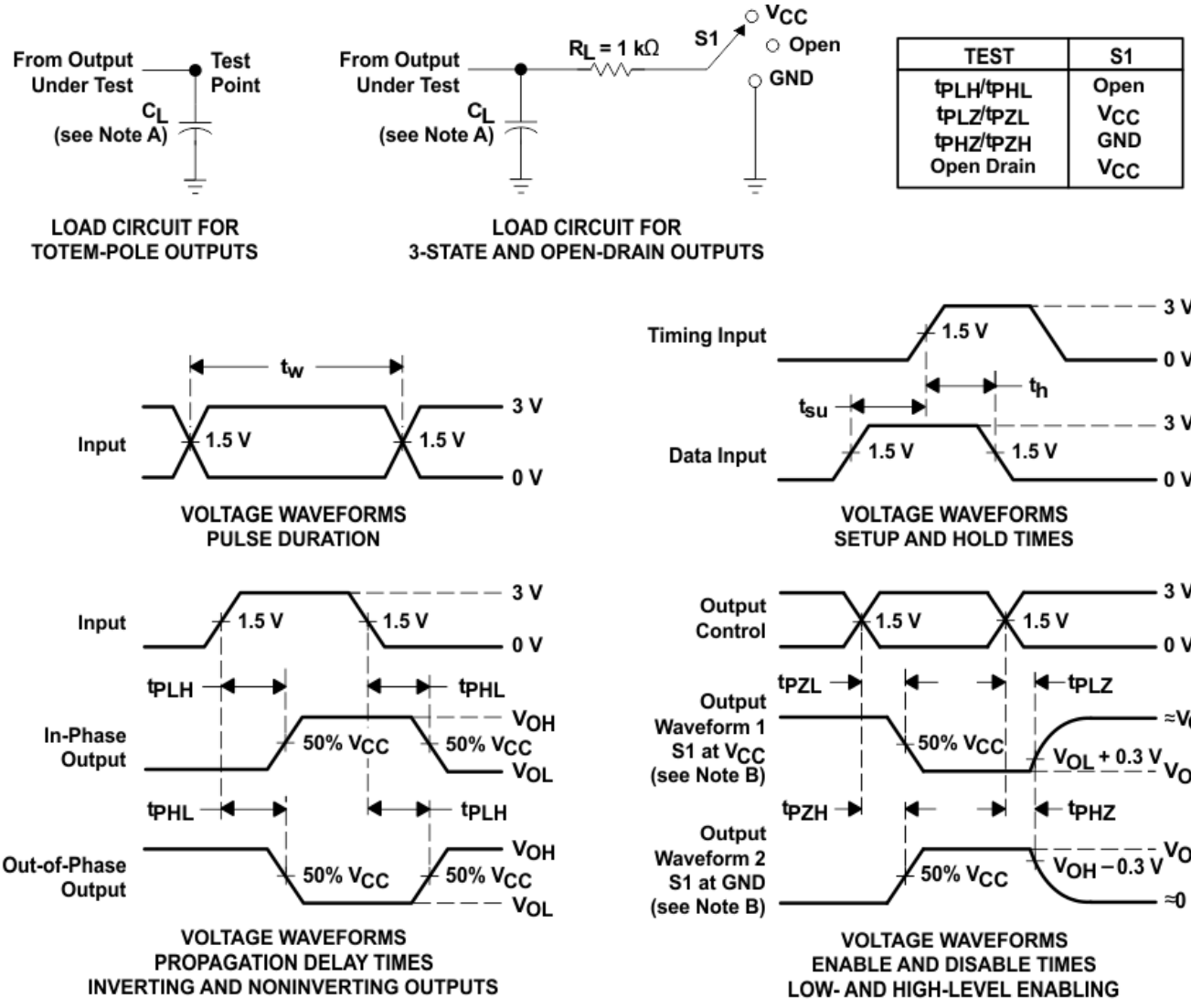



**Figure 6-1. TPD vs Temperature, 15 pF Load**

## 7 Parameter Measurement Information




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

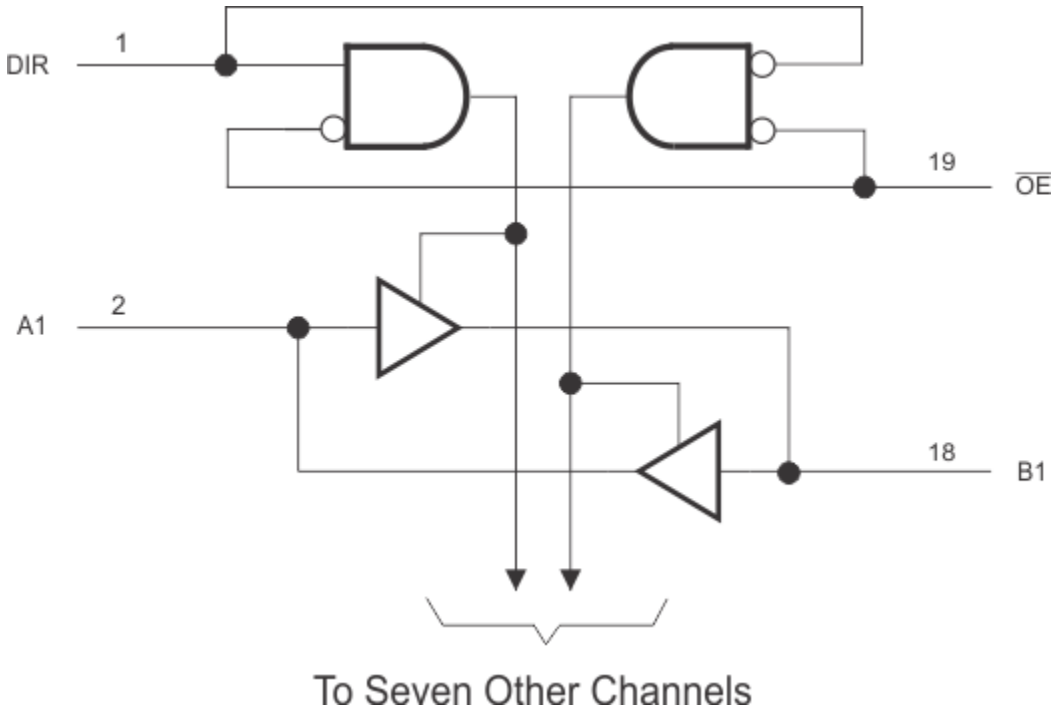
**Figure 7-1. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SNx4AHCT244 devices are organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

- $V_{CC}$ is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
  - Inputs Accept $V_{IH}$ levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

## 8.4 Device Functional Modes

**Table 8-1. Function Table (Each 4-Bit Buffer/Driver)**

| INPUTS | | OUTPUT Y |
|---|---|---|
| $\overline{OE}$ | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74AHCT244 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V $V_{IL}$ and 2-V $V_{IH}$. This feature makes it ideal for translating up from 3.3 V to 5 V. Figure 9-1 shows this type of translation.

### 9.1.1 Typical Application

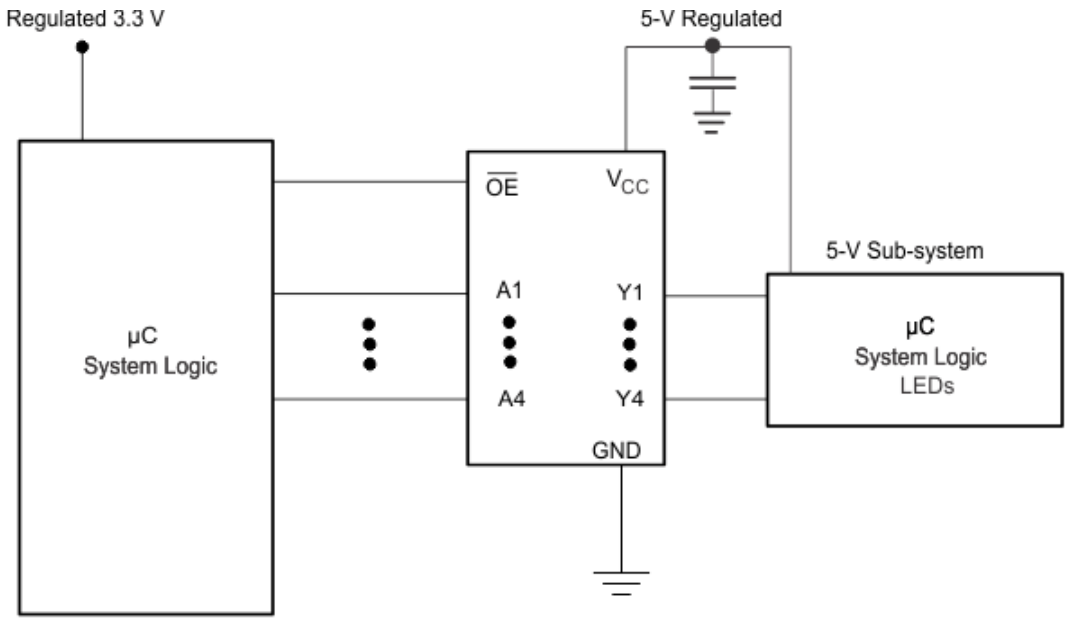



**Figure 9-1. Specific Application Schematic**

#### *9.1.1.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### *9.1.1.2 Detailed Design Procedure*

1. Recommended Input conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$
2. Recommend output conditions
   - Load currents should not exceed 25 mA on the output and 50 mA total for the part
   - Outputs should not be pulled above $V_{CC}$

#### 9.1.1.3 Application Curves

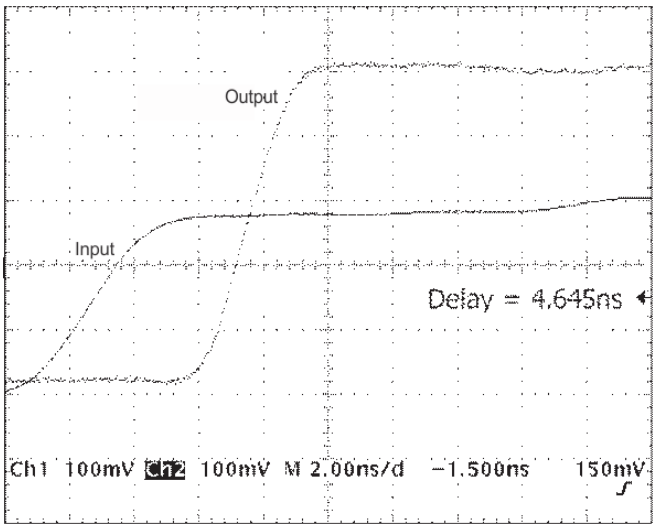



**Figure 9-2. Application Curve**

## 9.2 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple $V_{CC}$ pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 9.3 Layout

### 9.3.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 9-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 9.3.2 Layout Example

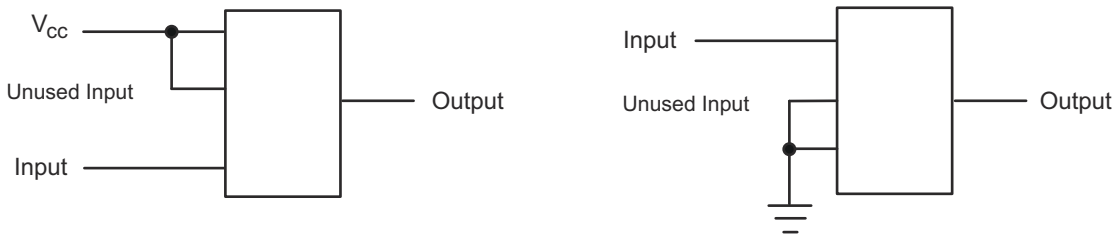



**Figure 9-3. Layout Diagram**

# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 10-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54AHCT244 | Click here | Click here | Click here | Click here | Click here |
| SN74AHCT244 | Click here | Click here | Click here | Click here | Click here |

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9678301Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678301Q2A SNJ54AHCT 244FK | Samples |
| 5962-9678301QRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678301QR A SNJ54AHCT244J | Samples |
| 5962-9678301QSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678301QS A SNJ54AHCT244W | Samples |
| SN74AHCT244DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HB244 | Samples |
| SN74AHCT244DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HB244 | Samples |
| SN74AHCT244DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT244 | Samples |
| SN74AHCT244N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74AHCT244N | Samples |
| SN74AHCT244NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHCT244 | Samples |
| SN74AHCT244PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HB244 | Samples |
| SN74AHCT244PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HB244 | Samples |
| SNJ54AHCT244FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678301Q2A SNJ54AHCT 244FK | Samples |
| SNJ54AHCT244J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678301QR A SNJ54AHCT244J | Samples |
| SNJ54AHCT244W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678301QS A SNJ54AHCT244W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54AHCT244, SN74AHCT244 :**

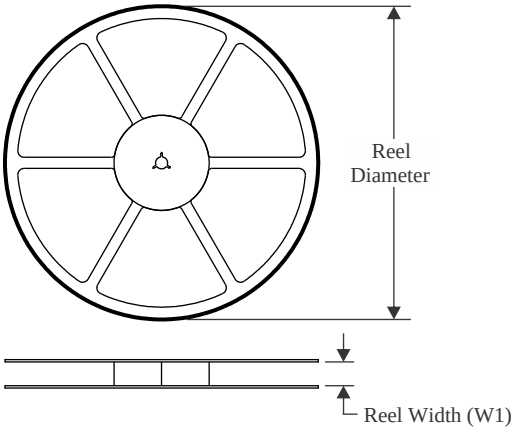
- Catalog : SN74AHCT244
- Automotive : SN74AHCT244-Q1, SN74AHCT244-Q1
- Enhanced Product : SN74AHCT244-EP, SN74AHCT244-EP
- Military : SN54AHCT244

NOTE: Qualified Version Definitions:

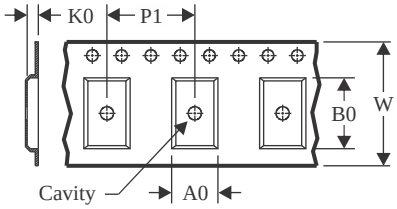
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

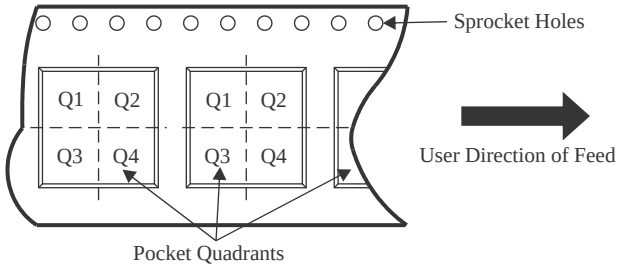



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

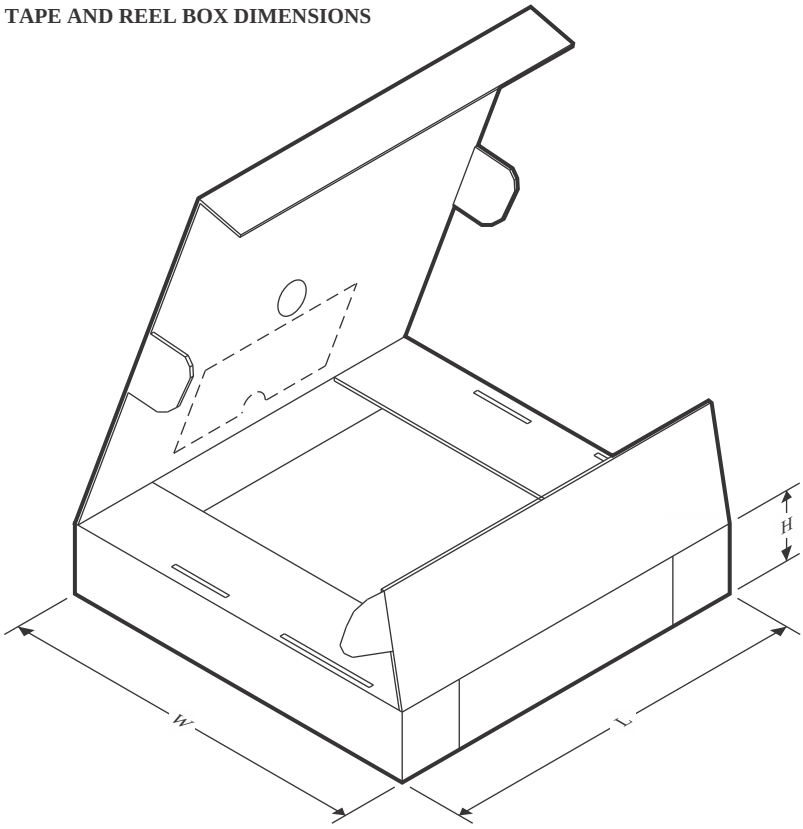
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHCT244DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT244DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHCT244NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHCT244PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHCT244PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

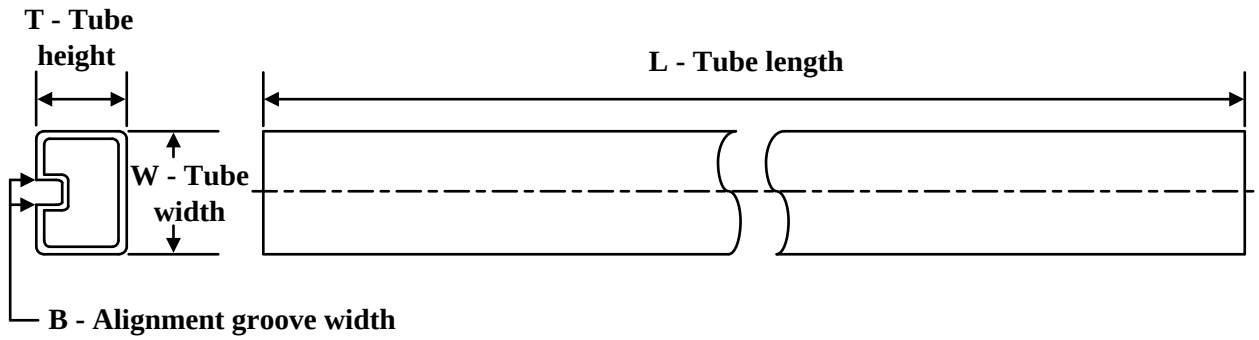
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHCT244DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT244DGVR | TVSOP | DGV | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT244DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT244NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT244PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT244PWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

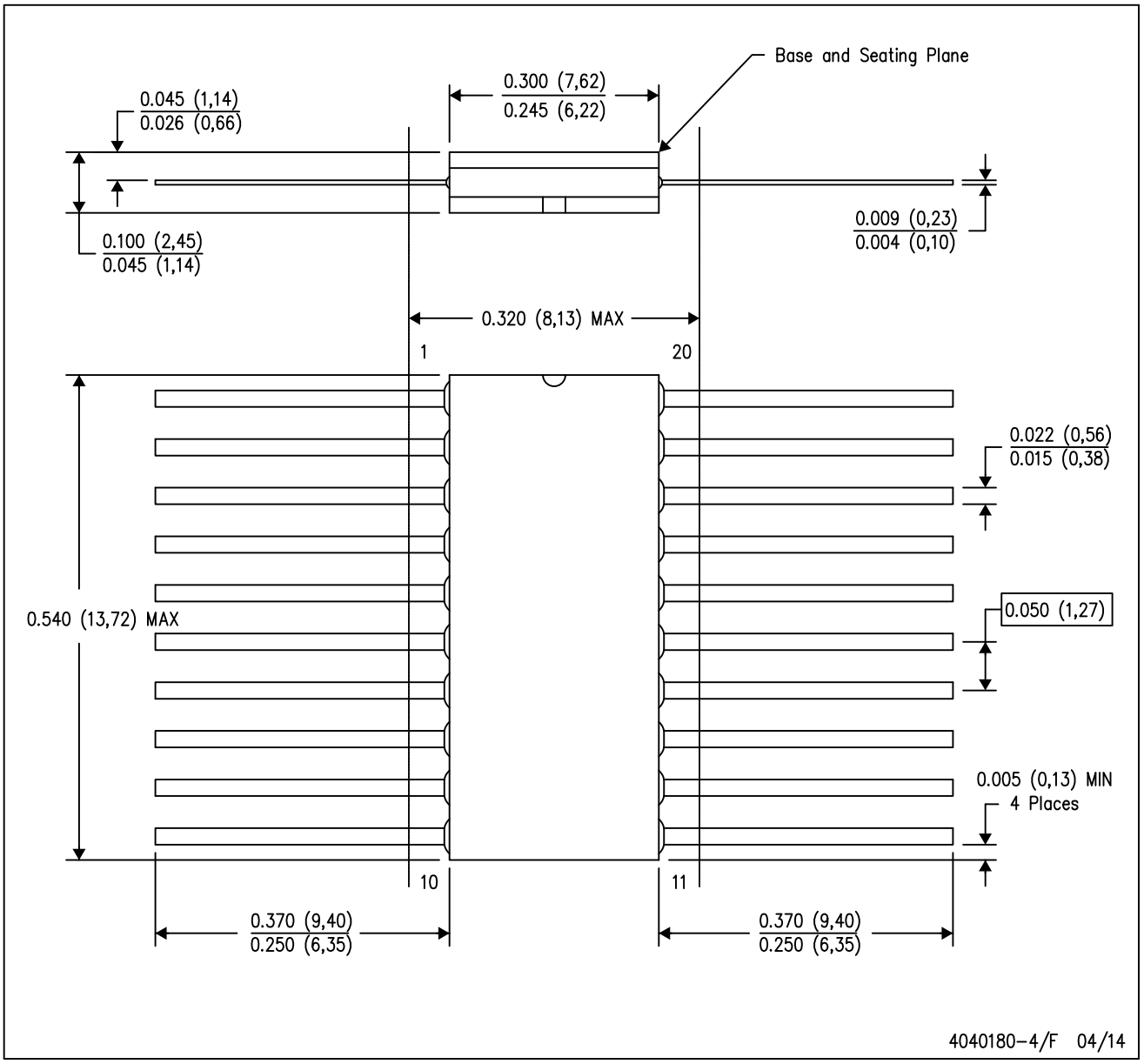
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9678301Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9678301QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHCT244N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHCT244FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHCT244W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



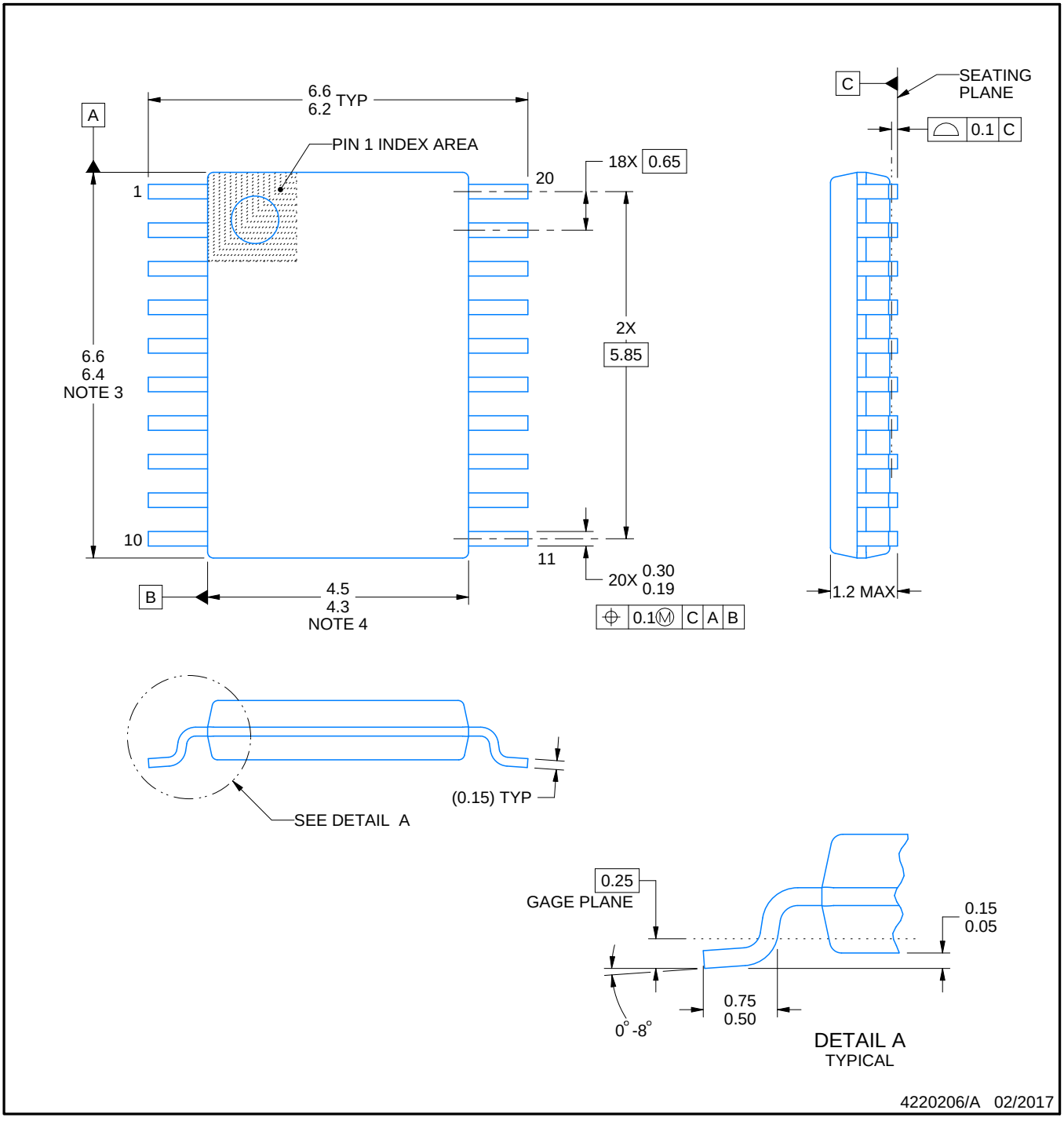

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

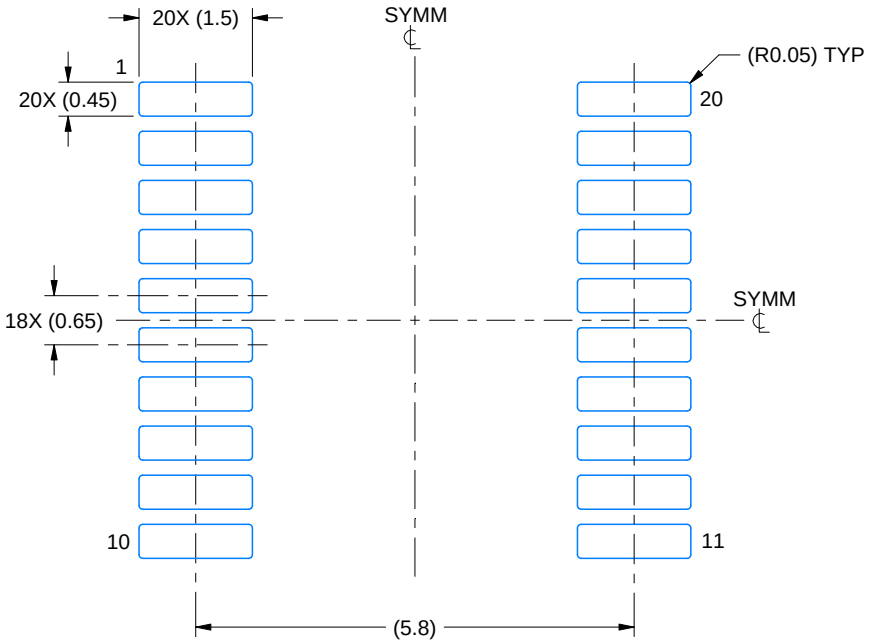
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



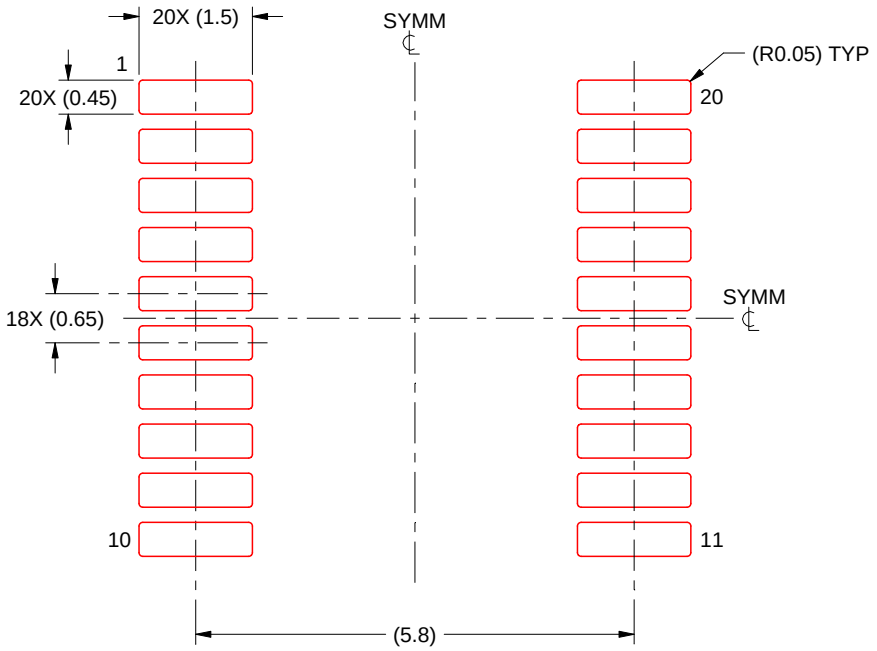

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



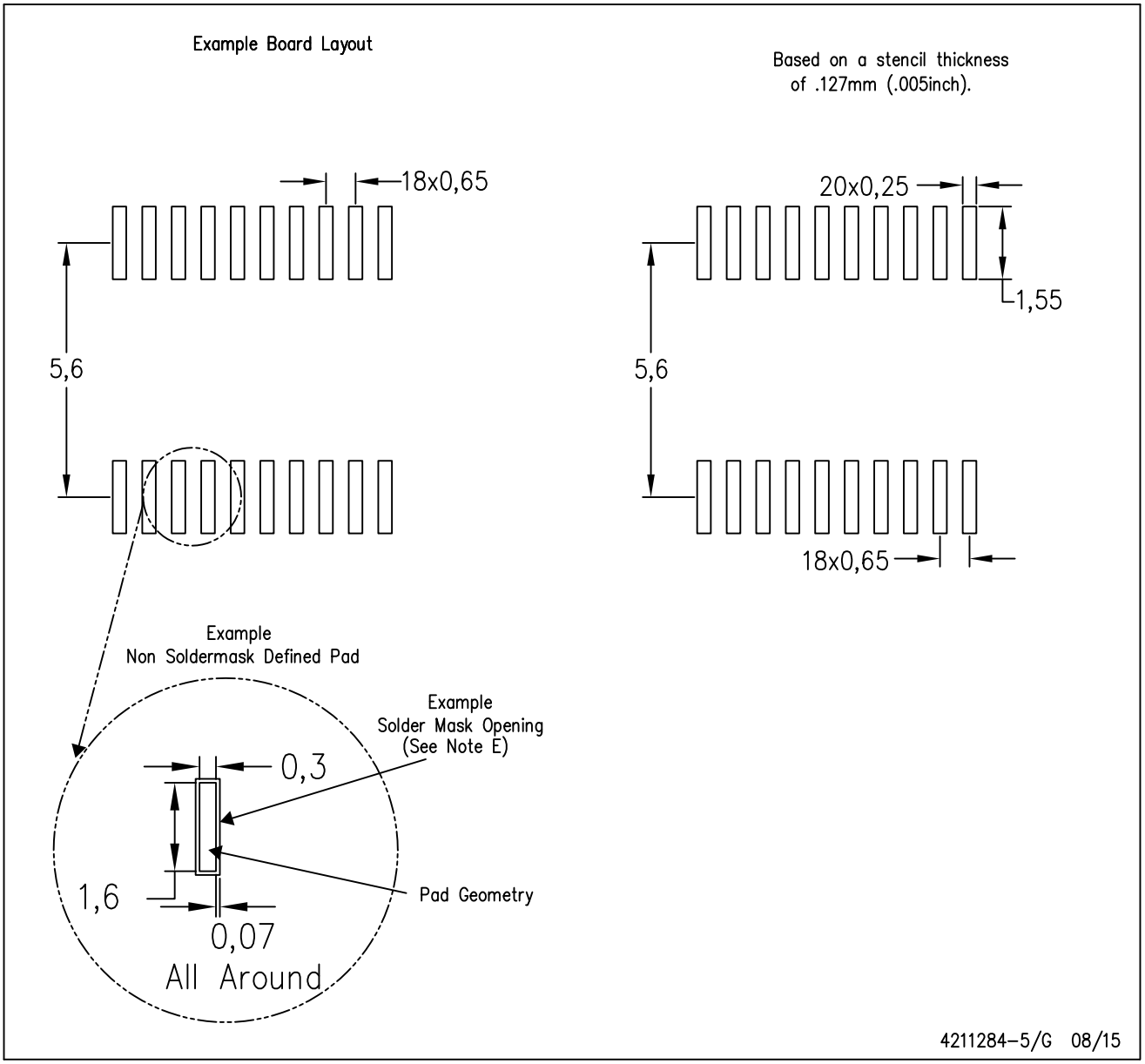

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



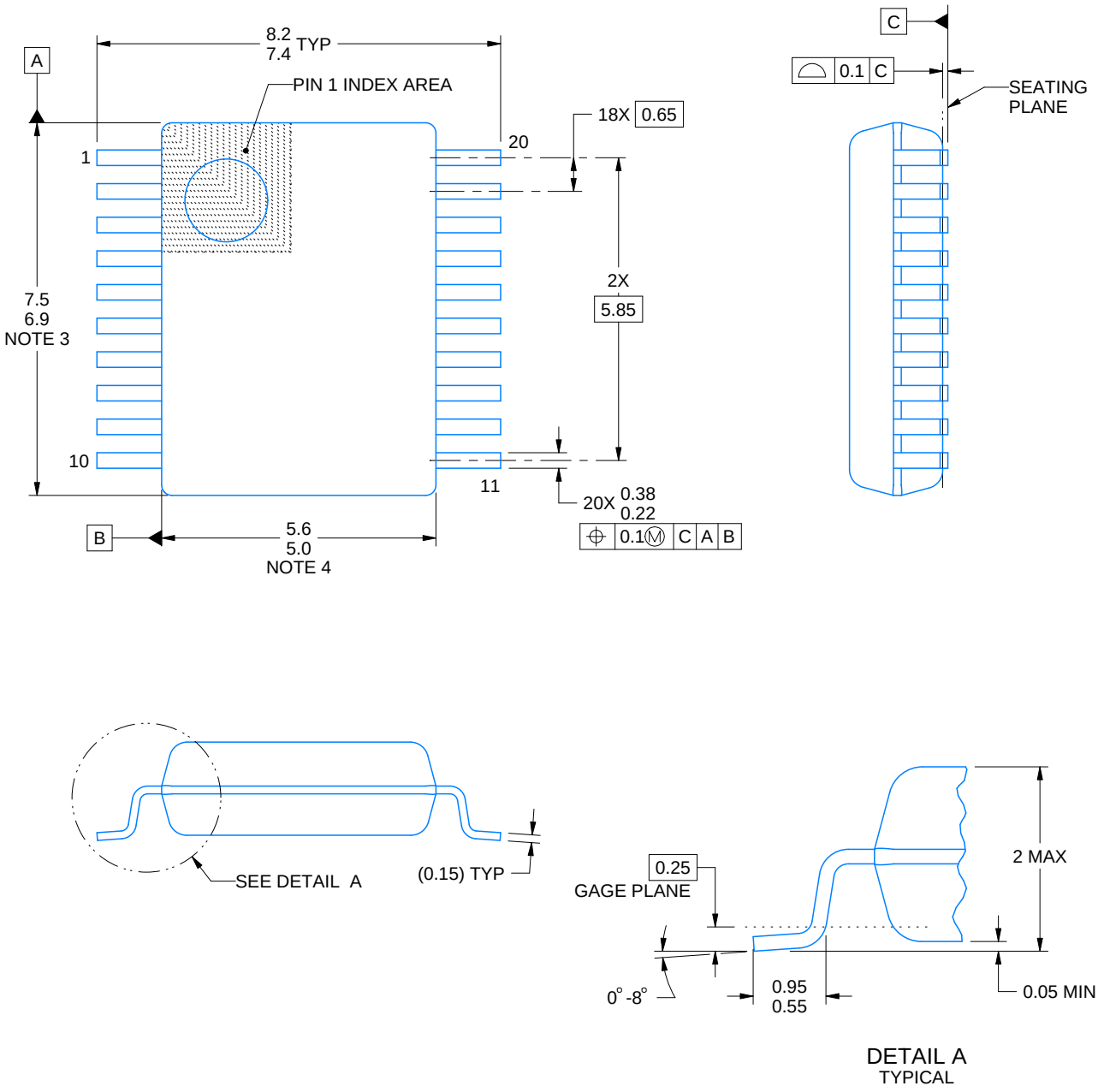

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

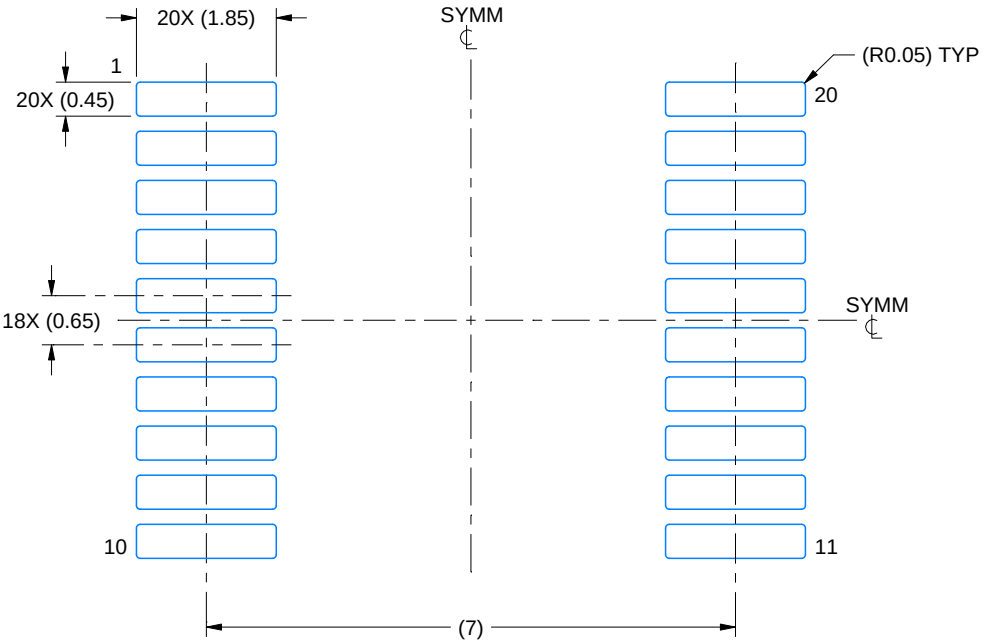
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

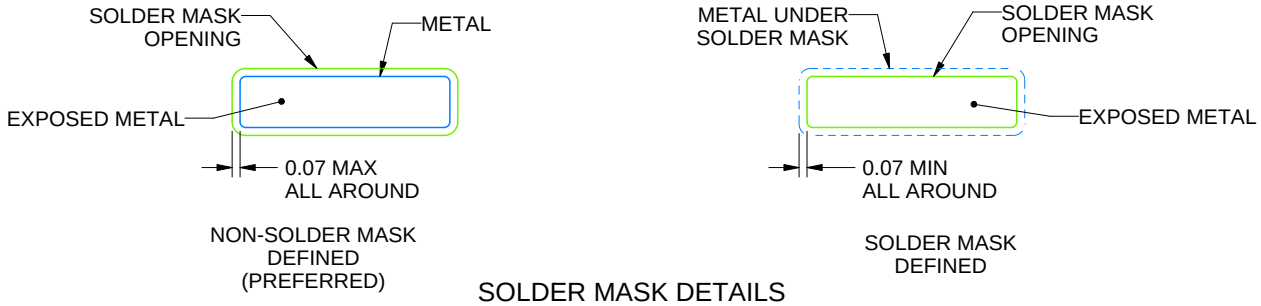
## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

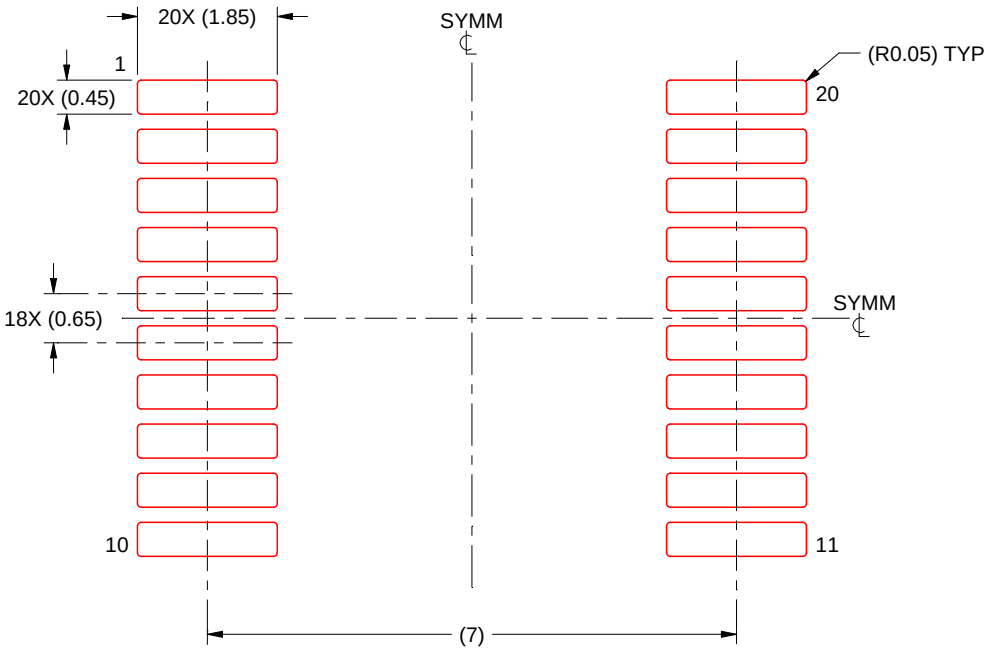
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

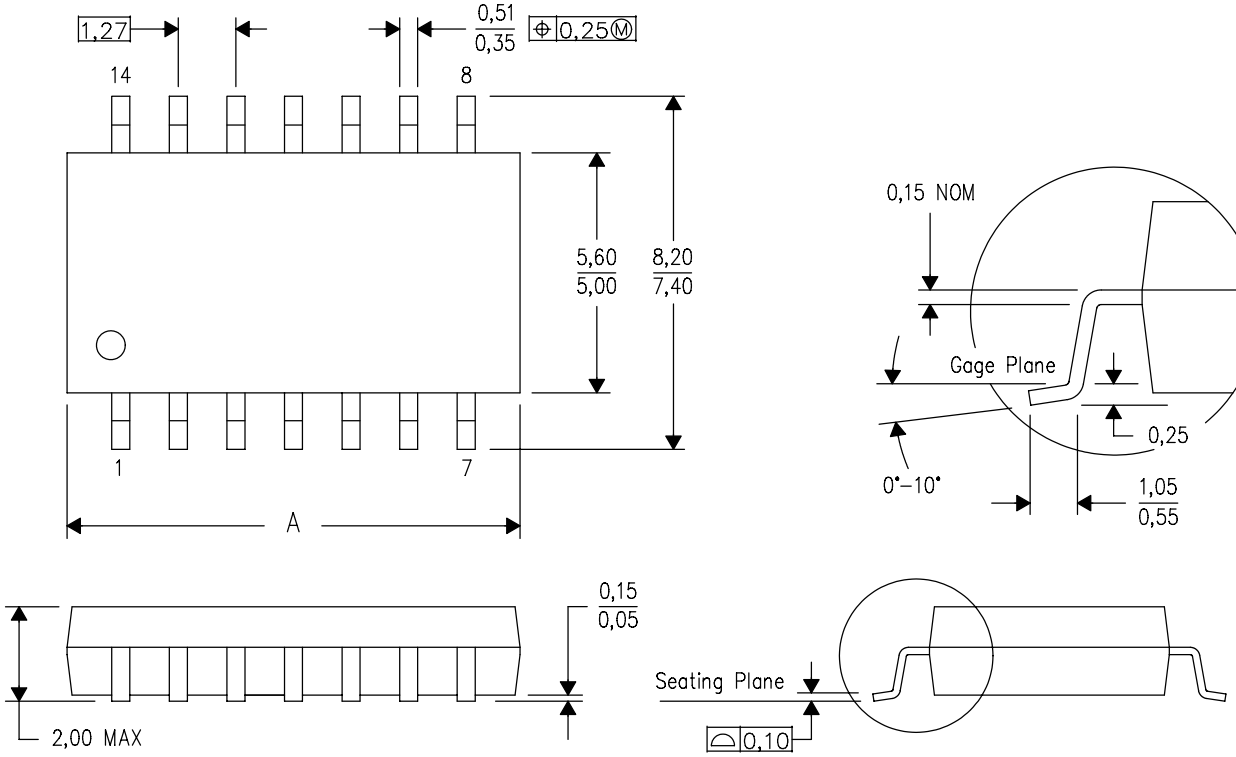
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

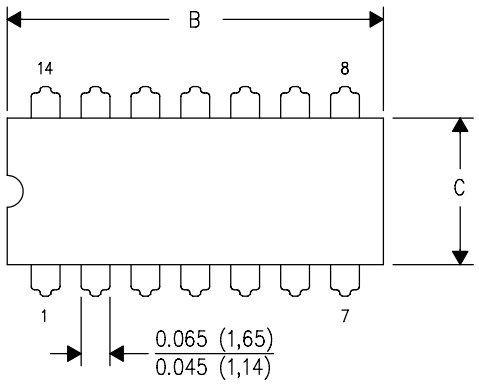
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

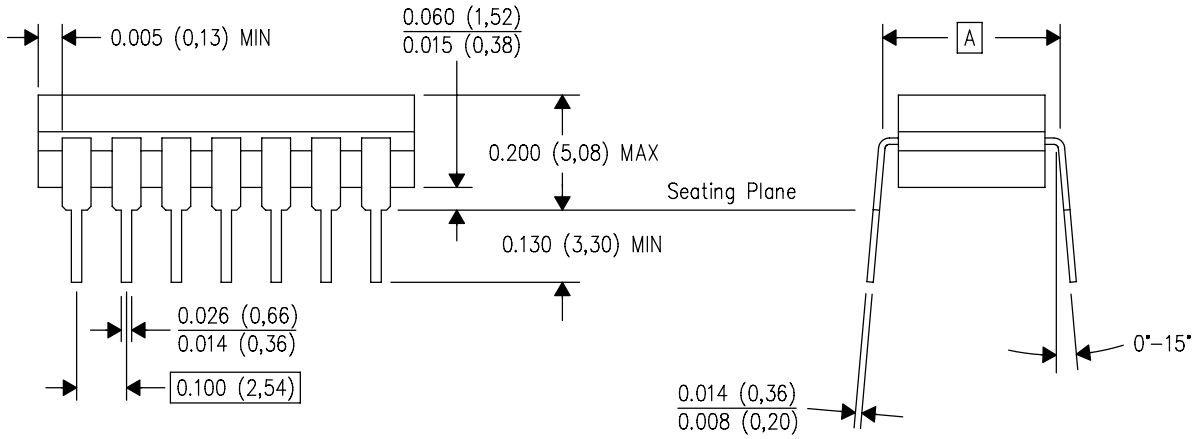
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

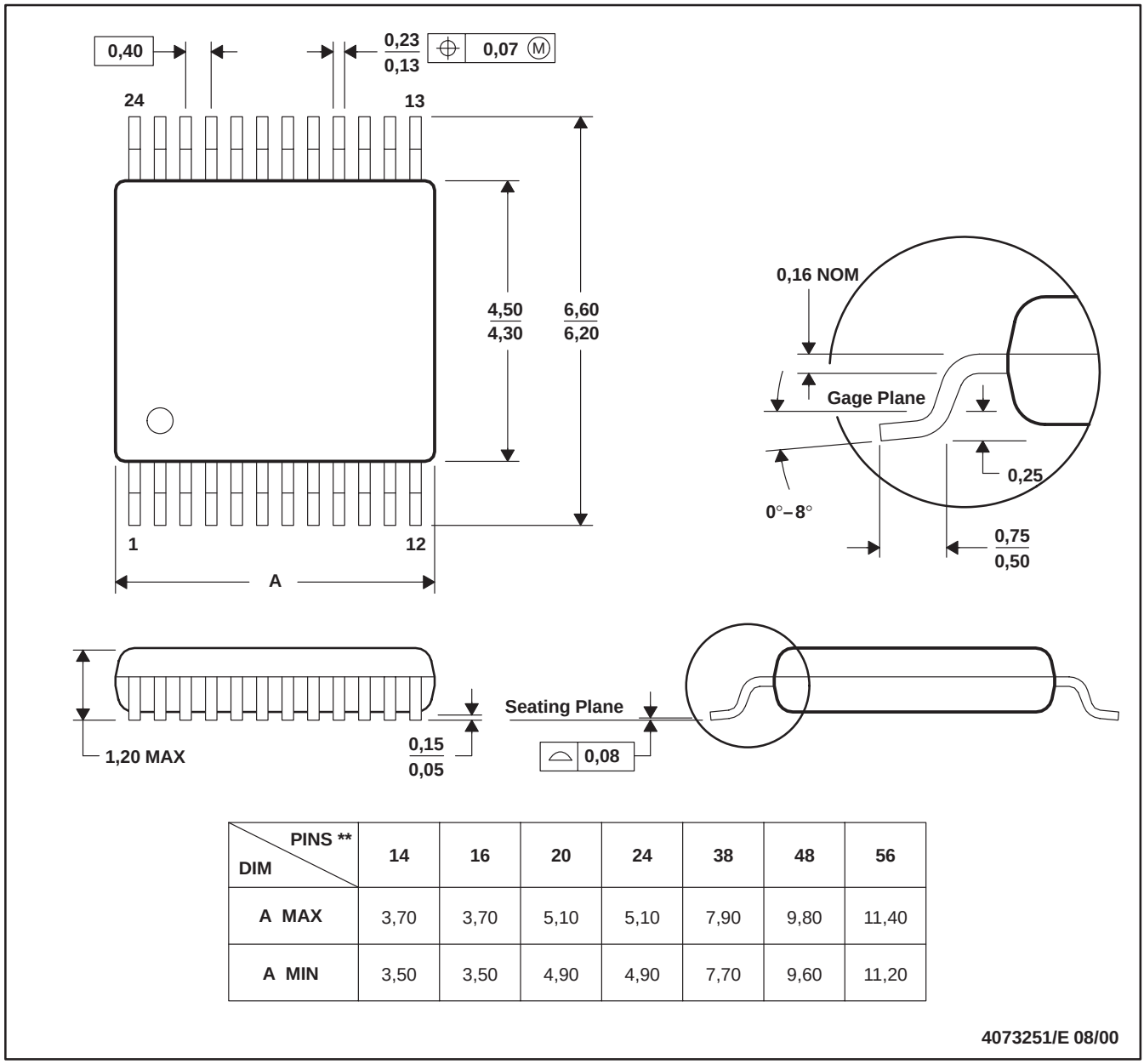



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

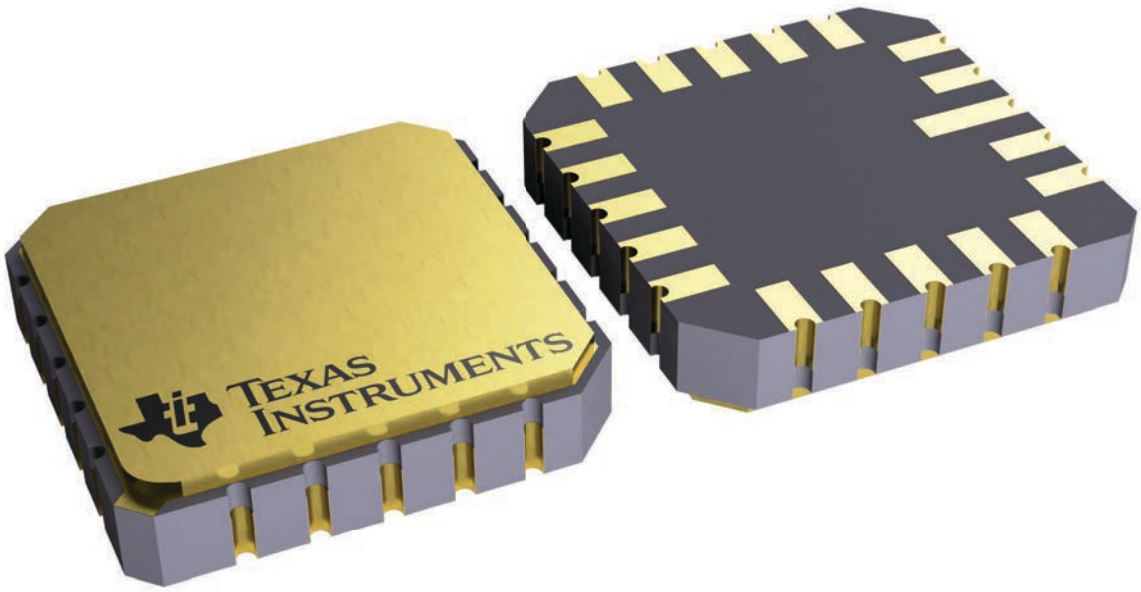
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

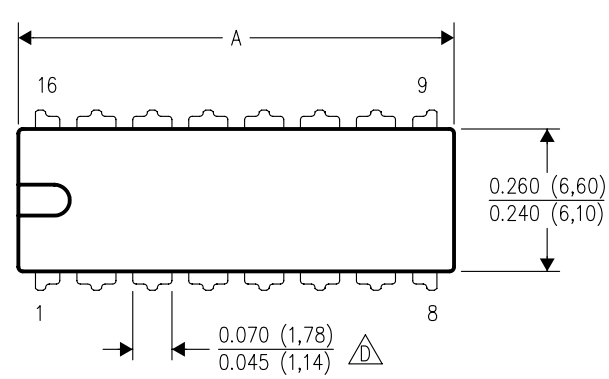



4229370VA\

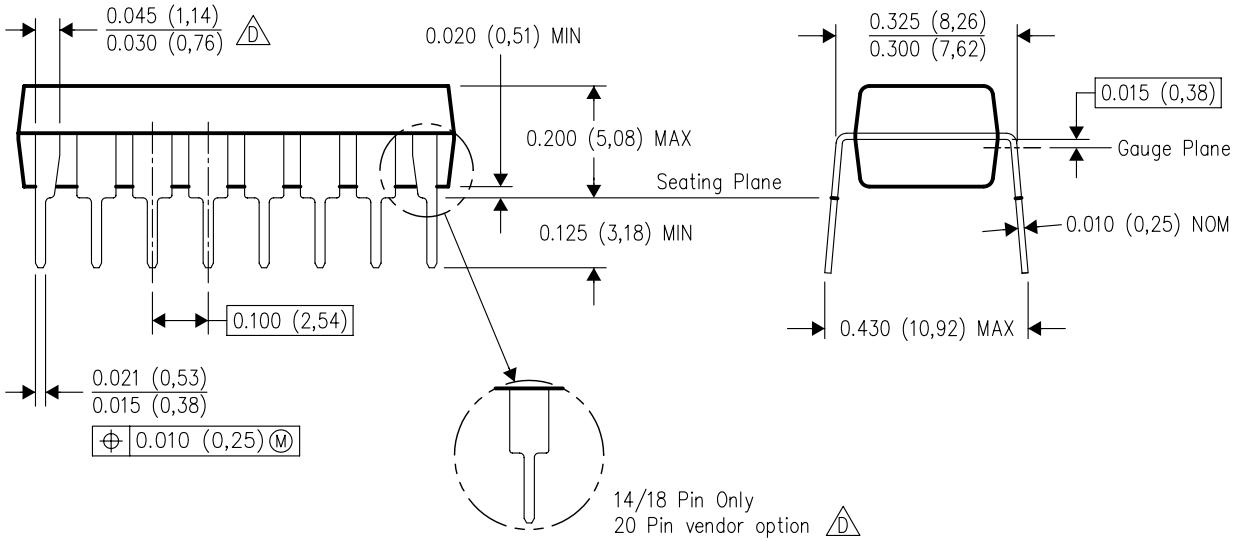
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

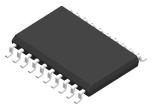



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

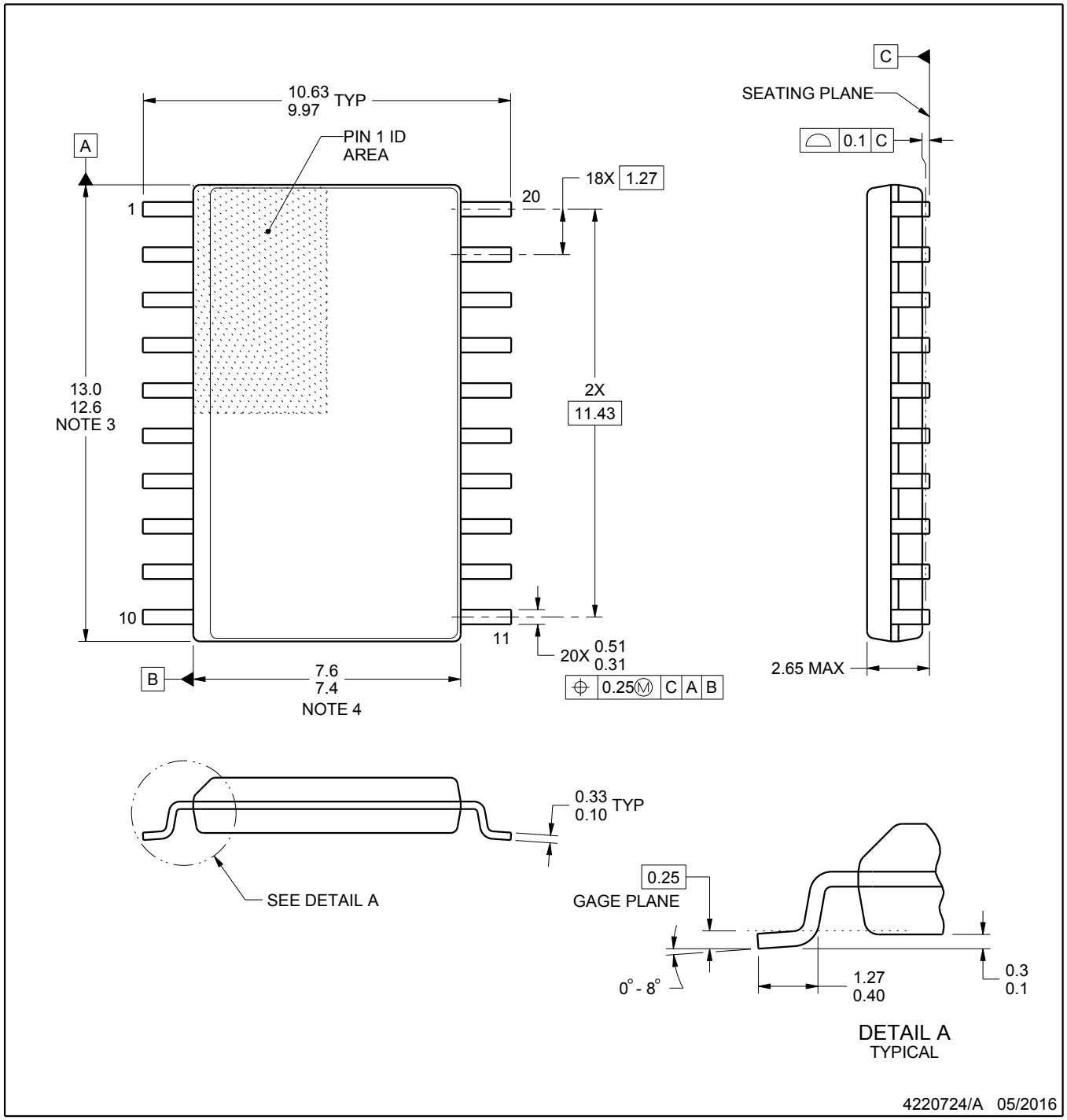


# PACKAGE OUTLINE

## DW0020A

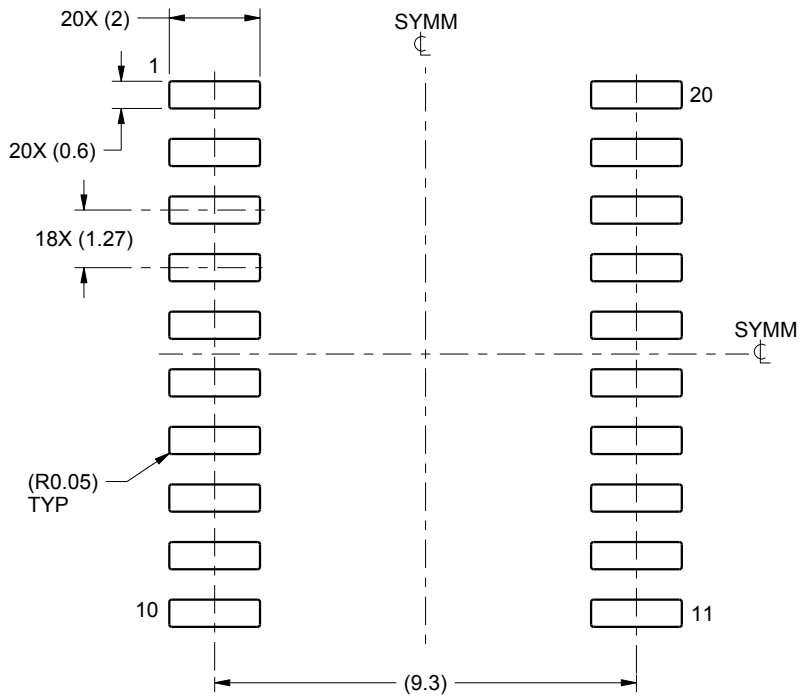
## SOIC - 2.65 mm max height

SOIC

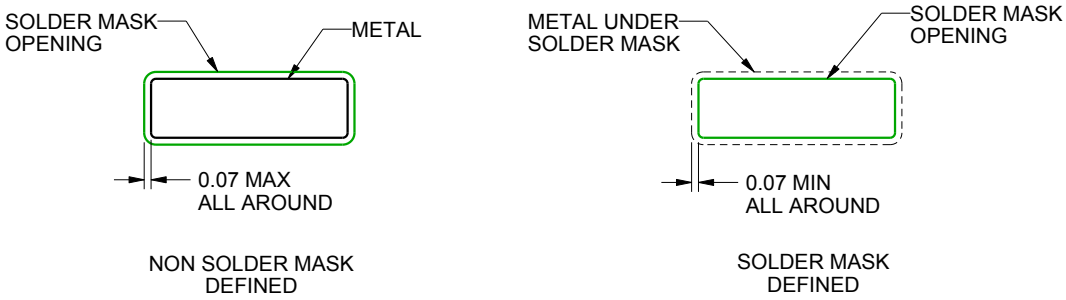



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

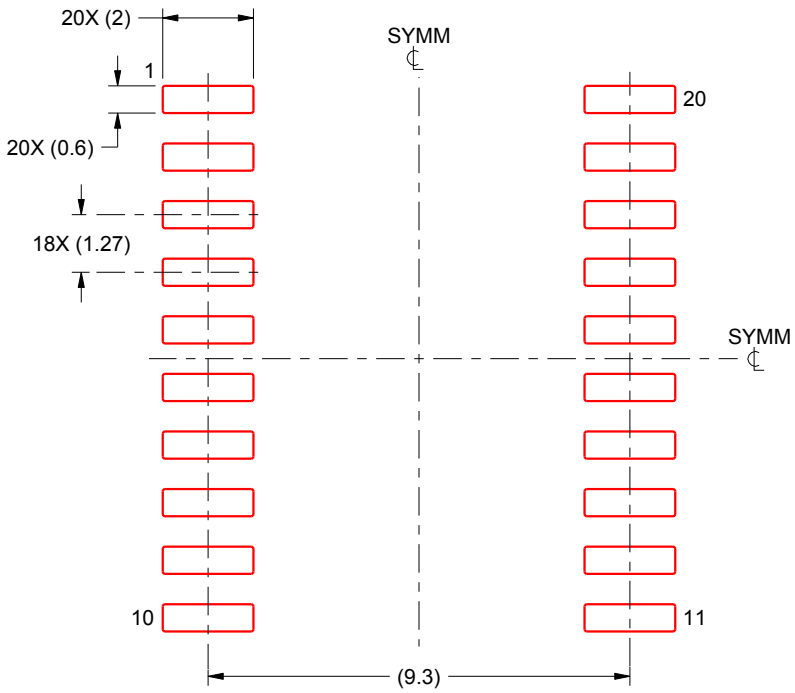



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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>>TI(德州仪器)