DDC264 64-Channel, Current-Input Analog-to-Digital Converter

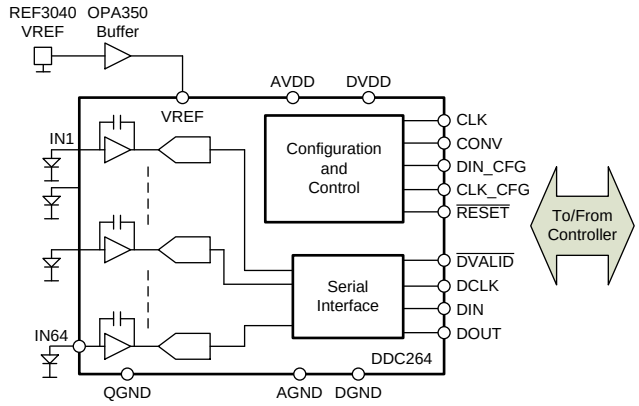
1 Features

- Single-Chip Solution to Directly Measure 64 Low-Level Currents
- Proven High-Precision, True Integrating Architecture With 100% Charge Collection
- Easy Upgrade for Existing DDC Family Applications
- Very Low Power: 3 mW/channel
- Extremely Linear:
  INL = ±0.025% of Reading ±1 ppm of FSR
- Low Noise: 6.3 ppm of FSR
- Adjustable Full-Scale Range
- Adjustable Speed
  - Data Rates up to 6 kSPS With 20-bit Performance
  - Integration Times as low as 160 µs
- Daisy-Chainable Serial Interface
- In-Package Bypass Capacitors Simplify PCB Design

2 Applications

- CT Scanner DAS
- Photodiode Sensors
- X-Ray Detection Systems

Simplified Schematic



3 Description

The DDC264 is a 20-bit, 64-channel, current-input analog-to-digital (A/D) converter. It combines both current-to-voltage and A/D conversion so that 64 separate low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized.

For each of the 64 inputs, the DDC264 uses the proven dual switched integrator front-end. This configuration allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. This architecture provides both a very stable offset and a loss-less collection of the input current. Adjustable integration times range from 160 µs to 1 s, allowing currents from fAs to µAs to be continuously measured with outstanding precision.

The DDC264 has a serial interface designed for daisy-chaining in multi-device systems. Simply connect the output of one device to the input of the next to create the chain. Common clocking feeds all the devices in the chain so that the digital overhead in a multi-DDC264 system is minimal.

The DDC264 uses a 5-V analog supply and a 2.7-V to 3.6-V digital supply. Bypass capacitors within the DDC264 package help minimize the external component requirements. Operating over the temperature range of 0°C to 70°C, the DDC264 100-pin NFBGA package is offered in two versions: the DDC264C for low-power applications, and the DDC264CK when higher speeds are required.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DDC264	NFBGA (100)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2011) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved AVDD and DVDD rows to *Recommended Operating Conditions* table ... 6
- Moved Dynamic Characteristics rows to *Recommended Operating Conditions* table ... 6
- Deleted Voltage row from *Electrical Characteristics* table ... 6
- Changed 1.65 mA to 825 µA in *Voltage Reference* section ... 16
- Changed 680 µA to 340 µA in *Voltage Reference* section ... 16
- Changed 64 to 128 in the formula in *Reading the Measurement* section ... 27
- Changed high-impedance to low-impedance in *Shielding Analog Signal Paths* section ... 30

Changes from Revision B (January, 2011) to Revision C — **Page**

- Updated *NOISE vs* C_{SENSOR} table; revised values for Range 0 performance in fC and Electrons ... 7

Changes from Revision A (January, 2011) to Revision B — **Page**

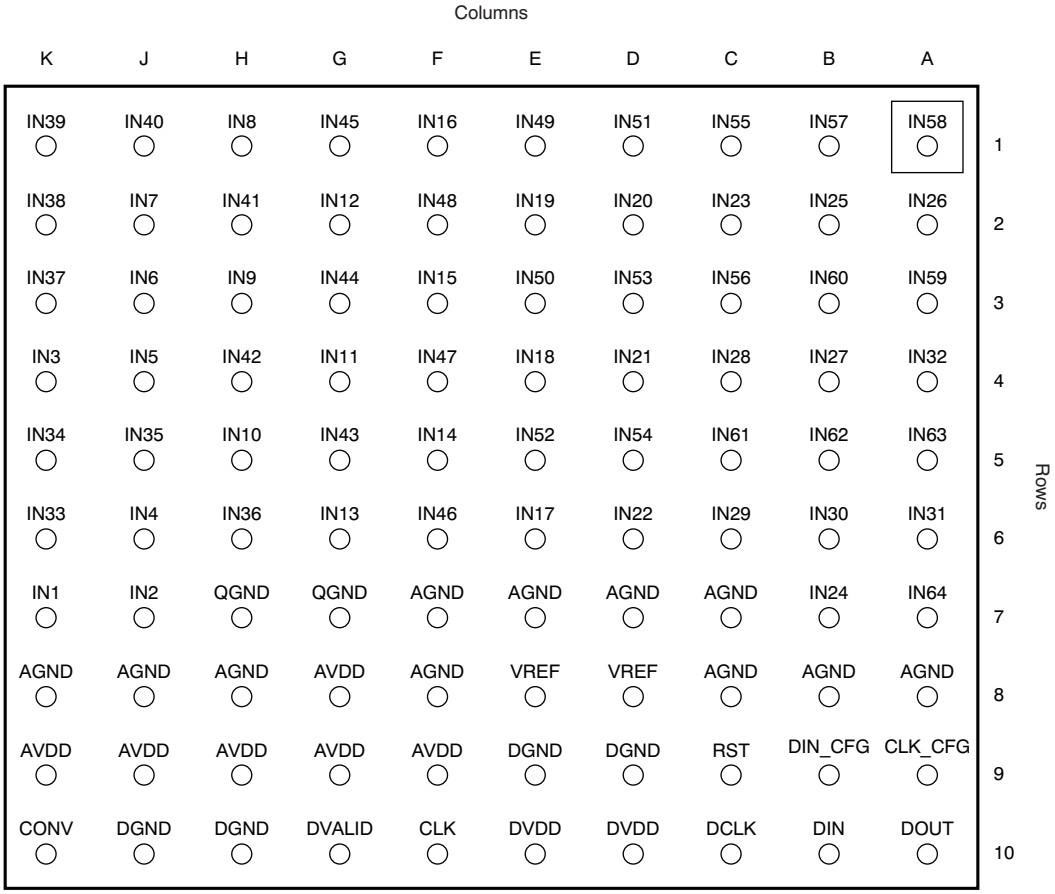
- Changed second paragraph of *Basic Integration Cycle* section to correct CONV timing description error ... 13

5 Device Comparison Table

PRODUCT	NO. OF CHANNELS	FULL-SCALE	MAXIMUM DATA RATE	POWER/CHANNEL AT MAX DATA RATE	PACKAGE-PIN
DDC112	2	1000 pC	2 KSPS	80 mW	SO-28, TQFP-32
DDC112K	2	1000 pC	3 KSPS	85 mW	SO-28, TQFP-32
DDC114	4	350 pC	3.1 KSPS	18 mW	QFN-48
DDC118	8	350 pC	3.1 KSPS	18 mW	QFN-48
DDC316	16	12 pC	100 KSPS	28 mW	BGA-64
DDC232C	32	350 pC	3.1 KSPS	7 mW	BGA-64
DDC232CK	32	350 pC	6.2 KSPS	10 mW	BGA-64
DDC264C	64	150 pC	3.1 KSPS	3 mW	BGA-100
DDC264CK	64	150 pC	6.2 KSPS	5.5 mW	BGA-100
DDC1128	128	150 pC	6.2 KSPS	5.5 mW	BGA-192
DD2256A	256	150 pC	17 KSPS	2.2 mW	BGA-323

6 Pin Configuration and Functions

ZAW Package
100-Pin NFBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	A8, B8, C7, C8, D7, E7, F7, F8, H8, J8. K8	Analog	Analog ground
AVDD	F9, G8, G9, H9, J9, K9	Analog	Analog power supply, 5-V nominal
CLK	F10	Digital input	Master clock input
CLK_CFG	A9	Digital input	Configuration register clock input
CONV	K10	Digital input	Conversion control input: 0 = integrate on side B; 1 = integrate on side A
DCLK	C10	Digital input	Serial data clock input
DGND	D9, E9, H10, J10	Digital	Digital ground
DIN	B10	Digital input	Serial data input
DIN_CFG	B9	Digital input	Configuration register data input
DOUT	A10	Digital output	Serial data output
$\overline{\text{DVALID}}$	G10	Digital output	Data valid output, active low
DVDD	D10, E10	Digital	Digital power supply, 3.3-V nominal
IN1-IN64	Rows 1-6, A7, B7, J7, K7	Analog input	Analog inputs for channels 1 to 64
QGND	G7, H7	Analog	Quiet analog ground; see the guidelines described in *Layout*
$\overline{\text{RESET}}$	C9	Digital input	Digital reset, active low
VREF	D8, E8	Analog input	External voltage reference input, 4.096-V nominal

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
AVDD to AGND	–0.3	6	V
DVDD to DGND	–0.3	3.6	V
AGND to DGND		±0.2	V
VREF input to AGND	2	AVDD + 0.3	V
Analog input to AGND	–0.3	0.7	V
Digital input voltage to DGND	–0.3	0.3	V
Digital output voltage to DGND	–0.3	0.3	V
Operating temperature	0	70	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{REF}	Reference voltage			4	4.096	4.2	V
POWER-SUPPLY REQUIREMENTS							
	Analog power supply voltage (AVDD)		DDC264C	4.75	5	5.25	V
			DDC264CK	4.9	5	5.1	
	Digital power supply voltage (DVDD)			2.7	3.3	3.6	V
DYNAMIC CHARACTERISTICS							
	Data rate		DDC264C		3	3.125	kSPS
			DDC264CK		6	6.25	
t_{INT}	Integration time		DDC264C	320	333	1,000,000	µs
			DDC264CK	160	166	1,000,000	
	System clock	Clkdiv = 0	DDC264C	1		5	MHz
			DDC264CK	1		10	
		Clkdiv = 1	DDC264C	4		20	MHz
			DDC264CK	4		40	
	Data clock (DCLK)					32	MHz
	Configuration clock (CLK_CFG)					20	MHz

7.4 Thermal Information

THERMAL METRIC[1]		DDC264C, DDC264CK ZAW (NFBGA) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, VREF = 4.096 V, t_{INT} = 333 µs for DDC264C or 166 µs for DDC264CK, and range = 3 (150 pC) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Range 0		10.5	12.5	14.5	pC
Range 1		47.5	50	52.5	pC
Range 2		95	100	105	pC
Range 3		142.5	150	157.5	pC
Negative full-scale range		–0.4% of Positive full-scale range			pC
ACCURACY					
Noise, low-level input[1]	Range = 3, C_{SENSOR}[2] = 35 pF		6.3		ppm of FSR[3], rms
Integral linearity error[4]			±0.025% Reading ±1-ppm FSR	±0.05% Reading ±1.5-ppm FSR	
Resolution	No missing codes, format = 1	20			Bits
	No missing codes, format = 0	16			
Input bias current	T_A = 25°C to 45°C		±0.5	±5	pA
Range error match[5]			0.1%	0.5%	FSR
Range sensitivity to VREF	VREF = 4.096 ±0.1 V		1:1		
Offset error			±500	±1000	ppm of FSR
Offset error match[5]			±150		ppm of FSR
DC bias voltage[6]	Low-level input (< 1% FSR)		±0.1	±1	mV
Power-supply rejection ratio	At DC		100	±300	ppm of FSR/V
PERFORMANCE OVER TEMPERATURE					
Offset drift			±0.5	5[7]	ppm of FSR/°C
Offset drift stability			±0.2	2[7]	ppm of FSR/minute
DC bias voltage drift[6]			±3		µV/°C
Input bias current drift	T_A = 25°C to 45°C		0.01	1[7]	pA/°C
Range drift[8]			25	50	ppm/°C
Range drift match[5]			±5		ppm/°C
REFERENCE					
Input current[9]	Average value with t_{INT} = 333 µs		825		µA
	Average value with t_{INT} = 166 µs (DDC264CK)		1650		µA

(1) Input is less than 1% of full-scale.
(2) C_{SENSOR} is the capacitance seen at the DDC264 inputs from wiring, photodiode, etc.
(3) FSR is full-scale range.
(4) A best-fit line is used in measuring nonlinearity.
(5) Matching between side A and side B of the same input.
(6) Voltage produced by the DDC264 at its input that is applied to the sensor.
(7) Ensured by design; not production tested.
(8) Range drift does not include external reference drift.
(9) Input reference current decreases with increasing t_{INT} (see *Voltage Reference*).

Electrical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, VREF = 4.096 V, t_{INT} = 333 µs for DDC264C or 166 µs for DDC264CK, and range = 3 (150 pC) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT AND OUTPUT						
V_{IH}			0.8 × DVDD		DVDD + 0.1	V
V_{IL}			–0.1		0.2 × DVDD	V
V_{OH}		I_{OH} = –500 µA	DVDD – 0.4			V
V_{OL}		I_{OL} = 500 µA			0.4	V
I_{IN}	Input current	0 < V_{IN} < DVDD			±10	µA
	Data format(10)			Straight binary		
POWER-SUPPLY REQUIREMENTS						
	Analog current	DDC264C		34		mA
		DDC264CK		60		
	Digital current	DDC264C		7.5		mA
		DDC264CK		15		
	Total power dissipation	DDC264C		192	256	mW
		DDC264CK		350		
	Per channel power dissipation	DDC264C		3	4	mW/Channel
		DDC264CK		5.5		

(10) Data format is straight binary with a small offset. The number of bits in the output word is controlled by the format bit.

Table 1. NOISE vs C_{SENSOR}(1)

RANGE	C_{SENSOR}								
	0 pF	10 pF	30 pF	43 pF	57 pF	100 pF	270 pF	470 pF	1000 pF
ppm of FSR, rms									
Range 0: 12.5 pC	16	20	30	37	44	71	160	270	510
Range 1: 50 pC	6.4	7.4	10	12	14	21	45	74	130
Range 2: 100 pC	5.1	5.5	7.1	8	9.1	12	25	39	71
Range 3: 150 pC	4.8	5	6	6.5	7.2	9.6	17	27	49
fC, rms									
Range 0: 12.5 pC	0.2	0.25	0.38	0.46	0.55	0.89	2	3.38	6.38
Range 1: 50 pC	0.32	0.37	0.53	0.62	0.73	1.09	2.29	3.73	6.88
Range 2: 100 pC	0.51	0.55	0.71	0.8	0.91	1.28	2.5	3.97	7.16
Range 3: 150 pC	0.72	0.75	0.9	0.98	1.08	1.45	2.67	4.14	7.36
Electrons, rms									
Range 0: 12.5 pC	1250	1560	2340	2890	3430	5540	12480	21070	39790
Range 1: 50 pC	2010	2310	3340	3910	4570	6800	14200	23300	42900
Range 2: 100 pC	3220	3440	4450	5000	5680	7990	15600	24800	44700
Range 3: 150 pC	4530	4730	5610	6120	6770	9050	16700	25800	45900

(1) Noise in Table 1 is expressed in three different units for reader convenience. The first section lists noise in units of parts per million of full-scale range; the second section shows noise as an equivalent input charge (in fC); and the third section converts noise to electrons.

7.6 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

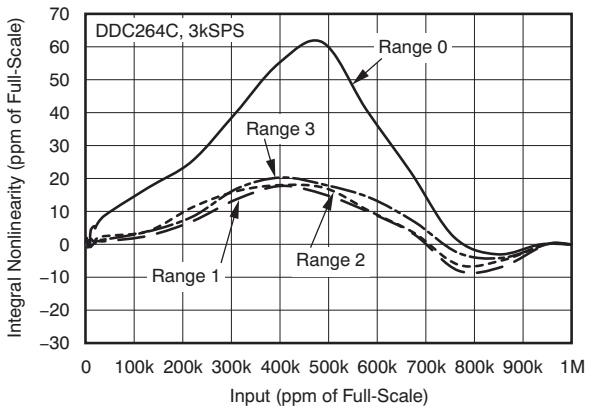


Figure 1. Integral Nonlinearity

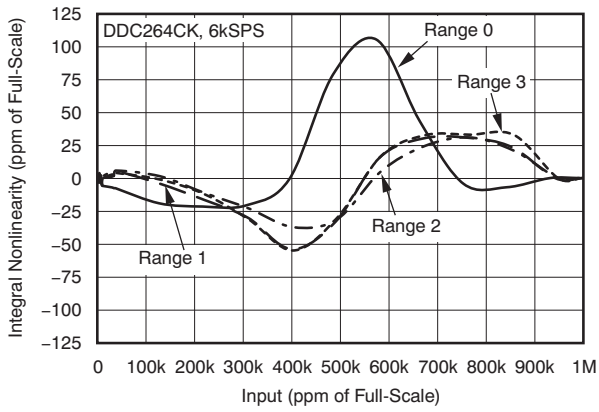


Figure 2. Integral Nonlinearity

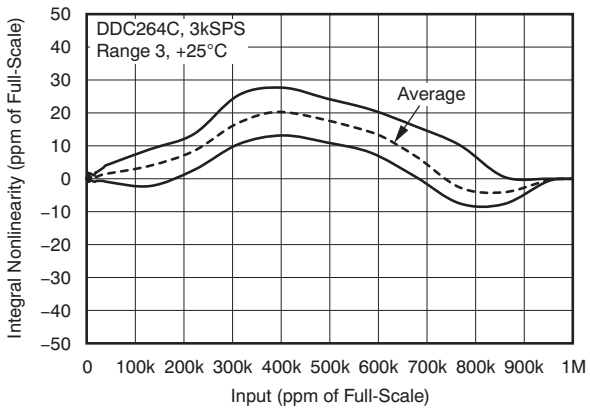


Figure 3. Integral Nonlinearity Envelope of All 64 Channels

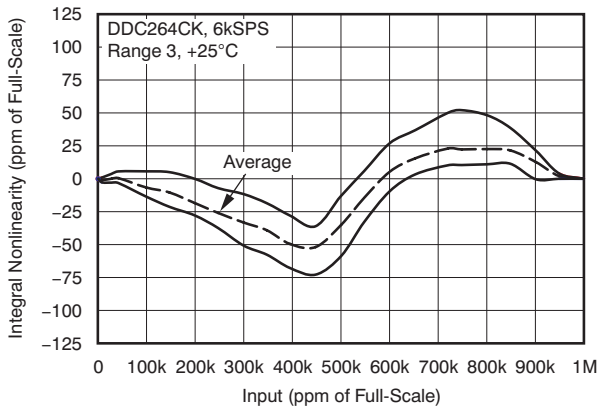


Figure 4. Integral Nonlinearity Envelope of All 64 Channels

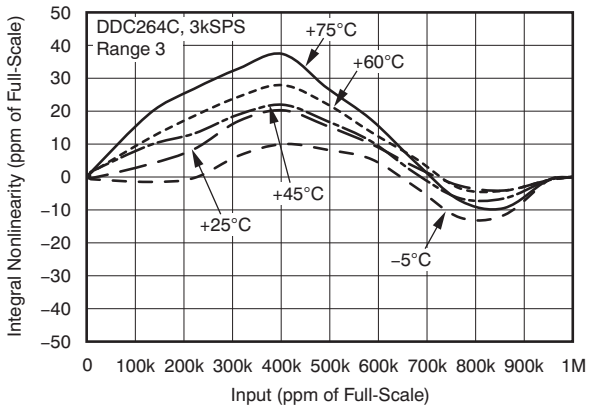


Figure 5. Integral Nonlinearity vs Temperature

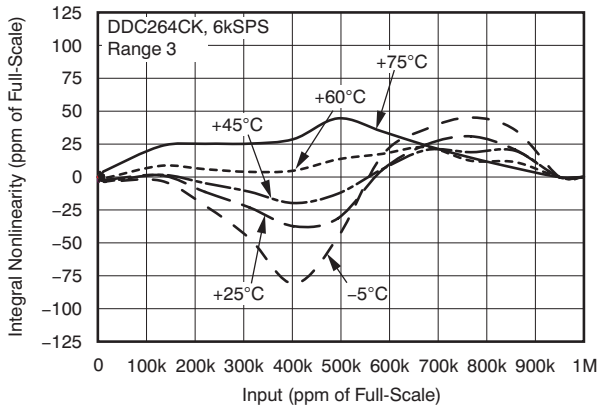


Figure 6. Integral Nonlinearity vs Temperature

Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

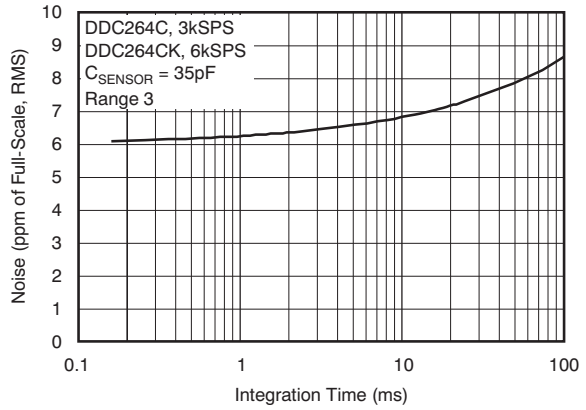


Figure 7. NOISE vs Integration Time

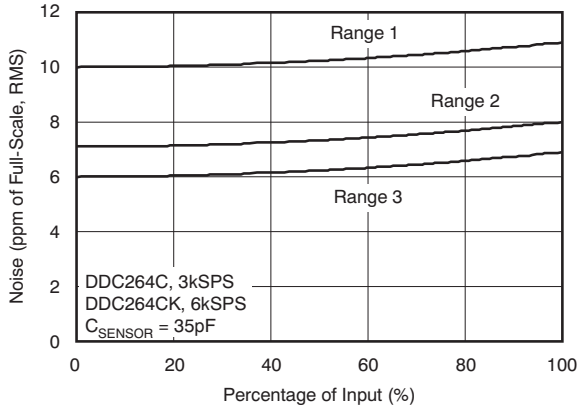


Figure 8. NOISE vs Input Level

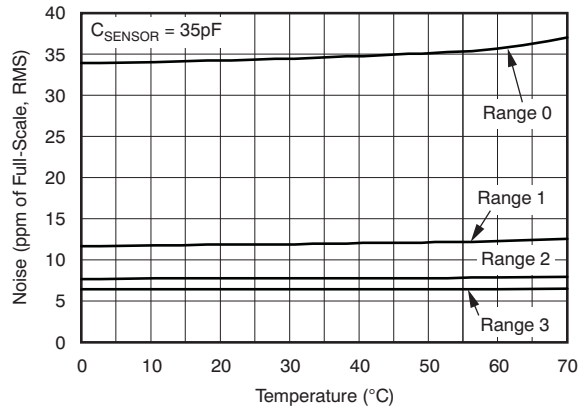


Figure 9. NOISE vs Temperature

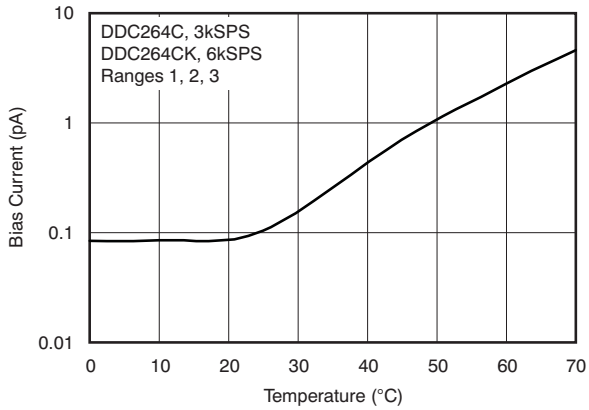


Figure 10. Input BIAS Current vs Temperature

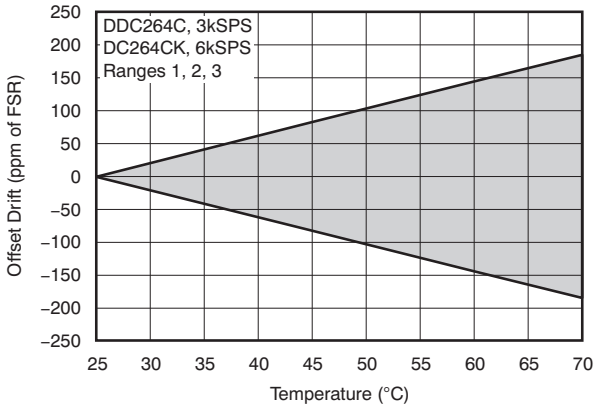


Figure 11. Offset Drift vs Temperature

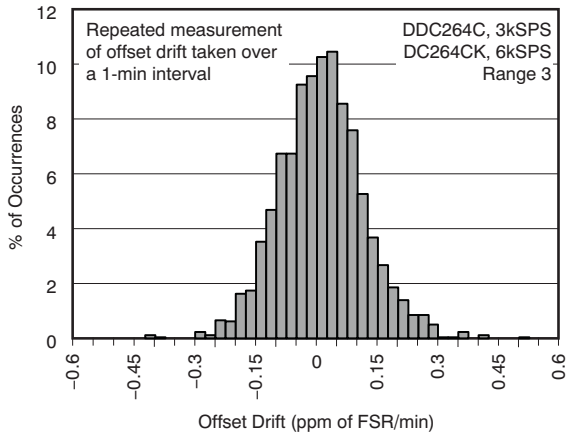


Figure 12. Offset Drift Stability Over Time Histogram

Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

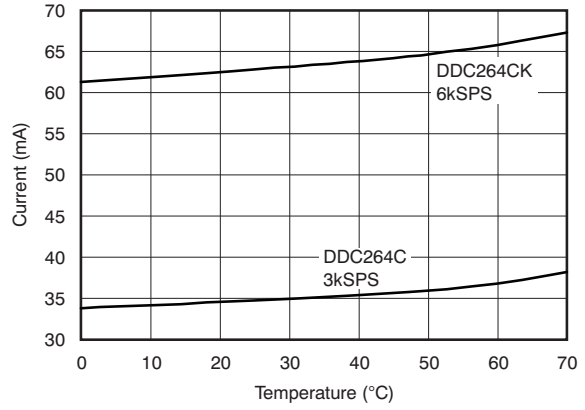


Figure 13. Analog Supply Current vs Temperature

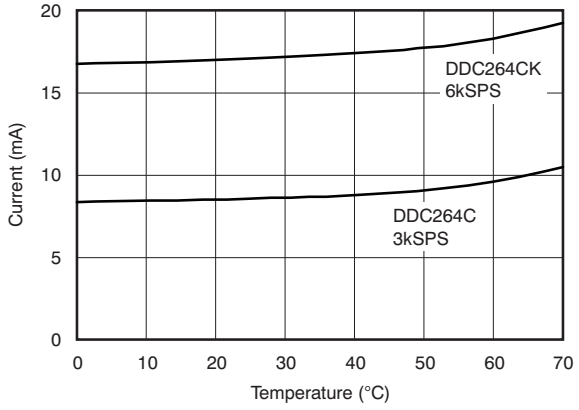


Figure 14. Digital Supply Current vs Temperature

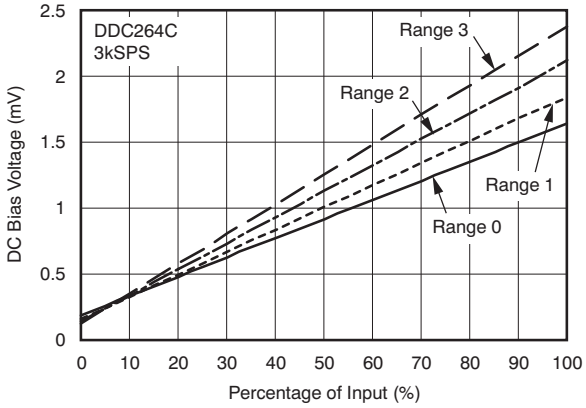


Figure 15. DC BIAS Voltage vs Input Percentage

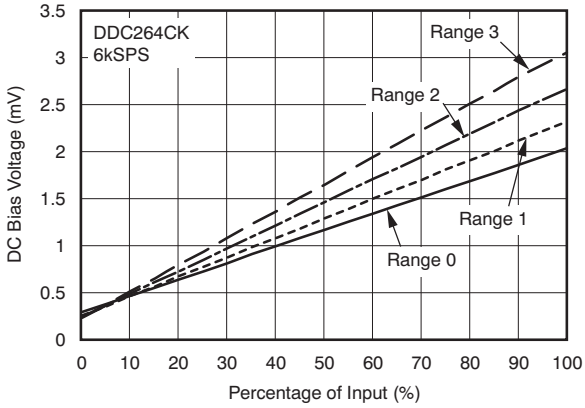


Figure 16. DC BIAS Voltage vs Input Percentage

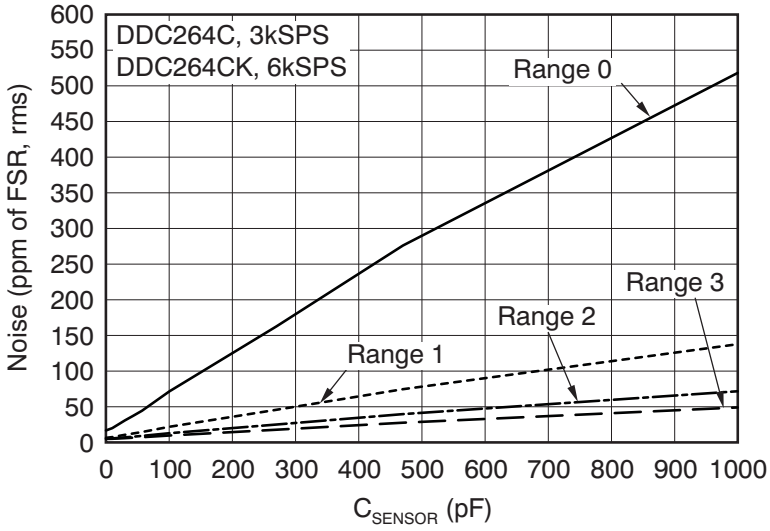


Figure 17. NOISE vs C_{SENSOR}

8 Detailed Description

8.1 Overview

The DDC264 contains 64 identical input channels (see *Functional Block Diagram*) that perform the function of current-to-voltage integration followed by a multiplexed A/D conversion. Each input has two integrators (see Figure 18) so that the current-to-voltage integration can be continuous in time. The DDC264 continuously integrates the input signal by switching integrations between side A and side B.

For example, while side A integrates the input signal, the side B outputs are digitized by the onboard ADC. This integration and A/D conversion process is controlled by the convert pin, CONV. The results from side A and side B of each signal input are stored in a serial output shift register. The DVALID output goes low when the shift register data are ready to be retrieved.

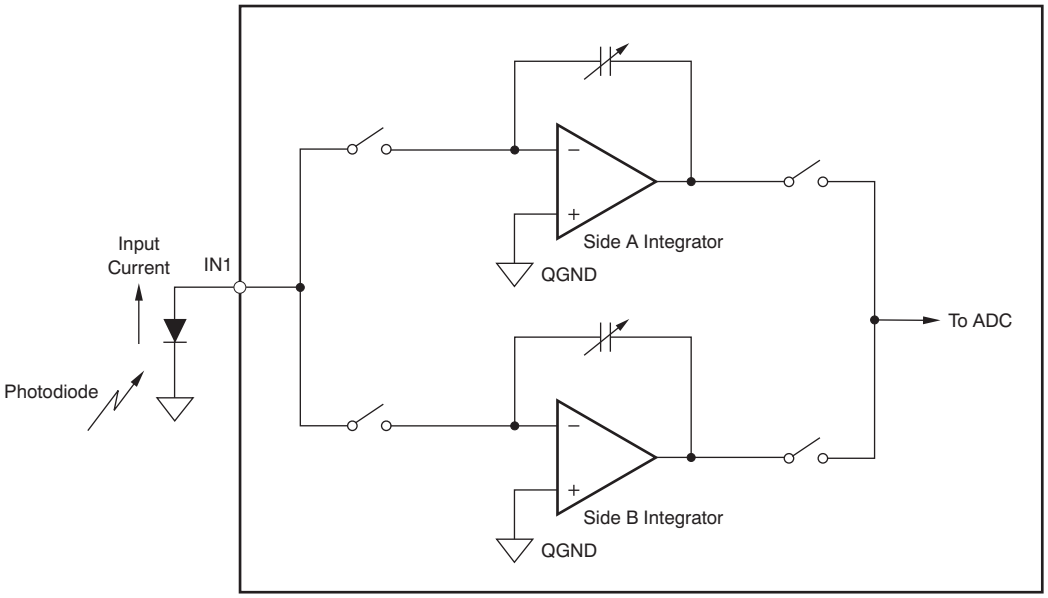


Figure 18. Dual Switched Integrator Architecture

Figure 19 shows a few integration cycles beginning after the device has been powered up, reset, and the Configuration Register has been programmed. The top signal is CONV and is supplied by the user. The *integration status* trace indicates which side is integrating. The output digital interface of the DDC264 sends the digital results through a synchronous serial interface that consists of a data clock (DCLK), a valid data pin (DVALID), a serial data output pin (DOUT), and a serial data input pin (DIN). As described above, DVALID goes active low when data are ready to be retrieved from the DDC264. It stays low until DCLK is taken high and then back low by the user. The text below the DVALID pulse indicates the side of the data available to be read. The arrow is used to match the data to the corresponding integration. Table 2 shows the timing specifications for Figure 19.

Overview (continued)

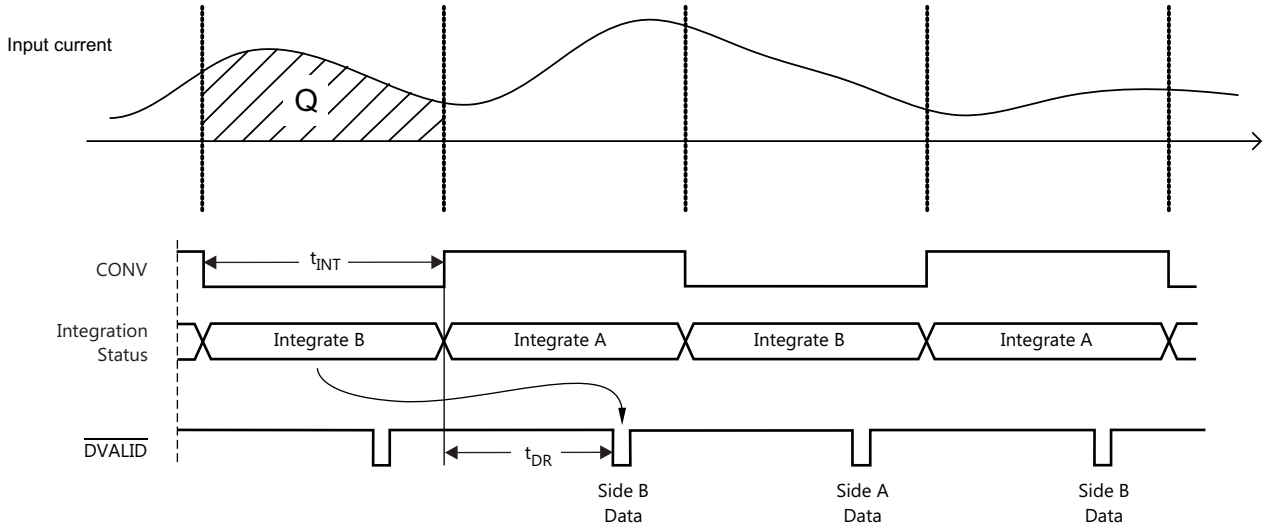


Figure 19. Integration Sequence Timing

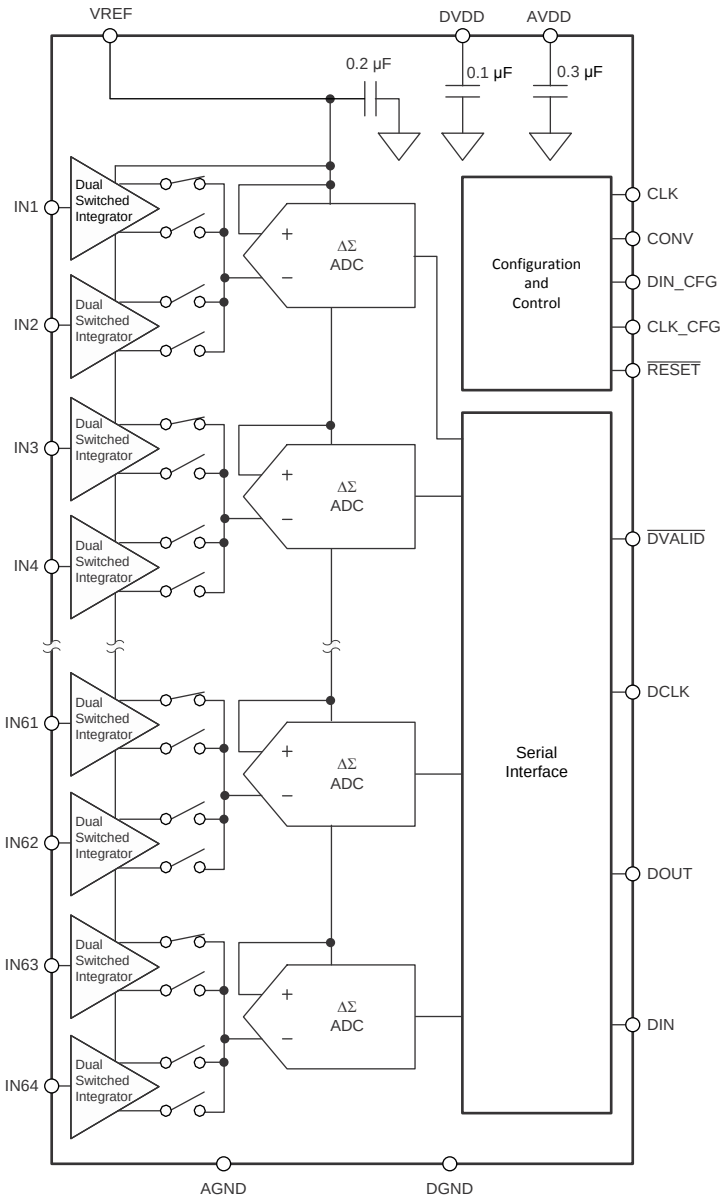
Table 2. Timing Requirements for Integration Sequence Timing

			MIN	TYP	MAX	UNIT
t_{INT}	Integration time	DDC264C(1)	320		1,000,000	µs
		DDC264CK(2)	160			
t_{DR}	Time until data ready	DDC264C(1)		276.4 ±0.4		µs
		DDC264CK(2)		138.2 ±0.2		

(1) Internal clock frequency = 5 MHz
(2) Internal clock frequency = 10 MHz

Finally, a second set of digital signals (DIN_CFG and CLK_CFG pins, see *Configuration Register — Read and Write Operations*) is used to configure the DDC264 by addressing a dedicated register.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dual Switched Integrator: Basic Integration Cycle

The topology of the front end of the DDC264 is an analog integrator as shown in Figure 20. In this diagram, only input IN1 is shown. The input stage consists of an operational amplifier, a selectable feedback capacitor network (C_F), and several switches that implement the integration cycle. The timing relationships of all of the switches shown in Figure 20 are illustrated in Figure 21. Figure 21 conceptualizes the operation of the integrator input stage of the DDC264 and must not be used as an exact timing tool for design.

Feature Description (continued)

See Figure 22 for the block diagrams of the reset, integrate, wait, and convert states of the integrator section of the DDC264. This internal switching network is controlled externally with the convert pin (CONV) and the system clock (CLK). For the best noise performance, CONV must be synchronized with the falling edge of CLK. TI recommends toggling CONV within ±10 ns of the falling edge of CLK.

The noninverting inputs of the integrators are connected to the QGND pin. Consequently, the DDC264 analog ground, QGND, must be as clean as possible. In Figure 20, the feedback capacitors (C_F) are shown in parallel between the inverting input and output of the operational amplifier. At the beginning of a conversion, the switches $S_{A/D}$, S_{INTA}, S_{INTB}, S_{REF1}, S_{REF2}, and S_{RESET} are set (see Figure 21).

At the completion of an A/D conversion, the charge on the integration capacitor (C_F) is reset with S_{REF1} and S_{RESET} (see Figure 21 and Figure 22a). This process is done during reset. In this manner, the selected capacitor is charged to the reference voltage, VREF. Once the integration capacitor is charged, S_{REF1} and S_{RESET} are switched so that VREF is no longer connected to the amplifier circuit while it waits to begin integrating (see Figure 22b). With the rising edge of CONV, S_{INTA} closes, which begins the integration of side A. This process puts the integrator stage into its integrate mode (see Figure 22c).

Charge from the input signal is collected on the integration capacitor, causing the voltage output of the amplifier to decrease. The falling edge of CONV stops the integration by switching the input signal from side A to side B (S_{INTA} and S_{INTB}). Prior to the falling edge of CONV, the signal on side B was converted by the A/D converter and reset during the time that side A was integrating. With the falling edge of CONV, side B starts integrating the input signal. At this point, the output voltage of the side A operational amplifier is presented to the input of the A/D converter (see Figure 22d).

A special elecrostatic discharge (ESD) structure protects the inputs but does not increase current leakage on the input pins.

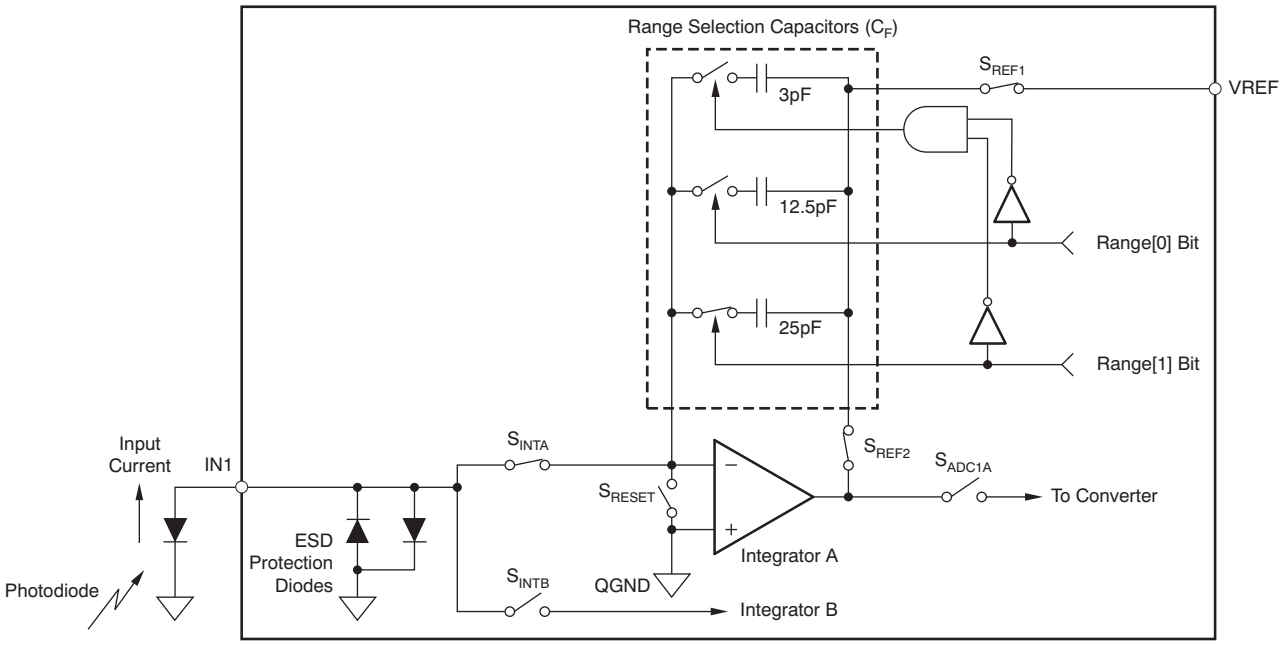


Figure 20. Basic Integration Configuration

Feature Description (continued)

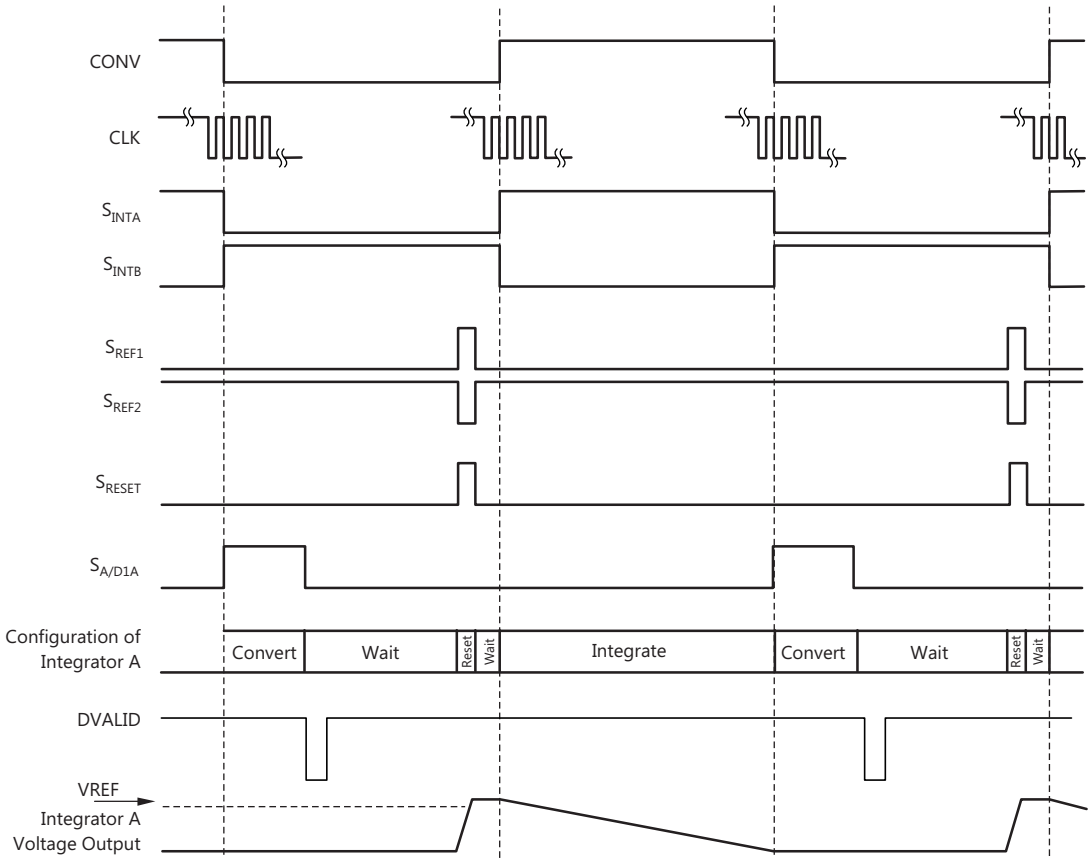
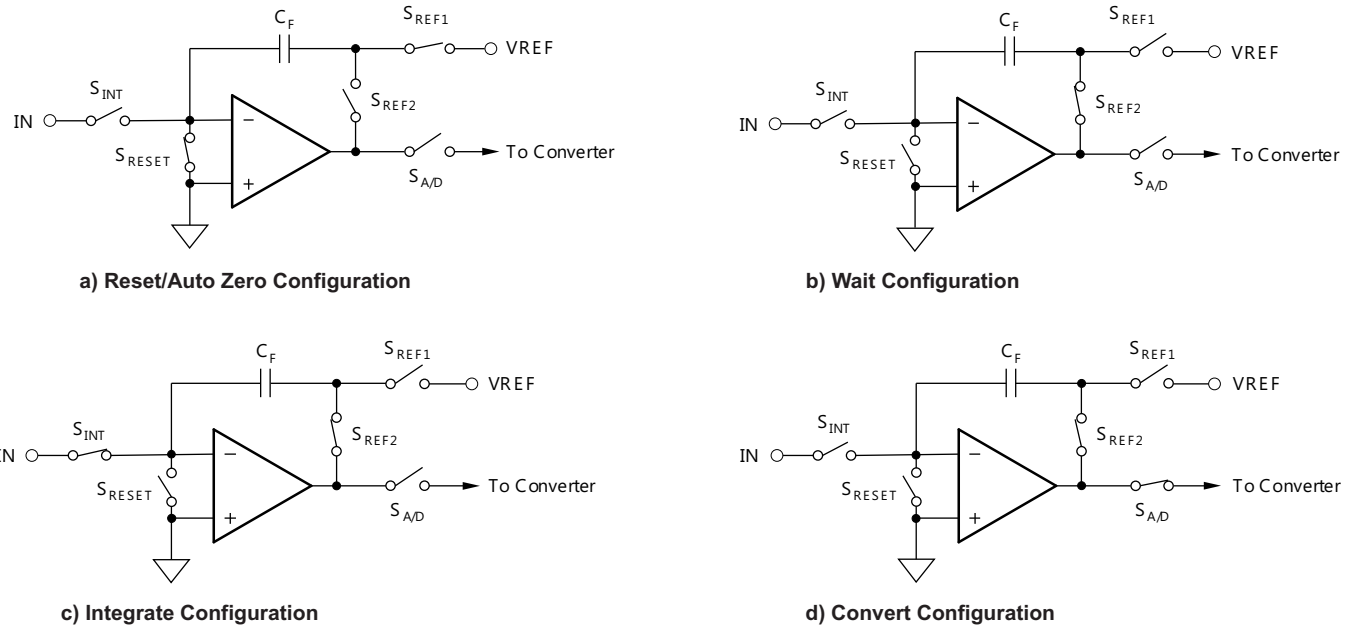


Figure 21. Integration Timing (see Figure 20)



a) Reset/Auto Zero Configuration

b) Wait Configuration

c) Integrate Configuration

d) Convert Configuration

Figure 22. Four Configurations of the Front-End Integrators

Feature Description (continued)

8.3.2 Integration Capacitors

There are four different capacitor configurations available on-chip for both sides of every channel in the DDC264. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC264. The range control bits (Range[1:0]) set the capacitor value for all integrators. Consequently, all inputs and both sides of each input always have the same full-scale range. Table 3 shows the capacitor value selected for each range selection.

Table 3. Range Selection

RANGE	RANGE CONTROL BITS		C_F	INPUT RANGE
	Range[1]	Range[0]		
0	0	0	3 pF	–0.04 to 12.5 pC
1	0	1	12.5 pF	–0.2 to 50 pC
2	1	0	25 pF	–0.4 to 100 pC
3	1	1	37.5 pF	–0.6 to 150 pC

8.3.3 Voltage Reference

The external voltage reference is used to reset the integration capacitors before an integration cycle begins. It is also used by the A/D converter while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling, the external reference must supply the charge required by the A/D converter. For an integration time of 333 µs, this charge translates to an average V_{REF} current of approximately 825 µA. The amount of charge required by the A/D converter is independent of the integration time; therefore, increasing the integration time lowers the average current. For example, an integration time of 800 µs lowers the average V_{REF} current to 340 µA.

8.3.4 Serial Data Output and Control Interface

8.3.4.1 System and Data Clocks (CLK and DCLK)

The device internal clock is derived directly or after a divide by 4 from the CLK input (see Bit[13] in the configuration register). TI recommends driving the CLK pin with a free-running clock source (that is, do not start and stop CLK between conversions). Make sure the clock signals are clean—avoid overshoot or ringing.

As explained in *Overview*, DCLK is used to read out the data (more details in the following sections). For best performance, generate CLK and DCLK clocks from the same clock source. Disable DCLK by taking it low after the data have been shifted out and while CONV is transitioning.

When using multiple DDC264 devices, pay close attention to the DCLK distribution on the printed-circuit board (PCB). In particular, make sure to minimize skew in the DCLK signal because this can lead to timing violations in the serial interface specifications. See *Cascading Multiple Converters* for more details.

8.3.4.2 CONV: Setting the Integration Time

As explained in *Overview*, one integration cycle happens between two consecutive CONV signal edges. For the best noise performance, CONV must be synchronized with the falling edge of CLK. TI recommends toggling CONV within ±10 ns of the falling edge of CLK.

The minimum t_{INT} for the DDC264 scales directly with the internal clock frequency. With an internal clock frequency of 10 MHz, the minimum time is 160 µs, which is achieved with the right register settings (see *Configuration Register — Read and Write Operations* for more details). If the minimum integration time is violated, the DDC264 stops continuously integrating the input signal. To return to normal operation (that is, continuous integration) after a violation of the minimum tINT specification, perform three integrations that each last for a minimum of 5000 internal clock periods. In other words, integrate three times with each integration lasting for at least 1 ms when using an internal clock frequency of 5 MHz. During this time, ignore the $\overline{\text{DVALID}}$ pin. Once the three integrations complete, normal continuous operation resumes, and data can be retrieved.

8.3.4.3 Data Valid (DVALID)

The DVALID signal indicates that data are ready to be read. Data retrieval may begin after DVALID goes low. This signal is generated using an internal clock divided down from the system clock, CLK. The phase relationship between this internal clock and CLK is set when power is first applied and is random. Because the user must synchronize CONV with CLK, the DVALID signal has a random phase relationship with CONV. This uncertainty is $\pm 1/f_{CLK}$. Polling DVALID eliminates any concern about this relationship. If the data readback is timed from CONV, make sure to wait for the required amount of time. The data stored internally is lost if not read before the next DVALID.

8.3.4.4 Data Format

The serial output data are provided in an offset binary code as shown in Table 4. The format bit in the configuration register selects how many bits are used in the output word. When format = 1, 20 bits are used. When format = 0, the lower four bits are truncated so that only 16 bits are used. Note that the LSB size is 16 times bigger when format = 0. An offset is included in the output to allow slightly negative inputs (for example, from board leakages) from clipping the reading. This offset is approximately 0.4% of the positive full-scale.

Table 4. Ideal Output Code vs Input Signal(1)

INPUT SIGNAL	IDEAL OUTPUT CODE FORMAT = 1	IDEAL OUTPUT CODE FORMAT = 0
≥ 100% FS	1111 1111 1111 1111 1111	1111 1111 1111 1111
0.001531% FS	0000 0001 0000 0001 0000	0000 0001 0000 0001
0.001436% FS	0000 0001 0000 0000 1111	0000 0001 0000 0000
0.000191% FS	0000 0001 0000 0000 0010	0000 0001 0000 0000
0.000096% FS	0000 0001 0000 0000 0001	0000 0001 0000 0000
0% FS	0000 0001 0000 0000 0000	0000 0001 0000 0000
–0.3955% FS	0000 0000 0000 0000 0000	0000 0000 0000 0000

(1) Excludes the effects of noise, INL, offset, and gain errors.

8.3.4.5 Data Retrieval

The data from the last conversion are available for retrieval on the falling edge of DVALID (see Figure 23 and Table 5). Data are shifted out on the falling edge of the data clock, DCLK.

Make sure not to retrieve data around changes in CONV because this change can introduce noise. Stop activity on DCLK at least 2 µs before or after a CONV transition.

Setting the format bit = 0 (16-bit output word) reduces the time required to retrieve data by 20% because there are fewer bits to shift out. This technique can be useful in multichannel systems requiring only 16 bits of resolution.

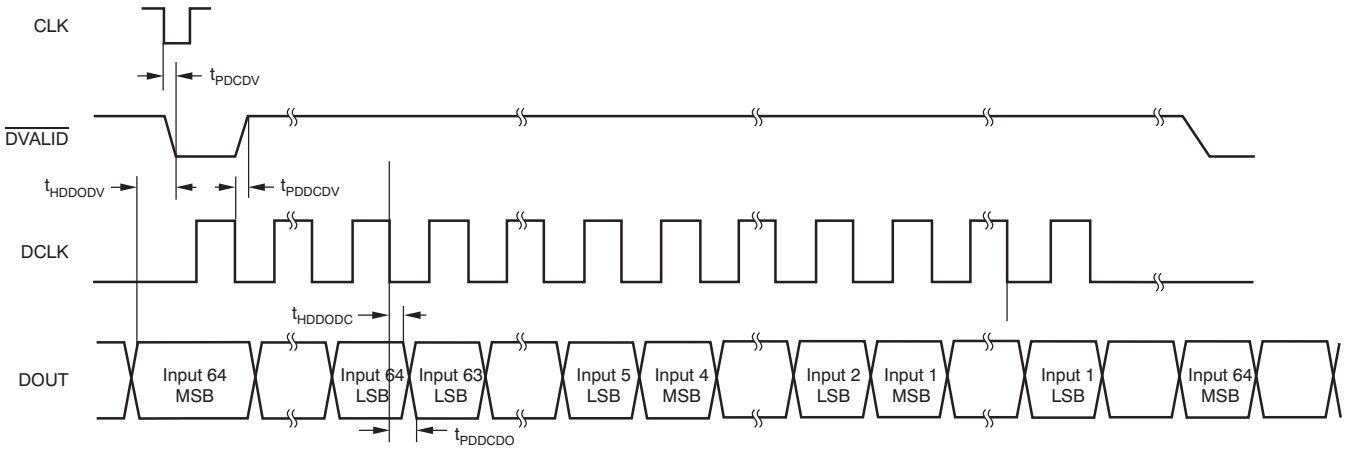


Figure 23. Digital Interface Timing Diagram for Data Retrieval From a Single DDC264

Table 5. Timing for DDC264 Data Retrieval

		MIN	TYP	MAX	UNIT
t_{PDCDV}	Propagation delay from falling edge of CLK to $\overline{DVALID}$ Low	10			ns
t_{PDDCDV}	Propagation delay from falling edge of DCLK to $\overline{DVALID}$ High	5			ns
t_{HDDODV}	Hold time that DOUT is valid before the falling edge of $\overline{DVALID}$		400		ns
t_{HDDODC}	Hold time that DOUT is valid after falling edge of DCLK	4			ns
t_{PDDCDO}	Propagation delay from falling edge of DCLK to valid DOUT			25	ns

8.3.4.5.1 Cascading Multiple Converters

Multiple DDC264 devices can be connected in a serial configuration; see Figure 24.

DOUT can be used with DIN to daisy-chain multiple DDC264 devices together to minimize wiring. In this mode of operation, the serial data output is shifted through multiple DDC264s; see Figure 24.

Figure 25 shows the timing diagram when the DIN input is used to daisy-chain several devices. Table 6 gives the timing specification for data retrieval using DIN.

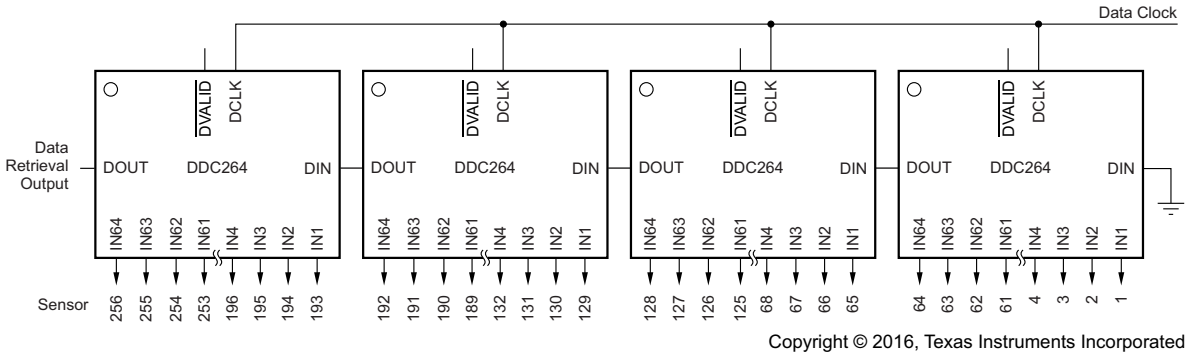
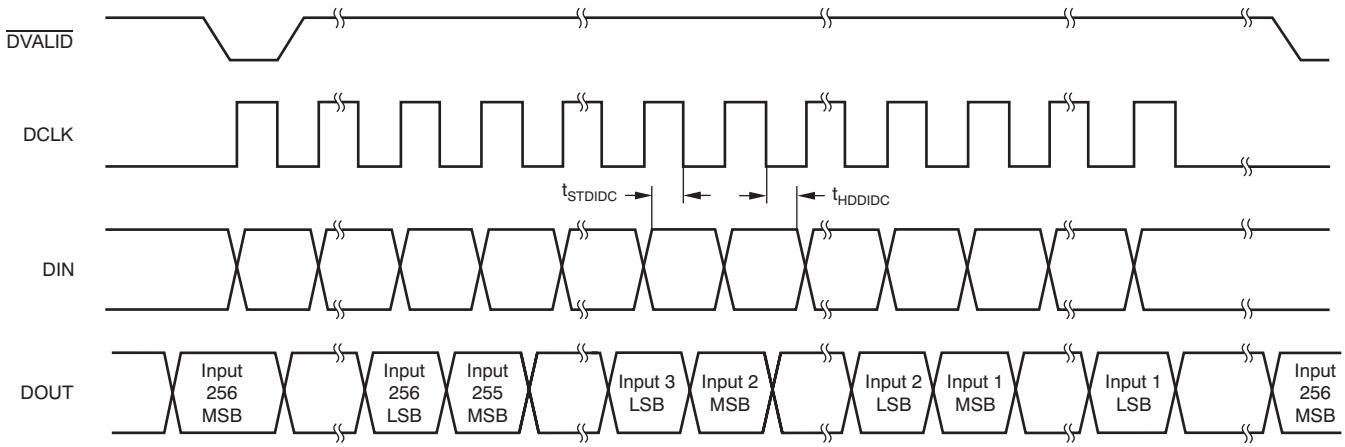


Figure 24. Daisy-Chained DDC264s



(1) See *Cascading Multiple Converters*.

Figure 25. Timing Diagram When Using DDC264 DIN Function

Table 6. Timing for DDC264 Data Retrieval Using DIN

		MIN	TYP	MAX	UNIT
t_{STDIDC}	Setup time from DIN to falling edge of DCLK	10			ns
t_{HDDIDC}	Hold time for DIN after falling edge of DCLK	10			ns

8.3.4.5.2 Retrieval Before CONV Toggles

In this method, data retrieval begins soon after $\overline{\text{DVALID}}$ goes low and finishes before CONV toggles, as shown in Figure 26. For best performance, data retrieval must stop t_{SDCV} before CONV toggles. This method is most appropriate for longer integration times and yields the best performance results as the output interface toggling noise does not interfere with the ADC conversion operation. The maximum time available for readback is $t_{INT} - t_{CMDR} - t_{SDCV}$. The maximum number of DDC264s that can be daisy-chained together (format = 1) is calculated by Equation 1.

$$\frac{t_{INT} - (t_{DR} + t_{SDCV})}{(20 \times 64)\tau_{DCLK}} \quad (1)$$

Note: $(16 \times 64)\tau_{DCLK}$ is used for format = 0, where τ_{DCLK} is the period of the data clock

For example, if t_{INT} = 1000 µs and DCLK = 20 MHz, the maximum number of DDC264s with format = 1 is shown in Equation 2.

$$\frac{1000\mu s - 278.4\mu s}{(1280)(50ns)} = 11.5 \rightarrow 11 \text{ DDC264s} \quad (2)$$

or 14 DDC264s for format = 0

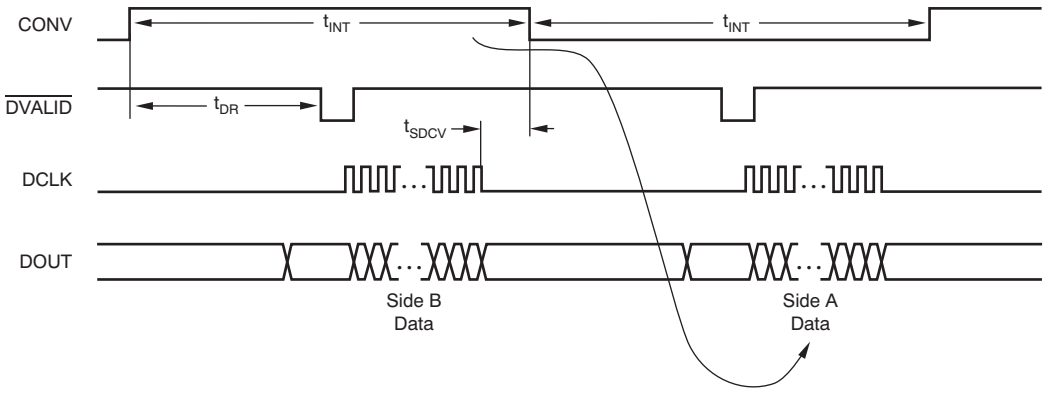


Figure 26. Readback Before CONV Toggles

Table 7. Timing for Readback

		MIN	TYP	MAX	UNIT
t_{SDCV}	Data retrieval shutdown before or after edge of CONV	2			µs

8.3.4.5.3 Retrieval After CONV Toggles

For shorter integration times, more time is available if data retrieval begins after CONV toggles and ends before the new data are ready. Data retrieval must wait t_{SDCV} after CONV toggles before beginning. See Figure 27 for an example of this timing sequence. The maximum time available for retrieval is $t_{DR} - (t_{SDCV} + t_{HDDODV})$, regardless of t_{INT}. The maximum number of DDC264s that can be daisy-chained together with format = 1 is calculated by Equation 3.

$$\frac{274\mu s}{(20 \times 64)\tau_{DCLK}} \quad (3)$$

Note: $(16 \times 64)\tau_{DCLK}$ is for format = 0

For DCLK = 20 MHz, the maximum number of DDC264s is four (or five for format = 0).

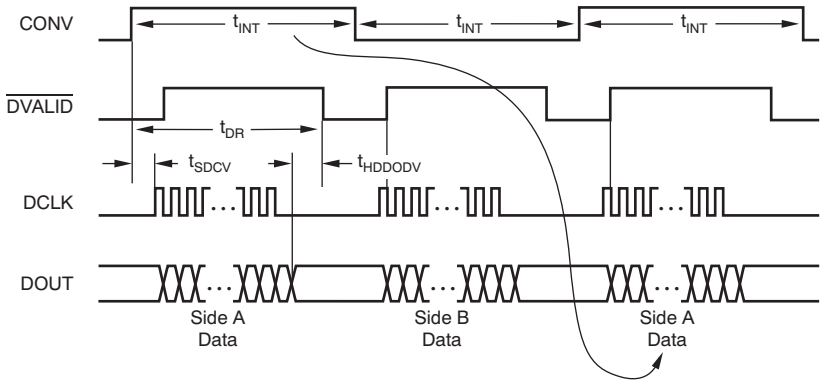


Figure 27. Readback After CONV Toggles

8.3.4.5.4 Retrieval Before and After CONV Toggles

For the absolute maximum time for data retrieval, data can be retrieved before and after CONV toggles. Nearly all of t_{INT} is available for data retrieval. Figure 28 illustrates how this process is done by combining the two previous methods. Pause the retrieval during CONV toggling to prevent digital noise, as discussed previously, and finish before the next data are ready. The maximum number of DDC264s that can be daisy-chained together with format = 1 is calculated by Equation 4.

$$\frac{t_{INT} - (t_{SDCV} + t_{SDCV} + t_{HDDODV})}{(20 \times 64)\tau_{DCLK}}$$

Note: $(16 \times 64)\tau_{DCLK}$ is used for format = 0 (4)

For t_{INT} = 400 µs and DCLK = 20 MHz, the maximum number of DDC264s is six (or seven for format = 0).

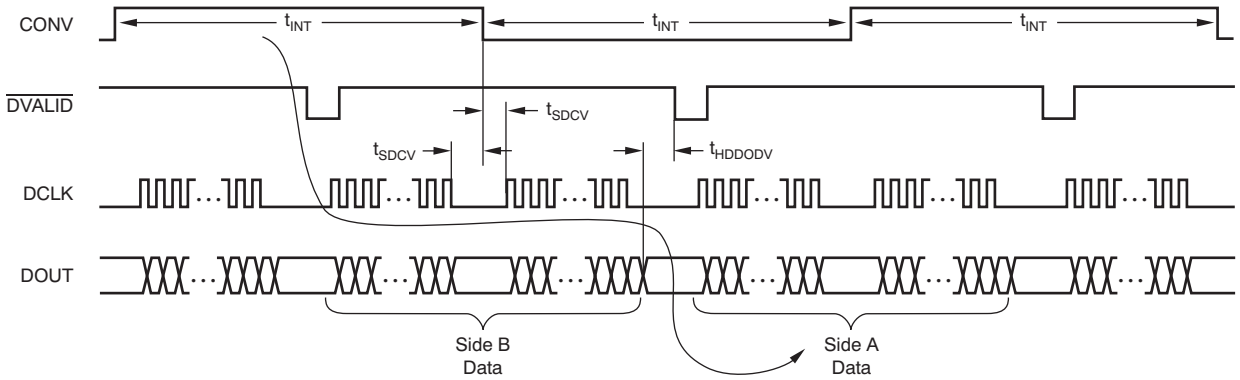


Figure 28. Readback Before and After CONV Toggles

8.4 Device Functional Modes

There are no functional modes for this device.

8.5 Programming

8.5.1 Reset ($\overline{\text{RESET}}$)

The DDC264 is reset asynchronously by taking the $\overline{\text{RESET}}$ input low, as shown in Figure 29. Make sure the release pulse is a minimum of t_{RST} wide. It is very important that $\overline{\text{RESET}}$ is glitch-free to avoid unintentional resets. The Configuration Register must be programmed immediately afterwards. After programming the DDC264, wait at least four conversions before using the data.

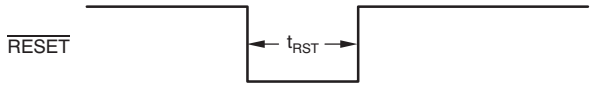


Figure 29. Reset Timing

8.5.2 Configuration Register — Read and Write Operations

The Configuration Register must be programmed after power-up or a device reset. The DIN_CFG, CLK_CFG, and $\overline{\text{RESET}}$ pins are used to write to this register. When beginning a write operation, hold CONV low and strobe $\overline{\text{RESET}}$; see Figure 30. Then begin shifting in the configuration data on DIN_CFG. Data are written to the Configuration Register most significant bit first. The data are internally latched on the falling edge of CLK_CFG. Partial writes to the Configuration Register are not allowed, that is, make sure to send all 16 bits when updating the register.

Optional readback of the Configuration Register is available immediately after the write sequence. During readback, 320 '0's, then the 16-bit configuration data followed by a 4-bit revision ID and the check pattern are shifted out on the DOUT pin on the rising edge of DCLK. The check pattern can be used to check or verify the DOUT functionality.

NOTE

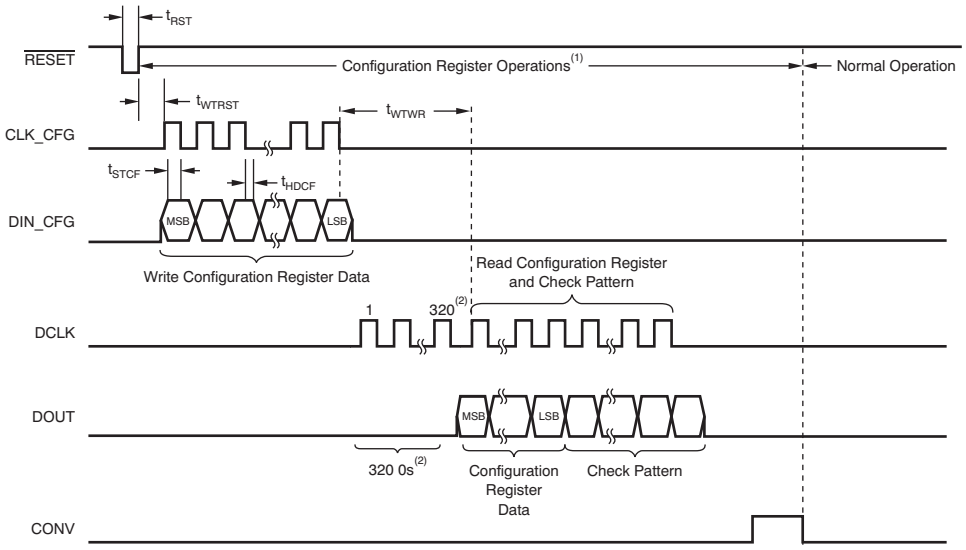
With format = 1, the check pattern is 300 bits, with only the last 72 bits non-zero. This sequence of outputs is repeated twice for each DDC264 block and daisy-chaining is supported in configuration readback. Table 9 shows the check pattern configuration during readback. Table 8 shows the timing for the Configuration Register read and write operations. Strobe CONV to begin normal operation, that is, CONV must not toggle during the readback operation.

Table 8. Timing Requirements for the Configuration Register Read/Write

		MIN	TYP	MAX	UNIT
t_{WTRST}	Wait Required from Reset High to First Rising Edge of CLK_CFG	2			µs
t_{WTWR}	Wait Required from Last CLK_CFG of Write Operation to First DCLK of Read Operation	2			µs
t_{STCF}	Set-Up Time from DIN_CFG to Falling Edge of CLK_CFG	10			ns
t_{HDCF}	Hold Time for DIN_CFG After Falling Edge of CLK_CFG	10			ns
t_{RST}	Pulse Width for $\overline{\text{RESET}}$ Active	1			µs

Table 9. Check Pattern During Readback

FORMAT BIT	CHECK PATTERN (Hex)	TOTAL READBACK BITS
0	180 0s, 30F066012480F6h	1024
1	228 0s, 30F066012480F69055h	1280



CLK must be running during Configuration Register write and read operations.

In 16-bit mode (format = 0), only 256 0s are read before the Configuration Register write and read operations.

Figure 30. Configuration Register Write and Read Operations

8.6 Register Maps

Configuration Register Bit Assignments

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0	0	Clkdiv	0	0	Range[1]	Range[0]	Format
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Version	0	0	Reserved	0	0	0	Test

Bits 15:14 **These bits must always be set to *0*.**

Bit 13 **Clkdiv**

The Clkdiv input enables an internal divider on the system clock as shown in Table 10. When Clkdiv = 1, the system clock is divided by 4. This configuration allows a system clock that is faster by a factor of four, which in turn provides a finer quantization of the integration time, because the CONV signal must be synchronized with the system clock for the best performance.

0 = Internal clock divider set to 1
1 = Internal clock divider set to 4

Table 10. Clkdiv Operation

Clkdiv BIT	CLK DIVIDER VALUE	CLK FREQUENCY	INTERNAL CLOCK FREQUENCY
0	1	5 MHz	5 MHz
1	4	20 MHz	5 MHz

Bits 12:11 **These bits must always be set to *0*.**

Bits 10:9 **Range[1:0]**

These bits set the full-scale range.

00 = Range 0 = 12.5 pC
01 = Range 1 = 50 pC
10 = Range 2 = 100 pC
11 = Range 3 = 150 pC

Bit 8 **Format**

Format selects how many bits are used in the data output word.

0 = 16-bit output
1 = 20-bit output

Bit 7 **Version**

This bit must be set to match the device being used.
Must be set to *0* for DDC264C.
Must be set to *1* for DDC264CK.

Bits 6:5 **These bits must always be set to *0*.**

Bit 4 **Reserved**

This bit is reserved and must be set to *0*.

Bits 3:1 **These bits must always be set to *0*.**

Bit 0 **Test**

When Test Mode is used, the inputs (IN1 through IN64) are disconnected from the DDC264 integrators to enable the user to measure a *zero* input signal regardless of the current supplied to the inputs.

0 = TEST mode off
1 = TEST mode on

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application case of the DDC family of products, including the DDC264, is the measurement of currents produced by photodiodes when excited by light, or the equivalent charge over a period of time (see Equation 5). The DDC264 can measure 64 channels simultaneously. As explained in *Functional Block Diagram*, the measurement is done by integrating the currents during a given time, set by the two consecutive edges of the CONV signal, provided by the system, see Figure 19. The result of the integration is shown in Equation 5.

$$Q = \int_{t_i}^{t_f} i(t)\,dt \tag{5}$$

where

- t_i and t_f represent the instant where the integration starts and finishes, respectively
- i(t) the input current (which is a function of time)
- Q the reported result by the DDC

All temporal information of i in that interval is lost and only an equivalent average i can be obtained.

The user must also provide a CLK signal used to run all the internal circuits, including the ADCs, which converts the result of the integration and generate a DVALID pulse to indicate that the conversion is done. The controller, then, can read that data, before it gets erased by the next conversion. The following sections explain the necessary control signals to operate the device, and the choices that the circuit designer can make.

9.2 Typical Application

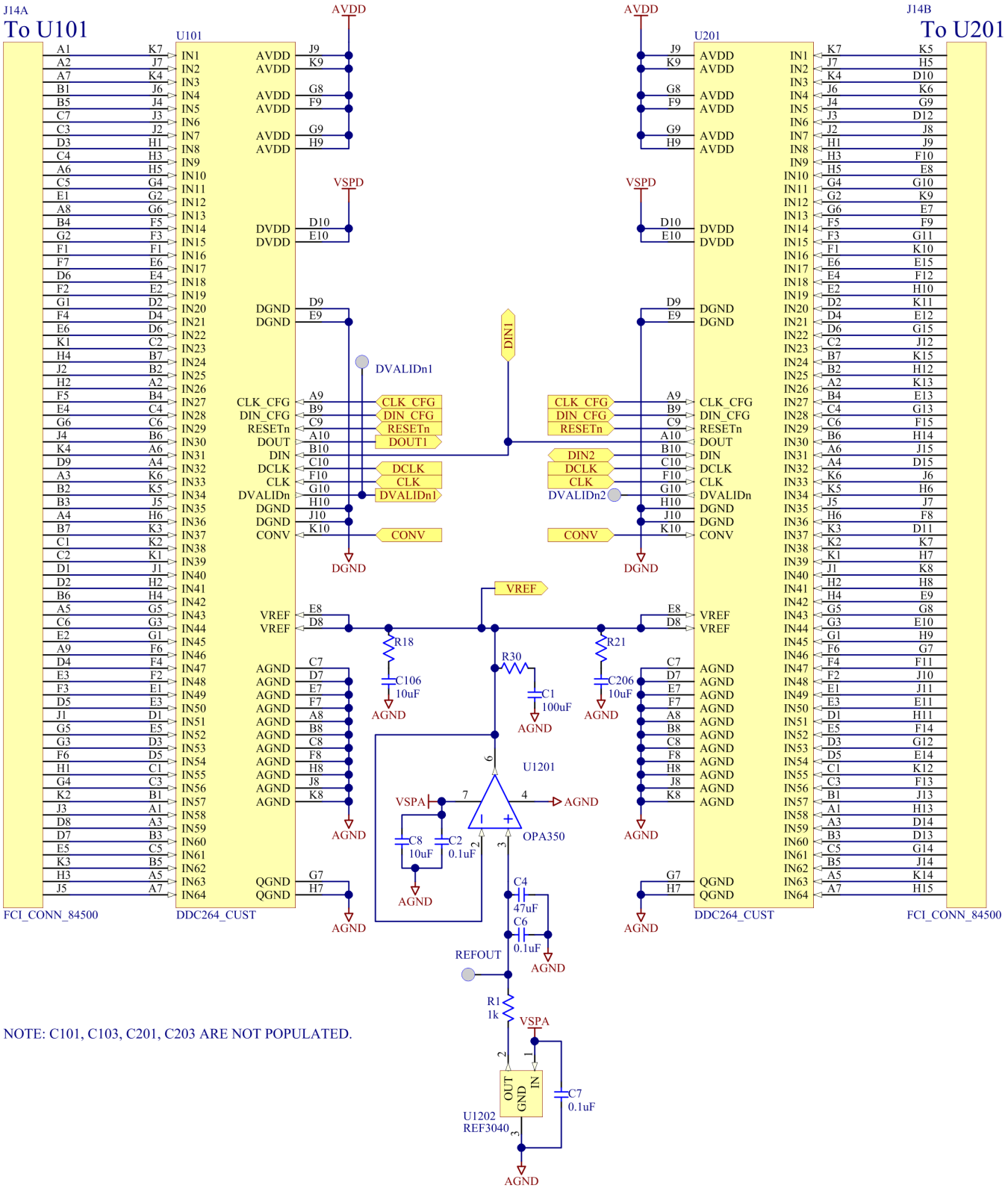


Figure 31. Typical Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

For the following example, assume the user wants to measure the current coming from 128 photodiodes every 500 µs, and the maximum current per photodiode is 250 nA.

9.2.2 Detailed Design Procedure

9.2.2.1 Input Connection

Figure 31 represents a top level schematic of a solution for this case. 2 DDC264 are used. Inputs are represented on the top schematic by the two connectors on the left and right sides.

The photodiodes must be connected to the inputs in such a way that the current flows into the device. To achieve that, usually the anode of the photodiode is connected to the input of the device (see Figure 20) and the cathode to a node with the same or higher voltage, in such a way that the photodiode is reverse biased or not biased at all. The application usually determines the choice. No bias minimizes dark current in the photodiode; therefore, minimizing errors during the integration or measurement of small signal currents. Nevertheless, the parasitic junction capacitance of the photodiode decreases with the reverse bias voltage. The lower the input capacitance, the lower the input noise (see Table 1). As such, applying a reverse bias reduces the noise of the measurement while increasing the dark current. The user must choose depending on their application. In applications with small signal currents, usually no bias is applied. In that case, the cathodes can be connected to AGND.

Notice that although only positive currents (in the direction towards the inside of the device) can be measured, the device has around 0.4% margin towards the negative excursion. In this way, small offsets and negative currents do not saturate the device in the bottom rail and can be detected and measured.

9.2.2.2 Selecting Integration Time, Device Clock, and Range

The second step is to select the right integration time. There may be system level constraints that set this. For instance, to get at least a given number of readings per second. Going faster than that may not be helpful, degrade performance and increase power unnecessarily. In this case, the user wants to, at least, get 2 KSPS (integration time = 500 µs). With 500 µs, the maximum integrated charge would be 250 nA × 500 µs = 125 pC. This is too much for Range 2 (100 pC full scale) but falls comfortably in Range 3 (150 pC). As such, the likely preferred option is to use Range 3 by setting bits 9 and 10 to one. Another potential option is to run the device slightly faster such that Range 2 can be used. In this case, 100 pC/250 nA = 400 µs, or 2.5 KSPS. Notice that this frequency (the frequency at which input currents are sampled) is actually 2× the frequency of the CONV signal. That is, 400 µs is half the period of the CONV signal, i.e. the time between two consecutive edges of the CONV signal.

The user must check the specification and performance curves to see the differences between both ranges for the specific conditions. Normally, performance may be close in both cases and operating the device slower may give some extra advantage on power and help relax practical system constraints.

For this particular case, both choices can be supported with the lower speed version device (DDC264C version), which supports up to 3 KSPS. As such, to benefit from this, the user must set bit 7 to zero. In this mode, the maximum internal clock is 5 MHz, so the user can choose to drive the CLK pin of the device with a 5-MHz clock maximum or with a 20-MHz clock maximum and the internal divide by 4 (setting register bit 13 to one).

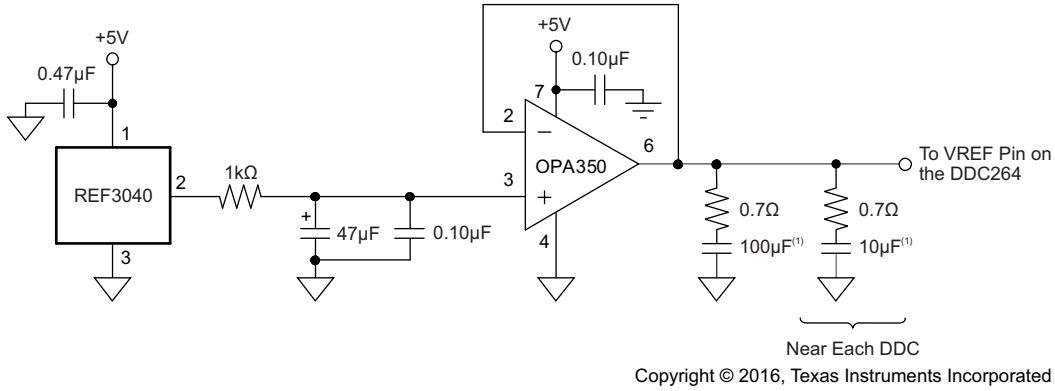
Notice that using a slower external clock is also possible, but the ADC conversion lasts longer (see t_{DR} in *Table 2*). This affects the time left to capture data after DVALID and before CONV edge (see *Reading the Measurement*)

9.2.2.3 Voltage Reference

It is critical that V_{REF} be stable during the different modes of operation (see Figure 22). The A/D converter measures the voltage on the integrator with respect to V_{REF}. Because the integrator capacitors are initially reset to V_{REF}, any drop in V_{REF} from the time the capacitors are reset to the time when the converter measures the integrator output introduces an offset. It is also important that V_{REF} be stable over longer periods of time because changes in V_{REF} correspond directly to changes in the full-scale range. Finally, V_{REF} must introduce as little additional noise as possible.

Typical Application (continued)

For these reasons, it is strongly recommended that the external reference source be buffered with an operational amplifier, as shown in Figure 32. In this circuit, the voltage reference is generated by a +4.096 V reference. A low-pass filter to reduce noise connects the reference to an operational amplifier configured as a buffer. This amplifier must have low noise and input/output common-mode ranges that support V_{REF}. Even though the circuit in Figure 32 might appear to be unstable because of the large output capacitors, it works well for the OPA350. TI does not recommend a series resistor be placed at its output to improve stability, because this can cause a drop in V_{REF} which produces large offsets. 10 µF and 0.7 Ω are good initial values for the decoupling network close to the DDC264, but may have to be optimized depending on its placement and board layout.



(1) Ceramic X5R capacitors are recommended.

Figure 32. Recommended External Voltage Reference Circuit for Best Low-Noise Operation

Figure 31 shows a portion of the driving circuit on the top part, driving one of the DDC264. This assumes that the output of the reference IC is routed from somewhere else, due, for instance, to space limitations on the board. Being the reference noise critical for the final performance of the system, TI recommends shielding and passing the filter the signal low. The bottom of Figure 31 shows the second DDC264 where the reference is driven by the same buffer as the first DDC and only a decoupling network is added close to the device. This is again assuming space and cost limitations. Ideally the use of two different buffers, one close to each reference, isolates interactions between both devices from being coupled through the reference line.

9.2.2.4 Reading the Measurement

As explained in *Data Retrieval*, the data can be read as soon as $\overline{\text{DVALID}}$ goes low. The user can choose to monitor this signal or simply wait a period of time predicted by t_{DR} in Table 2. For this example, assuming that a CLK frequency of 5 MHz was selected, the data would be ready after approximately 276 µs. Staying with Range 3, the integration time is 500 µs and as such, after detecting DVALID, there is approximately 500 µs – 276 µs to read the data. We assume 220 µs to avoid getting too close to the CONV edge. In 20 bit mode, reading two DDC264, with daisy chain between $\overline{\text{DOUT}}$ and DIN, see Figure 31, would take 128 × 20 × (1/32 MHz) = 80 µs, which fits in the interval between $\overline{\text{DVALID}}$ and next CONV edge. This minimizes noise due to the DCLK and DOUT switching during the conversion of the ADC (which happens from CONV edge to /DVALID) and can help improve the performance. In Figure 31, both converters are connected in daisy chain, which minimizes the number of traces being routed back to the controller. One small drawback of this approach versus shifting the data of both DDC264 in parallel (without the daisy chain) is that the outputs switch for longer time (2×), increasing the total power by a small fraction (as the output switching power is only a small portion of the total power consumption). Another solution is to transfer part or all the data during the ADC conversion (see *Retrieval Before and After CONV Toggles* and *Retrieval After CONV Toggles*). A potential way to minimize this noise, specially if the DOUT traces are long is to buffer them on board, close to the device.

9.2.3 Application Curve

The frequency response of the DDC264 is set by the front-end integrators and is that of a traditional continuous time integrator, as shown in Figure 33. By adjusting the integration time, t_{INT}, the user can change the 3-dB bandwidth and the location of the notches in the response. The frequency response of the A/D converter that follows the front-end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the A/D converter is always a DC signal. The output of the front-end integrators are sampled; therefore, aliasing can occur. Whenever the frequency of the input signal exceeds one-half of the sampling rate the signal folds back down to lower frequencies.

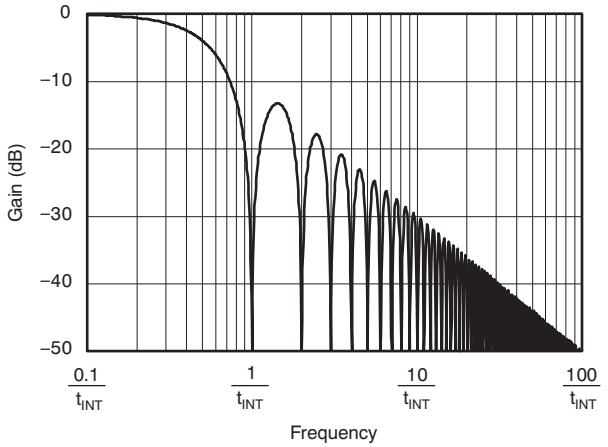


Figure 33. Frequency Response

10 Power Supply Recommendations

10.1 Power-Up Sequencing

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals must remain low until the power supplies have stabilized, as shown in Figure 34. The analog supply must come up before or at the same time as the digital supply. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then give a $\overline{\text{RESET}}$ pulse. After releasing $\overline{\text{RESET}}$, the Configuration Register must be written. Table 11 shows the timing for the power-up sequence.

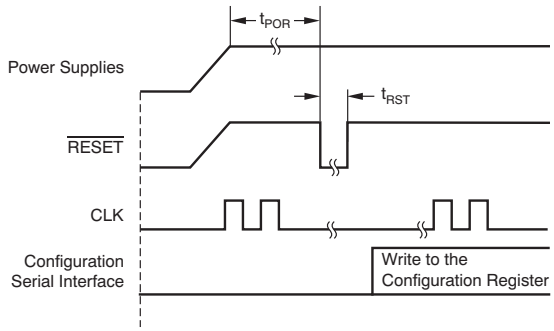


Figure 34. DDC264 Timing Diagram at Power-Up

Table 11. Timing for DDC264 Power-Up Sequence

		MIN	TYP	MAX	UNIT
t_{POR}	Wait after power-up until reset	250			ms

10.2 Power Supplies and Grounding

Both AVDD and DVDD must be as quiet as possible. It is particularly important to eliminate noise from AVDD that is non-synchronous with the DDC264 operation. Figure 35 illustrates how to supply power to the DDC264. Each DDC264 has internal bypass capacitors on AVDD and DVDD; therefore, the only external bypass capacitors typically required are 10-µF ceramic capacitors, one per PCB. TI recommends connecting both the analog and digital grounds (AGND and DGND) to a single ground plane on the PCB.

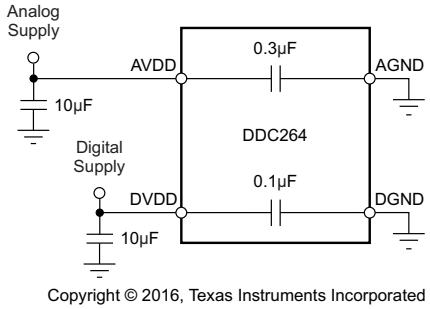


Figure 35. Power Supply Connections

11 Layout

11.1 Layout Guidelines

11.1.1 Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and QGND. The analog input pins are low-impedance and extremely sensitive to extraneous noise. The QGND pin must be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the DDC264 if shielding (guard) is not implemented. Digital signals (including digital supply) must be kept as far as possible from the analog input signals on the PCB. If possible, avoid running digital supply planes over analog ground or signals.

11.1.2 Power Supply Routing

Figure 36 shows a diagram summarizing the concept behind the power supply distribution used in the DDC264 evaluation module (EVM).

In theoretical terms, from an isolation perspective, generating all required supplies from different sources (LDOs) may be the best but may actually be not practical/too costly. In Figure 36, an analog supply is used to generate and drive the VREF/Buffer supplies and the DDC AVDD. The AGND runs parallel to this plane (above or below). The VREF signal is also routed in the same location. As seen on the figure, these do not overlap with the digital supply/ground/signals at any moment.

Away from the analog portion, a digital supply can be used/shared between the FPGA and the DDC. Nevertheless a star configuration is used to isolate the effect between both as much as possible. For the same reason, the physical planes of both digital supplies are also separated.

Notice nevertheless, that it is not a bad practice to include places along the separation between all these planes to allow for shorts, whether through a zero value resistor or a ferrite bead. This enables fine tuning of the design performance.

11.1.3 Reference Routing

In the case where only one reference buffer is used for multiple DDCs, all reference pins must be as isolated as possible from each other to avoid interactions between devices. One potential approach to this is to do a star connection where the traces to the reference of each device are connected to the others only at the output of the driver. Keep VREF shielded from any noisy signals, like digital traces or supplies.

11.2 Layout Example

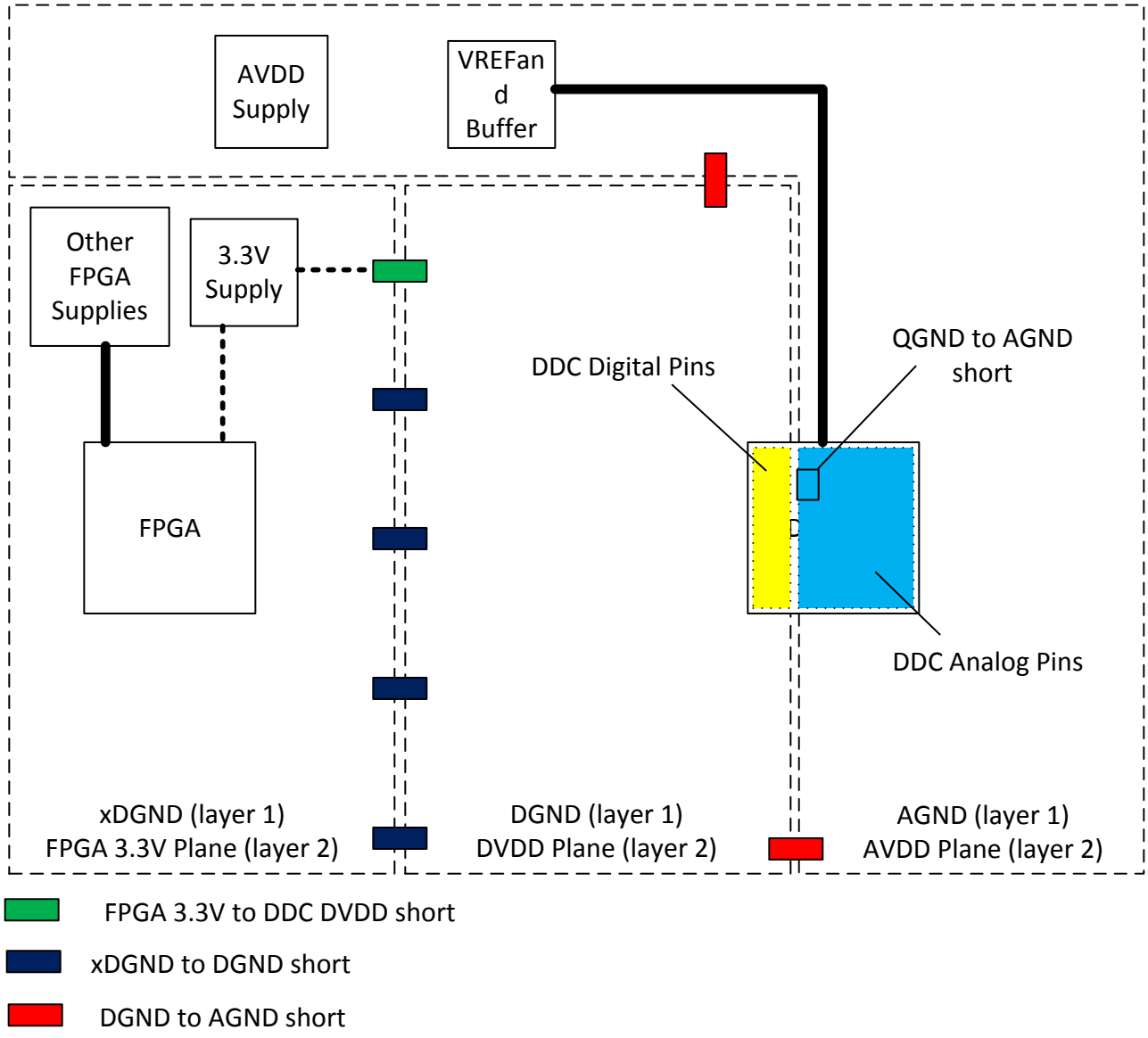


Figure 36. DDC264 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DDC264CKZAW	ACTIVE	NFBGA	ZAW	100	168	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264K	Samples
DDC264CKZAWR	ACTIVE	NFBGA	ZAW	100	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264K	Samples
DDC264CZAW	ACTIVE	NFBGA	ZAW	100	168	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264	Samples
DDC264CZAWR	ACTIVE	NFBGA	ZAW	100	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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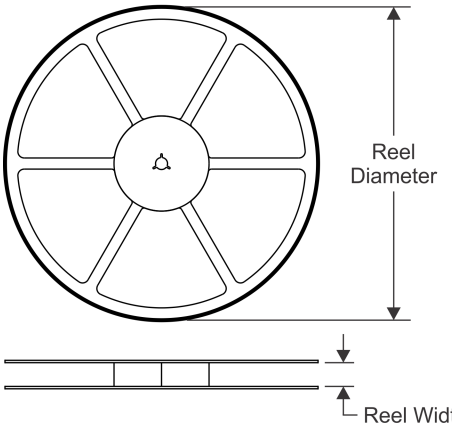
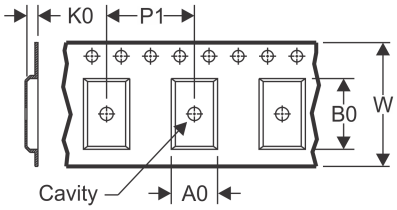
TAPE AND REEL INFORMATION

REEL DIMENSIONS

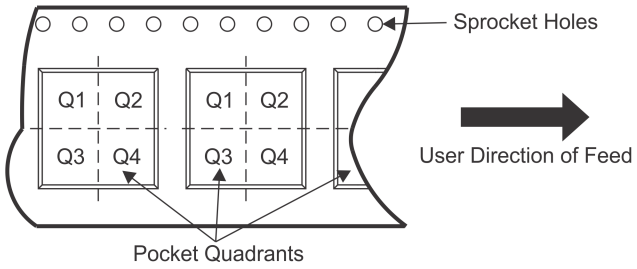


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

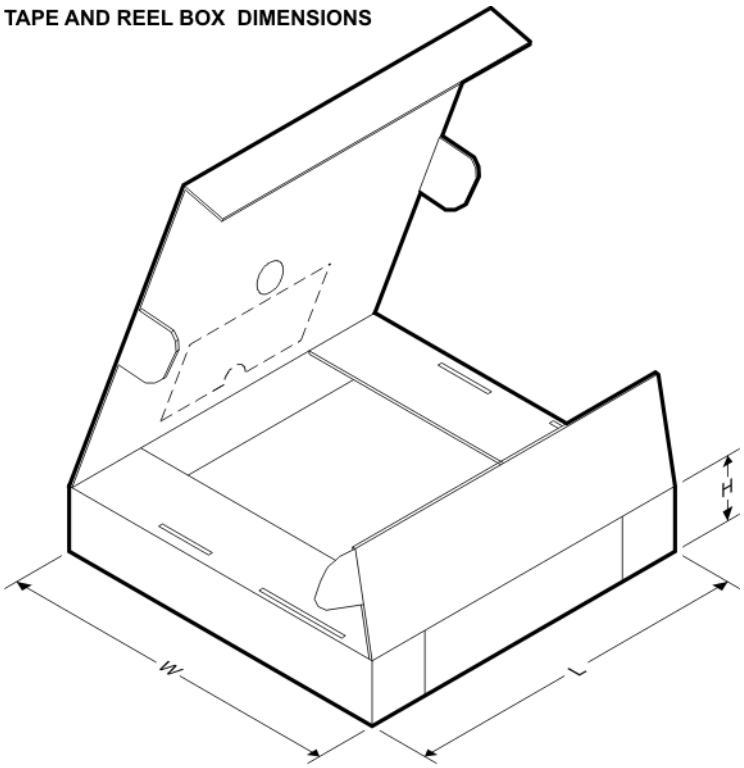
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DDC264CKZAWR	NFBGA	ZAW	100	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
DDC264CZAWR	NFBGA	ZAW	100	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1

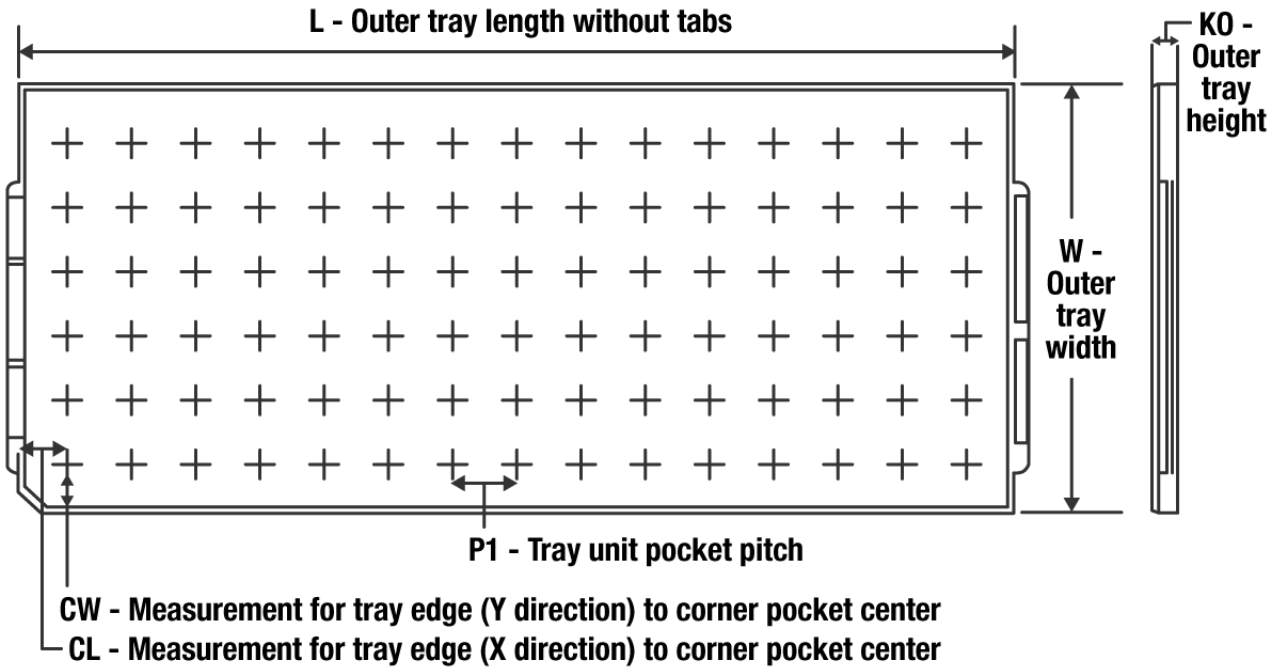
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DDC264CKZAWR	NFBGA	ZAW	100	1000	350.0	350.0	43.0
DDC264CZAWR	NFBGA	ZAW	100	1000	350.0	350.0	43.0

TRAY

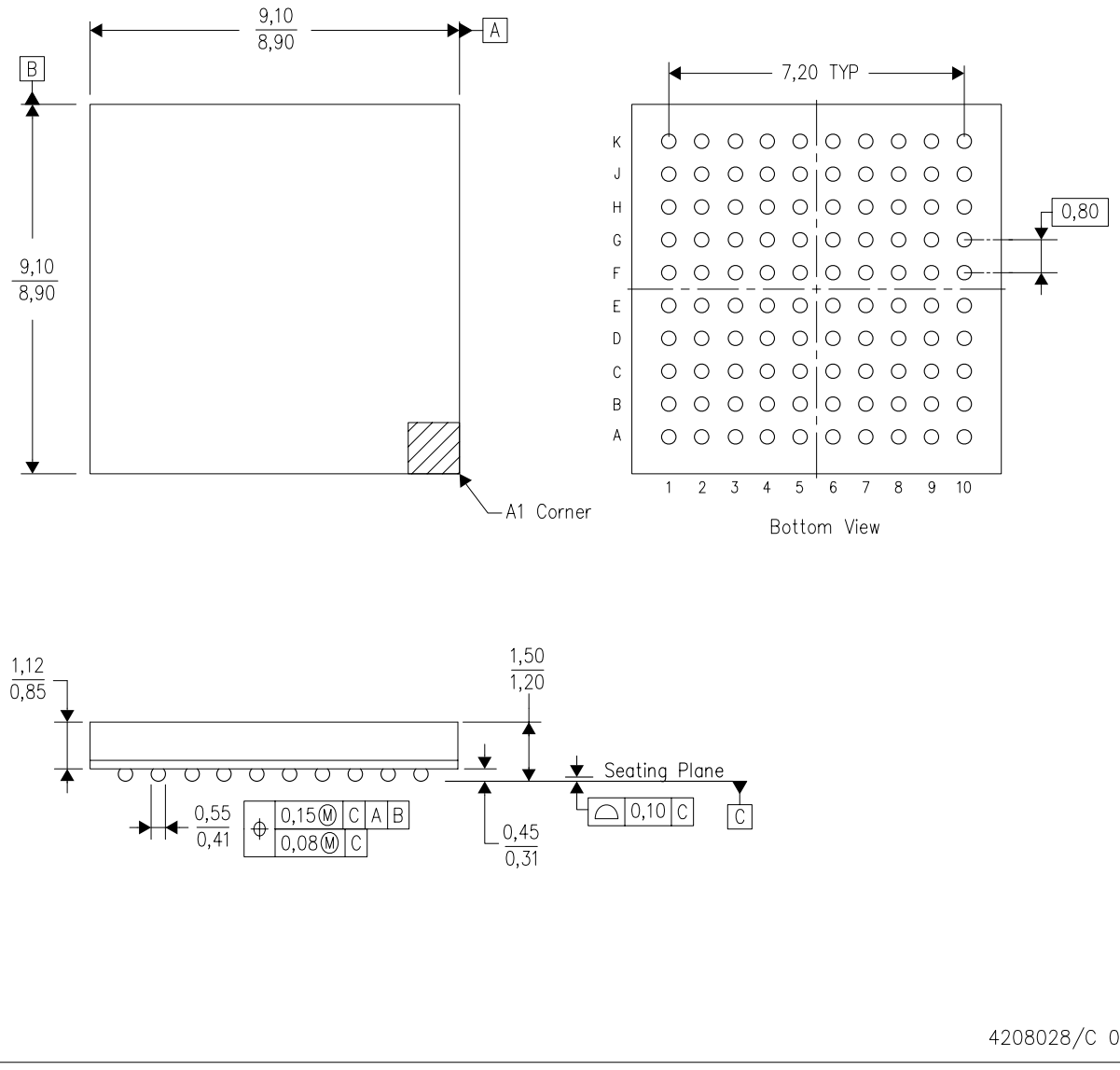


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DDC264CKZAW	ZAW	NFBGA	100	168	8 x 21	150	315	135.9	7620	14.75	10	12.7
DDC264CZAW	ZAW	NFBGA	100	168	8 x 21	150	315	135.9	7620	14.75	10	12.7

ZAW (S–PBGA–N100) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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