

采用 QFN 或 SOT563 封装的 TLV62585 3A 高效同步降压转换器

1 特性

- 效率高达 95%
- 低 $R_{DS(ON)}$ 电源开关: 56mΩ/32mΩ
- 输入电压范围为 2.5V 至 5.5V
- 可调输出电压范围为 0.6V 至 V_{IN}
- 可实现轻负载效率的省电模式
- 可实现最低压降的 100% 占空比
- 35μA 工作静态电流
- 1.5MHz 典型开关频率
- 短路保护 (HICCUP)
- 输出放电
- 电源正常状态输出
- 热关断保护
- 采用 2mm × 2mm QFN 封装或 1.6mm × 1.6mm SOT563 封装
- 使用 TLV62585 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 通用负载点电源
- 电池供电型应用
- 无线路由器、固态硬盘
- 机顶盒、多功能打印机
- 电机控制

3 说明

TLV62585 器件是一款高频同步降压转换器，经优化具有解决方案尺寸紧凑和高效率两大优点。该器件集成了可提供高达 3A 输出电流的开关。在中等负载至重负载情况下，该转换器将以 1.5MHz 典型开关频率在脉宽调制 (PWM) 模式下运行。在轻载情况下，该器件自动进入节能模式 (PSM)，从而在整个负载电流范围内保持高效率。关断时，流耗减少至 2μA 以下。

内部补偿电路可实现紧凑型解决方案和较少外部组件数。内部软启动电路可限制启动期间的浪涌电流。此外，还内置了其他功能，如短路保护、热关断保护、输出放电和电源良好指示。

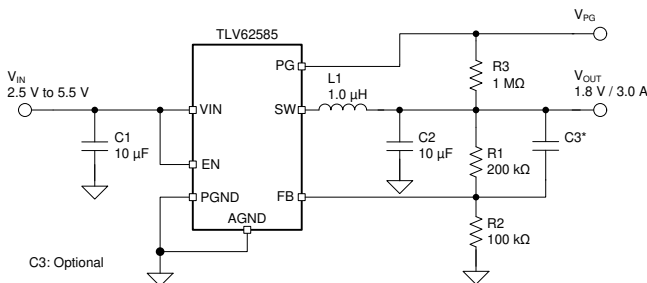
该器件采用 2mm × 2mm QFN 封装或 1.6mm × 1.6mm SOT563 封装。

器件信息(1)

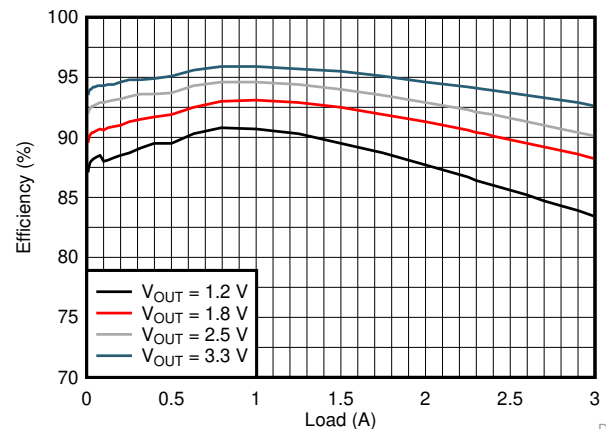
器件型号	封装	封装尺寸 (标称值)
TLV62585RWT	QFN (12)	2.00mm × 2.00mm
TLV62585DRL	SOT563 (6)	1.60mm × 1.60mm
TLV62585PDRL		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用原理图



5V 输入电压效率



D008



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (June 2018) to Revision F	Page
• Changed Temperature Range for 1% Accuracy from 25°C to 0°C-85°C	5

Changes from Revision D (April 2018) to Revision E	Page
• 将 TLV62585DRL 和 TLV62585PDRL 从产品预发布 更改为生产 数据	1
• 已添加 PCB layout recommendation for TLV62585PDRL	14

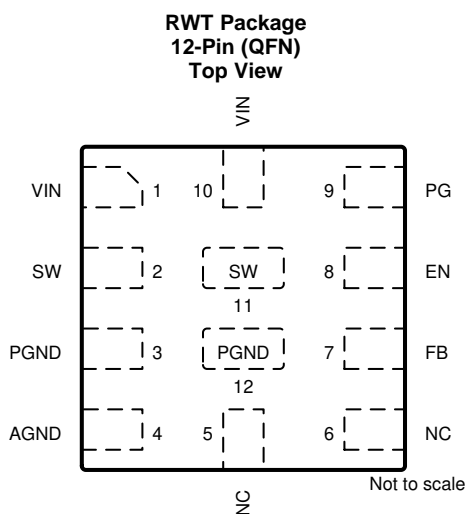
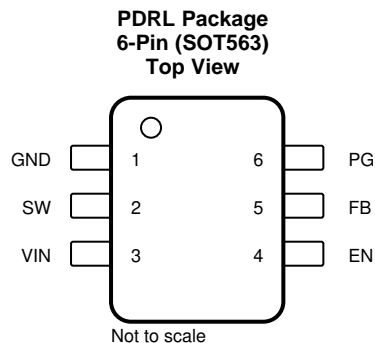
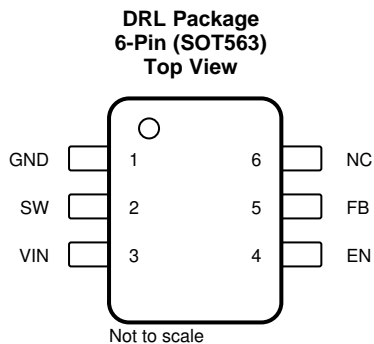
Changes from Revision C (November 2017) to Revision D	Page
• 向器件信息 表添加了 TLV62585DRL 和 TLV62585PDRL	1
• Added DRL and PDRL devices to the <i>Pin Configurations and Functions</i>	3
• Added the DRL Thermal Information	4
• Added 图 22	13

Changes from Revision B (September 2017) to Revision C	Page
• Changed HBM From: ± 1000 To: ± 2000 in the <i>ESD Ratings</i> table	4

Changes from Revision A (August 2017) to Revision B	Page
• 将器件状态从“预告信息”更改为“生产数据”	1
• Changed HBM From: TBD To: ± 1000 in the <i>ESD Ratings</i> table	4

Changes from Original (July 2017) to Revision A	Page
• 将器件状态从“生产”更改为“预告信息”	1
• Changed HBM From: ± 2000 To: TBD in the <i>ESD Ratings</i> table	4

5 Pin Configuration and Functions



Pin Functions

NAME	PIN			I/O	DESCRIPTION
	RWT (QFN)	DRL (SOT563)	PDRL (SOT563)		
VIN	1, 10	3	3	PWR	Power supply voltage pin.
SW	2, 11	2	2	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
GND	-	1	1	PWR	Ground pin.
PGND	3, 12	-	-	PWR	Power ground pin.
AGND	4	-	-	-	Ground pin.
NC	5, 6	6	-	-	No connection pin. Leave these pins open, or connect those pins to the output or to AGND.
FB	7	5	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
EN	8	4	4	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
PG	9	-	6	O	Power good open drain output pin. The pull-up resistor can not be connected to any voltage higher than 5.5 V. If unused, leave it floating or connect to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage at Pins ⁽¹⁾	VIN, EN, PG	-0.3	6	V
	FB	-0.3	3	
	SW (DC)	-0.3	V _{IN} + 0.3	
	SW (AC, less than 10ns) ⁽²⁾	-3.0	9	
Temperature	Operating Junction, T _J	-40	150	°C
	Storage, T _{stg}	-65	150	°C

- (1) All voltage values are with respect to network ground terminal.
(2) While switching

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	2.5		5.5	V
V _{OUT}	Output voltage range	0.6		V _{IN}	V
I _{SINK_PG}	Sink current at PG pin			1	mA
I _{OUT}	Output current	0		3	A
T _J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV62585		UNIT
		RWT [QFN]	DRL [SOT]	
R _{θJA}	Junction-to-ambient thermal resistance	95.7	132.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	74.1	43.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	29.4	27.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	5.8	1.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	29.7	26.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

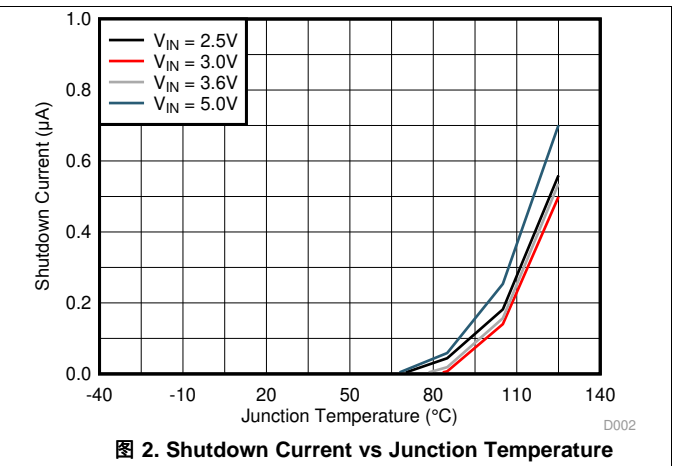
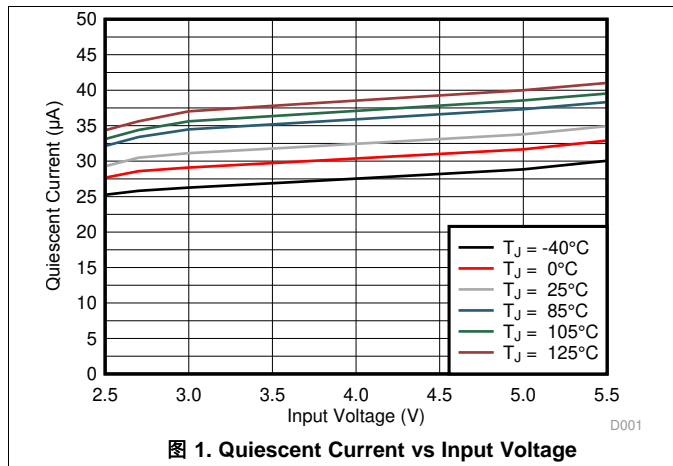
- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

T_J = 25 °C, and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _Q	Quiescent current into VIN	No load, device not switching		35		μA
I _{SD}	Shutdown current into VIN	EN = Low		0.7	2	μA
V _{UVLO}	Under voltage lock out threshold	V _{IN} falling		2.3	2.45	V
	Under voltage lock out hysteresis			150		mV
T _{JSD}	Thermal shutdown threshold	T _J rising		150		°C
	Thermal shutdown hysteresis			20		°C
LOGIC INTERFACE EN						
V _{IH}	High-level input voltage	V _{IN} = 2.5 V to 5.5 V	1.2			V
V _{IL}	Low-level input voltage	V _{IN} = 2.5 V to 5.5 V			0.4	V
SOFT START, POWER GOOD						
t _{SS}	Soft start time	Time from EN high to 95% of V _{OUT} nominal		900		μs
V _{PG}	Power good threshold	V _{OUT} rising, referenced to V _{OUT} nominal		95%		
		V _{OUT} falling, referenced to V _{OUT} nominal		90%		
V _{PG,OL}	Low-level output voltage	I _{sink} = 1 mA			0.4	V
I _{PG,LKG}	Input leakage current into PG pin	V _{PG} = 5.0 V		0.01		μA
t _{PG,DLY}	Power good delay	V _{FB} falling		40		μs
OUTPUT						
V _{FB}	Feedback regulation voltage	PWM mode, 2.5 V ≤ V _{IN} ≤ 5.5 V, 0°C to 85°C	594	600	606	mV
		PWM mode, 2.5 V ≤ V _{IN} ≤ 5.5 V, -40°C to 125°C	588	600	612	
I _{FB,LKG}	Feedback input leakage current	V _{FB} = 0.6 V		0.01		μA
R _{DIS}	Output discharge FET on-resistance	EN = Low, V _{OUT} = 1.8 V		10		Ω
POWER SWITCH						
R _{DS(on)}	High-side FET on-resistance			56		mΩ
	Low-side FET on-resistance			32		mΩ
I _{LIM}	High-side FET switch current limit		4	4.6		A
f _{SW}	PWM switching frequency	V _{OUT} = 1.8V, I _{OUT} = 1 A		1.5		MHz

6.6 Typical Characteristics



7 Detailed Description

7.1 Overview

The TLV62585 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off-time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.2 Functional Block Diagram

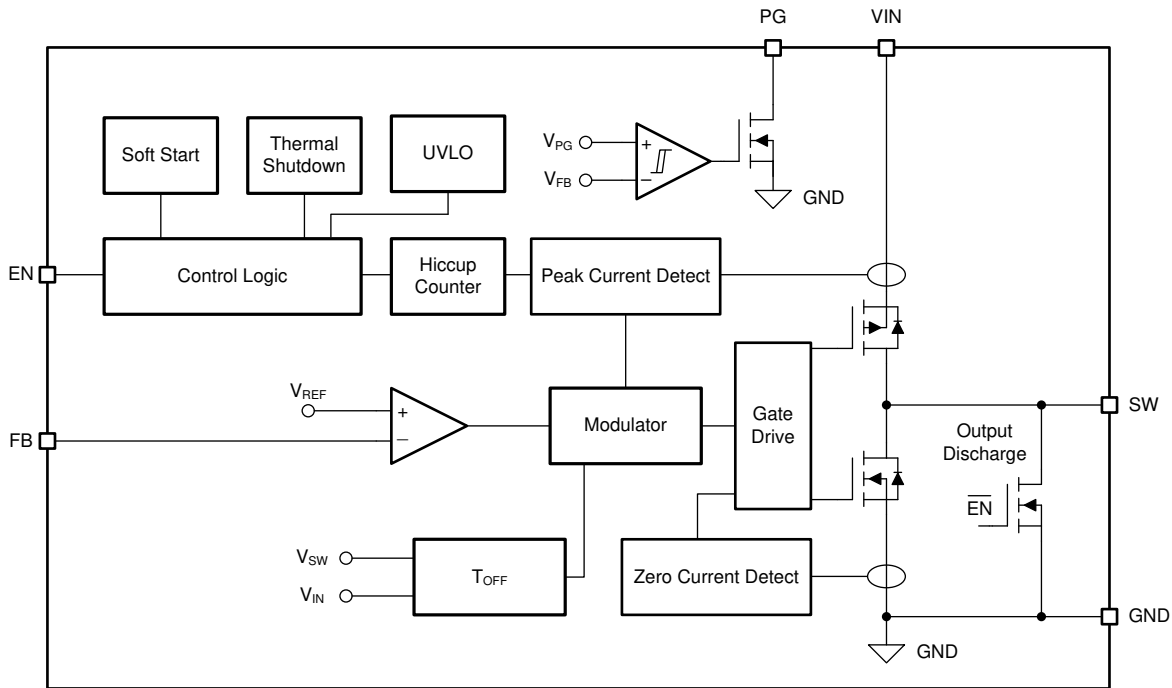


图 3. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor, or adding a feed forward capacitor, as shown in [图 14](#).

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times R_{DS(ON)} + R_L$$

Where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

(1)

Feature Description (接下页)

7.3.3 Soft Start

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TLV62585 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.4 Switch Current Limit and Short Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a over load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM} , the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off-time.

When this switch current limits is triggered 32 times, the device reduces the current limit for further 32 cycles and then stops switching to protect the output. The device then automatically start a new startup after a typical delay time of 500 μ s has passed. This is named HICCUP short circuit protection. The devices repeat this mode until the high load condition disappears. HICCUP protection is also enabled during the startup.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 150 mV.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD} . When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7 μ A.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal output discharge FET discharges the output through the SW pin smoothly.

7.4.2 Power Good

The TLV62585 has a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown			√
UVLO	$1.4\text{ V} < V_{IN} < 2.3\text{ V}$		√
Power Supply Removal	$V_{IN} \leq 1.4\text{ V}$	√	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62585 is a synchronous step-down converter in which output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

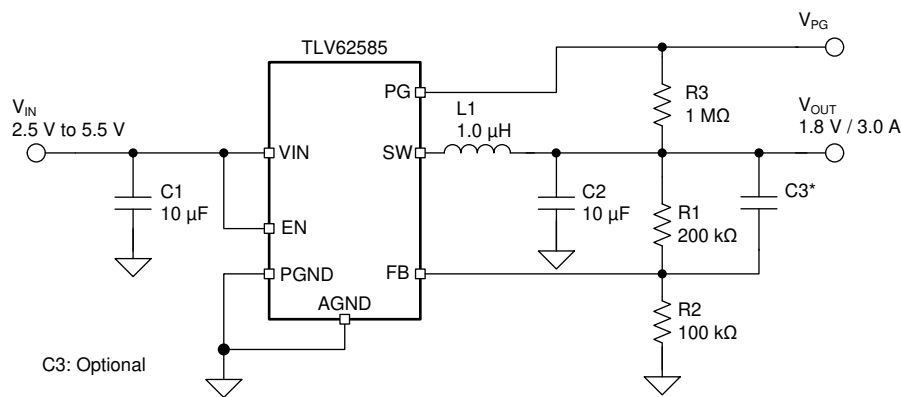


图 4. 1.8-V Output Voltage Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	3 A

表 3 lists the components used for the example.

表 3. List of Components⁽¹⁾

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 10 V, X7R, size 0805, GRM21BR71A106ME51	Murata
C2	22 µF, Ceramic capacitor, 6.3 V, X7T, size 0805, GRM21BD70J226ME44	Murata
C3	Optional	Std
L1	1 µH, Power Inductor, size 4 mm × 4 mm × 1.5 mm, XFL4020-102ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603;	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0603;	Std
R3	1 MΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See [Third-Party Products](#) disclaimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TLV62585 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to [公式 2](#):

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

R2 must not be higher than 100 k Ω to achieve high efficiency at light load while providing acceptable noise sensitivity.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, [表 4](#) outlines possible inductor and capacitor value combinations for most applications.

表 4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [μ H] ⁽¹⁾	NOMINAL C _{OUT} [μ F] ⁽²⁾⁽³⁾			
	10	22	47	100
0.47				
1	+	+ ⁽⁴⁾	+	
2.2				

- (1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
- (2) For low output voltage applications (< 1.8 V), more output capacitance is recommended (usually \geq 22 μ F) for smaller ripple. For output capacitance higher than 47 μ F, a feed forward capacitor is needed.
- (3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
- (4) Typical application configuration. Other '+' mark indicates recommended filter combinations.

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 公式 3 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

(3)

TI recommends choosing the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of 公式 3. A higher inductor value is also useful to lower ripple current but increases the transient response time as well.

8.2.2.5 Input and Output Capacitor Selection

The architecture of the TLV62585 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 10- μ F input capacitor is sufficient; a larger value reduces input voltage ripple.

The TLV62585 is designed to operate with an output capacitor of 10 μ F to 47 μ F, as outlined in 表 4.

A feed forward capacitor reduces the output ripple in PSM and improves the load transient response. A 22-pF capacitor is good for the 1.8-V output typical application.

8.2.3 Application Curves

$V_{IN} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted.

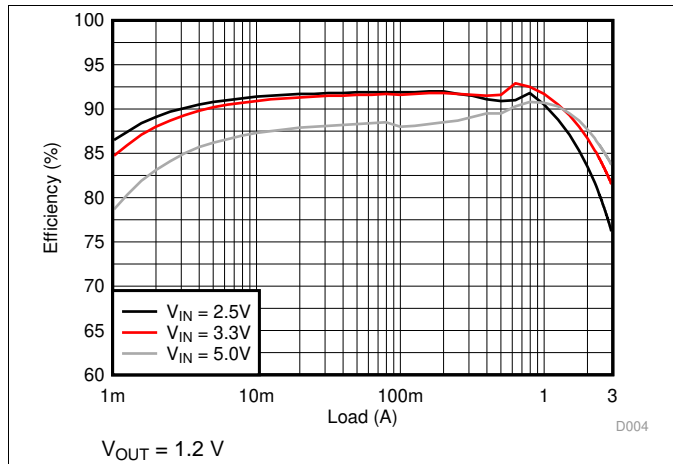


图 5. Efficiency

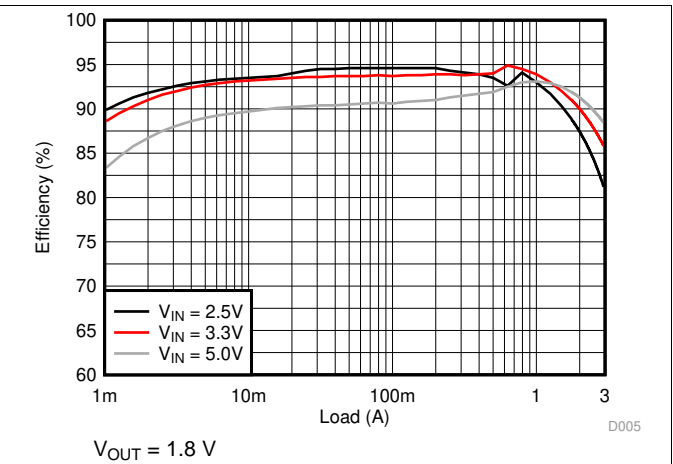


图 6. Efficiency

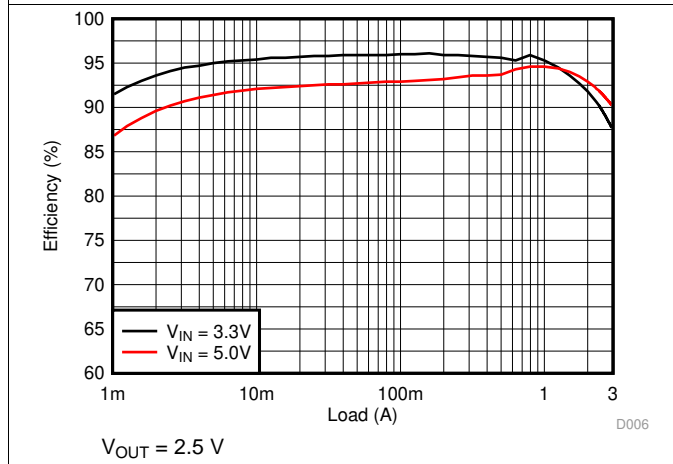


图 7. Efficiency

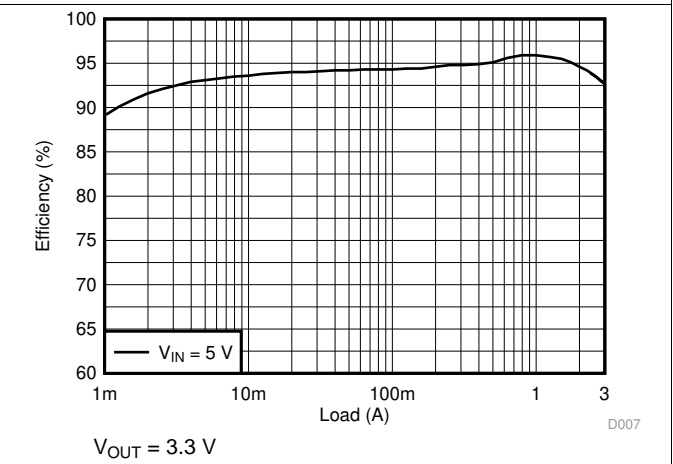


图 8. Efficiency

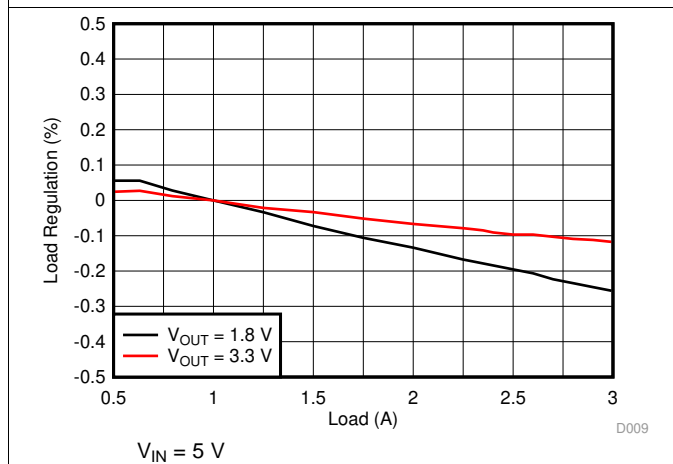


图 9. Load Regulation

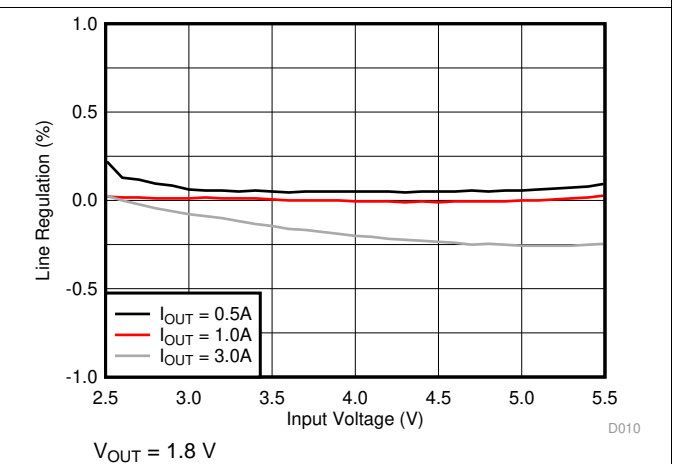
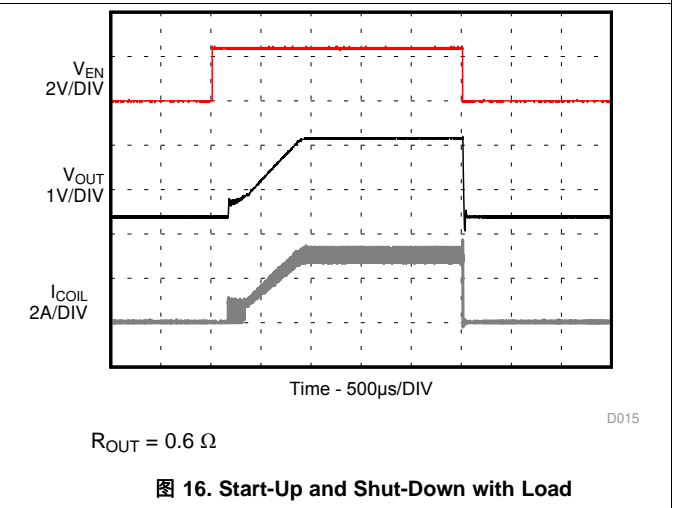
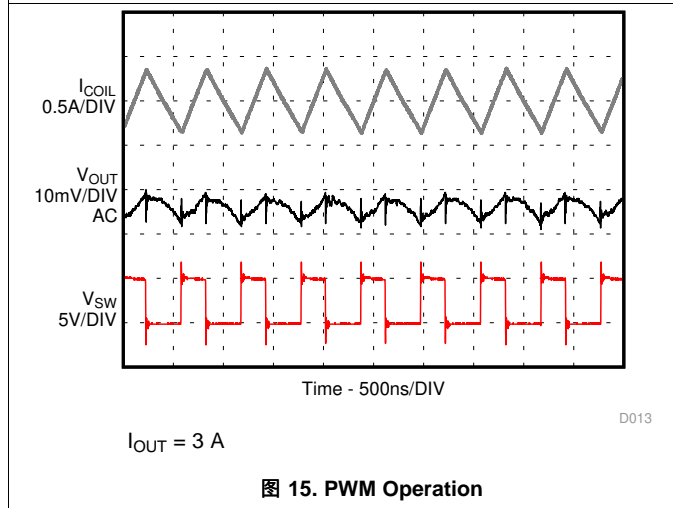
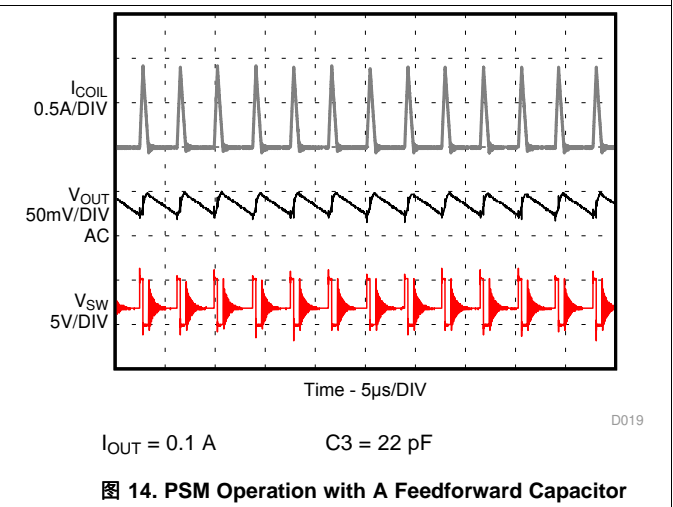
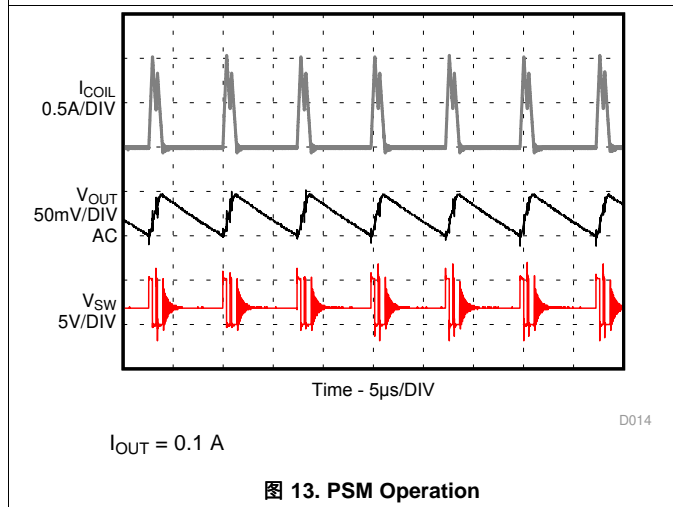
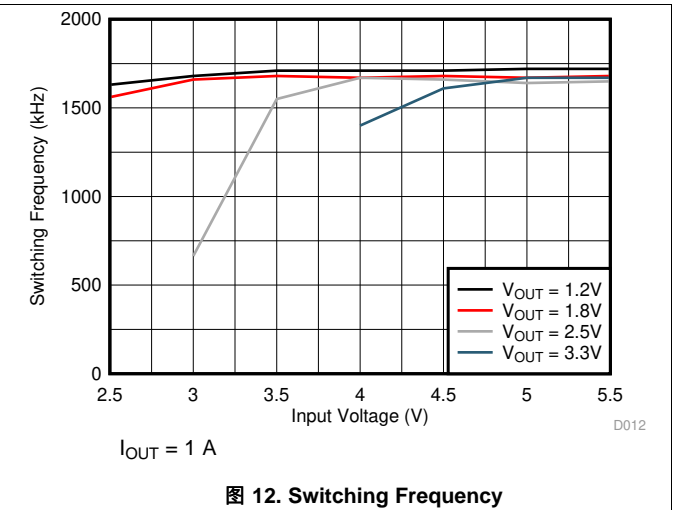
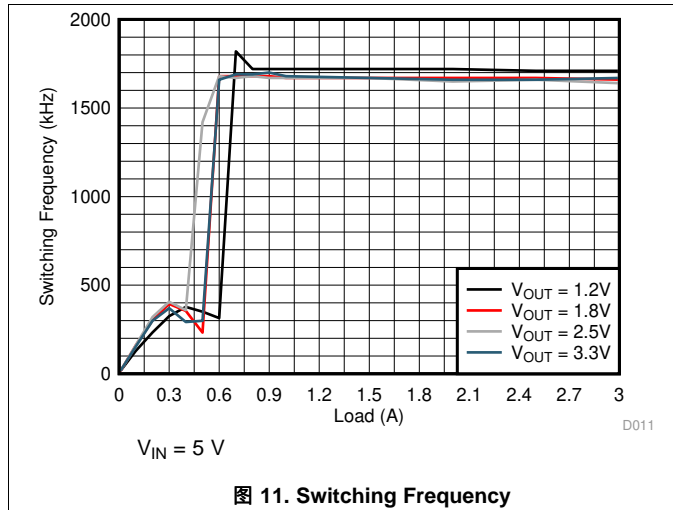
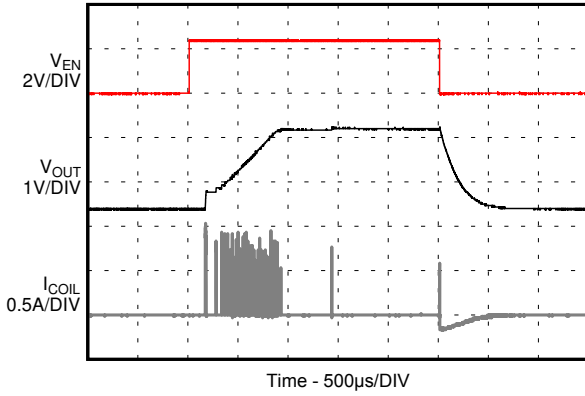


图 10. Line Regulation

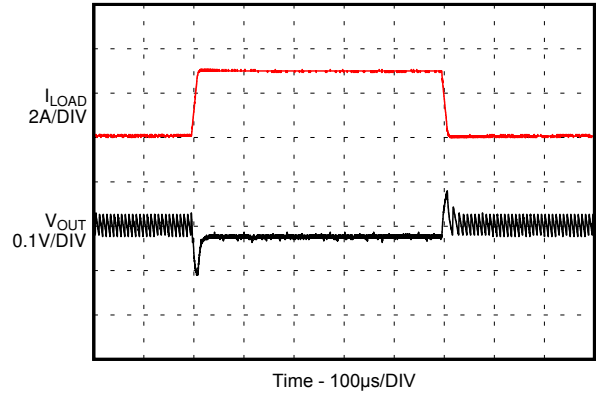




No Load

D016

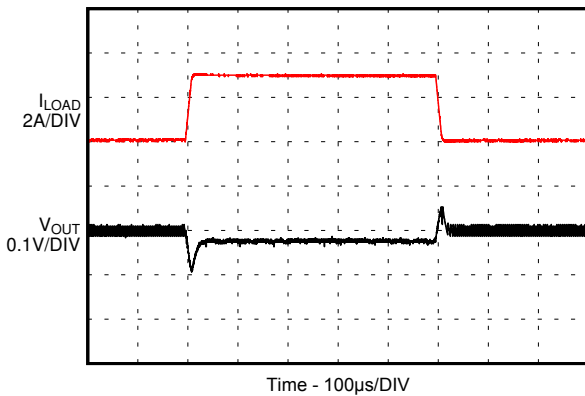
图 17. Start-Up and Shut-Down without Load



$I_{OUT} = 0.1 \text{ A to } 3 \text{ A}$

D017

图 18. Load Transient

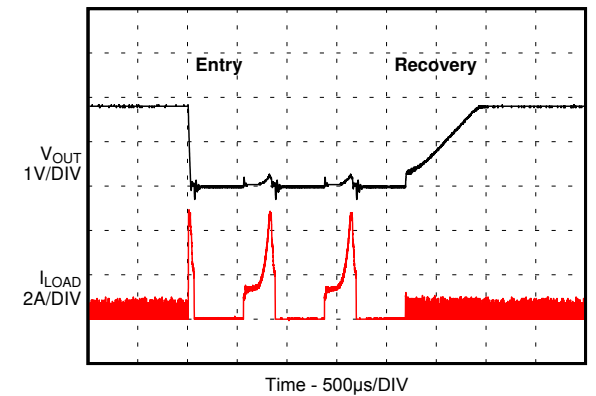


$I_{OUT} = 0.1 \text{ A to } 3 \text{ A}$

$C3 = 22 \text{ pF}$

D018

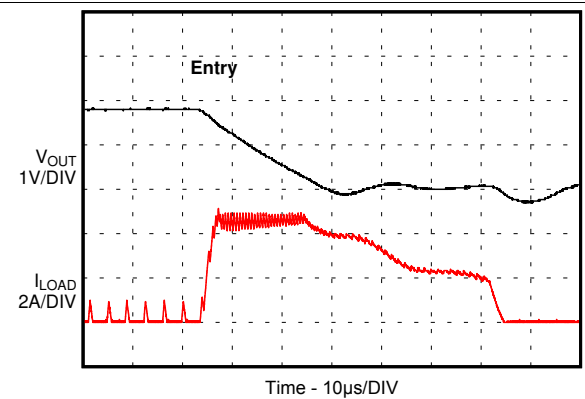
图 19. Load Transient with A Feedforward Capacitor



$I_{OUT} = 0.1 \text{ A}$

D020

图 20. Output Short Protection (HICCUP)



$I_{OUT} = 0.1 \text{ A}$

D021

图 21. Output Short Protection (HICCUP) - Zoom In

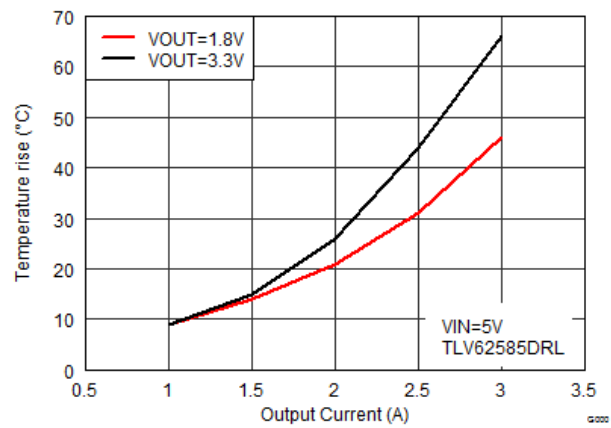


图 22. Temperature Rise of DRL Package on EVM

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

10 Layout

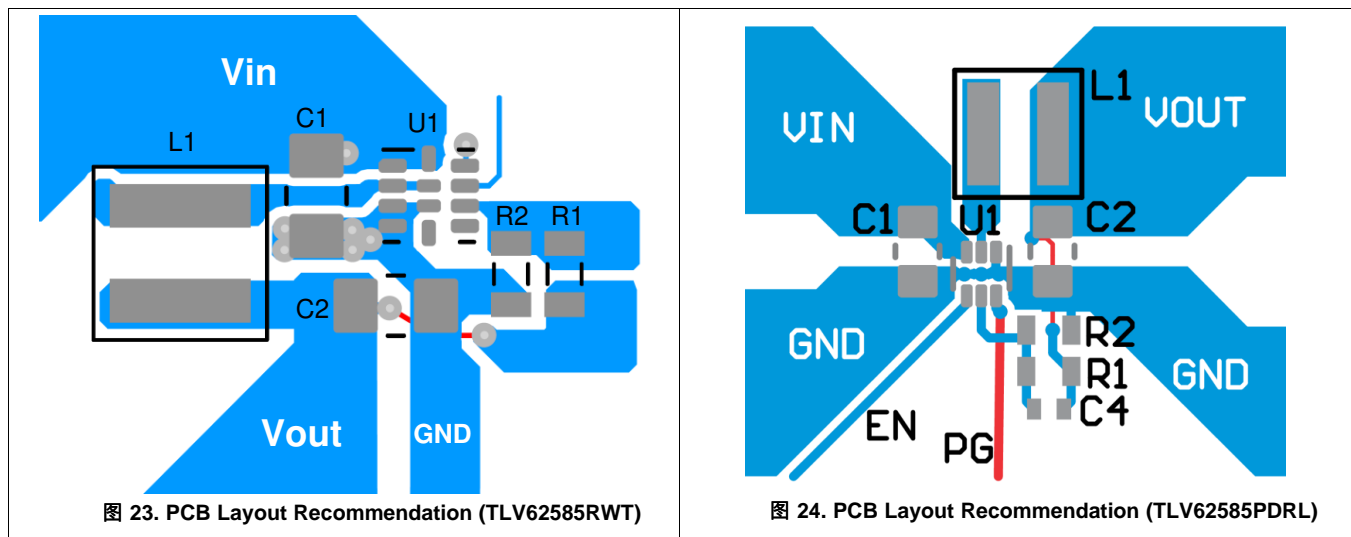
10.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TLV62585 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- A common ground should be used. GND layers might be used for shielding.

See [图 23](#) and [图 24](#) for the recommended PCB layout.

10.2 Layout Example



10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see: .

- *Thermal Characteristics Application Notes*, [SZZA017](#) and [SPRA953](#)

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.1.2 使用 WEBENCH® 工具创建定制设计方案

[单击此处](#)，使用 TLV62585 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- [《热工特性应用手册》](#)
- [《热工特性应用手册》](#)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 商标

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62585DRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BQ	Samples
TLV62585DRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BQ	Samples
TLV62585PDRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BP	Samples
TLV62585PDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BP	Samples
TLV62585RWTR	ACTIVE	VQFN-HR	RWT	12	3000	RoHS & Green	Call TI SN	Level-2-260C-1 YEAR	-40 to 125	17BI	Samples
TLV62585RWTT	ACTIVE	VQFN-HR	RWT	12	250	RoHS & Green	Call TI SN	Level-2-260C-1 YEAR	-40 to 125	17BI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62585DRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585DRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585RWTR	VQFN-HR	RWT	12	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV62585RWTR	VQFN-HR	RWT	12	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV62585RWTT	VQFN-HR	RWT	12	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV62585RWTT	VQFN-HR	RWT	12	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

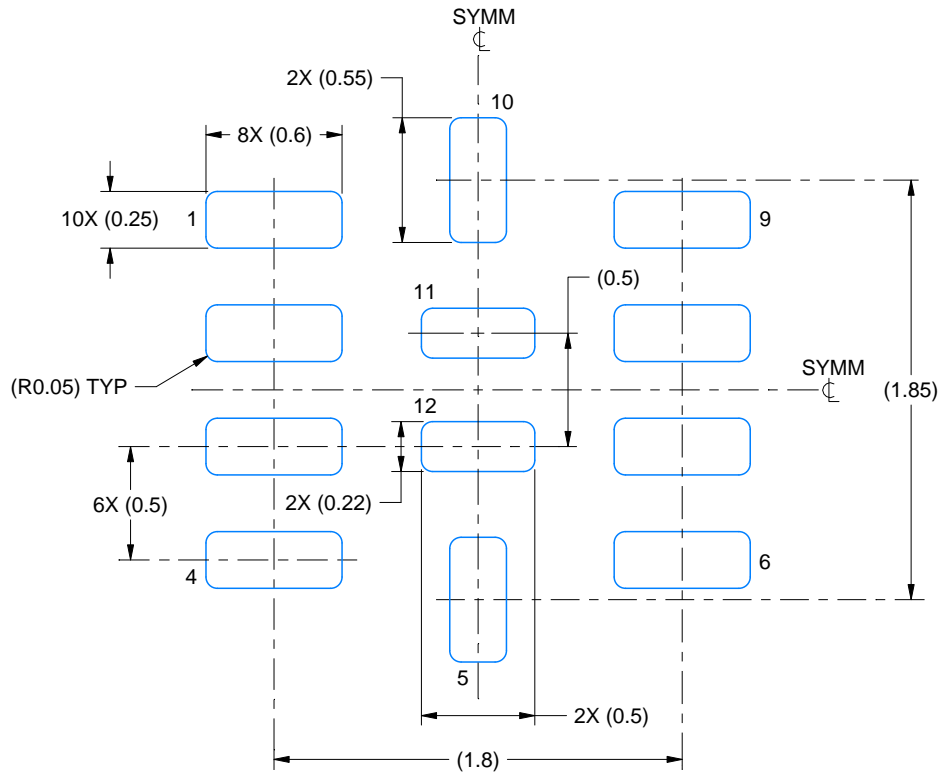
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62585DRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62585DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62585PDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62585PDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62585RWTR	VQFN-HR	RWT	12	3000	182.0	182.0	20.0
TLV62585RWTR	VQFN-HR	RWT	12	3000	210.0	185.0	35.0
TLV62585RWTT	VQFN-HR	RWT	12	250	182.0	182.0	20.0
TLV62585RWTT	VQFN-HR	RWT	12	250	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

RWT0012A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4223084/B 10/2018

NOTES: (continued)

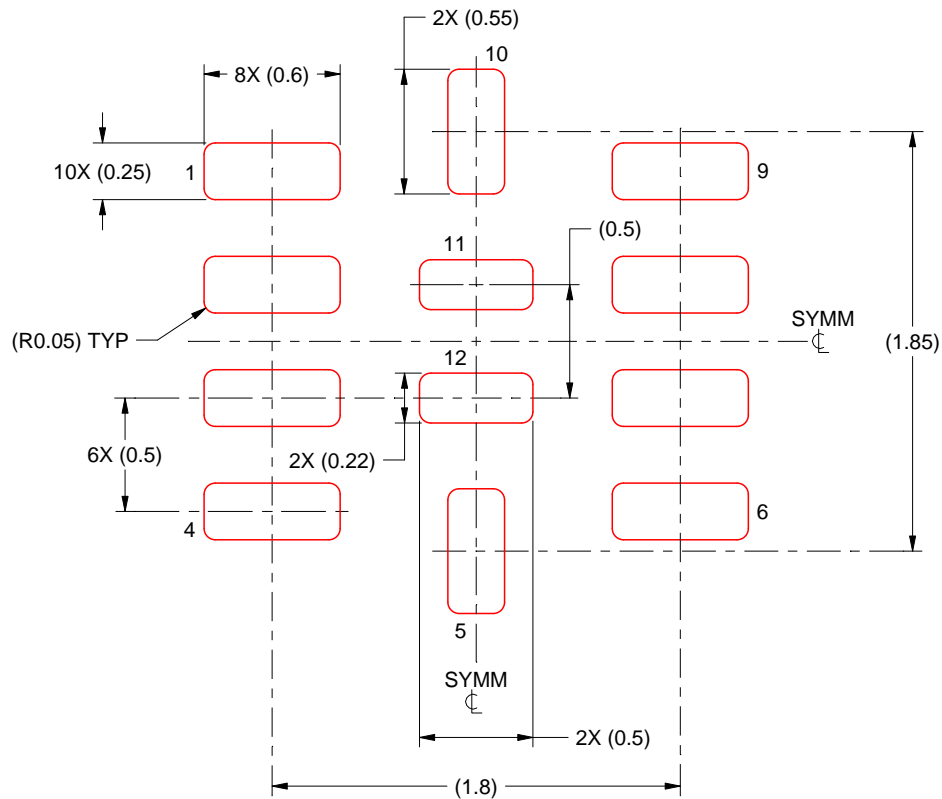
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RWT0012A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



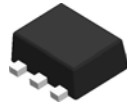
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223084/B 10/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

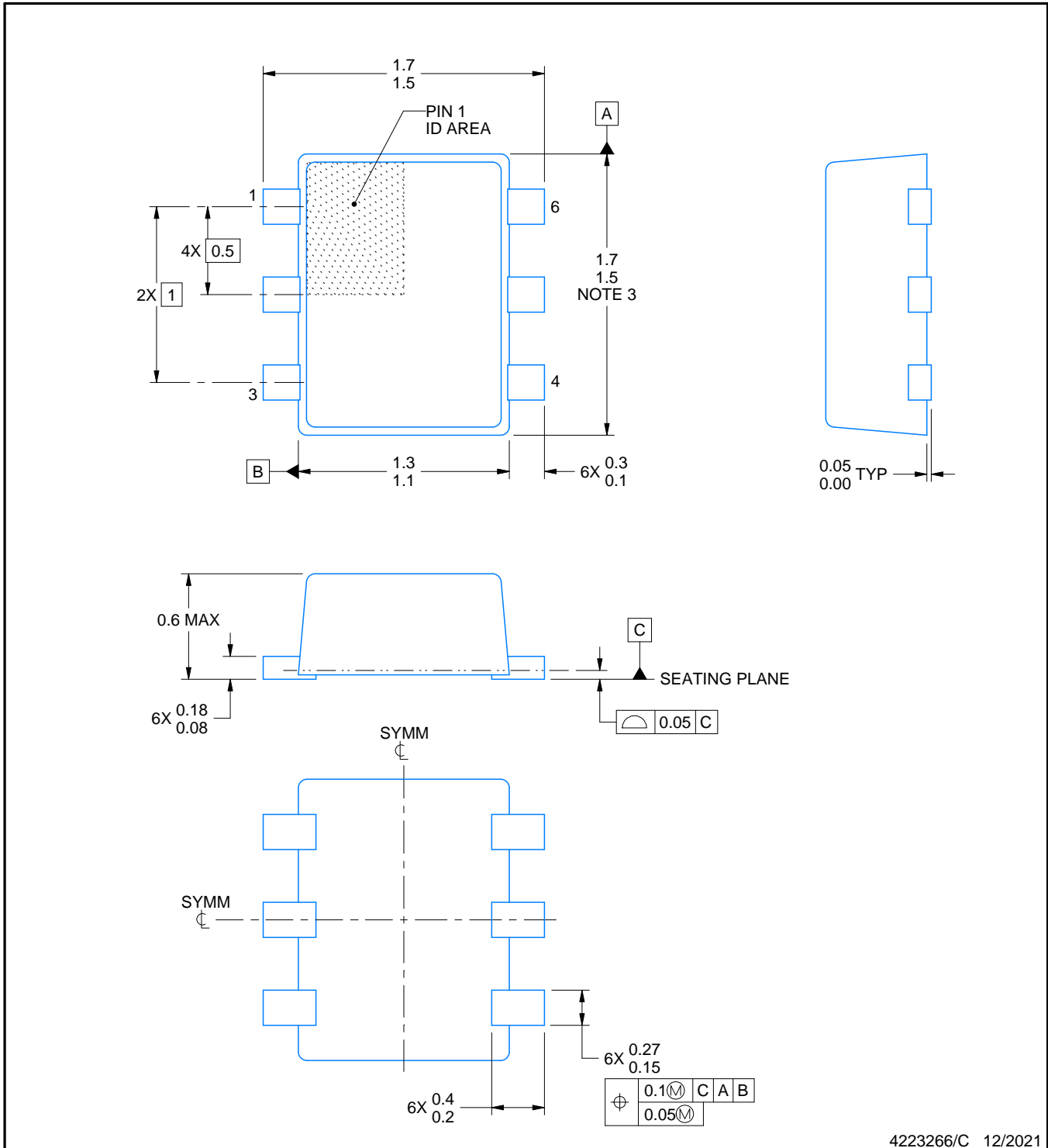
DRL0006A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/C 12/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

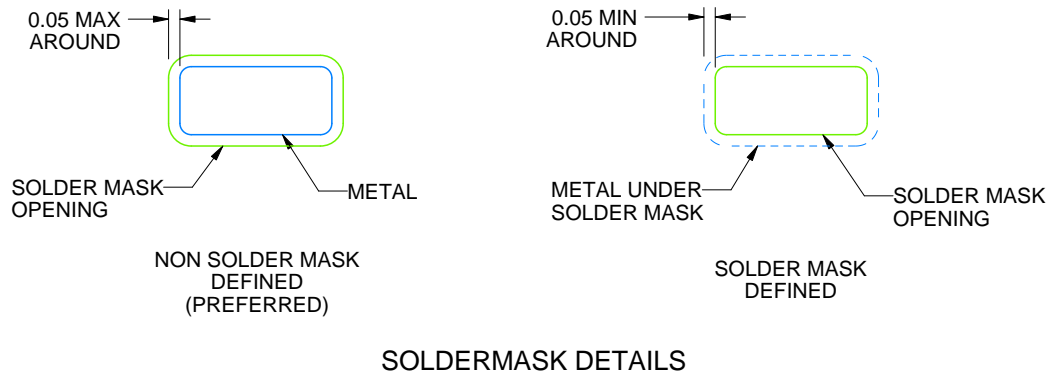
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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