LMK00304 3GHz 4 路输出 超低附加抖动差动时钟缓冲器/电平转换器

1 特性

- 3：1 输入多路复用器
  - 两个通用输入运行频率高达 3.1GHz，并且接受低电压正射极耦合逻辑 (LVPECL)，低压差分信令 (LVDS)，电流模式逻辑 (CML)，短截线串联端接逻辑 (SSTL), 高速收发器逻辑 (HSTL)，主机时钟信号电平 (HCSL) 或单端时钟
  - 一个晶体输入可接受 10MHz 至 40MHz 的晶体或单端时钟
- 共两组，每组均具有 2 路差动输出
  - LVPECL、LVDS、HCSL 或 Hi-Z（可选）
  - LMK03806 时钟源为 156.25MHz 时，LVPECL 附加抖动：
    - 20fs RMS（10kHz 至 1MHz）
    - 51fs RMS（12kHz 至 20MHz）
- 高 PSRR：156.25MHz 时为 -65/-76dBc (LVPECL/LVDS)
- 具有同步使能驶入的 LVCMOS 输出
- 由引脚控制的配置
- V_{CC}内核电源：3.3V ± 5%
- 3 个独立的 V_{CCO}输出电源：3.3V/2.5V ± 5%
- 工业温度范围：-40°C 至 +85°C
- 32 接线超薄型四方扁平无引线 (WQFN) 封装 (5mm x 5mm)

2 应用

- 针对模数转换器 (ADC)，数模转换器 (DAC)，多千兆以太网，XAUI，光纤通道，SATA/SAS，SONET/SDH，通用公共无线接口 (CPRI)，高频背板的时钟分配和电平转换
- 交换机、路由器、线路接口卡、定时卡
- 服务器，计算，PCI Express (PCIe 3.0)
- 远程无线电单元和基带单元

3 说明

LMK00304 是一款 3GHz、4 路输出差动扇出缓冲器，用于高频、低抖动时钟/数据分配和电平转换。可从两个通用输入或一个晶振输入中选择输入时钟。所选择的的输入时钟被分配到两组输出，每组输出包含 2 个差分输出和 1 个 LVCMOS 输出。两个差分输出组可一起被配置为 LVPECL、LVDS 或 HCSL 驱动器，或者被禁用。LVCMOS 输出具有同步使能输入，在使能或禁用后可实现无短脉冲运行。LMK00304 由一个 3.3V 内核电源和 3 个独立的 3.3V/2.5V 输出电源供电运行。

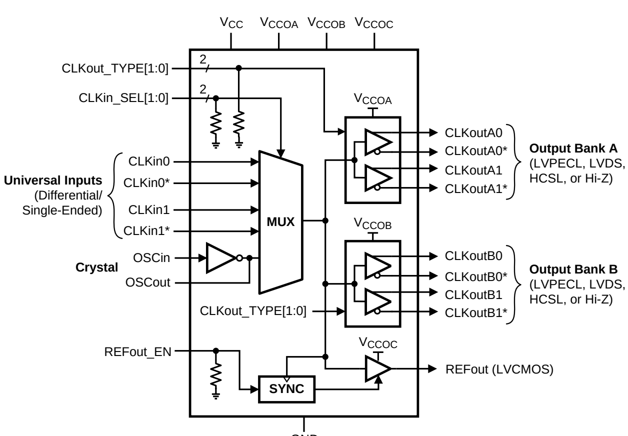
LMK00304 具有高性能、多用途和电源效率特性，这使得它成为替代固定输出缓冲器器件的理想选择，同时还能增加系统中的时序余裕。

器件信息[(1)]

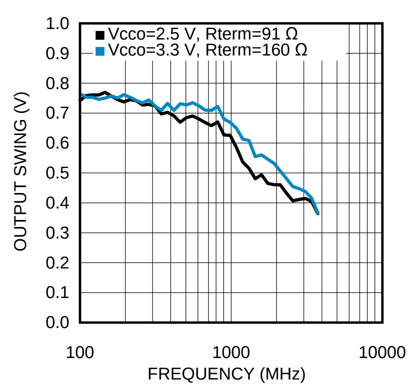
器件型号	封装	封装尺寸（标称值）
LMK00304	WQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

功能框图



LVPECL 输出摆幅 (V_{OD}) 与频率间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (March 2016) to Revision G	Page
• Added new rows to the *Thermal Information* table	6
• Added the *Support for PCB Temperature up to 105°C* section	32

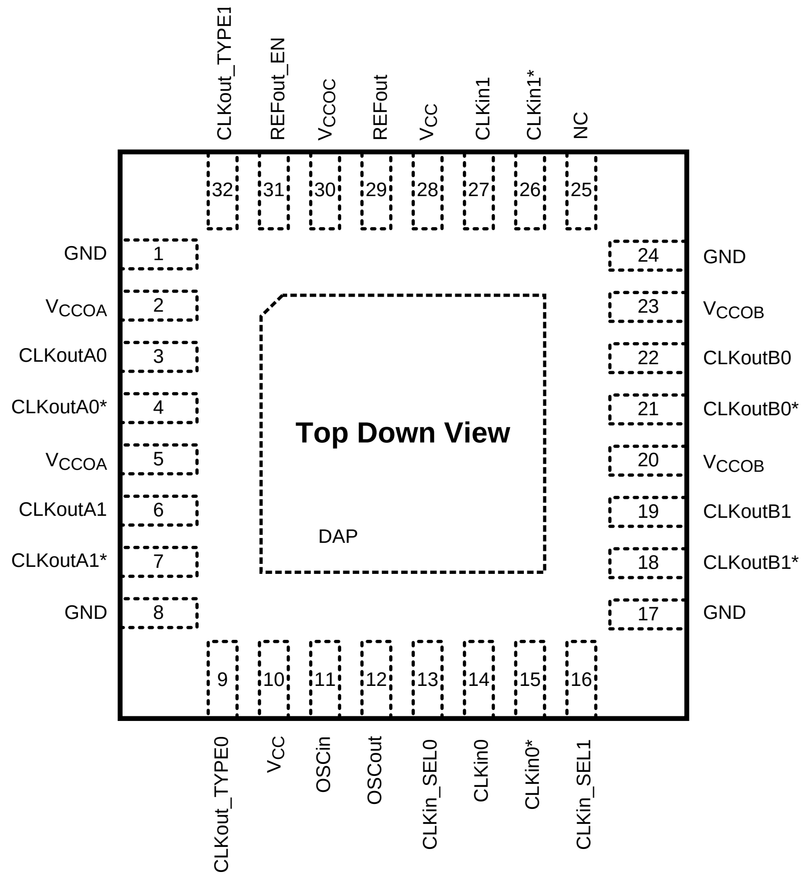
Changes from Revision E (May 2013) to Revision F	Page
• 已添加 "超低附加抖动"至文档标题	1
• 已添加、更新或重命名以下部分：*规范*；*详细 说明*；*应用和实施*；*电源相关建议*；*器件和文档支持*；*机械、封装和可订购信息*	1
• Changed Cin (typ) from 1 pF to 4 pF (based on updated test method) in *Electrical Characteristics: Crystal Interface*	8
• Added footnote for V_{I_SE} parameter in the *Electrical Characteristics* table.	8
• Added "Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz" parameter with 100 MHz and 156.25 MHz Test conditions, Typical values, Max values, and footnotes in Electrical Characteristics: LVPECL Outputs	9
• Added "Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz" parameter with 100 MHz and 156.25 MHz Test conditions, Typical values, Max values, and footnotes in Electrical Characteristics: LVDS Outputs	10
• Added new paragraph at end of *Driving the Clock Inputs*	22
• Changed "LMK00301" to "LMK00304" in Figure 27 and Figure 28	23
• Changed Cin = 4 pF (typ, based on updated test method) in *Crystal Interface*	23
• Added POWER SUPPLY SEQUENCING	29

Changes from Revision D (February 2013) to Revision E	Page
• Changed V_{CM} text to condition for V_{IH} to V_{CM} parameter group.	8
• Deleted V_{IH} min value from Electrical Characteristics table.	8
• Deleted V_{IL} max value from Electrical Characteristics table.	8
• Added V_{I_SE} parameter and spec limits with corresponding table note to Electrical Characteristics Table.	8
• Changed third paragraph in *Driving the Clock Inputs section* to include CLKin* and LVCMOS text. Revised to better	

correspond with information in Electrical Characteristics Table. 22
- Changed bypass cap text to signal attenuation text of the fourth paragraph in *Driving the Clock Inputs* section. 22
- Changed *Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing* image with revised graphic. 23
- Added text to second paragraph of *Termination for AC Coupled Differential Operation* to explain graphic update to *Differential LVDS Operation with AC Coupling to Receivers.* 26
- Changed graphic for *Differential LVDS Operation, AC Coupling, No Biasing by the Receiver* and updated caption. 26

5 Pin Configuration and Functions

32-Pin WQFN
Package RTV0032A
Top View



Pin Functions[1]

PIN		TYPE	DESCRIPTION
NO.	NAME		
DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
1, 8 17, 24	GND	GND	Ground
2, 5	V_{CCOA}	PWR	Power supply for Bank A Output buffers. V_{CCOA} operates from 3.3 V or 2.5 V. The V_{CCOA} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. [2]
3, 4	CLKoutA0, CLKoutA0*	O	Differential clock output A0. Output type set by CLKout_TYPE pins.
6, 7	CLKoutA1, CLKoutA1*	O	Differential clock output A1. Output type set by CLKout_TYPE pins.
9, 32	CLKout_TYPE0, CLKout_TYPE1	I	Bank A and Bank B output buffer type selection pins [3]
10, 28	Vcc	PWR	Power supply for Core and Input Buffer blocks. The Vcc supply operates from 3.3 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcc pin.
11	OSCin	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
12	OSCout	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
13, 16	CLKin_SEL0, CLKin_SEL1	I	Clock input selection pins [3]
14, 15	CLKin0, CLKin0*	I	Universal clock input 0 (differential/single-ended)
18, 19	CLKoutB1*, CLKoutB1	O	Differential clock output B1. Output type set by CLKout_TYPE pins.
20, 23	V_{CCOB}	PWR	Power supply for Bank B Output buffers. V_{CCOB} operates from 3.3 V or 2.5 V. The V_{CCOB} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. See *Absolute Maximum Ratings*
21, 22	CLKoutB0*, CLKoutB0	O	Differential clock output B0. Output type set by CLKout_TYPE pins.
25	NC	—	Not connected internally. Pin may be floated, grounded, or otherwise tied to any potential within the Supply Voltage range stated in the *Absolute Maximum Ratings* .
26, 27	CLKin1*, CLKin1	I	Universal clock input 1 (differential/single-ended)
29	REFout	O	LVCMOS reference output. Enable output by pulling REFout_EN pin high.
30	V_{CCOC}	PWR	Power supply for REFout buffer. V_{CCOC} operates from 3.3 V or 2.5 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. [2]
31	REFout_EN	I	REFout enable input. Enable signal is internally synchronized to selected clock input. [3]

(1) Any unused output pins should be left floating with minimum copper length (see note in *Clock Outputs*), or properly terminated if connected to a transmission line, or disabled/Hi-Z if possible. See *Clock Outputs* for output configuration and *Termination and Use of Clock Drivers* for output interface and termination techniques.
(2) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
(3) CMOS control input with internal pull-down resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}, V_{CCO}	Supply Voltages	-0.3	3.6	V
V_{IN}	Input Voltage	-0.3	(V_{CC} + 0.3)	V
T_{STG}	Storage Temperature Range	-65	+150	°C
T_L	Lead Temperature (solder 4 s)		+260	°C
T_J	Junction Temperature		+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Machine model (MM)	±150	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
T_A	Ambient Temperature Range	-40	25	85	°C
T_J	Junction Temperature			125	°C
V_{CC}	Core Supply Voltage Range	3.15	3.3	3.45	V
V_{CCO}	Output Supply Voltage Range (1)(2)	3.3 – 5% 2.5 – 5%	3.3 2.5	3.3 + 5% 2.5 + 5%	V

(1) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
(2) Vcco for any output bank should be less than or equal to Vcc (Vcco ≤ Vcc).

6.4 Thermal Information

THERMAL METRIC (1)		LMK00304 RTV0032A (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION(3)							
I_{CC_CORE}	Core Supply Current, All Outputs Disabled	CLKinX selected			8.5	10.5	mA
		OSCin selected			10	13.5	mA
I_{CC_PECL}	Additive Core Supply Current, LVPECL Banks Enabled				38	48	mA
I_{CC_LVDS}	Additive Core Supply Current, LVDS Banks Enabled				43	52	mA
I_{CC_HCSL}	Additive Core Supply Current, HCSL Banks Enabled				50	58.5	mA
I_{CC_CMOS}	Additive Core Supply Current, LVCMOS Output Enabled				3.5	5.5	mA
I_{CCO_PECL}	Additive Output Supply Current, LVPECL Banks Enabled	Includes Output Bank Bias and Load Currents for both banks, R_T = 50 Ω to Vcco – 2 V on all outputs			135	163	mA
I_{CCO_LVDS}	Additive Output Supply Current, LVDS Banks Enabled				25	34.5	mA
I_{CCO_HCSL}	Additive Output Supply Current, HCSL Banks Enabled	Includes Output Bank Bias and Load Currents for both banks, R_T = 50 Ω on all outputs			65	81.5	mA
I_{CCO_CMOS}	Additive Output Supply Current, LVCMOS Output Enabled	200 MHz, C_L = 5 pF	Vcco = 3.3 V ± 5%		9	10	mA
			Vcco = 2.5 V ± 5%		7	8	mA
POWER SUPPLY RIPPLE REJECTION (PSRR)							
$PSRR_{PECL}$	Ripple-Induced Phase Spur Level Differential LVPECL Output(4)	100 kHz, 100 mVpp Ripple Injected on Vcco, Vcco = 2.5 V	156.25 MHz		–65		dBc
			312.5 MHz		–63		
$PSRR_{LVDS}$	Ripple-Induced Phase Spur Level Differential LVDS Output(4)		156.25 MHz		–76		dBc
			312.5 MHz		–74		
$PSRR_{HCSL}$	Ripple-Induced Phase Spur Level Differential HCSL Output(4)		156.25 MHz		–72		dBc
			312.5 MHz		–63		
CMOS CONTROL INPUTS (CLKin_SELn, CLKout_TYPEn, REFout_EN)							
V_{IH}	High-Level Input Voltage			1.6		Vcc	V
V_{IL}	Low-Level Input Voltage			GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = Vcc, Internal pulldown resistor				50	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V, Internal pulldown resistor		-5	0.1		µA

(1) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) See *Power Supply Recommendations* for more information on current consumption and power dissipation calculations.
(4) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = $[\,(2 \times 10^{(PSRR\,/\,20)}) / (\pi \times f_{CLK})\,] \times$ 1E12

Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLOCK INPUTS (CLKin0/CLKin0*, CLKin1/CLKin1*)							
f_{CLKin}	Input Frequency Range (5)	Functional up to 3.1 GHz Output frequency range and timing specified per output type (refer to LVPECL, LVDS, HCSL, LVCMOS output specifications)		DC		3.1	GHz
V_{IHD}	Differential Input High Voltage	CLKin driven differentially				Vcc	V
V_{ILD}	Differential Input Low Voltage	CLKin driven differentially		GND			V
V_{ID}	Differential Input Voltage Swing (6)	CLKin driven differentially		0.15		1.3	V
V_{CMD}	Differential Input Common Mode Voltage	V_{ID} = 150 mV		0.25		Vcc – 1.2	V
		V_{ID} = 350 mV		0.25		Vcc – 1.1	V
		V_{ID} = 800 mV		0.25		Vcc – 0.9	V
V_{IH}	Single-Ended Input High Voltage	CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within V_{CM} range				Vcc	V
V_{IL}	Single-Ended Input Low Voltage			GND			V
V_{I_SE}	Single-Ended Input Voltage Swing (7) (8)			0.3		2	Vpp
V_{CM}	Single-Ended Input Common Mode Voltage			0.25		Vcc – 1.2	V
ISO_{MUX}	Mux Isolation, CLKin0 to CLKin1	f_{OFFSET} > 50 kHz, P_{CLKinX} = 0 dBm	f_{CLKin0} = 100 MHz		–84		dBc
			f_{CLKin0} = 200 MHz		–82		dBc
			f_{CLKin0} = 500 MHz		–71		dBc
			f_{CLKin0} = 1000 MHz		–65		dBc
CRYSTAL INTERFACE (OSCin, OSCout)							
F_{CLK}	External Clock Frequency Range (5)	OSCin driven single-ended, OSCout floating				250	MHz
F_{XTAL}	Crystal Frequency Range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) (9)		10		40	MHz
C_{IN}	OSCin Input Capacitance				4		pF

(5) Specification is ensured by characterization and is not tested in production.
(6) See *Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.
(7) Parameter is specified by design, not tested in production.
(8) For clock input frequency ≥ 100 MHz, CLKinX can be driven with single-ended (LVCMOS) input swing up to 3.3 Vpp. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 Vpp max to prevent input saturation (refer to *Driving the Clock Inputs* for interfacing 2.5 V/3.3 V LVCMOS clock input < 100 MHz to CLKinX).
(9) The ESR requirements stated must be met to ensure that the oscillator circuitry has no startup issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal. Refer to *Crystal Interface* for crystal drive level considerations.

Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVPECL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing (5) (10)	V_{OD} ≥ 600 mV, R_L = 100=Ω differential	Vcco = 3.3 V ± 5%, R_T = 160 Ω to GND	1.0	1.2		GHz
			Vcco = 2.5 V ± 5%, R_T = 91 Ω to GND	0.75	1		
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing (5) (10)	V_{OD} ≥ 400 mV, R_L = 100-Ω differential	Vcco = 3.3 V ± 5%, R_T = 160 Ω to GND	1.5	3.1		GHz
			Vcco = 2.5 V ± 5%, R_T = 91 Ω to GND	1.5	2.3		
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz (5) (11) (12)	Vcco = 2.5 V ± 5%: R_T = 91 Ω to GND, Vcco = 3.3 V ± 5%: R_T = 160 Ω to GND, R_L = 100-Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		77	98	fs
			CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns		54	78	
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (11)	Vcco = 3.3 V, R_T = 160 Ω to GND, R_L = 100-Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		59		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		64		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		30		
$Jitter_{ADD}$	Additive RMS Jitter with LVPECL clock source from LMK03806 (11) (13)	Vcco = 3.3 V, R_T = 160 Ω to GND, R_L = 100-Ω differential	CLKin: 156.25 MHz, J_{SOURCE} = 190 fs RMS (10 kHz to 1 MHz)		20		fs
			CLKin: 156.25 MHz, J_{SOURCE} = 195 fs RMS (12 kHz to 20 MHz)		51		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz (14) (15)	Vcco = 3.3 V, R_T = 160 Ω to GND, R_L = 100 Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		–162.5		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		–158.1		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		–154.4		
DUTY	Duty Cycle (5)	50% input clock duty cycle		45%		55%	
V_{OH}	Output High Voltage	T_A = 25°C, DC Measurement, R_T = 50 Ω to Vcco - 2 V		Vcco – 1.2	Vcco – 0.9	Vcco – 0.7	V
V_{OL}	Output Low Voltage			Vcco – 2	Vcco – 1.75	Vcco – 1.5	V
V_{OD}	Output Voltage Swing (6)			600	830	1000	mV

(10) See *Typical Characteristics* for output operation over frequency.
(11) For the 100 MHz and 156.25 MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method #1: $J_{ADD} = SQRT(J_{OUT}^2 – J_{SOURCE}^2)$, where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKin. For the 625 MHz clock input condition, Additive RMS Jitter is approximated using Method #2: $J_{ADD} = SQRT(2 \times 10^{dBc/10}) / (2 \times \pi \times f_{CLK})$, where dBc is the phase noise power of the Output Noise Floor integrated from 1 to 20 MHz bandwidth. The phase noise power can be calculated as: dBc = Noise Floor + 10 × log_{10}(20 MHz – 1 MHz). The additive RMS jitter was approximated for 625 MHz using Method #2 because the RMS jitter of the clock source was not sufficiently low enough to allow practical use of Method #1. Refer to the "Noise Floor vs. CLKin Slew Rate" and "RMS Jitter vs. CLKin Slew Rate" plots in *Typical Characteristics*.
(12) 100-MHz and 156.25-MHz input source from Rohde & Schwarz SMA100A Low-Noise Signal Generator and Sine-to-Square-wave Conversion block.
(13) 156.25-MHz LVPECL clock source from LMK03806 with 20-MHz crystal reference (crystal part number: ECS-200-20-30BU-DU). J_{SOURCE} = 190 fs RMS (10 kHz to 1 MHz) and 195 fs RMS (12 kHz to 20 MHz). Refer to the LMK03806 datasheet for more information.
(14) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations.
(15) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, TI recommends using the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_R	Output Rise Time 20% to 80%(7)	R_T = 160 Ω to GND, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R_L = 100-Ω differential C_L ≤ 5 pF			175	300	ps
t_F	Output Fall Time 80% to 20%(7)				175	300	ps
LVDS OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing (5)(10)	V_{OD} ≥ 250 mV, R_L = 100-Ω differential		1.0	1.6		GHz
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing(5)(10)	V_{OD} ≥ 200 mV, R_L = 100-Ω differential		1.5	2.1		GHz
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz (5)(11)(12)	R_L = 100-Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		94	115	fs
			CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns		70	90	
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz(11)	Vcco = 3.3 V, R_L = 100-Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		89		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		77		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		37		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz(14)(15)	Vcco = 3.3 V, R_L = 100-Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		–159.5		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		–157		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		–152.7		
DUTY	Duty Cycle(5)	50% input clock duty cycle		45%		55%	
V_{OD}	Output Voltage Swing(6)	T_A = 25°C, DC Measurement, R_L = 100-Ω differential		250	400	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States			–50		50	mV
V_{OS}	Output Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States			–35		35	mV
I_{SA} I_{SB}	Output Short Circuit Current Single Ended	T_A = 25°C, Single-ended outputs shorted to GND		–24		24	mA
I_{SAB}	Output Short Circuit Current Differential	Complementary outputs tied together		–12		12	mA
t_R	Output Rise Time 20% to 80%(7)	Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 100 Ω differential, C_L ≤ 5 pF			175	300	ps
t_F	Output Fall Time 80% to 20%(7)				175	300	ps

Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HCSL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout}	Output Frequency Range(5)	R_L = 50 Ω to GND, C_L ≤ 5 pF		DC		400	MHz
$Jitter_{ADD\_PCIe}$	Additive RMS Phase Jitter for PCIe 3.0(5)	PCIe Gen 3, PLL BW = 2–5 MHz, CDR = 10 MHz	CLKin: 100 MHz, Slew rate ≥ 0.6 V/ns		0.03	0.15	ps
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz(11)	Vcco = 3.3 V, R_T = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		77		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		86		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz(14)(15)	Vcco = 3.3 V, R_T = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		–161.3		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		–156.3		
DUTY	Duty Cycle(5)	50% input clock duty cycle		45%		55%	
V_{OH}	Output High Voltage	T_A = 25°C, DC Measurement, R_T = 50 Ω to GND		520	810	920	mV
V_{OL}	Output Low Voltage			–150	0.5	150	mV
V_{CROSS}	Absolute Crossing Voltage(5)(16)	R_L = 50 Ω to GND, C_L ≤ 5 pF		250	350	460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS}(5)(16)					140	mV
t_R	Output Rise Time 20% to 80%(7)(16)	250 MHz, Unifrom transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 50 Ω to GND, C_L ≤ 5 pF			300	500	ps
t_F	Output Fall Time 80% to 20%(7)(16)				300	500	ps

(16) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.

Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS OUTPUT (REFout)							
f_{CLKout}	Output Frequency Range (5)	C_L ≤ 5 pF		DC		250	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (11)	Vcco = 3.3 V, C_L ≤ 5 pF	100 MHz, Input Slew rate ≥ 3 V/ns		95		fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz (14) (15)	Vcco = 3.3 V, C_L ≤ 5 pF	100 MHz, Input Slew rate ≥ 3 V/ns		–159.3		dBc/Hz
DUTY	Duty Cycle (5)	50% input clock duty cycle		45%		55%	
V_{OH}	Output High Voltage	1-mA load		Vcco – 0.1			V
V_{OL}	Output Low Voltage					0.1	V
I_{OH}	Output High Current (Source)	Vo = Vcco / 2	Vcco = 3.3 V		28		mA
			Vcco = 2.5 V		20		
I_{OL}	Output Low Current (Sink)		Vcco = 3.3 V		28		mA
			Vcco = 2.5 V		20		
t_R	Output Rise Time 20% to 80% (7) (16)	250 MHz, Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 50 Ω to GND, C_L ≤ 5 pF			225	400	ps
t_F	Output Fall Time 80% to 20% (7) (16)				225	400	ps
t_{EN}	Output Enable Time (17)	C_L ≤ 5 pF				3	cycles
t_{DIS}	Output Disable Time (17)					3	cycles

(17) Output Enable Time is the number of input clock cycles it takes for the output to be enabled after REFout_EN is pulled high. Similarly, Output Disable Time is the number of input clock cycles it takes for the output to be disabled after REFout_EN is pulled low. The REFout_EN signal should have an edge transition much faster than that of the input clock period for accurate measurement.

Electrical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1) (2)

		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PROPAGATION DELAY and OUTPUT SKEW							
t_{PD_PECL}	Propagation Delay CLKin-to-LVPECL(7)	R_T = 160 Ω to GND, R_L = 100-Ω differential, C_L ≤ 5 pF		180	360	540	ps
t_{PD_LVDS}	Propagation Delay CLKin-to-LVDS(7)	R_L = 100-Ω differential, C_L ≤ 5 pF		200	400	600	ps
t_{PD_HCSL}	Propagation Delay CLKin-to-HCSL(7)(16)	R_T = 50 Ω to GND, C_L ≤ 5 pF		295	590	885	ps
t_{PD_CMOS}	Propagation Delay CLKin-to-LVCMOS(7)(16)	C_L ≤ 5 pF	Vcco = 3.3 V	900	1475	2300	ps
			Vcco = 2.5 V	1000	1550	2700	
$t_{SK(O)}$	Output Skew LVPECL/LVDS/HCSL (5)(16)(18)	Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications.			30	50	ps
$t_{SK(PP)}$	Part-to-Part Output Skew LVPECL/LVDS/HCSL (7)(16)(18)				80	120	ps

(18) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

6.6 Typical Characteristics

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Consult Table 1 at the end of the *Typical Characteristics* section for graph notes.

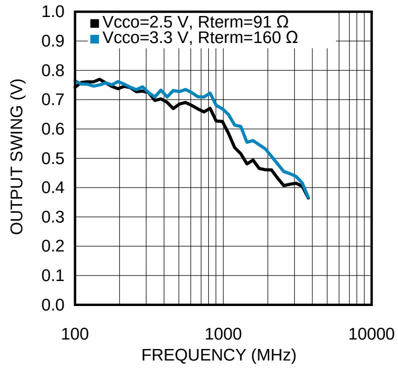


Figure 1. LVPECL Output Swing (V_{OD}) vs. Frequency

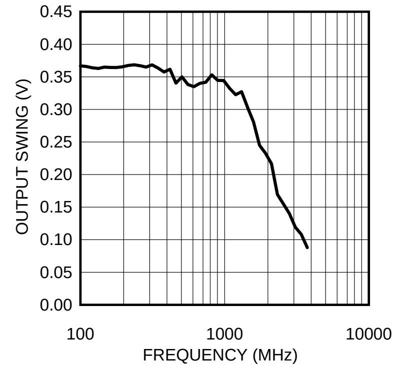


Figure 2. LVDS Output Swing (V_{OD}) vs. Frequency

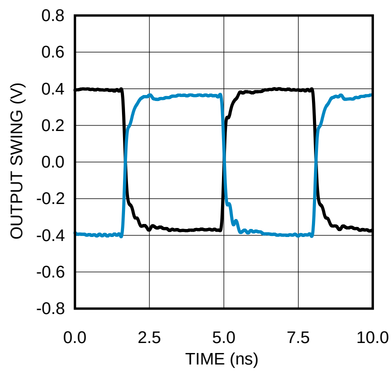


Figure 3. LVPECL Output Swing at 156.25 MHz

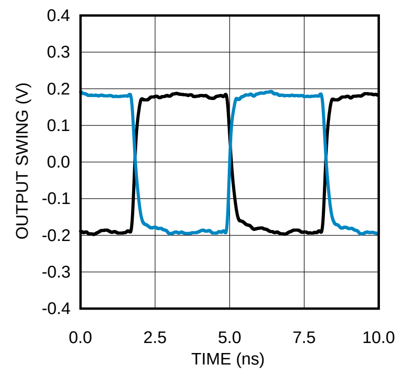


Figure 4. LVDS Output Swing at 156.25 MHz

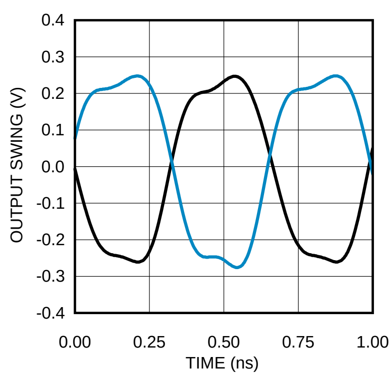


Figure 5. LVPECL Output Swing at 1.5 GHz

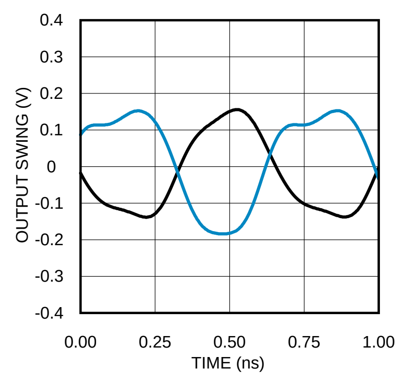


Figure 6. LVDS Output Swing at 1.5 GHz

Typical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Consult Table 1 at the end of the *Typical Characteristics* section for graph notes.

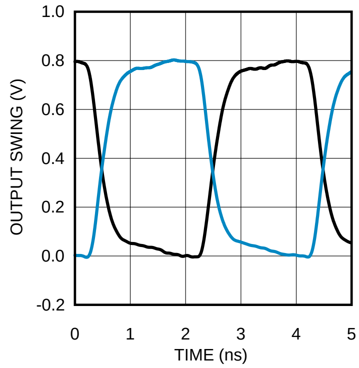


Figure 7. HCSL Output Swing at 250 MHz

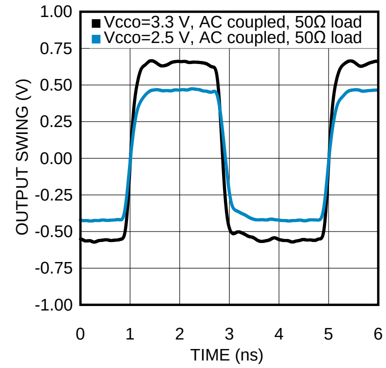


Figure 8. LVCMOS Output Swing at 250 MHz

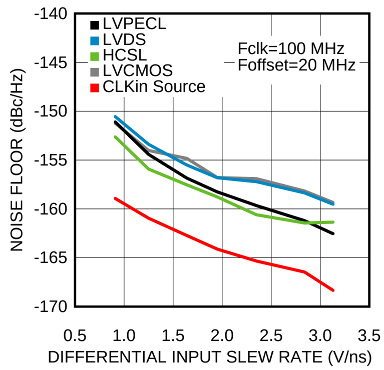


Figure 9. Noise Floor vs. CLKin Slew Rate at 100 MHz

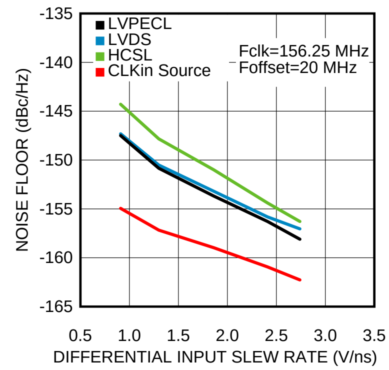


Figure 10. Noise Floor vs. CLKin Slew Rate at 156.25 MHz

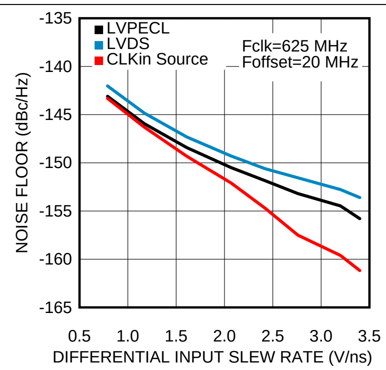
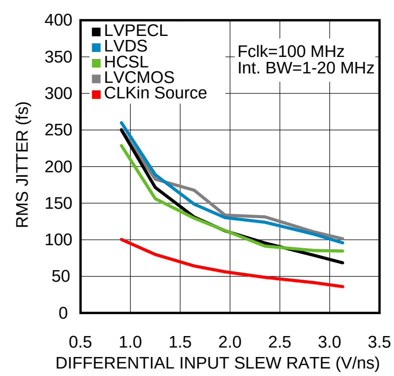


Figure 11. Noise Floor vs. CLKin Slew Rate at 625 MHz

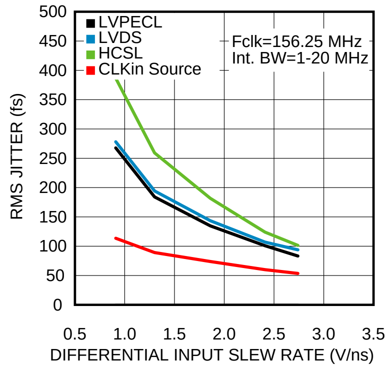


See Note 1 in Graph Notes table

Figure 12. RMS Jitter vs. CLKin Slew Rate at 100 MHz

Typical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Consult Table 1 at the end of the *Typical Characteristics* section for graph notes.



See Note 1 in Graph Notes table

Figure 13. RMS Jitter vs. CLKin Slew Rate at 156.25 MHz

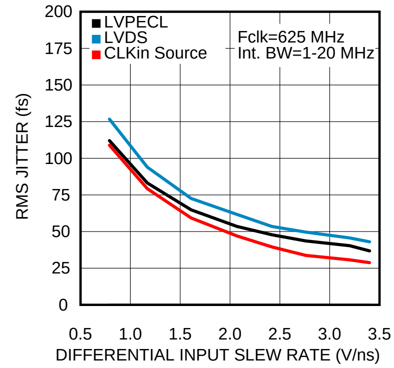


Figure 14. RMS Jitter vs. CLKin Slew Rate at 625 MHz

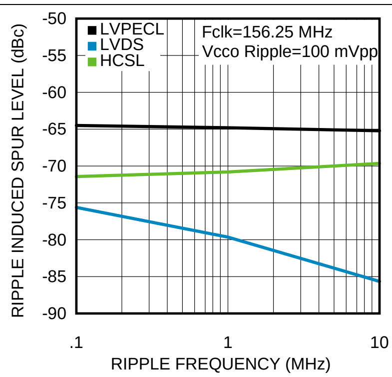


Figure 15. PSRR vs. Ripple Frequency at 156.25 MHz

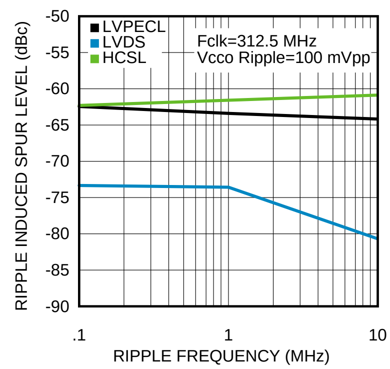


Figure 16. PSRR vs. Ripple Frequency at 312.5 MHz

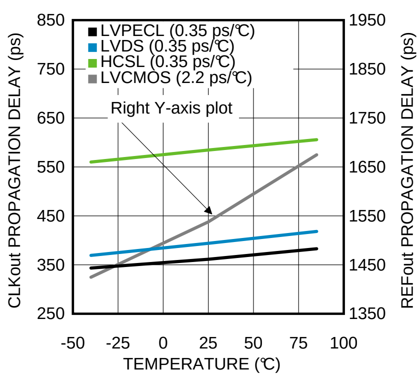
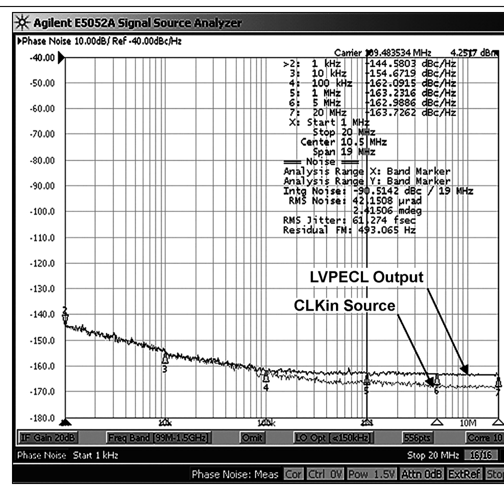


Figure 17. Propagation Delay vs. Temperature

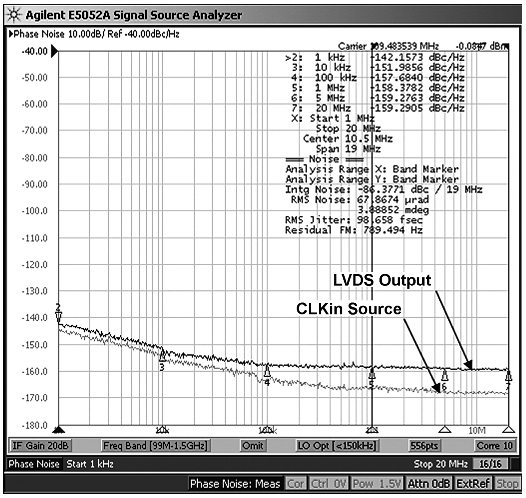


See Note 1 in Graph Notes table

Figure 18. LVPECL Phase Noise at 100 MHz

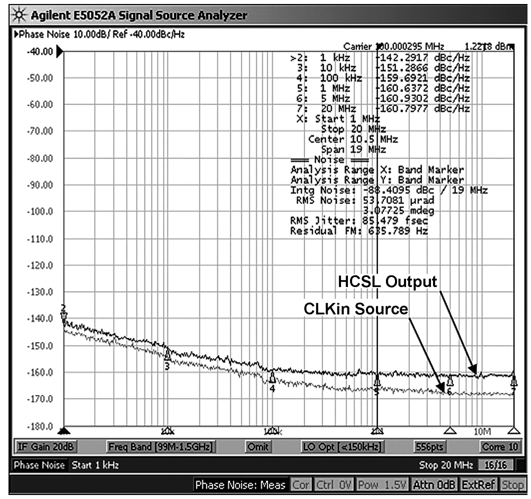
Typical Characteristics (continued)

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Consult Table 1 at the end of the *Typical Characteristics* section for graph notes.



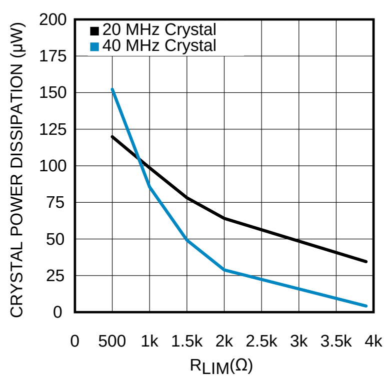
See Note 1 in Graph Notes table

Figure 19. LVDS Phase Noise at 100 MHz



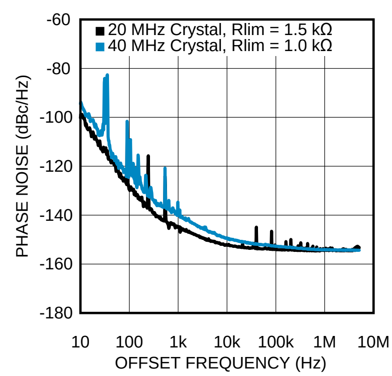
See Note 1 in Graph Notes table

Figure 20. HCSL Phase Noise at 100 MHz



See Notes 2 and 3 in Graph Notes table

Figure 21. Crystal Power Dissipation vs. R_{LIM}



See Notes 2 and 3 in Graph Notes table

Figure 22. LVDS Phase Noise in Crystal Mode

Table 1. Graph Notes

NOTE	
(1)	The typical RMS jitter values in the plots show the total output RMS jitter (J_{OUT}) for each output buffer type and the source clock RMS jitter (J_{SOURCE}). From these values, the Additive RMS Jitter can be calculated as: J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2).
(2)	20 MHz crystal characteristics: Abracon ABL series, AT cut, C_L = 18 pF , C_0 = 4.4 pF measured (7 pF max), ESR = 8.5 Ω measured (40 Ω max), and Drive Level = 1 mW max (100 µW typical).
(3)	40 MHz crystal characteristics: Abracon ABLS2 series, AT cut, C_L = 18 pF , C_0 = 5 pF measured (7 pF max), ESR = 5 Ω measured (40 Ω max), and Drive Level = 1 mW max (100 µW typical).

7 Parameter Measurement Information

7.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 23 illustrates the two different definitions side-by-side for inputs and Figure 24 illustrates the two different definitions side-by-side for outputs. The V_{ID} (or V_{OD}) definition show the DC levels, V_{IH} and V_{OL} (or V_{OH} and V_{OL}), that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

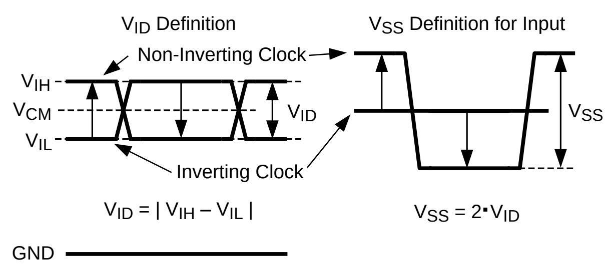


Figure 23. Two Different Definitions for Differential Input Signals

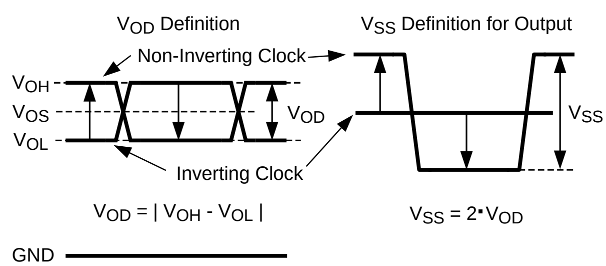


Figure 24. Two Different Definitions for Differential Output Signals

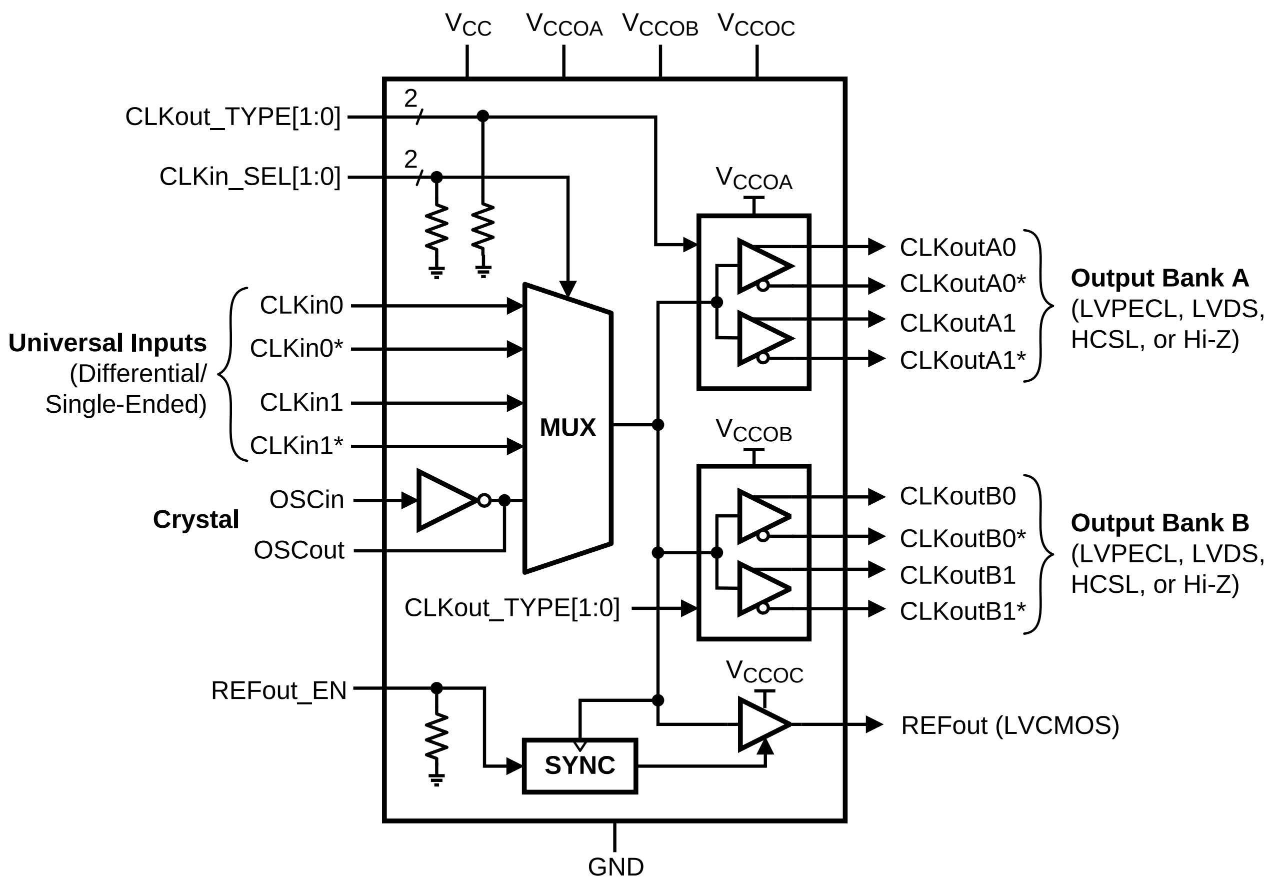
Refer to Application Note AN-912 *Common Data Transmission Parameters and their Definitions* (SNLA036) for more information.

8 Detailed Description

8.1 Overview

The LMK00304 is a 4-output differential clock fanout buffer with low additive jitter that can operate up to 3.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 2 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 32-pin WQFN package and leverages much of the high-speed, low-noise circuit design employed in the LMK04800 family of clock conditioners.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 V_{CC} and V_{CCO} Power Supplies

The LMK00304 has separate 3.3 V core supply (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}). Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to its respective Vcco supply, while the output levels for LVDS and HCSL are relatively constant over the specified Vcco range. Refer to *Power Supply Recommendations* for additional supply related considerations, such as power dissipation, power supply bypassing, and power supply ripple rejection (PSRR).

NOTE

Care should be taken to ensure the Vcco voltages do not exceed the Vcc voltage to prevent turning-on the internal ESD protection circuitry.

8.3.2 Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in Table 2. Refer to *Driving the Clock Inputs* for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator circuit will start-up and its clock will be distributed to all outputs. Refer to *Crystal Interface* for more information. Alternatively, OSCin may be driven by a single-ended clock (up to 250 MHz) instead of a crystal.

Table 2. Input Selection

CLKin_SEL1	CLKin_SEL0	SELECTED INPUT
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin

Table 3 shows the output logic state vs. input state when either CLKin0/CLKin0* or CLKin1/CLKin1* is selected. When OSCin is selected, the output state will be an inverted copy of the OSCin input state.

Table 3. CLKin Input vs. Output States

STATE of SELECTED CLKin	STATE of ENABLED OUTPUTS
CLKinX and CLKinX* inputs floating	Logic low
CLKinX and CLKinX* inputs shorted together	Logic low
CLKin logic low	Logic low
CLKin logic high	Logic high

8.3.3 Clock Outputs

The differential output buffer type for both Bank A and B outputs are configured using the CLKout_TYPE[1:0] as shown in Table 4. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length (see note below) to minimize capacitance and potential coupling and reduce power consumption. If all differential outputs are not used, it is recommended to disable (Hi-Z) the banks to reduce power. Refer to *Termination and Use of Clock Drivers* for more information on output interface and termination techniques.

NOTE

For best soldering practices, the minimum trace length for any unused pin should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

Table 4. Differential Output Buffer Type Selection

CLKout_ TYPE1	CLKout_ TYPE0	CLKoutX BUFFER TYPE (BANK A and B)
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Disabled (Hi-Z)

8.3.3.1 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the Vcco voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN, as shown in Table 5.

Table 5. Reference Output Enable

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

The REFout_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout will be enabled within 3 cycles (t_{EN}) of the input clock after REFout_EN is toggled high. REFout will be disabled within 3 cycles (t_{DIS}) of the input clock after REFout_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1 kΩ load to ground, then the output will be pulled to low when disabled.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Driving the Clock Inputs

The LMK00304 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept DC-coupled 3.3V/2.5V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in *Electrical Characteristics*. The device can accept a wide range of signals due to its wide input common mode voltage range (V_{CM}) and input voltage swing (V_{ID}) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling may also be employed to shift the input signal to within the V_{CM} range. Refer to *Termination and Use of Clock Drivers* for signal interfacing and termination techniques.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode-rejection. Refer to the "Noise Floor vs. CLKin Slew Rate" and "RMS Jitter vs. CLKin Slew Rate" plots in *Typical Characteristics*.

While it is recommended to drive the CLKin/CLKin* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the *Electrical Characteristics*. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50 Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. Again, the single-ended input slew rate should be as high as possible to minimize performance degradation. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in Figure 25. The output impedance of the LVCMOS driver plus Rs should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.

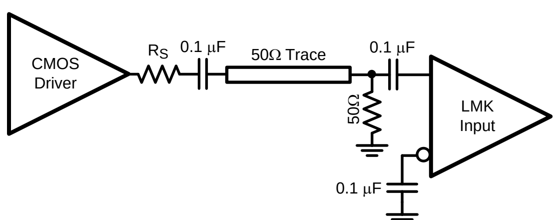


Figure 25. Single-Ended LVCMOS Input, AC Coupling

A single-ended clock may also be DC coupled to CLKinX as shown in Figure 26. A 50-Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKinX, CLKinX* should be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage should be within the specified input common voltage (V_{CM}) range. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

If the LVCMOS driver cannot achieve sufficient swing with a DC-terminated 50Ω load at the CLKinX input as shown in Figure 26, then consider connecting the 50Ω load termination to ground through a capacitor (C_{AC}). This AC termination blocks the DC load current on the driver, so the voltage swing at the input is determined by the voltage divider formed by the source (Ro+Rs) and 50Ω load resistors. The value for C_{AC} depends on the trace delay, Td, of the 50Ω transmission line, where C_{AC} >= 3*Td/50Ω.

Driving the Clock Inputs (continued)

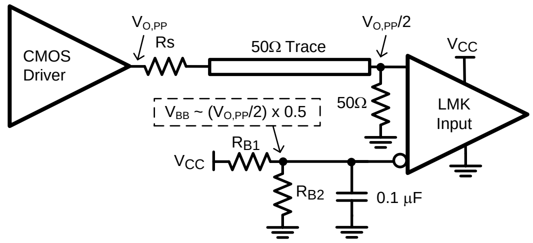


Figure 26. Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with an single-ended external clock as shown in Figure 27. The input clock should be AC coupled to the OSCin pin, which has an internally-generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either universal input (CLKinX) since it offers higher operating frequency, better common mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.

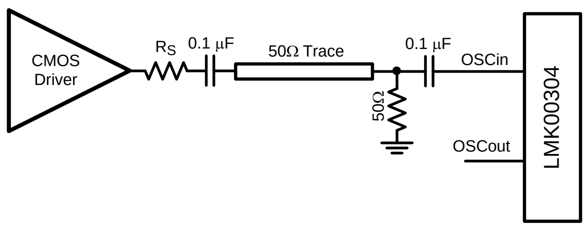


Figure 27. Driving OSCin with a Single-Ended Input

9.2 Crystal Interface

The LMK00304 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 28.

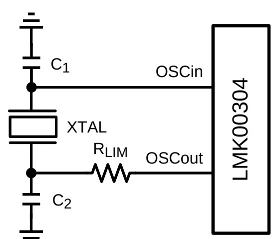


Figure 28. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 - 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 4 pF typical) of the device and PCB stray capacitance (C_{STRAY} ~ 1~3 pF) can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so Equation 1 can be rewritten in terms of C_1 only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY})*2 \quad (3)$$

Crystal Interface (continued)

Electrical Characteristics provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR}*(1 + C_0/C_L)^2$$

where

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the max. equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_0 is the min. shunt capacitance specified for the crystal (4)

I_{RMS} can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in Figure 28, an external resistor, R_{LIM}, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ.

9.3 Termination and Use of Clock Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
  - LVDS outputs are current drivers and require a closed current loop.
  - HCSL drivers are switched current outputs and require a DC path to ground via 50 Ω termination.
  - LVPECL outputs are open emitter and require a DC path to ground.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC coupled.

It is possible to drive a non-LVPECL or non-LVDS receiver with a LVDS or LVPECL driver as long as the above guidelines are followed. Check the data sheet of the receiver or input being driven to determine the best termination and coupling method to be sure the receiver is biased at the optimum DC voltage (common mode voltage).

9.3.1 Termination for DC-Coupled Differential Operation

For DC-coupled operation of an LVDS driver, terminate with 100 Ω as close as possible to the LVDS receiver as shown in Figure 29.

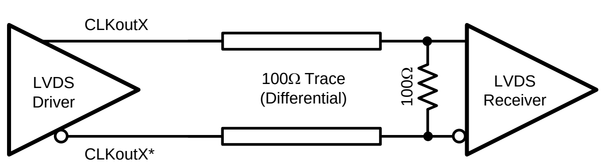


Figure 29. Differential LVDS Operation, DC Coupling, No Biasing by the Receiver

Termination and Use of Clock Drivers (continued)

For DC-coupled operation of an HCSL driver, terminate with 50 Ω to ground near the driver output as shown in Figure 30. Series resistors, Rs, may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50-Ω termination resistors.

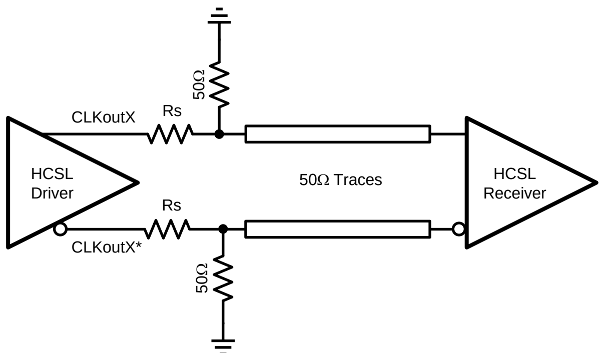


Figure 30. HCSL Operation, DC Coupling

For DC-coupled operation of an LVPECL driver, terminate with 50 Ω to Vcco - 2 V as shown in Figure 31. Alternatively terminate with a Thevenin equivalent circuit as shown in Figure 32 for Vcco (output driver supply voltage) = 3.3 V and 2.5 V. In the Thevenin equivalent circuit, the resistor dividers set the output termination voltage (V_{TT}) to Vcco – 2 V.

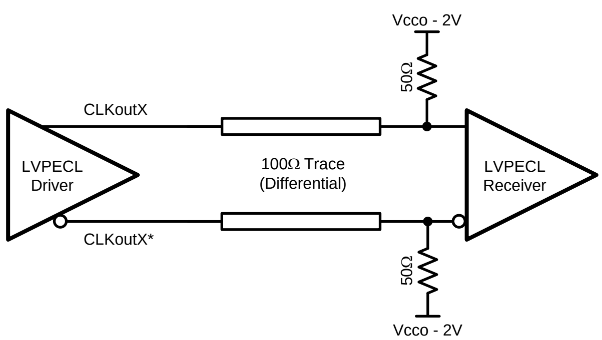
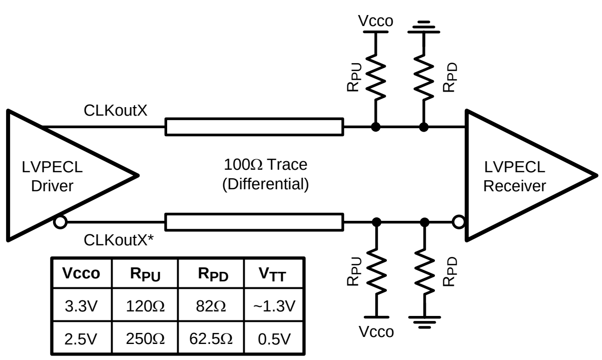


Figure 31. Differential LVPECL Operation, DC Coupling



Vcco	R_{PU}	R_{PD}	V_{TT}
3.3V	120Ω	82Ω	~1.3V
2.5V	250Ω	62.5Ω	0.5V

Figure 32. Differential LVPECL Operation, DC Coupling, Thevenin Equivalent

Termination and Use of Clock Drivers (continued)

9.3.2 Termination for AC-Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common mode voltage) when driving different receiver standards. Because AC coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level.

When driving differential receivers with an LVDS driver, the signal may be AC coupled by adding DC-blocking capacitors; however the proper DC bias point needs to be established at both the driver side and the receiver side. The recommended termination scheme depends on whether the differential receiver has integrated termination resistors or not.

When driving a differential receiver without internal 100-Ω differential termination, the AC-coupling capacitors should be placed between the load termination resistor and the receiver to allow a DC path for proper biasing of the LVDS driver. This is shown in Figure 33. The load termination resistor and AC-coupling capacitors should be placed as close as possible to the receiver inputs to minimize stub length. The receiver can be biased internally or externally to a reference voltage within the receiver's common mode input range through resistors in the kilo-ohm range.

When driving a differential receiver with internal 100-Ω differential termination, a source termination resistor should be placed before the AC-coupling capacitors for proper DC biasing of the driver as shown in Figure 34. However, with a 100-Ω resistor at the source and the load (that is, double terminated), the equivalent resistance seen by the LVDS driver is 50 Ω which causes the effective signal swing at the input to be reduced by half. If a self-terminated receiver requires input swing greater than 250 mVpp (differential) as well as AC coupling to its inputs, then the LVDS driver with the double-terminated arrangement in Figure 34 may not meet the minimum input swing requirement; alternatively, the LVPECL or HCSL output driver format with AC coupling is recommended to meet the minimum input swing required by the self-terminated receiver.

When using AC coupling with LVDS outputs, there may be a startup delay observed in the clock output due to capacitor charging. The examples in Figure 33 and Figure 34 use 0.1-µF capacitors, but this value may be adjusted to meet the startup requirements for the particular application.

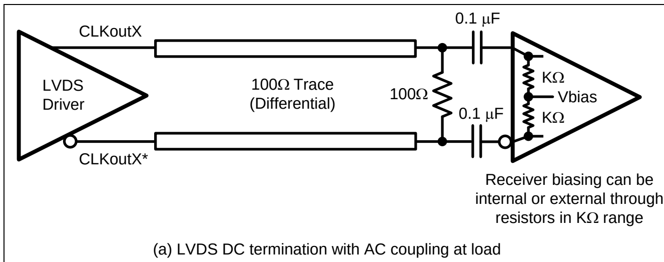


Figure 33. Differential LVDS Operation With AC Coupling to Receivers
(a) Without Internal 100-Ω Termination

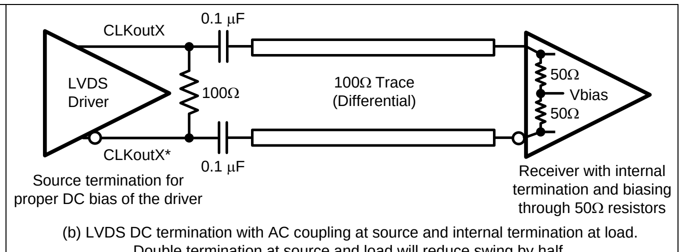


Figure 34. Differential LVDS Operation With AC Coupling to Receivers
(b) With Internal 100-Ω Termination

LVPECL drivers require a DC path to ground. When AC coupling an LVPECL signal use 160-Ω emitter resistors (or 91 Ω for Vcco = 2.5 V) close to the LVPECL driver to provide a DC path to ground as shown in Figure 38. For proper receiver operation, the signal should be biased to the DC bias level (common mode voltage) specified by the receiver. The typical DC bias voltage (common mode voltage) for LVPECL receivers is 2 V. Alternatively, a Thevenin equivalent circuit forms a valid termination as shown in Figure 35 for Vcco = 3.3 V and 2.5 V. Note: this Thevenin circuit is different from the DC coupled example in Figure 32, since the voltage divider is setting the input common mode voltage of the receiver.

Termination and Use of Clock Drivers (continued)

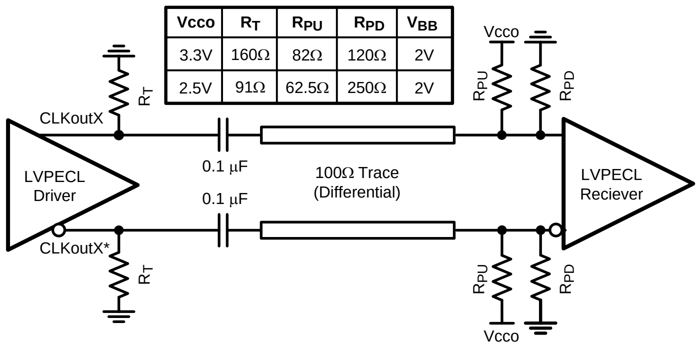


Figure 35. Differential LVPECL Operation, AC Coupling, Thevenin Equivalent

9.3.3 Termination for Single-Ended Operation

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal.

It is possible to use an LVPECL driver as one or two separate 800 mV p-p signals. When DC coupling one of the LMK00304 LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminate the unused driver. When DC coupling on of the LMK00304 LVPECL drivers, the termination should be 50 Ω to Vcco – 2 V as shown in Figure 36. The Thevenin equivalent circuit is also a valid termination as shown in Figure 37 for Vcco = 3.3 V.

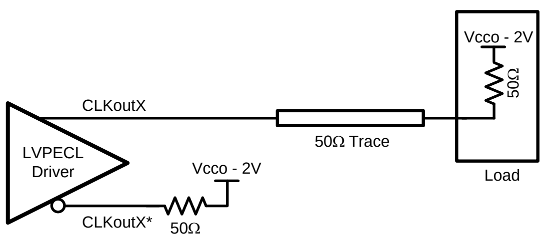


Figure 36. Single-Ended LVPECL Operation, DC Coupling

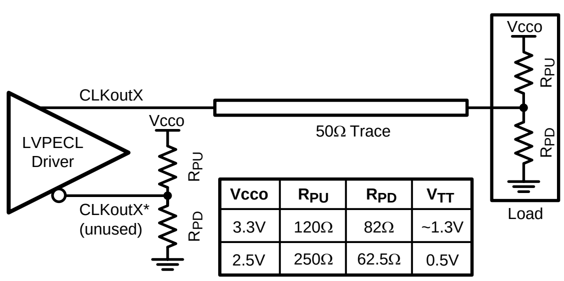
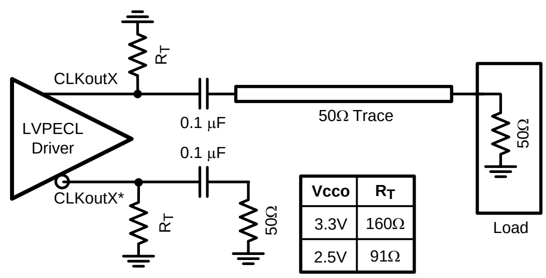


Figure 37. Single-Ended LVPECL Operation, DC Coupling, Thevenin Equivalent

Termination and Use of Clock Drivers (continued)

When AC coupling an LVPECL driver use a 160-Ω emitter resistor (or 91 Ω for Vcco = 2.5 V) to provide a DC path to ground and ensure a 50-Ω termination with the proper DC bias level for the receiver. The typical DC bias voltage for LVPECL receivers is 2 V. If the companion driver is not used, it should be terminated with either a proper AC or DC termination. This latter example of AC coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment no DC bias point (0 VDC) is required for safe and proper operation. The internal 50 Ω termination the test equipment correctly terminates the LVPECL driver being measured as shown in Figure 38. When using only one LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminated the unused driver.



Vcco	R_T
3.3V	160Ω
2.5V	91Ω

Figure 38. Single-Ended LVPECL Operation, AC Coupling

10 Power Supply Recommendations

10.1 Power Supply Sequencing

When powering the Vcc and Vcco pins from separate supply rails, TI recommends that the supplies to reach their regulation point at approximately the same time while ramping up, or reach ground potential at the same time while ramping down. Using simultaneous or ratiometric power supply sequencing prevents internal current flow from Vcc to Vcco pins that could occur when Vcc is powered before Vcco.

10.2 Current Consumption and Power Dissipation Calculations

The current consumption values specified in *Electrical Characteristics* can be used to calculate the total power dissipation and IC power dissipation for any device configuration. The total V_{CC} core supply current (I_{CC_TOTAL}) can be calculated using Equation 5:

$$I_{CC\_TOTAL} = I_{CC\_CORE} + I_{CC\_BANKS} + I_{CC\_CMOS}$$

where

- I_{CC_CORE} is the V_{CC} current for core logic and input blocks and depends on selected input (CLKinX or OSCin).
- I_{CC_BANKS} is the V_{CC} current for Banks A & B and depends on the selected output type (I_{CC_PECL}, I_{CC_LVDS}, I_{CC_HCSL}, or 0 mA if disabled).
- I_{CC_CMOS} is the V_{CC} current for the LVCMOS output (or 0 mA if REFout is disabled). (5)

Because the output supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}) can be powered from 3 independent voltages, the respective output supply currents ($I_{CCO\_BANK\_A}$, $I_{CCO\_BANK\_B}$, and I_{CCO_CMOS}) should be calculated separately.

I_{CCO_BANK} for either Bank A or B may be taken as 50% of the corresponding output supply current specified for two banks (I_{CCO_PECL}, I_{CCO_LVDS}, or I_{CCO_HCSL}) **provided the output loading matches the specified conditions**. Otherwise, I_{CCO_BANK} should be calculated per bank using Equation 6:

$$I_{CCO\_BANK} = I_{BANK\_BIAS} + (N \times I_{OUT\_LOAD})$$

where

- I_{BANK_BIAS} is the output bank bias current (fixed value).
- I_{OUT_LOAD} is the DC load current per loaded output pair.
- N is the number of loaded output pairs (N = 0 to 2). (6)

Table 6 shows the typical I_{BANK_BIAS} values and I_{OUT_LOAD} expressions for LVPECL, LVDS, and HCSL.

For LVPECL, it is possible to use a larger termination resistor (R_T) to ground instead of terminating with 50 Ω to V_{TT} = Vcco - 2 V; this technique is commonly used to eliminate the extra termination voltage supply (V_{TT}) and potentially reduce device power dissipation at the expense of lower output swing. For example, when Vcco is 3.3 V, a R_T value of 160 Ω to ground will eliminate the 1.3 V termination supply without sacrificing much output swing. In this case, the typical I_{OUT_LOAD} is 25 mA, so I_{CCO_BANK} for one LVPECL bank reduces to 63 mA (vs. 67.5 mA with 50 Ω resistors to Vcco - 2 V).

Table 6. Typical Output Bank Bias and Load Currents

CURRENT PARAMETER	LVPECL	LVDS	HCSL
I_{BANK_BIAS}	13 mA	11.6 mA	2.4 mA
I_{OUT_LOAD}	$(V_{OH} - V_{TT})/R_T + (V_{OL} - V_{TT})/R_T$	0 mA (No DC load current)	V_{OH}/R_T

Once the current consumption is known for each supply, the total power dissipation (P_{TOTAL}) can be calculated:

$$P_{TOTAL} = (V_{CC} \times I_{CC\_TOTAL}) + (V_{CCOA} \times I_{CCO\_BANK}) + (V_{CCOB} \times I_{CCO\_BANK}) + (V_{CCOC} \times I_{CCO\_CMOS}) \quad (7)$$

If the device is configured with LVPECL and/or HCSL outputs, then it is also necessary to calculate the power dissipated in any termination resistors (P_{RT_PECL} and P_{RT_HCSL}) and in any LVPECL termination voltages (P_{VTT_PECL}). The external power dissipation values can be calculated as follows:

$$P_{RT\_PECL} \text{ (per LVPECL pair)} = (V_{OH} - V_{TT})^2/R_T + (V_{OL} - V_{TT})^2/R_T \quad (8)$$

$$P_{VTT\_PECL} \text{ (per LVPECL pair)} = V_{TT} \times [(V_{OH} - V_{TT})/R_T + (V_{OL} - V_{TT})/R_T] \quad (9)$$

$$P_{RT\_HCSL} \text{ (per HCSL pair)} = V_{OH}^2 / R_T \quad (10)$$

Finally, the IC power dissipation (P_{DEVICE}) can be computed by subtracting the external power dissipation values from P_{TOTAL} as follows:

$$P_{DEVICE} = P_{TOTAL} – N_1 \times (P_{RT\_PECL} + P_{VTT\_PECL}) – N_2 \times P_{RT\_HCSL} \quad (11)$$

where

- N_1 is the number of LVPECL output pairs with termination resistors to V_{TT} (usually Vcco - 2 V or GND).
- N_2 is the number of HCSL output pairs with termination resistors to GND.

10.2.1 Power Dissipation Example: Worst-Case Dissipation

This example shows how to calculate IC power dissipation for a configuration to estimate **worst-case power dissipation**. In this case, the maximum supply voltage and supply current values specified in *Electrical Characteristics* are used.

- Max V_{CC} = V_{CCO} = 3.465 V. Max I_{CC} and I_{CCO} values.
- CLKin0/CLKin0* input is selected.
- Banks A and B are configured for LVPECL: all outputs terminated with 50 Ω to V_T = Vcco – 2 V.
- REFout is enabled with 5-pF load.
- T_A = 85°C

Using the power calculations from the previous section and *maximum* supply current specifications, we can compute P_{TOTAL} and P_{DEVICE}.

- From Equation 5: I_{CC_TOTAL} = 10.5 mA + 48 mA + 5.5 mA = 64 mA
- From I_{CCO_PECL} max spec: I_{CCO_BANK} = 50% of I_{CCO_PECL} = 81.5 mA
- From Equation 7: P_{TOTAL} = (3.465 V × 64 mA) + (3.465 V × 81.5 mA)+ (3.465 V × 81.5 mA) + (3.465 V × 10 mA) = 821 mW
- From Equation 8: P_{RT_PECL} = ((2.57 V – 1.47 V)^2/50 Ω) + ((1.72 V – 1.47 V)^2/50 Ω) = 25.5 mW (per output pair)
- From Equation 9: P_{VTT_PECL} = 1.47 V × [((2.57 V – 1.47 V) / 50 Ω) + ((1.72 V – 1.47 V) / 50 Ω)] = 39.5 mW (per output pair)
- From Equation 10: P_{RT_HCSL} = 0 mW (no HCSL outputs)
- From Equation 11: P_{DEVICE} = 821 mW – (4 × (25.5 mW + 39.5 mW)) – 0 mW = 561 mW

In this worst-case example, the IC device will dissipate about 561 mW or 68% of the total power (821 mW), while the remaining 32% will be dissipated in the emitter resistors (102 mW for 4 pairs) and termination voltage (158 mW into Vcco – 2 V). Based on θ_{JA} of 38.1°C/W, the estimate die junction temperature would be about 21.4°C above ambient, or 106.4°C when T_A = 85°C.

10.3 Power Supply Bypassing

The Vcc and Vcco power supplies should have a high-frequency bypass capacitor, such as 0.1 µF or 0.01 µF, placed very close to each supply pin. 1-µF to 10-µF decoupling capacitors should also be placed nearby the device between the supply and ground planes. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

10.3.1 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, and so forth. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00304, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

Power Supply Bypassing (continued)

For the LMK00304, power supply ripple rejection, or PSRR, was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the Vcco supply. The PSRR test setup is shown in Figure 39.

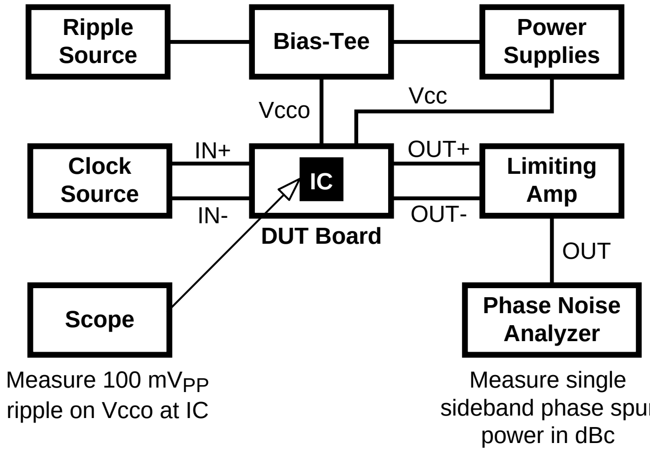


Figure 39. PSRR Test Setup

A signal generator was used to inject a sinusoidal signal onto the Vcco supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the Vcco pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 156.25 MHz and 312.5 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on Vcco = 2.5 V
- Ripple frequencies: 100 kHz, 1 MHz, and 10 MHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$\text{DJ (ps pk-pk)} = [(2 \times 10^{(PSRR\ /\ 20)}) / (\pi \times f_{CLK})] \times 10^{12} \quad (12)$$

The “PSRR vs. Ripple Frequency” plots in *Typical Characteristics* show the ripple-induced phase spur levels for the differential output types at 156.25 MHz and 312.5 MHz. The LMK00304 exhibits very good and well-behaved PSRR characteristics across the ripple frequency range for all differential output types. The phase spur levels for LVPECL are below –64 dBc at 156.25 MHz and below –62 dBc at 312.5 MHz. Using Equation 12, these phase spur levels translate to Deterministic Jitter values of 2.57 ps pk-pk at 156.25 MHz and 1.62 ps pk-pk at 312.5 MHz. Testing has shown that the PSRR performance of the device improves for Vcco = 3.3 V under the same ripple amplitude and frequency conditions.

10.4 Thermal Management

Power dissipation in the LMK00304 device can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power dissipation times θ_{JA} should not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

Thermal Management (continued)

A recommended land and via pattern is shown in Figure 40. More information on soldering WQFN packages can be obtained at: http://www.ti.com/packaging.

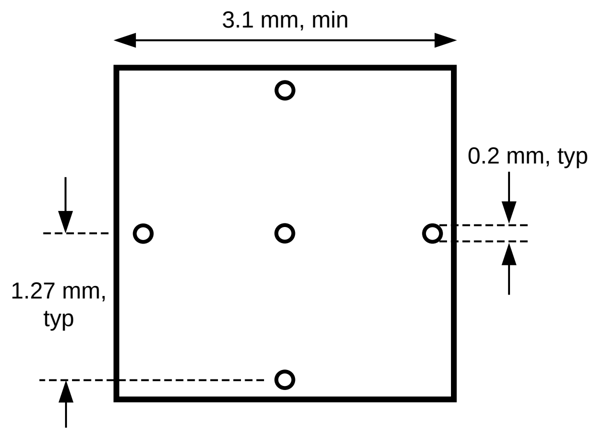


Figure 40. Recommended Land and Via Pattern

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 40 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

10.4.1 Support for PCB Temperature up to 105°C

The LMK00304 can maintain a safe junction temperature below the recommended maximum value of 125°C even when operated on a PCB with a maximum board temperature (T_b) of 105°C. This is shown by the following example calculation, which assumes the worst-case IC power dissipation (P_{DEVICE}) from Power Dissipation Example: Worst-Case Dissipation and a 4-layer JEDEC test board with no airflow.

$$T_J = T_b + (\psi_{jb} \times P_{DEVICE})$$

where

- T_b = 105°C
- ψ_{jb} = 11.9°C/W
- P_{DEVICE} = 561 mW (13)

$$T_J = 111.7°C \quad (14)$$

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

《AN-912 通用数据传输参数及其定义》(SNLA036)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK00304SQ/NOPB	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	K00304	Samples
LMK00304SQE/NOPB	ACTIVE	WQFN	RTV	32	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	K00304	Samples
LMK00304SQX/NOPB	ACTIVE	WQFN	RTV	32	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	K00304	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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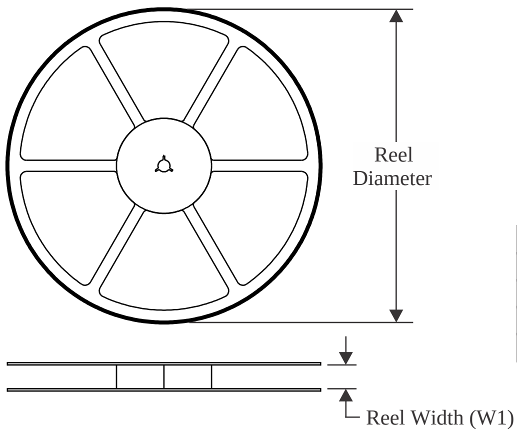
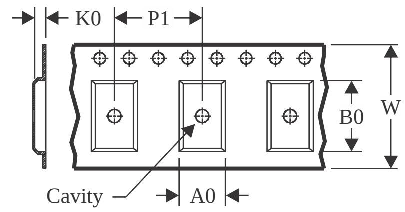
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

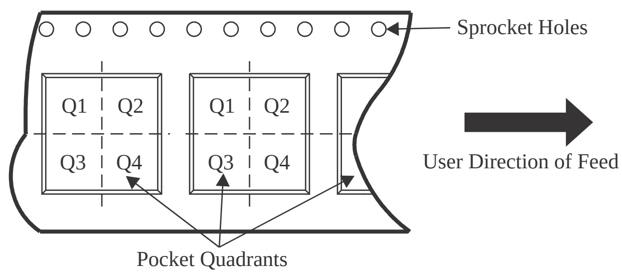


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

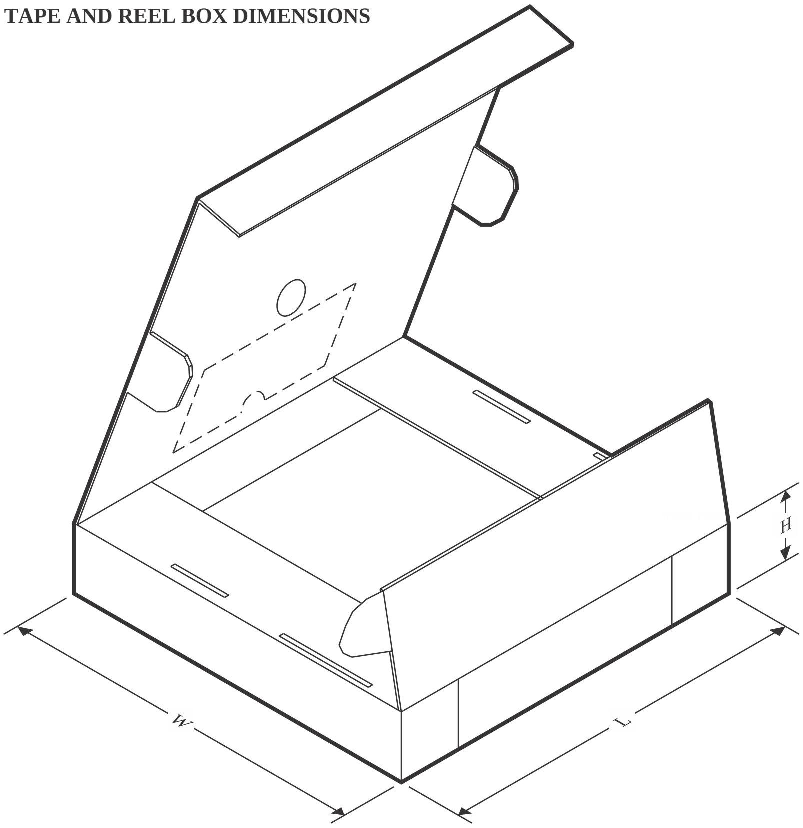
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

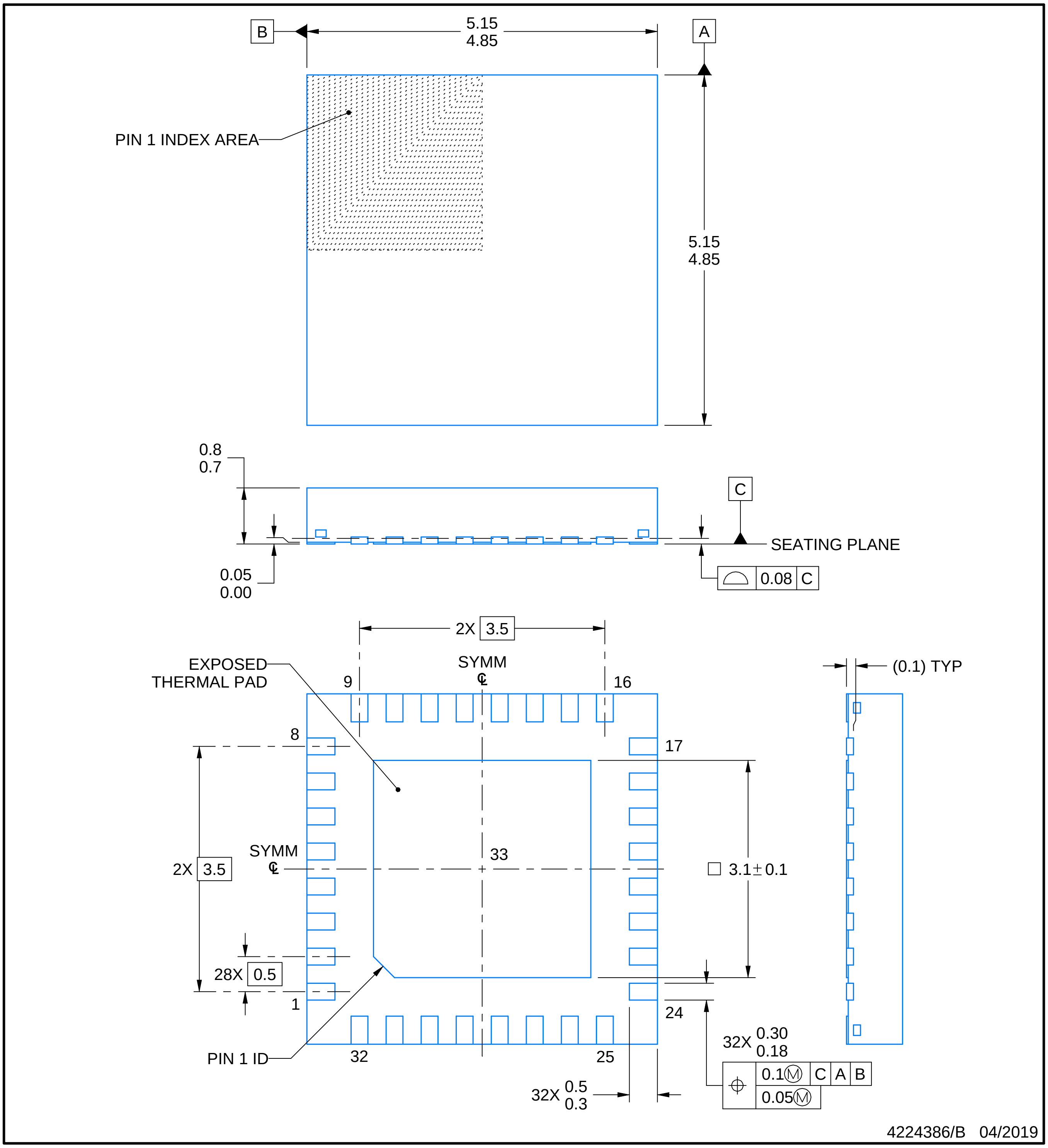
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00304SQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMK00304SQE/NOPB	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMK00304SQX/NOPB	WQFN	RTV	32	2500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



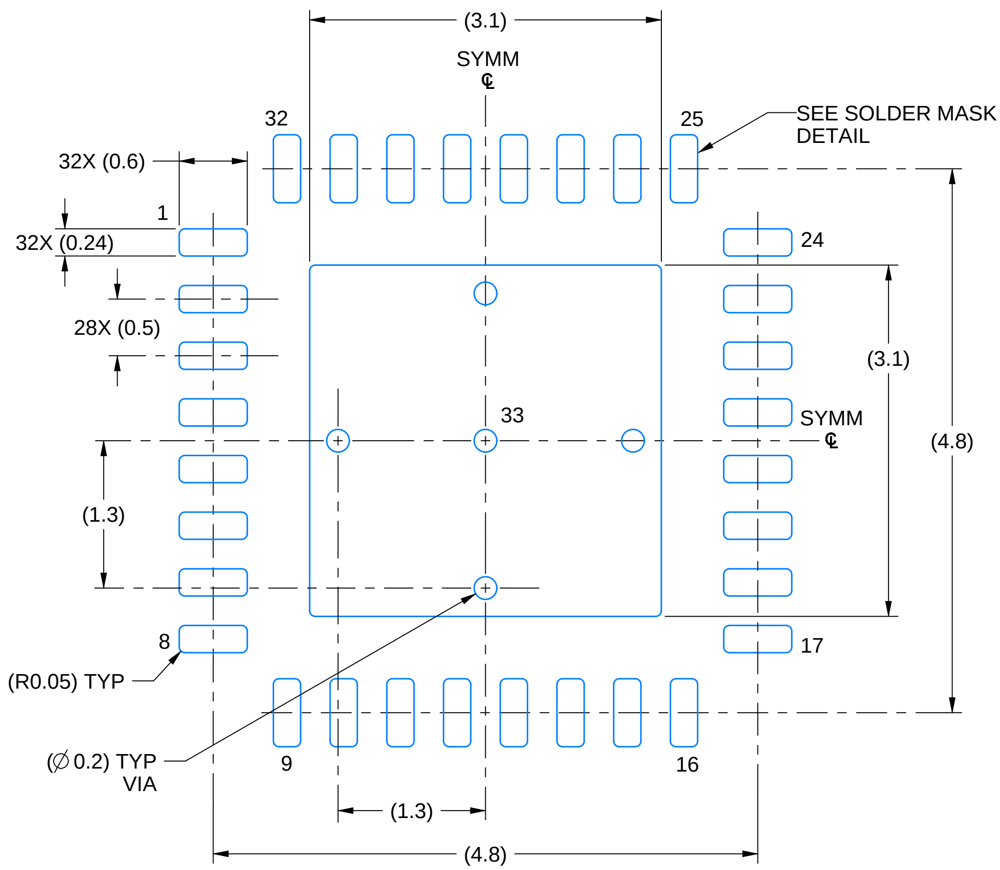
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00304SQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
LMK00304SQE/NOPB	WQFN	RTV	32	250	208.0	191.0	35.0
LMK00304SQX/NOPB	WQFN	RTV	32	2500	356.0	356.0	35.0

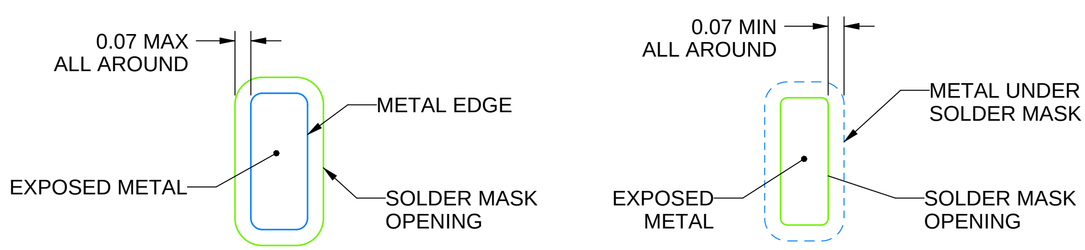


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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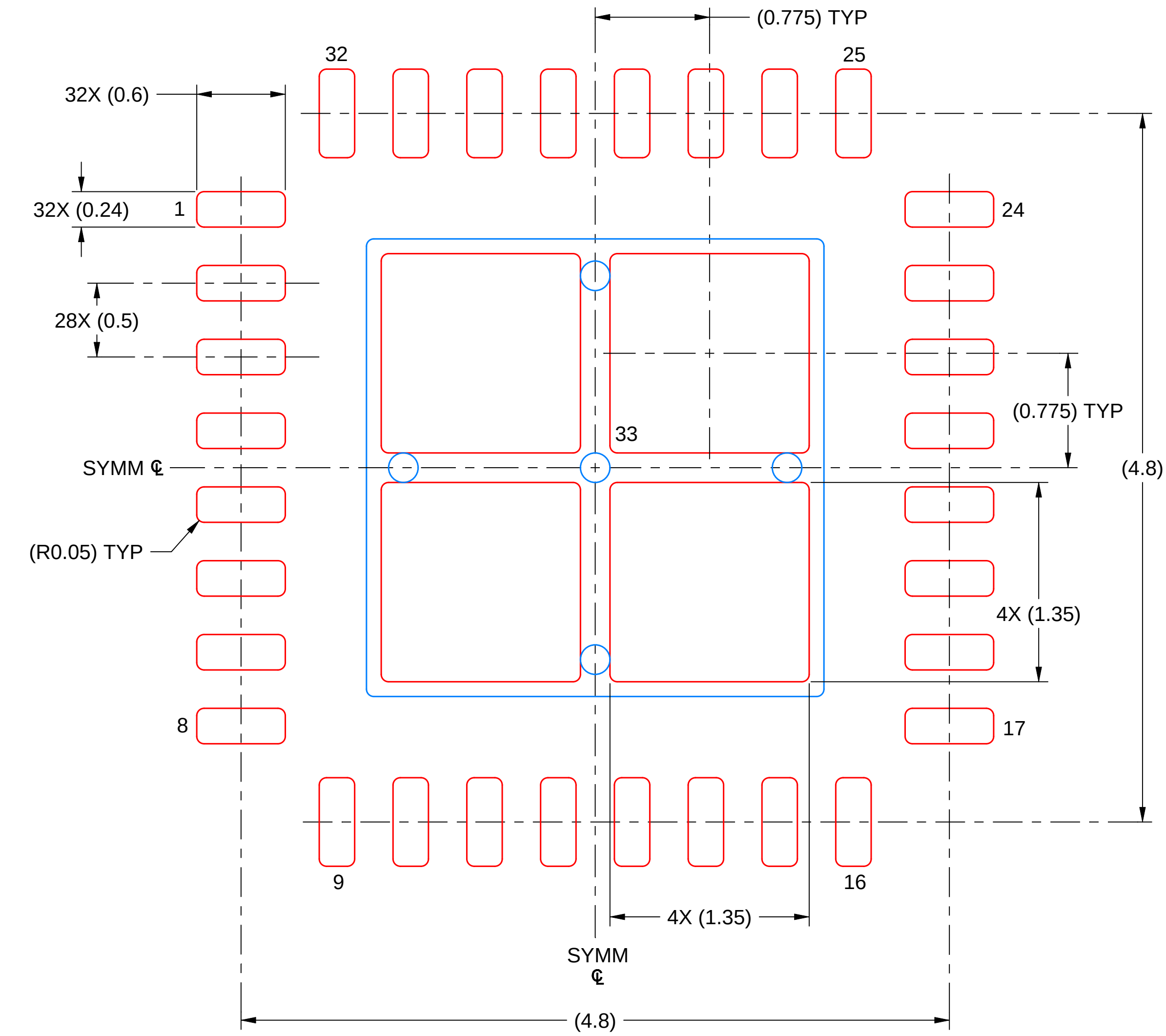
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.