



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V- .....	36V
Input Voltage .....	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit <sup>(2)</sup> .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-40°C to +125°C
Junction Temperature .....	150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# ELECTRICAL CHARACTERISTICS

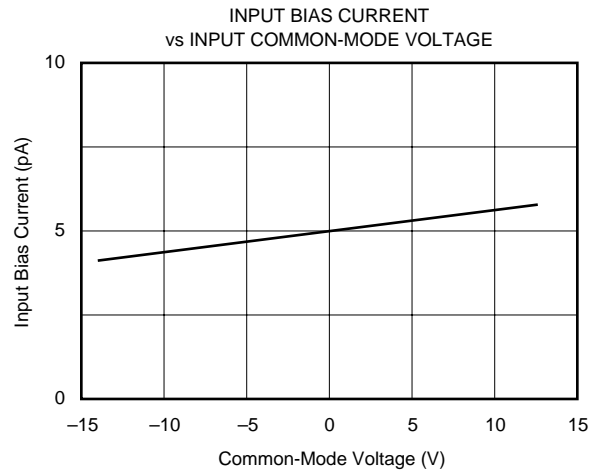
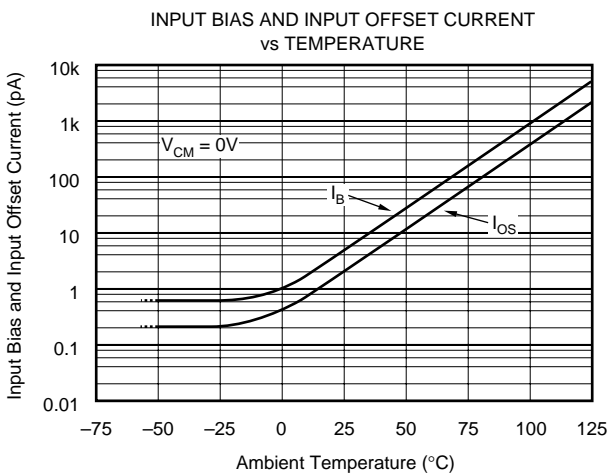
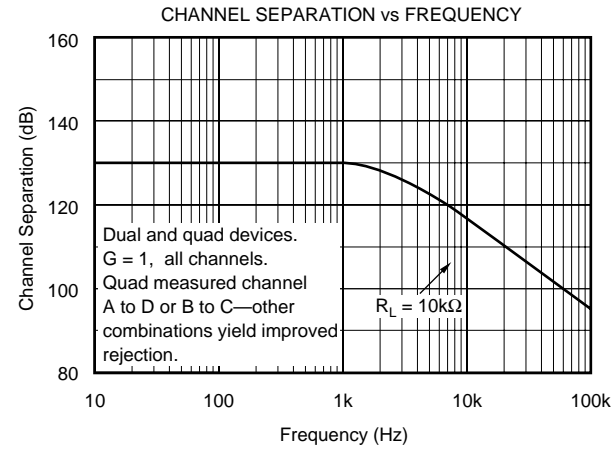
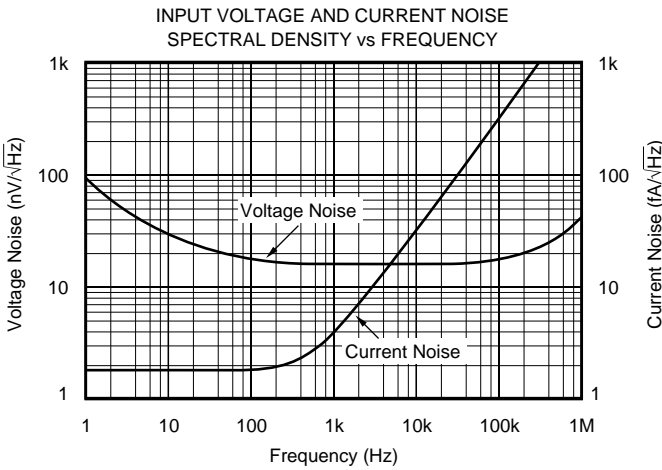
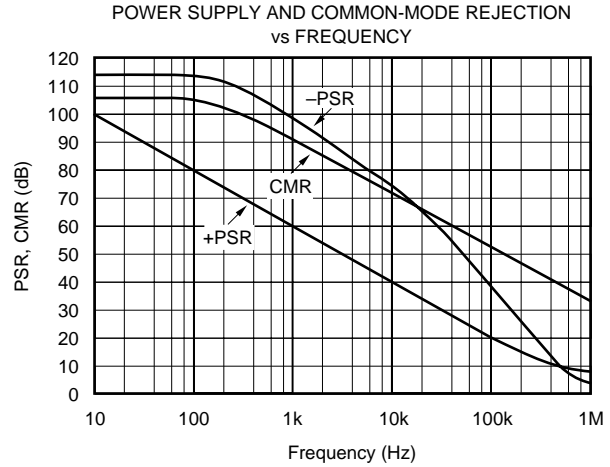
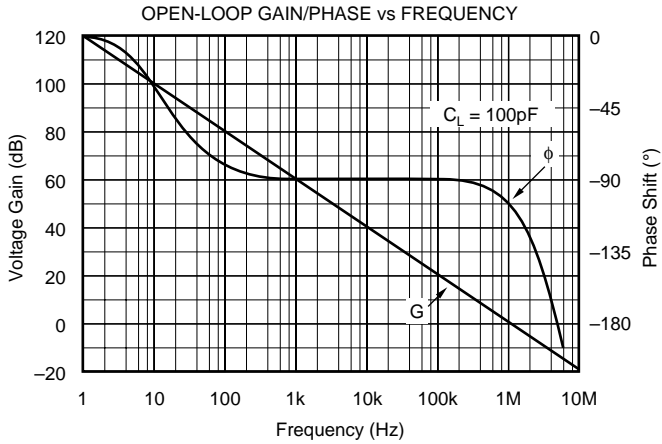
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITION	OPA130PA, UA OPA2130PA, UA OPA4130PA, UA			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage vs Temperature <sup>(1)</sup> vs Power Supply Channel Separation (dual and quad)	Operating Temperature Range $V_S = \pm 2.25\text{V to } \pm 18\text{V}$		$\pm 0.2$ $\pm 2$ 2 0.3	$\pm 1$ $\pm 10$ 20	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b> <sup>(2)</sup> Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		See Typical Characteristics $+5$ $\pm 2$		pA pA
<b>NOISE</b> Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			30 18 16 16 4		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range, Positive Negative Common-Mode Rejection	$V_{CM} = -13\text{V to } +13\text{V}$	$(V^+)-2$ $(V^-)+2$ 90	$(V^+)-1.5$ $(V^-)+1.2$ 105		V V dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode	$V_{CM} = -13\text{V to } +13\text{V}$		$10^{13} \parallel 1$ $10^{13} \parallel 3$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b> Open-loop Voltage Gain	$V_O = -13.8\text{V to } +13\text{V}$ $R_L = 2\text{k}\Omega$ , $V_O = -13\text{V to } +12\text{V}$	120 120	135 135		dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	$G = 1$ , 10V Step, $C_L = 100\text{pF}$ $G = 1$ , 10V Step, $C_L = 100\text{pF}$ $G = 1$ , $V_{IN} = \pm 15\text{V}$ 1kHz, $G = 1$ , $V_O = 3.5\text{Vrms}$		1 2 5.5 7 2 0.0003		MHz V/ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ %
<b>OUTPUT</b> Voltage Output, Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation)	$R_L = 2\text{k}\Omega$ $R_L = 2\text{k}\Omega$	$(V^+)-2$ $(V^-)+1.2$ $(V^+)-3$ $(V^-)+2$	$(V^+)-1.5$ $(V^-)+1$ $(V^+)-2.5$ $(V^-)+1.5$ $\pm 18$ 10		V V V V mA nF
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	$\pm 2.25$	$\pm 15$ $\pm 530$	$\pm 18$ $\pm 650$	V V $\mu\text{A}$
<b>TEMPERATURE RANGE</b> Operating Range Storage Thermal Resistance, $\theta_{JA}$ DIP-8 SO-8 Surface-Mount DIP-14 SO-14 Surface-Mount		-40 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Ensured by wafer test. (2) High-speed test at  $T_J = 25^\circ\text{C}$ .

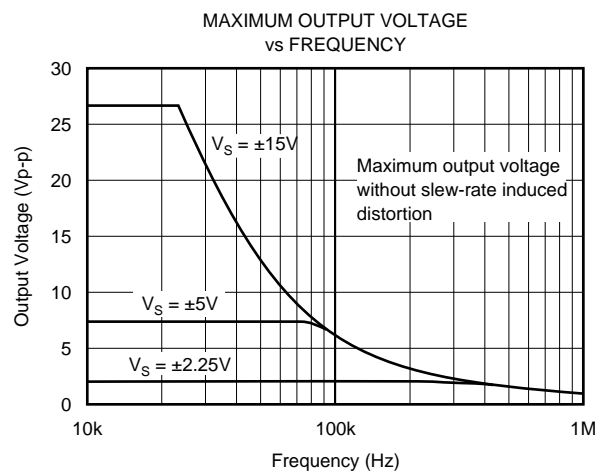
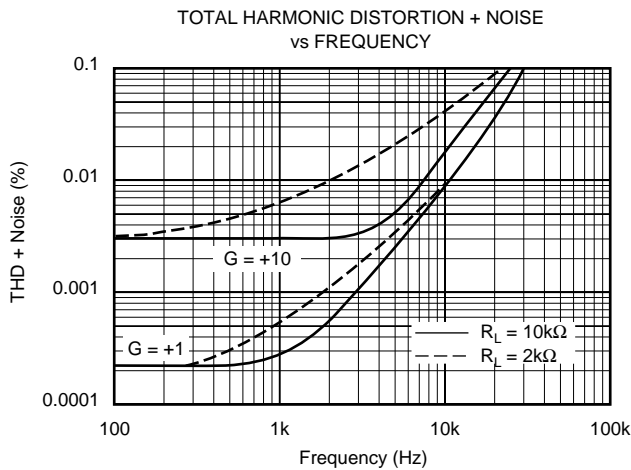
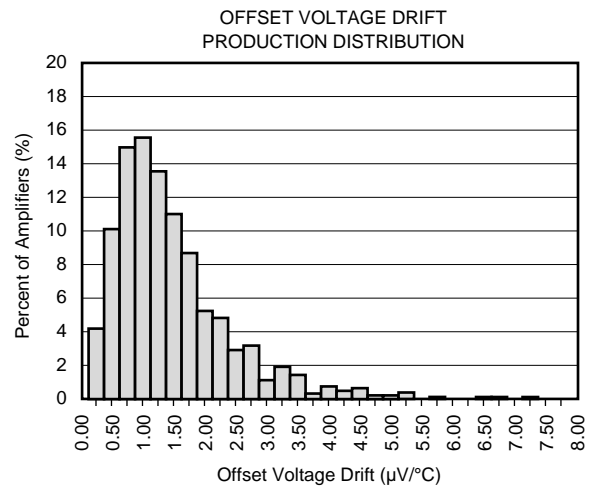
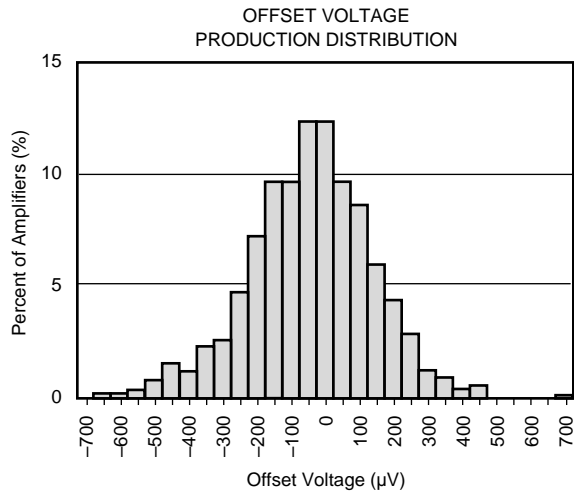
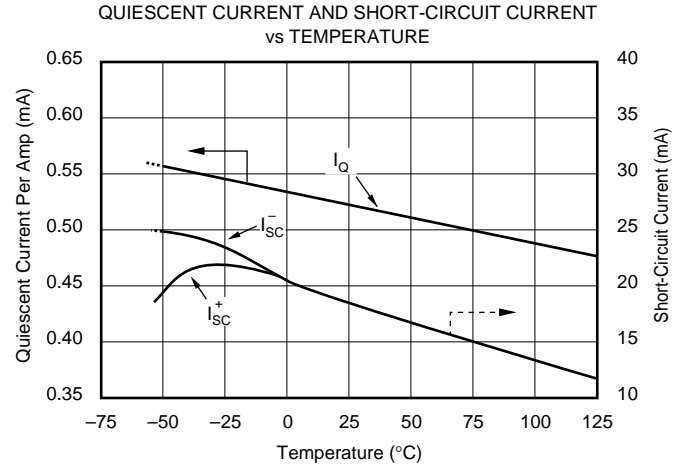
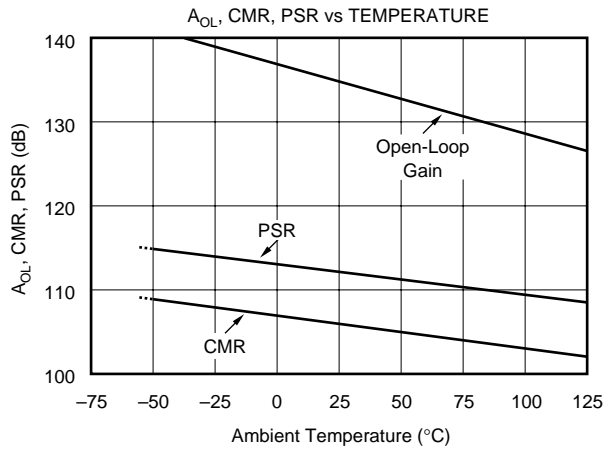
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



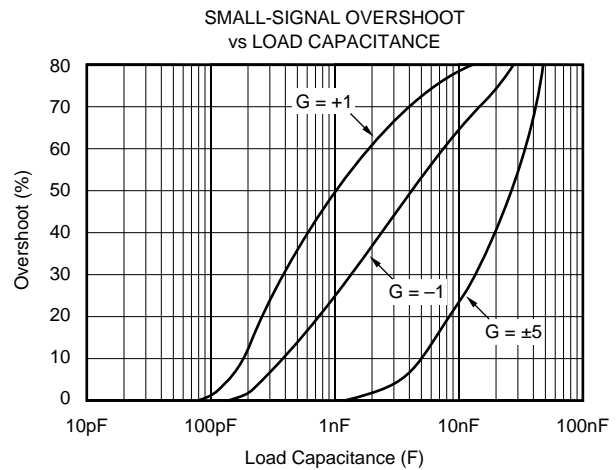
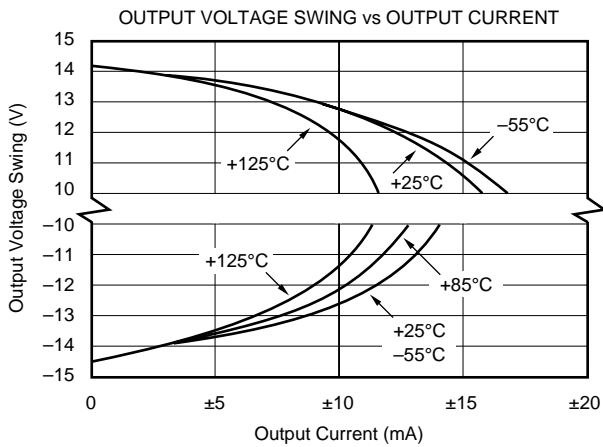
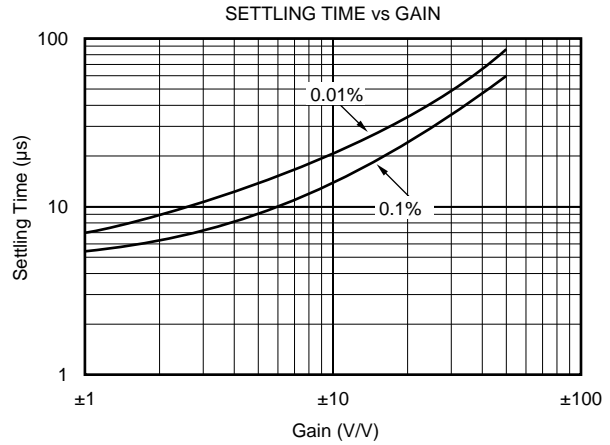
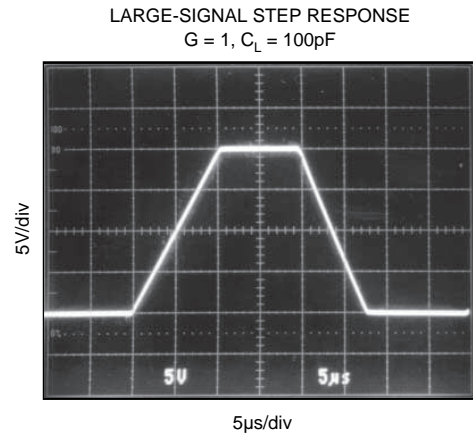
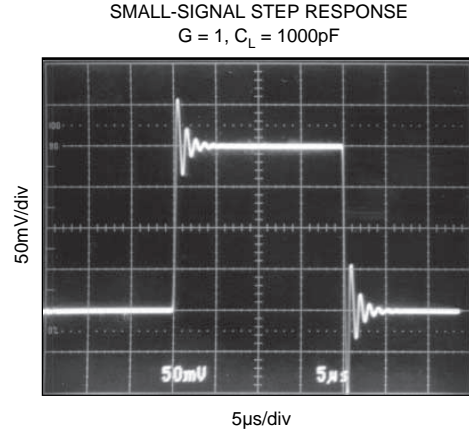
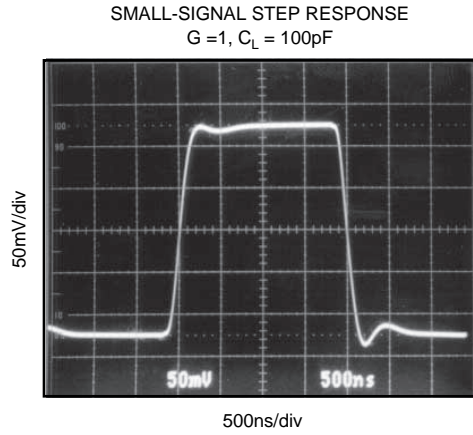
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



## APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

### OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$  with excellent performance. Although specifications are production tested with  $\pm 15\text{V}$  supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

### OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

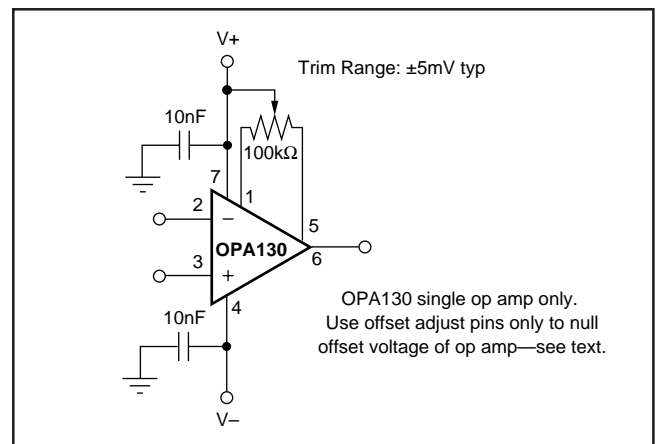


FIGURE 1. OPA130 Offset Voltage Trim Circuit.

### INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the Typical Characteristic curve *Input Bias Current vs Temperature*.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA130. See the Typical Characteristic curve *Input Bias Current vs Common-Mode Voltage*.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA130UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 130UA	<a href="#">Samples</a>
OPA130UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 130UA	<a href="#">Samples</a>
OPA2130UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2130UA	<a href="#">Samples</a>
OPA2130UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2130UA	<a href="#">Samples</a>
OPA4130UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4130UA	<a href="#">Samples</a>
OPA4130UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4130UA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4130UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA130UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2130UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4130UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA130UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2130UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4130UA	D	SOIC	14	50	506.6	8	3940	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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