用于发光二极管 (LED) 照明的谐振开关驱动器控制器

查询样品: TPS92023

特性

- 用于多灯串 **LED** 照明应用的线路电平控制 **(LLC)** 谐振开关驱动器控制器
- 半桥拓扑结构
- 固定或变化的开关频率控制
- 可编程软启动时间
- 可编程死区时间以实现最佳效率
- 简便的开/关控制
- 过流保护
- 过温保护
- 偏置电压欠压闭锁 **(UVLO)** 和过压保护 **(OVP)**
- 具有 **0.4A** 拉电流和 **0.8A** 灌电流能力的集成栅级驱动器
- 运行温度范围：**-40°C** 至 **125°C**
- 小外形尺寸集成电路 **(SOIC) 8** 引脚封装

应用范围

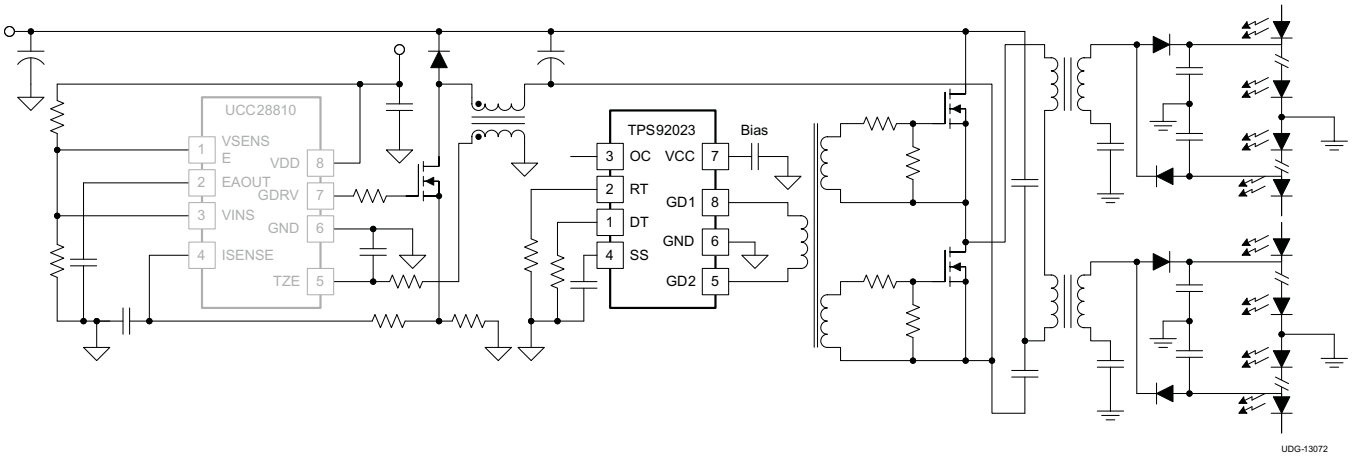
- 商用/工业用 **LED** 照明驱动器
- 高棚灯 **LED** 照明
- 低棚灯 **LED** 照明
- 街道 **LED** 照明
- 区域 **LED** 照明
- 体育场馆 **LED** 照明
- **LED** 洗墙灯
- **LED** 数字电视 **(DTV)** 和显示器背光
- 电子照明镇流器

说明

TPS92023 是一款高性能谐振-开关 LED 驱动器控制器。 它设计用于较高功率 LED 照明系统。 相对于传统的半桥转换器，TPS92023 使用拓扑结构为 LLC 的谐振开关，来实现极高的效率。

可编程死区时间用最少的磁化电流来实现零电压开关，从而在多种应用中大大提高了系统效率。

TPS92023 能够以两个开关频率模式运行。 当负载电流为恒定时，固定频率可实现简单设计，而可变开关可针对电流不断变化的负载实现最佳的闭环控制。 内部振荡器支持 30kHz 至 380kHz 范围内的开关频率。 这个高精度振荡器实现了限制在 4% 耐受以内的最小开关频率，从而使得设计人员能够避免功率级的*过度设计*，并因此减少了总体系统成本。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The programmable soft-start timer maximizes design flexibility demanded by the varied requirements of end equipments utilizing a half-bridge topology. The TPS92023 incorporates a 0.4-A source and 0.8-A sink for driving a low-cost gate driver transformer, delivering complete system protection functions including overcurrent, UVLO, bias supply OVP and OTP.

Table 1. PACKAGE INFORMATION(1)

ORDERABLE DEVICE	PINS	PACKAGE	OPERATING FREQUENCY	OPERATING TEMPERATURE
TPS92023D	8	SOIC	Variable	-40°C to 125°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com/package.

ABSOLUTE MAXIMUM RATINGS(1) (2) (3) (4)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNITS
		MIN	MAX	
Voltage range	VCC		22	V
	GD1, GD2	-0.5	V_{VCC} + 0.5	
Gate drive current – continuous	GD1, GD2		± 25	mA
Current range	RT		–5	
	DT		-0.7	
Operating junction temperature	T_J	−40	125	°C
Storage temperature	T_{stg}	−65	150	
Electrostatic Discharge	Human Body Model (HBM)		2,000	V
	Charged Device Model (CDM)		500	
Lead temperature (10 seconds)			260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) In normal use, terminals GD1 and GD2 are connected to an external gate driver and are internally limited in output current.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{VCC}	VCC input voltage from a low-impedance source	11.5		18.0	V
R_{RT}	RT resistor	1		8.666	kΩ
R_{DT}	DT resistor	3.3		39	
C_{SS}	SS capacitor	0.01		1	µF

THERMAL INFORMATION

THERMAL METRIC(1)		TPS92023 D (SOIC) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	117.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	63.4	
θ_{JB}	Junction-to-board thermal resistance(4)	57.5	
ψ_{JT}	Junction-to-top characterization parameter(5)	15.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	57.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, −40°C < T_A < 125°C, T_J = T_A, V_{VCC} = 12 V, GND = 0 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, C_{VCC} = 1 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY (VCC)						
	VCC current, disabled	SS = 0 V		1	1.5	mA
	VCC current, enabled	SS = 5 V, C_{GD1} = C_{GD2} = 1 nF	2.5	5	7.5	mA
	VCC current, UVLO	VCC = 9 V		100	400	µA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC rising	9.9	10.5	11.1	V
	UVLO turn-off threshold	Measured at VCC falling	8.9	9.5	10.1	V
	UVLO hysteresis	Measured at VCC	0.7	1	1.3	V
V_{OVP}	OVP turn-off threshold	Measured at VCC rising	18	20	22	V
	OVP turn-on threshold	Measured at VCC falling	16	18	20	V
	OVP hysteresis	Measured at VCC	1.5	2	2.5	V
DEAD TIME (DT)						
t_{DT}	Dead time	R_{DT} = 16.9 kΩ	390	420	450	ns
OSCILLATOR						
$f_{SW(min)}$	Minimum switching frequency at GD1, GD2	-40°C ≤ T_A ≤ 125°C	40.04	41.70	43.36	kHz
		-20°C ≤ T_A ≤ 105°C	40.45	41.70	42.95	kHz
K_{ICO}	Switching frequency gain/I (RT)	R_{RT} = 4.7 kΩ, I_{RT} = 0 to 1 mA	60	80	100	Hz/µA
t	GD1, GD2 on- time mismatching		-50		50	ns
$f_{SW(clamp)}$	Switching frequency clamp mode	V_{SS} = 5 V	330	380	430	kHz
$f_{SW(start)}$	Switching frequency at soft start	-40°C ≤ T_A ≤ 125°C	122	142.5	162	
		-20°C ≤ T_A ≤ 105°C	125	142.5	160	
EXTERNAL DISABLE/SOFT START						
	Enable threshold	Measure at SS rising	1.1	1.2	1.3	V
	Disable threshold	Measured at SS falling	0.85	1	1.1	V
	Disable hysteresis	Measured at SS	0.15		0.35	V
	Disable prop. delay	Measured between SS (falling) and GD2 (falling)	250	500	750	ns
I_{SS}	Source current on SS pin	V_{SS} = 0.5 V	-225	-175	-125	µA
	Source current on SS pin	V_{SS} = 1.35 V	-5.5	-5	-4.5	µA

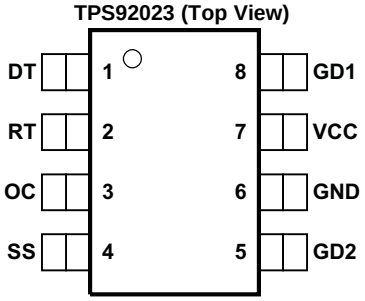
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, −40°C < T_A < 125°C, T_J = T_A, V_{VCC} = 12 V, GND = 0 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, C_{VCC} = 1 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PEAK CURRENT LIMIT						
$V_{OC1(off)}$	Level 1 over current threshold – V_{OC} rising		0.9	1	1.1	V
$V_{OC2(off)}$	Level 2 overcurrent latch threshold – V_{OC} rising		1.8	2.0	2.2	
$V_{OC1(on)}$	Level 1 over current threshold – V_{OC} falling		0.5	0.6	0.7	
t_{dOC}	Propagation delay		60	200	500	ns
I_{OC}	OC bias current	V_{OC} = 0.8 V	-200		200	nA
GATE DRIVE						
	GD1, GD2 output voltage high	I_{GD1} = −20 mA, I_{GD2} = −20 mA	9		11	V
	GD1, GD2 on-resistance high	I_{GD1} = −20 mA, I_{GD2} = −20 mA		12	30	Ω
	GD1, GD2 output voltage low	I_{GD1} = −20 mA, I_{GD2} = 20 mA		0.08	0.2	V
	GD1, GD2 on-resistance low	I_{GD1} = −20 mA, I_{GD2} = 20 mA		4	10	Ω
t_{RISE}	Rise time GDx	V_{VCC} rising from 1 V to 9 V, C_{LOAD} = 1 nF		18	35	ns
t_{FALL}	Fall time GDx	V_{VCC} falling from 9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GD1, GD2 output voltage during UVLO	V_{VCC} = 6 V, I_{GD1} = 1.2 mA, I_{GD2} = 1.2 mA	0.5		1.75	V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			160		°C
	Thermal shutdown recovery threshold			140		

DEVICE INFORMATION

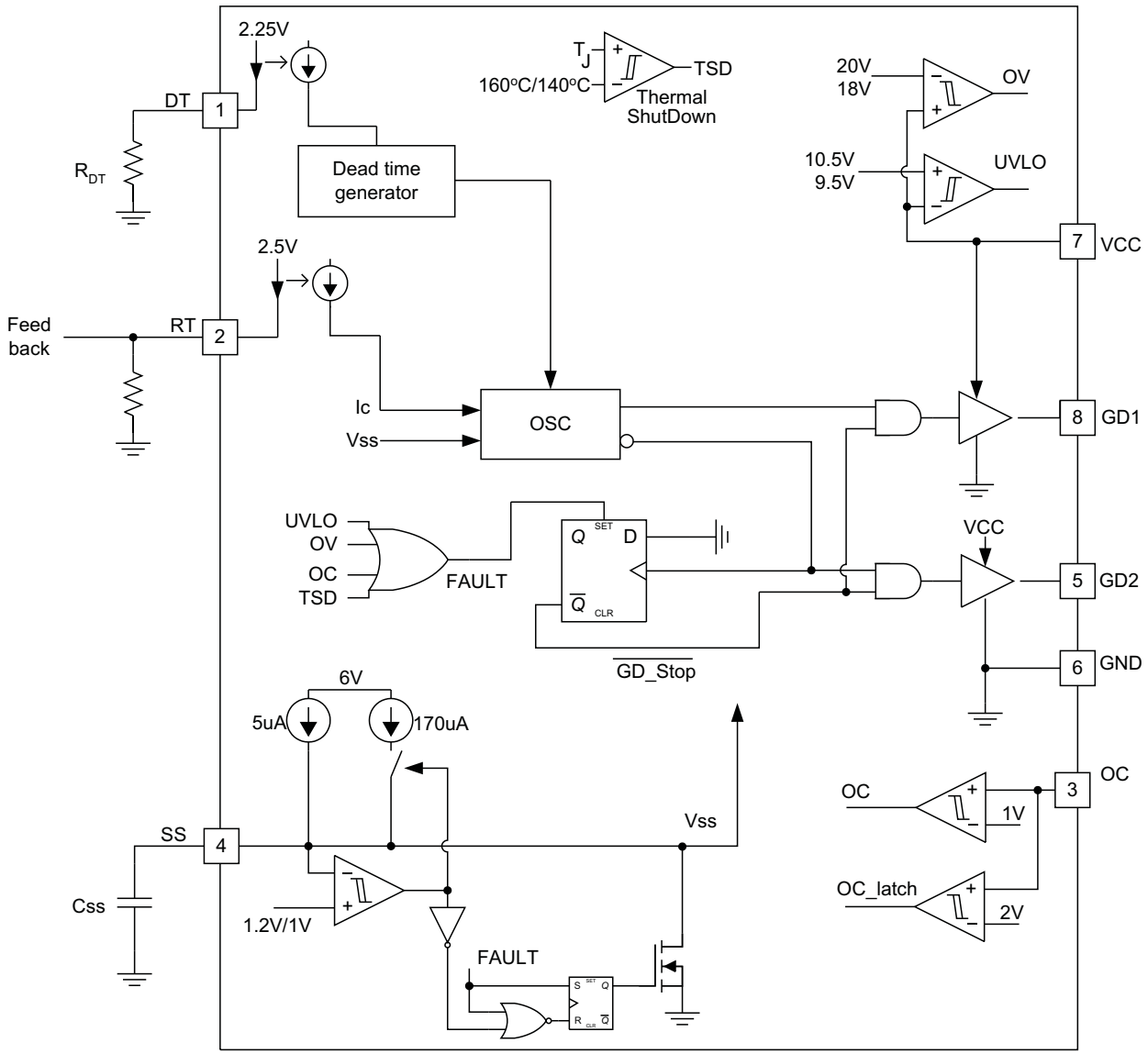
TPS92023 (Top View)



TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
DT	1	I	Sets the dead time of high-side and low-side switch driving signals. Connect a resistor to ground. With internal 2.25-V voltage reference, the current flowing through the resistor sets the dead time. To prevent shoot through when this pin is accidentally short to ground, the minimum dead time is set to 120 ns. Any dead time setting less than 120 ns defaults to 120-ns dead time.
GD1	8	O	High-side and low-side switch gate driver. Connect gate driver transformer primary side to these two pins to drive the half bridge.
GD2	5	O	
GND	6	-	Ground.
OC	3	I	Overcurrent protection. When the voltage on this pin is above 1 V, gate driver signals are actively pulled low. After the voltage falls below 0.6 V, the gate driver signal recovers with soft start. When OC pin voltage is above 2 V, the device is latched off. Bringing VCC below UVLO level resets the overcurrent latch off.
RT	2	I	The current flowing out of this pin sets the frequency of the gate driver signals. Connect the opto-coupler collector to this pin to control the switching frequency for regulation purpose. Parallel a resistor to ground to set the minimum current flowing out of the pin and set the minimum switching frequency. To set the maximum switching frequency limiting, place a resistor in series with the opto-coupler transistor. This resistor sets the maximum current flowing out of the pin and limits the maximum switching frequency.
SS	4	I	Soft-start. This pin sets the soft-start time of the system. Connect a capacitor to ground. Pulling this pin below 1 V disables the device to allow easy ON/OFF control. The soft-start function is enabled after all fault conditions, including bias supply OV, UVLO, overcurrent protection and over-temperature protection.
VCC	7	-	Bias supply. Connect this pin to a power supply less than 20 V. Place a 1-µF capacitor in parallel to ground to filter out noise.

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At V_{VCC} = 12 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, V_{SS} = 5 V, V_{OC} = 0 V; all voltages are with respect to GND, T_J = T_A = 25°C, unless otherwise noted.

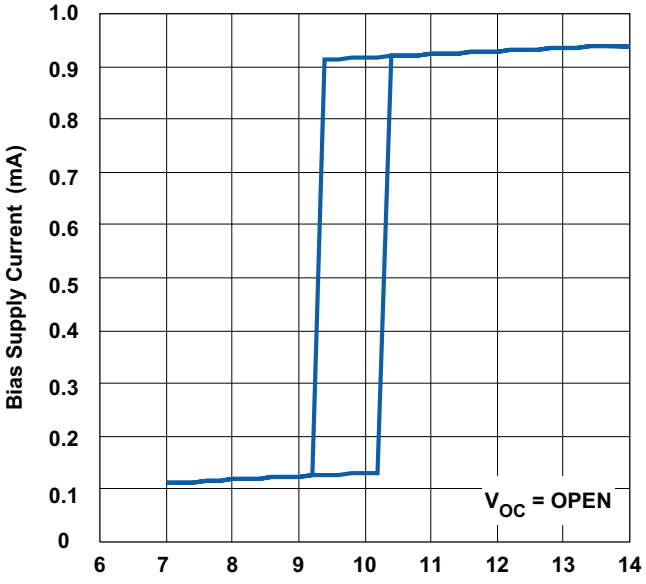


Figure 1. Bias Supply Current vs. Bias Supply Voltage

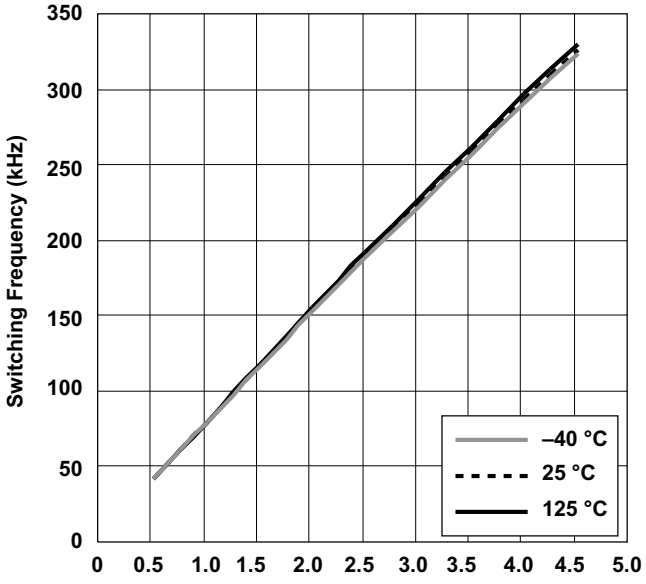


Figure 2. Switching Frequency vs. Timing Resistance

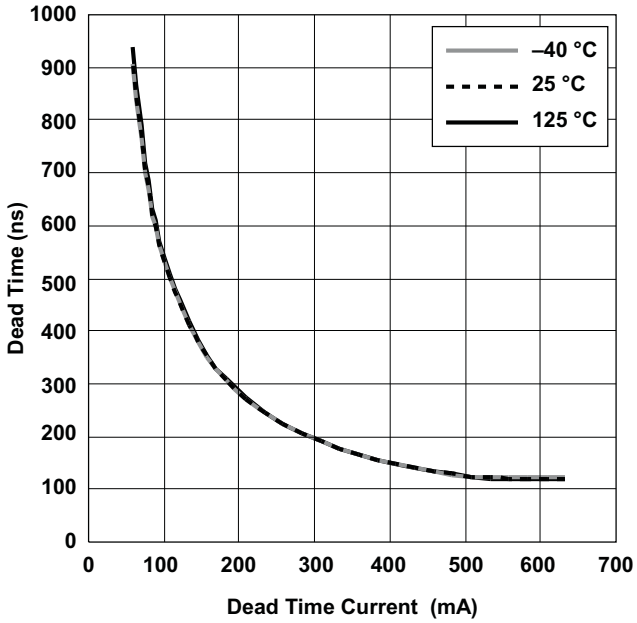


Figure 3. Dead Time vs. Dead Time Current

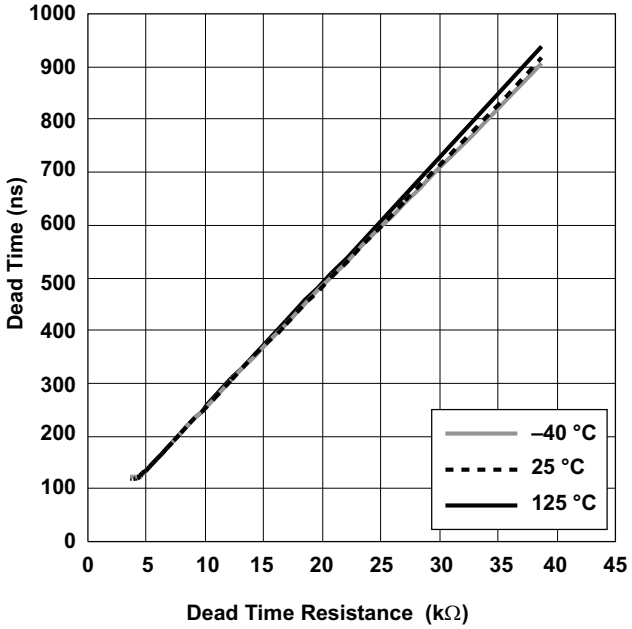


Figure 4. Dead Time vs. Dead Time Resistance

TYPICAL CHARACTERISTICS (continued)

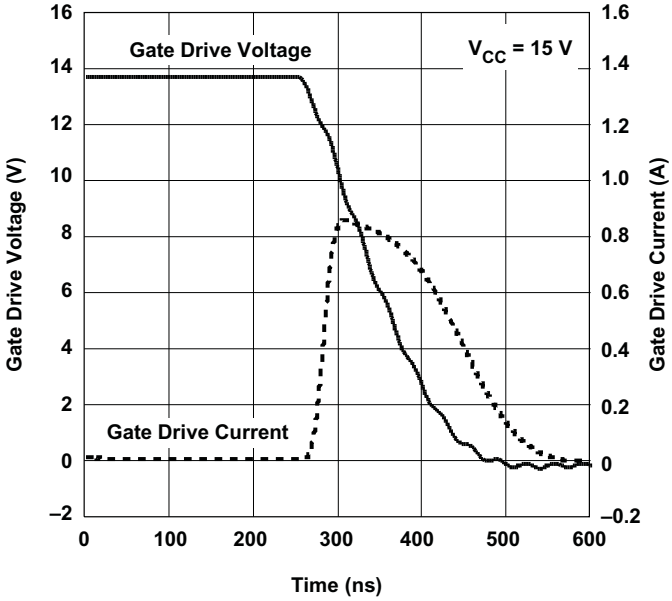


Figure 5. Gate Drive Voltage vs. Gate Drive Current vs. Time

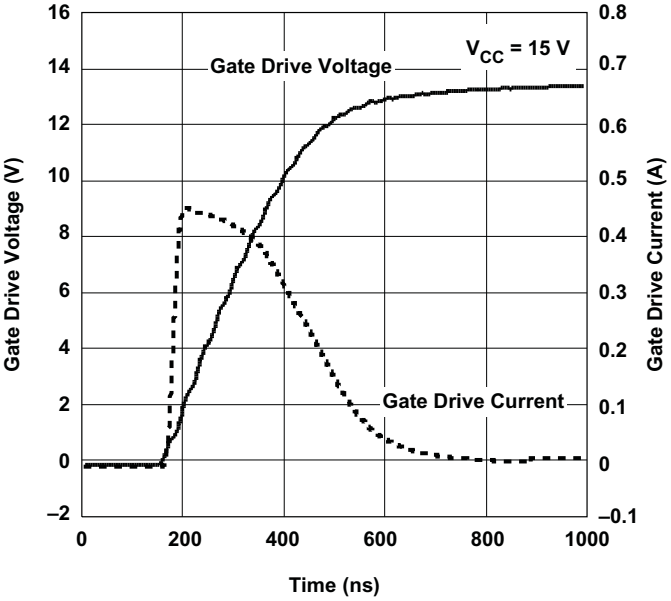


Figure 6. Gate Drive Voltage vs. Gate Drive Current vs. Time

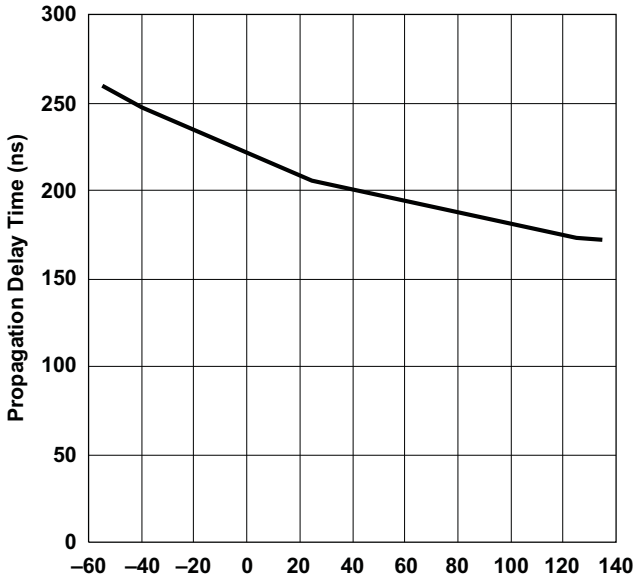


Figure 7. Propagation Delay Time vs. Temperature

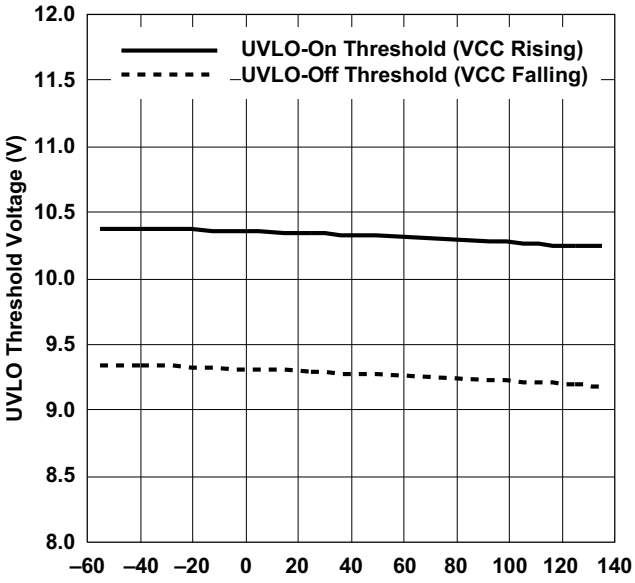


Figure 8. UVLO Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

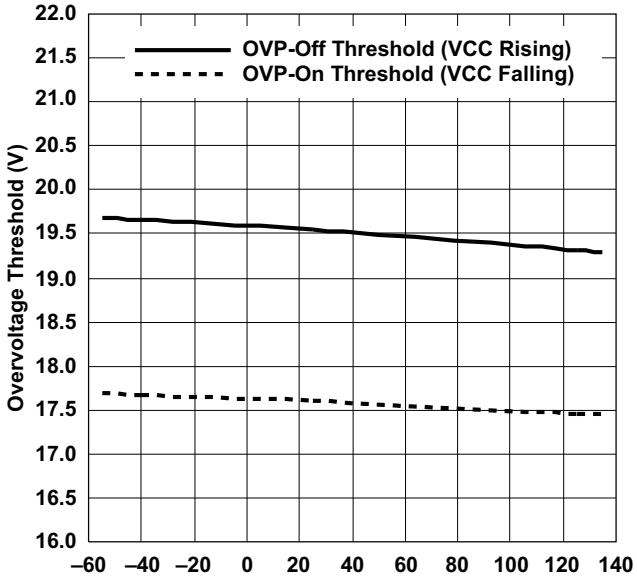


Figure 9. Overvoltage Threshold vs. Temperature

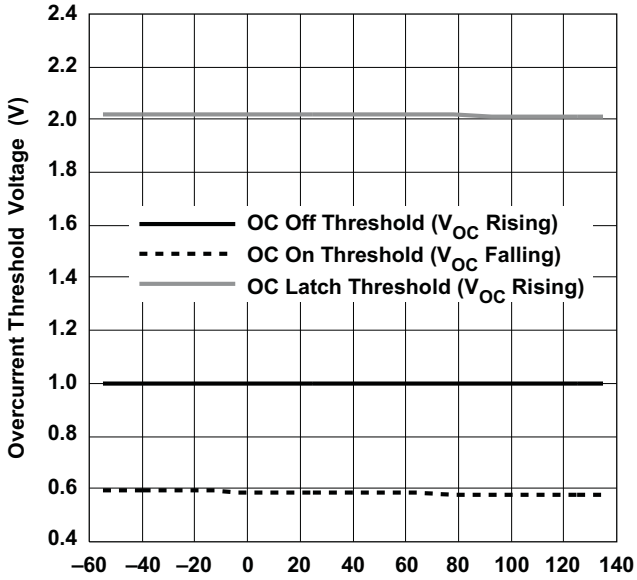


Figure 10. Overcurrent Threshold Voltage vs. Temperature

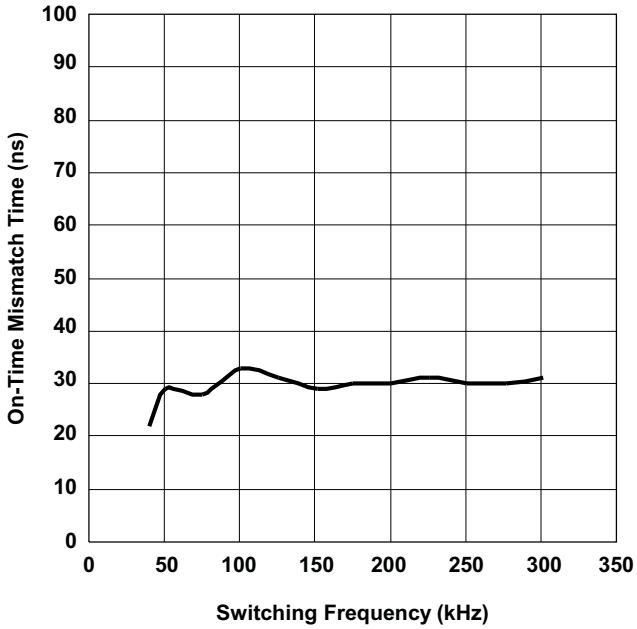


Figure 11. On-Time Mismatch vs. Switching Frequency

APPLICATION INFORMATION

Principle of Operation

The soft-switching capability, high efficiency and long holdup time make the LLC resonant converter attractive for many applications, such as digital TV, ac/dc adapters and computer power supplies. Figure 12 shows the schematic of the LLC resonant converter.

The LLC resonant converter is based on the series resonant converter (SRC). By using the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than resonant frequency. This simplifies the converter design to avoid the zero-current switching region, which can lead to system damage. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage boost PFC pre-regulator, allowing it to hold up through brief periods of ac line-voltage dropout.

Due to the nature of resonant converter, all the voltages and currents on the resonant components are approximately sinusoidal. The gain characteristic of LLC resonant converter is analyzed based on the First Harmonic Approximation (FHA), which means all the voltages and currents are treated as sinusoidal shape with the frequency same as switching frequency.

According to the operation principle of the converter, the LLC resonant converter can be draw as the equivalent circuit as shown in Figure 13.

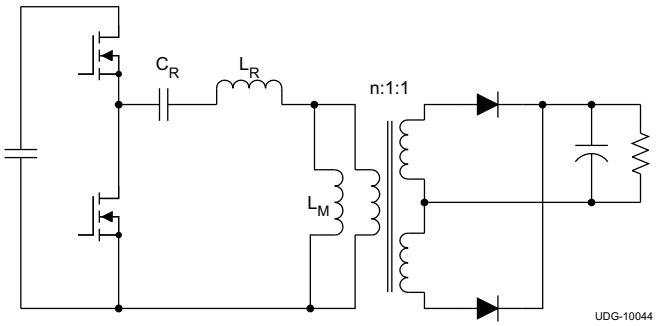


Figure 12. LLC Resonant Converter

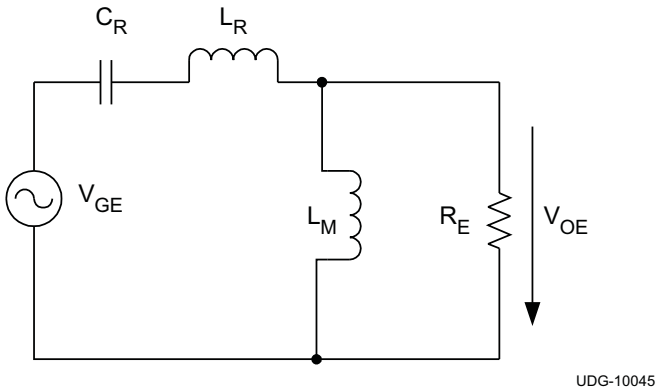


Figure 13. LLC Resonant Converter Equivalent Circuit

In this equivalent circuit, the V_{ge} and V_{oe} are the fundamental harmonics of the voltage generated by the half bridge and the voltage on the transformer primary side, respectively. These voltages can be calculated through Fourier analysis. The load resistor R_e is the equivalent resistor of the load, and it can be calculated as:

$$R_E = \left(\frac{8}{(\pi)^2}\right) \times (n)^2 \times R \tag{1}$$

Based on this equivalent circuit, the converter gain at different switching frequencies can be calculated as:

$$\left(\frac{V_{OUT}}{\left(\frac{V_{DC}}{2}\right)}\right) = \left| \frac{\frac{j\omega \times L_M \times R_E}{(j\omega \times L_M) + R_E}}{\frac{j\omega \times L_M \times R_E}{(j\omega \times L_M) + R_E} + \frac{1}{j\omega \times C_R} + j\omega \times L_R} \right| \tag{2}$$

where

- $V_{DC}/2$ is the equivalent input voltage due to the half-bridge structure

Table 2. Circuit Definition Calculations

NORMALIZED GAIN	RESONANT FREQUENCY	QUALITY FACTOR	NORMALIZED FREQUENCY	INDUCTOR RATIO
$M = \left(\frac{V_{OUT}}{\left(\frac{V_{DC}}{2} \right)} \right)$ (3)	$f_0 = \frac{1}{2\pi \times \sqrt{L_R \times C_R}}$ (4)	$Q_E = \frac{\sqrt{L_R / C_R}}{R_E}$ (5)	$f_n = \left(\frac{f}{f_0} \right)$ (6)	$L_n = \left(\frac{L_M}{L_R} \right)$ (7)

Following the definitions in Table 2, the converter gain at different switching frequencies can be calculated in Equation 8.

$$M = \frac{L_n \times (f_n)^2}{L_n \times (f_n)^2 + (f_n - 1) \times (f_n + 1 + j \times f_n \times L_n \times Q_e)}$$

where

- M is the converter voltage gain
- Ln is the ratio of the magnetizing inductance to the resonant inductance
- f_n is the normalized switching frequency
- Q_e is the quality factor (8)

Because of the FHA, Equation 8 is an approximation. When the switching frequency moves away from the resonant frequency, the error becomes larger. However, this equation can be used as the design tool. The final results need to be verified by the time based simulation or hardware test.

From Equation 8, when switching frequency is equal to resonant frequency, f_n = 1 and converter voltage gain is equal to 1. Converter gain at different loads and inductor ratio conditions are shown in Figure 14 through Figure 17.

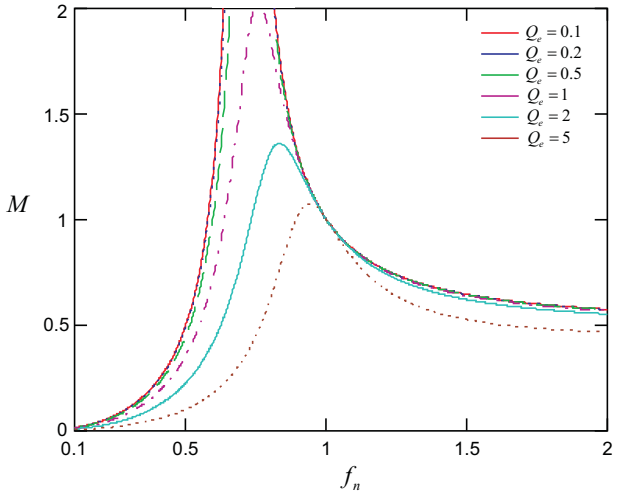


Figure 14. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=1

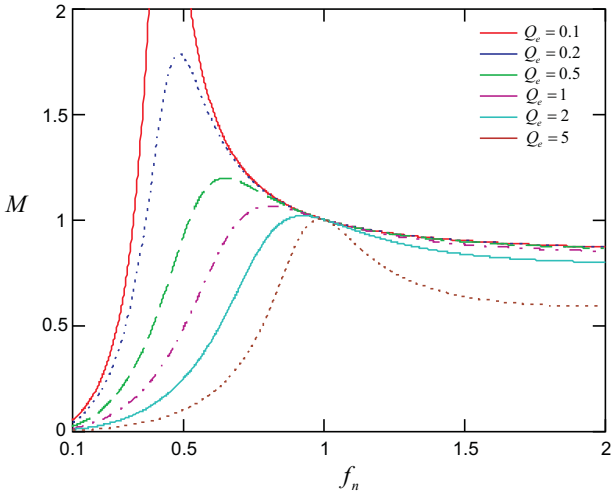


Figure 15. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=5

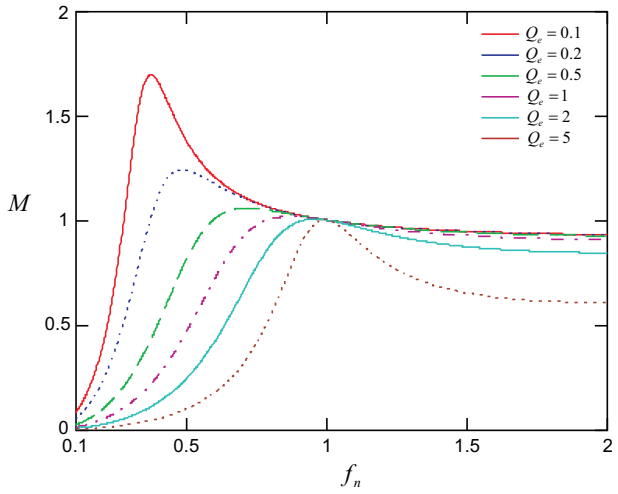


Figure 16. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=10

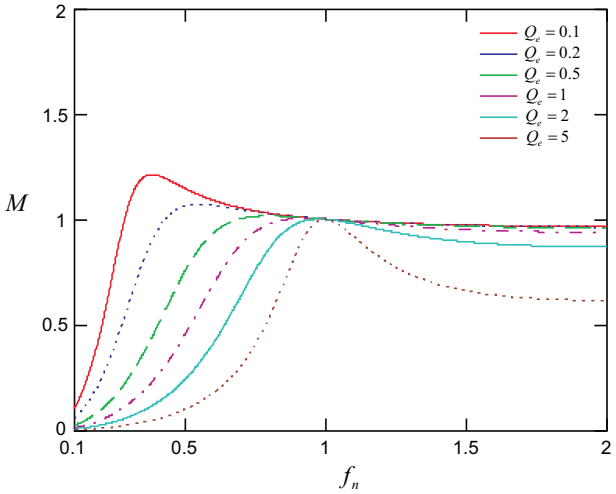


Figure 17. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=20

Based on its theory of operation the LLC resonant converter is controlled through Pulse Frequency Modulation (PFM). The output voltage is regulated by adjusting the switching frequency according to the input and output conditions. Optimal efficiency is achieved at the nominal input voltage by setting the switching frequency close to the resonant frequency. When the input voltage droops low the switching frequency is decreased to boost the gain and maintain regulation.

The TPS92023 resonant half-bridge controller uses variable switching frequency control to adjust the resonant tank impedance and regulate output voltage. This 8-pin package device integrates the critical functions for optimizing the system performance while greatly simplifying the design and layout.

Adjustable Dead Time

Resonant half-bridge converter relies on the resonant tank current at MOSFETs turn-off to achieve soft switching and reduce switching loss. Higher turn-off current provides more energy to discharge the junction capacitor, while it generates more turn-off loss. Smaller turn-off current reduces turn-off loss, but it requires longer time to discharge MOSFETs junction capacitors and achieve soft switching. By choosing an appropriate dead time, turn-off current is minimized while still maintaining zero-voltage switching, and best system performance is realized.

In TPS92023, dead time can be adjusted through a single resistor from DT pin to ground. With internal 2.25-V voltage reference, the current flow through the resistor sets the dead time.

$$t_D = 20\,ns + R_{DT} \times 24\,ns \tag{9}$$

To prevent shoot through when the DT pin accidentally connects to ground, the two gate driver outputs limit the dead-time to a minimum of 120-ns. Any dead-time setting less than 120-ns, defaults to the minimum 120-ns limit.

Oscillator

With variable switching frequency control, TPS92023 relies on the internal oscillator to vary the switching frequency. The oscillator is controlled by the current flowing out of RT pin. Except during soft start, the relationship between the gate signal frequency and the current flowing out of RT pin can be represented in Equation 10.

$$f_{SW} = \frac{1}{2} \times \frac{1}{\left(\frac{6\,ns \times 1A}{I_{RT}}\right) + 150\,ns} \approx I_{RT} \times 83\,Hz/\mu A \tag{10}$$

Since the switching frequency is proportional to the current, by limiting the maximum and minimum current flowing out of RT pin, the minimum and maximum switching frequency of the converter could be easily limited. As shown in Figure 18, putting a resistor from RT pin to ground limits the minimum current and putting a resistor in series with the opto-coupler limits the maximum current.

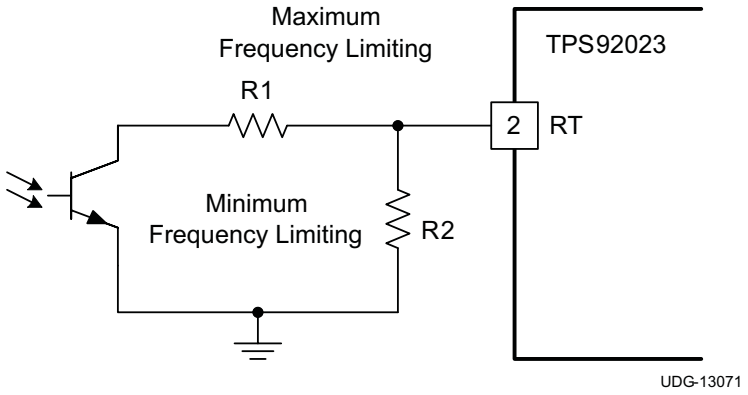


Figure 18. Maximum and Minimum Frequency Setting for TPS92023

The frequency limiting resistor can be calculated in Equation 11 through Equation 14.

$$I_{F(max)} = \frac{6\,ns}{\left(\frac{1}{(2 \times f_{MAX})}\right) - 150\,ns} \tag{11}$$

$$I_{F(max)} = 2.5\,V\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{12}$$

$$I_{F(min)} = \frac{6\,ns}{\left(\frac{1}{(2 \times f_{MIN})}\right) - 150\,ns} \tag{13}$$

$$I_{F(min)} = \frac{2.5\,V}{R_2} \tag{14}$$

Soft Start

During start up and fault recovery conditions, soft start is always implemented to prevent excessive resonant tank current and ensure Zero-Voltage Switching (ZVS). During soft start, the switching frequency is increased. The soft-start time can be programmed by placing a capacitor from SS pin to ground.

The soft-start pin also serves as an ON/OFF control pin of the device. By actively pulling the SS pin below 1 V, the device is disabled. When the pull down is removed, SS pin voltage is increased because of internal charging current. Once SS pin becomes above 1.2 V, the device starts to generated gate-driver signal and enters soft-start mode. The time sequence of soft start is shown in Figure 19.

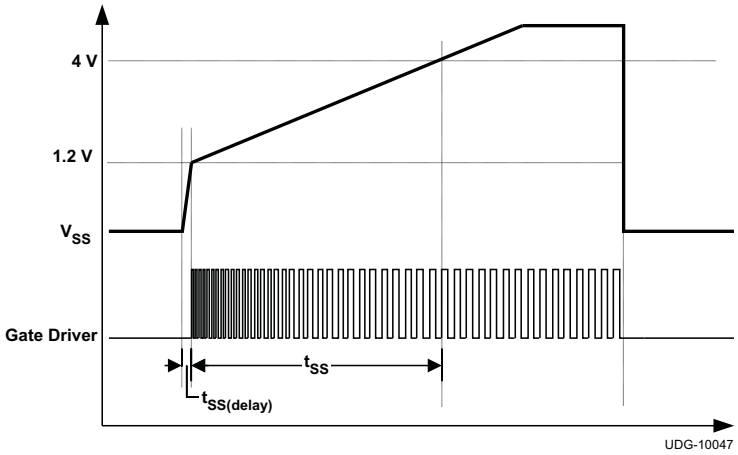


Figure 19. Soft-Start Sequence

To prevent a long delay between the ON command and appearance of a gate driver signal, the SS pin current is set as two different levels. When SS pin voltage is below 1.2 V, its output current is 175 µA. This high current could charge the soft-start pin capacitor to 1.2 V in a short period of time, and reduces the time delay. This time delay is calculated in Equation 15.

$$t_{SS(delay)} = \frac{1.2\,V}{175\,\mu A} \times C_{SS} \tag{15}$$

The switching frequency during soft start is determined by both the current flowing out of the RT pin and the voltage on SS pin. The switching frequency can be calculated based on the Equation 16.

$$f_{SW} = \frac{1}{2} \times \frac{1}{\frac{6\,ns \times 1A}{I_{RT} + \left(1.81mA - \frac{V_{VSS}}{2.2k\Omega}\right)} + 150\,ns} \tag{16}$$

After the SS pin voltage reaches 4 V, the soft-start period ends and the switching frequency equals that as demanded by the RT pin current. The time used to charge the SS pin from 1.2 V to 4 V is defined as the soft-start time and can be calculated in Equation 17.

$$t_{SS} = \frac{2.8\,V}{5\,\mu A} \times C_{SS} \tag{17}$$

To ensure reliable operation, the gate drivers restart with GD2 turning high. This prevents uncertainty during system start up.

Overcurrent Protection

To prevent power stage failure under excessive load current condition, the TPS92023 includes an overcurrent protection function. With a dedicated OC pin, the power stage is shut down when OC pin voltage is above 1 V. Once the OC pin voltage falls below 0.6 V, the gate driver recovers with a soft start. To enhance system safety, the TPS92023 latches up the entire system when the OC pin voltage rises above 2 V. Bringing the VCC voltage below the UVLO voltage level resets the device.

The current can be indirectly sensed through the voltage across resonant capacitor by using the sensing network shown in Figure 20.

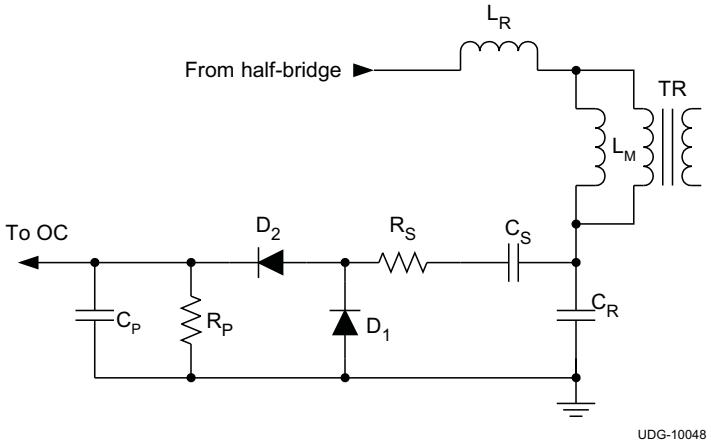


Figure 20. Current Sensing for LLC Resonant Converter

The general concept of this sensing method is that the ac voltage across the resonant capacitor is proportional to load current.

According to the FHA model, peak voltage of the ac component on the resonant capacitor can be calculated in Equation 18.

$$V_{CR(pk)} = \frac{4}{\pi} \times n \times V_{OUT} \left| \frac{j\omega_n \times L_n \times (Q_e + 1)}{(\omega_n)^2 \times L_n} \right| \quad (18)$$

Therefore, the resonant capacitor voltage reaches its maximum value at the minimum switching frequency and maximum load. According to Equation 18, the current sensing network components can be calculated. Due to the nature of FHA, the final circuit parameters must be verified through actual hardware test.

Table 3. Calculated Current Sensing Network Components

SYMBOL	FUNCTION	DESIGN EQUATION
R_S	Transfer ac voltage across resonant capacitor into current source	$R_s = \frac{\left(V_{CR(pk)MAX}\right)^2}{2 \times P_{RS(max)}}$ (19)
C_S	Blocking dc voltage on resonant capacitor	$C_S = \frac{10}{R_S \times f_{MIN}}$ (20)
R_P	Load resistor of the current source	$R_P = \frac{R_S}{V_{CR(pk)MAX}} \times \frac{\pi}{2}$ (21)
C_P	Filter capacitor	$C_P = \frac{10}{(R_P \times f_{MIN})}$ (22)

Gate Driver

Half-bridge resonant converter is controlled by the nearly 50% duty cycle variable frequency square wave voltage. This allows the half bridge to be easily driven by the gate-driver transformer. Compared with a half-bridge driver device, a gate-driver transformer provides a simple and reliable solution, which:

- Eliminate the need for gate driver power supply
- Enable simplified layout
- Preventing shoot through due to the transformer coupling
- No latch up

The TPS92023 integrates two-gate drivers with 0.4-A source and 0.8-A sink capability to directly drive the gate driver transformer.

For LLC resonant converter, it is critical for the gate-driver signal to be precisely symmetrical. Otherwise, the resonant tank operation is symmetrical. The load current distribution is unbalanced for the output rectifiers, which in turn requires over design of the power stages and thermal management.

In TPS92023, the gate-driver output is precisely trimmed to have less than 50 ns mismatch. Although the gate-driver signal is quite symmetrical, it is still recommended to insert the dc blocking capacitor in the gate-driver transformer primary side to prevent transformer saturation during fast transients.

VCC Pin

Connect a regulated bias supply to VCC pin. When VCC becomes above 10.5 V the device is enabled and after all fault conditions are cleared the gate driver starts with soft start. When the VCC voltage drops below 9.5 V, the device enters UVLO protection mode and both gate drivers are actively pulled low. When VCC rises above 20 V the device enters VCC overvoltage protection mode and the device is disabled with both gate drivers actively pulled low. VCC overvoltage protection recovers with soft-start operation when the VCC voltage returns below 18 V.

Over-Temperature Protection

TPS92023 continuously senses its junction temperature. When the junction temperature rises above 160°C the device enters over-temperature protection mode with both gate drivers actively pulled low. When junction temperature drops below 140°C, gate driver restarts with soft start.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92023D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92023D	Samples
TPS92023DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92023D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

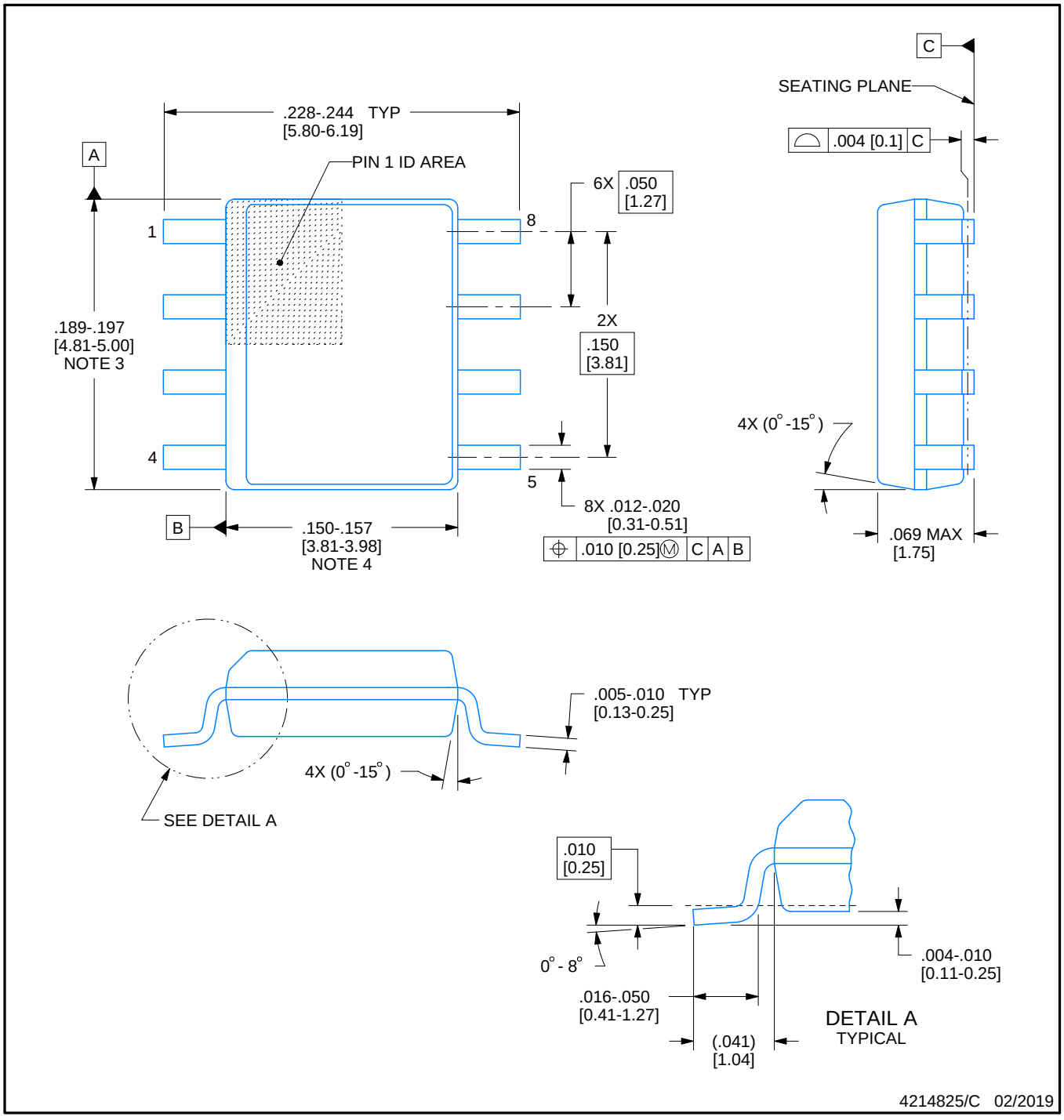
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

D0008A

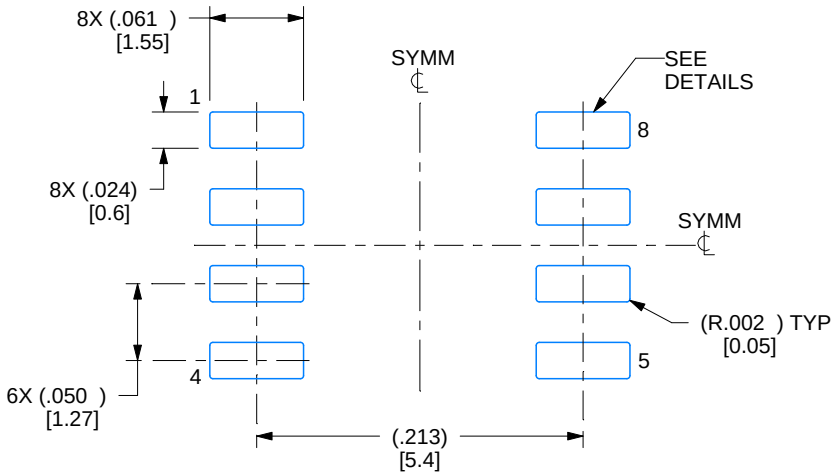
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

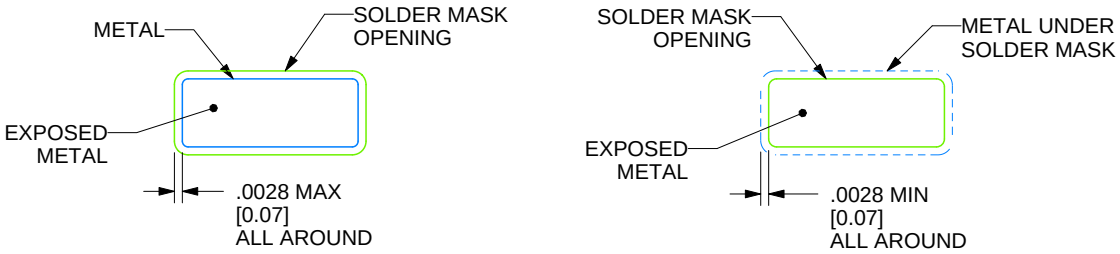


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

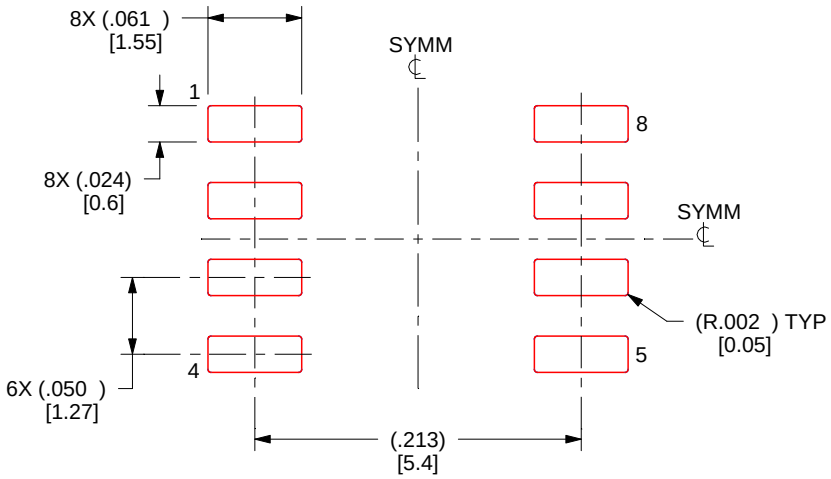
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

单击下面可查看定价，库存，交付和生命周期等信息

>>TI(德州仪器)