TEXAS INSTRUMENTS

TPS2H000-Q1

SLVSD72D – DECEMBER 2015 – REVISED DECEMBER 2019

TPS2H000-Q1 40-V, 1000-mΩ Dual-Channel Smart High-Side Power Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C4B
- Functional safety capable
  - Documentation available to aid functional safety system design
- Dual-Channel 1000-mΩ smart high-side switch with full diagnostics
  - Version A: Open-drain status output
  - Version B: Current-Sense analog output
- Wide operating voltage 3.4 to 40 V
- Ultralow standby current, <500 nA
- High-Accuracy current sense:
  - ±10% Under >5-mA load
- Adjustable current limit with external resistor ±20% under >100-mA load
- Protection:
  - Short-to-GND protection by current limit (internal or external)
  - Thermal shutdown with latch-off option and thermal swing
  - Inductive load negative voltage clamp with optimized slew rate
  - Loss of GND and loss of battery protection

- Diagnostic:
  - Overcurrent and short-to-ground detection
  - Open-Load and short-to-battery detection
  - Global fault for fast interrupt
- 16-Pin Thermally-Enhanced PWP package

2 Applications

- Dual-Channel LED drivers
- Dual-Channel high-side switches for sub-modules
- Dual-Channel high-side relay drivers

3 Description

The TPS2H000-Q1 family is a fully protected dual-channel smart high-side switch, with integrated 1000-mΩ NMOS power FETs.

Full diagnostics and high-accuracy current-sense features enable intelligent control of the load.
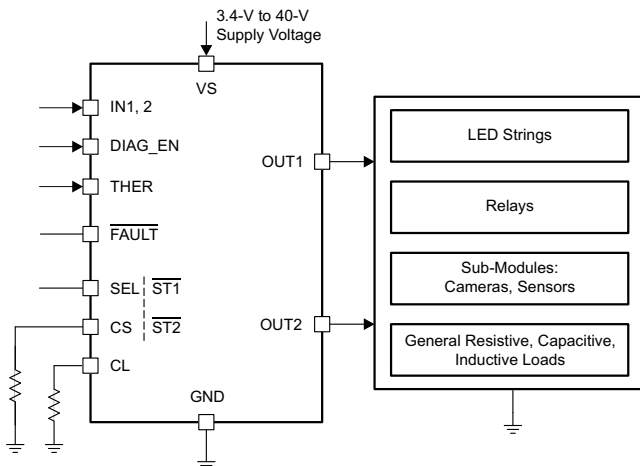
An external adjustable current limit improves reliability of the whole system by limiting the inrush or overload current.

Device Information[1]

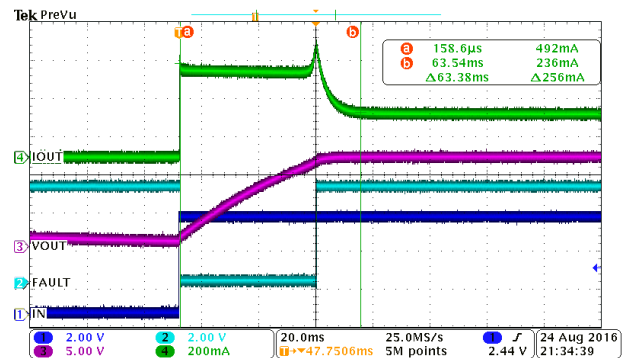| PART NUMBER	PACKAGE	CHANNELS
TPS2H000-Q1 Ver. A	HTSSOP (16)	2
TPS2H000-Q1 Ver. B		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

Driving a Capacitive Load With Adjustable Current Limit

Table of Contents

4 Revision History

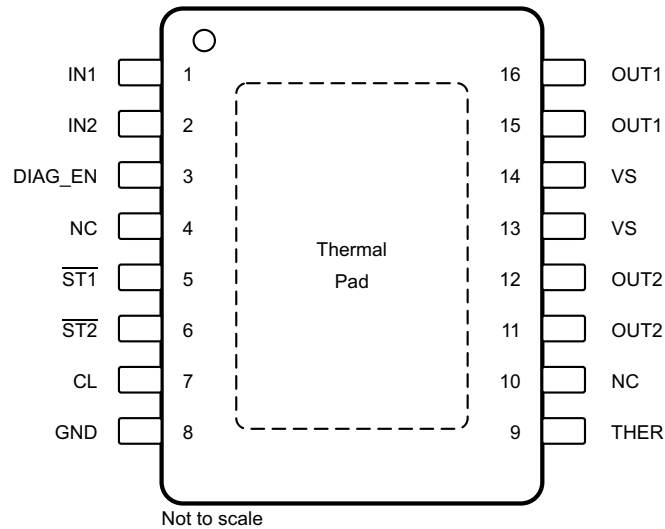**Changes from Revision C (July 2019) to Revision D**   **Page**

- Added Functional safety capable link to the *Features* section 1

Changes from Revision B (March 2018) to Revision C   **Page**

- Changed the adjustable current limit from 2.5 A to 0.5 A in the *Detailed Design Procedure* section 28

Changes from Revision A (October 2016) to Revision B   **Page**

- Added footnote 2 to the *Electrical Characteristics* table 8
- Added reverse current protection information to the *Reverse-Current Protection* section 24

Changes from Original (December 2015) to Revision A   **Page**

- Changed data sheet from PRODUCT PREVIEW to PRODUCTION DATA 1

5 Device Comparison Table

PART NUMBER	FAULT REPORTING MODE
TPS2H000-Q1 Version A	Open-drain digital output
TPS2H000-Q1 Version B	Current-sense analog output

6 Pin Configuration and Functions

PWP PowerPAD™ Package
16-Pin HTSSOP With Exposed Thermal Pad
TPS2H000-Q1 Version A Top View

Pin	Left	Pin	Right
1	IN1	16	OUT1
2	IN2	15	OUT1
3	DIAG_EN	14	VS
4	NC	13	VS
5	$\overline{ST1}$	12	OUT2
6	$\overline{ST2}$	11	OUT2
7	CL	10	NC
8	GND	9	THER

Thermal Pad

Not to scale

NC – No internal connection

PWP PowerPAD Package
16-Pin HTSSOP With Exposed Thermal Pad
TPS2H000-Q1 Version B Top View

IN1	1	16 OUT1
IN2	2	15 OUT1
DIAG_EN	3	14 VS
$\overline{FAULT}$	4	13 VS
SEL	5	Thermal Pad	12 OUT2
CS	6	11 OUT2
CL	7	10 NC
GND	8	9 THER

Not to scale
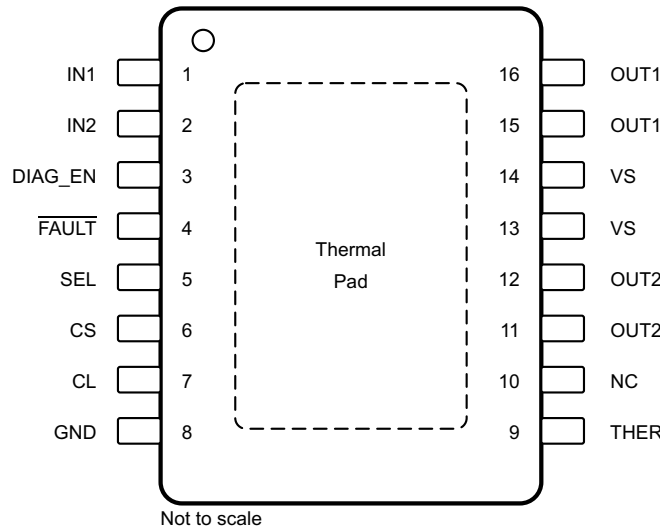
NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	VERSION A	VERSION B		
CL	7	7	O	Adjustable current limit. Connect to device GND if external current limit is not used.
CS	—	6	O	Current-sense output
DIAG_EN	3	3	I	Enable-disable pin for diagnostics; internal pulldown
$\overline{FAULT}$	—	4	O	Global fault report with open-drain structure, ORed logic for dual-channel fault conditions
GND	8	8	—	Ground pin
IN1	1	1	I	Input control for channel 1 activation; internal pulldown
IN2	2	2	I	Input control for channel 2 activation; internal pulldown
NC	4, 10	10	—	No internal connection
$\overline{ST1}$	5	—	O	Open-drain diagnostic status output for channel 1
$\overline{ST2}$	6	—	O	Open-drain diagnostic status output for channel 2
SEL	—	5	I	CS channel-selection bit; internal pulldown
THER	9	9	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown
OUT1	15, 16	15, 16	O	Output of the channel 1 high side-switch, connected to the load
OUT2	11, 12	11, 12	O	Output of the channel 2 high side-switch, connected to the load
VS	13, 14	13, 14	I	Power supply
Thermal pad	—	—	—	Connect to device GND or leave floating

Product Folder Links: *TPS2H000-Q1*

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) [1][2]

		MIN	MAX	UNIT
Supply voltage	t < 400 ms		45	V
Reverse polarity voltage[3]		−36		V
Current on GND pin	t < 2 minutes	−100	250	mA
Voltage on INx, DIAG_EN, SEL, and THER pins		−0.3	7	V
Current on INx, DIAG_EN, SEL, and THER pins		−10	—	mA
Voltage on $\overline{STx}$ or $\overline{FAULT}$ pins		−0.3	7	V
Current on $\overline{STx}$ or $\overline{FAULT}$ pins		−30	10	mA
Voltage on CS pin		−2.7	7	V
Current on CS pin		—	30	mA
Voltage on CL pin		−0.3	7	V
Current on CL pin		—	6	mA
Inductive load switch-off energy dissipation, single pulse, single channel[4]		—	40	mJ
Operating junction temperature, T_J		−40	150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground plane.
(3) Reverse polarity condition: t < 60 s, reverse current < $I_{R(2)}$, V_{INx} = 0 V, all channels reverse, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: V_{VS} = 13.5 V, L = 300 mH, T_J = 150°C. FR4 2s2p board, 2 × 70-μm Cu, 2 × 35-μm Cu. 600 mm^2 thermal pad copper area.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	All pins	±4000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	
			Corner pins (1, 8, 9, and 16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VS}	Supply operating voltage	4	40	V
	Voltage on INx, DIAG EN, SEL, and THER pins	0	5	V
	Voltage on $\overline{STx}$ and $\overline{FAULT}$ pins	0	5	V
	Nominal dc load current	0	0.75	A
T_A	Operating ambient temperature	−40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS2H000-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		TPS2H000-Q1	UNIT
		PWP (HTSSOP)	
		16 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

7.5 Electrical Characteristics

5 V < V_{VS} < 40 V; −40°C < T_J < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{VS(nom)}$	Nominal operating voltage		4		40	V
$V_{VS(uvr)}$	Undervoltage turnon	V_{VS} rises up	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	V_{VS} falls down	3	3.2	3.4	V
$V_{(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V

Product Folder Links: *TPS2H000-Q1*

Electrical Characteristics (continued)

$5\ V < V_{VS} < 40\ V$; $-40°C < T_J < 150°C$, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
$I_{(op)}$	Nominal operating current[1]	V_{VS} = 13.5 V, V_{INx} = 5 V, V_{DIAG_EN} = 0 V, I_{OUTx} = 0.1 A, current limit = 0.5 A, all channels on			7	mA
$I_{(off)}$	Standby current	V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTx} = THER = 0 V, T_J = 25°C			0.5	µA
		V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTx} = THER = 0 V, T_J = 125°C			3	
$I_{(off,diag)}$	Standby current with diagnostic enabled	V_{VS} = 13.5 V, V_{INx} = 0 V, V_{DIAG_EN} = 5 V, V_{VS} − V_{OUTx} > $V_{(ol,off)}$, not in open-load mode			3	mA
$t_{(off,diag)}$	Standby mode deglitch time[1]	IN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode.	10	12.5	15	ms
$I_{lkg(out)}$	Output leakage current in off-state	V_{VS} = 13.5 V, V_{INx} = V_{OUTx} = 0, V_{DIAG_EN} = 5 V			2	µA
POWER STAGE						
$r_{DS(on)}$	On-state resistance[1]	V_{VS} ≥ 3.5 V, T_J = 25°C		1000		mΩ
		V_{VS} ≥ 3.5 V, T_J = 150°C			2000	
$I_{CL(int)}$	Internal current limit	Internal current limit value, CL pin connected to GND	1		1.6	A
$I_{CL(TSD)}$	Current limit during thermal shutdown[1]	Internal current limit value under thermal shutdown		0.8		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		60%		
$V_{DS(clamp)}$	Drain-to-source internal clamp voltage			46	65	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain−source diode voltage	IN = 0, I_{OUTx} = −0.15 A.	0.3	0.8	1	V
$I_{R(1)}$, $I_{R(2)}$	Continuous reverse current from source to drain[1]	t < 60 s, V_{INx} = 0 V, T_J = 25°C, single channel reversed, short-to-battery condition		1		A
		t < 60 s, V_{INx} = 0 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. Reverse-polarity condition, all channels reversed		1		
LOGIC INPUT (INx, DIAG_EN, SEL, THER)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(logic,pd)}$	Logic-pin pulldown resistor	INx, SEL, THER, V_{INx} = V_{SEL} = V_{THER} = 5 V	100	175	250	kΩ
		DIAG_EN. V_{VS} = V_{DIAG_EN} = 5 V	150	275	400	
DIAGNOSTICS						
$I_{lkg(GND\_loss)}$	Output leakage current under GND loss condition				100	µA
$V_{(ol,off)}$	Open-load detection threshold	IN = 0 V, when V_{VS} − V_{OUTx} < $V_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state	1.6		2.6	V
$t_{d(ol,off)}$	Open-load detection threshold deglitch time (see Figure 3)	IN = 0 V, when V_{VS} − V_{OUTx} < $V_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state	300	600	800	µs
$I_{(ol,off)}$	Off-state output sink current	V_{INx} = 0 V, V_{DIAG_EN} = 5 V, V_{VS} = V_{OUTx} = 13.5 V, T_J = 125°C, open load	−75			µA
$V_{OL(STx)}$	Status low-output voltage	I_{STx} = 2 mA, version A only			0.2	V
$V_{OL(FAULT)}$	Fault low-output voltage	I_{FAULT} = 2 mA, version B only			0.2	V
$t_{CL(deg)}$	Deglitch time when current limit occurs[1]	V_{INx} = V_{DIAG_EN} = 5 V, the deglitch time from current limit toggling to FAULT, STx, CS report.	80		180	µs
$T_{(SD)}$	Thermal shutdown threshold[1]		160	175		°C
$T_{(SD,rst)}$	Thermal shutdown status reset threshold[1]			155		°C
$T_{(SW)}$	Thermal swing shutdown threshold[1]			60		°C
$T_{(hys)}$	Hysteresis for resetting the thermal shutdown or thermal swing[1]			10		°C

(1) Value specified by design, not subject to production test

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Product Folder Links: *TPS2H000-Q1*

Electrical Characteristics (continued)

5 V < V_{VS} < 40 V; −40°C < T_J < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE (Version B) AND CURRENT LIMIT						
$K_{(CS)}$	Current-sense ratio			80		
$K_{(CL)}$	Current-limit ratio			300		
$V_{CL(th)}$	Current limit internal threshold[1]			0.8		V
$dK_{(CS)}$ / $K_{(CS)}$	Current-sense accuracy, ($I_{CS} \times K_{(CS)} - I_{OUTx}$) /$I_{OUTx} \times 100$	V_{VS} = 13.5 V, $I_{OUTx} \geq$ 1 mA	−50%		50%	
		V_{VS} = 13.5 V, $I_{OUTx} \geq$ 2 mA	−25%		25%	
		V_{VS} = 13.5 V, $I_{OUTx} \geq$ 5 mA	−10%		10%	
		V_{VS} = 13.5 V, $I_{OUTx} \geq$ 25 mA	−3%		3%	
		V_{VS} = 13.5 V, $I_{OUTx} \geq$ 100 mA	−2.5%		2.5%	
$dK_{(CL)}$ / $K_{(CL)}$	External current limit accuracy[2] ($I_{OUTx} - I_{CL} \times K_{(CL)}$) $\times$ 100 / ($I_{CL} \times K_{(CL)}$)	V_{VS} = 13.5 V, $I_{(limit)} \geq$ 50 mA	−25%		25%	
		$I_{(limit)} \geq$ 100 mA	−20%		20%	
		$I_{(limit)} \geq$ 200 mA	−15%		15%	
		V_{VS} = 13.5 V, 0.5 A $\leq I_{(limit)} \leq$ 0.9 A	−10%		10%	
$V_{CS(lin)}$	Current-sense voltage linear range[1]	$V_{VS} \geq$ 6.5 V	0		4	V
		5 V $\leq V_{VS}$ < 6.5 V	0		$V_{VS} -$ 2.5	
$I_{OUTx(lin)}$	Output-current linear range[1]	V_{VS} = 13.5 V, $V_{CS(lin)} \leq$ 4 V	0		0.75	A
		5 V $\leq V_{VS}$ < 6.5 V, $V_{CS(lin)} \leq V_{VS} -$ 2.5 V	0		0.5	
$V_{CS(H)}$	Current sense pin output voltage[1]	$V_{VS} \geq$ 7 V, fault mode	4.5		6.5	V
		5 V $\leq V_{VS}$ < 7 V, fault mode	Min($V_{VS} -$ 2, 4.5)		6.5	V
$I_{CS(H)}$	Current-sense pin output current	V_{CS} = 4.5 V, V_{VS} = 13.5 V		15		mA
$I_{lkg(CS)}$	Current-sense leakage current in disabled mode	V_{DIAG_EN} = 0 V, T_J = 125ºC			0.5	µA

(2)   External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting

7.6   Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Delay time, V_{OUTx} 10% after $V_{INx}\uparrow$ (See Figure 1.)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, IN rising edge to 10% of V_{OUTx}	10	30	60	µs
$t_{d(off)}$	Delay time, V_{OUTx} 90% after $V_{INx}\downarrow$ (See Figure 1.)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, IN falling edge to 90% of V_{OUTx}	10	30	60	µs
dV/dt(on)	Turnon slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, V_{OUTx} from 10% to 90%	0.1	0.25	0.5	V/µs
dV/dt(off)	Turnoff slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, V_{OUTx} from 90% to 10%	0.3	0.5	0.9	V/µs
$t_{d(match)}$	$t_{d(rise)} - t_{d(fall)}$ (See Figure 1.)	V_{VS} = 13.5 V, I_L = 0.1 A. $t_{d, rise}$ is the IN rising edge to V_{OUTx} = 90%. $t_{d(fall)}$ is the IN falling edge to V_{OUTx} = 10%.	−60		60	µs
CURRENT-SENSE CHARACTERISTICS (See Figure 2.)						
$t_{CS(off1)}$	CS settling time from DIAG_EN disabled[1]	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUTx} = 0.1 A. current limit = 0.5 A. DIAG_EN falling edge to 10% of V_{CS}.			20	µs
$t_{CS(on1)}$	CS settling time from DIAG_EN enabled[1]	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUTx} = 0.1 A. current limit is 0.5 A. DIAG_EN rising edge to 90% of V_{CS}.			20	µs
$t_{CS(off2)}$	CS settling time from IN falling edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A. current limit = 0.5 A. IN falling edge to 10% of V_{CS}			70	µs
$t_{CS(on2)}$	CS settling time from IN rising edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A. current limit = 0.5 A. IN rising edge to 90% of V_{CS}	40		120	µs
t_{SEL}	Multi-sense transition delay from channel to channel	V_{DIAG_EN} = 5 V, current sense output delay when multi-sense pin SEL transitions from channel to channel			50	µs

(1)   Value specified by design, not subject to production test

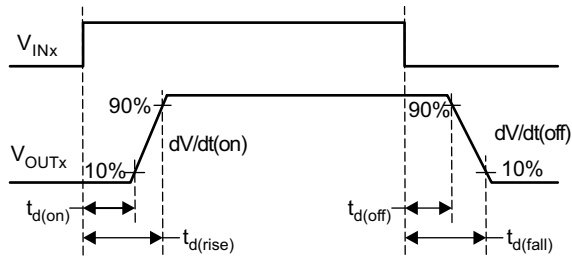Product Folder Links: *TPS2H000-Q1*
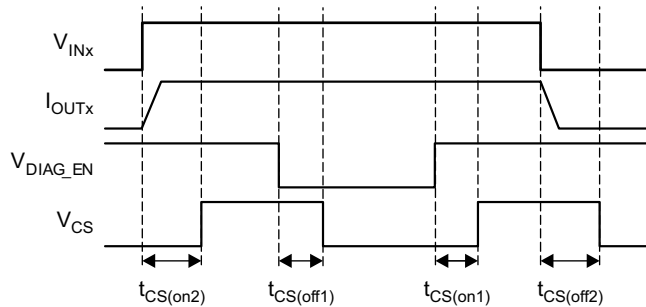
Figure 1. Output Delay Characteristics
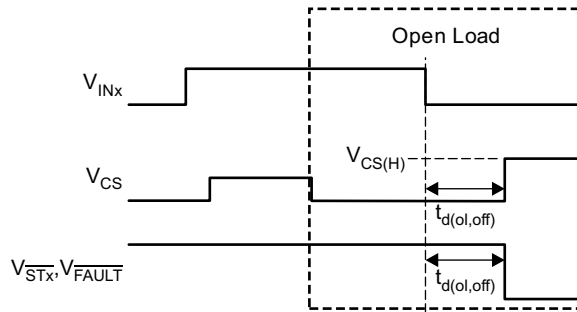

Figure 2. CS Delay Characteristics
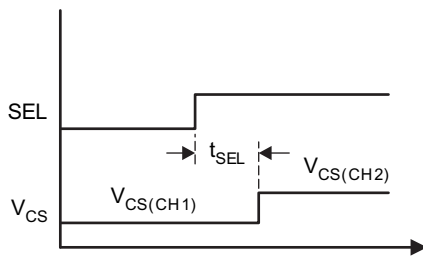

Figure 3. Open-Load Blanking-Time Characteristics

Figure 4. Multi-Sense Transition Delay
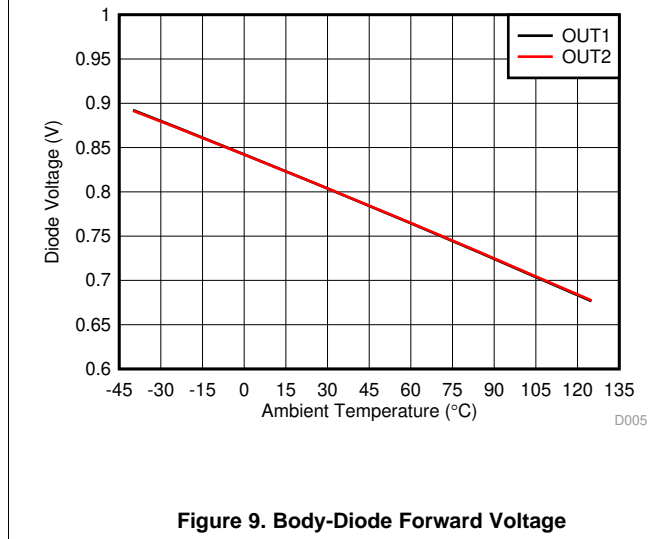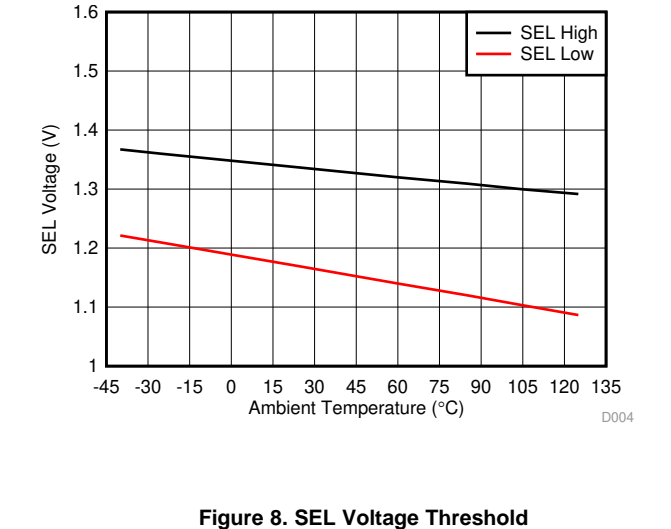
Product Folder Links: *TPS2H000-Q1*

7.7 Typical Characteristics

Figure 5. UVLO Voltage Threshold

Figure 6. INx Voltage Threshold

Figure 7. DIAG_EN Voltage Threshold

Figure 8. SEL Voltage Threshold

Figure 9. Body-Diode Forward Voltage

Figure 10. Drain-to-Source Clamp Voltage

Product Folder Links: *TPS2H000-Q1*
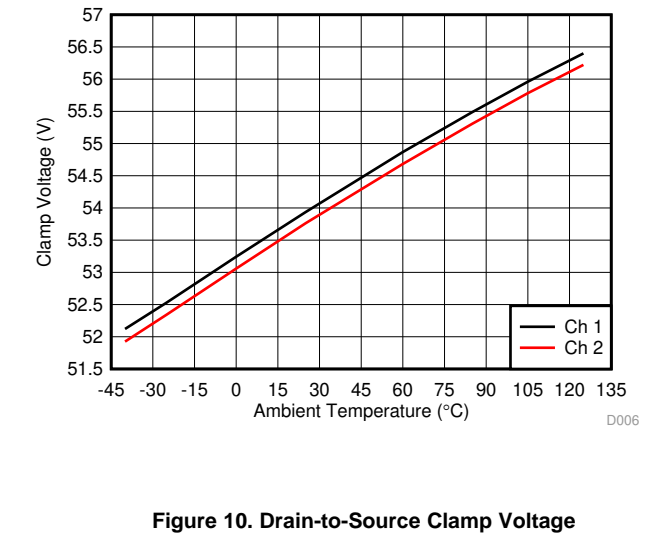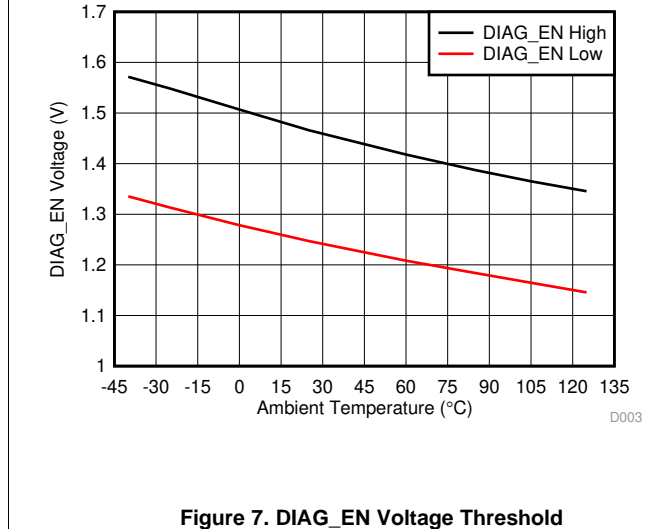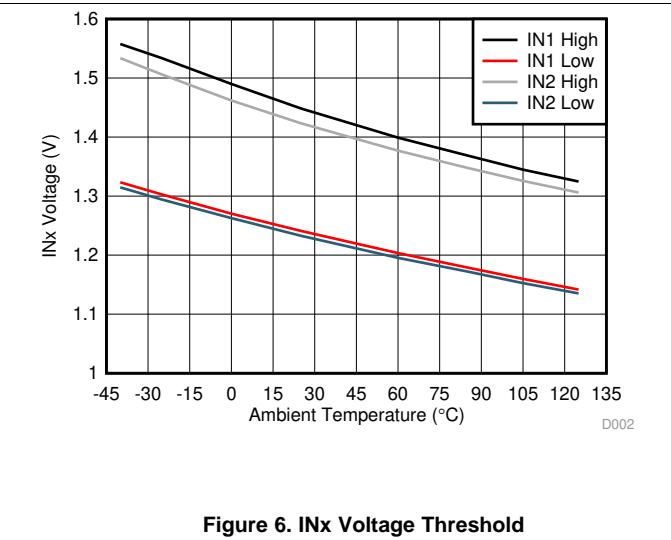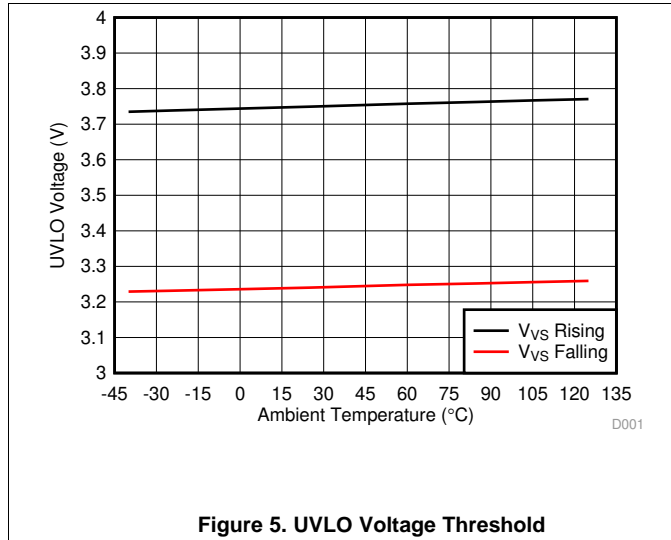
Typical Characteristics (continued)
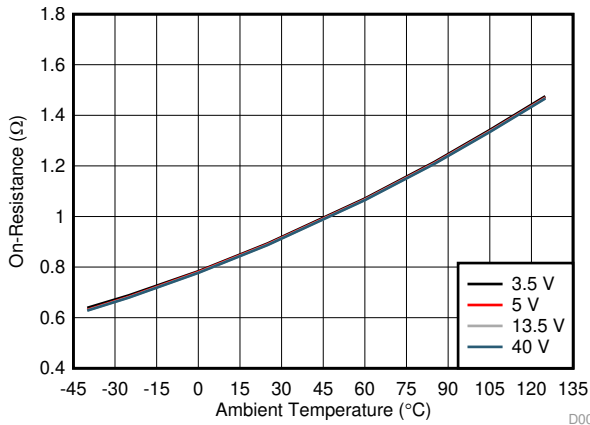
Figure 11. Channel-1 FET On-Resistance
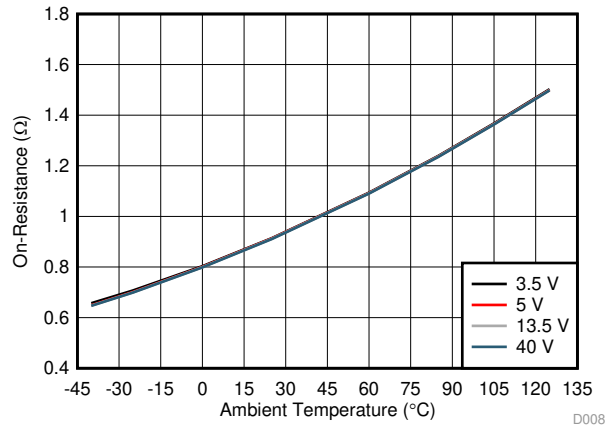
Figure 12. Channel-2 FET On-Resistance
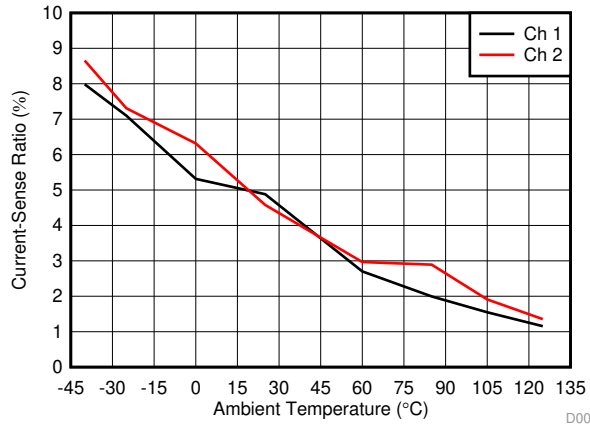
Figure 13. Current-Sense Ratio at 1 mA
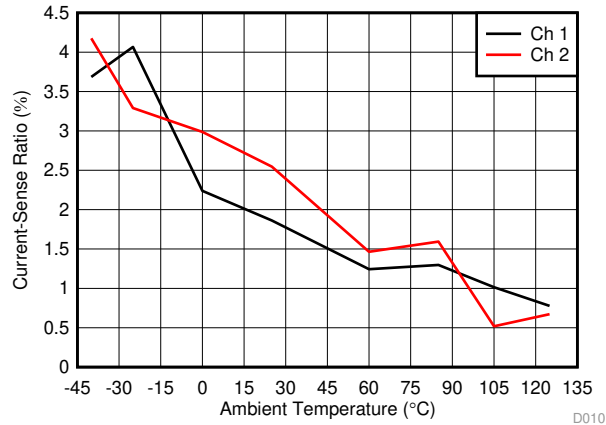
Figure 14. Current-Sense Ratio at 2 mA
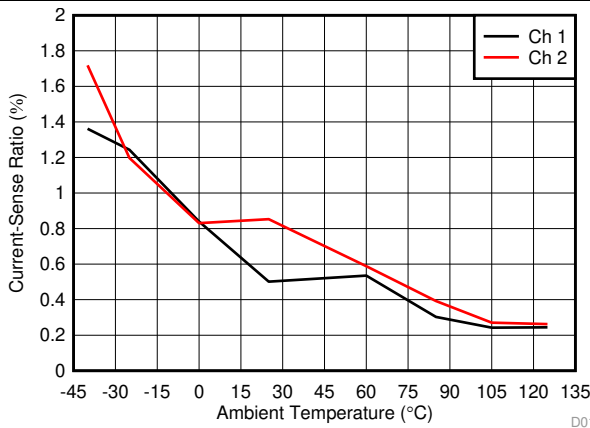
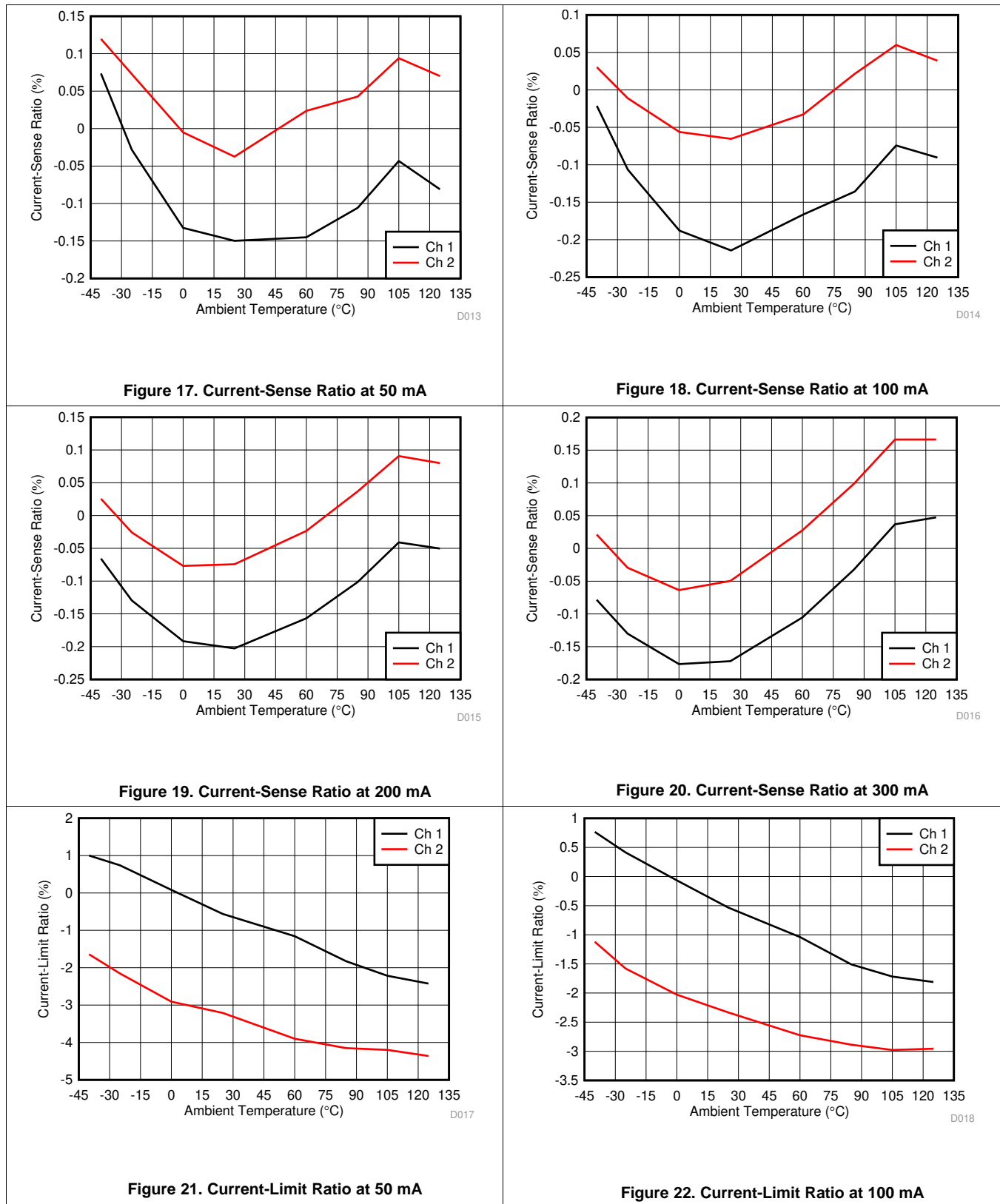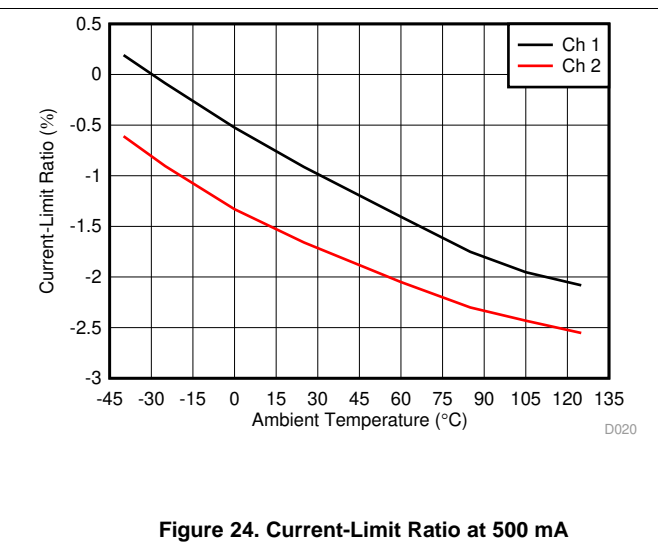**Figure 15. Current-Sense Ratio at 5 mA**
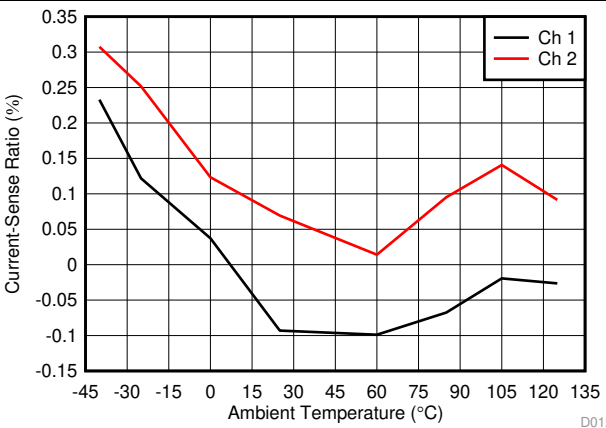
Figure 16. Current-Sense Ratio at 25 mA

Product Folder Links: *TPS2H000-Q1*

Typical Characteristics (continued)

Figure 17. Current-Sense Ratio at 50 mA

Figure 18. Current-Sense Ratio at 100 mA

Figure 19. Current-Sense Ratio at 200 mA

Figure 20. Current-Sense Ratio at 300 mA

Figure 21. Current-Limit Ratio at 50 mA

Figure 22. Current-Limit Ratio at 100 mA

Product Folder Links: *TPS2H000-Q1*

Typical Characteristics (continued)

Figure 23. Current-Limit Ratio at 200 mA

Figure 24. Current-Limit Ratio at 500 mA

Product Folder Links: *TPS2H000-Q1*
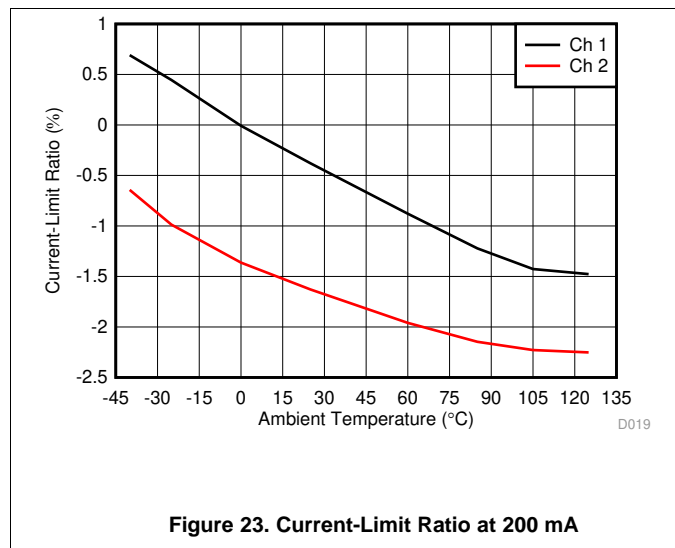
8 Detailed Description

8.1 Overview

The TPS2H000-Q1 device is a smart high-side switch, with internal charge pump and dual-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

For version A, the device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the $\overline{STx}$ pins together.
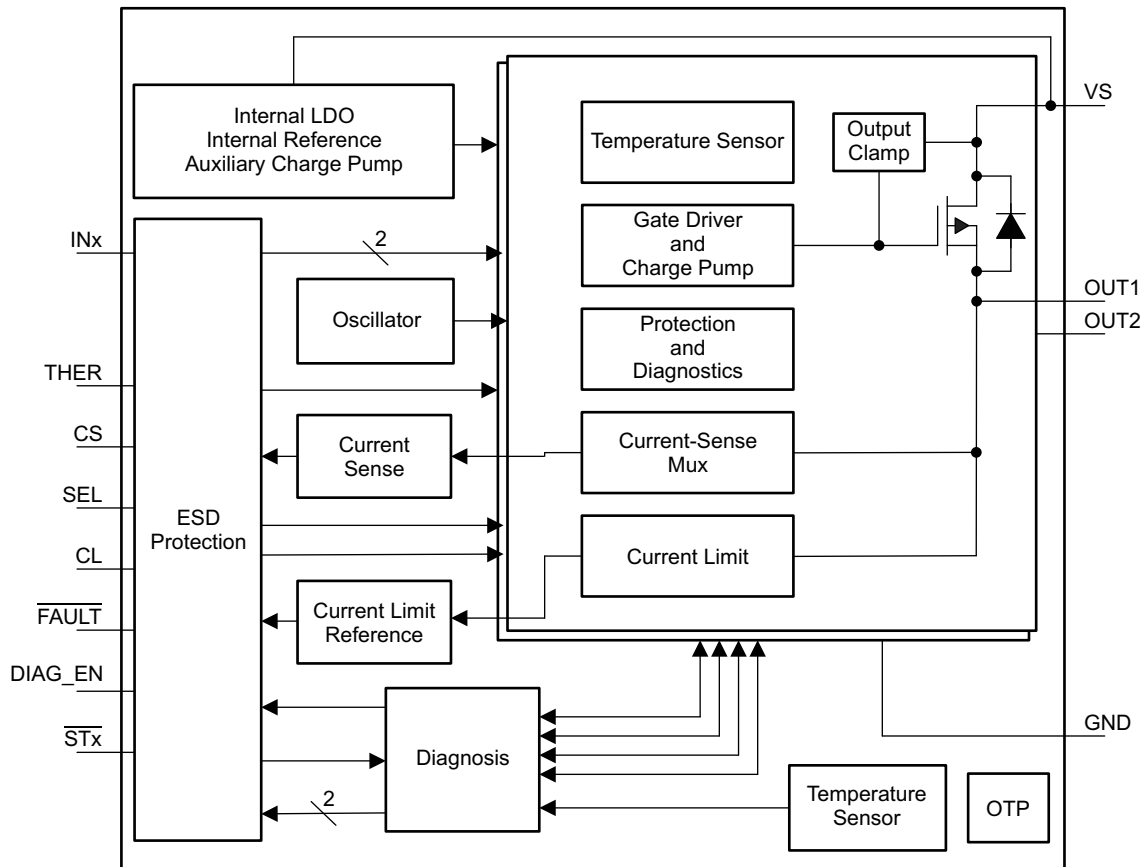
For version B, high-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source 1 / $K_{(CS)}$ of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. $K_{(CS)}$ is a constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of $V_{CS(H)}$.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS2H000-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in Figure 25. All voltages are measured relative to the ground plane.
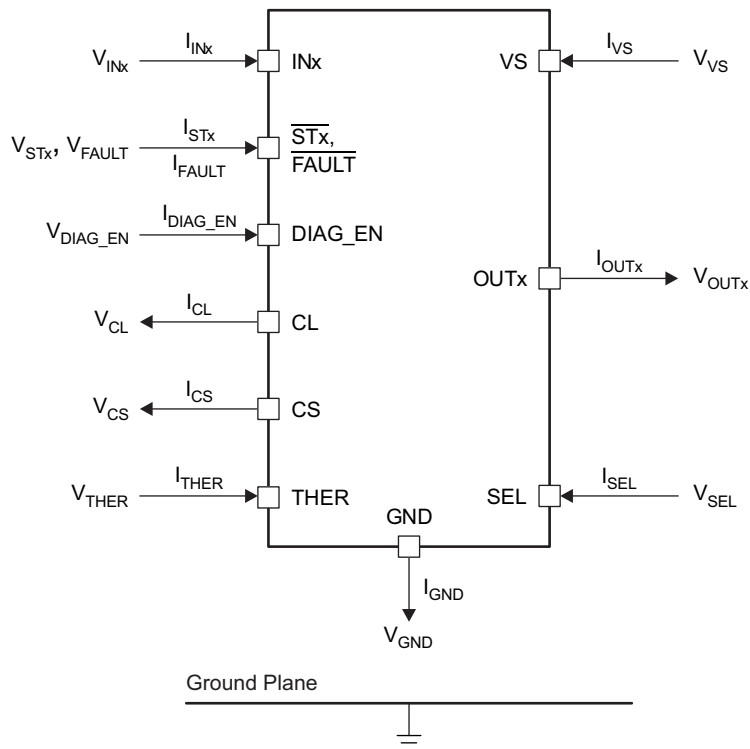
Product Folder Links: *TPS2H000-Q1*

Feature Description (continued)

Figure 25. Voltage and Current Conventions

8.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the version-B device. It allows a better real-time monitoring effect and more-accurate diagnostics without further calibration.

One integrated current mirror can source $1 / K_{(CS)}$ of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the dual channels. $K_{(CS)}$ is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device is calibrated accurately during production, so post-calibration is not required. See Figure 26 for more details.
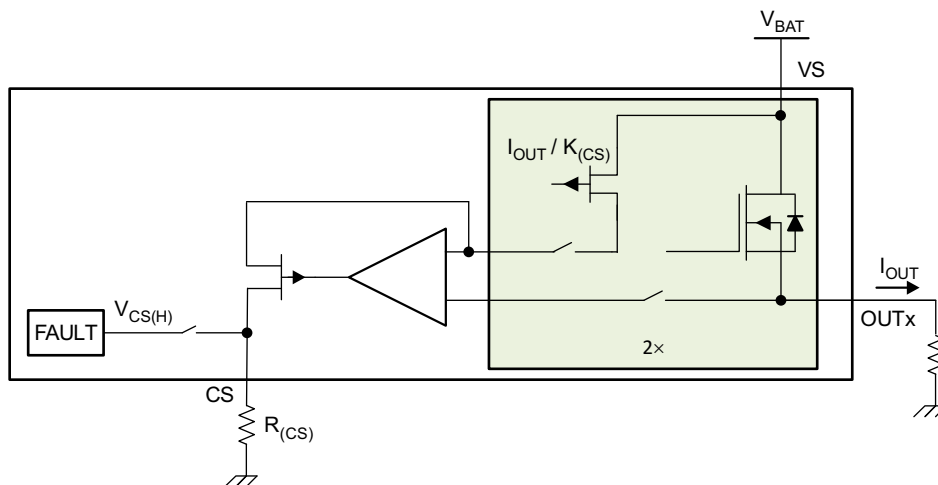

Figure 26. Current-Sense Block Diagram

Product Folder Links: *TPS2H000-Q1*

Feature Description (continued)

When a fault occurs, the CS pin also works as a fault report with a pullup voltage, $V_{CS(H)}$. See Figure 27 for more details.
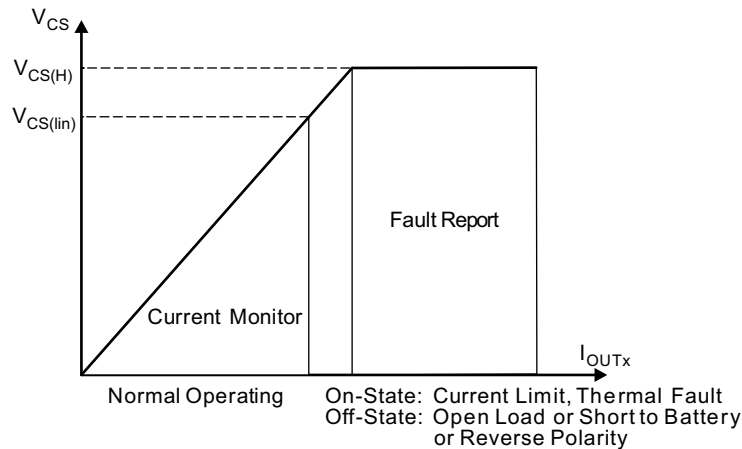

Figure 27. Current-Sense Output-Voltage Curve

Use Equation 1 to calculate $R_{(CS)}$.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUTx}} \tag{1}$$

Take the following points into consideration when calculating $R_{(CS)}$.

- Ensure V_{CS} is within the current-sense linear region (V_{CS}, $I_{OUTx(lin)}$) across the full range of the load current. Check $R_{(CS)}$ with Equation 2.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \leq \frac{V_{CS(lin)}}{I_{CS}} \tag{2}$$

- In fault mode, ensure I_{CS} is within the source capacity of the CS pin ($I_{CS(H)}$). Check $R_{(CS)}$ with Equation 3.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \geq \frac{V_{CS(H,min)}}{I_{CS(H,min)}} \tag{3}$$

8.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{CL(TSD)}$ to reduce the power dissipation on the power FET. See Figure 28 for more details.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threshold. Use the Equation 4 to calculate the $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

Product Folder Links: *TPS2H000-Q1*

Feature Description (continued)

$$I_{CL} = \frac{V_{CL(th)}}{R_{(CL)}} = \frac{I_{OUT}}{K_{(CL)}}$$

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}}$$

(4)
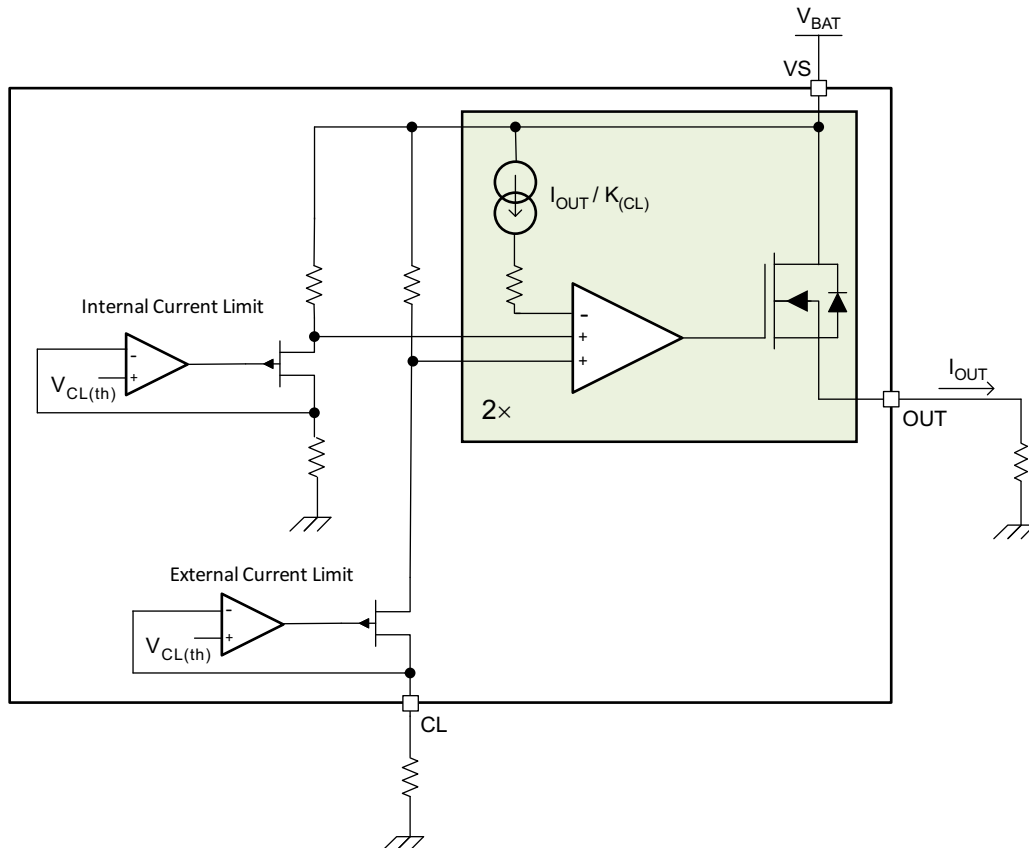
Figure 28. Current-Limit Block Diargam

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the INx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 μs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT}$$

(5)

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

Feature Description (continued)

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \tag{6}$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.
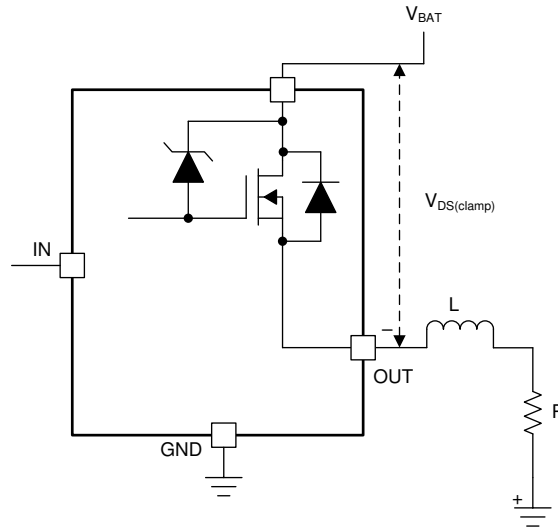

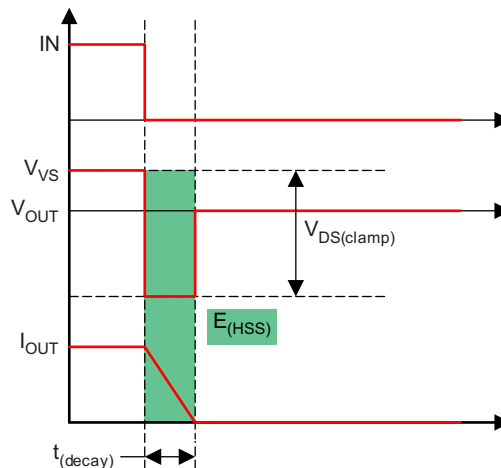**Figure 29. Drain-to-Source Clamping Structure**

Figure 30. Inductive Load Switching-Off Diagram

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)\,dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|} \right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|} \right) \right] \tag{7}$$

Product Folder Links: *TPS2H000-Q1*

Feature Description (continued)

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I^2_{OUT(max)} \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|}$$

(8)

Note that for PWM-controlled inductive loads, it is recommended to add the external free-wheeling circuitry shown in Figure 31 to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See Figure 31 for more details.
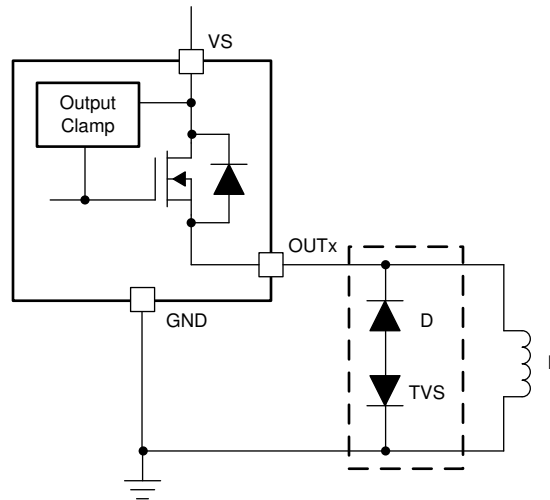

Figure 31. Protection With External Circuitry

8.3.5 Fault Detection and Reporting

8.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and INx low.

8.3.5.2 Multiplexing of Current Sense

For version B, SEL is used to multiplex the shared current-sense function between the two channels. See Table 1 for more details.

Table 1. Diagnosis Configuration Table

DIAG_EN	INx	SEL	CS ACTIVATED CHANNEL	CS, $\overline{FAULT}$, $\overline{STx}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	High impedance	Diagnostics disabled, full protection
	L				Diagnostics disabled, no protection
H	—	0	Channel 1	See Table 2	See Table 2
		1	Channel 2		

8.3.5.3 Fault Table

Table 2 applies when the DIAG_EN pin is enabled.

Table 2. Fault Table

CONDITIONS	INx	OUTx	THER	CRITERION	$\overline{STx}$ (VER. A)	CS (VER. B)	$\overline{FAULT}$ (VER. B)	FAULT RECOVERY
Normal	L	L	—	—	H	0	H	—
Normal	H	H	—	—	H	In linear region	H	—
Overlaod, short to ground	H	L	—	Current limit triggered	L	$V_{CS(H)}$	L	Auto
Open load[1], short to battery, reverse polarity	L	H	—	$V_{VS} - V_{OUTx} < V_{(ol,off)}$	L	$V_{CS(H)}$	L	Auto
Thermal shutdown	H	—	L	T_{SD} triggered	L	$V_{CS(H)}$	L	Output auto-retry. Fault recovers when $T_J < T_{(SD,rst)}$ or when INx toggles.
Thermal shutdown	H	—	H	T_{SD} triggered	L	$V_{CS(H)}$	L	Output latch off. Fault recovers when INx toggles.
Thermal swing	H	—	—	T_{SW} triggered	L	$V_{CS(H)}$	L	Auto

(1)   An external pullup is required for open-load detection.

8.3.5.4 $\overline{STx}$ and $\overline{FAULT}$ Reporting

For version A, two individual $\overline{STx}$ pins report the fault conditions, each pin for its respective channel. When a fault condition occurs, it pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the $\overline{STx}$ pins together.

For version B, a global $\overline{FAULT}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{FAULT}$ pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller.

After the $\overline{FAULT}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, $V_{CS(H)}$.

8.3.6 Full Diagnostics

8.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{CL(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

8.3.6.2 Open-Load Detection

8.3.6.2.1 Channel On

When a channel on, benefiting from the high-accuracy current sense in a small current range, if an open-load event occurs, it can be detected as an ultralow V_{CS} and handled by the microcontroller. Note that the detection is not reported on the $\overline{STx}$ or $\overline{FAULT}$ pins. The microcontroller must set the SEL pin to detect the channel-on open-load fault proactively.

8.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{VS} - V_{OUTx} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 20 kΩ.
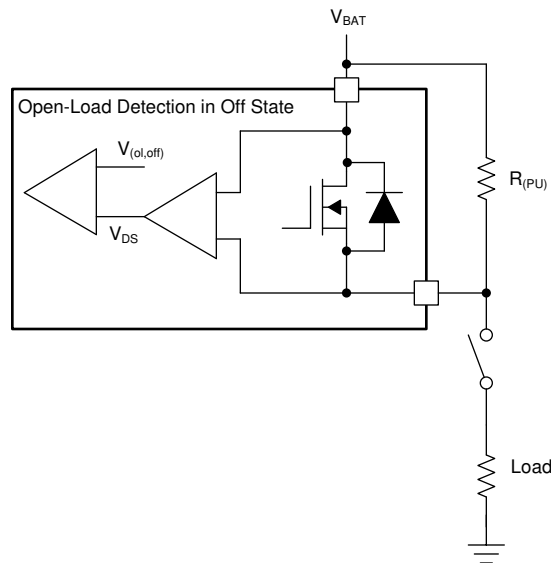

Figure 32. Open-Load Detection in Off-State

8.3.6.3 Short-to-Battery Detection

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 2 for more details.

In the on-state, reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state.
- If $V_{OUTx} - V_{VS} < V_{(F)}$ (body diode forward voltage), no reverse current occurs.
- If $V_{OUTx} - V_{VS} > V_{(F)}$, reverse current occurs. The current must be limited to less than $I_{R(1)}$. Setting an INx pin high can minimize the power stress on its channel. Also, for external reverse protection, see *Reverse-Current Protection* for more details.

8.3.6.4 Reverse Polarity Detection

Reverse polarity detection has the same detection mechanism and behavior as open-load detection both in the on-state and off-state. See Table 2 for more details.

In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state. The reverse current must be limited to less than $I_{R(2)}$. Set the related INx pin high to keep the power dissipation to a minimum. For external reverse-blocking circuitry, see *Reverse-Current Protection* for more details.

8.3.6.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

8.3.6.5.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs.
- When the THER pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when $T_J < T_{(SD)} - T_{(hys)}$, but the current is limited to $I_{CL(TSD)}$ to avoid repetitive thermal shutdown. The

Product Folder Links: *TPS2H000-Q1*

thermal shutdown fault signal is cleared when $T_J < T_{(SD,rst)}$ or after toggling the related INx pin.

- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related INx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in Figure 33, multiple thermal swings are triggered before thermal shutdown occurs.
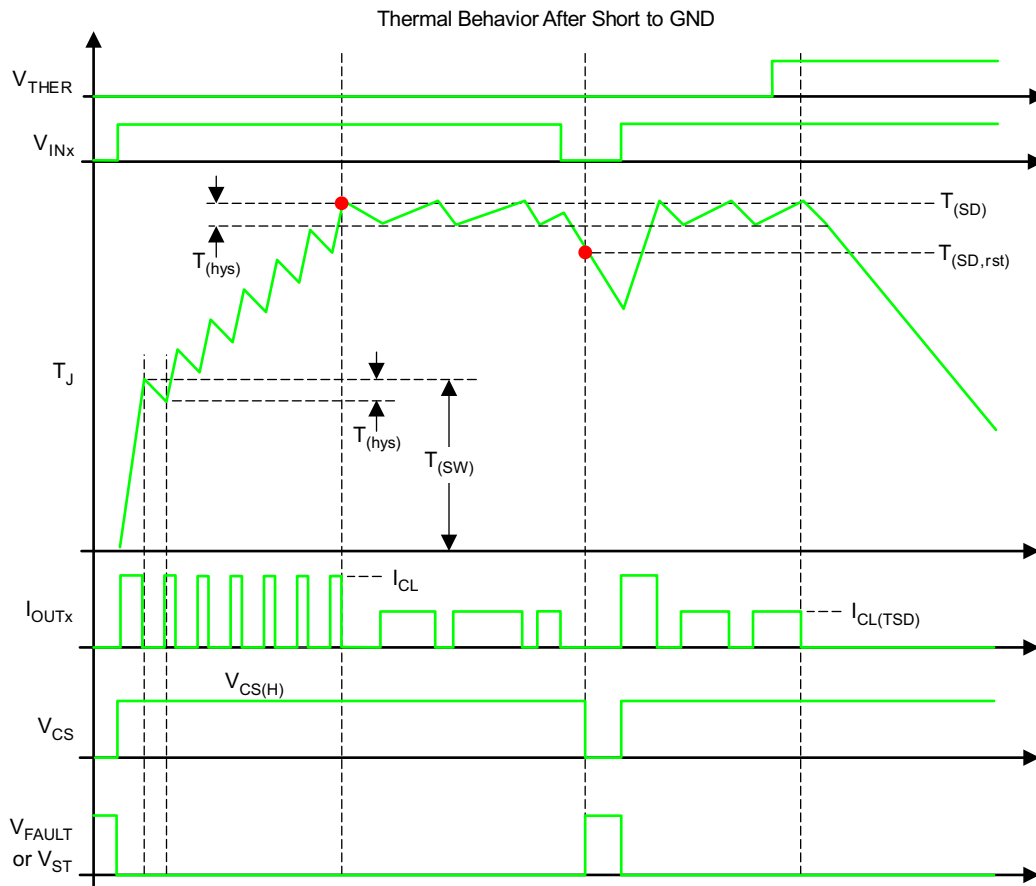

Figure 33. Thermal Behavior Diagram

8.3.7 Full Protections

8.3.7.1 UVLO Protection

The device monitors the supply voltage V_{VS}, to prevent unpredicted behaviors when V_{VS} is too low. When V_{VS} falls down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

8.3.7.2 Loss-of-GND Protection

When loss of GND occurs, output is shut down regardless of whether the INx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

8.3.7.3 Protection for Loss of Power Supply

When loss of supply occurs, the output is shut down regardless of whether the INx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, TI recommends the external free-wheeling diode as shown in *Figure 34*.
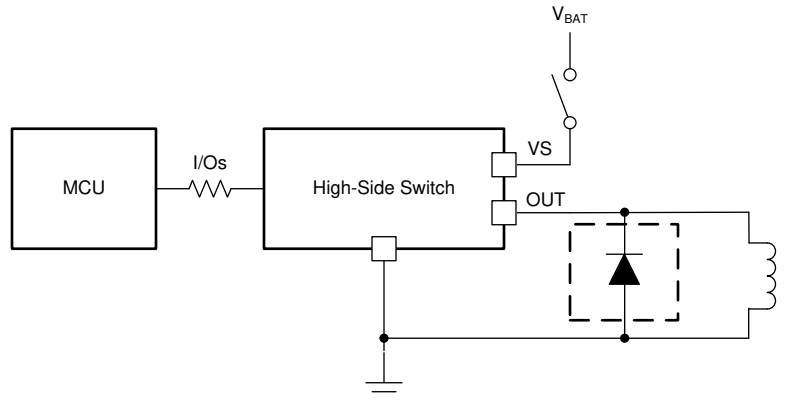

**Figure 34. Protection for Loss of Power Supply**

8.3.7.4 Reverse-Current Protection

Reverse current occurs in two conditions: short to battery and reverse polarity.

- When a short to the battery occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current. The GND pin maximum current is specified in the *Absolute Maximum Ratings*.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.
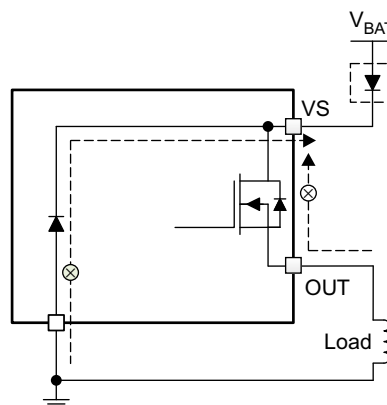
Figure 35. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an >100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.
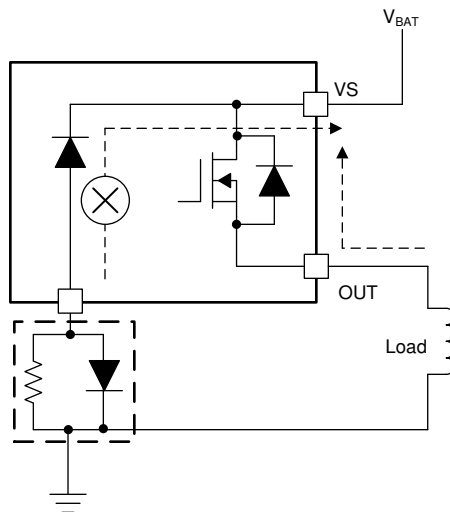

Figure 36. Reverse-Current External Protection, Method 2

8.3.7.5 *MCU I/O Protection*

In some severe conditions, such as the ISO7637-2 test or the loss of battery with inductive loads, a negative pulse occurs on the GND pin This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.
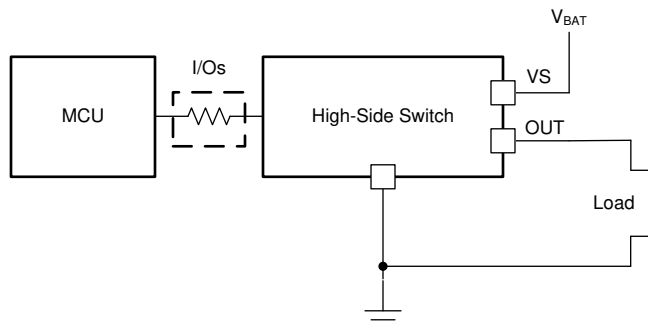

Figure 37. MCU I/O External Protection

8.4 Device Functional Modes

8.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics.

Note that IN must be low for t > $t_{(off,deg)}$ to enter the standby mode, where $t_{(off,deg)}$ is the standby mode deglitch time used to avoid false triggering. Figure 38 shows a working-mode diagram.
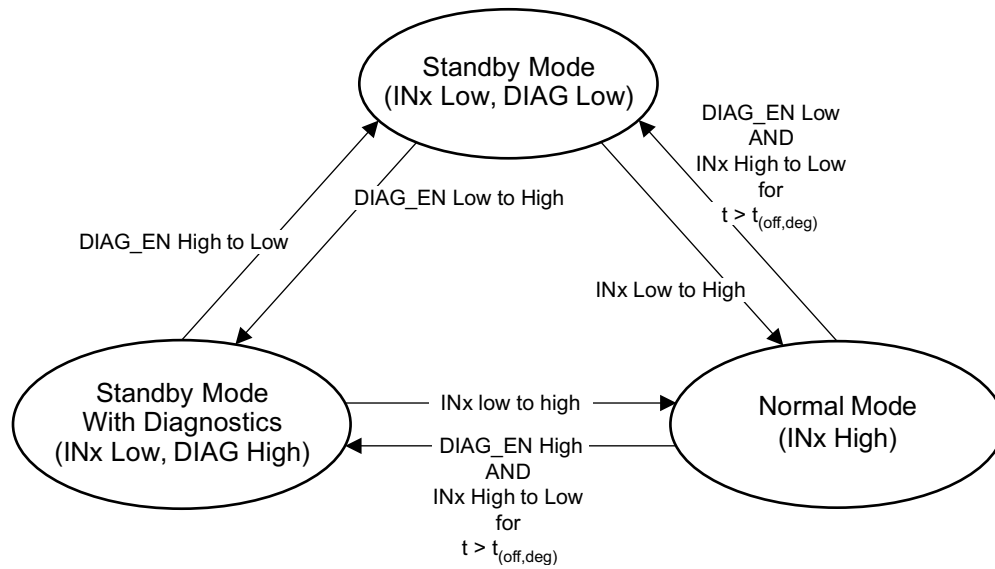
Product Folder Links: *TPS2H000-Q1*

Device Functional Modes (continued)

Figure 38. Working Modes

Product Folder Links: *TPS2H000-Q1*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2H000-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

9.2 Typical Application

The following figure shows an example of the external circuitry connections based on the version-B device.
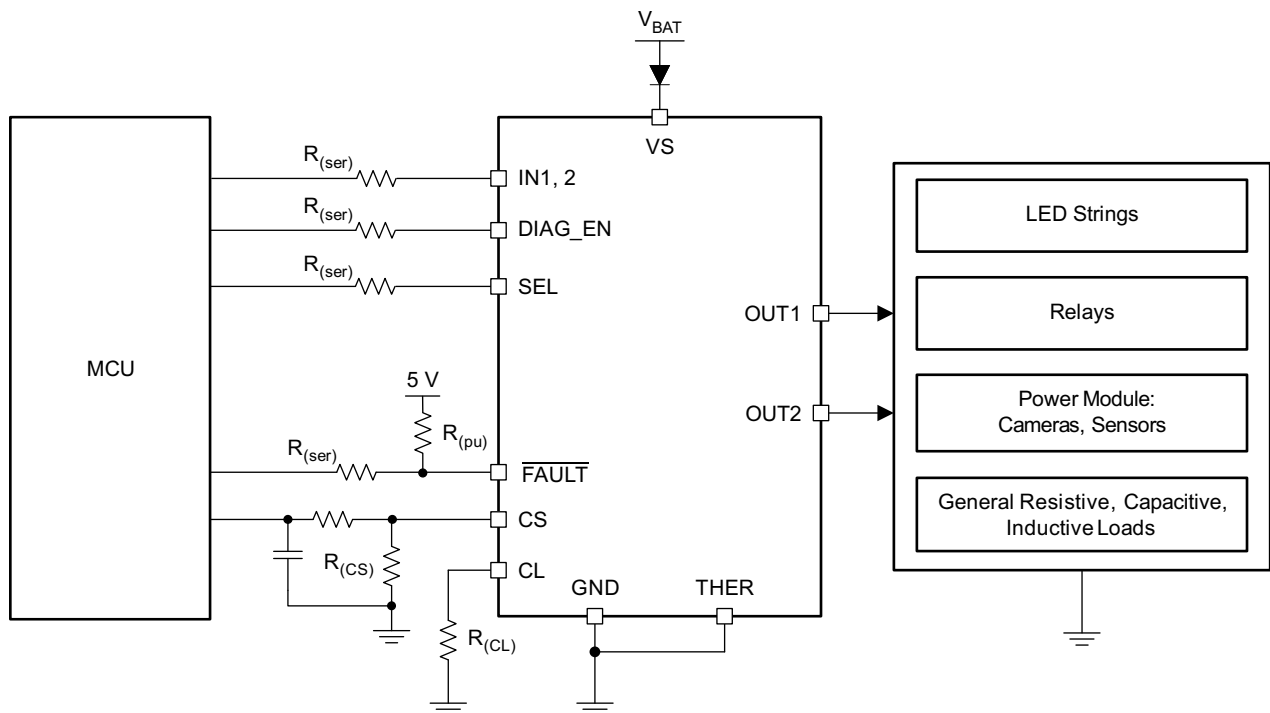
Copyright © 2016, Texas Instruments Incorporated

Figure 39. Typical Application Diagram

9.2.1 Design Requirements

- V_{VS} range from 9 V to 16 V
- Load range is from 0.1 A to 0.25 A for each channel
- Current sense for fault monitoring
- Expected current-limit value of 0.5 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU
- Reverse-voltage protection with a blocking diode in the power-supply line

Product Folder Links: *TPS2H000-Q1*

Typical Application (continued)

9.2.2 Detailed Design Procedure

To keep the 0.25-A nominal current in the 0 to 4-V current-sense range, calculate the $R_{(CS)}$ resistor using Equation 9. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 80}{0.25} = 1280 \ \Omega$$
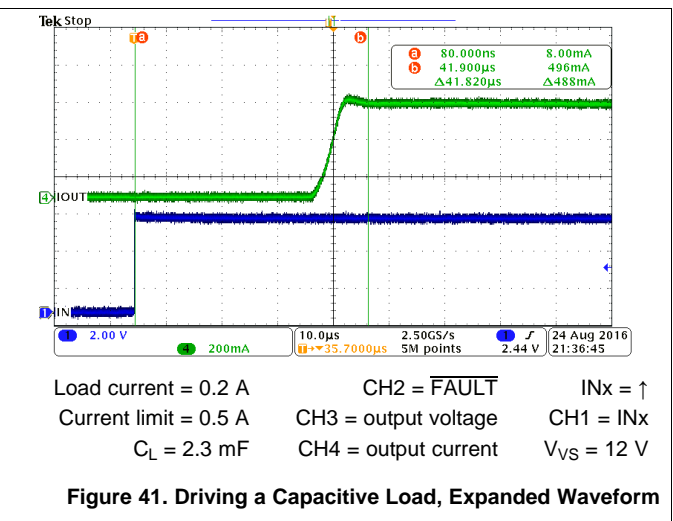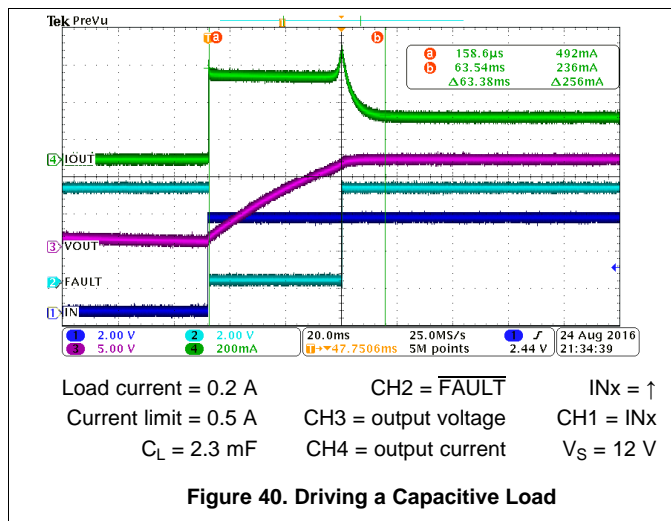
(9)

To set the adjustable current limit value at 0.5 A, calculate $R_{(CL)}$ using Equation 10.

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 300}{0.5} = 480 \ \Omega$$

(10)

TI recommends $R_{(ser)}$ = 10 kΩ for 5-V MCU, and $R_{(pu)}$ = 10 kΩ as the pullup resistor.

9.2.3 Application Curves

Figure 40 shows a test example of soft-start when driving a big capacitive load. Figure 41 shows an expanded waveform of the output current.

Load current = 0.2 A	CH2 = $\overline{FAULT}$	INx = ↑
Current limit = 0.5 A	CH3 = output voltage	CH1 = INx
C_L = 2.3 mF	CH4 = output current	V_S = 12 V

Figure 40. Driving a Capacitive Load

Load current = 0.2 A	CH2 = $\overline{FAULT}$	INx = ↑
Current limit = 0.5 A	CH3 = output voltage	CH1 = INx
C_L = 2.3 mF	CH4 = output current	V_{VS} = 12 V

Figure 41. Driving a Capacitive Load, Expanded Waveform

Typical Application (continued)

Figure 42 shows a test example of PWM-mode driving. Figure 43 shows the expanded waveform of the rising edge. Figure 44 shows the expanded waveform of the falling edge.
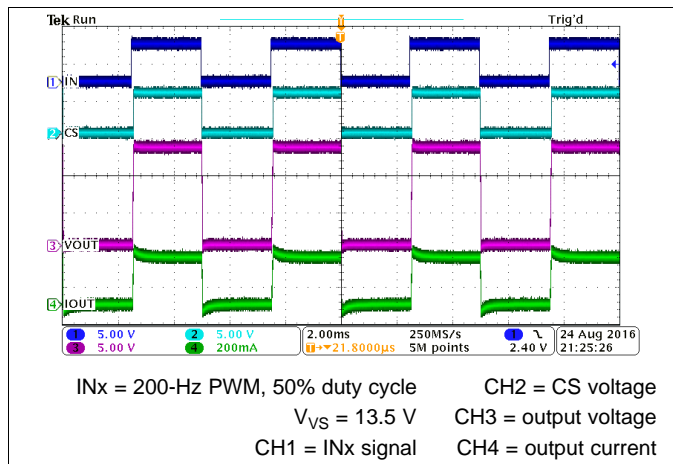

INx = 200-Hz PWM, 50% duty cycle   CH2 = CS voltage
V_{VS} = 13.5 V   CH3 = output voltage
CH1 = INx signal   CH4 = output current

Figure 42. PWM Signal Driving

INx = 200-Hz PWM, 50% duty cycle   CH2 = CS voltage
V_{VS} = 13.5 V   CH3 = output voltage
CH1 = INx signal   CH4 = output current
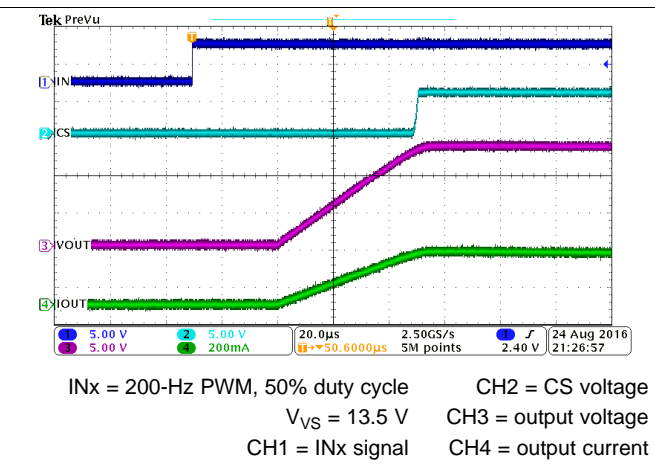
Figure 43. Expanded Waveform of Rising Edge

INx = 200-Hz PWM, 50% duty cycle   CH2 = CS voltage
V_{VS} = 13.5 V   CH3 = output voltage
CH1 = INx signal   CH4 = output current
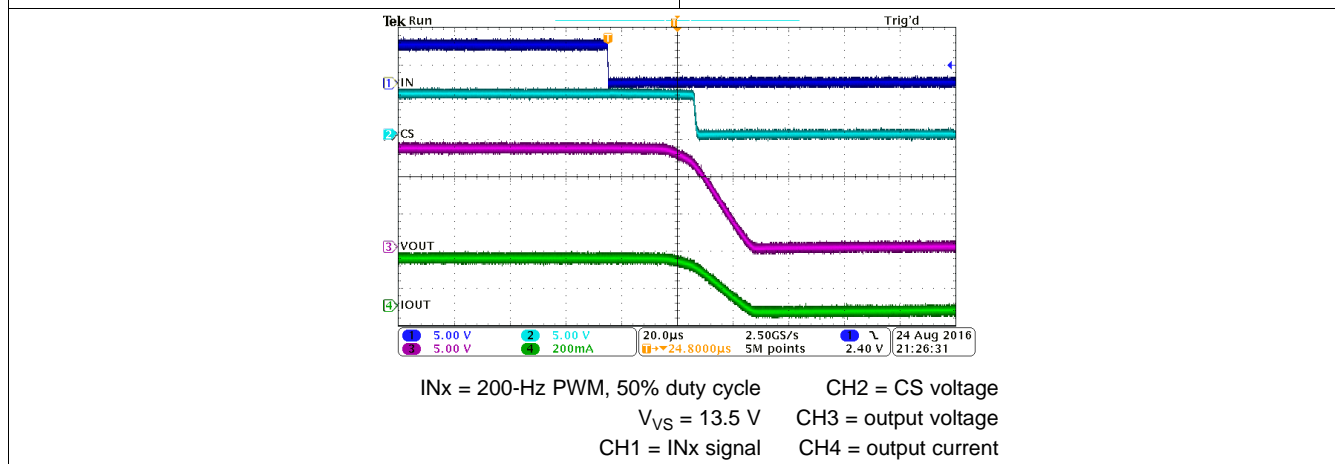
Figure 44. Expanded Waveform of Falling Edge

10 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system or 24-V industrial system. Detailed supply voltage should be within the range specified in the *Recommended Operating Conditions*.

Product Folder Links: *TPS2H000-Q1*

11 Layout

11.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Examples

11.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.
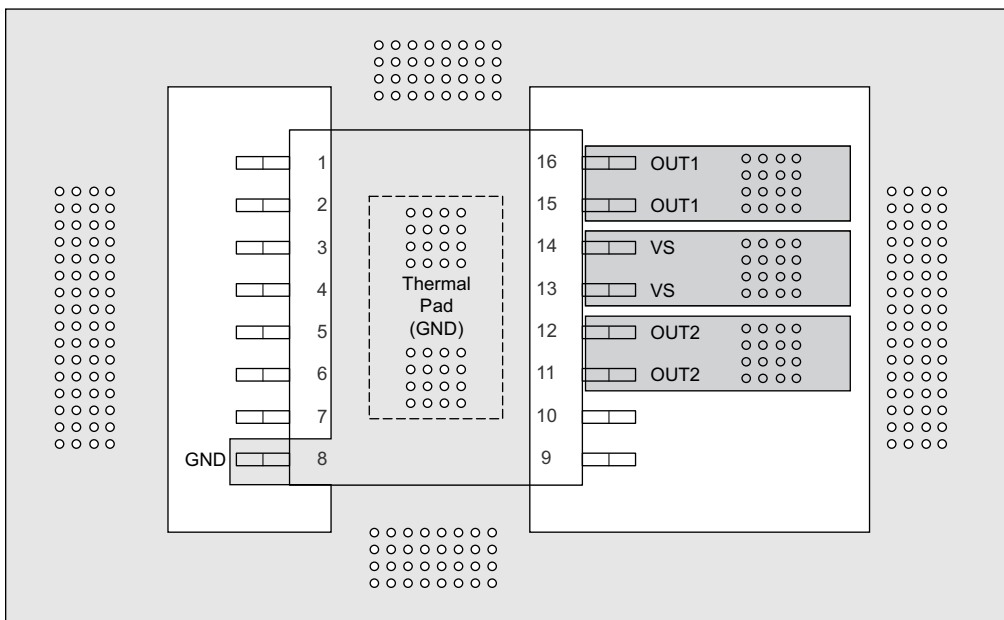

Figure 45. Layout Example Without a GND Network

Layout Examples (continued)

11.2.2 With a GND Network

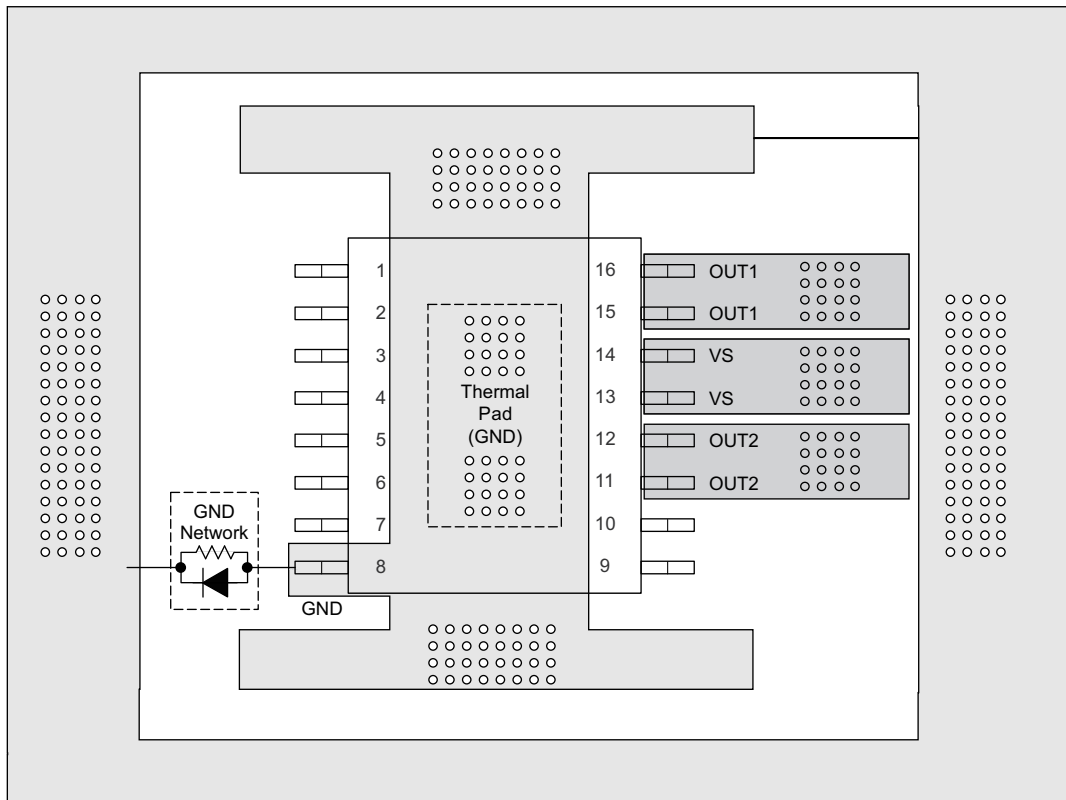With a GND network, tie the thermal pad as one trace to the board GND copper.

Figure 46. Layout Example With a GND Network

Product Folder Links: *TPS2H000-Q1*

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.
    This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2H000AQPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	2H000AQ	Samples
TPS2H000BQPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	2H000BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
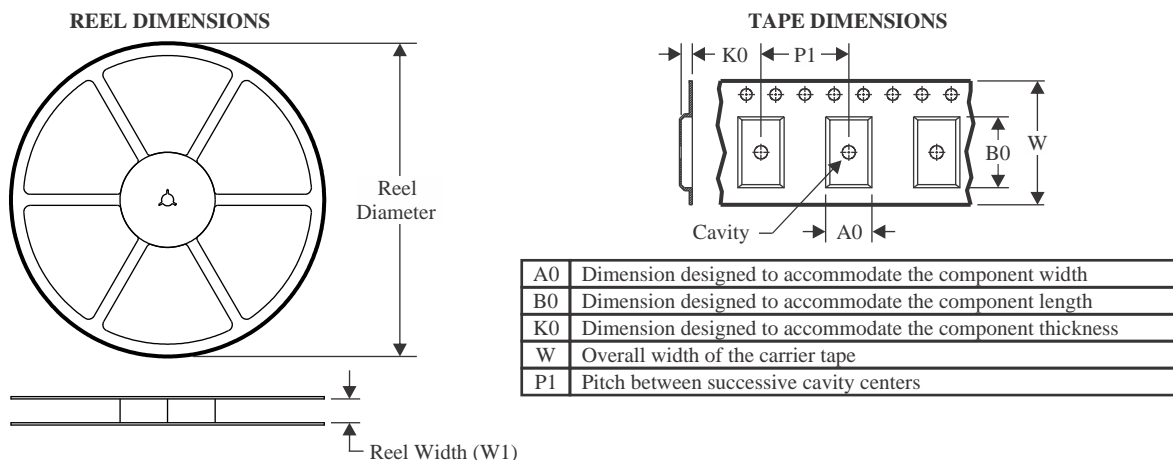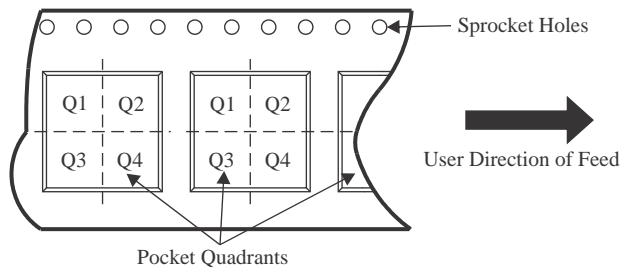
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2H000AQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2H000BQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2H000AQPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS2H000BQPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE
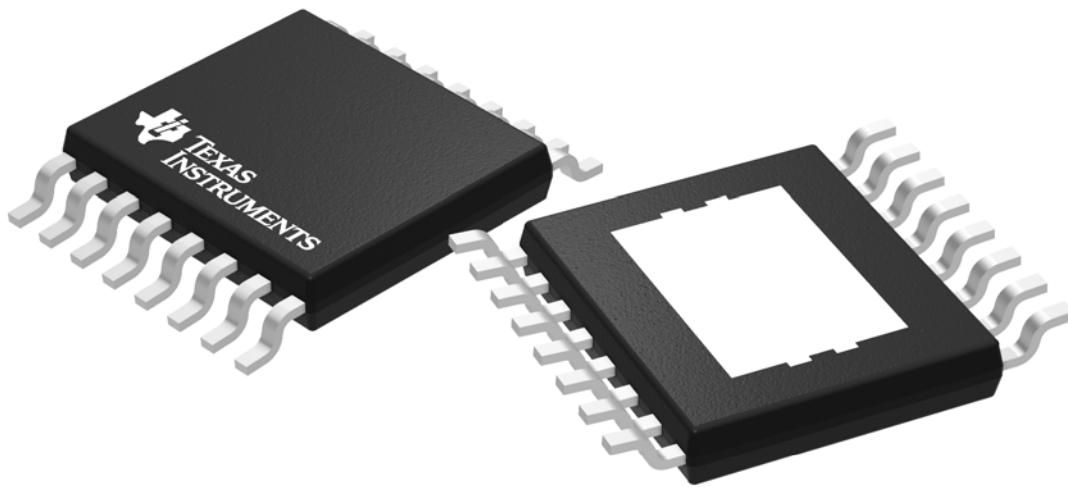
Images above are just a representation of the package family, actual package may vary.
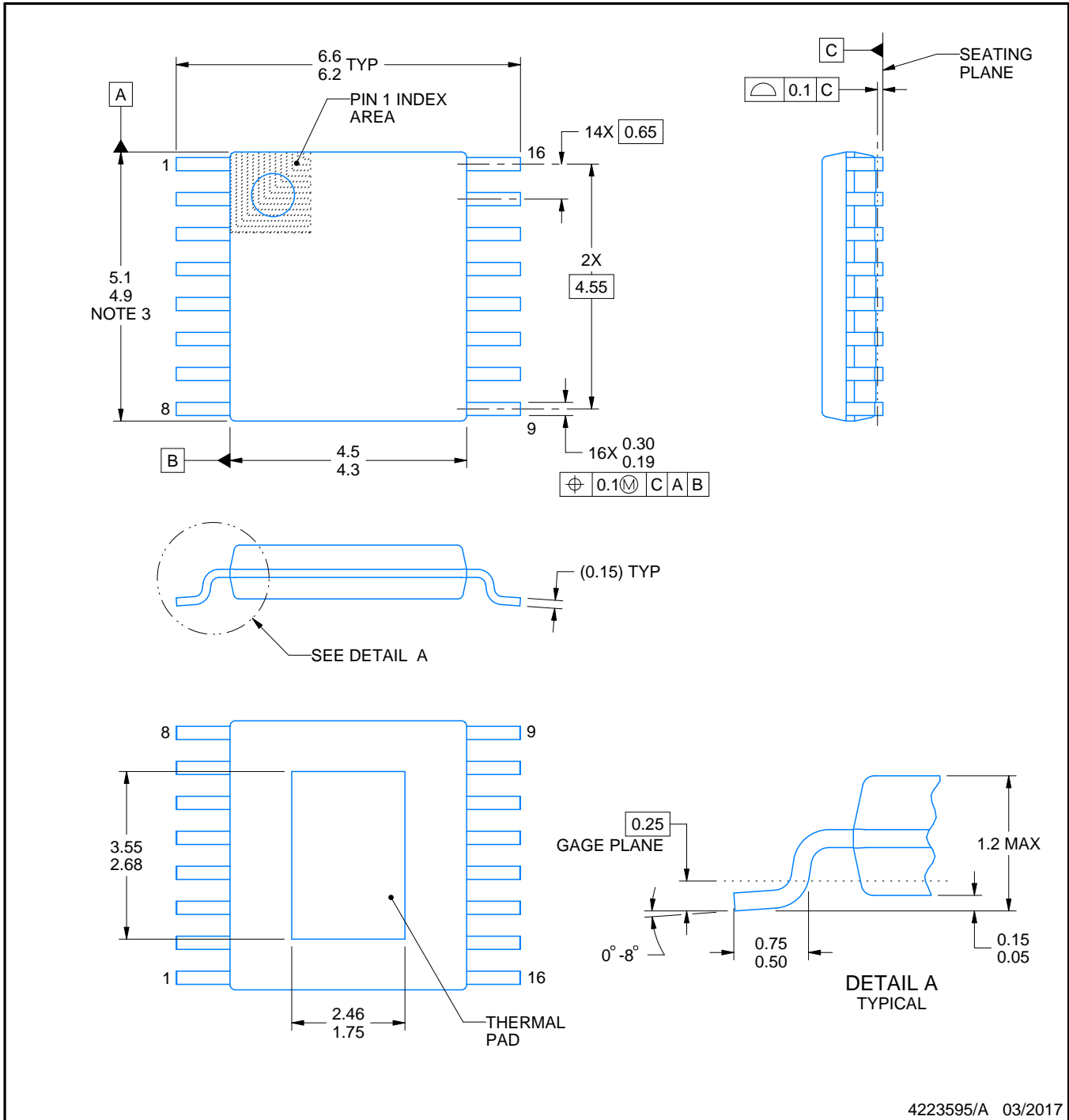Refer to the product data sheet for package details.

4073225-3/J

TEXAS INSTRUMENTS

SMALL OUTLINE PACKAGE

6.6 / 6.2 TYP

A

PIN 1 INDEX AREA

14X [0.65]

1   16

5.1 / 4.9 NOTE 3

2X [4.55]

8   9

B

4.5 / 4.3

16X 0.30 / 0.19

[⊕ 0.1Ⓜ C A B]

C   SEATING PLANE

[⌒ 0.1 C]

(0.15) TYP

SEE DETAIL A

8   9

3.55 / 2.68

1   16

2.46 / 1.75

THERMAL PAD

GAGE PLANE
[0.25]

0°-8°

0.75 / 0.50

1.2 MAX

0.15 / 0.05

DETAIL A
TYPICAL

4223595/A   03/2017

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
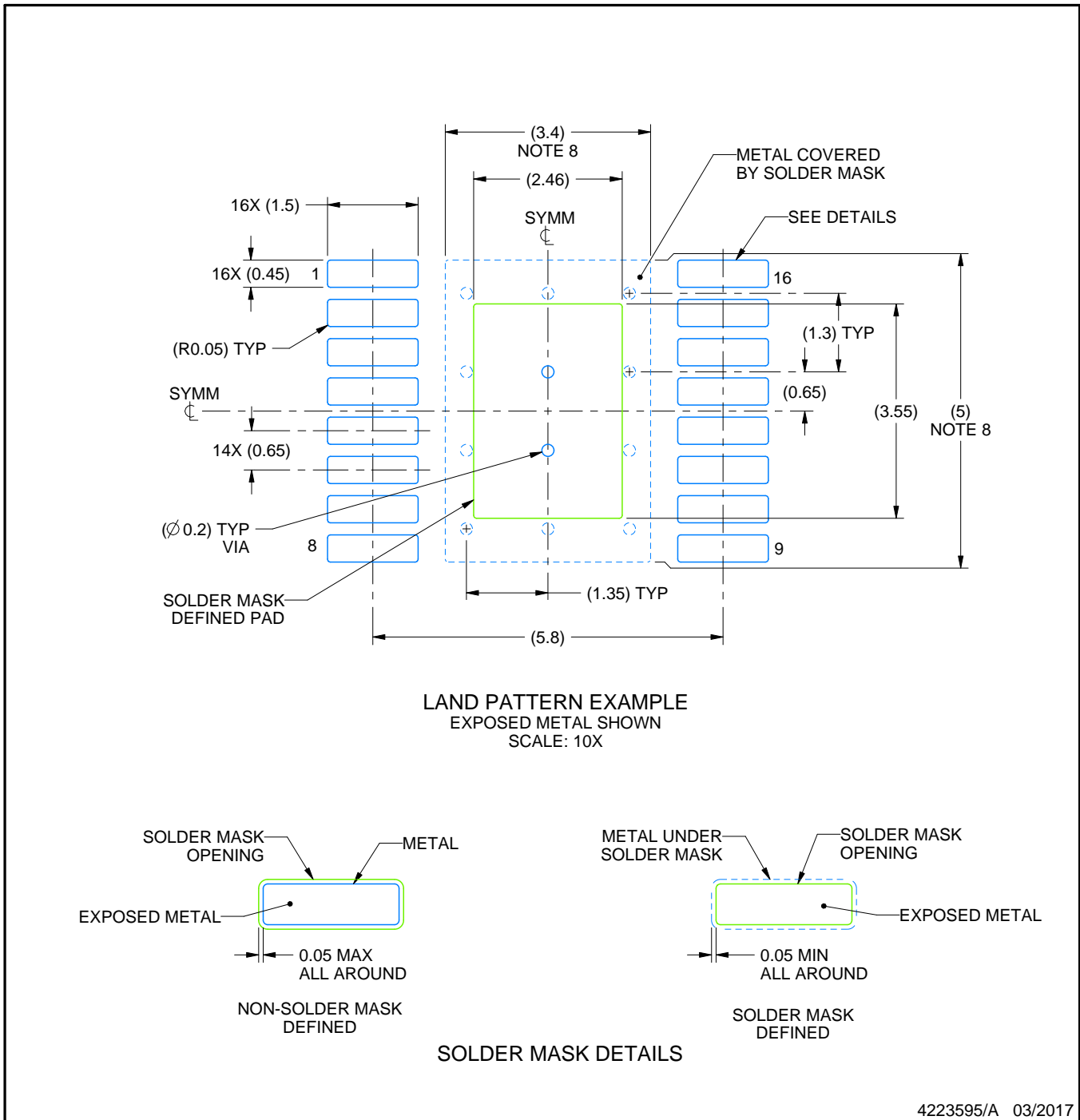4. Reference JEDEC registration MO-153.

TEXAS INSTRUMENTS

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

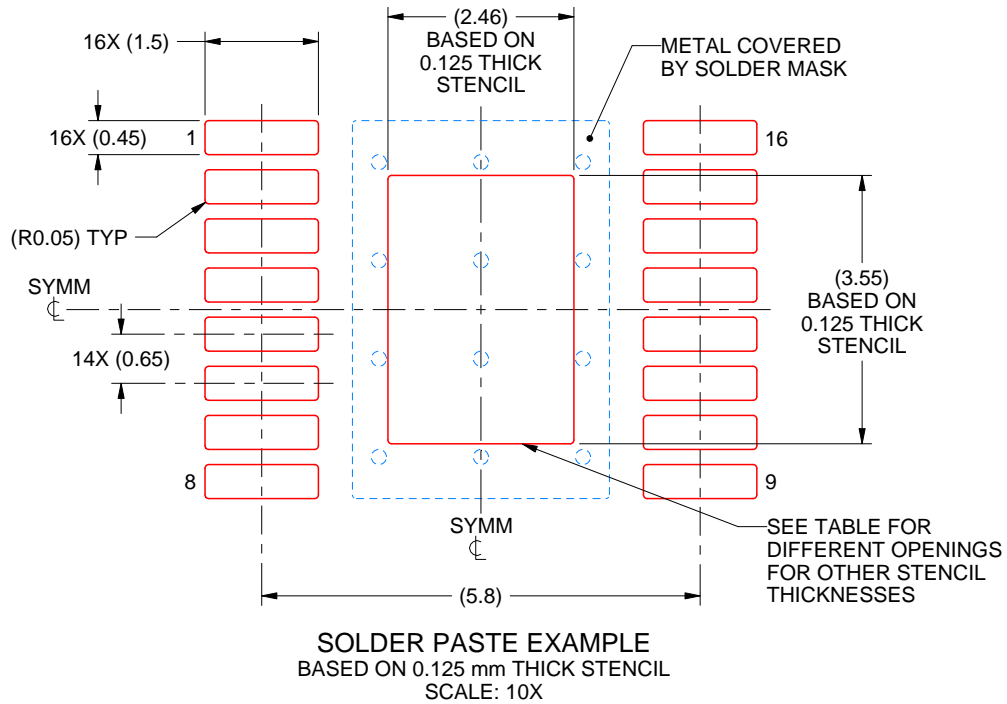4223595/A   03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

16X (1.5)

16X (0.45)   1

(R0.05) TYP

SYMM

14X (0.65)

8

(2.46)
BASED ON
0.125 THICK
STENCIL

METAL COVERED
BY SOLDER MASK

16

(3.55)
BASED ON
0.125 THICK
STENCIL

9

SYMM

(5.8)

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A   03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

TEXAS
INSTRUMENTS

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