

# PCA9306-Q1 Dual Bidirectional I<sup>2</sup>C Bus and SMBus Voltage-Level Translator

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 2: –40°C to 105°C, T<sub>A</sub>
  - HBM ESD classification level H2
  - CDM ESD classification level C4B
- 2-Bit bidirectional translator for SDA and SCL lines in mixed-mode I<sup>2</sup>C applications
- Compatible with I<sup>2</sup>C and SMBus
- Less than 1.5-ns maximum propagation delay to accommodate standard-mode and fast-mode I<sup>2</sup>C devices and multiple controllers
- Allows voltage-level translation between
  - 1.2-V V<sub>REF1</sub> and 1.8-V, 2.5-V, 3.3-V, or 5-V V<sub>REF2</sub>
  - 1.8-V V<sub>REF1</sub> and 2.5-V, 3.3-V, or 5-V V<sub>REF2</sub>
  - 2.5-V V<sub>REF1</sub> and 3.3-V, or 5-V V<sub>REF2</sub>
  - 3.3-V V<sub>REF1</sub> and 5-V V<sub>REF2</sub>
- Provides bidirectional voltage translation with no direction pin
- Low 3.5-Ω ON-state connection between input and output ports provides less signal distortion
- Open-drain I<sup>2</sup>C I/O Ports (SCL1, SDA1, SCL2, and SDA2)
- 5-V tolerant I<sup>2</sup>C I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = low
- Lock-up-free operation for isolation when EN = Low
- Flow-through pinout for ease of printed-circuit board trace routing
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V Human-body model (A114-A)
  - 200-V Machine model (A115-A)
  - 1000-V Charged-device model (C101)

## 2 Applications

- I<sup>2</sup>C, SMBus, PMBus, MDIO, UART, low-speed SDIO, GPIO, and other two-signal interfaces
- Automotive head units
- Automotive instrument clusters
- Automotive driver assistance cameras

## 3 Description

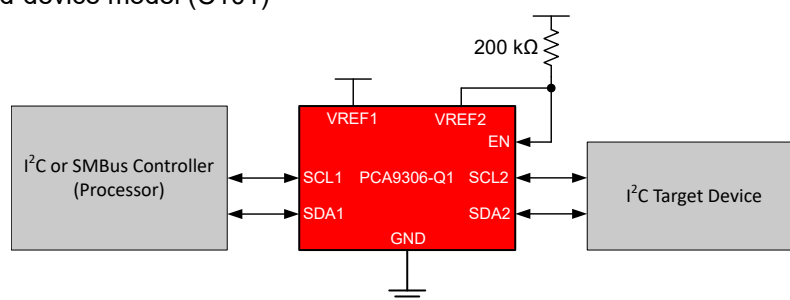
This dual bidirectional I<sup>2</sup>C and SMBus voltage-level translator, with an enable (EN) input, is operational from 1.2-V to 3.3-V V<sub>REF1</sub> and 1.8-V to 5.5-V V<sub>REF2</sub>.

The PCA9306-Q1 allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin. The low ON-state resistance (r<sub>on</sub>) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
PCA9306-Q1	VSSOP (8)	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2016) to Revision C (April 2022)	Page
• Changed all instances of legacy terminology to controller and target where I <sup>2</sup> C is mentioned.....	1
• Added text when <i>disabled</i> to the first paragraph in the <a href="#">Description (continued)</a> .....	3
• Changed the $\theta_{JA}$ MAX value from 227°C/W to 275°C/W in the <a href="#">Absolute Maximum Ratings</a> .....	5
• Changed the <a href="#">Thermal Information</a> table.....	5
• Changed the $V_{IK}$ MIN value to -1.2 V and the MAX value to 0 V in the <a href="#">Electrical Characteristics</a> table.....	6
• Changed the $t_{PHL}$ MAX value at $C_L = 15$ pF from: 0.5 ns to: 0.75 ns in the <a href="#">Switching Characteristics: Translating Down, <math>V_{IH} = 3.3</math> V</a> .....	6
• Changed the $t_{PHL}$ MAX value at $C_L = 15$ pF from: 0.5 ns to: 0.75 ns in the <a href="#">Switching Characteristics: Translating Down, <math>V_{IH} = 2.5</math> V</a> .....	6
• Added Note <i>Specified by design</i> to the <a href="#">Switching Characteristics: Translating Up, <math>V_{IH} = 2.3</math> V</a> .....	7
• Added Note <i>Specified by design</i> to the <a href="#">Switching Characteristics: Translating Up, <math>V_{IH} = 1.5</math> V</a> .....	7
• Changed figure "ON-Resistance vs. Input Voltage" for $V_{EN} = 4.5V$ .....	7
• Added sections <a href="#">Definition of threshold voltage</a> through <a href="#">Current Limiting Resistance on <math>V_{REF2}</math></a> .....	9

Changes from Revision A (March 2013) to Revision B (April 2016)	Page
• Added <a href="#">ESD Ratings</a> table, <a href="#">Feature Description</a> section, <a href="#">Device Functional Modes</a> , <a href="#">Application and Implementation</a> section, <a href="#">Power Supply Recommendations</a> section, <a href="#">Layout</a> section, <a href="#">Device and Documentation Support</a> section, and <a href="#">Mechanical, Packaging, and Orderable Information</a> section .....	1

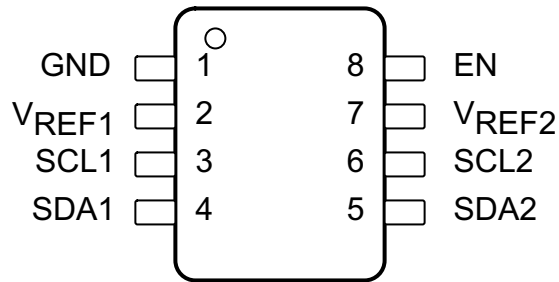
## 5 Description (continued)

In I<sup>2</sup>C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9306-Q1 enables the system designer to isolate halves of a bus when disabled; therefore, more I<sup>2</sup>C devices or longer trace length can be accommodated.

The PCA9306-Q1 also can be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the controller is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

All channels have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less ESD-resistant devices.

## 6 Pin Configuration and Functions



**Figure 6-1. DCU Package, 8-Pin VSSOP, Top View**

**Table 6-1. Pin Functions**

PIN		DESCRIPTION
NO.	NAME	
1	GND	Ground, 0 V
2	$V_{REF1}$	Low-voltage-side reference supply voltage for SCL1 and SDA1
3	SCL1	Serial clock, low-voltage side. Connect to $V_{REF1}$ through a pullup resistor.
4	SDA1	Serial data, low-voltage side. Connect to $V_{REF1}$ through a pullup resistor.
5	SDA2	Serial data, high-voltage side. Connect to $V_{REF2}$ through a pullup resistor.
6	SCL2	Serial clock, high-voltage side. Connect to $V_{REF2}$ through a pullup resistor.
7	$V_{REF2}$	High-voltage-side reference supply voltage for SCL2 and SDA2
8	EN	Switch enable input. Connected to $V_{REF2}$ and pulled up through a high resistor.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>REF1</sub>	DC reference voltage	-0.5	7	V
V <sub>REF2</sub>	DC reference bias voltage	-0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	7	V
V <sub>I/O</sub>	Input/output voltage <sup>(2)</sup>	-0.5	7	V
	Continuous channel current		128	mA
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
θ <sub>JA</sub>	Package thermal impedance		275.5	°C/W
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>I/O</sub>	Input/output voltage	SCL1, SDA1, SCL2, SDA2	0	5	V
V <sub>REF1</sub>	Reference voltage		0	5	V
V <sub>REF2</sub>	Reference voltage		0	5	V
EN	Enable input voltage		0	5	V
I <sub>PASS</sub>	Pass switch current			64	mA
T <sub>A</sub>	Operating free-air temperature		-40	105	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DCU (VSSOP)	UNIT
		8 PINS	
R <sub>θJA</sub> <sup>(2)</sup>	Junction-to-ambient thermal resistance	275.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	127.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	186.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	65.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	185.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_{IK}$	Input clamp voltage	$I_I = -18$ mA,	EN = 0 V	-1.2		0	V	
$I_{IH}$	Input leakage current	$V_I = 5$ V,	EN = 0 V			5	$\mu$ A	
$C_i(EN)$	Input capacitance	$V_I = 3$ V or 0 V			11		pF	
$C_{io(off)}$	Off capacitance	SCLn, SDAn	$V_O = 3$ V or 0 V, EN = 0 V		4	6	pF	
$C_{io(on)}$	On capacitance	SCLn, SDAn	$V_O = 3$ V or 0 V, EN = 3 V		10.5	12.5	pF	
$r_{on}^{(2)}$	ON-state resistance	SCLn, SDAn	$V_I = 0$ V, $I_O = 64$ mA	EN = 4.5 V	3.5	5.5	$\Omega$	
				EN = 3 V	4.7	7		
				EN = 2.3 V	6.3	9.5		
				EN = 1.5 V	25.5	32		
			$V_I = 2.4$ V, $I_O = 15$ mA	EN = 4.5 V	1	6		15
				EN = 3 V	20	60		140
$V_I = 1.7$ V, $I_O = 15$ mA	EN = 2.3 V	20	60	140				

(1) All typical values are at  $T_A = 25^\circ\text{C}$ .

(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

## 7.6 Switching Characteristics: Translating Down, $V_{IH} = 3.3$ V

over recommended operating free-air temperature range, EN = 3.3 V,  $V_{IH} = 3.3$  V,  $V_{IL} = 0$ , and  $V_M = 1.15$  V (unless otherwise noted) (see [Figure 8-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$	SCL2 or SDA2	SCL1 or SDA1	$C_L = 50$ pF		0.8	ns
			$C_L = 30$ pF		0.6	
			$C_L = 15$ pF		0.3	
$t_{PHL}$	SCL2 or SDA2	SCL1 or SDA1	$C_L = 50$ pF		1.2	ns
			$C_L = 30$ pF		1	
			$C_L = 15$ pF		0.75	

## 7.7 Switching Characteristics: Translating Down, $V_{IH} = 2.5$ V

over recommended operating free-air temperature range, EN = 2.5 V,  $V_{IH} = 2.5$  V,  $V_{IL} = 0$ , and  $V_M = 0.75$  V (unless otherwise noted) (see [Figure 8-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$	SCL2 or SDA2	SCL1 or SDA1	$C_L = 50$ pF		1	ns
			$C_L = 30$ pF		0.7	
			$C_L = 15$ pF		0.4	
$t_{PHL}$	SCL2 or SDA2	SCL1 or SDA1	$C_L = 50$ pF		1.3	ns
			$C_L = 30$ pF		1	
			$C_L = 15$ pF		0.75	

### 7.8 Switching Characteristics: Translating Up, $V_{IH} = 2.3\text{ V}$

over recommended operating free-air temperature range,  $V_{EN} = 3.3\text{ V}$ ,  $V_{IH} = 2.3\text{ V}$ ,  $V_{IL} = 0$ ,  $V_T = 3.3\text{ V}$ ,  $V_M = 1.15\text{ V}$ , and  $R_L = 300\ \Omega$  (unless otherwise noted) (see Figure 8-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$	SCL1 or SDA1	SCL2 or SDA2	$C_L = 50\text{ pF}$		0.9 <sup>(1)</sup>	ns
			$C_L = 30\text{ pF}$		0.6 <sup>(1)</sup>	
			$C_L = 15\text{ pF}$		0.4 <sup>(1)</sup>	
$t_{PHL}$	SCL1 or SDA1	SCL2 or SDA2	$C_L = 50\text{ pF}$		1.4 <sup>(1)</sup>	ns
			$C_L = 30\text{ pF}$		1.1 <sup>(1)</sup>	
			$C_L = 15\text{ pF}$		0.7 <sup>(1)</sup>	

(1) Specified by design

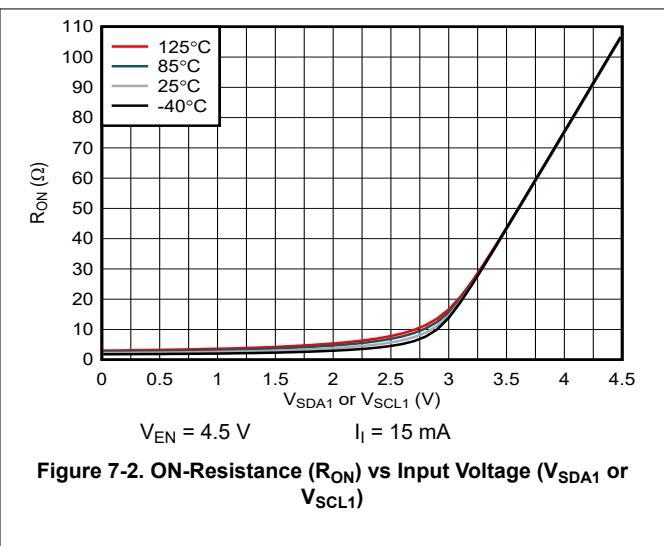
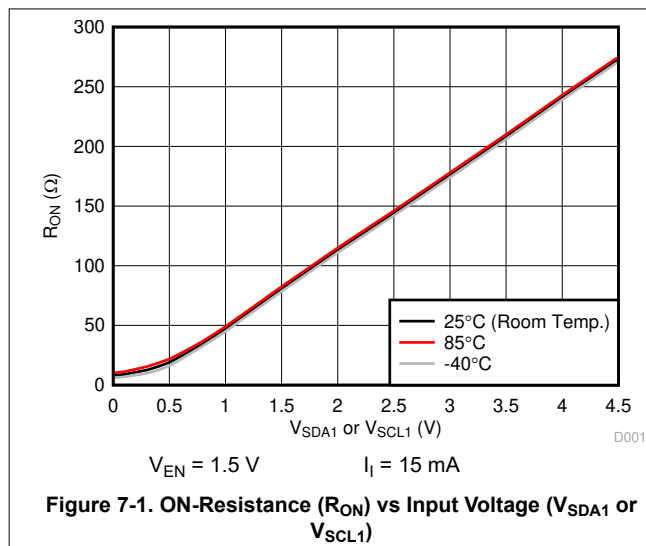
### 7.9 Switching Characteristics: Translating Up, $V_{IH} = 1.5\text{ V}$

over recommended operating free-air temperature range,  $V_{EN} = 2.5\text{ V}$ ,  $V_{IH} = 1.5\text{ V}$ ,  $V_{IL} = 0$ ,  $V_T = 2.5\text{ V}$ ,  $V_M = 0.75\text{ V}$ , and  $R_L = 300\ \Omega$  (unless otherwise noted) (see Figure 8-1)

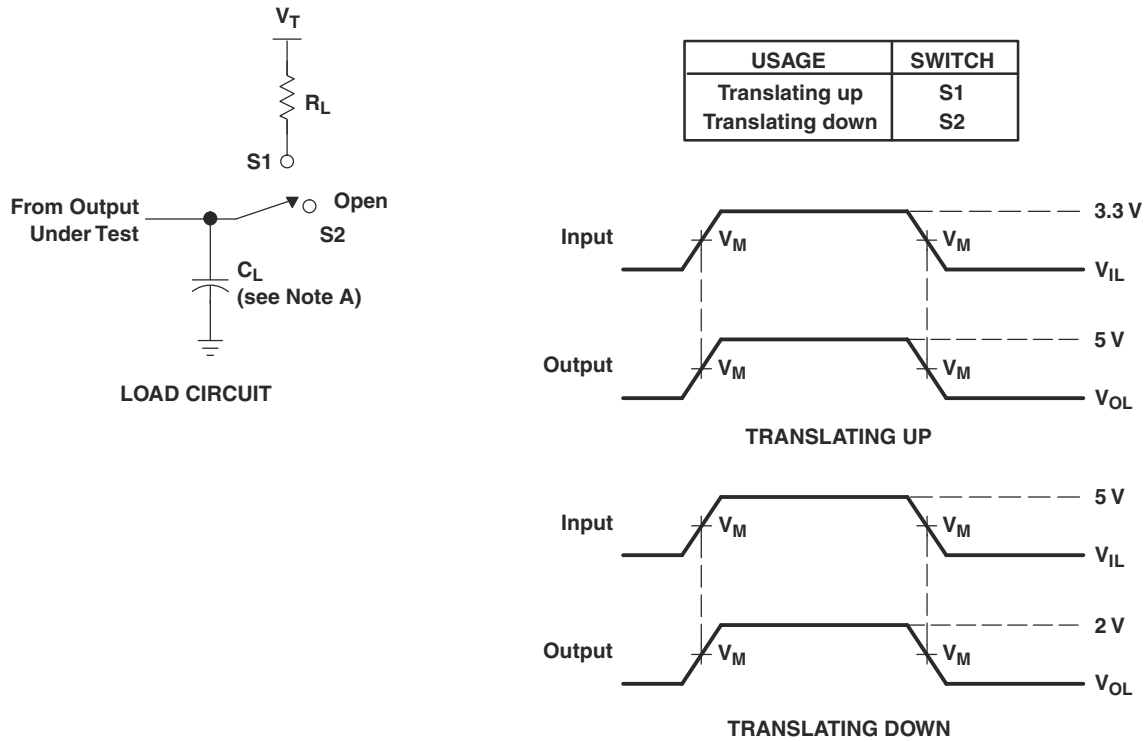
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$	SCL1 or SDA1	SCL2 or SDA2	$C_L = 50\text{ pF}$		1 <sup>(1)</sup>	ns
			$C_L = 30\text{ pF}$		0.6 <sup>(1)</sup>	
			$C_L = 15\text{ pF}$		0.4 <sup>(1)</sup>	
$t_{PHL}$	SCL1 or SDA1	SCL2 or SDA2	$C_L = 50\text{ pF}$		1.3 <sup>(1)</sup>	ns
			$C_L = 30\text{ pF}$		1.3 <sup>(1)</sup>	
			$C_L = 15\text{ pF}$		0.8 <sup>(1)</sup>	

(1) Specified by design

### 7.10 Typical Characteristics



## 8 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 C. The outputs are measured one at a time, with one transition per measurement.

**Figure 8-1. Load Circuit for Outputs**



## 9 Detailed Description

### 9.1 Overview

The PCA9306-Q1 is a dual bidirectional I<sup>2</sup>C and SMBus voltage-level translator with an enable (EN) input that operates without the use of a direction pin. The voltage supply range for VREF1 is 1.2 V to 3.3 V and the supply range for VREF2 is 1.8 V to 5.5 V.

The PCA9306-Q1 can also be used to run two buses, one at a 400-kHz operating frequency and the other at a 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated by using the EN pin when the 400-kHz operation of the main bus is required. If the controller is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

In I<sup>2</sup>C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. The capacitive load on both sides of the PCA9306-Q1 must be considered when approximating the total load of the system, ensuring the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the PCA9306-Q1 have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This characteristic is a benefit over discrete transistor voltage translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less ESD-resistant devices.

#### 9.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as  $V_{th}$ , which appears multiple times throughout this document when discussing the NFET between VREF1 and VREF2. The value of  $V_{th}$  is approximately 0.6 V at room temperature.

#### 9.1.2 Correct Device Set Up

In a normal set up shown in Figure 9-1, the enable pin and VREF2 are shorted together and tied to a 200-kΩ resistor, and a reference voltage equal to VREF1 plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

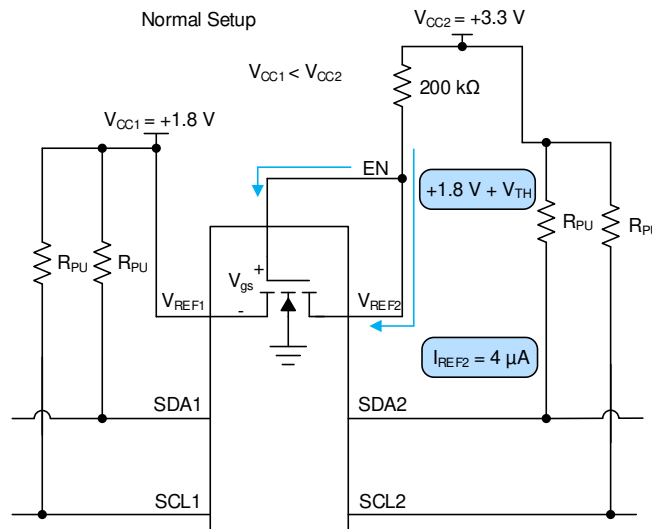
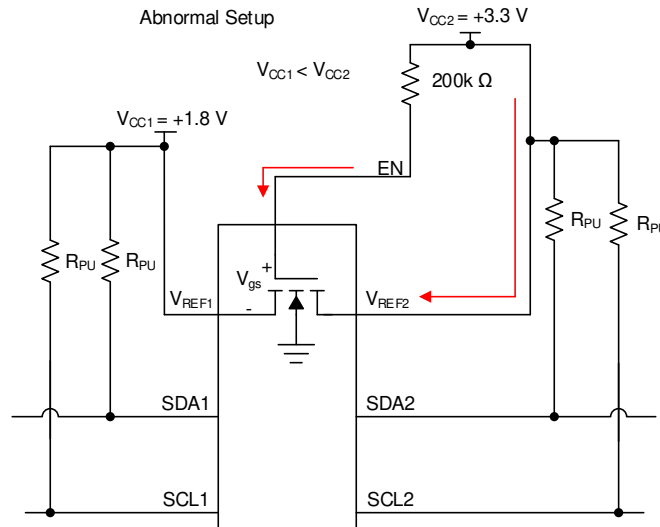


Figure 9-1. Normal Setup

Care should be taken to ensure VREF2 has an external resistor tied between it and VCC2. If VREF2 is tied directly to the VCC2 rail without a resistor, then there is no external resistance from the VCC2 to VCC1 to limit the current such as in Figure 9-2. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute

maximum continuous channel current specified in section 6.1. The continuous channel current is larger with a higher voltage difference between  $V_{CC1}$  and  $V_{CC2}$ .

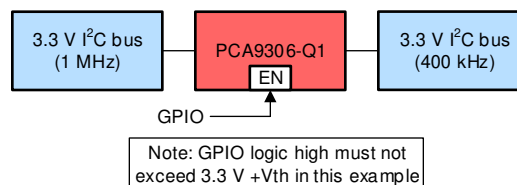
Figure 9-2 shows an improper set up. If  $V_{CC2}$  is larger than  $V_{CC1}$  but less than  $V_{th}$ , the impedance between  $V_{CC1}$  and  $V_{CC2}$  is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when  $V_{CC2}$  becomes larger than  $V_{CC1}$  by  $V_{th}$ . During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.



**Figure 9-2. Abnormal Setup**

### 9.1.3 Disconnecting a Target from the Main I2C Bus Using the EN Pin

PCA9306-Q1 can be used as a switch to disconnect one side of the device from the main I2C bus. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I2C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in Figure 9-3.

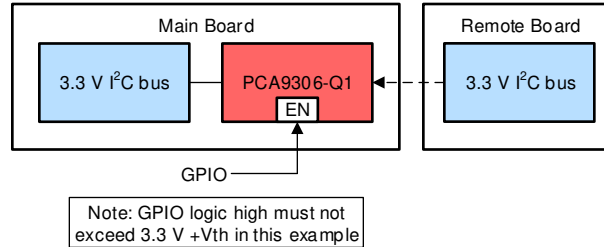


**Figure 9-3. Example of an I2C bus with multiple supported frequencies**

In this situation, if the controller is on the 1 MHz side then communicating at 1 MHz should not be attempted if PCA9306-Q1 were enabled. It needs to be disabled for PCA9306-Q1 to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When PCA9306-Q1 is disabled, the controller can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the PCA9306-Q1 is enabled, communication across both sides at 400 kHz is acceptable.

### 9.1.4 Supporting Remote Board Insertion to Backplane with PCA9306-Q1

Another situation where PCA9306-Q1 is advantageous when using its enable feature is when a remote board with I2C lines needs to be attached to a main board (backplane) with an I2C bus such as in Figure 9-4. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I2C device state machine causing the I2C bus to get stuck.

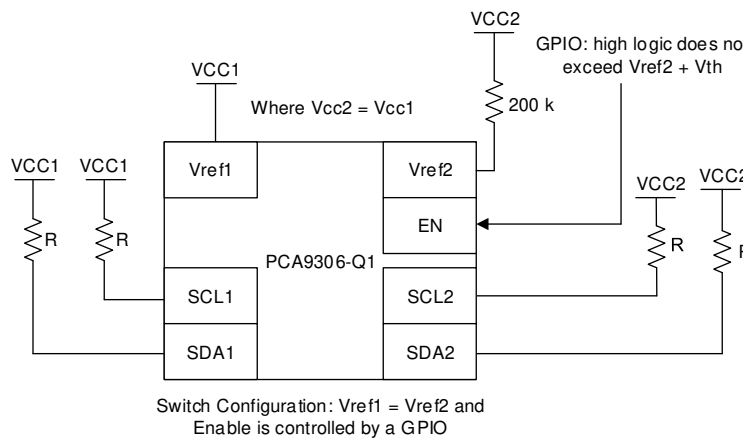


**Figure 9-4. An example of connecting a remote board to a main board (backplane)**

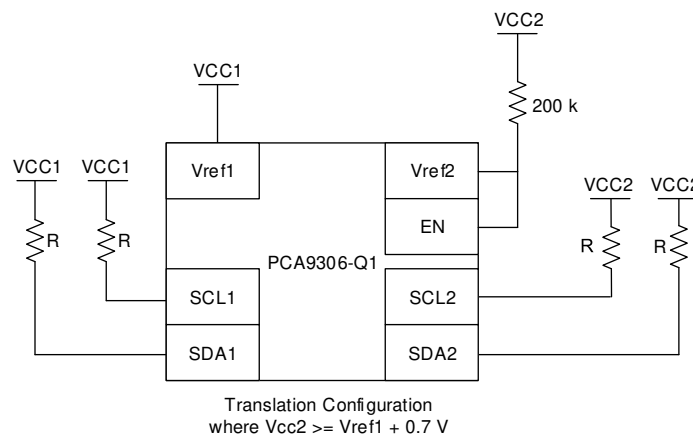
PCA9306-Q1 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

### 9.1.5 Switch Configuration

PCA9306-Q1 has the capability of being used with its  $V_{REF1}$  voltage equal to  $V_{REF2}$ . This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in Figure 9-5 and translation mode is shown in Figure 9-6.



**Figure 9-5. Switch Configuration**



**Figure 9-6. Translation Configuration**

When PCA9306-Q1 is in the switch configuration ( $V_{REF1} = V_{REF2}$ ), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the PCA9306-Q1 has the same propagation delay from side one to two and side two to one. The propagation delays become lower when  $V_{CC1}/V_{CC2}$  is

larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When PCA9306-Q1 is in translation mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference increases as the difference between  $V_{CC2}$  and  $V_{CC1}$  becomes larger.

### 9.1.6 Controller on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. PCA9306-Q1 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to placed on either side of the device. Figure 9-7 shows the controller on side two as opposed to the *Simplified Application Diagram* on page 1 of this data sheet.

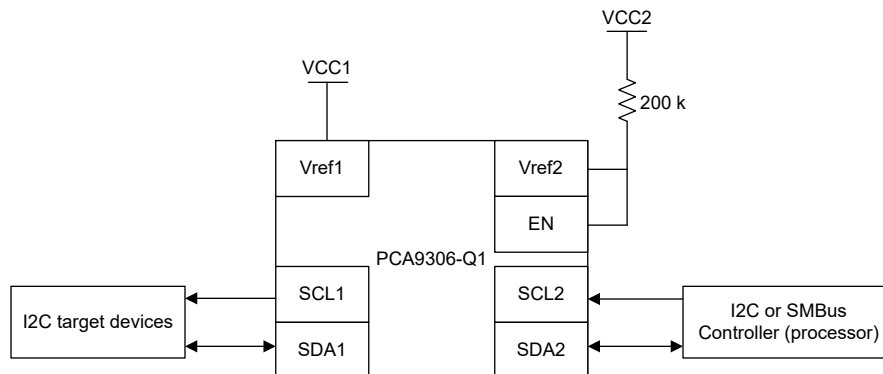


Figure 9-7. Controller on side 2 of PCA9306-Q1

### 9.1.7 LDO and PCA9306-Q1 Concerns

The  $V_{REF1}$  pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO can lose its regulation because of the bias current from  $V_{REF2}$  to  $V_{REF1}$ . If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the  $V_{REF1}$  node (both external and parasitic). This results in an increase in voltage on the  $V_{REF1}$  node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the  $V_{REF1}$  node), then the  $V_{REF1}$  voltage ends up stabilizing when  $V_{gs}$  of the pass FET is equal to  $V_{th}$ . This means  $V_{REF1}$  node voltage is  $V_{CC2} - V_{th}$ . Note that any target or controllers running off of the LDO now see the  $V_{CC2} - V_{th}$  voltage which may cause damage to those target or controllers if they are not rated to handle the increased voltage.

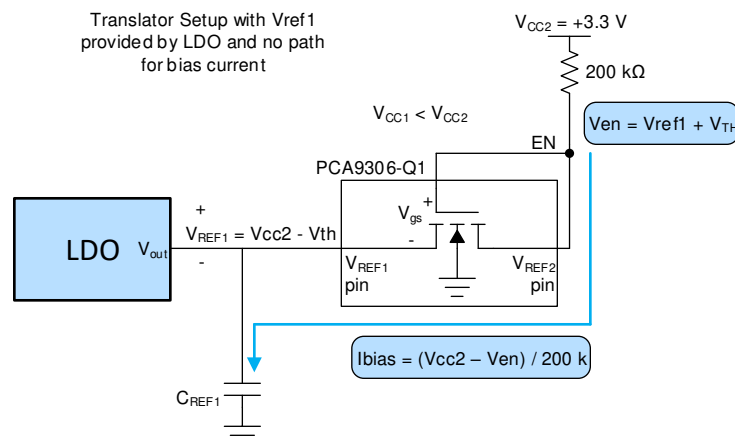


Figure 9-8. Example of no leakage current path when using LDO

To ensure LDO does not lose regulation due to the bias current of PCA9306-Q1, a weak pull down resistor can be placed on  $V_{REF1}$  to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by Equation 4 where 0.75 gives about 25% margin for error in case bias current increases during operation.

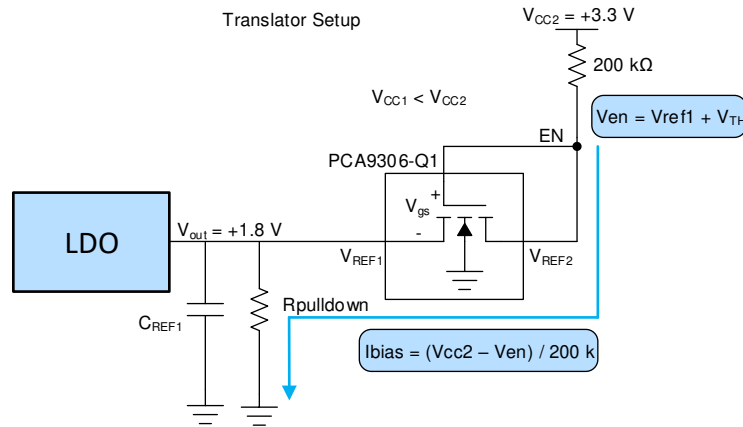


Figure 9-9. Example with Leakage current path when using an LDO

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

where

- $V_{th}$  is approximately 0.6 V

$$I_{bias} = (V_{CC2} - V_{en})/200k \quad (2)$$

$$R_{pulldown} = V_{OUT}/I_{bias} \quad (3)$$

$$\text{Recommended } R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

### 9.1.8 Current Limiting Resistance on $V_{REF2}$

The resistor is used to limit the current between  $V_{REF2}$  and  $V_{REF1}$  (denoted as  $R_{CC}$ ) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} : V_{en} = V_{REF1} + V_{th} \quad (5)$$

where

- $V_{th}$  is approximately 0.6V

Keep in mind  $R_{CC}$  should not be sized low enough that  $I_{CC}$  exceeds the absolute maximum continuous channel current specified in section 6.1 which is described in [Equation 6](#).

$$R_{CC}(\text{min}) \geq (V_{CC2} - V_{en})/0.128 : V_{en} = V_{REF1} + V_{th} \quad (6)$$

where

- $V_{th}$  is approximately 0.6V

## 9.2 Functional Block Diagram

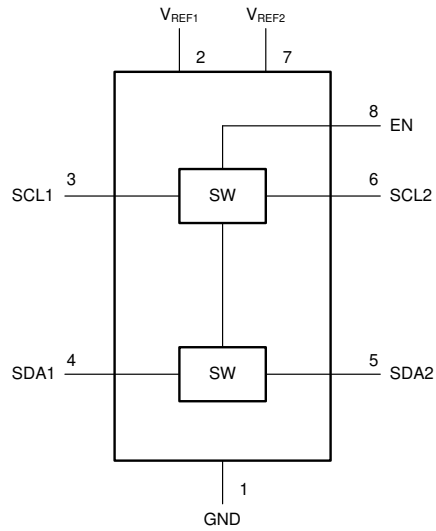


Figure 9-10. Logic Diagram (Positive Logic)

## 9.3 Feature Description

### 9.3.1 Enable (EN) Pin

The PCA9306-Q1 is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In [Figure 10-1](#), the PCA9306-Q1 always remains enabled when power is applied to VREF2. [Figure 10-1](#), the device becomes enabled when a control signal from a processor is in a logic high state. In another variation, the EN pin can be controlled by the output of a processor, but VREF2 can be connected to a power supply through a 200-kΩ resistor. In this case, VREF2 and EN are not to be tied together and the SCL and SDA switches are in a high impedance state when EN is in a logic-low state, as shown in the [Section 9.4](#) section.

### 9.3.2 Voltage Translation

The primary feature of the PCA9306-Q1 is translating voltage from an I<sup>2</sup>C bus referenced to VREF1 up to an I<sup>2</sup>C bus referenced to VDPU, to which VREF2 is connected through a 200-kΩ pullup resistor. When translating a standard, open-drain I<sup>2</sup>C bus, this is achieved by simply connecting pullup resistors from SCL1 and SDA1 to VREF1 and connecting pullup resistors from SCL2 and SDA2 to VDPU. Find more information on sizing the pullup resistors in the [Sizing Pullup Resistor](#) section.

## 9.4 Device Functional Modes

[Table 9-1](#) describes the two functions of the translation device.

**Table 9-1. Function Table**

INPUT EN <sup>(1)</sup>	TRANSLATOR FUNCTION
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

- (1) EN is controlled by the VREF2 logic levels and must be at least 1 V higher than VREF1 for best translator operation.

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Application Information

#### 10.1.1 General Applications of I<sup>2</sup>C

As with the standard I<sup>2</sup>C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I<sup>2</sup>C devices, in addition to SMBus devices. Standard-mode I<sup>2</sup>C devices only specify 3 mA in a generic I<sup>2</sup>C system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by  $V_{REF1}$ . When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain ( $V_{DPU}$ ) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

#### 10.2 Typical Application

Figure 10-1 and Figure 10-2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

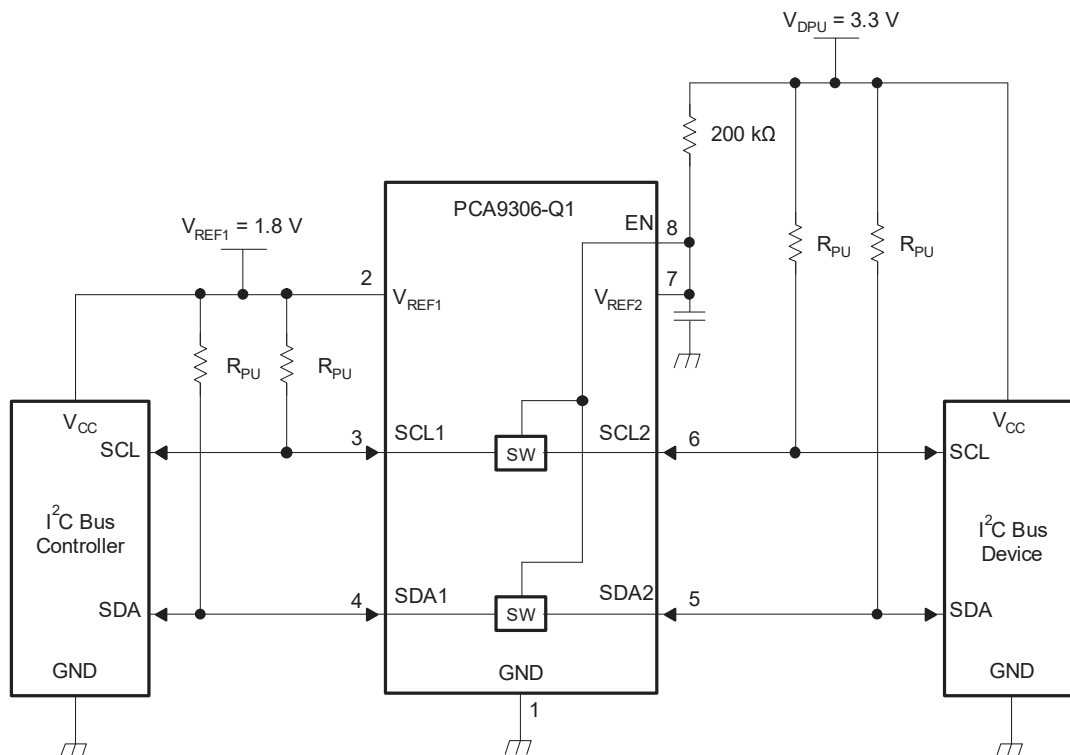


Figure 10-1. Typical Application Circuit (Switch Always Enabled) Diagram



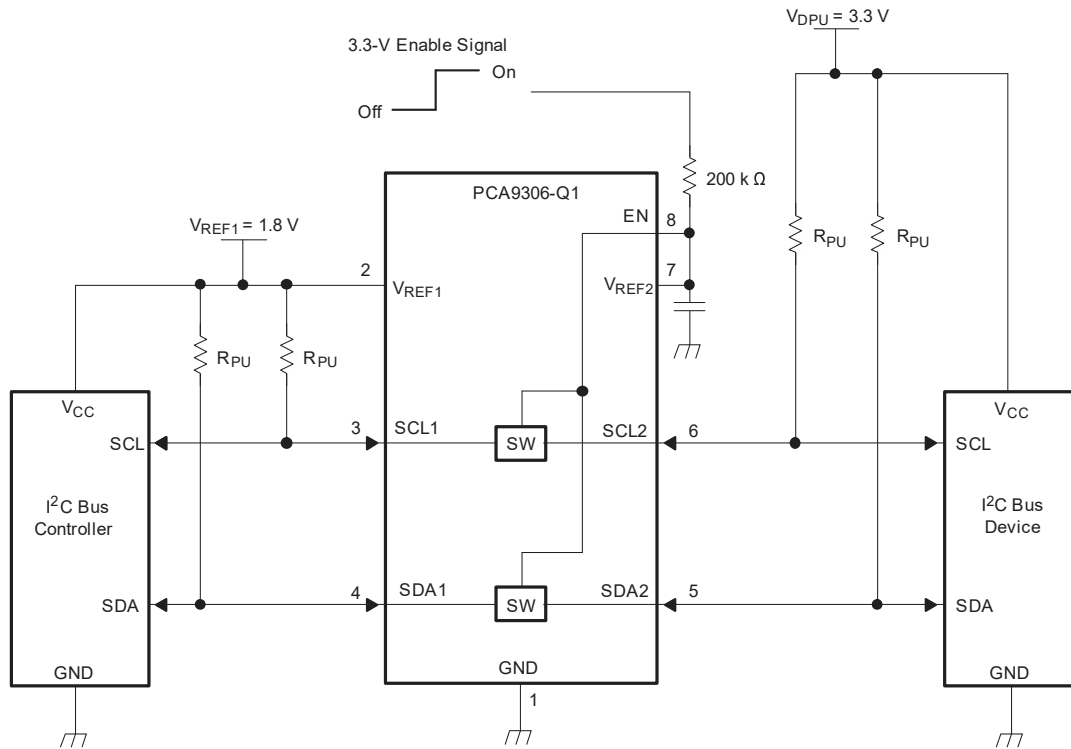


Figure 10-2. Typical Application Circuit (Switch Enable Control) Diagram

## 10.2.1 Design Requirements

Table 10-1 lists the design parameters for this example.

Table 10-1. Design Parameters

		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{REF2}$	Reference voltage	$V_{REF1} + 0.6$	2.1	5	V
EN	Enable input voltage	$V_{REF1} + 0.6$	2.1	5	V
$V_{REF1}$	Reference voltage	0	1.5	4.4	V
$I_{PASS}$	Pass switch current		14		mA
$I_{REF}$	Reference-transistor current		5		$\mu$ A
$T_A$	Operating free-air temperature	-40		105	$^{\circ}$ C

(1) All typical values are at  $T_A = 25^{\circ}$ C.

## 10.2.2 Detailed Design Procedure

### 10.2.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to  $V_{REF2}$  and both pins pulled to high-side  $V_{DDPU}$  through a pullup resistor (typically 200 k $\Omega$ ). This allows  $V_{REF2}$  to regulate the EN input. A filter capacitor on  $V_{REF2}$  is recommended. The I<sup>2</sup>C bus controller output can be totem-pole or open-drain (pullup resistors may be required) and the I<sup>2</sup>C bus device output can be totem-pole or open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to  $V_{DDPU}$ ). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ( $V_{REF1}$ ) is connected to the processor core power-supply voltage.

### 10.2.2.2 Sizing Pullup Resistor

The pullup resistor value must limit the current through the pass transistor, when it is in the ON state, to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35 \text{ V}}{0.015 \text{ A}} \quad (7)$$

Table 10-2 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) must be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the PCA9306-Q1 device.

**Table 10-2. Pullup Resistor Values**

PULLUP RESISTOR VALUE ( $\Omega$ ) <sup>(1) (2)</sup>						
$V_{DPU}$	15 mA		10 mA		3 mA	
	NOMINAL	+10% <sup>(3)</sup>	NOMINAL	+10% <sup>(3)</sup>	NOMINAL	+10% <sup>(3)</sup>
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for  $V_{OL} = 0.35 \text{ V}$

(2) Assumes output driver  $V_{OL} = 0.175 \text{ V}$  at stated current

(3) +10% to compensate for  $V_{DD}$  range and resistor tolerance

### 10.2.2.3 PCA9306-Q1 Bandwidth

The maximum frequency of the PCA9306-Q1 device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The PCA9306-Q1 device behaves like a standard switch where the bandwidth of the device is dictated by the ON-resistance and ON-capacitance of the device.

Figure 10-5 shows a bandwidth measurement of the PCA9306-Q1 device using a two-port network analyzer.

The 3-dB point of the PCA9306-Q1 device is approximately 600 MHz. However, this is an analog type of measurement. For digital applications, the signal must not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth must be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the PCA9306-Q1 device, digital clock frequency of > 100 MHz can be achieved.

The PCA9306-Q1 device does not provide any drive capability like the PCA9515 or PCA9517 series of devices. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the PCA9306-Q1 device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from the PCA9306-Q1 device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency ( $f_{knee}$ ). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than  $f_{knee}$  are insignificant in determining the shape of the signal.

To calculate  $f_{knee}$ :

$$f_{knee} = 0.5 / RT \text{ (10–90\%)} \tag{8}$$

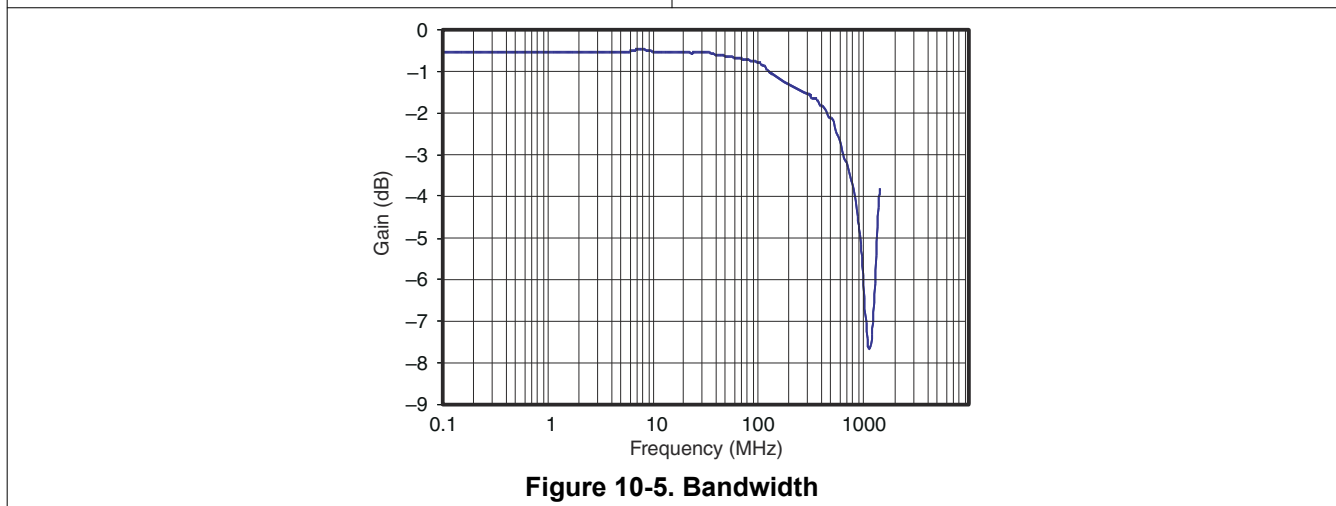
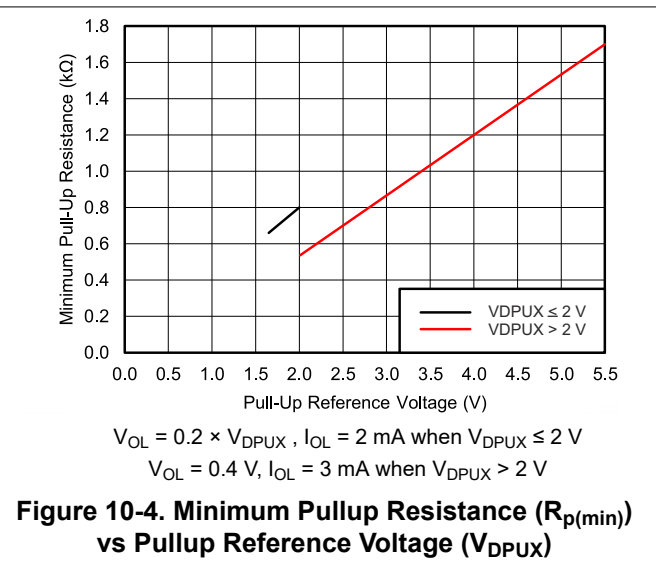
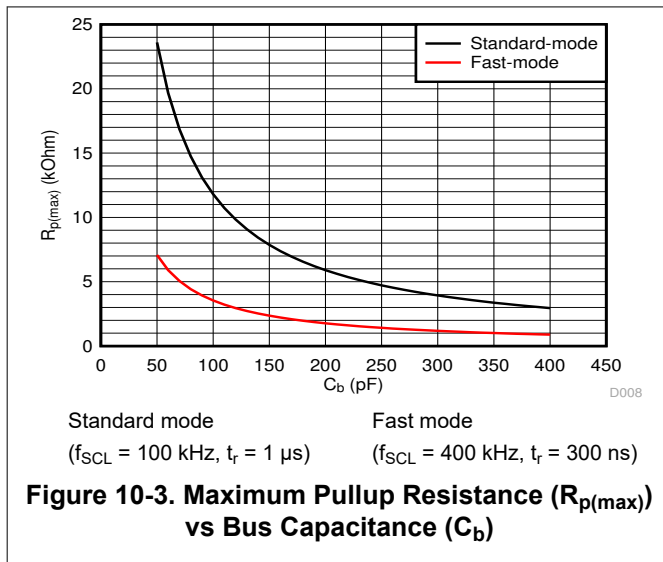
$$f_{knee} = 0.4 / RT \text{ (20–80\%)} \tag{9}$$

For signals with rise-time characteristics based on 10- to 90-percent thresholds,  $f_{knee}$  is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications,  $f_{knee}$  is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306-Q1 device close to the I<sup>2</sup>C output of the processor.
- The trace length must be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8-V side; be aware that a slower fall time is to be expected.

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

For supplying power to the PCA9306-Q1, the VREF1 pin can be connected directly to a power supply. The VREF2 pin must be connected to the VDPU power supply through a 200-k $\Omega$  resistor. Failure to have a high impedance resistor between VREF2 and VDPU results in excessive current draw and unreliable device operation.

## 12 Layout

### 12.1 Layout Guidelines

For printed-circuit board (PCB) layout of the PCA9306-Q1, common PCB layout practices must be followed; however, additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor must be placed as close to V<sub>REF2</sub> as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the PCA9306-Q1 device. These best practices are shown in Figure 12-1.

For the layout example provided in Figure 12-1, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to V<sub>CC</sub> or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in Figure 12-1.

### 12.2 Layout Example

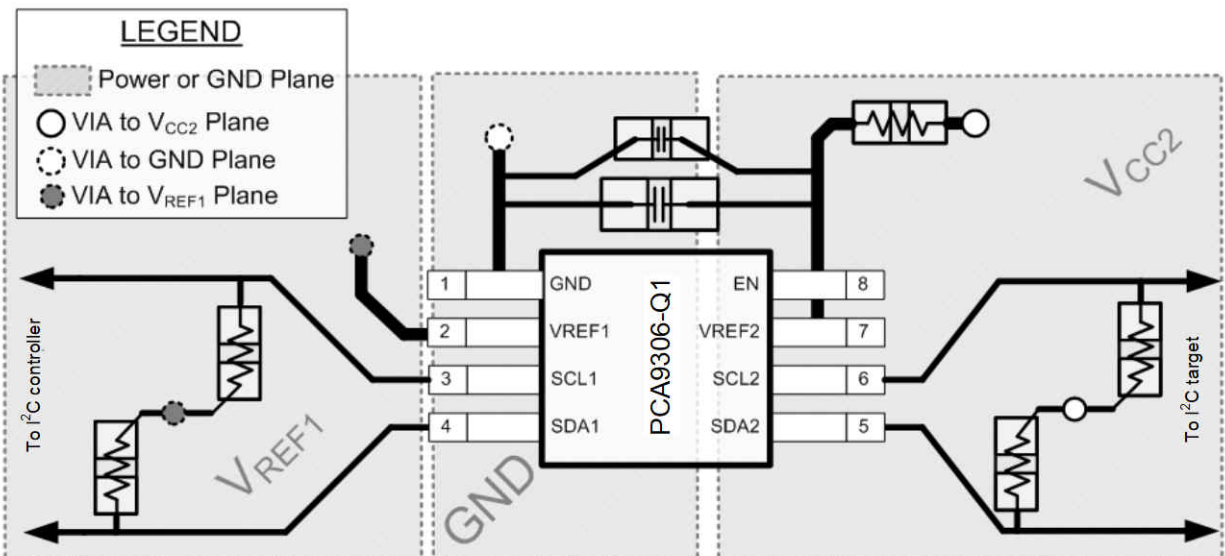


Figure 12-1. PCA9306-Q1 Layout Example

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

Technical Documents – [PCA9306-Q1 technical documents](#)

### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 13.4 Trademarks

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### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9306IDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CCUS	<a href="#">Samples</a>
PCA9306TDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(CCUS, YAAS)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF PCA9306-Q1 :**

- Catalog : [PCA9306](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9306IDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306TDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9306IDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0
PCA9306TDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

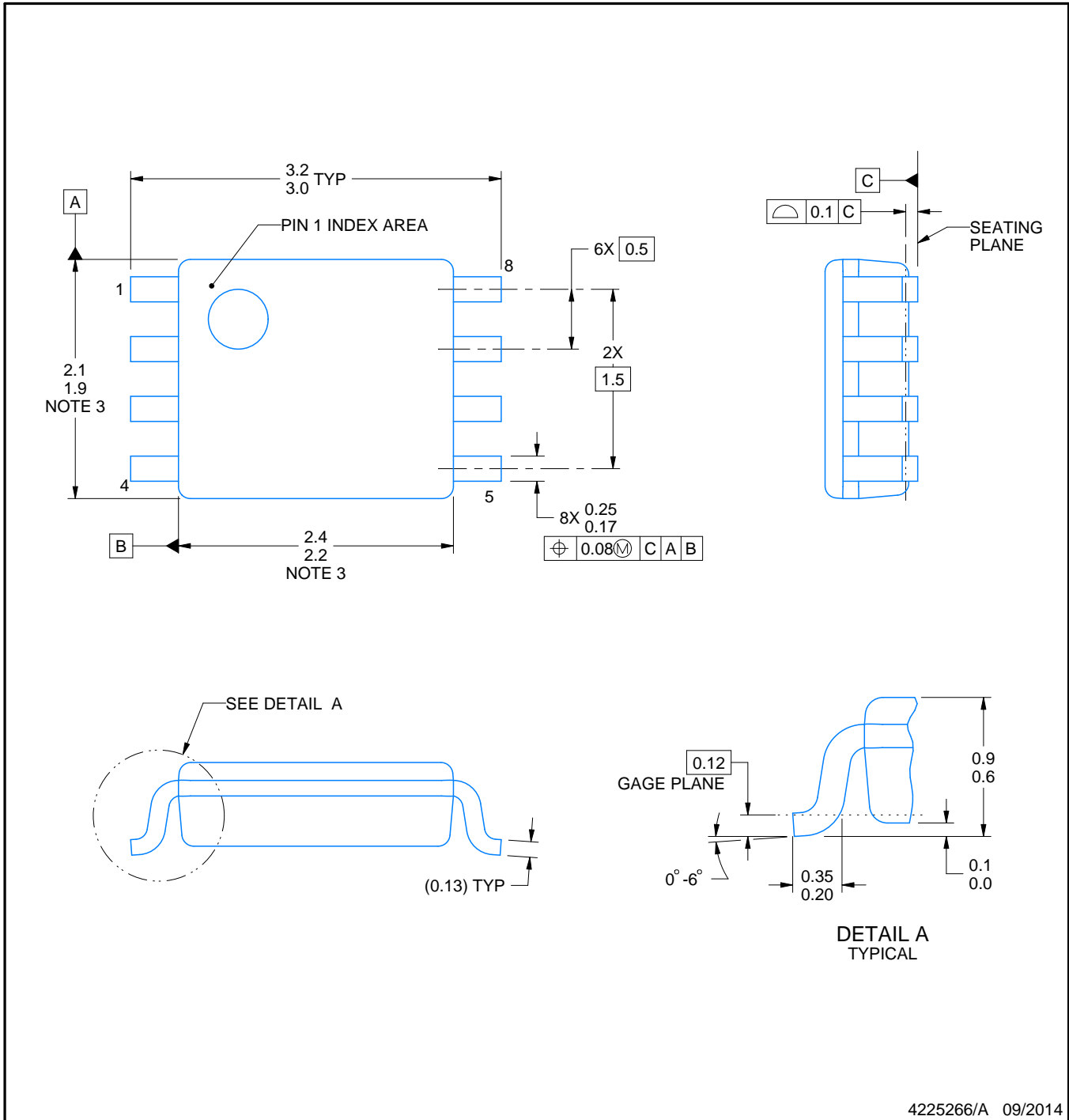
# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



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**NOTES:**

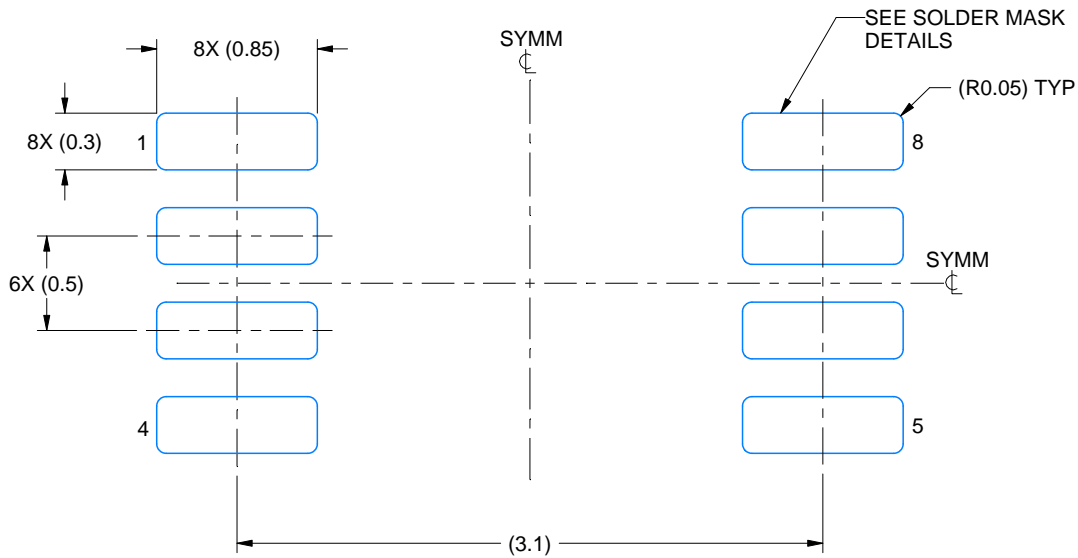
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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