CSD88537ND 双路 60V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低 Q_g 和 Q_{gd}
- 雪崩额定值
- 无铅
- 符合 RoHS 环保标准
- 无卤素

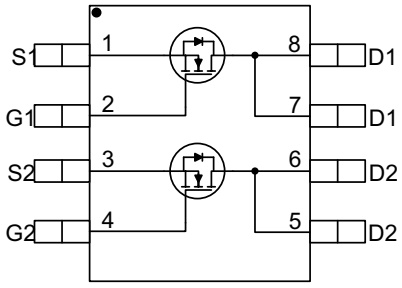
2 应用范围

- 用于电机控制的半桥
- 同步降压转换器

3 说明

这款双路小外形尺寸 (SO)-8，60V，12.5mΩ NexFET™ 功率 MOSFET 旨在用作低电流电机控制应用中的半桥。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	60		V
Q_g	栅极电荷总量 (10V)	14		nC
Q_{gd}	栅漏栅极电荷	2.3		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	15	mΩ
		V_{GS} = 10V	12.5	mΩ
$V_{GS(th)}$	阈值电压	3.0		V

订购信息(1)

器件	介质	数量	封装	出货
CSD88537ND	13 英寸卷带	2500	SO-8 塑料封装	卷带封装
CSD88537NDT	7 英寸卷带	250		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

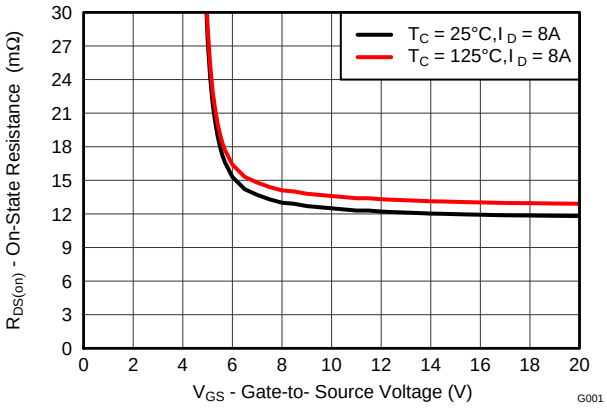
T_A = 25°C		值	单位
V_{DS}	漏源电压	60	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	15	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	16	
	持续漏极电流 (1)	8.0	
I_{DM}	脉冲漏极电流，T_A = 25°C 时测得(2)	108	A
P_D	功率耗散(1)	2.1	W
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 32，L = 0.1mH，R_G = 25Ω	51	mJ

(1) $R_{\theta JA}$ = 60°C/W，这是在一个厚度 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司 的铜焊盘上测得的典型值

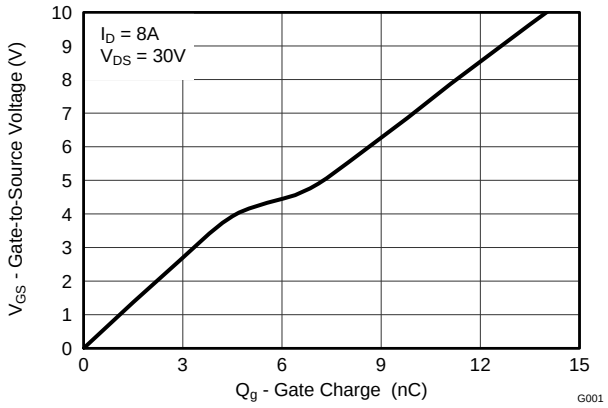
。

(2) 最大 $R_{\theta JL}$ = 20°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

Changes from Original (January 2014) to Revision A **Page**

- 已将脉冲漏极电流从 62A 增加为 108A 1
- 更新了脉冲漏极电流条件 1
- Changed $R_{\theta JC}$ to $R_{\theta JL}$ in *Thermal Information* 4
- Updated the SOA in Figure 10 7

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.6	3	3.6	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V, I_D = 8 A		15	19	mΩ
		V_{GS} = 10 V, I_D = 8 A		12.5	15	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 8 A		42		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		1080	1400	pF
C_{oss}	Output Capacitance			133	173	pF
C_{rss}	Reverse Transfer Capacitance			4	5.2	pF
R_G	Series Gate Resistance			5.5	11	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 30 V, I_D = 8 A		14	18	nC
Q_{gd}	Gate Charge Gate-to-Drain			2.3		nC
Q_{gs}	Gate Charge Gate-to-Source			4.6		nC
$Q_{g(th)}$	Gate Charge at V_{th}			3.4		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		25		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 8 A, R_G = 0 Ω		6		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			5		ns
t_f	Fall Time			19		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 8 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 8 A, di/dt = 300 A/µs		50		nC
t_{rr}	Reverse Recovery Time			30		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JL}$	Junction-to-Lead Thermal Resistance(1)			20	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			75	

(1) $R_{\theta JL}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JL}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

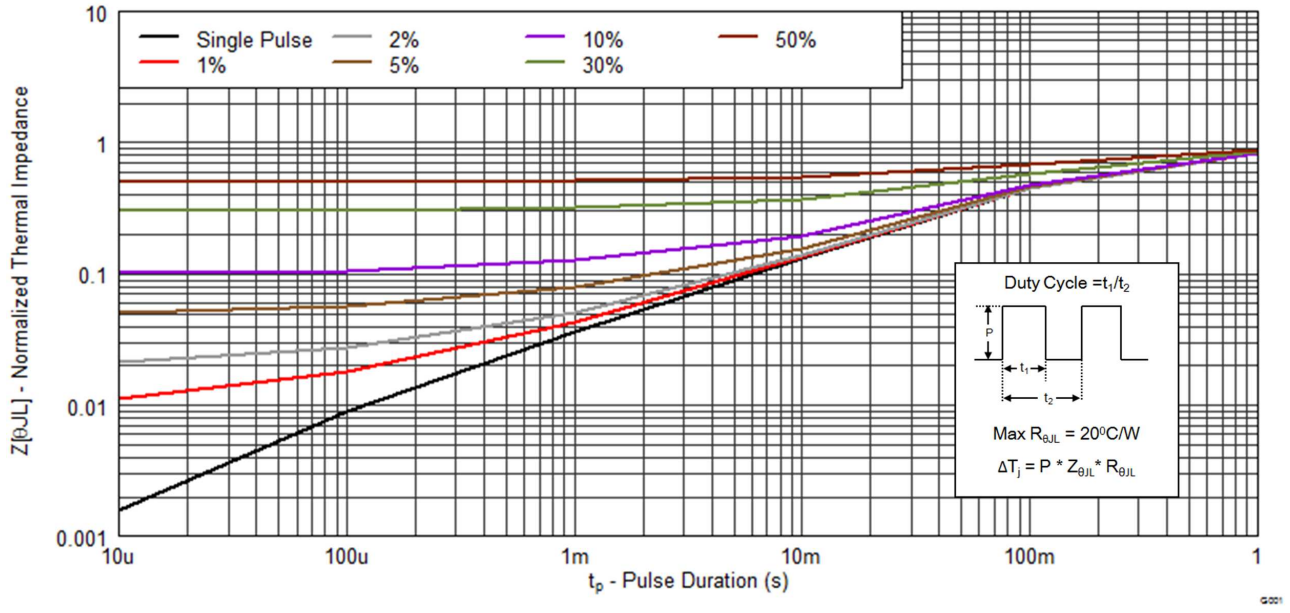


Figure 1. Transient Thermal Impedance

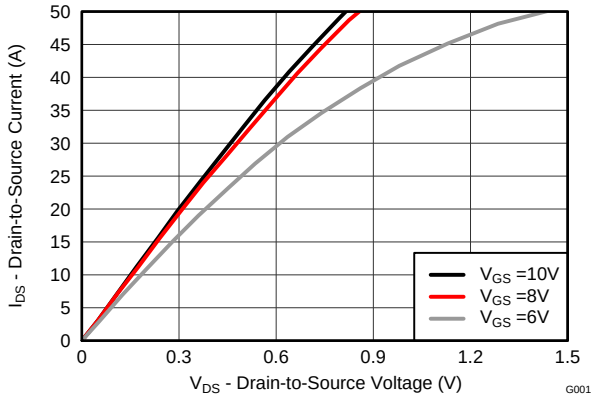


Figure 2. Saturation Characteristics

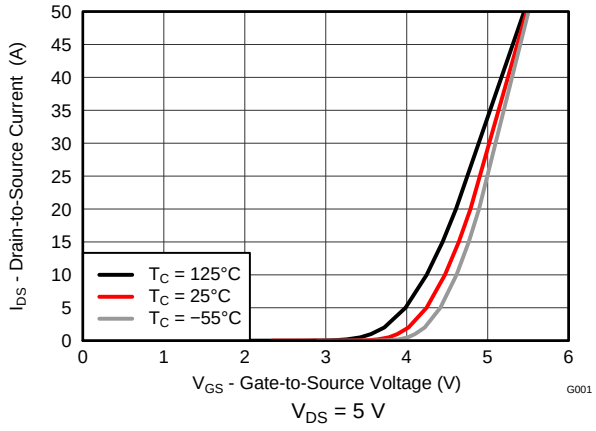


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

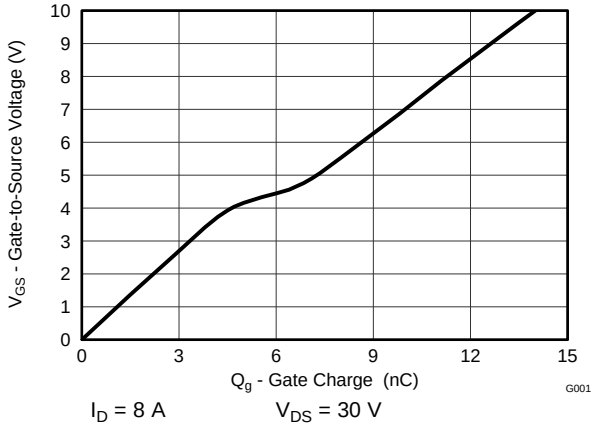


Figure 4. Gate Charge

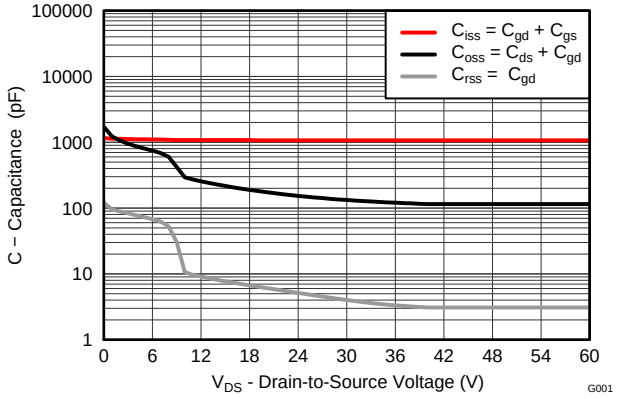


Figure 5. Capacitance

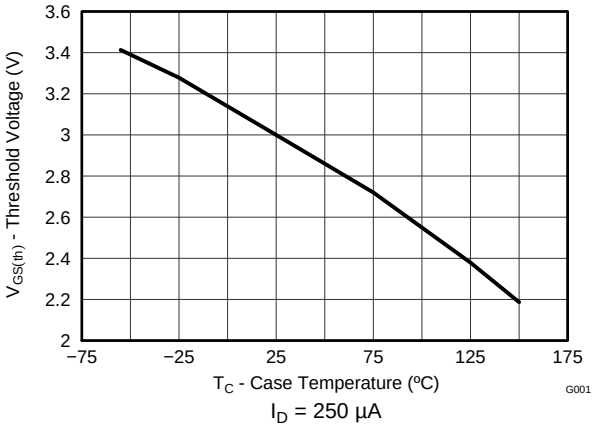


Figure 6. Threshold Voltage vs Temperature

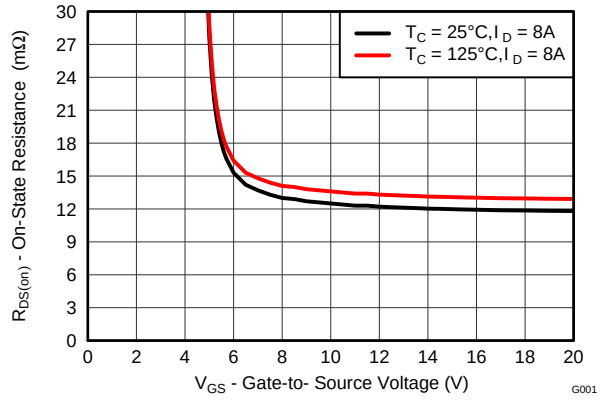


Figure 7. On-State Resistance vs Gate-to-Source Voltage

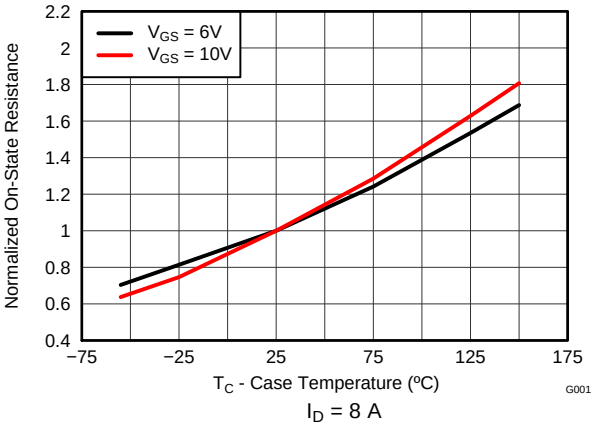


Figure 8. Normalized On-State Resistance vs Temperature

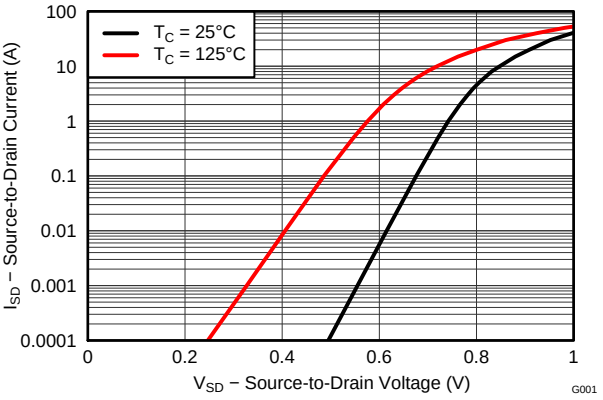


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

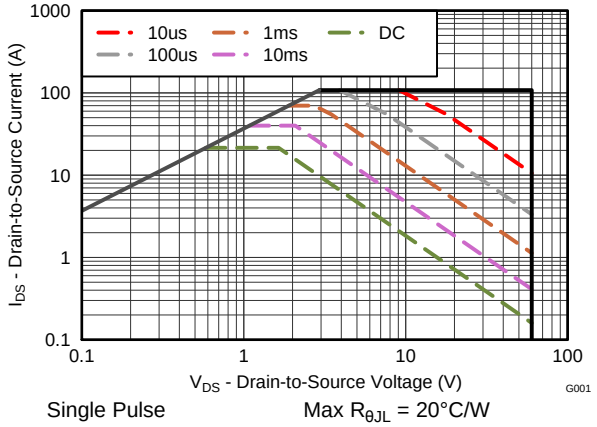


Figure 10. Maximum Safe Operating Area

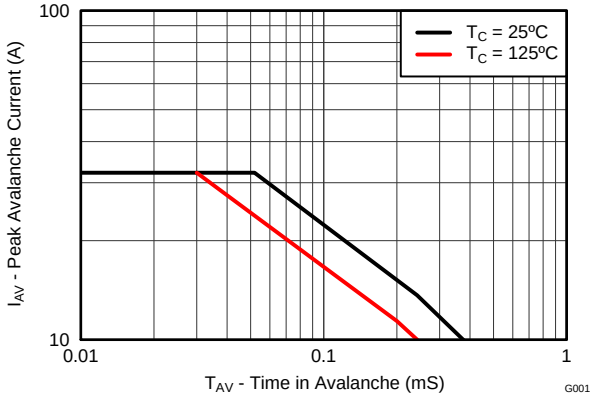


Figure 11. Single Pulse Unclamped Inductive Switching

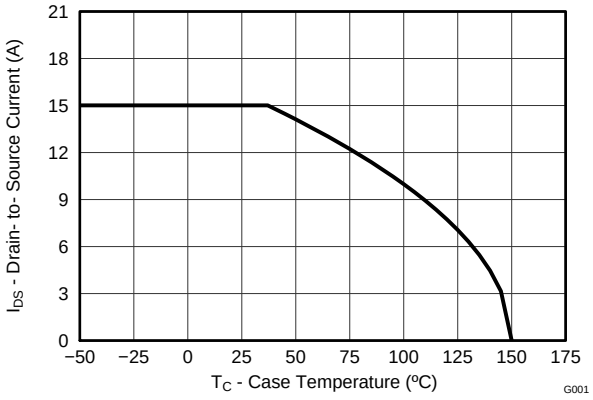


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

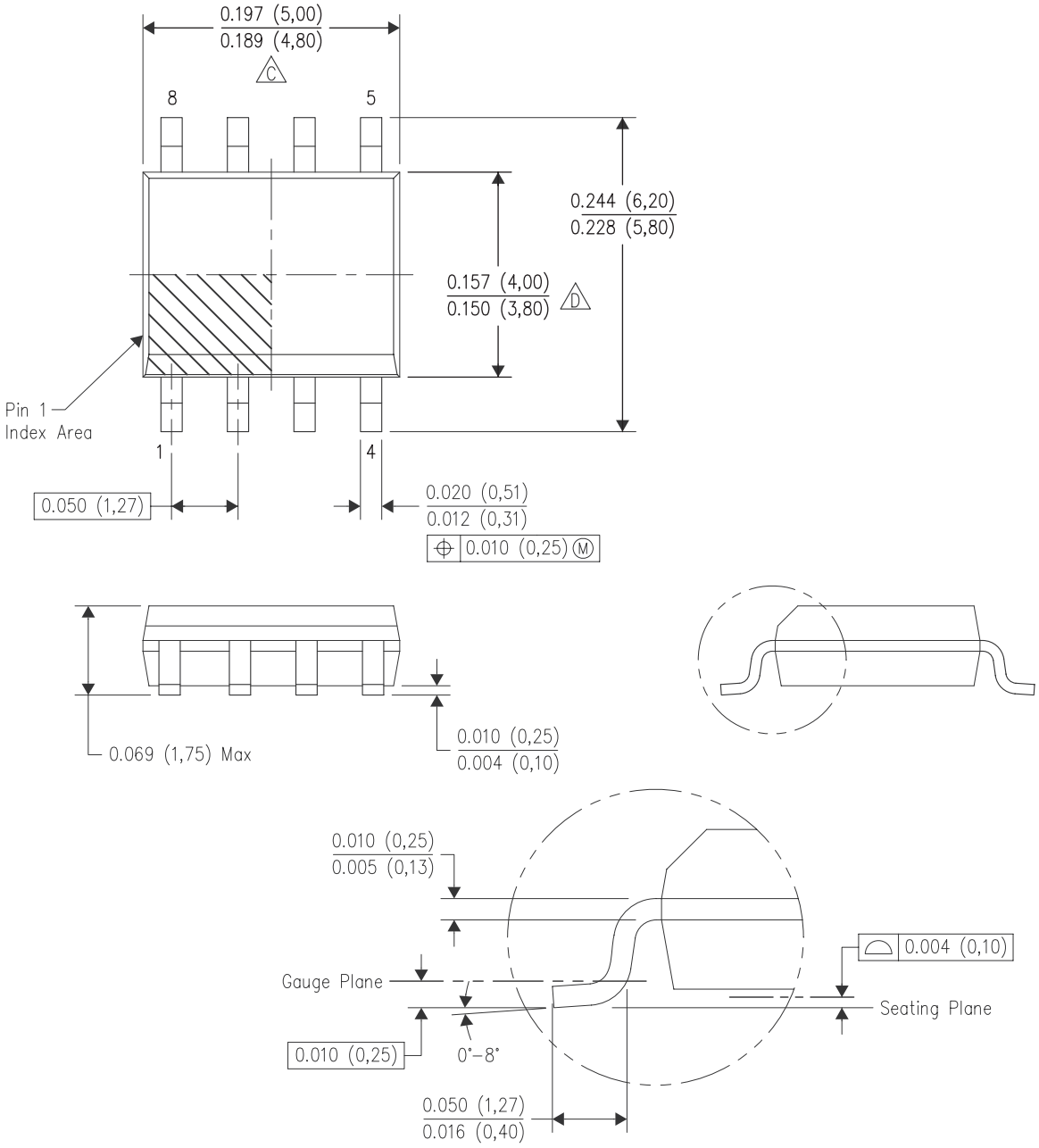
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

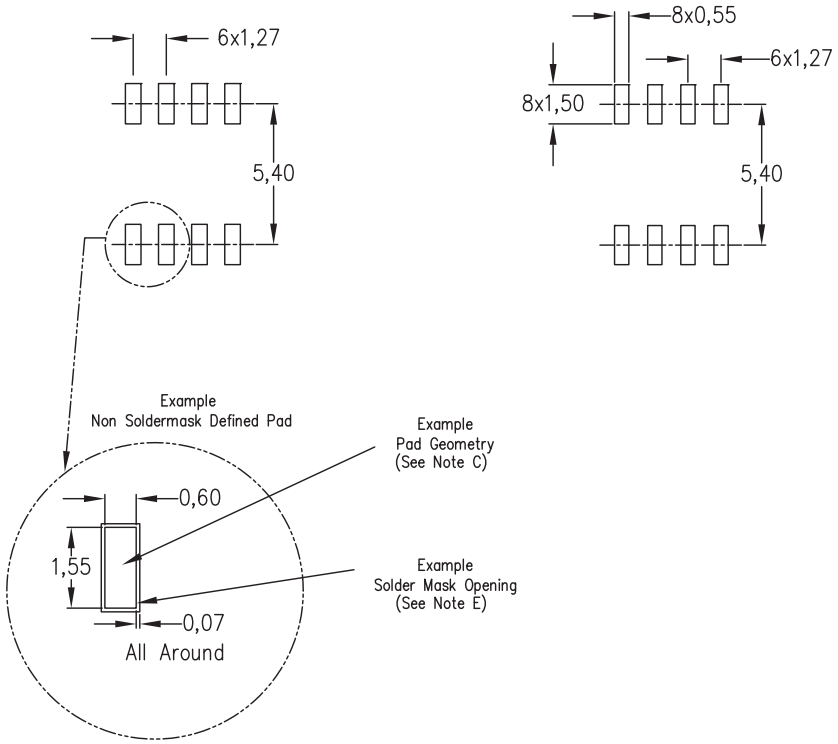
以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 SO-8 封装尺寸



1. 所有线性尺寸的单位均为英寸（毫米）。
2. 本图纸如有变更，恕不通知。
3. 主体长度不包括模具毛边、突出或料口毛刺。 每侧的模具毛边、突出或料口毛刺不得超过 0.006 英寸（0.15 毫米）。
4. 主体宽度不包括引脚间的毛边。 每侧的引脚间毛边不得超过 0.017 英寸（0.43 毫米）。
5. 参考 JEDEC MS-012 变体 AA。

7.2 建议的 PCB 模板布局和开口



1. 所有线性尺寸的单位是毫米。
2. 本图纸如有变更，恕不通知。
3. 建议在替代设计中采用公布的 IPC-7351 标准。
4. 具有漏斗形壁和圆角的激光切割窗孔将提供更佳的焊锡膏脱离。 客户应联系其电路板组装站点获取漏网印板设计建议。 关于其他模板建议，请参见 IPC-7525。
5. 客户应联系其电路板生产厂获取有关信号盘之间以及信号盘周围的阻焊层容差的信息。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88537ND	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88537N	Samples
CSD88537NDT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88537N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

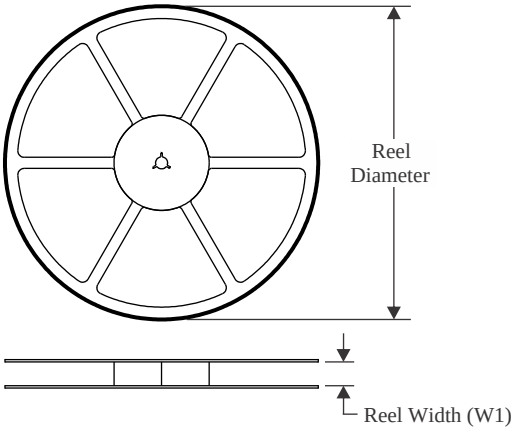
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

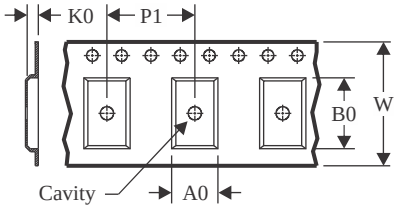
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

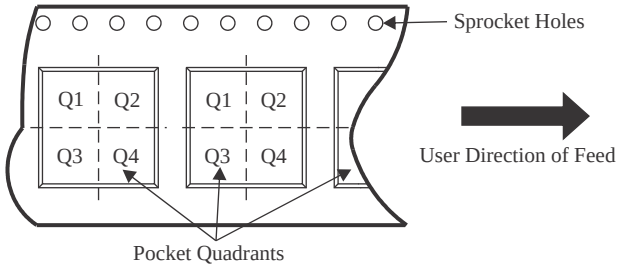


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

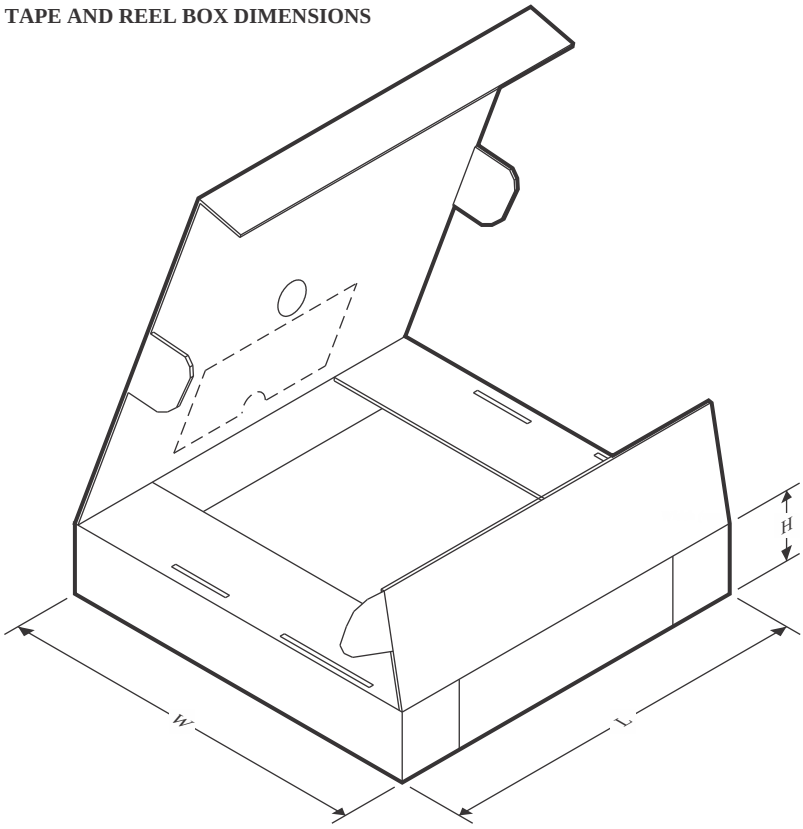
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD88537NDT	SOIC	D	8	250	178.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

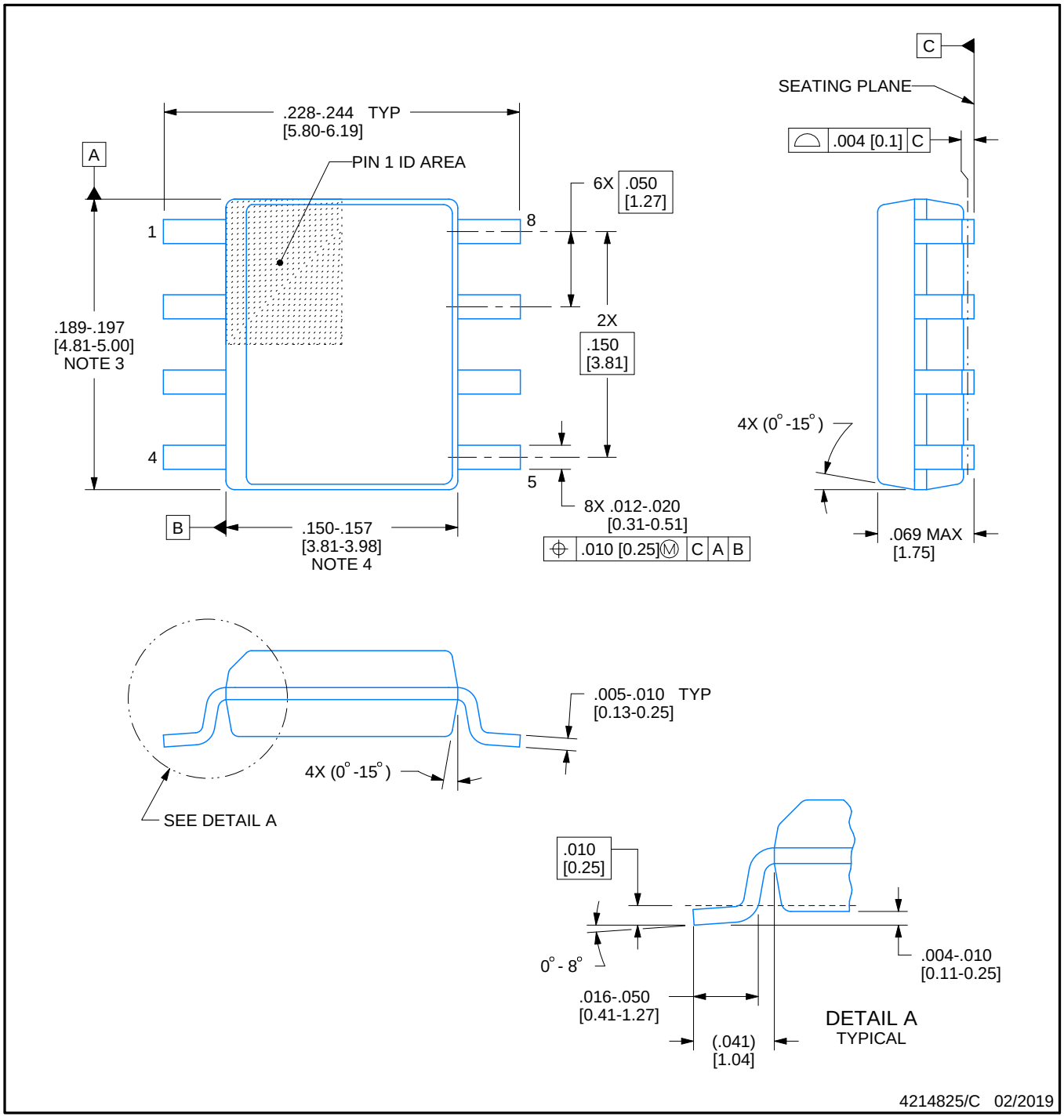
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD88537NDT	SOIC	D	8	250	180.0	180.0	79.0

PACKAGE OUTLINE

D0008A

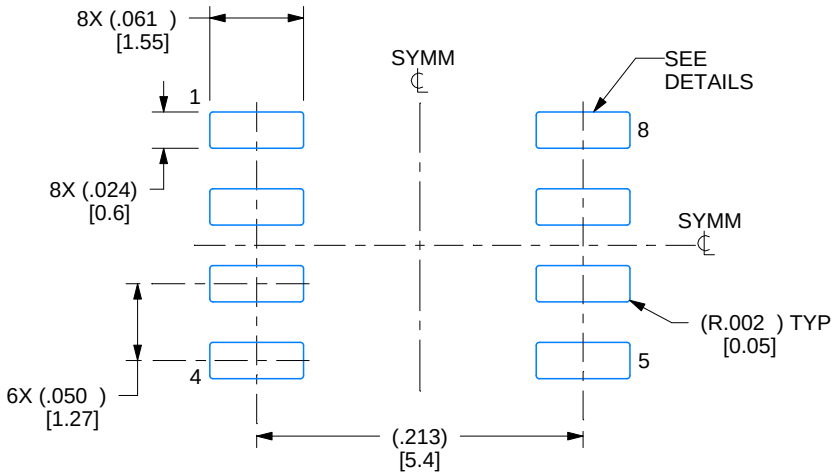
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

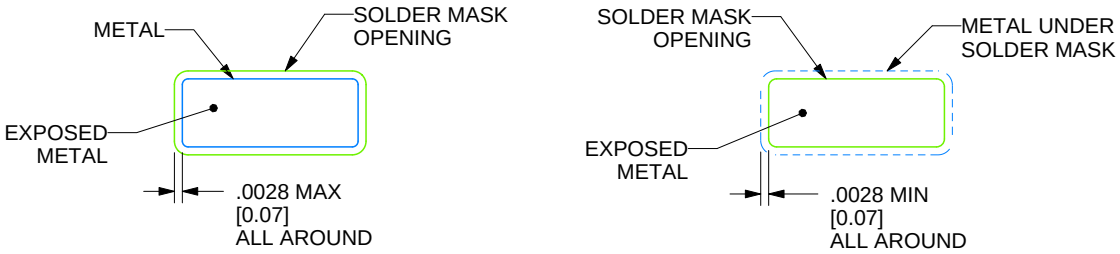


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

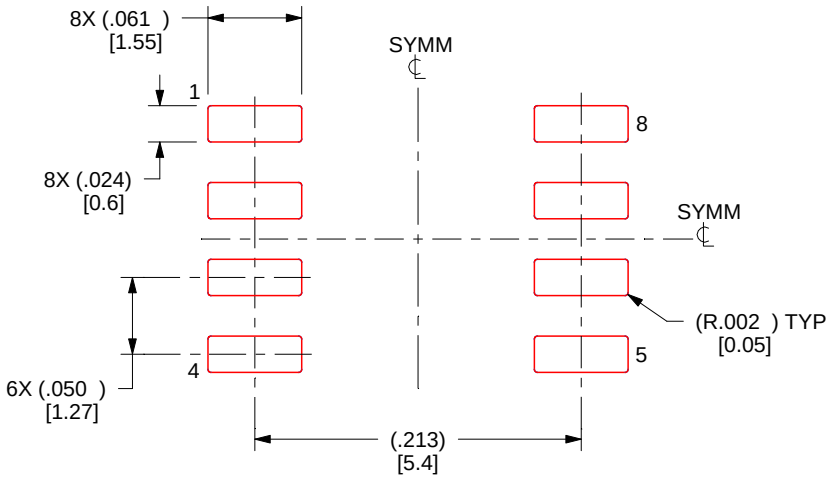
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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