TPS51275B-1 Dual Synchronous, Step-Down Controller With 5-V and 3.3-V LDOs

1 Features

- Input Voltage Range: 5 V to 24 V
- Output Voltages: 5 V and 3.3 V (Adjustable Range ±10%)
- Built-in, 100-mA, 5-V, and 3.3-V LDOs
- Clock Output for Charge-Pump
- ±1% Reference Accuracy
- Adaptive On-Time D-CAP™ Mode Control Architecture with 300-kHz and 355-kHz Frequency Setting
- Out-of-Audio™ (OOA) Light-Load Operation
- Internal 3.2-ms Voltage Servo Soft-Start
- Low-Side $R_{DS(on)}$ Current Sensing Scheme
- Built-In Output Discharge Function
- Separate Enable Input for Switchers
- Dedicated OC Setting Terminals
- Power Good Indicator
- OVP, UVP, and OCP Protection
- Non-Latch UVLO and OTP Protection
- 20-Pin, 3-mm × 3-mm, WQFN (RUK) Package

2 Applications

- Notebook Computers
- Tablet Computers
- Desktop Computers

3 Description

The TPS51275B-1 device is a cost-effective, dual-synchronous buck controller targeted for notebook system-power supply solutions. The device has 5-V and 3.3-V low-dropout regulators (LDOs) and requires few external components. The 260-kHz VCLK output can be used to drive an external charge pump, generating gate drive voltage for the load switches without reducing the main converter efficiency. The TPS51275B-1 device supports high efficiency, fast transient response and provides a combined power-good signal. Adaptive on-time, D-CAP control provides convenient and efficient operation. The device operates with a supply input voltage ranging from 5 to 24 V and supports output voltages of 5 V and 3.3 V. The TPS51275B-1 device is available in a 20-pin, 3-mm × 3-mm, WQFN package and is specified from –40°C to 85°C.

Device Information(1)

PART NUMBER	SKIP MODE	ALWAYS ON-LDO
TPS51275B-1	OOA	VREG3 and VREG5

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Diagram

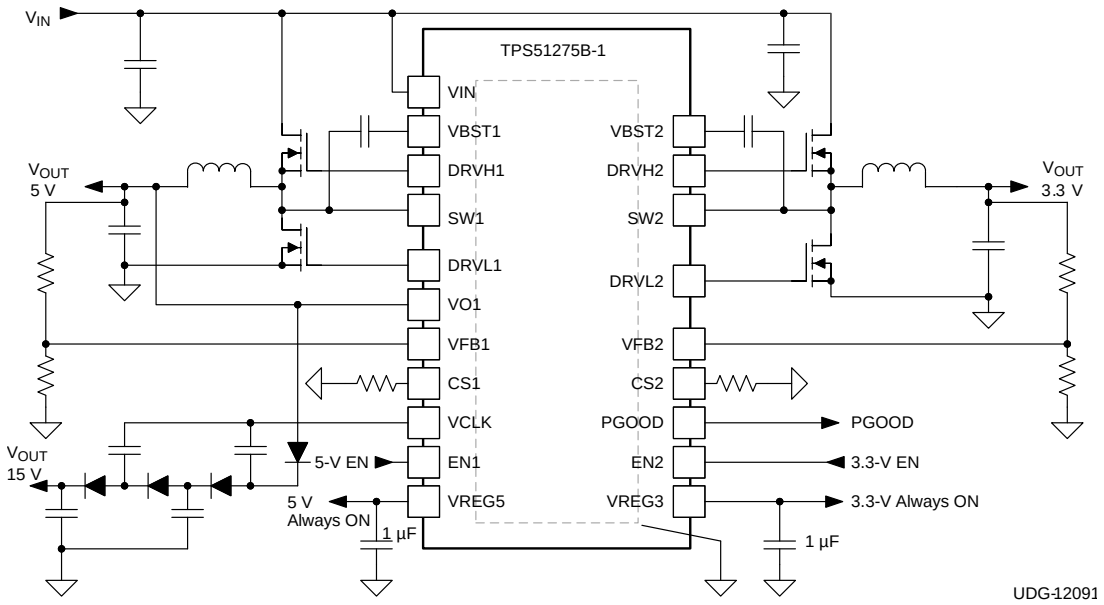


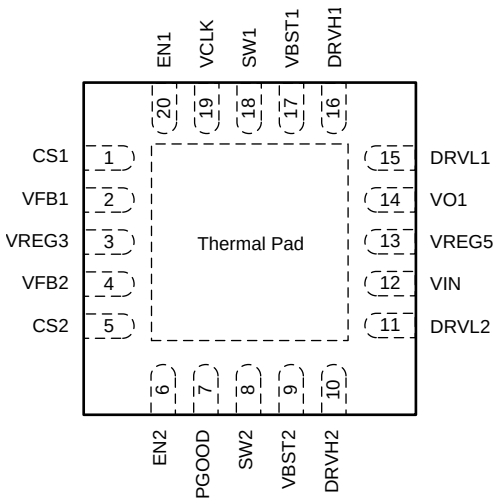
Table of Contents

5 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

6 Pin Configuration and Functions

RUK Package
20-Pin WQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS1	1	O	Sets the channel 1 OCL trip level
CS2	5	O	Sets the channel 2OCL trip level
DRVH1	16	O	High-side driver output
DRVH2	10	O	High-side driver output
DRVL1	15	O	Low-side driver output
DRVL2	11	O	Low-side driver output
EN1	20	I	Channel 1 enable
EN2	6	I	Channel 2 enable
PGOOD	7	O	Power good output flag. Open drain output. Pull up to external rail through a resistor
SW1	18	O	Switch-node connection
SW2	8	O	Switch-node connection
VBST1	17	I	Supply input for high-side MOSFET (bootstrap terminal). Connect a capacitor from this pin to the SWx pin.
VBST2	9	I	
VCLK	19	O	Clock output for charge pump
VFB1	2	I	Voltage feedback input
VFB2	4	I	
VIN	12	I	Power conversion voltage input. Apply the same voltage as drain voltage of high-side MOSFETs of channel 1 and channel 2.
VO1	14	I	Output voltage input, 5-V input for switch-over
VREG3	3	O	3.3-V LDO output
VREG5	13	O	5-V LDO output
Thermal pad		—	Ground (GND) terminal, solder to the ground plane

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage(2)	VBST1, VBST2	–0.3	32	V
	VBST1, VBST2(3)	–0.3	6	
	SW1, SW2	–6.0	26	
	VIN	–0.3	26	
	EN1, EN2	–0.3	6	
	VFB1, VFB2	–0.3	3.6	
	VO1	–0.3	6	
Output voltage(2)	DRVH1, DRVH2	–6.0	32	V
	DRVH1, DRVH2(3)	–0.3	6	
	DRVH1, DRVH2(3) (pulse width < 20 ns)	–2.5	6	
	DRVL1, DRVL2	–0.3	6	
	DRVL1, DRVL2 (pulse width < 20 ns)	–2.5	6	
	PGOOD, VCLK, VREG5	–0.3	6	
	VREG3, CS1, CS2	–0.3	3.6	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted
(3) Voltage values are with respect to SW terminals.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VIN	5	24	V
Input voltage (1)	VBST1, VBST2	–0.1	30	V
	VBST1, VBST2 (2)	–0.1	5.5	
	SW1, SW2	–5.5	24	
	EN1, EN2	–0.1	5.5	
	VFB1, VFB2	–0.1	3.5	
	VO1	–0.1	5.5	
Output voltage (1)	DRVH1, DRVH2	–5.5	30	V
	DRVH1, DRVH2 (2)	–0.1	5.5	
	DRVL1, DRVL2	–0.1	5.5	
	PGOOD, VCLK, VREG5	–0.1	5.5	
	VREG3, CS1, CS2	–0.1	3.5	
Operating free-air temperature, T_A		–40	85	°C

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) Voltage values are with respect to the SW terminal.

7.4 Thermal Information

THERMAL METRIC (1)		RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	
ψ_{JT}	Junction-to-top characterization parameter	31.8	
ψ_{JB}	Junction-to-board characterization parameter	58.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN1}	VIN supply current-1	T_A = 25°C, No load, V_{VO1} = 0 V		860		µA
I_{VIN2}	VIN supply current-2	T_A = 25°C, No load		30		µA
I_{VO1}	VO1 supply current	T_A = 25°C, No load, V_{VFB1} = V_{VFB2} = 2.05 V		900		µA
$I_{VIN(STBY)}$	VIN stand-by current	T_A = 25°C, No load, V_{VO1} = 0 V, V_{EN1}= V_{EN2} = 0 V		180		µA
INTERNAL REFERENCE						
V_{FBx}	VFB regulation voltage	T_A = 25°C	1.99	2	2.01	V
			1.98	2	2.02	
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, No load, V_{VO1} = 0 V	4.9	5	5.1	V
		V_{VIN} > 7 V , V_{VO1} = 0 V, I_{VREG5} < 100 mA	4.85	5	5.1	
		V_{VIN} > 5.5 V , V_{VO1} = 0 V, I_{VREG5} < 35 mA	4.85	5	5.1	
		V_{VIN} > 5 V, V_{VO1} = 0 V, I_{VREG5} < 20 mA	4.50	4.75	5.1	
I_{VREG5}	VREG5 current limit	V_{VO1} = 0 V, V_{VREG5} = 4.5 V, V_{VIN} = 7 V	100	150		mA
R_{V5SW}	5-V switch resistance	T_A = 25°C, V_{VO1} = 5 V, I_{VREG5} = 50 mA		1.8		Ω

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREG3 OUTPUT						
V_{VREG3}	VREG3 output voltage	No load, V_{VO1}= 0 V, T_A = 25°C	3.267	3.3	3.333	V
		V_{VIN} > 7 V , V_{VO1}= 0 V, I_{VREG3}< 100 mA	3.217	3.3	3.383	
		5.5 V < V_{VIN} , V_{VO1}= 0 V, I_{VREG3}< 35 mA	3.234	3.3	3.366	
		0°C ≤ T_A ≤ 85°C, V_{VIN} > 5.5 V, V_{VO1} = 0 V, I_{VREG3}< 35 mA	3.267	3.3	3.333	
		0°C ≤ T_A ≤ 85°C, V_{VIN} > 5.5 V, V_{VO1} = 5 V, I_{VREG3} < 35 mA	3.267	3.3	3.333	
		V_{VIN} > 5 V, V_{VO1} = 0 V, I_{VREG3}< 35 mA	3.217	3.3	3.366	
I_{VREG3}	VREG3 current limit	V_{VO1} = 0 V, V_{VREG3} = 3.0 V, V_{VIN}= 7 V	100	150		mA
MOSFET DRIVERS						
R_{DRVH}	DRVH resistance	Source, (V_{VBST} – V_{DRVH}) = 0.25 V, (V_{VBST} – V_{SW}) = 5 V		3		Ω
		Sink, (V_{DRVH} – V_{SW}) = 0.25 V, (V_{VBST} – V_{SW}) = 5 V		1.9		
R_{DRVL}	DRVL resistance	Source, (V_{VREG5} – V_{DRVL}) = 0.25 V, V_{VREG5} = 5 V		3		Ω
		Sink, V_{DRVL} = 0.25 V, V_{VREG5}= 5 V		0.9		
INTERNAL BOOT STRAP SWITCH						
$R_{VBST\ (ON)}$	Boost switch on-resistance	T_A = 25°C, I_{VBST} = 10 mA		13		Ω
I_{VBSTLK}	VBST leakage current	T_A = 25°C			1	µA
CLOCK OUTPUT						
$R_{VCLK\ (PU)}$	VCLK on-resistance (pullup)	T_A = 25°C		10		Ω
$R_{VCLK\ (PD)}$	VCLK on-resistance (pulldown)	T_A = 25°C		10		Ω
OUTPUT DISCHARGE						
R_{DIS1}	CH1 discharge resistance	T_A = 25°C, V_{VO1} = 0.5 V V_{EN1} = V_{EN2} = 0 V		35		Ω
R_{DIS2}	CH2 discharge resistance	T_A = 25°C, V_{SW2} = 0.5 V, V_{EN1} = V_{EN2} = 0 V		70		Ω
POWER GOOD						
V_{PGTH}	PG threshold	Lower (rising edge of PG-in)	92.5%	95.0%	97.5%	
		Hysteresis		5%		
		Upper (rising edge of PG-out)	107.5%	110.0%	112.5%	
		Hysteresis		5%		
I_{PGMAX}	PG sink current	V_{PGOOD} = 0.5 V		6.5		mA
I_{PGLK}	PG leakage current	V_{PGOOD} = 5.5 V			1	µA
CURRENT SENSING						
I_{CS}	CS source current	T_A = 25°C, V_{CS}= 0.4 V	9	10	11	µA
TC_{CS}	CS current temperature coefficient(1)	On the basis of 25°C		4500		ppm/°C
V_{CS}	CS current-limit setting range		0.2		2	V
V_{ZC}	Zero cross detection offset	T_A = 25°C	–1	1	3	mV
LOGIC THRESHOLD						
$V_{ENX(ON)}$	EN threshold high-level	SMPS on level			1.6	V
$V_{ENX(OFF)}$	EN threshold low-level	SMPS off level	0.3			V
I_{EN}	EN input current	V_{ENx}= 3.3 V	–1		1	µA
OUTPUT OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold		112.5%	115.0%	117.5%	
OUTPUT UNDERVOLTAGE PROTECTION						
V_{UVP}	UVP trip threshold		55%	60%	65%	

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
$V_{UVL0VIN}$	VIN UVLO threshold	Wake up		4.58		V
		Hysteresis		0.5		
V_{UVLO5}	VREG5 UVLO threshold	Wake up		4.38	4.5	V
		Hysteresis		0.4		
V_{UVLO3}	VREG3 UVLO threshold	Wake up		3.15		V
		Hysteresis		0.15		
OVERTEMPERATURE PROTECTION						
T_{OTP}	OTP threshold(1)	Shutdown temperature		155		°C
		Hysteresis		10		

7.6 Timing Requirements

over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
DUTY CYCLE AND FREQUENCY CONTROL						
f_{sw1}	CH1 frequency(1)	T_A = 25°C, V_{VIN}= 20 V	240	300	360	kHz
f_{SW2}	CH2 frequency(1)	T_A = 25°C, V_{VIN}= 20 V	280	355	430	kHz
$t_{OFF(MIN)}$	Minimum off-time	T_A = 25°C	200	300	500	ns
MOSFET DRIVERS						
t_D	Dead time	DRVH-off to DRVL-on		12		ns
		DRVL-off to DRVH-on		20		

(1) Ensured by design. Not production tested.

7.7 Switching Characteristics

over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK OUTPUT						
f_{CLK}	Clock frequency	T_A = 25°C		260		kHz
SOFT-START OPERATION						
t_{SS}	Soft-start time	From ENx = HI and V_{VREG5} > V_{UVLO5} to V_{OUT} = 95%		3.25		ms
t_{SSRAMP}	Soft-start time (ramp-up)	V_{OUT}= 0% to V_{OUT} = 95%, V_{VREG5} = 5 V		3.12		ms
POWER GOOD						
t_{PGDEL}	PG delay	From PG lower threshold (95% = typical) to PG flag high		1.38		ms
OUTPUT OVERVOLTAGE PROTECTION						
t_{OVPDLY}	OVP propagation delay	T_A = 25°C		0.5		µs
OUTPUT UNDERVOLTAGE PROTECTION						
t_{UVPDLY}	UVP propagation delay			250		µs
$t_{UVPENDLY}$	UVP enable delay	From ENx = HI and V_{VREG5} > V_{UVLO5} to UV latch off		4.3		ms

7.8 Typical Characteristics

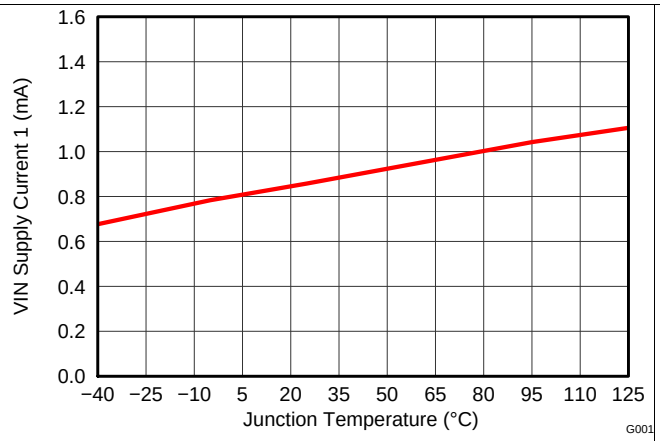


Figure 1. VIN Supply Current 1 vs Junction Temperature

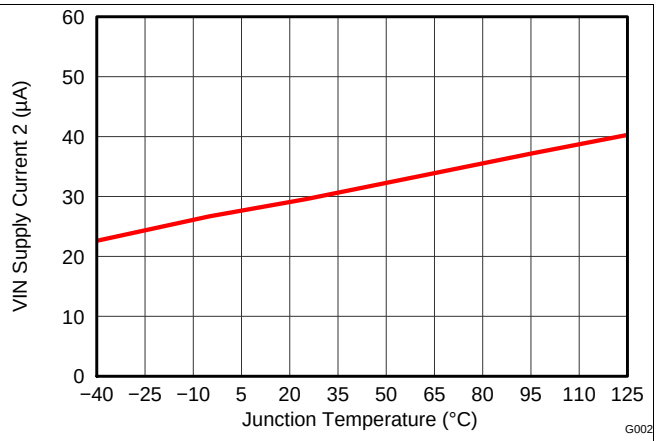


Figure 2. VIN Supply Current 2 vs Junction Temperature

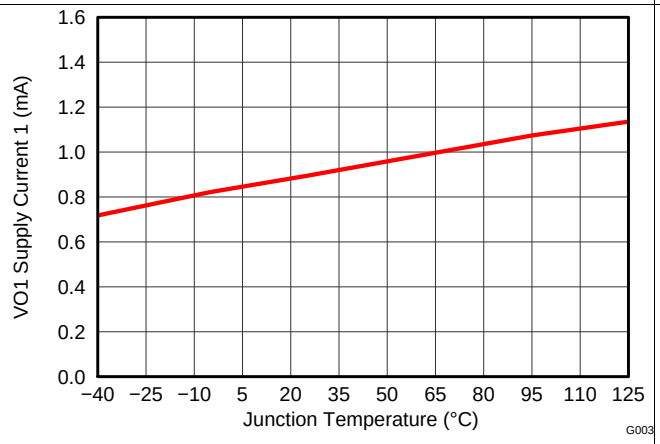


Figure 3. VO1 Supply Current 1 vs Junction Temperature

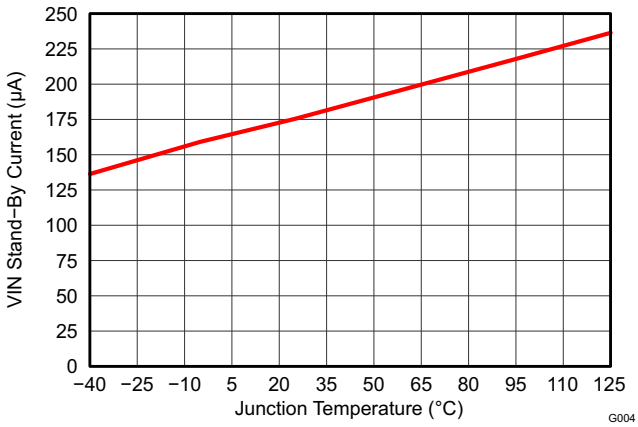


Figure 4. VIN Stand-By Current vs Junction Temperature

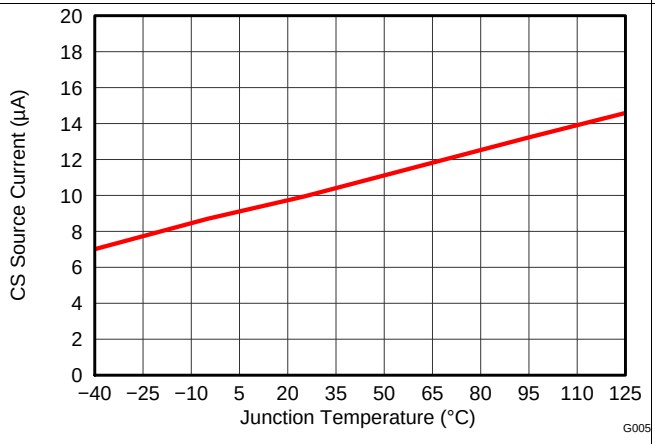


Figure 5. CS Source Current vs Junction Temperature

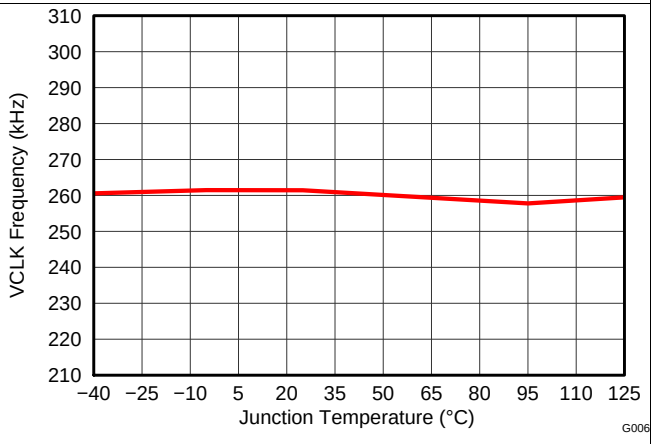


Figure 6. Clock Frequency vs Junction Temperature

Typical Characteristics (continued)

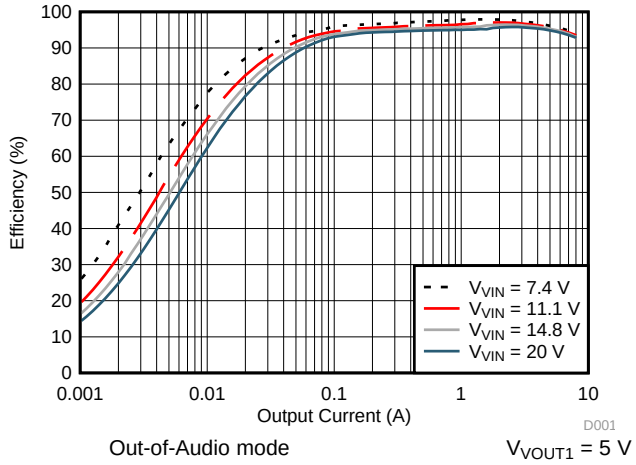


Figure 7. Efficiency vs Output Current

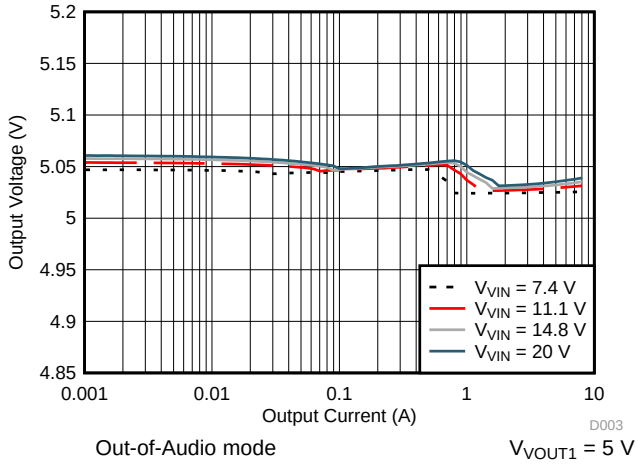


Figure 8. Load Regulation

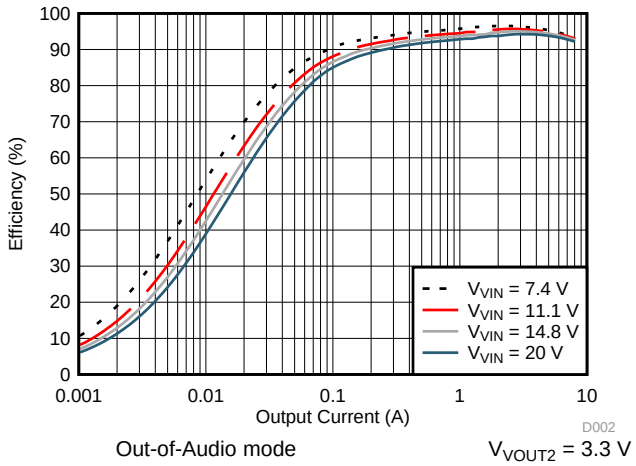


Figure 9. Efficiency vs Output Current

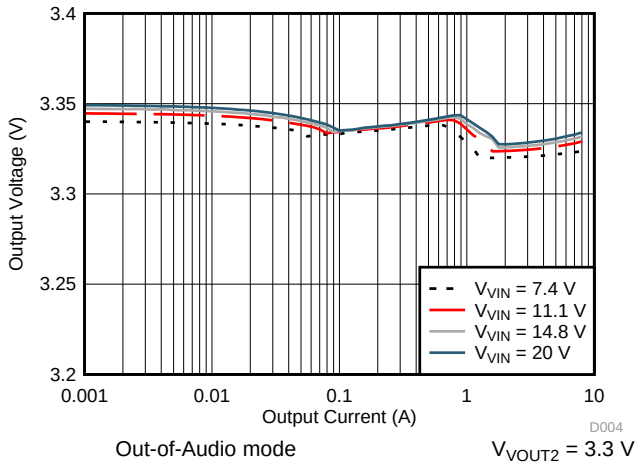


Figure 10. Load Regulation

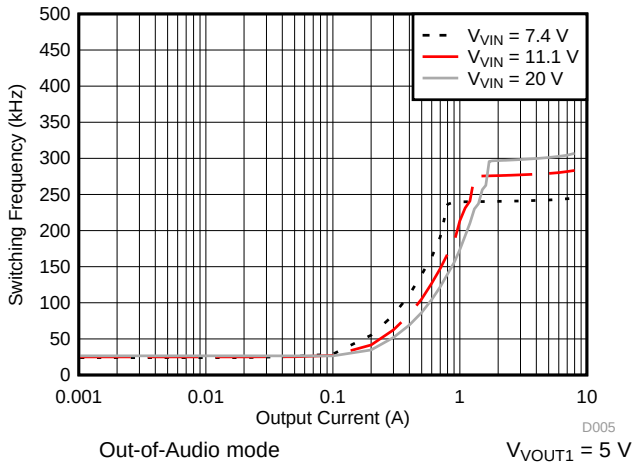


Figure 11. Switching Frequency vs Output Current

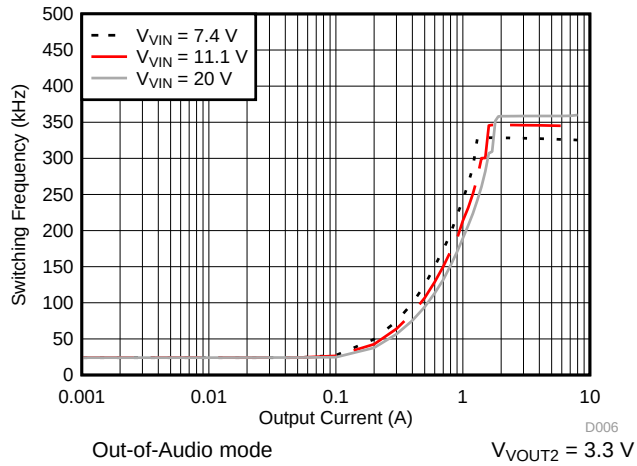
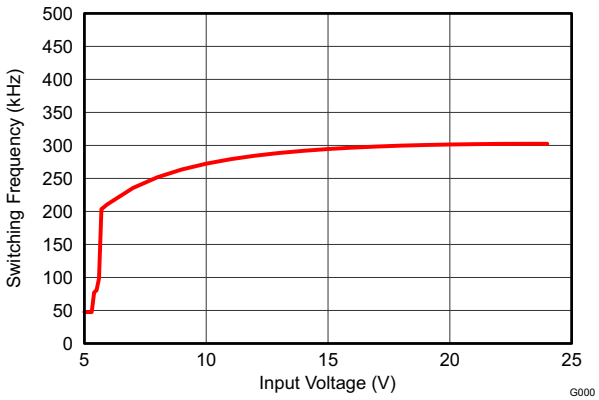


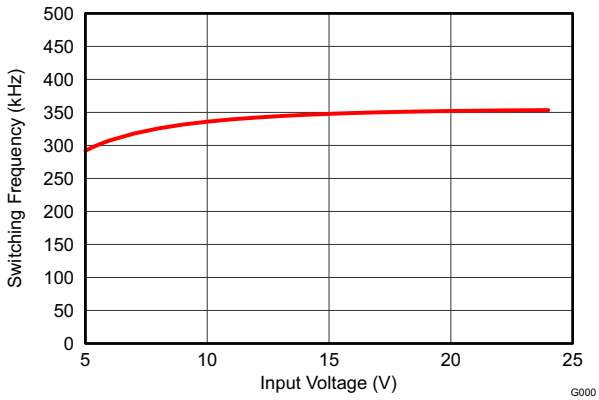
Figure 12. Switching Frequency vs Output Current

Typical Characteristics (continued)



V_{OUT1} = 5 V I_{OUT1} = 6 A

Figure 13. Switching Frequency vs Input Voltage



V_{OUT2} = 3.3 V I_{OUT2} = 6 A

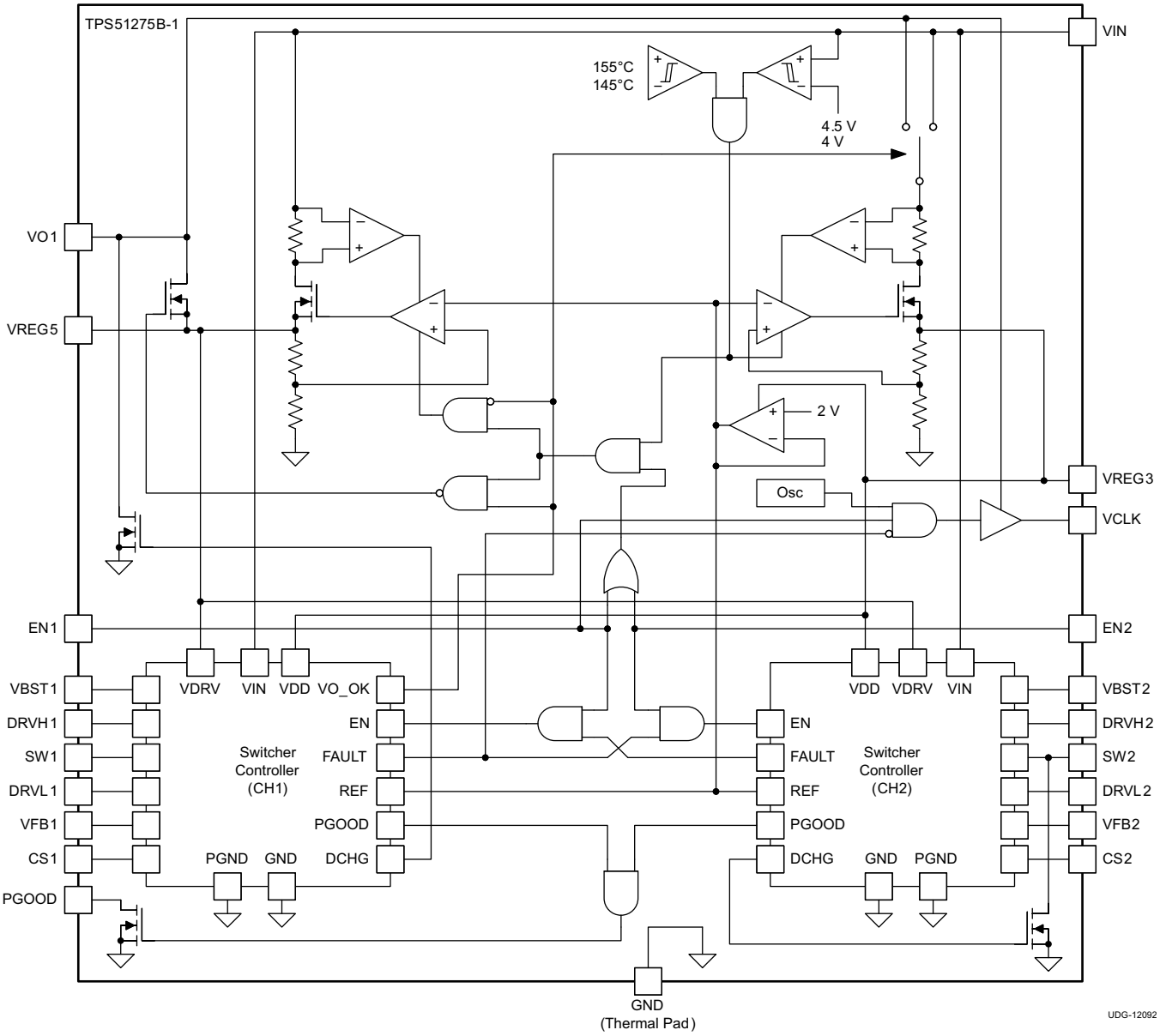
Figure 14. Switching Frequency vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS51275B-1 device is a cost-effective, dual-synchronous buck controller targeted for power-supply solutions for notebook and desktop computer systems. The device has 5-V and 3.3-V low-dropout regulators (LDOs) and requires few external components. With D-CAP control mode implemented, the compensation network can be removed. The fast transient response also reduces the output capacitance.

8.2 Functional Block Diagram



Functional Block Diagram (continued)

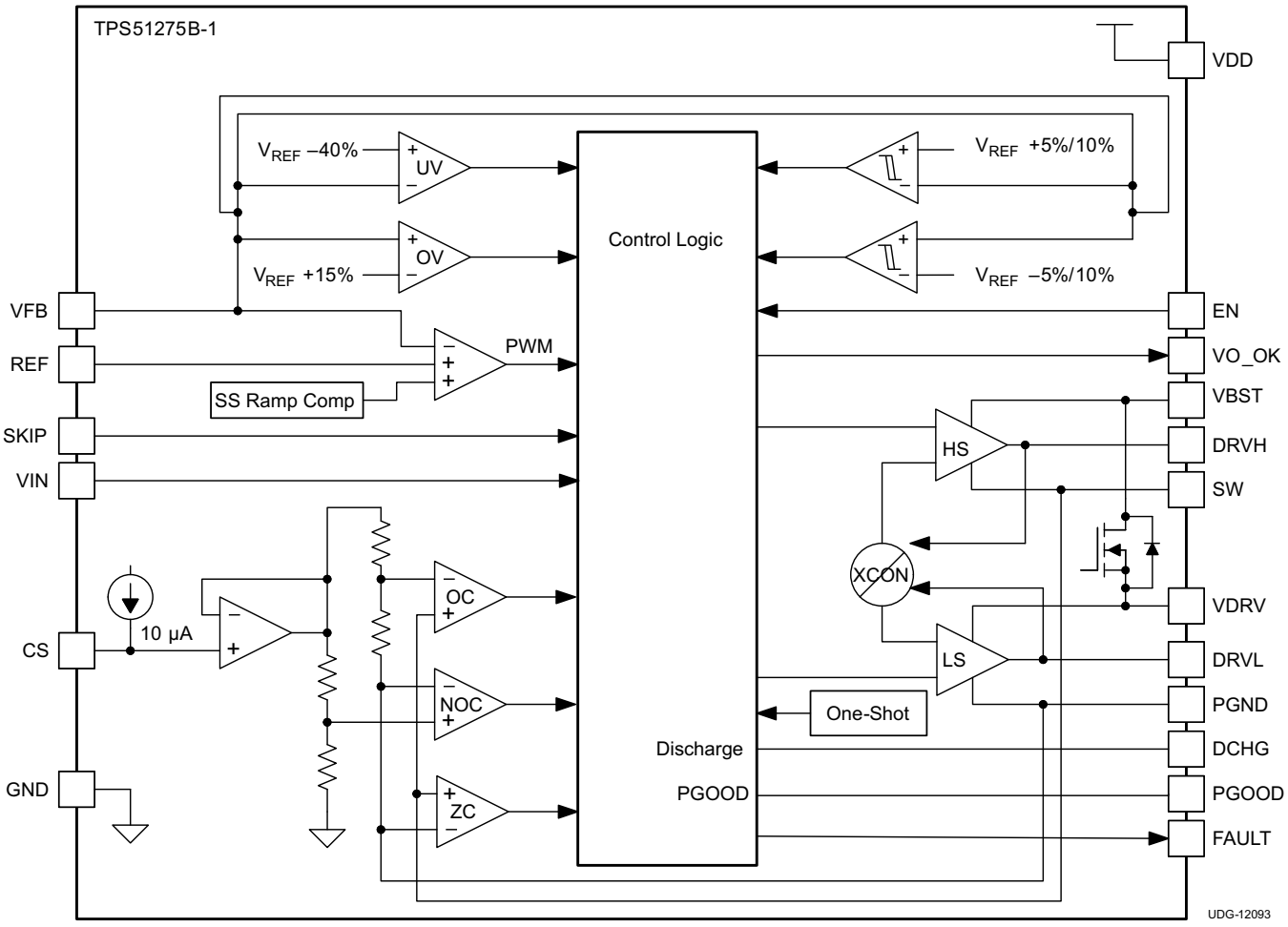


Figure 15. Switcher Controller Block Diagram

8.3 Feature Description

8.3.1 PWM Operations

The main control loop of the switch-mode power supply (SMPS) is designed as an adaptive on-time pulse-width-modulation (PWM) controller. The control loop supports a proprietary D-CAP mode. D-CAP mode does not require an external conpensation circuit and is suitable for low external component-count configuration when used with an appropriate amount of ESR at the output capacitors.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or enters the ON state. After the internal, one-shot timer expires, this MOSFET is turned off, or enters the OFF state. The MOSFET is turned on again when the feedback point voltage, V_{VFB}, decreases to match the internal 2-V reference. The inductor current information is also monitored and should be below the overcurrent threshold to initiate this new cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side (rectifying) MOSFET is turned on at the beginning of each OFF state to maintain a minimum of conduction loss. The low-side MOSFET is turned off before the high-side MOSFET turns on at next switching cycle or when inductor current information detects a zero level. When the low-side MOSFET is turned off when the inductor current detects a zero level, a seamless transition to the reduced frequency operation during light-load conditions is enabled so that high efficiency is maintained over a broad range of load current.

Feature Description (continued)

8.3.2 Adaptive On-Time and PWM Frequency Control

Because the TPS51275B-1 device does not have a dedicated oscillator for the on-board control loop. The switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The target switching frequency is varied according to the input voltage to achieve higher duty operation for lower input voltage application. The switching frequency of CH1 (5-V output) is 300 kHz during continuous-conduction-mode (CCM) operation when V_{VIN} = 20 V. The CH2 (3.3-V output) is 355 kHz during CCM when V_{VIN} = 20 V (see Figure 13 and Figure 14).

To improve load transient performance and load regulation in lower input voltage conditions, the TPS51275B-1 device can extend the on-time. The maximum on-time extension for CH1 is 4 times and for CH2 is 3 times. To maintain a reasonable inductor ripple current during on-time extension, the inductor ripple current should be set to less than half of the OCL (valley) threshold (see the *Step 2. Select the Inductor* section). The on-time extension function provides high duty-cycle operation and shows better DC (static) performance. AC performance is determined mostly by the output LC filter and resistive factor in the loop.

8.3.3 Light-Load Condition in Out-of-Audio Operation

The TPS51275B-1 device automatically reduces switching frequency during light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without an increase in output voltage ripple. A more detailed description of this operation follows. As the output current decreases from a heavy-load condition, the inductor current is also reduced and eventually approaches valley zero current, which is the boundary between continuous conduction mode and discontinuous conduction mode (DCM). The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs in DCM and requires a longer and longer time to discharge the output capacitor to the level that requires the next ON cycle. The ON time is maintained the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches to the continuous conduction. Use Equation 1 to calculate the transition load point to the light load operation $I_{OUT(LL)}$ (for example the threshold between continuous and discontinuous conduction mode).

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{VIN} - V_{OUT}) \times V_{OUT}}{V_{VIN}} \quad (1)$$

where

- f_{SW} is the PWM switching frequency

The switching frequency versus the output current during light-load conditions is a function of the inductance (L), input voltage (V_{VIN}) and output voltage (V_{OUT}), but it decreases almost proportional to the output current from the $I_{OUT(LL)}$. As the load current continues to decrease, the switching frequency can decrease into the acoustic audible frequency range. To prevent this from happening, Out-of-Audio (OOA) light-load mode is implemented.

During Out-of-Audio operation, the OOA control circuit monitors the states of both the high-side and low-side MOSFETs and forces them switching if both MOSFETs are off for more than 40 µs. When both high-side and low-side MOSFETs are off for 40 µs during a light-load condition, the operation mode is changed to forced CCM (FCCM). This mode change initiates one cycle of turning on both the low-side MOSFET and the high-side MOSFET. Then, both MOSFETs remain turned off waiting for another 40 µs.

8.3.4 Enable and Power Good

The VREG3 and VREG5 pins are always-on regulators, when the input voltage is beyond the UVLO threshold it turns ON. The VCLK signal initiates when the EN1 pin enters the ON state. Table 1 lists the enable states.

Table 1. Enabling and PGOOD State

EN1	EN2	VREG5	VREG3	CH1 (5 V_{OUT})	CH2 (3.3 V_{OUT})	VCLK	PGOOD
OFF	OFF	ON	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

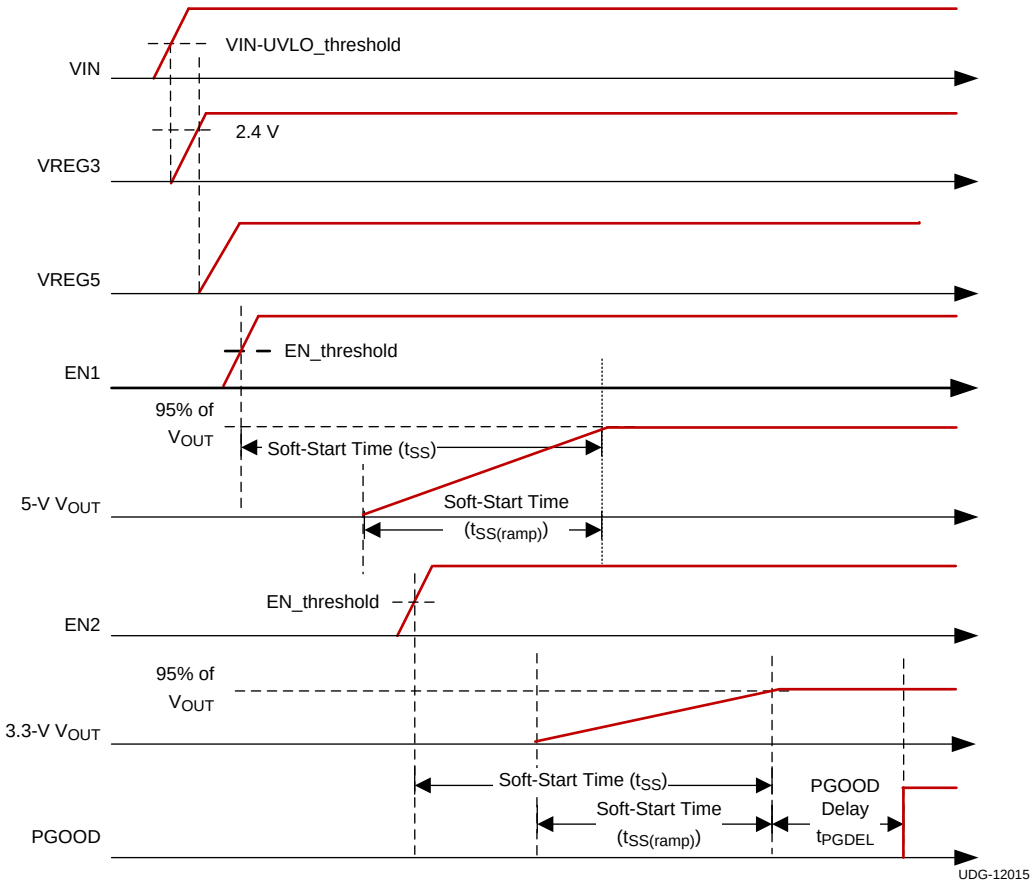


Figure 16. Timing Diagram

8.3.5 Soft-Start and Discharge

The TPS51275B-1 device operates an internal, 3.2-ms, voltage servo soft-start for each channel. When the ENx pin becomes higher than the enable threshold voltage, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during startup. When the ENx pin becomes lower than the lower level of threshold voltage, the TPS51275B-1 device discharges the outputs using internal MOSFETs through VO1 (CH1) and SW2 (CH2).

8.3.6 VREG5 and VREG3 Linear Regulators

The two sets of 100-mA standby linear regulators output 5 V and 3.3 V, respectively. The VREG5 pin provides the current for the gate drivers. The VREG3 pin functions as the main power supply for the analog circuitry of the device. Both the VREG5 and VREG3 regulators are always-ON LDOs (see Table 1).

To stabilize regulators, add ceramic capacitors with a value of 1 µF or larger (X5R grade or better) placed close to the VREG5 and VREG3 pins.

The VREG5 pin switchover function is asserted when the following three conditions are present:

- CH1 internal PGOOD is high
- CH1 is not in overcurrent-limit (OCL) condition
- VO1 voltage is higher than VREG5-1V

In this switchover condition the following three things occur:

- The internal 5-V LDO regulator is shut off
- The VREG5 output is connected to VO1 by internal switchover MOSFET
- VREG3 input pass is changed from VIN to VO1

8.3.7 VCLK for Charge Pump

The 260-kHz VCLK signal can be used in the charge pump circuit. The VCLK signal becomes available when the EN1 pin is in the ON state. The VCLK driver is driven by the VO1 voltage. In a design that does not require VCLK output, leave the VCLK pin open.

8.3.8 Overcurrent Protection

The TPS51275B-1 device has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the inductor current is larger than the overcurrent trip level. To provide both good accuracy and a cost effective solution, the TPS51275B-1 device supports temperature-compensated MOSFET $R_{DS(on)}$ sensing. Connect the CSx pin to ground (GND) through the CS voltage setting resistor, R_{CS}. The CSx pin sources CS current (I_{CS}) which is 10 µA typically at room temperature, and the CSx terminal voltage (V_{CS}= R_{CS} × I_{CS}) should be in the range of 0.2 to 2 V over all operation temperatures. The trip level is set to the OCL trip voltage (V_{TRIP}) as shown in Equation 2.

$$V_{TRIP} = \frac{R_{CS} \times I_{CS}}{8} + 1\,mV \tag{2}$$

The inductor current is monitored by the voltage between the GND and the SWx pin so that SWx pin is connected to the drain terminal of the low-side MOSFET properly. The CS pin current has a 4500 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the source terminal of the low-side MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in Equation 3.

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{VIN} - V_{OUT}) \times V_{OUT}}{V_{VIN}} \tag{3}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor and therefore the output voltage tends to fall down. Eventually, the output voltage ends up crossing the undervoltage protection threshold and both channels shut down.

8.3.9 Output Overvoltage and Undervoltage Protection

The TPS51275B-1 device asserts the overvoltage protection (OVP) when the VFBx voltage reaches the OVP-trip threshold level. When an OVP event is detected, the controller changes the output target voltage to 0 V which usually turns off the DRVHx pin and forces the DRVLx pin to turn on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, the DRVLx pin is turned off and the DRVHx pin is turned on. After the on-time expires, the DRVHx pin is turned off and the DRVLx pin is turned on again. This action minimizes the output node undershoot because of LC resonance. When the VFBx pin reaches 0 V, the driver output is latched as the DRVHx pin turns off, the DRVLx pin turns on. The undervoltage protection (UVP) latch is set when the VFBx voltage remains lower than UVP trip threshold voltage for 250 µs or longer. In this fault condition, the controller latches the DRVHx and DRVLx pins low and discharges the outputs. The UVP detection function is enabled after 4.3 ms of SMPS operation to ensure startup.

8.3.10 Undervoltage Lockout Protection

The TPS51275B-1 device has undervoltage lockout (UVLO) protection at the VIN, VREG5, and VREG3 pins. When each voltage is lower than the respective UVLO threshold voltage, both SMPSs are shut-off. The UNVLO is a non-latch protection.

8.3.11 Over-Temperature Protection (OTP)

The TPS51275B-1 device features an internal temperature monitor. If the temperature exceeds the threshold value (typically 155°C), the TPS51275B-1 device, including the regulators, shuts off. The OTP is anon-latch protection.

8.4 Device Functional Modes

8.4.1 D-CAP Mode

From small-signal loop analysis, a buck converter using D-CAP mode can be simplified as shown in Figure 17.

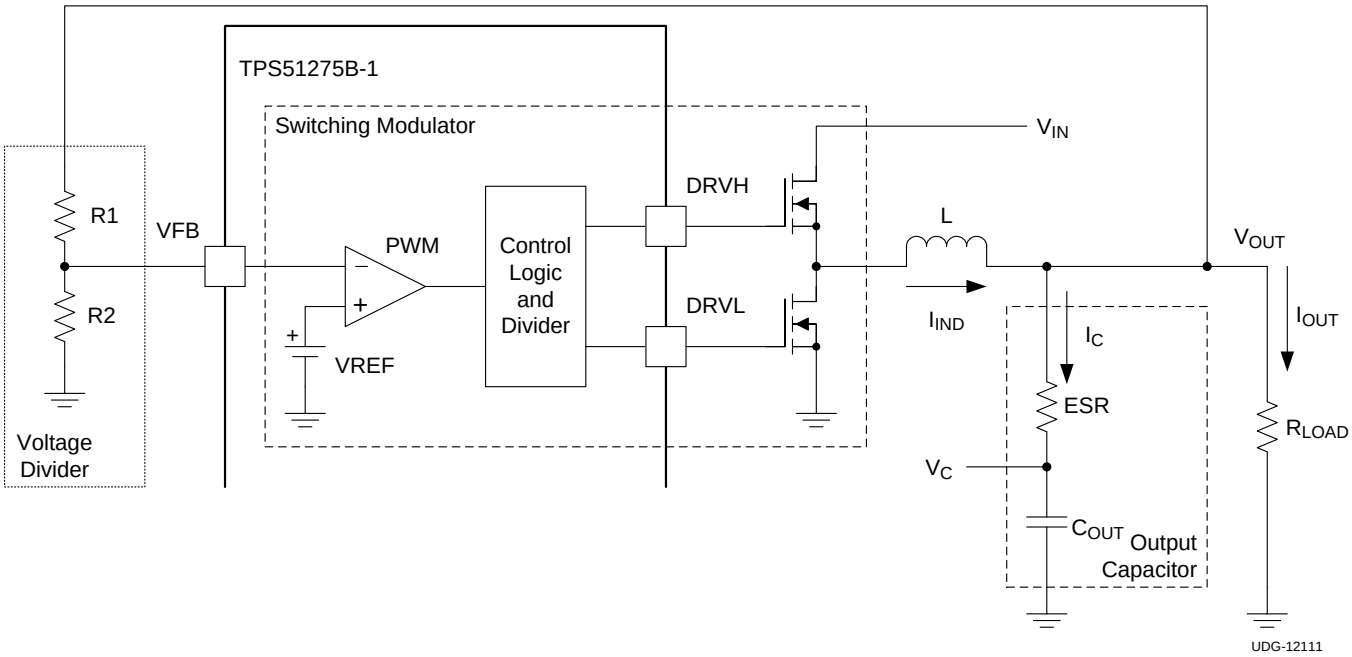


Figure 17. Simplifying the Modulator

The output voltage is compared with the internal reference voltage after the divider resistors, R1 and R2. The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each ON cycle substantially constant. For the loop stability, the 0-dB frequency, f_0, defined in Equation 4 must be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4} \tag{4}$$

As f_0 is determined solely by the output capacitor characteristics, the loop stability during D-CAP mode is determined by the capacitor chemistry. For example, specialty polymer capacitors have output capacitance in the order of several hundred micro-Farads and ESR in range of 10 mΩ. These capacitors yield an f_0 value on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS51275B-1 device is typically used as a dual-synchronous buck controller, which converts an input voltage ranging from 5 to 24 V, to output voltage of 5 V and 3.3 V (respectively). The device is targeted for power-supply solutions for notebook and desktop computer systems.

9.2 Typical Application

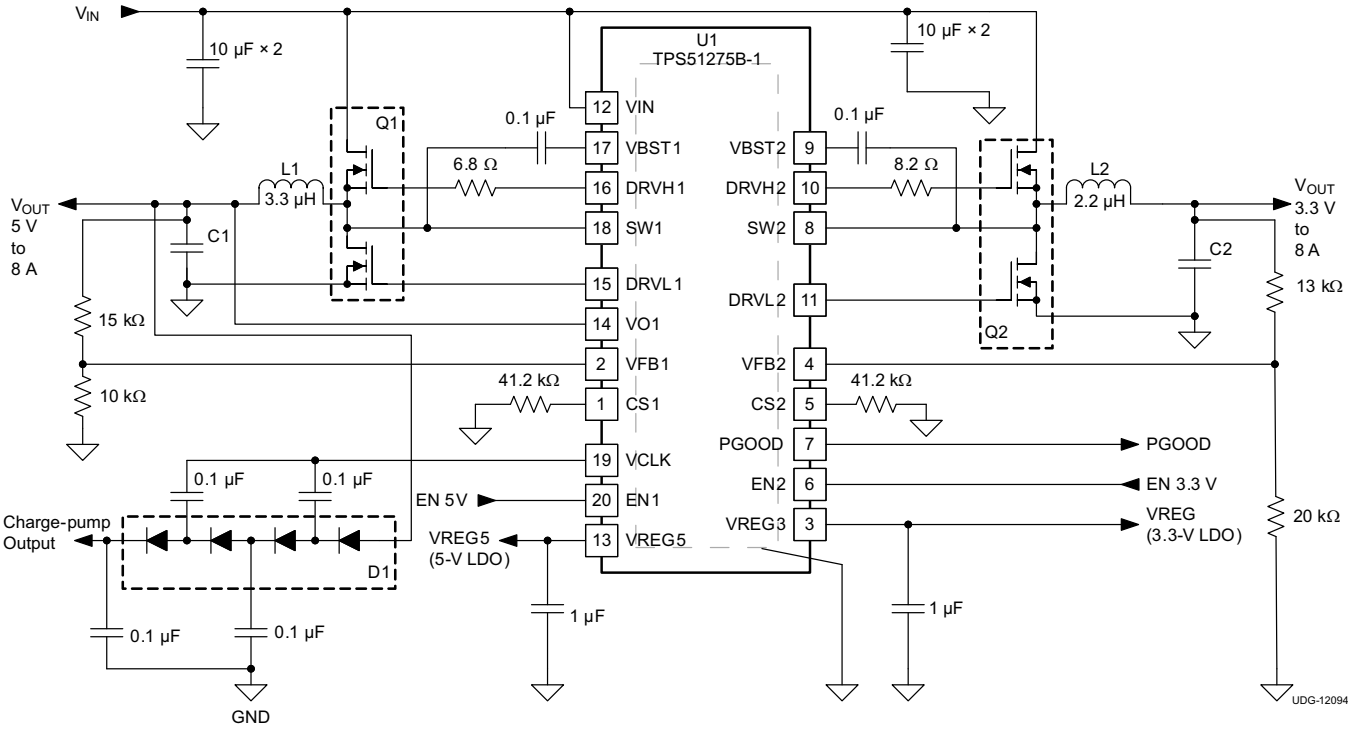


Figure 18. Detailed Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Input voltage range	5.5 to 24 V
Channel 1 output voltage	5 V
Channel 1 output voltage	8 A
Channel 2 output voltage	3.3 V
Channel 2 output voltage	8 A

9.2.2 Detailed Design Procedure

9.2.2.1 External Components Selection

The external components selection is relatively simple for a design using D-CAP mode. Table 3 lists the key external components that are recommended for this application design (see Figure 18).

Table 3. Key External Components

REFERENCE DESIGNATOR	FUNCTION	MANUFACTURER	PART NUMBER
L1	Output Inductor (5 V_{OUT})	Alps	GLMC3R303A
L2	Output Inductor (3.3 V_{OUT})	Alps	GLMC2R203A
C1	Output Capacitor (5 V_{OUT})	SANYO	6TPE220MAZB × 2
C2	Output Capacitor (3.3 V_{OUT})	SANYO	6TPE220MAZB × 2
Q1	MOSFET (5 V_{OUT})	TI	CSD87330Q3D
Q2	MOSFET (3.3 V_{OUT})	TI	CSD87330Q3D

9.2.2.1.1 Step 1. Determine the Value of R1 and R2

The recommended value of R2 is between 10 kΩ and 20 kΩ. Use Equation 5 to calculate the value of R1.

$$R1 = \frac{(V_{OUT} - 0.5 \times V_{RIPPLE} - 2)}{2} \times R2 \quad (5)$$

9.2.2.1.2 Step 2. Select the Inductor

The inductance value should be determined to give the ripple current of approximately ½ to ¼ of maximum output current and less than half of OCL (valley) threshold. A larger ripple current increases the output ripple voltage, improves signal-to-noise ratio, and helps ensure stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{(V_{VIN(max)} - V_{OUT}) \times V_{OUT}}{V_{VIN(max)}} = \frac{2}{I_{OUT(max)} \times f_{SW}} \times \frac{(V_{VIN(max)} - V_{OUT}) \times V_{OUT}}{V_{VIN(max)}} \quad (6)$$

The calculated inductance for channel1 and channel2 is 3.3 µH and 2 µH, respectively. For this design, select the inductance values of 3.3 µH and 2.2 µH for these two channels.

The inductor must also have low DCR to achieve good efficiency, as well as enough room above the peak inductor current before saturation. Use Equation 7 to calculate the peak inductor current.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{(V_{VIN(max)} - V_{OUT}) \times V_{OUT}}{V_{VIN(max)}} \quad (7)$$

9.2.2.1.3 Step 3. Select Output Capacitors

Organic semiconductor capacitors or specialty polymer capacitors are recommended. Determine the ESR to meet the required ripple voltage. Use Equation 8 to quickly calculate the ESR.

$$ESR = \frac{V_{OUT} \times 20\ mV \times (1 - D)}{2\ V \times I_{IND(ripple)}} = \frac{20\ mV \times L \times f_{SW}}{2\ V} \quad (8)$$

where

- D as the duty-cycle factor
- the required output ripple voltage slope is approximately 20 mV per t_{SW} (switching period) in terms of the VFBx pin

The calculated minimum-required ESR for channel1 and channel2 is 9.9 mΩ and 7.8 mΩ, respectively. For this design, use two 220-µF, 35-mΩ polymer capacitors in parallel for each channel. The equivalent ESR is 17.5 mΩ which meets the minimum ESR requirement. Using a value of 440 µF for the output capacitor and 17.5 mΩ of ESR, the resulting value of the 0-dB frequency, f_0 (see Equation 4), is approximately 21 kHz which is much less than f_{SW} / 4 for both channels.

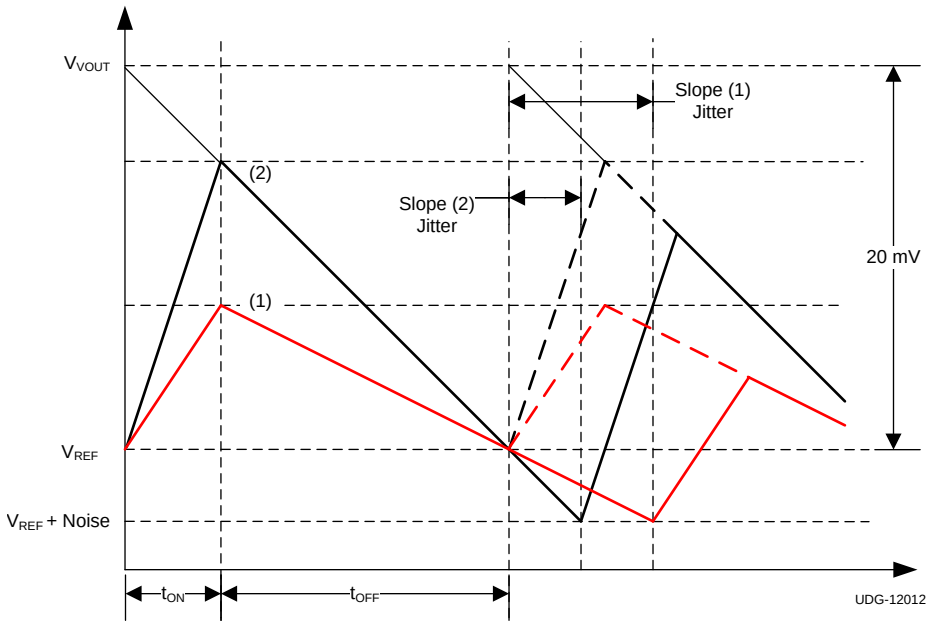


Figure 19. Ripple Voltage Slope and Jitter Performance

9.2.3 Application Curves

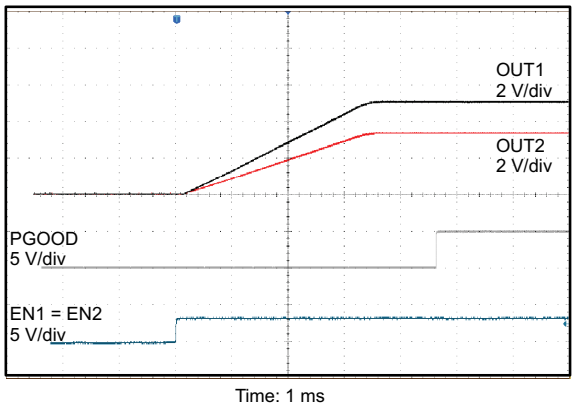


Figure 20. Startup

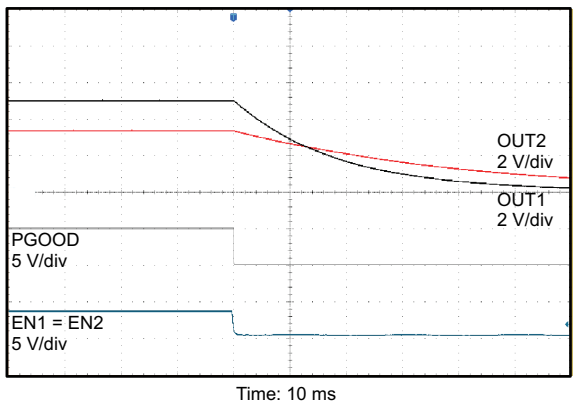
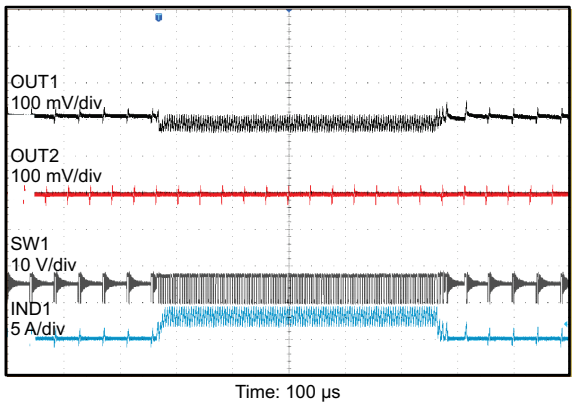
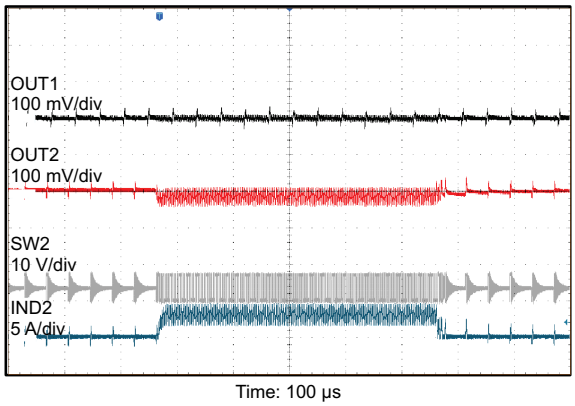


Figure 21. Shutdown



I_{OUT1} = 0 to 3 A I_{OUT2} = 0 A V_{VIN} = 7.4 V

Figure 22. 5-V Load Transient



I_{OUT1} = 0 A I_{OUT2} = 0 to 3 A V_{VIN} = 7.4 V

Figure 23. 3.3-V Load Transient

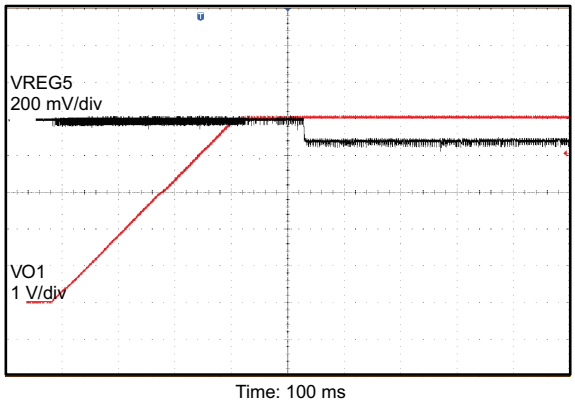


Figure 24. 5-V Switch Over

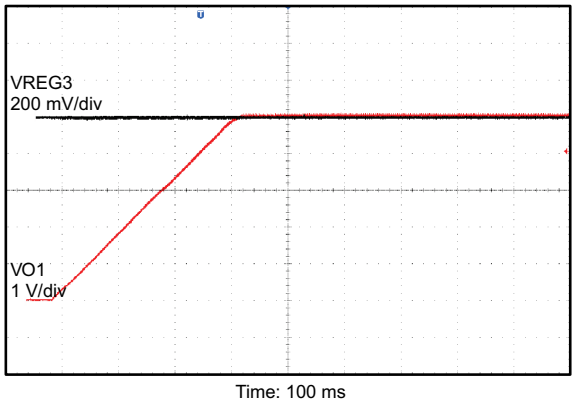


Figure 25. 3.3-V Switch Over

10 Power Supply Recommendations

The TPS51275B-1 device is designed to operate with an input supply-voltage range of 5 to 24 V. Ensure that the power-supply voltage in this range.

11 Layout

11.1 Layout Guidelines

Good layout is essential for stable power-supply operation. Follow these guidelines for an efficient PCB layout.

11.1.1 Placement

- Place voltage setting resistors close to the device pins.
- Place bypass capacitors for the VREG5 and VREG3 regulators close to the device pins.

11.1.2 Routing (Sensitive Analog Portion)

- Use small copper space for the VFBx pins. Short and narrow traces are available to avoid noise coupling.
- Connect the VFB resistor trace to the positive node of the output capacitor. Routing the inner layer away from power traces is recommended.
- Use short and wide trace from the VFB resistor to vias to GND (internal GND plane).

11.1.3 Routing (Power portion)

- Use wider and shorter traces of the DRVLx pin for the low-side gate drivers to reduce stray inductance.
- Use the parallel traces of the SWx and DRVHx pins for the high-side MOSFET gate drive in a same layer or on adjoin layers, and keep these traces away from the DRVLx pin.
- Use wider and shorter traces between the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET
- The thermal pad is the GND terminal of this device. Five or more vias with 0.33-mm (13-mils) diameter connected from the thermal pad to the internal GND plane should be used to have strong GND connection and help heat dissipation.

11.2 Layout Example

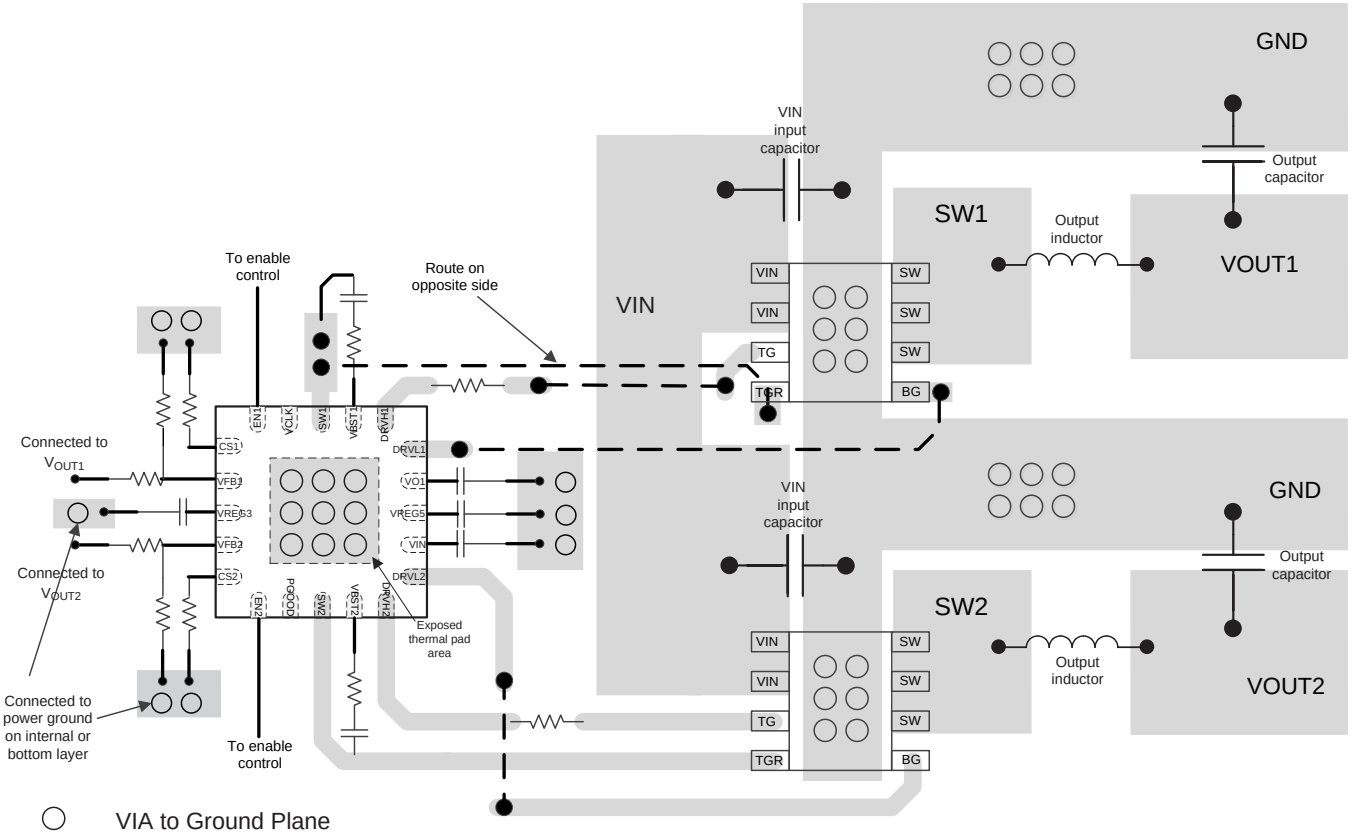


Figure 26. TPS51275B-Q1 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Trademarks

D-CAP, Out-of-Audio are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51275B-1RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1275B1	Samples
TPS51275B-1RUKT	ACTIVE	WQFN	RUK	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1275B1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

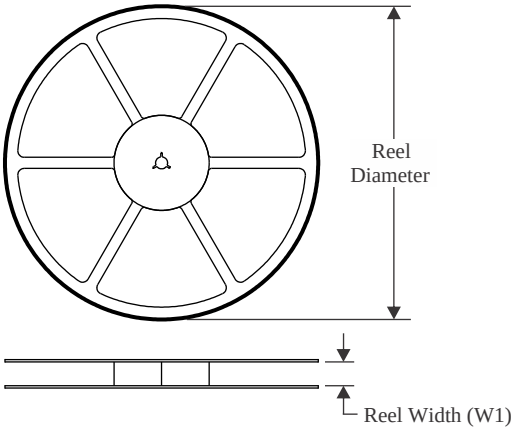
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

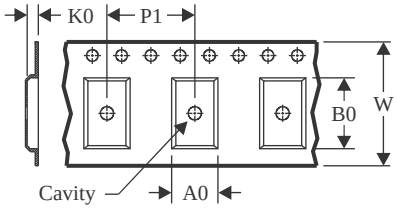
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

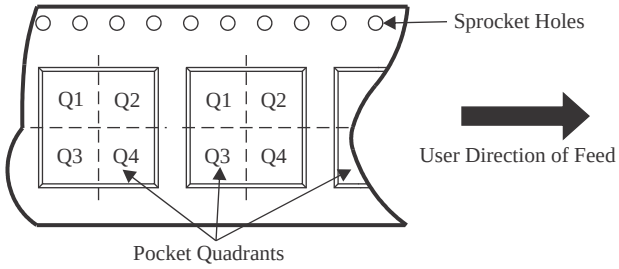


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

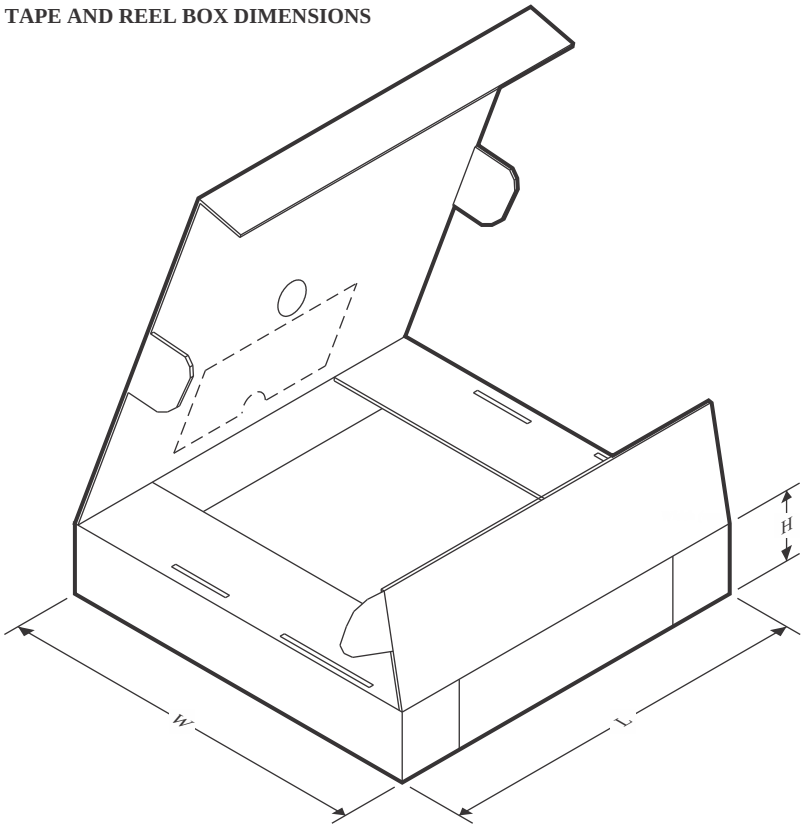
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51275B-1RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51275B-1RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51275B-1RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51275B-1RUKR	WQFN	RUK	20	3000	346.0	346.0	33.0
TPS51275B-1RUKT	WQFN	RUK	20	250	182.0	182.0	20.0
TPS51275B-1RUKT	WQFN	RUK	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

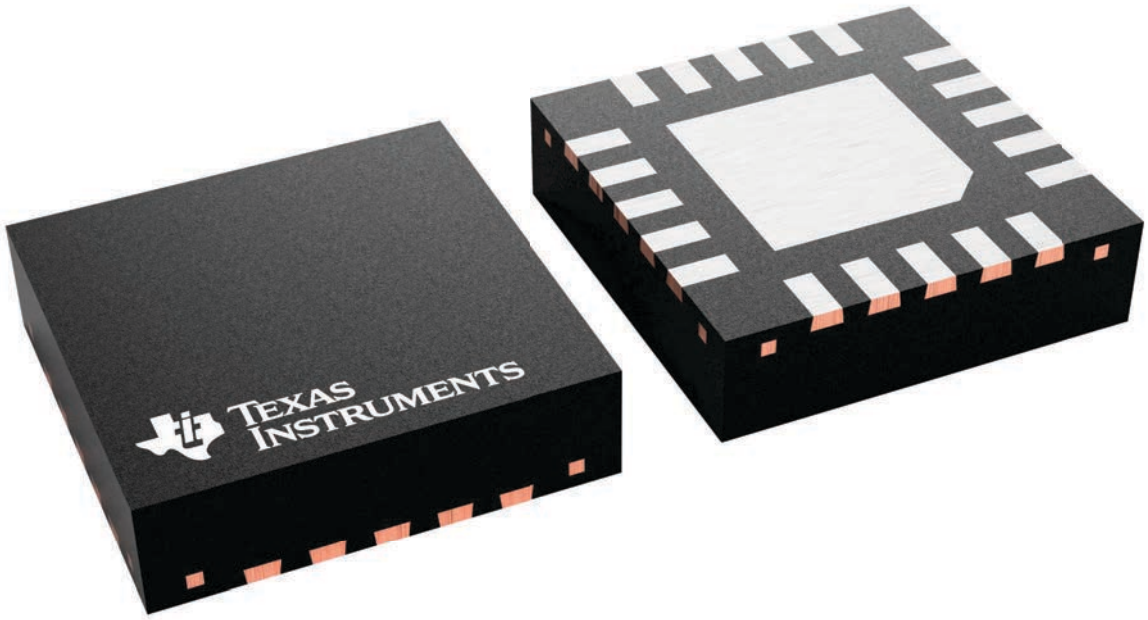
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



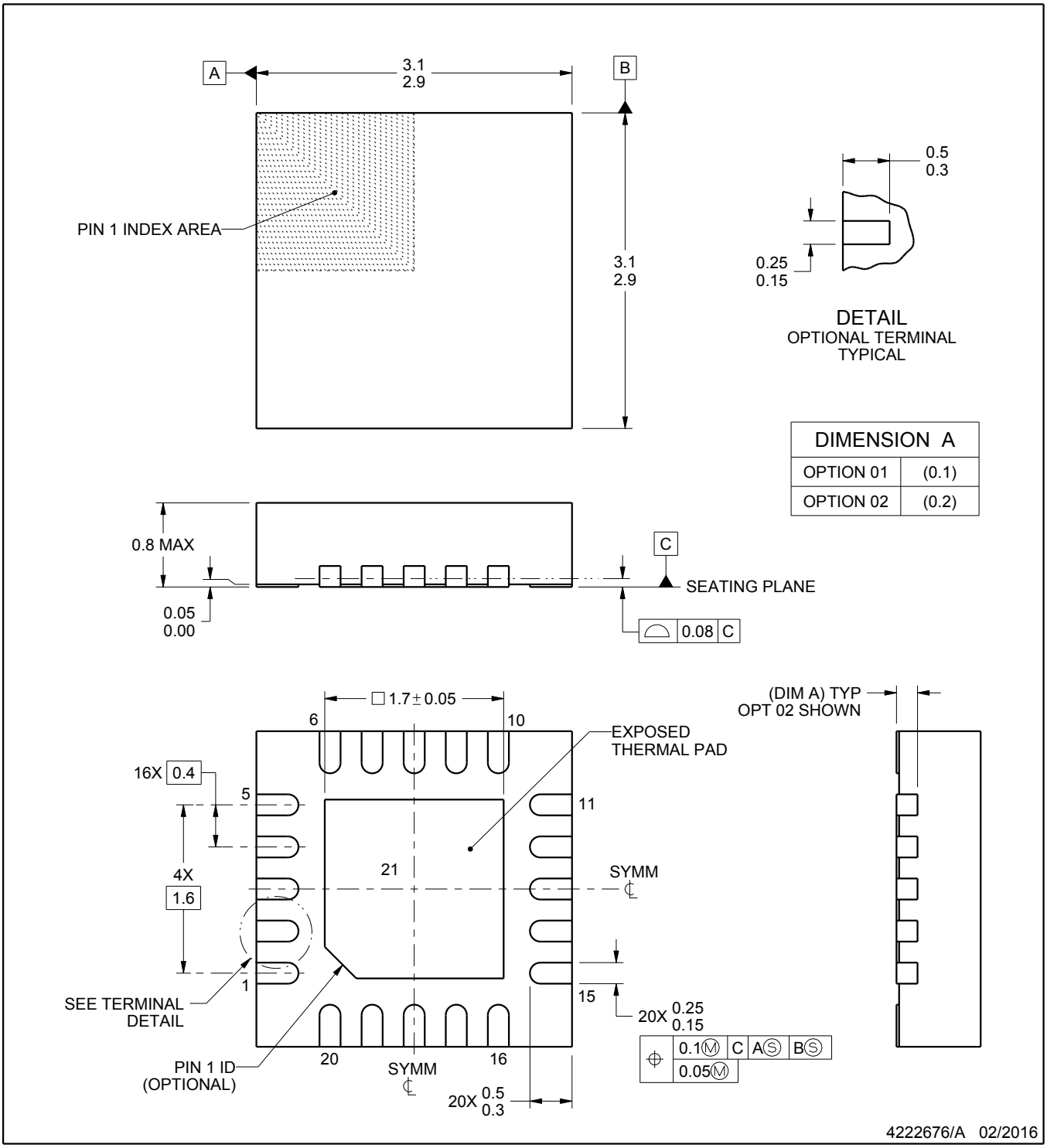
4229651/A

PACKAGE OUTLINE

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

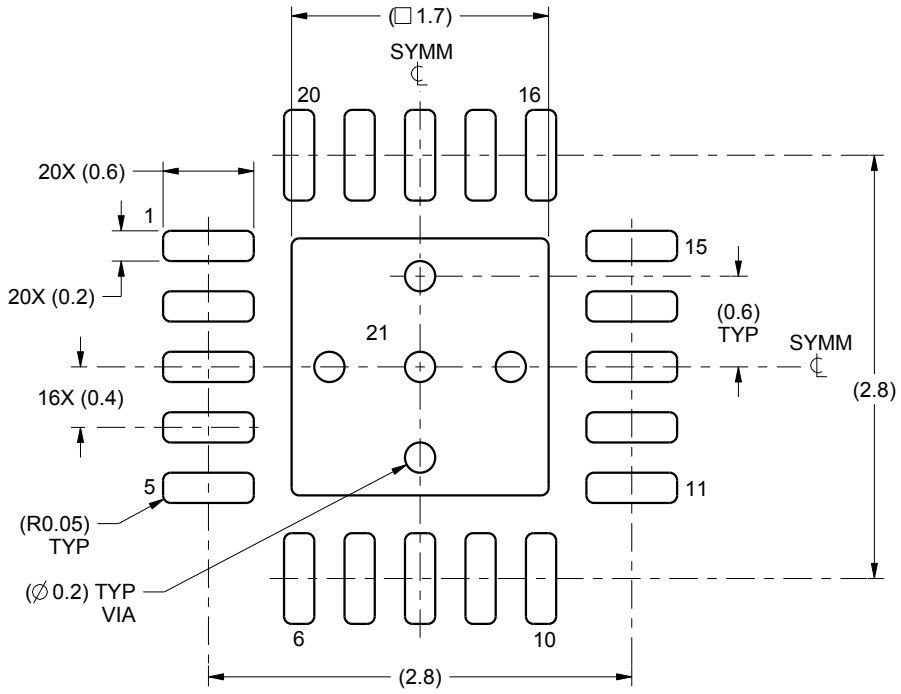
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

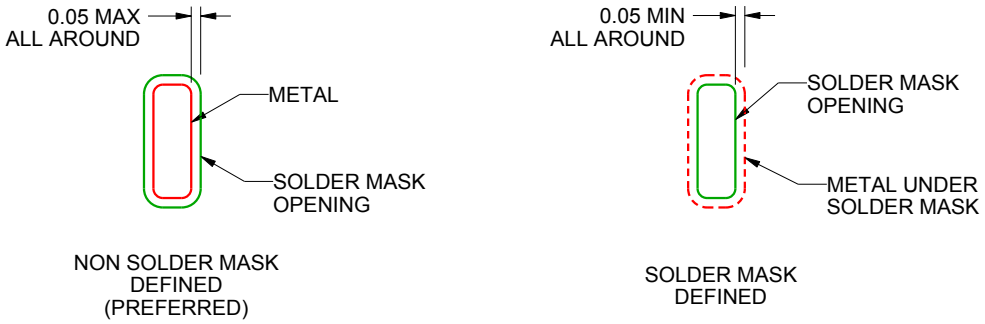
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X

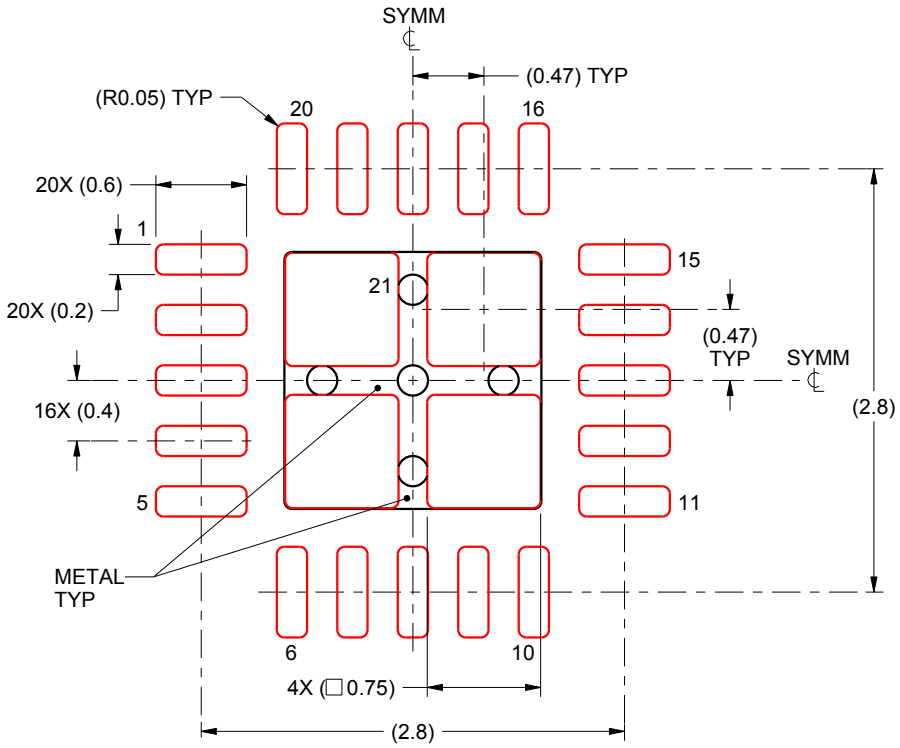


SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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