符合 RS-232 的 3V 至 5.5V 多通道线路驱动器和接收器

1 特性

- 由 3V 至 5.5V V_{CC} 电源供电
- 速率高达 1Mbit/s
- 低电源电流：300 µA（典型值）
- 外部电容器：4 × 0.1 µF
- 接受 5V 逻辑输入及 3.3V 电源
- RS-232 总线引脚 ESD 保护大于 ±15kV 人体放电模型 (HBM)

2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- 笔记本电脑
- 笔记本电脑
- 掌上电脑
- 手持设备

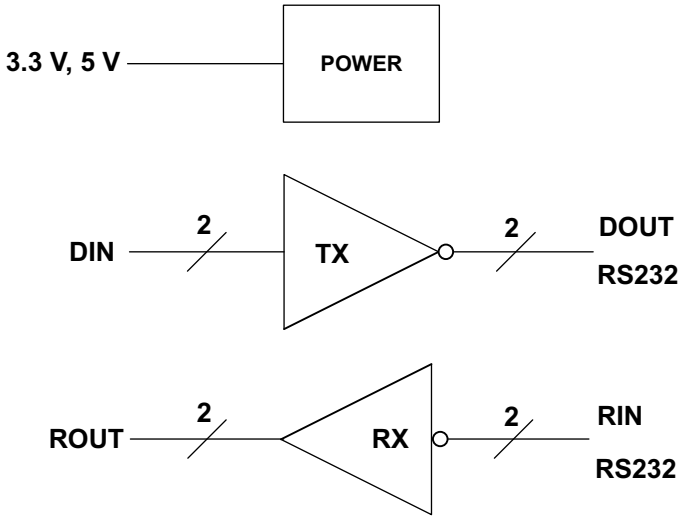
3 说明

SN65C3232 和 SN75C3232 由两个线路驱动器、两个线路接收器和一个双路电荷泵电路组成，具有引脚对引脚（串行端口连接引脚，包括 GND）±15kV ESD 保护。这些器件可在异步通信控制器和串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。该器件以高达 1Mbit/s 的典型数据信号传输速率运行，驱动器输出压摆率为 24V/µs 至 150V/µs。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN65C3232 SN75C3232	D (SOIC) (16)	9.90mm x 3.91mm
	DB (SSOP) (16)	6.20mm x 5.30mm
	DW (SOIC) (16)	10.3mm x 7.50mm
	PW (TSSOP) (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Downloaded From Oneyac.com

Table of Contents

1 特性.....1
2 应用.....1
3 说明.....1
4 Revision History.....2
5 Pin Configuration and Functions.....3
6 Specifications.....4
6.1 Absolute Maximum Ratings.....4
6.2 ESD Ratings.....4
6.3 Recommended Operating Conditions.....4
6.4 Thermal Information.....5
6.5 Electrical Characteristics.....5
6.6 Driver Section - Electrical Characteristics.....6
6.7 Switching Characteristics.....6
6.8 Receiver Section - Electrical Characteristics.....7
6.9 Switching Characteristics.....7
6.10 Typical Characteristics.....8
7 Parameter Measurement Information.....9
8 Detailed Description.....10
8.1 Overview.....10
8.2 Functional Block Diagram.....10
8.3 Feature Description.....10
8.4 Device Functional Modes.....11
9 Application and Implementation.....12
9.1 Application Information.....12
10 Layout.....14
10.1 Layout Guidelines.....14
10.2 Layout Example.....14
11 Device and Documentation Support.....15
11.1 Documentation Support.....15
11.2 接收文档更新通知.....15
11.3 支持资源.....15
11.4 Trademarks.....15
11.5 Electrostatic Discharge Caution.....15
11.6 Glossary.....15
12 Mechanical, Packaging, and Orderable Information.....15

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (November 2004) to Revision C (June 2021)	Page
• 添加了*器件信息*表、*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• 添加了*应用*工业 PC、有线网络、数据中心和企业级计算	1
• Added thermal parameter values for all packages and changed the thermal parameters for D package in the *Thermal Information* table	5

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

5 Pin Configuration and Functions

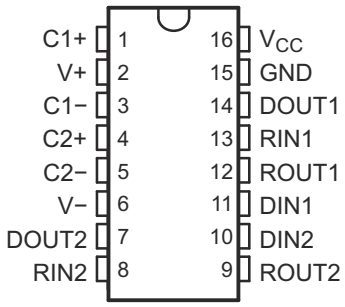


图 5-1. D, DW, DB and PW Package, 16-Pin SOIC, SSOP and TSSOP, Top View

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V+	2	O	Positive charge pump output for storage capacitor only
C1 –	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2 –	5	—	Negative lead of C2 capacitor
V –	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 3-V to 5.5-V power supply

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive-output supply voltage range(2)		–0.3	7	V
V–	Negative-output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Drivers	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute MaximumRatings do not imply functional operation of the device at these or any other conditions beyond those listed underRecommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except RIN and DOUT	±3000	V
			RIN and DOUT Pins	±15,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See 图 9-1, See (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver low-level input voltage	DIN				0.8	V
V_I	Driver input voltage	DIN		0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature		SN75C3232	0		70	°C
			SN65C3232	–40		85	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

6.4 Thermal Information

THERMAL METRIC(1)		SN65C3232, SN75C3232				UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.0	85.9	57.0	46.0	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	20.8	43.1	33.5	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	44.5	37.1	43.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	10.1	7.5	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.1	44.1	37.1	42.9	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	–	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1)

PARAMETER(2)		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

6.6 Driver Section - Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1)

PARAMETER		TEST CONDITIONS(3)		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	μA
I_{OS}	Short-circuit output current(2)	V_O = 0 V	V_{CC} = 3.6 V		±35	±60	mA
			V_{CC} = 5.5 V		±35	±90	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.7 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1)

PARAMETER		TEST CONDITIONS(3)			MIN	TYP(1)	MAX	UNIT
	Maximum data rate (see 图 7-1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew(2)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ,	See 图 7-2		300		ns
SR(tr)	Slew rate, transition region (see 图 7-1)	R_L = 3 kΩ to 7 kΩ,	C_L = 150 pF to 1000 pF,	V_{CC} = 3.3 V	18		150	V/μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

6.8 Receiver Section - Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.3		V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.9 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1)

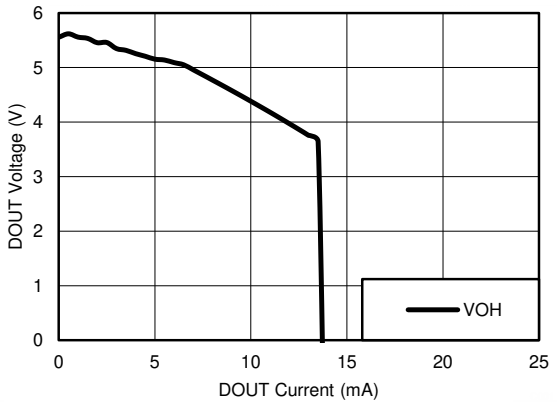
PARAMETER		TEST CONDITIONS(3)	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF	300	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF	300	ns
$t_{sk(p)}$	Pulse skew(2)		300	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

Copyright © 2021 Texas Instruments Incorporated

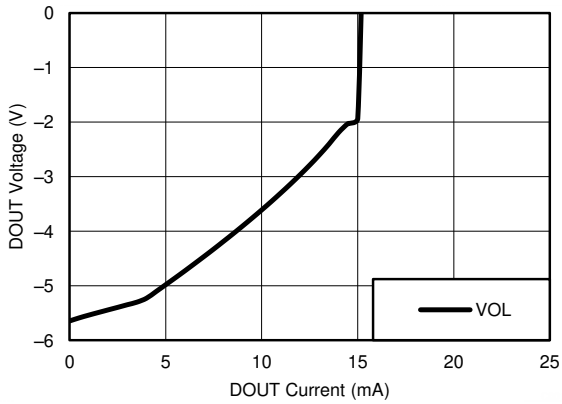
Downloaded From Oneyac.com

6.10 Typical Characteristics



V_{CC} = 3.3 V

图 6-1. DOUT V_{OH} vs Load Current, Both Drivers Loaded



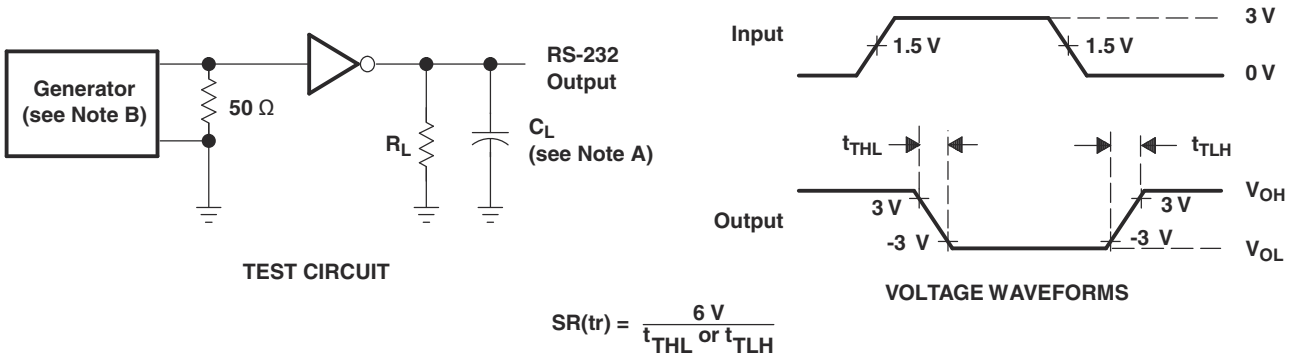
V_{CC} = 3.3 V

图 6-2. DOUT V_{OL} vs Load Current, Both Drivers Loaded

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

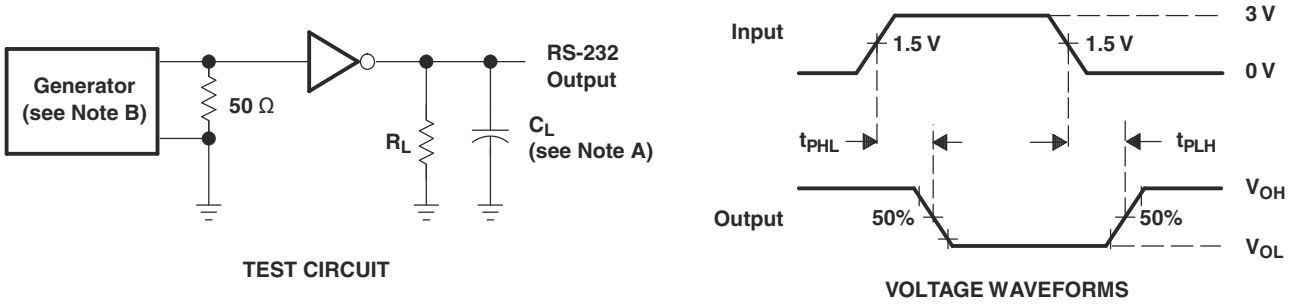
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

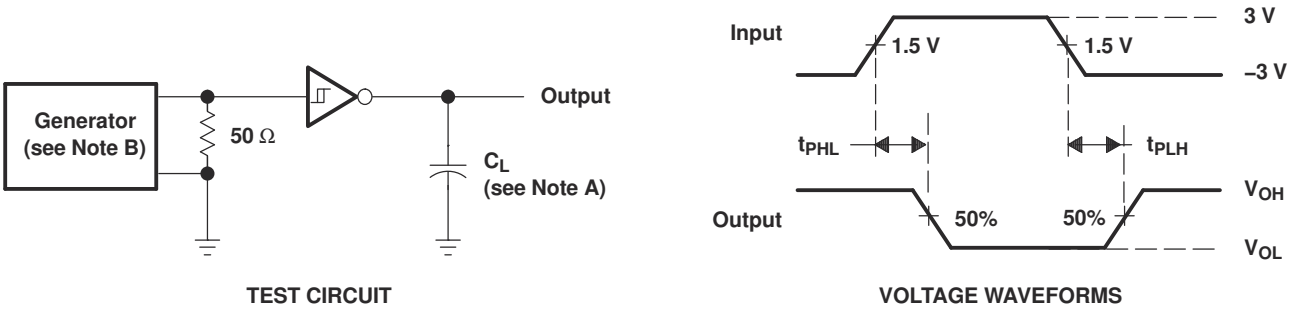
图 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

图 7-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

图 7-3. Receiver Propagation Delay Times

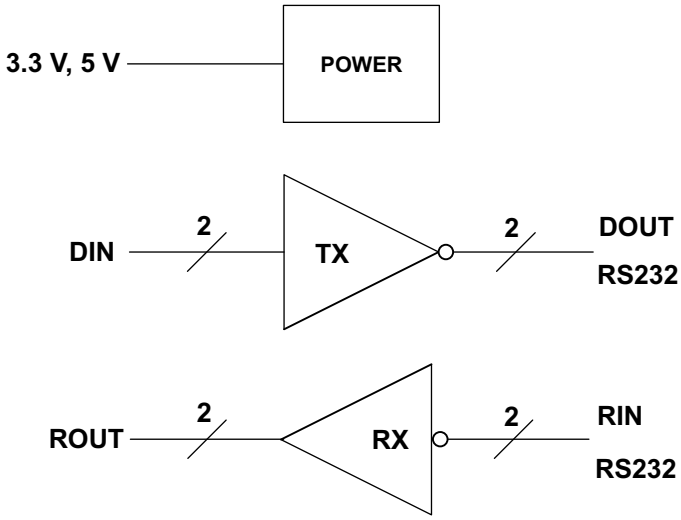
Downloaded From Oneyac.com

8 Detailed Description

8.1 Overview

The devices consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V – pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

8.4 Device Functional Modes

表 8-1 and 表 8-2 list the functional modes of the drivers and receivers of MAX3232E.

表 8-1. Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 8-2. Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

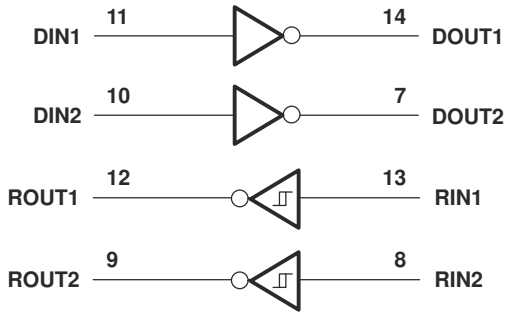


图 8-1. Logic Diagram

8.4.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered, V_{CC} = 0 V

When the device is unpowered, it can be safely connected to an active remote RS232 device.

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

9 Application and Implementation

Note

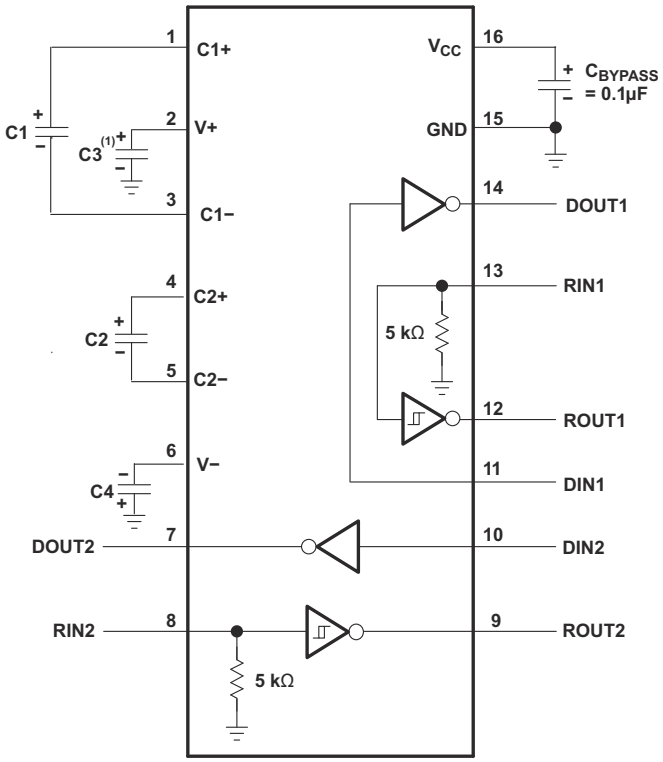
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

For proper operation, add capacitors as shown in 表 9-1.

9.1.1 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



A. C3 can be connected to V_{CC} or GND

A. Resistor values shown are nominal.

B. Nonpolorized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

图 9-1. Typical Operating Circuit and Capacitor Values

表 9-1. VCC vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

9.1.1.1 Design Requirements

The recommended V_{CC} is 3.3 V or 5 V. 3 V to 5.5 V is also possible

The maximum recommended bit rate is 250 kbit/s.

9.1.1.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.1.1.3 Application Performance Plots

图 9-2 curves are for 3.3-V VCC and 250-kbit/s alternative bit data stream.

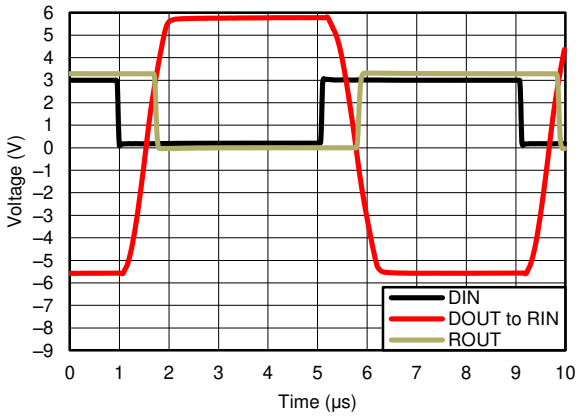


图 9-2. 250 kbit/s Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

Downloaded From Oneyac.com

10 Layout

10.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

10.2 Layout Example

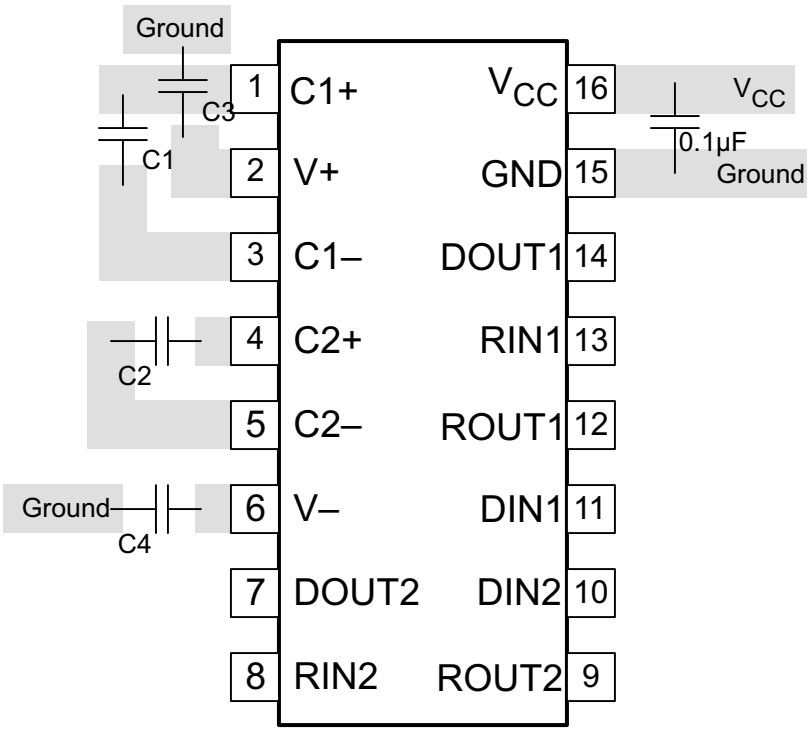


图 10-1. Layout Diagram

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2021 Texas Instruments Incorporated

Downloaded From Oneyac.com

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021，德州仪器 (TI) 公司

Downloaded From Oneyac.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C3232DBR	LIFEBUY	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232	
SN65C3232DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232	Samples
SN65C3232DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232	
SN65C3232DWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3232	
SN65C3232PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3232	Samples
SN75C3232DBR	LIFEBUY	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3232	
SN75C3232DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232	Samples
SN75C3232DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232	
SN75C3232DWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3232	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Downloaded From Oneyac.com

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

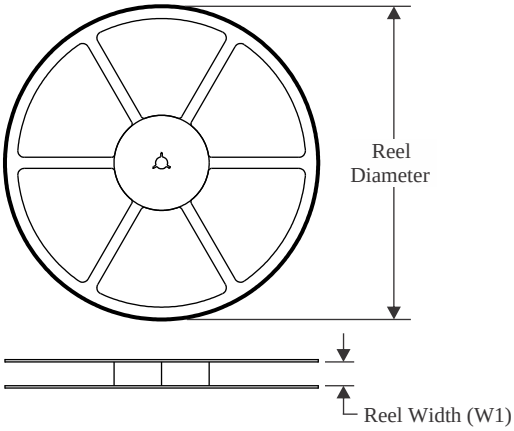
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

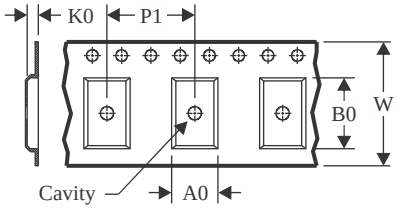
Downloaded From Oneyac.com

TAPE AND REEL INFORMATION

REEL DIMENSIONS

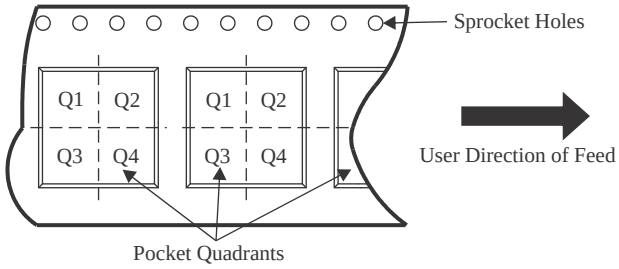


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

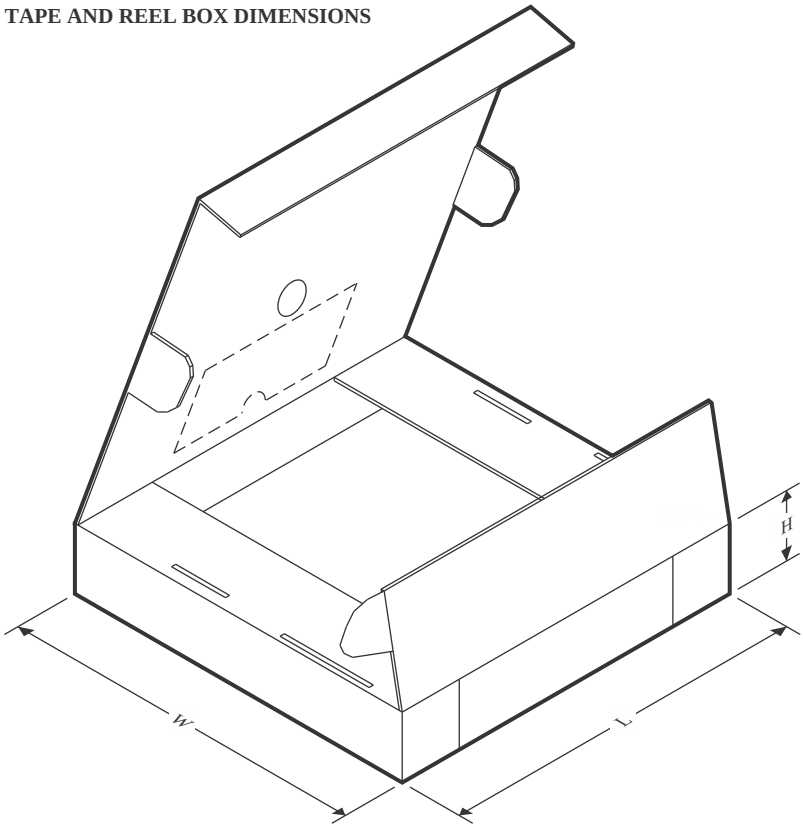


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3232DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN65C3232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65C3232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65C3232PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3232PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C3232DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C3232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75C3232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

Downloaded From Oneyac.com

TAPE AND REEL BOX DIMENSIONS

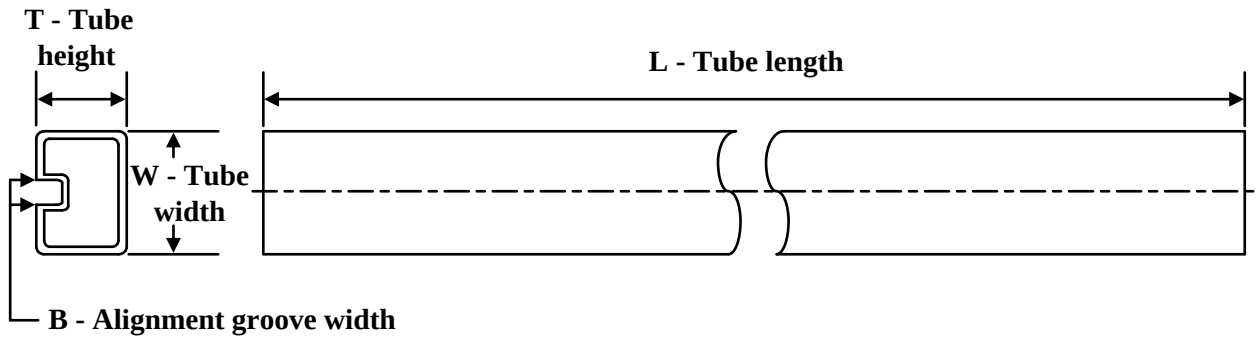


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3232DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN65C3232DR	SOIC	D	16	2500	356.0	356.0	35.0
SN65C3232DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN65C3232PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN65C3232PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN75C3232DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN75C3232DR	SOIC	D	16	2500	356.0	356.0	35.0
SN75C3232DWR	SOIC	DW	16	2000	350.0	350.0	43.0

Downloaded From Oneyac.com

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65C3232DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN75C3232DW	DW	SOIC	16	40	506.98	12.7	4826	6.6

Downloaded From Oneyac.com

GENERIC PACKAGE VIEW

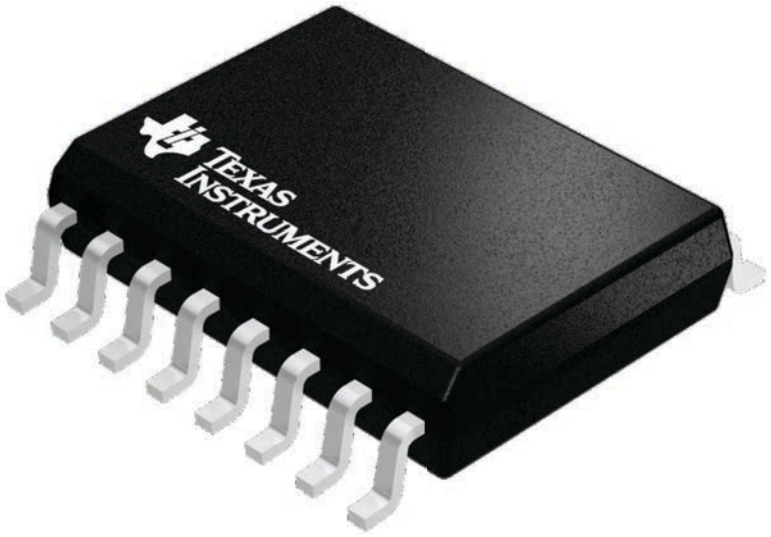
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

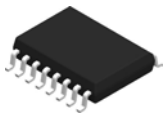
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

TEXAS INSTRUMENTS

Downloaded From Oneyac.com

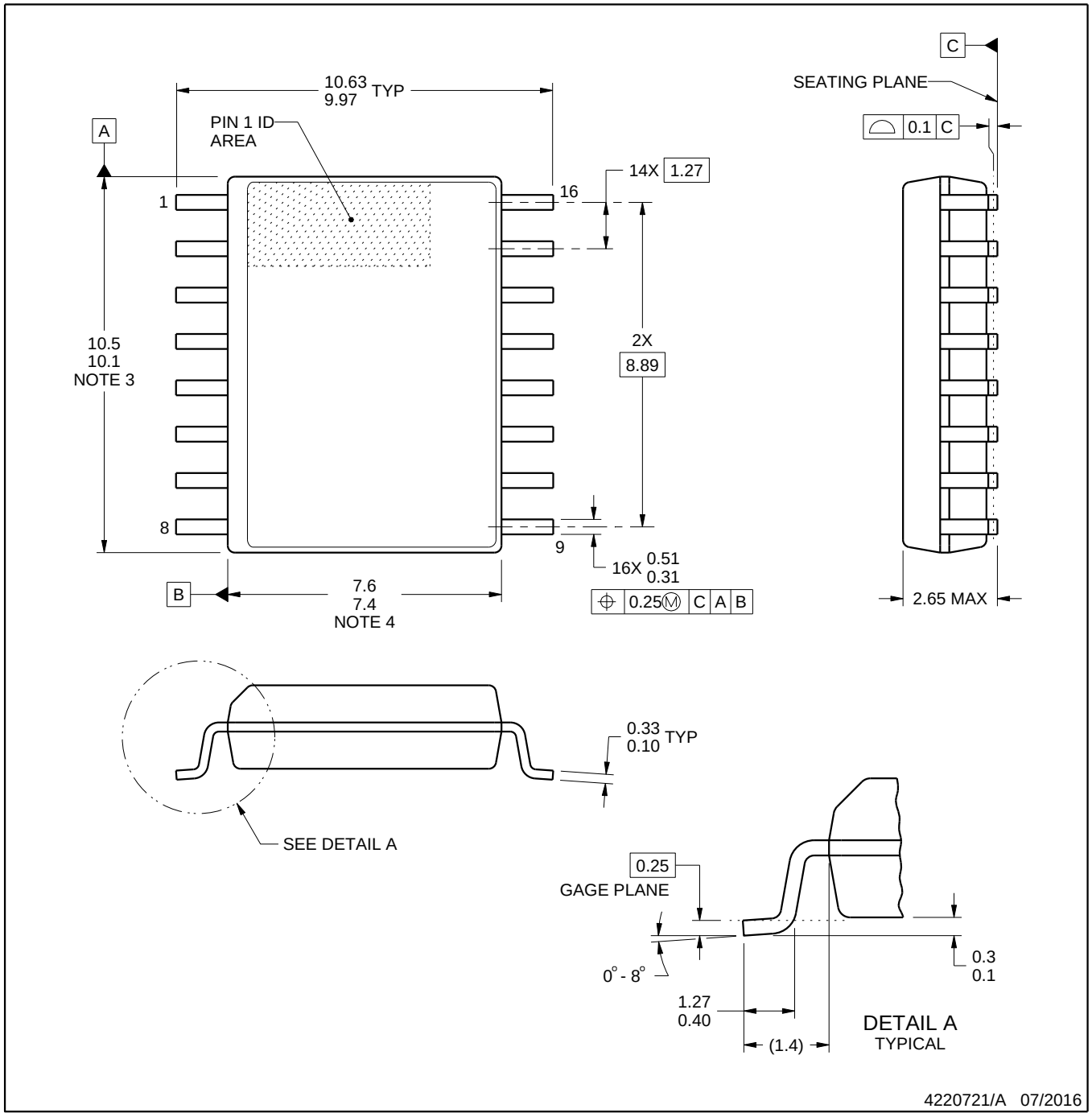


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

Texas Instruments

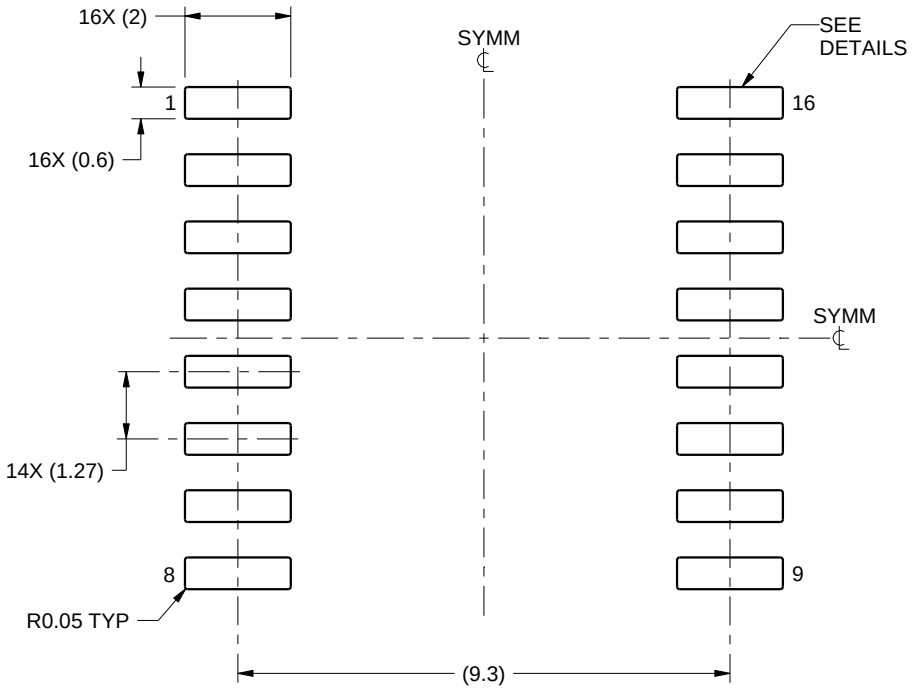
Downloaded From Oneyac.com

EXAMPLE BOARD LAYOUT

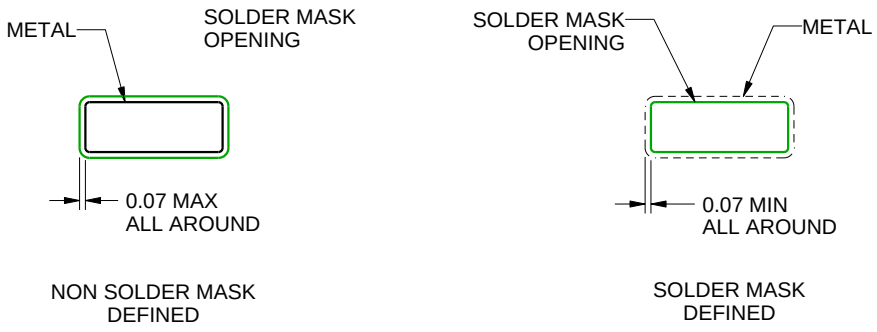
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



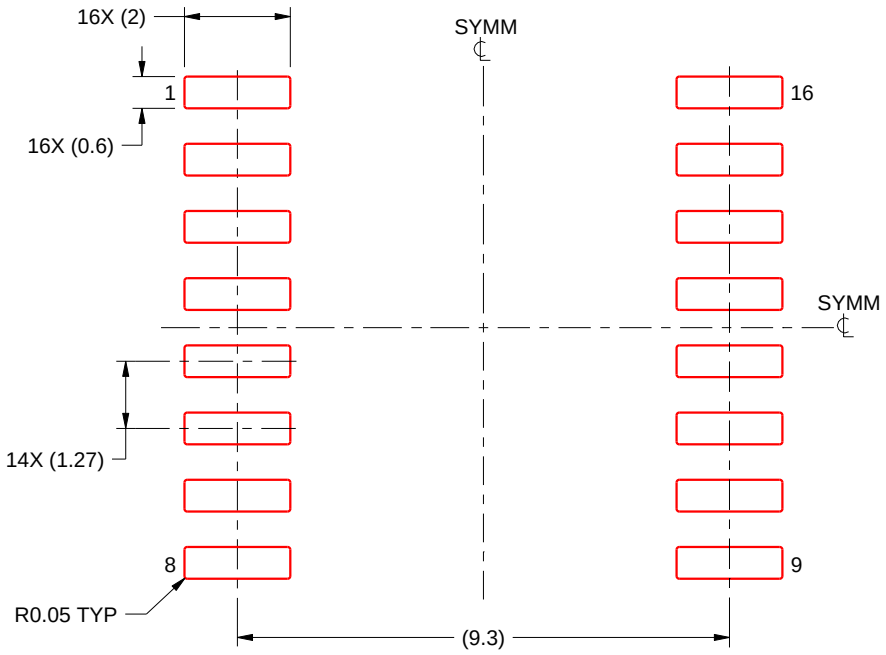
SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Texas Instruments
Downloaded From Oneyac.com



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

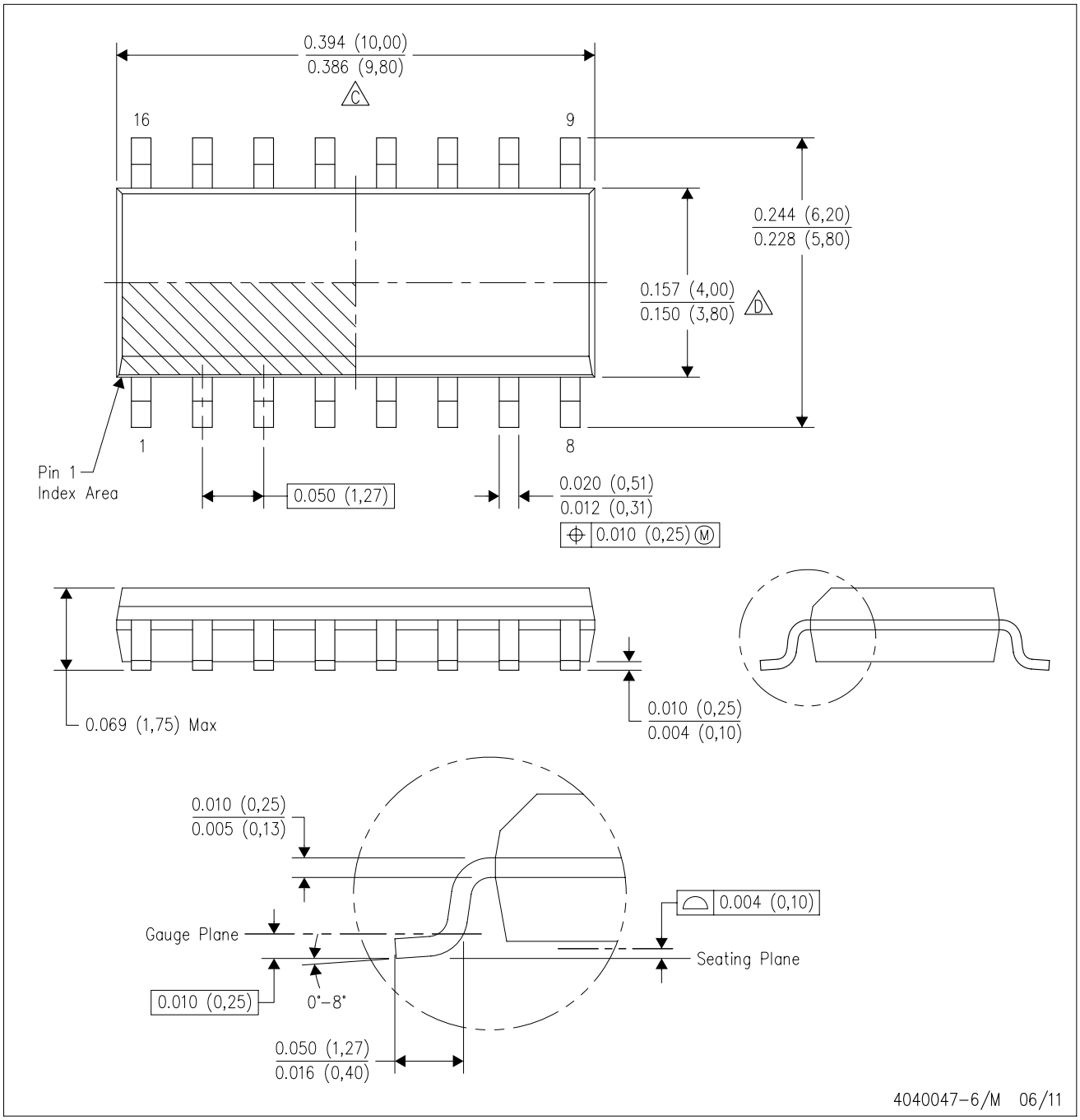
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Downloaded From Oneyac.com

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

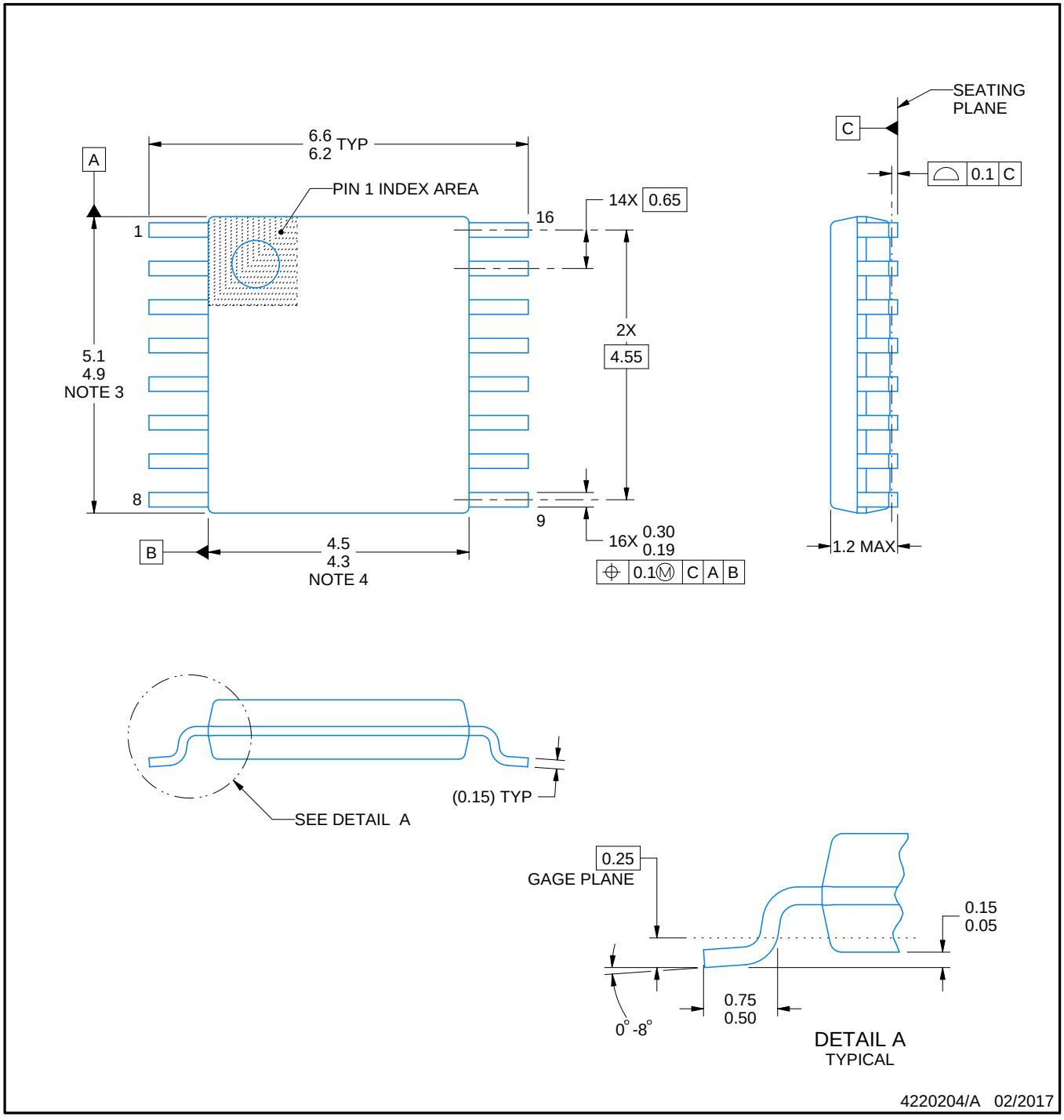
Downloaded From Oneyac.com

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

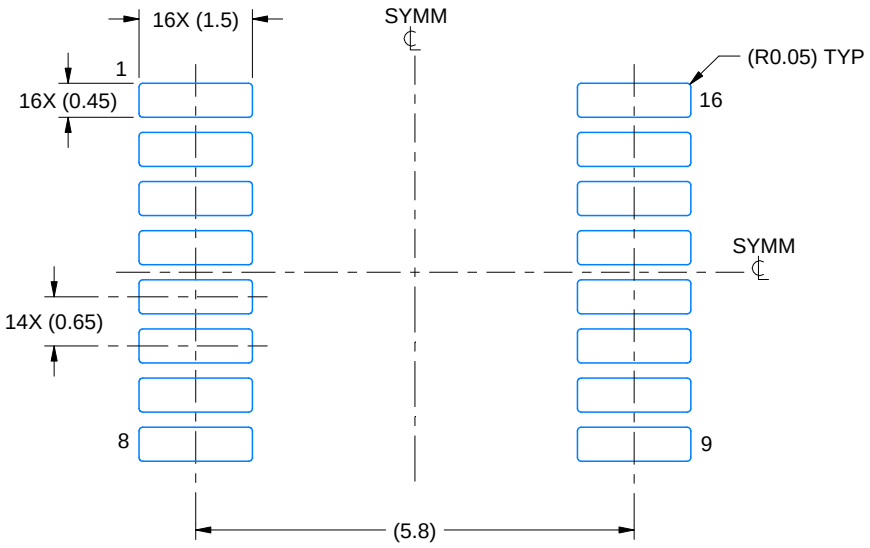


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

Texas Instruments

Downloaded From Oneyac.com



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Texas Instruments

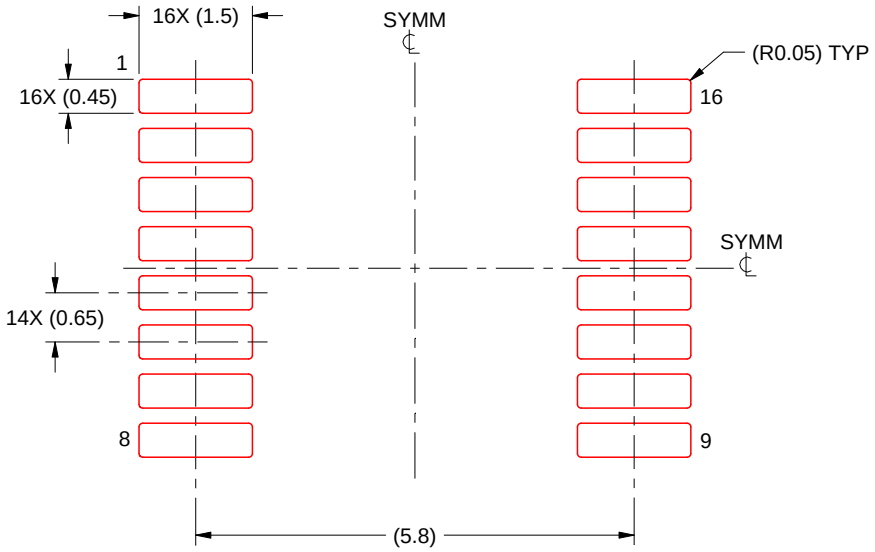
Downloaded From Oneyac.com

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

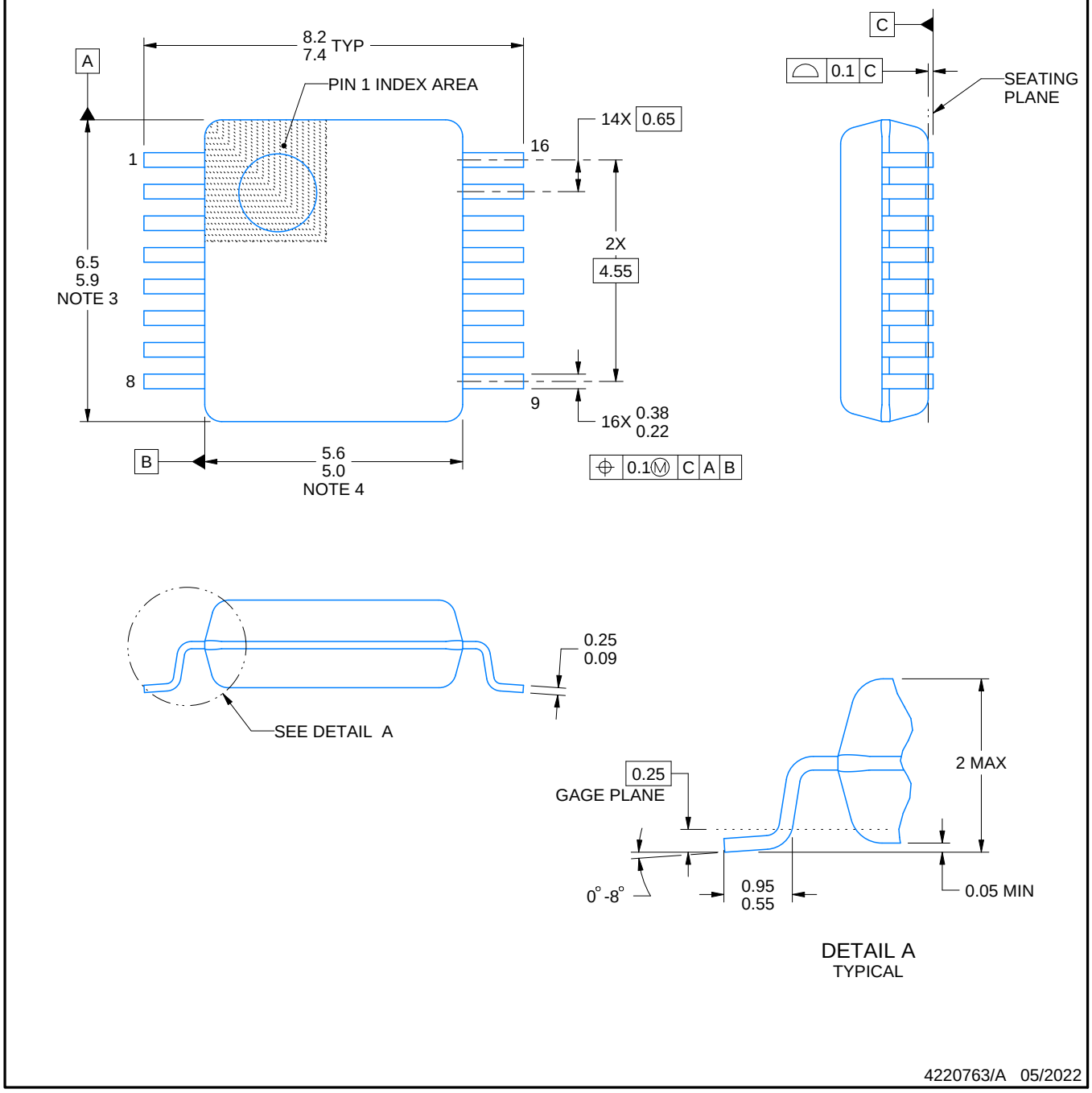
Texas Instruments
Downloaded From Oneyac.com

PACKAGE OUTLINE

DB0016A

SSOP - 2 mm max height

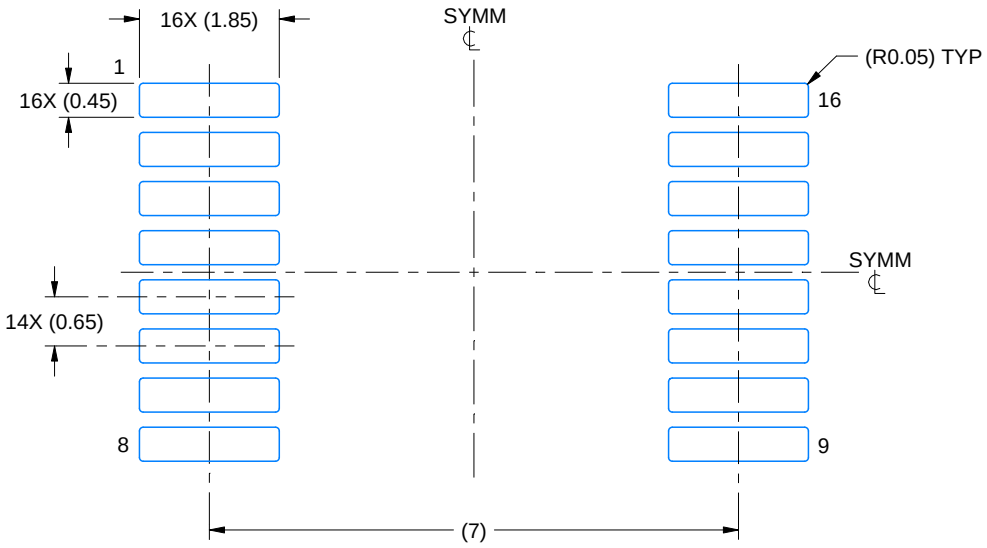
SMALL OUTLINE PACKAGE



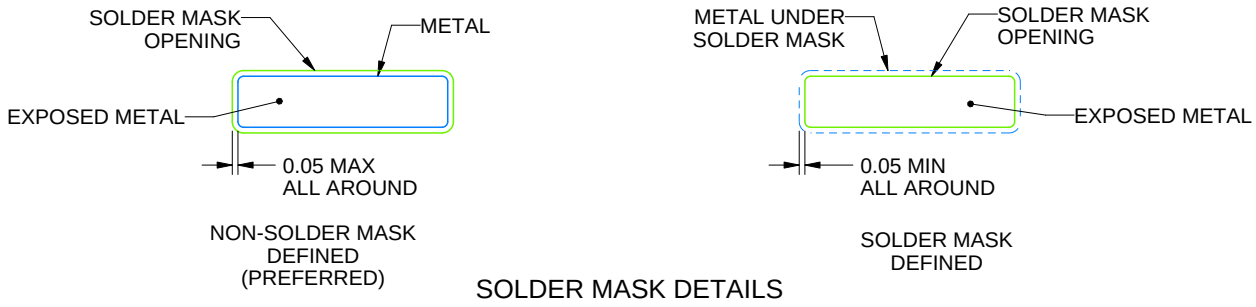
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

Texas Instruments
Downloaded From Oneyac.com



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Texas Instruments

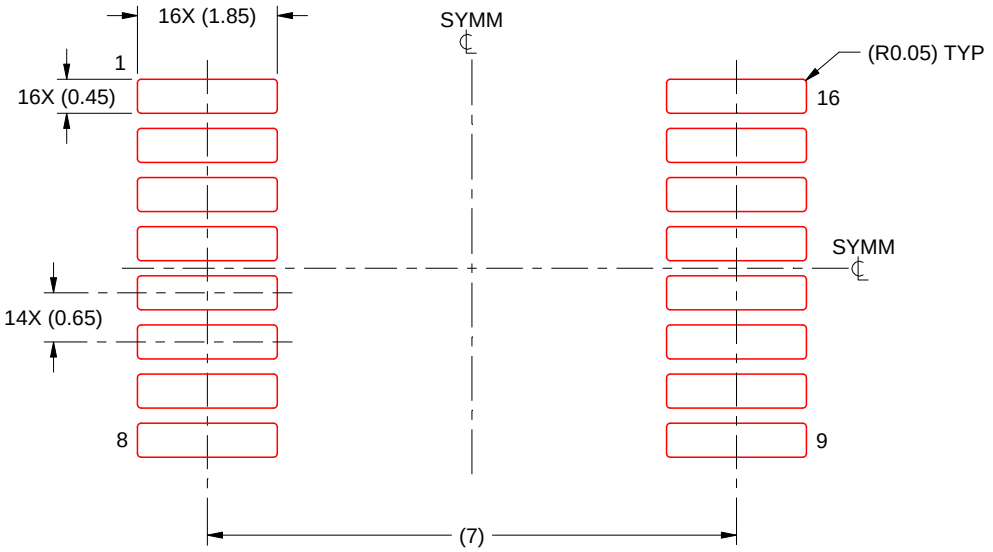
Downloaded From Oneyac.com

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

Texas Instruments
Downloaded From Oneyac.com

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023，德州仪器 (TI) 公司

Downloaded From Oneyac.com

单击下面可查看定价，库存，交付和生命周期等信息

>>TI(德州仪器)

Downloaded From Oneyac.com