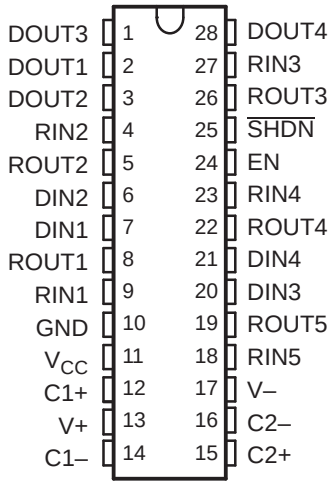
TRS213
5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

SLLS807 – JUNE 2007

FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Four Drivers and Five Receivers**
- **Operates up to 120 kbit/s**
- **Low Supply Current in Shutdown Mode . . . 15 µA Typ**
- **External Capacitors . . . 4 × 0.1 F**
- **Designed to Be Interchangeable With Industry Standard '213 Devices**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DB, DW, OR PW PACKAGE
(TOP VIEW)



APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION/ ORDER INFORMATION

The TRS213 device consists of four line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The devices operate at data signaling rates up to 120 kbit/s and a maximum of 30-V/µs driver output slew rate.

The TRS213 has an active-low shutdown ($\overline{SHDN}$) and an active-high enable control (EN). In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V– is pulled to GND, and the transmitter outputs are disabled. This reduces supply current typically to 1 µA. Two receivers of the TRS213 are active during shutdown.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 20	TRS213CDW	TRS213C
		Reel of 1000	TRS213CDWR	
	SSOP – DB	Tube of 50	TRS213CDB	TRS213C
		Reel of 2000	TRS213CDBR	
	TSSOP – PW	Tape and reel	TRS213CPWR	TRS213C
–40°C to 85°C	SOIC – DW	Tube of 20	TRS213IDW	TRS213I
		Reel of 1000	TRS213IDWR	
	SSOP – DB	Tube of 50	TRS213IDB	TRS213I
		Reel of 2000	TRS213IDBR	
	TSSOP – PW	Tape and reel	TRS213IPWR	TRS213I

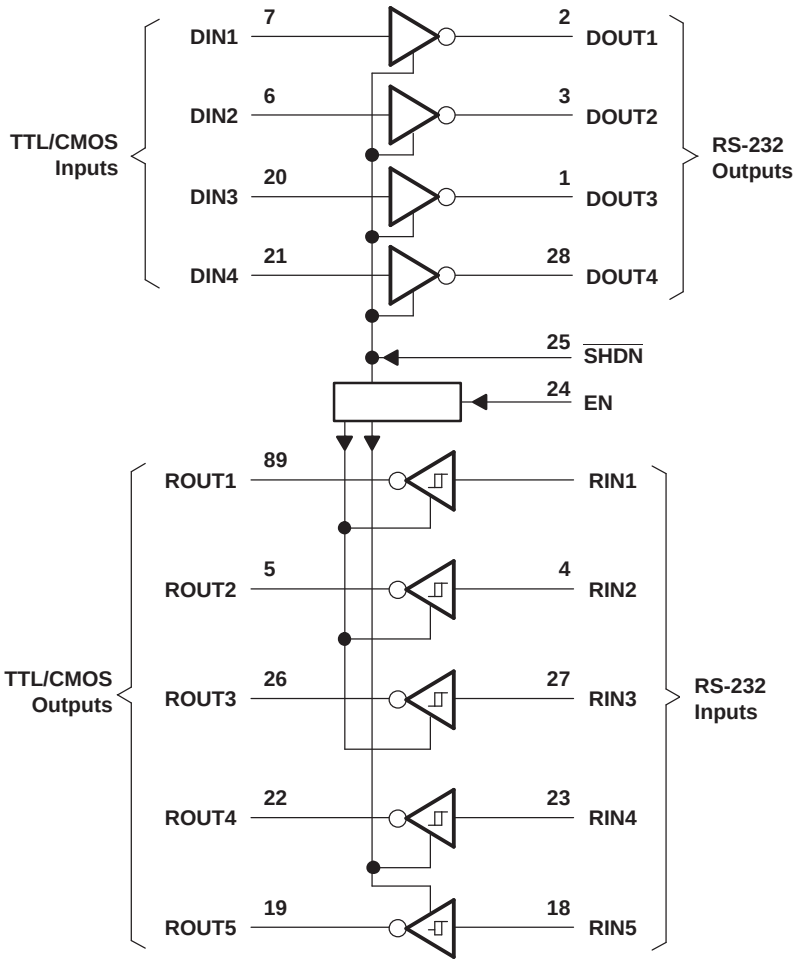
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

INPUTS		DRIVER D1–D4	RECEIVER		DEVICE STATUS
$\overline{SHDN}$	EN		R1–R3	R4–R5	
L	L	Z	Z	Z	Shutdown
L	H	Z	Z	Active(1)	Shutdown
H	L	All active	Z	Z	Normal operation
H	H	All active	Active	Active	Normal operation

(1) See the V_{IT+} and V_{IT-} change in the Electrical Characteristics table.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	6	V
V+	Positive charge-pump voltage range(2)		V_{CC} – 0.3	14	V
V–	Negative charge-pump voltage range(2)		0.3	–14	V
V_I	Input voltage range	Drivers	–0.3	V+ + 0.3	V
		Receivers		±30	
V_O	Output voltage range	Drivers	V– – 0.3	V+ + 0.3	V
		Receivers	–0.3	V_{CC} + 0.3	
DOUT	Short-circuit duration			Continuous	
θ_{JA}	Package thermal impedance(3)(4)	DB package		62	C°/W
		DW package		46	
		PW package			
T_J	Operating virtual junction temperature			150	C°
T_{stg}	Storage temperature range		–65	150	C°

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of $T_J(max)$,θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

See Figure 4

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
	Control high-level input voltage	EN, $\overline{SHDN}$	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, EN, $\overline{SHDN}$			0.8	V
V_I	Driver and control input voltage	DIN, EN, $\overline{SHDN}$	0		5.5	V
	Receiver input voltage	RIN	–30		30	
T_A	Operating free-air temperature	TRS213C	0		70	°C
		TRS213I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load,	See Figure 6		14	20	mA
I_{SHDN}	Shutdown supply current	T_A = 25°C,	See Figure 1		15	50	µA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics(1)

over operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND		5	9		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND		–5	–9		V
I_{IH}	Control high-level input current	EN, $\overline{SHDN}$ = 5 V			3	10	µA
I_{IL}	Driver low-level input current	DIN = 0 V			–15	–200	µA
	Control low-level input current	EN, $\overline{SHDN}$ = 0 V			–3	–10	
I_{OS}(3)	Short-circuit output current	V_{CC} = 5.5 V,	V_O = 0 V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300			Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 50 pF to 1000 pF, One DOUT switching,	R_L = 3 kΩ to 7 kΩ, See Figure 3	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500 pF, All drivers loaded,	R_L = 3 kΩ, See Figure 3		2		µs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500 pF, All drivers loaded,	R_L = 3 kΩ, See Figure 3		2		µs
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF, See Figure 3	R_L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 2)	C_L = 50 pF to 1000 pF, V_{CC} = 5 V	R_L = 3 kΩ to 7 kΩ,	3	6	30	V/µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as (t_{PLH} – t_{PHL}) of each channel of the same device.

ESD Protection

over operating free-air temperature range (unless otherwise noted)

PIN	TEST CONDITIONS	TYP	UNIT
DOUT	Human-Body Model	±15	kV

RECEIVER SECTION

Electrical Characteristics(1)

over operating free-air temperature range (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA			V_{CC} – 0.4		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA				0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C	Active mode		1.7	2.4	V
			Shutdown mode (R4–R5)		1.5	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C	Active mode	0.8	1.2		V
			Shutdown mode (R4–R5)	0.6	1.5		
V_{hys}(3)	Input hysteresis (V_{IT+}, $V_{IT–}$)	V_{CC} = 5 V			0.5	1	V
r_I	Input resistance	V_{CC} = 5 V, T_A = 25°C		3	5	7	kΩ
	Output leakage current	EN = 0 V, 0 ≤ ROUT ≤ V_{CC}, R1–R3			±0.05	±10	µA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) No hysteresis in shudown mode

Switching Characteristics(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150 pF,	See Figure 4	$\overline{SHDN}$ = V_{CC}		0.5	10	µs
				$\overline{SHDN}$ = 0 V, R4–R5		4	40	
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150 pF,	See Figure 4			0.5	10	µs
t_{en}	Output enable time	C_L = 150 pF,	See Figure 5			600		ns
t_{dis}	Output disable time	C_L = 150 pF,	See Figure 5			200		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

ESD Protection

over operating free-air temperature range (unless otherwise noted)

PIN	TEST CONDITIONS	TYP	UNIT
RIN	Human-Body Model	±15	kV

PARAMETER MEASUREMENT INFORMATION

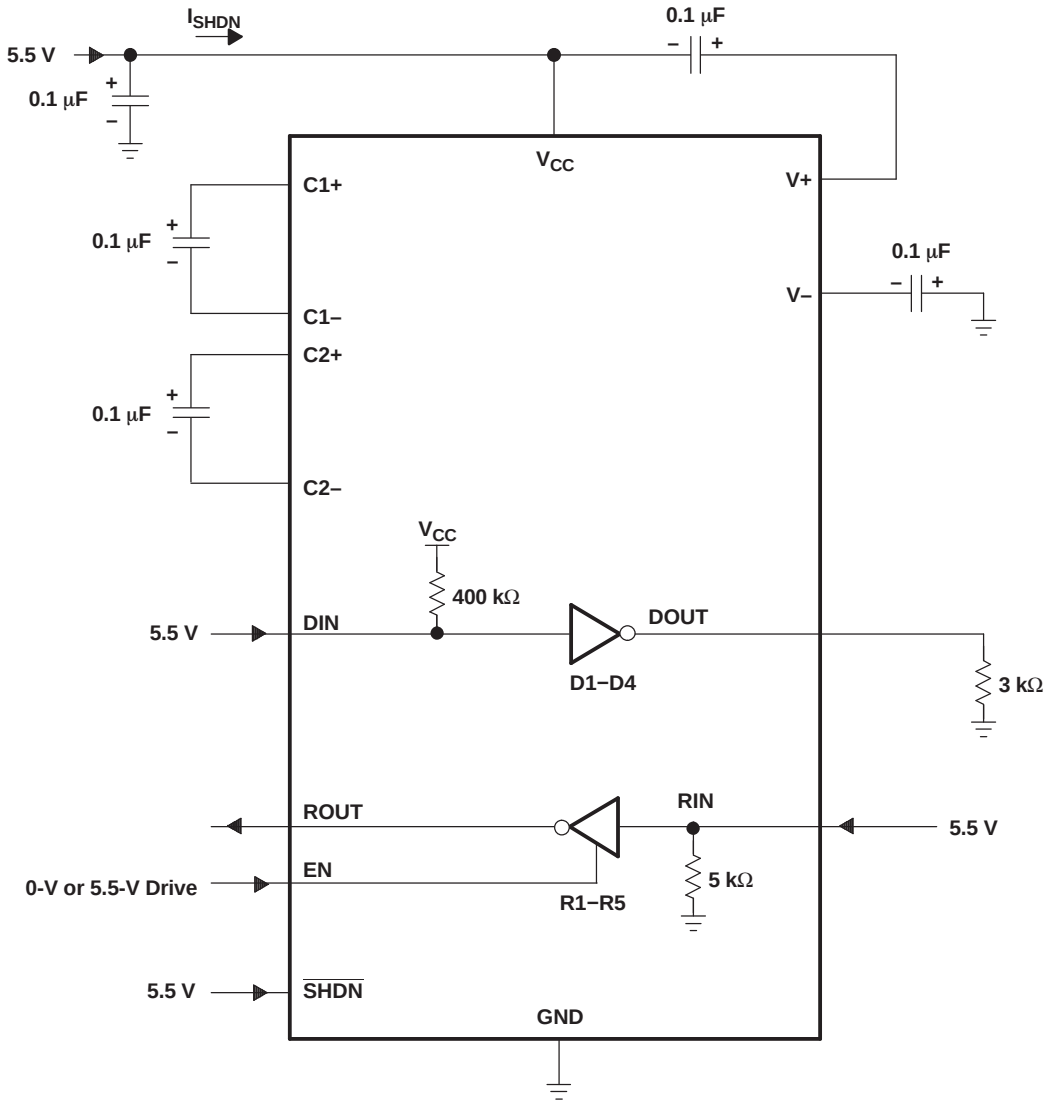
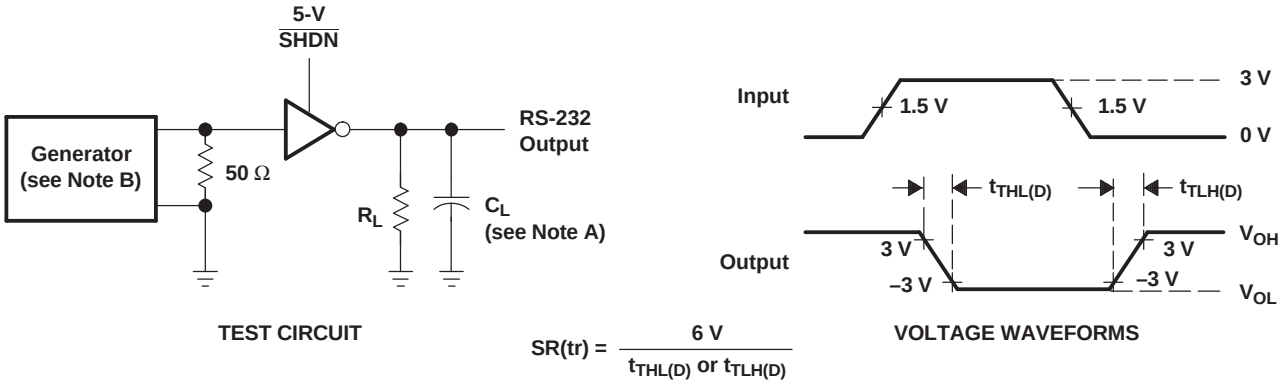


Figure 1. Shutdown Current Test Circuit



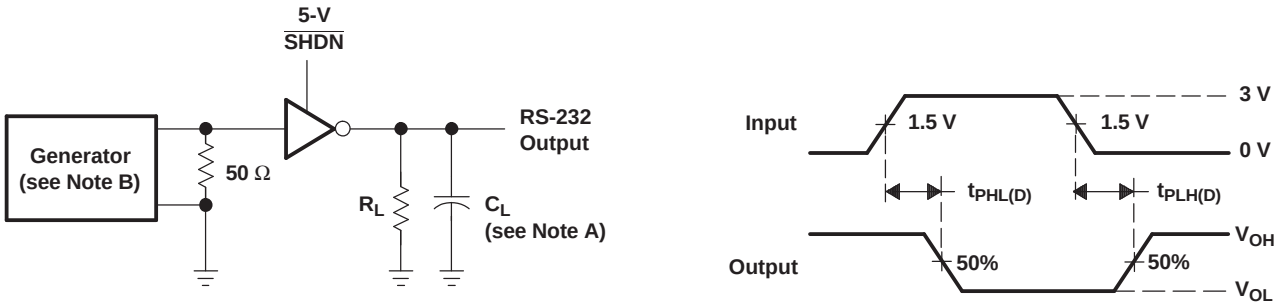
TEST CIRCUIT

$$SR(tr) = \frac{6\ V}{t_{THL(D)} \text{ or } t_{TLH(D)}}$$

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Slew Rate

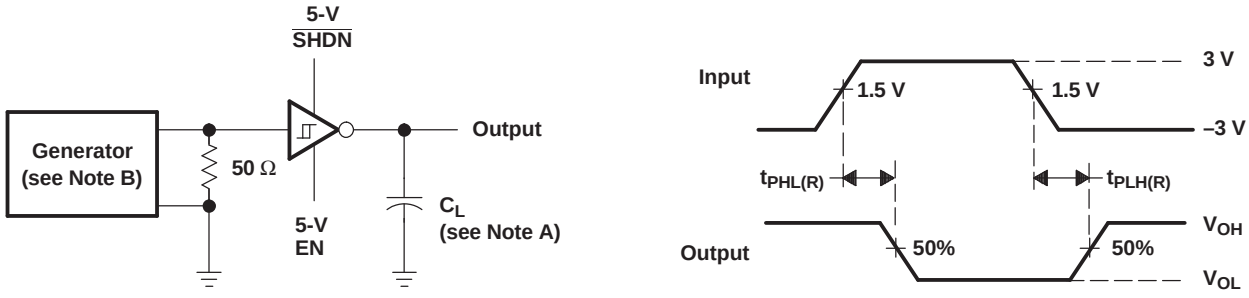


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Driver Pulse Skew and Propagation Delay Times

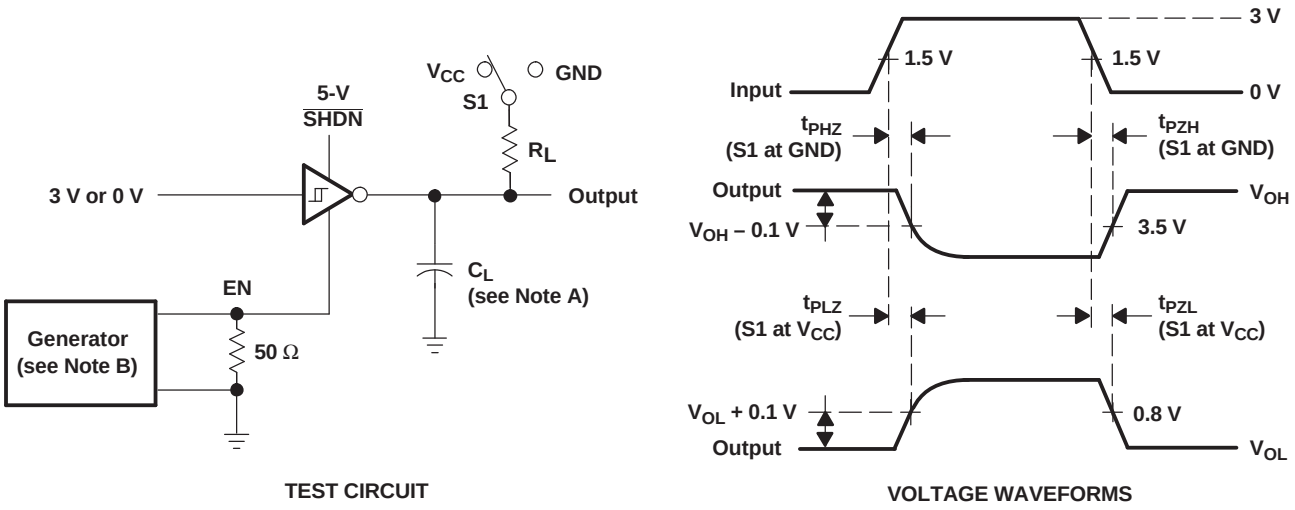


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

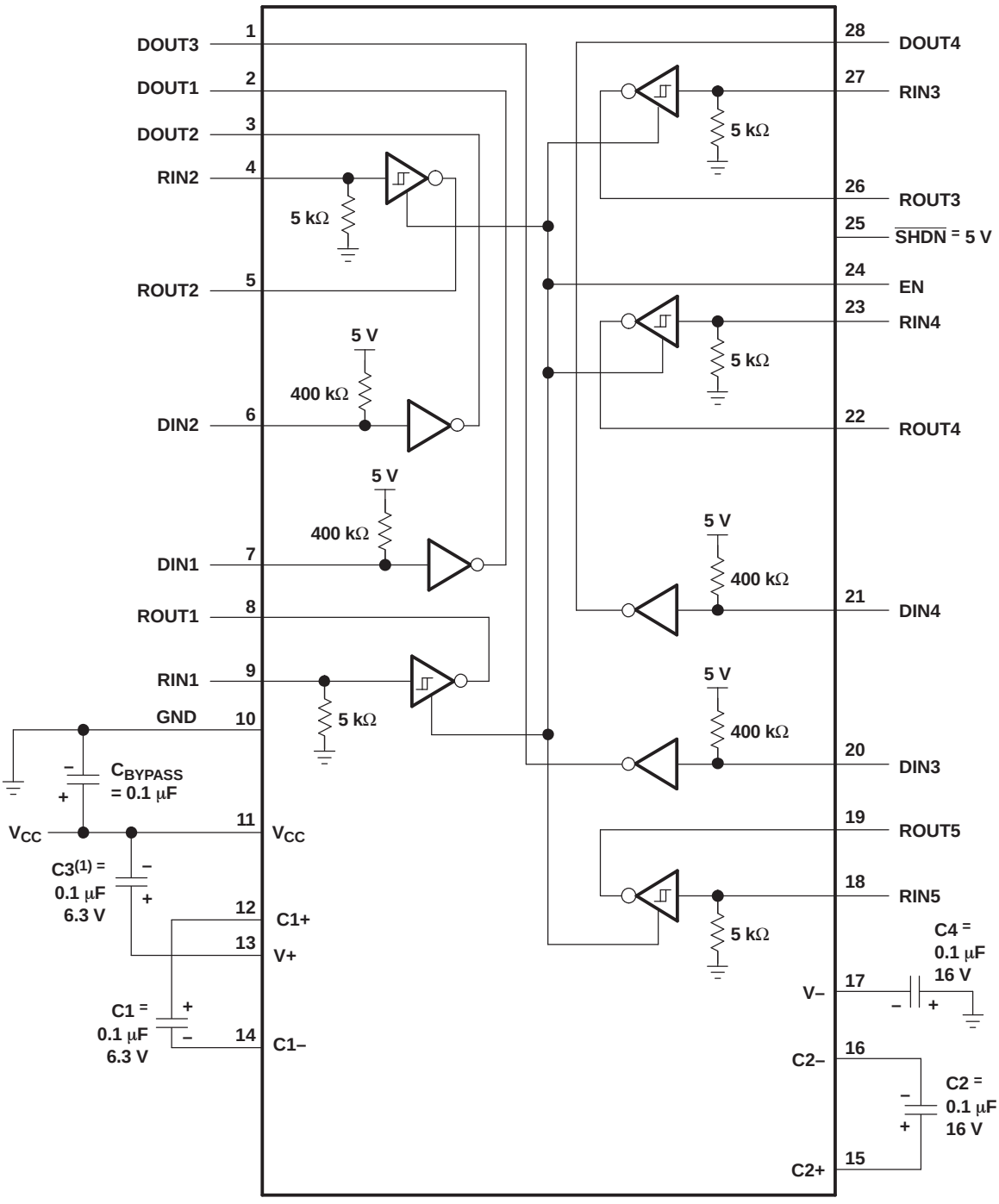
Figure 4. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Receiver Enable and Disable Times

APPLICATION INFORMATION



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS213CDBR	LIFEBUY	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS213C	
TRS213IDB	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I	
TRS213IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I	Samples
TRS213IDWR	LIFEBUY	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

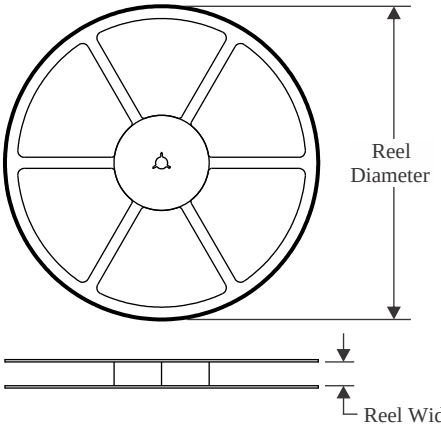
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

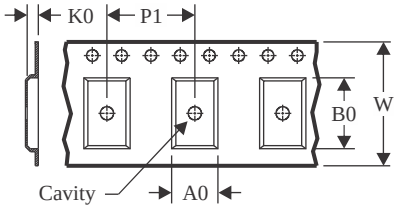
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

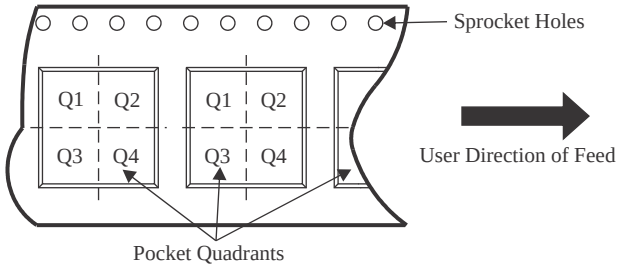


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

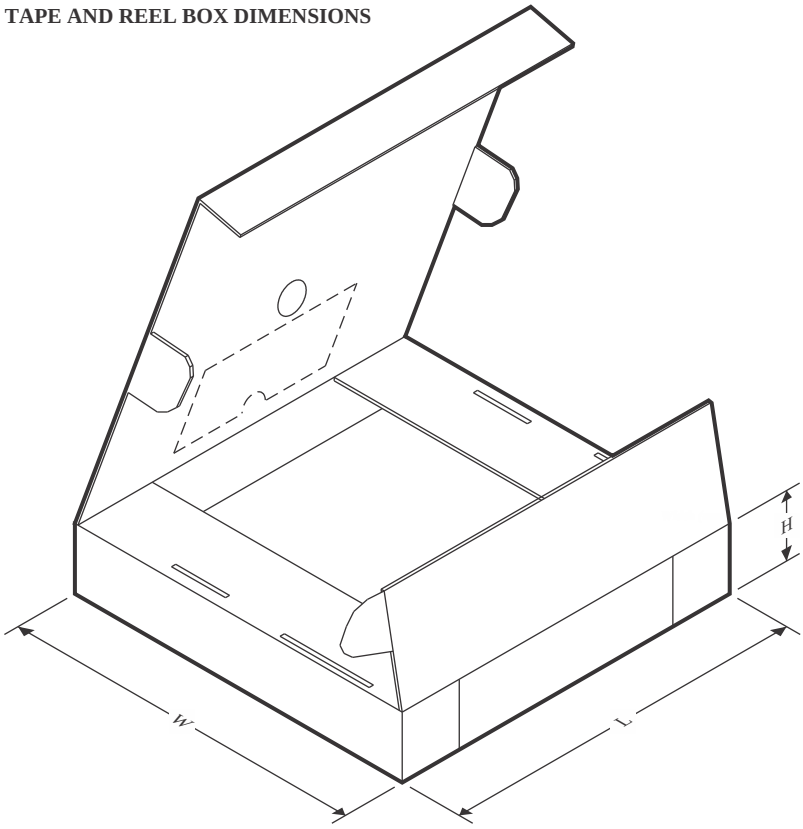
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS213CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS213IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS213IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

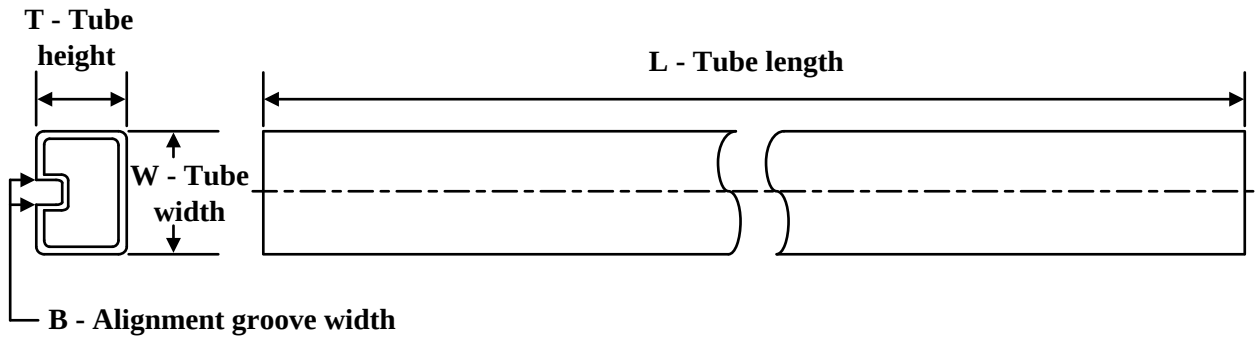
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS213CDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS213IDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS213IDWR	SOIC	DW	28	1000	350.0	350.0	66.0

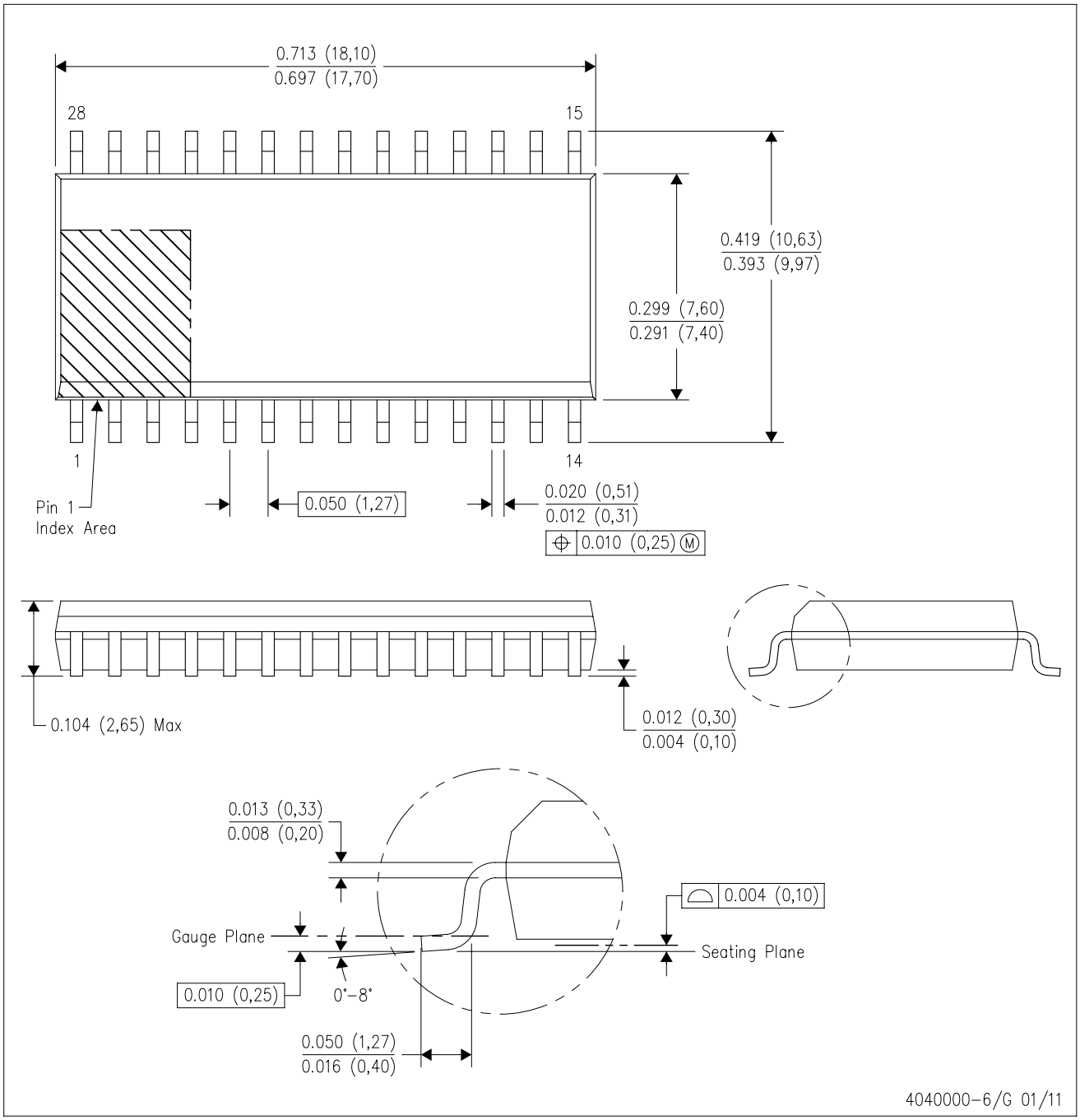
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TRS213IDB	DB	SSOP	28	50	530	10.5	4000	4.1

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



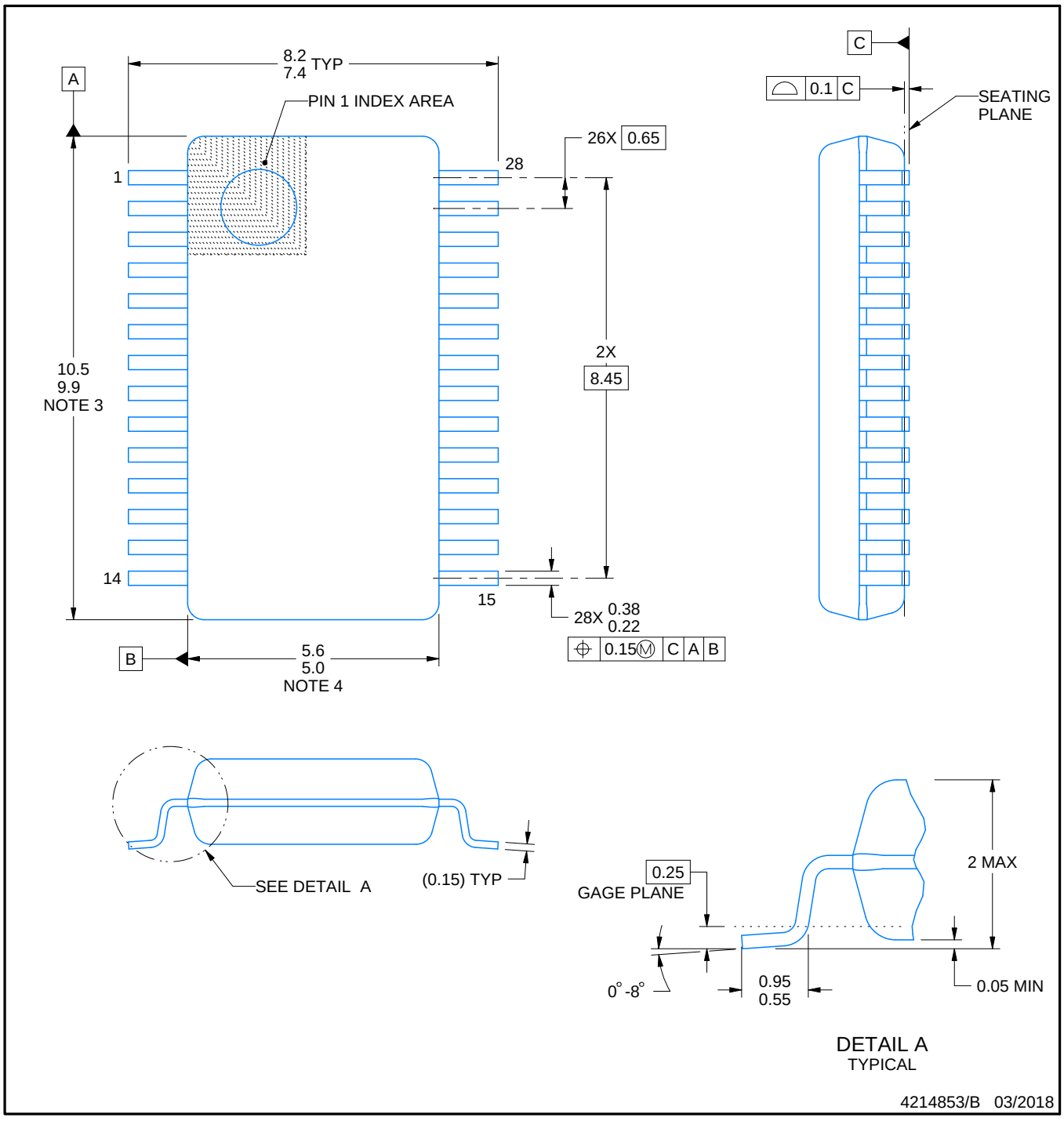
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PACKAGE OUTLINE

DB0028A

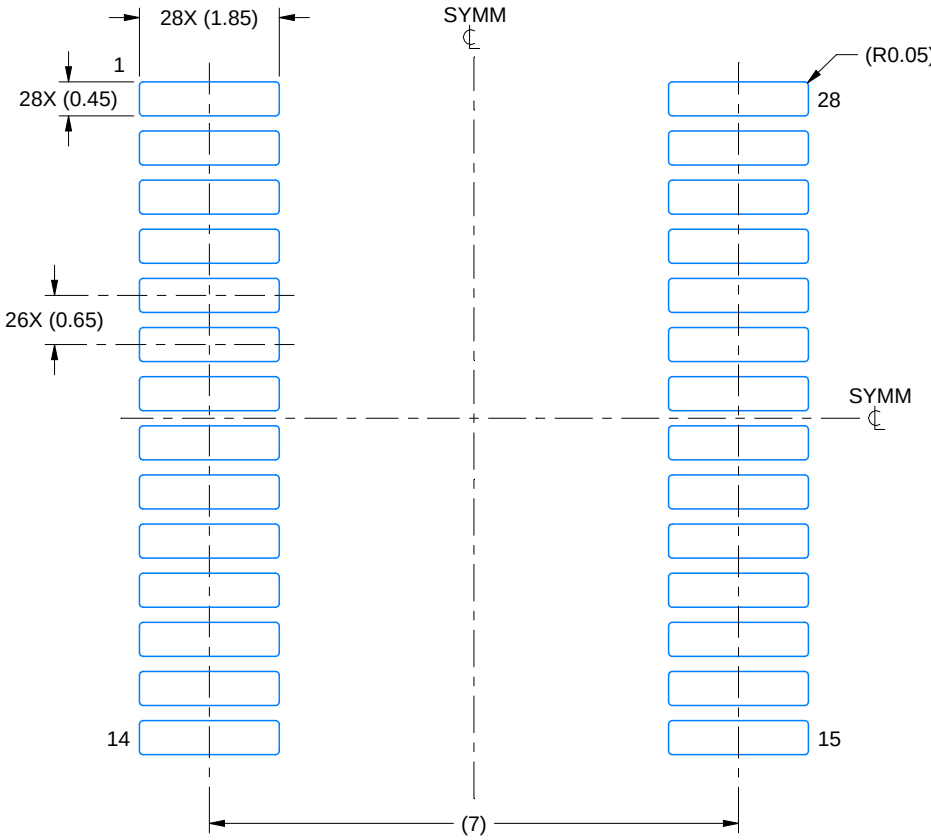
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

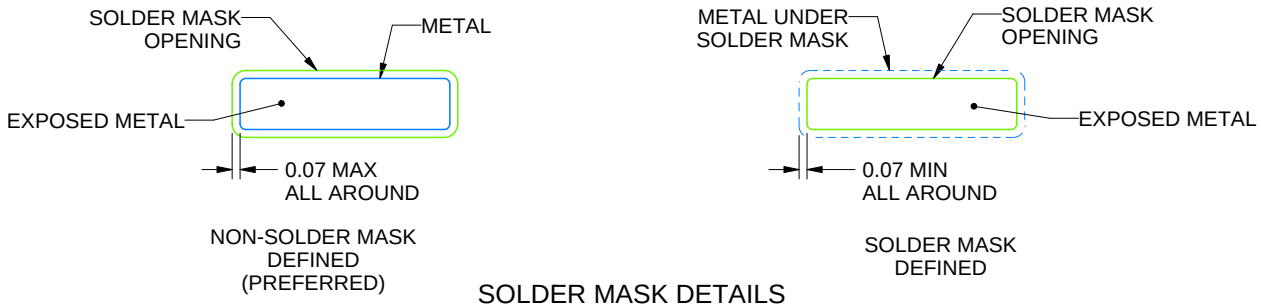


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

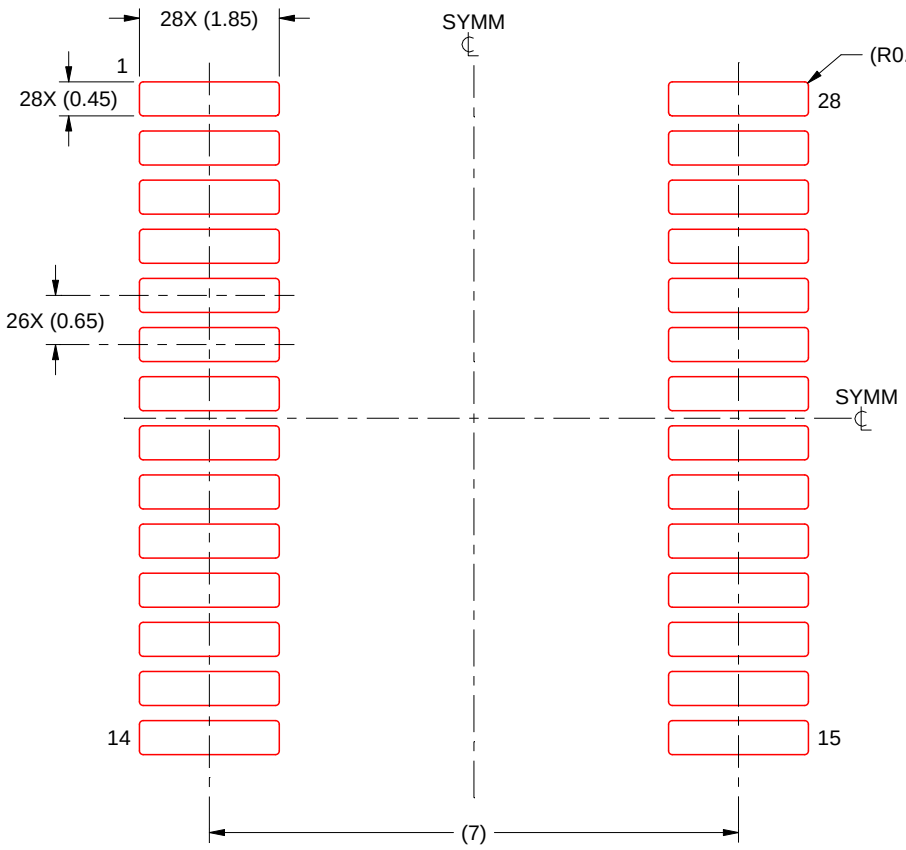
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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