TEXAS INSTRUMENTS
TPS54561
ZHCSBY9G – JULY 2013 – REVISED JUNE 2021

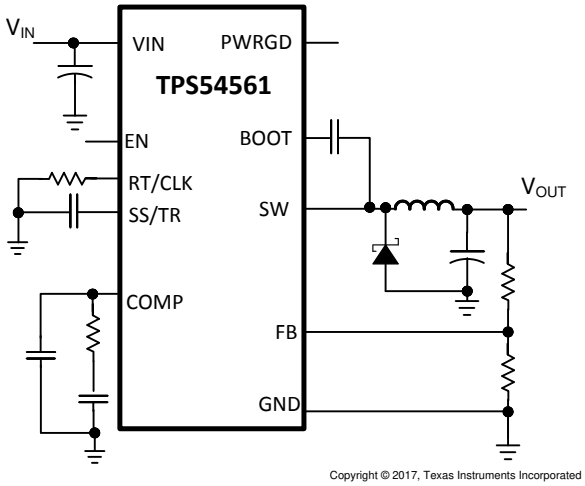
TPS54561 具有软启动和 Eco-mode™ 的 4.5V 至 60V 输入、5A 降压直流/直流转换器

1 特性

- 在轻负载条件下使用脉冲跳跃 Eco-mode™ 实现高效率
- 87mΩ 高侧 MOSFET
- 152μA 工作静态电流和 2μA 关断电流
- 100kHz 至 2.5MHz 可调开关频率
- 与外部时钟同步
- 轻负载条件下使用集成型 BOOT 再充电 FET 实现低压降
- 可调 UVLO 电压和迟滞
- UV 和 OV 电源正常输出
- 可调节软启动和时序
- 0.8V 1% 内部电压基准
- 带有散热焊盘的 10 引脚 WSON 封装
- –40°C 至 150°C T_J 工作范围
- 利用 TPS54561 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 工业自动化和电机控制
- 汽车配件：GPS（请参阅 SLVA412）、娱乐
- USB 专用充电端口和电池充电器（请参阅 SLVA464）
- 12V、24V 和 48V 工业、汽车及通信用电源系统



简化原理图

3 说明

TPS54561 是一款具有集成式高侧 MOSFET 的 60V、5A、降压稳压器。按照 ISO 7637 标准，此器件能够耐受的负载突降脉冲高达 65V。它采用电流模式控制，可实现简单的外部补偿和灵活的组件选择。一个低纹波脉冲跳跃模式将无负载时的电源电流减小至 152μA。当使能引脚被拉至低电平时，关断电源电流被减少至 2μA。

欠压闭锁在内部设定为 4.3V，但可用使能引脚上的一个外部电阻分压器将之提高。输出电压启动斜坡由软启动引脚控制，该引脚还可被配置用来控制时序/跟踪。开漏电源正常信号表示输出处于其标称电压的 93% 至 106% 之间。

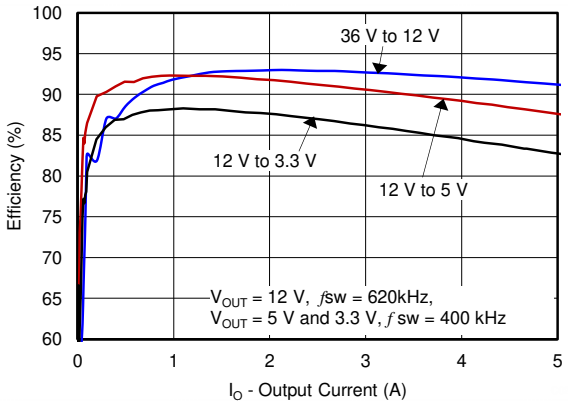
宽可调开关频率范围可针对效率或者外部组件尺寸进行优化。逐周期电流限制、频率折返和热关断在过载条件下保护内部和外部组件。

TPS54561 采用 10 引脚 4mm × 4mm WSON 封装。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS54561	WSON (10)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率和负载电流间的关系

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (January 2017) to Revision G (June 2021) — **Page**

- 更新了整个文档中的表、图和交叉参考的编号格式 1
- Added VIN - SW 5-ns and 10-ns transient 4
- Changed SW - GND 5-ns and 10-ns transient max values to 67 V 4

Changes from Revision E (February 2016) to Revision F (January 2017) — **Page**

- 向*特性*、*详细设计过程* 和*器件支持* 部分添加了 WEBENCH 信息 1
- Changed 方程式 10 and 方程式 11 20
- Changed 方程式 30 30
- Changed From: "power pad" To: "thermal pad" in the *Layout Guidelines* section 44

Changes from Revision C (November 2013) to Revision D (February 2016) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 1

Changes from Revision B (November 2013) to Revision C (November 2013) — **Page**

- 将器件状态从“产品预发布”更改为“量产” 1

Changes from Revision A (October 2013) to Revision B (November 2013) — **Page**

- 将*特性* 列表项中的“PowerPAD”更改为“散热焊盘” 1
- 删除了*说明* 部分对 PowerPAD 的引用 1
- Deleted *ORDERING INFORMATION* table before *DEVICE INFORMATION* section 3

Changes from Revision * (July 2013) to Revision A (October 2013) — **Page**

- 更改了效率和负载电流间的关系图，将 f_{SW} = 630KhZ 更改为 f_{SW} = 620kHz 1
- Added the APPLICATION INFORMATION section 30
- Added the Power Dissipation Estimate section 36

5 Pin Configuration and Functions

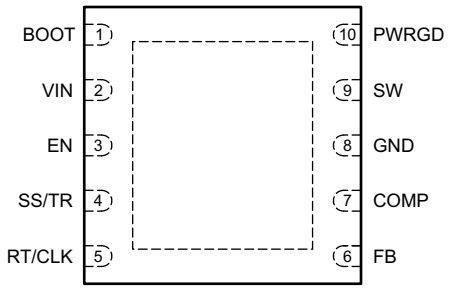


图 5-1. DPR Package 10-Pin WSON Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high-side MOSFET, the gate drive is switched off until the capacitor is refreshed.
VIN	2	I	Input supply voltage with 4.5-V to 60-V operating range.
EN	3	I	Enable pin, with internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See 节 7.3.7.
SS/TR	4	I	Soft-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	6	I	Inverting input of the transconductance (gm) error amplifier.
COMP	7	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
GND	8	–	Ground
SW	9	I	The source of the internal high-side power MOSFET and switching node of the converter.
PWRGD	10	O	Power Good is an open drain output that asserts low if the output voltage is out of regulation due to thermal shutdown, dropout, over-voltage or EN shut down
Thermal Pad	11	–	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VIN	– 0.3	65	V
	VIN - SW, 5-ns Transient	-7	67	
	VIN - SW, 10-ns Transient	-2	67	
	EN	– 0.3	8.4	
	BOOT – SW	– 0.3	8	
	FB	– 0.3	3	
	COMP	– 0.3	3	
	PWRGD	– 0.3	6	
	SS/TR	– 0.3	3	
	RT/CLK	– 0.3	3.6	
	SW - GND, 5-ns Transient	– 7	67	
	SW - GND, 10-ns Transient	– 2	67	
	SW	– 0.6	65	
Operating junction temperature, T_J		– 40	150	°C
Storage temperature range, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply input voltage, V_{VIN}	4.5		60	V
Output voltage, V_O	0.8		58.8	V
Output current, I_O	0		5	A
Operating junction temperature, T_J	-40		150	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS54561 DPR (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	°C/W

THERMAL METRIC(1) (2)		TPS54561 DPR (WSON) 10 PINS	UNIT
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Power rating at a specific ambient temperature TA should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See 节 *8.2.1.2.12* for more information.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 4.5 V to 60 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		4.5		60	V
Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
Internal undervoltage lockout threshold hysteresis			325		mV
Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 60 V		2.25	4.5	µA
Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		152	200	
ENABLE AND UVLO (EN PIN)					
Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
Input current	Enable threshold +50 mV		–4.6		µA
	Enable threshold –50 mV	–0.58	–1.2	-1.8	
Hysteresis current		–2.2	–3.4	-4.5	µA
Enable to COMP active	V_{IN} = 12 V, T_A = 25°C		540		µs
VOLTAGE REFERENCE					
Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET					
On-resistance	VIN = 12 V, BOOT-SW = 6 V		87	185	mΩ
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (g_M)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		350		µMhos
Error amplifier transconductance (g_M) during soft-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		µMhos
Error amplifier dc gain	V_{FB} = 0.8 V		10,000		V/V
Min unity gain bandwidth			2500		kHz
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±30		µA
COMP to SW current transconductance			17		A/V
CURRENT LIMIT					
Current limit threshold	All VIN and temperatures, Open Loop(1)	6.3	7.5	8.8	A
	All temperatures, VIN = 12 V, Open Loop(1)	6.3	7.5	8.3	
	VIN = 12 V, T_A = 25°C, Open Loop(1)	7.1	7.5	7.9	
Current limit threshold delay			60		ns
THERMAL SHUTDOWN					
Thermal shutdown			176		°C
Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
RT/CLK high threshold			1.55	2	V
RT/CLK low threshold		0.5	1.2		V
SOFT START AND TRACKING (SS/TR PIN)					
Charge current	$V_{SS/TR}$ = 0.4 V		1.7		µA
SS/TR-to-FB matching	$V_{SS/TR}$ = 0.4 V		42		mV
SS/TR-to-reference crossover	98% nominal		1.16		V
SS/TR discharge current (overload)	FB = 0 V, $V_{SS/TR}$ = 0.4 V		354		µA
SS/TR discharge voltage	FB = 0 V		54		mV
POWER GOOD (PWRGD PIN)					
FB threshold for PWRGD low	FB falling		90		%
FB threshold for PWRGD high	FB rising		93		%

T_J = –40°C to 150°C, V_{IN} = 4.5 V to 60 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FB threshold for PWRGD low	FB rising		108		%
FB threshold for PWRGD high	FB falling		106		%
Hysteresis	FB falling		2.5		%
Output high leakage	V_{PWRGD} = 5.5 V, T_A = 25°C		10		nA
On resistance	I_{PWRGD} = 3 mA, V_{FB} < 0.79 V		45		Ω
Minimum VIN for defined output	V_{PWRGD} < 0.5 V, I_{PWRGD} = 100 µA		0.9	2	V

(1) Open Loop current limit measured directly at the SW pin and is independent of the inductor value and slope compensation.

6.6 Timing Requirements

T_J = –40°C to 150°C, VIN = 4.5 V to 60 V (unless otherwise noted)

	MIN	NOM	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)				
Minimum CLK input pulse width		15		ns
RT/CLK falling edge to SW rising edge delay – Measured at 500 kHz with RT resistor in series		55		ns

6.7 Switching Characteristics

T_J = –40°C to 150°C, VIN = 4.5 V to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using RT mode		100		2500	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	PLL lock in time	Measured at 500 kHz		78		µs

6.8 Typical Characteristics

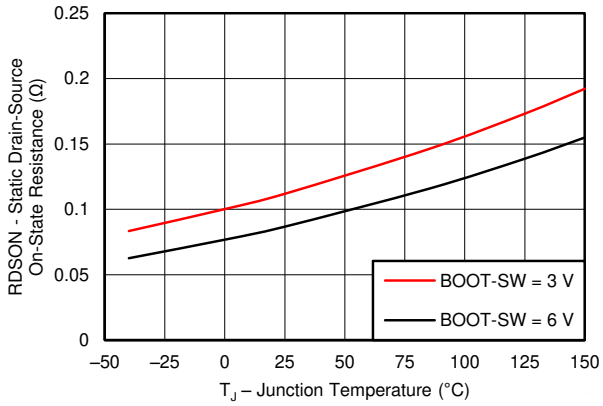


图 6-1. ON Resistance vs Junction Temperature

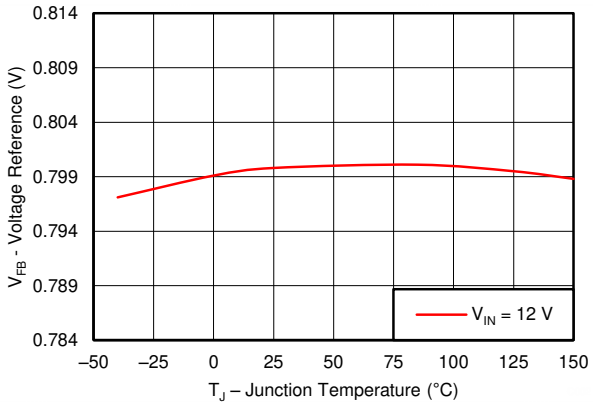


图 6-2. Voltage Reference vs Junction Temperature

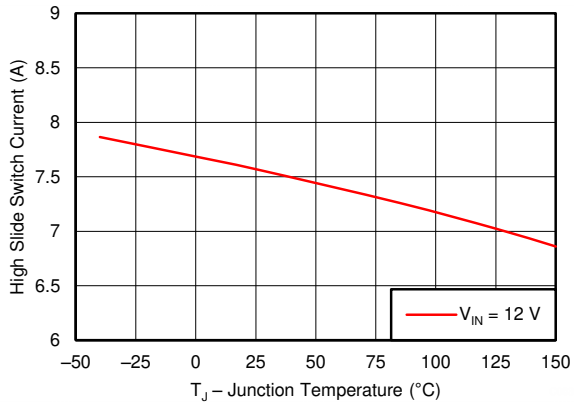


图 6-3. Switch Current Limit vs Junction Temperature

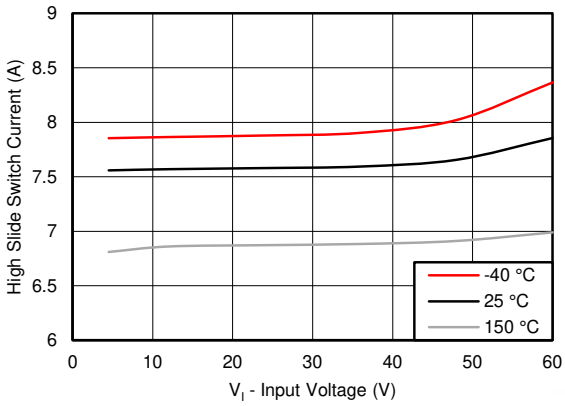


图 6-4. Switch Current Limit vs Input Voltage

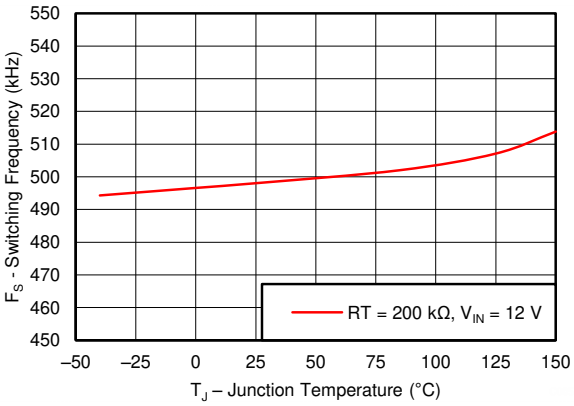


图 6-5. Switching Frequency vs Junction Temperature

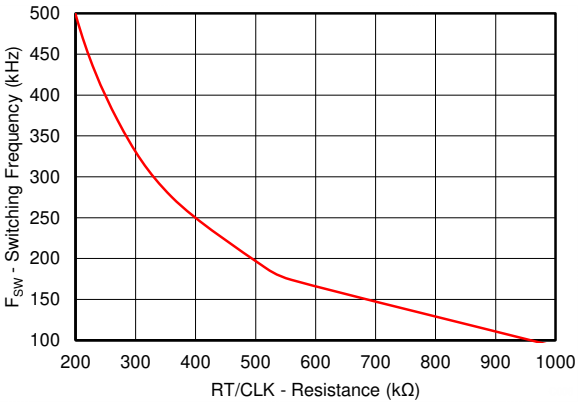


图 6-6. Switching Frequency vs RT/CLK Resistance Low Frequency Range

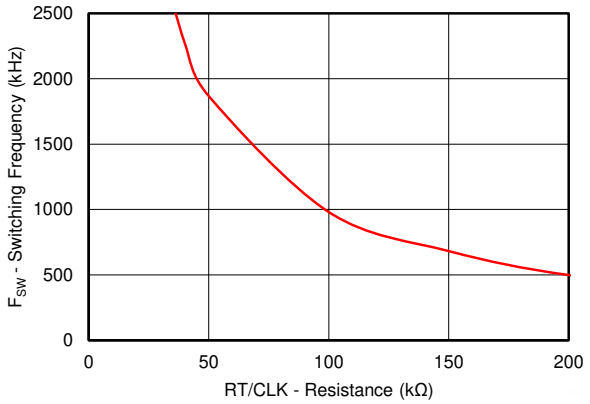


图 6-7. Switching Frequency vs RT/CLK Resistance High Frequency Range

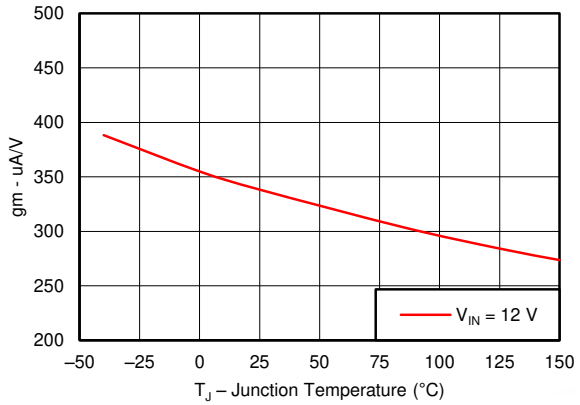


图 6-8. EA Transconductance vs Junction Temperature

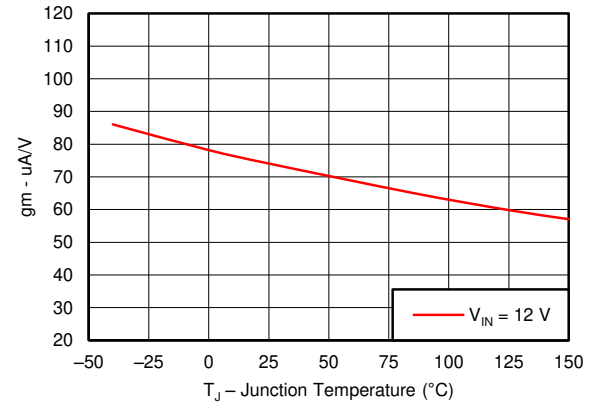


图 6-9. EA Transconductance During Soft-Start vs Junction Temperature

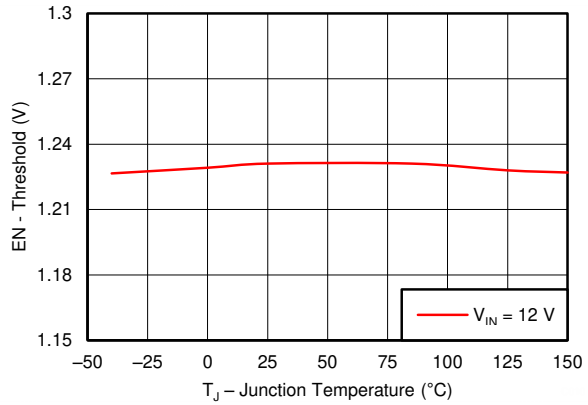


图 6-10. EN Pin Voltage vs Junction Temperature

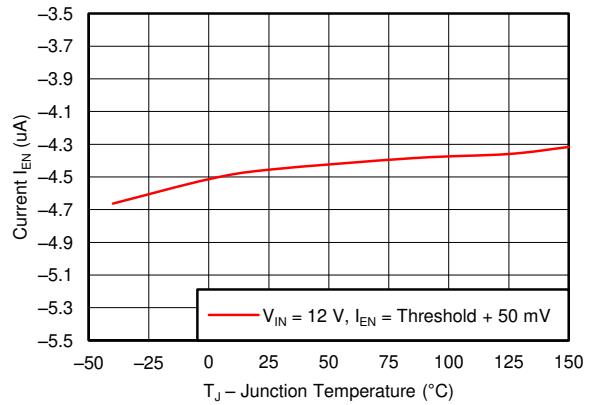


图 6-11. EN Pin Current vs Junction Temperature

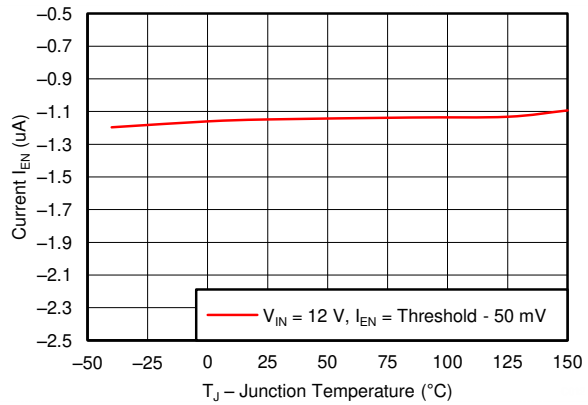


图 6-12. EN Pin Current vs Junction Temperature

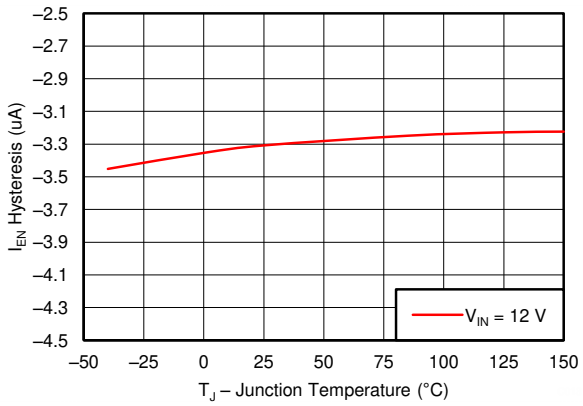


图 6-13. EN Pin Current Hysteresis vs Junction Temperature

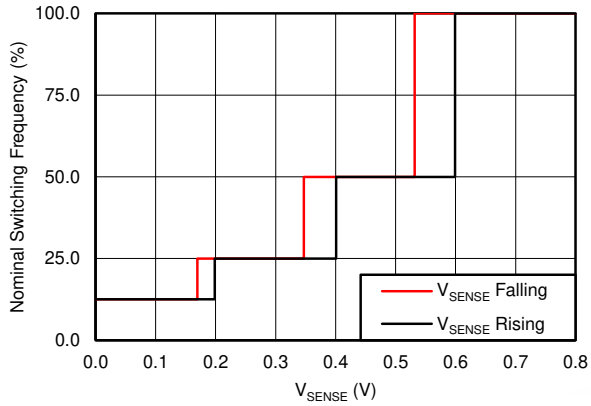


图 6-14. Switching Frequency vs FB

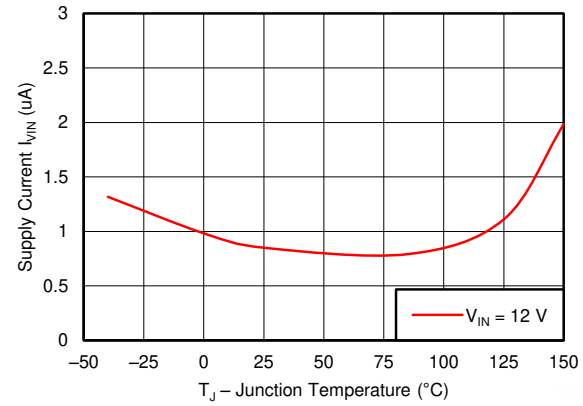


图 6-15. Shutdown Supply Current vs Junction Temperature

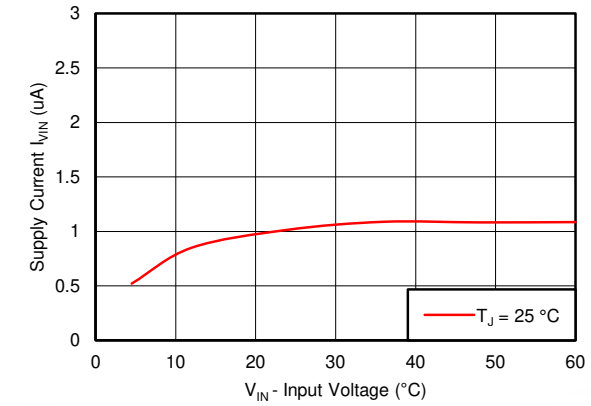


图 6-16. Shutdown Supply Current vs Input Voltage (V_{IN})

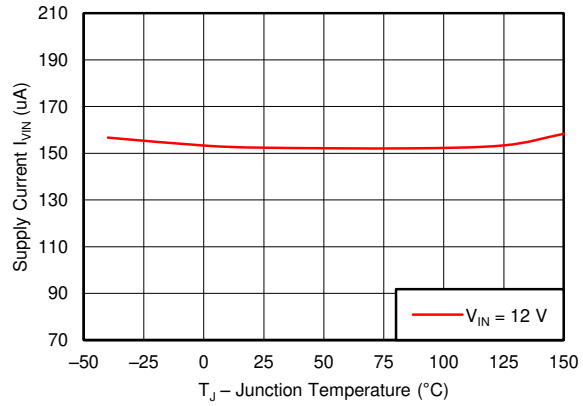


图 6-17. V_{IN} Supply Current vs Junction Temperature

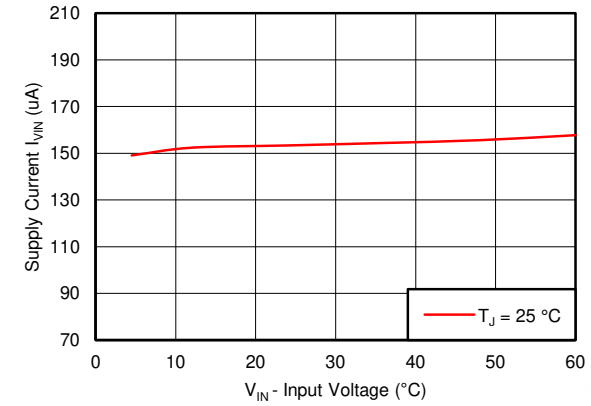


图 6-18. V_{IN} Supply Current vs Input Voltage

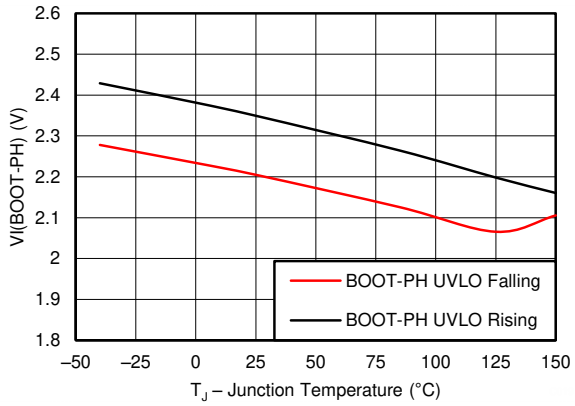


图 6-19. BOOT-SW UVLO vs Junction Temperature

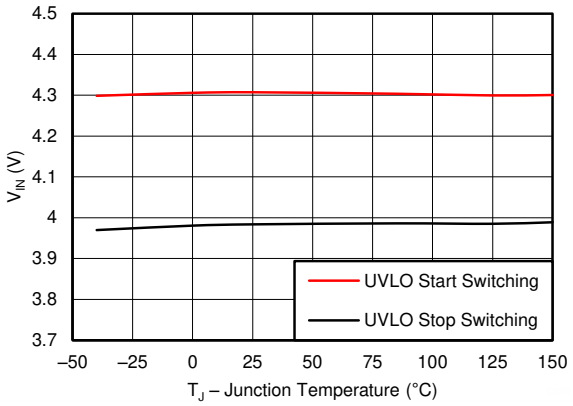


图 6-20. Input Voltage UVLO vs Junction Temperature

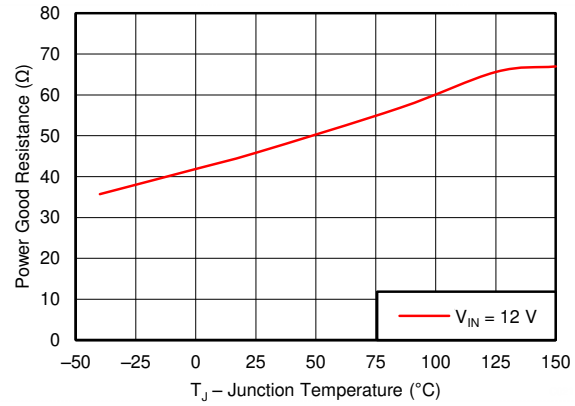


图 6-21. PWRGD ON Resistance vs Junction Temperature

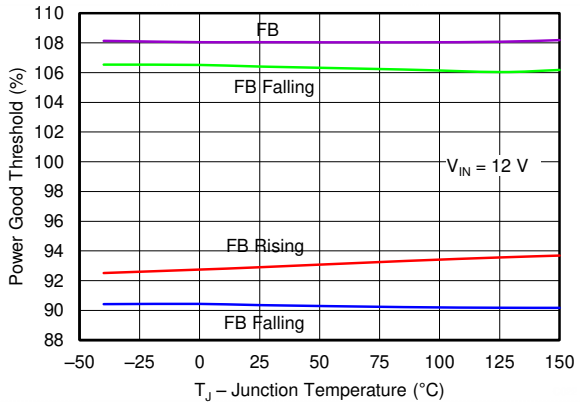


图 6-22. PWRGD Threshold vs Junction Temperature

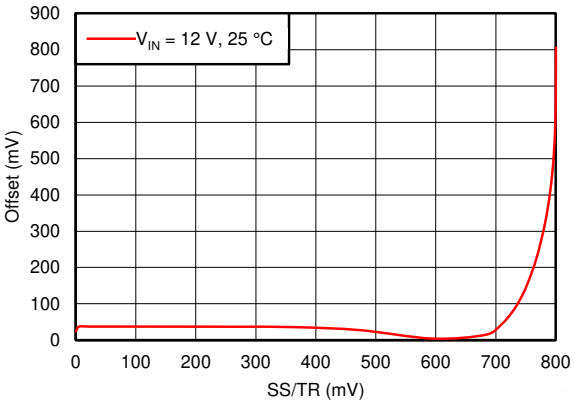


图 6-23. SS/TR to FB Offset vs FB

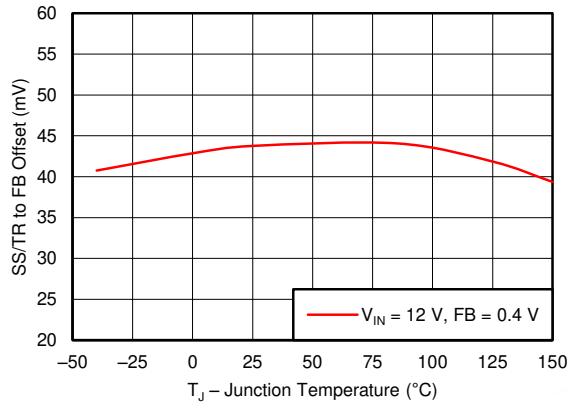


图 6-24. SS/TR to FB Offset vs Temperature

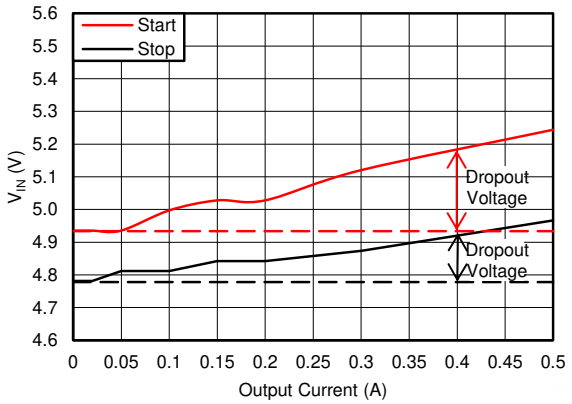


图 6-25. 5-V Start and Stop Voltage (see)

7 Detailed Description

7.1 Overview

The TPS54561 is a 60-V, 5-A, step-down (buck) regulator with an integrated high side n-channel MOSFET. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK pin. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that will synchronize the power switch turn on to a falling edge of an external clock signal.

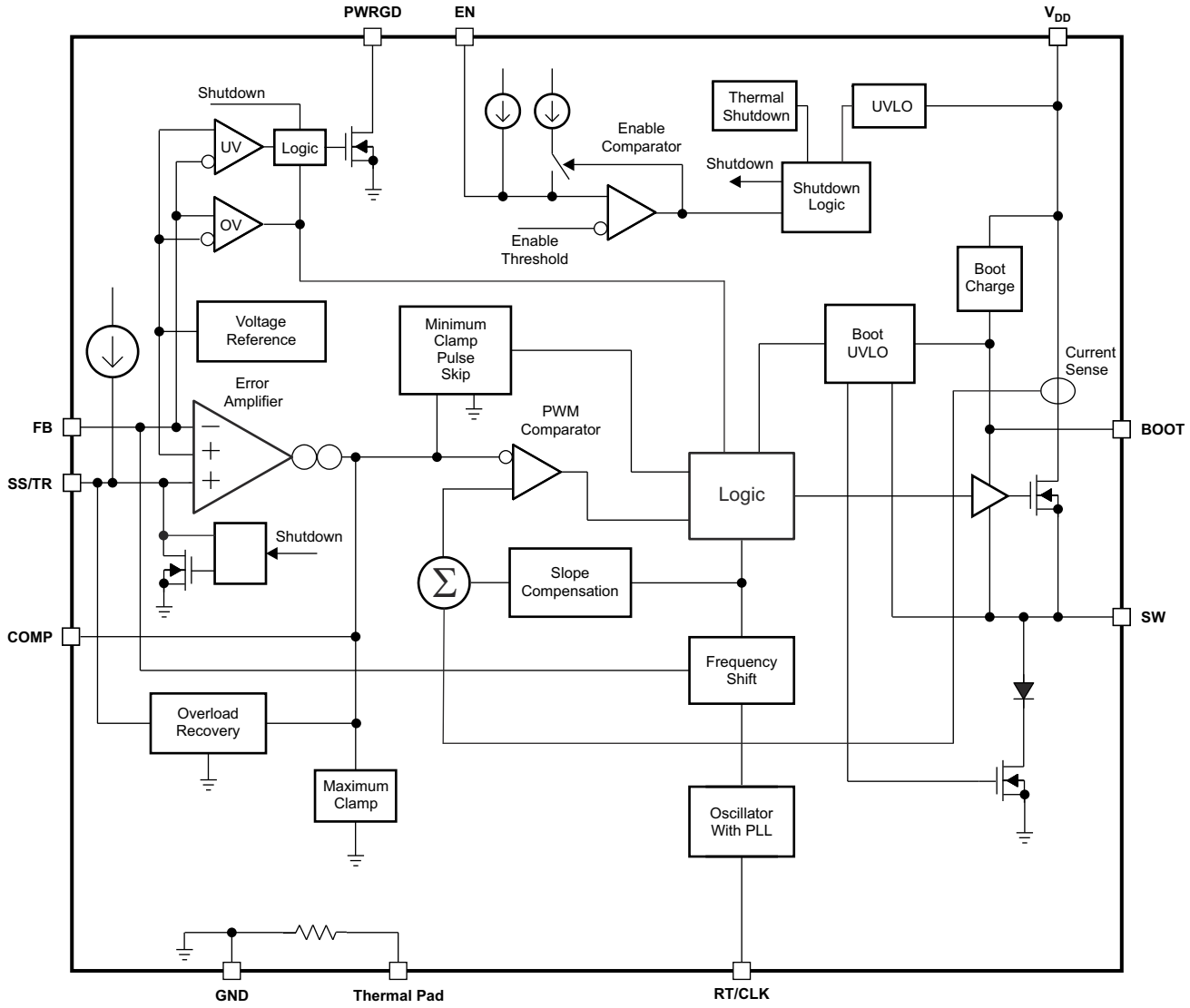
The TPS54561 has a default input start-up voltage of 4.3 V typical. The EN pin can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. An internal pull up current source enables operation when the EN pin is floating. The operating current is 152 μA under no load condition when not switching. When the device is disabled, the supply current is 2 μA.

The integrated 87-mΩ high side MOSFET supports high efficiency power supply designs capable of delivering 5 A of continuous current to a load. The gate drive bias voltage for the integrated high side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW pins. The TPS54561 reduces the external component count by integrating the bootstrap recharge diode. The BOOT pin capacitor voltage is monitored by a UVLO circuit which turns off the high side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54561 to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8-V feedback reference.

Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high side MOSFET is turned off and remains off until the output voltage is less than 106% of the desired output voltage.

The SS/TR (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be connected to the pin to adjust the soft start time. A resistor divider can be connected to the pin for critical power supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault, UVLO fault or a disabled condition. When the overload condition is removed, the soft start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start up and overcurrent fault conditions to help maintain control of the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54561 uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output at the COMP pin controls the high side power switch current. When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP pin.

7.3.2 Slope Compensation Output Current

The TPS54561 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

7.3.3 Pulse Skip Eco-mode

The TPS54561 operates in a pulse skipping Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco-mode. The pulse skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-mode, the COMP pin voltage is clamped at 600 mV and the high side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP pin voltage. The high side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54561 senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. As the load current approaches zero, the device enters a pulse skip mode during which it draws only 152-μA input quiescent current. The circuit in 图 8-1 enters Eco-mode at 25-mA output current and with no external load has an average input current of 280 μA.

7.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54561 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high side MOSFET. The BOOT capacitor is refreshed when the high side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high side MOSFET of the TPS54561 will operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1V. When the voltage from BOOT to SW drops below 2.1 V, the high side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low side MOSFET at high output voltages, it is disabled at 24 V output and re-enabled when the output reaches 21.5 V.

Since the gate drive current sourced from the BOOT capacitor is small, the high side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

The start and stop voltage for a typical 5-V output application is shown in 图 6-25 where the input voltage is plotted versus load current. The start voltage is defined as the input voltage needed to regulate the output within 1% of nominal. The stop voltage is defined as the input voltage at which the output drops by 5% or where switching stops.

During high duty cycle (low dropout) conditions, inductor current ripple increases when the BOOT capacitor is being recharged resulting in an increase in output voltage ripple. Increased ripple occurs when the off time required to recharge the BOOT capacitor is longer than the high side off time associated with cycle by cycle PWM control.

At heavy loads, the minimum input voltage must be increased to ensure a monotonic startup. 方程式 1 can be used to calculate the minimum input voltage for this condition.

$$V_O max = Dmax \times (V_{VIN} min - I_O max \times R_{DS(on)} + Vd) - Vd - I_O max \times R_{dc} \quad (1)$$

Where:

- Dmax ≥ 0.9
- Vd = Forward Drop of the Catch Diode

- R_{dc} = DC resistance of output inductor
- $R_{DS(on)}$ = 1 / (-0.3 × VB2SW^2 + 3.577 × VB2SW - 4.246)
- VB2SW = VBOOT + Vd
- VBOOT = (1.41 × V_{VIN} - 0.554 - Vd × fsw - 1.847 × 10^3 × IB2SW) / (1.41 + fsw)
- fsw = Operating frequency in MHz
- IB2SW = 100 × 10^{-6} A

7.3.5 Error Amplifier

The TPS54561 voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 350 μA/V during normal operation. During soft-start operation, the transconductance is reduced to 78 μA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP pin and GND pin.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8-V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. The output voltage is set by a resistor divider from the output node to the FB pin. Using 1% tolerance or better divider resistors is recommended. Select the low side resistor R_{LS} for the desired divider current and use 方程式 2 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \tag{2}$$

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54561 is enabled when the VIN pin voltage rises above 4.3 V and the EN pin voltage exceeds the enable threshold of 1.2 V. The TPS54561 is disabled when the VIN pin voltage falls below 4 V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pull-up current source, I1, of 1.2 μA that enables operation of the TPS54561 when the EN pin floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in 图 7-1 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.4 μA of hysteresis current, I_{HYS}, is sourced out of the EN pin. When the EN pin is pulled below 1.2 V, the 3.4-μA Ihys current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use 方程式 3 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use 方程式 4 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (that is, from 4.5 V to 9 V) and withstand high input voltages (that is, from 40 V to 60 V), the EN pin may experience a voltage greater than the absolute maximum voltage of 8.4 V during the high input voltage condition. To avoid exceeding this voltage when using the EN resistors, the EN pin is clamped internally with a 5.8-V zener diode that will sink up to 150 μA.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{3}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \tag{4}$$

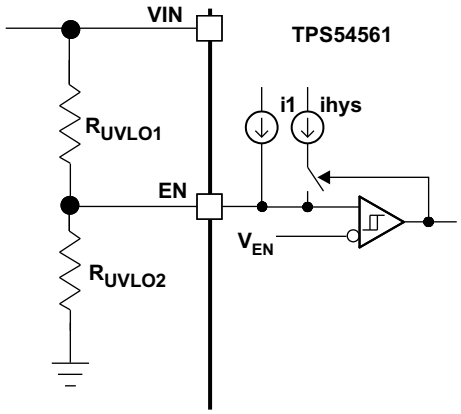


图 7-1. Adjustable Undervoltage Lockout (UVLO)

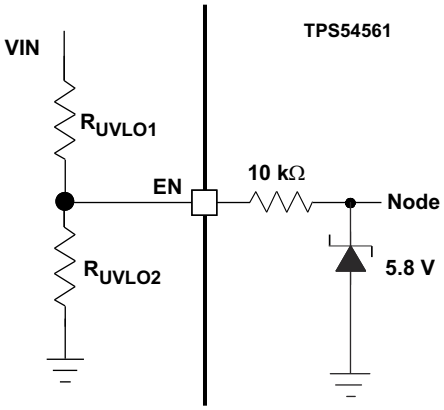


图 7-2. Internal EN Pin Clamp

7.3.8 Soft Start/Tracking Pin (SS/TR)

The TPS54561 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply's reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a soft start time. The TPS54561 has an internal pull-up current source of 1.7 μA that charges the external soft start capacitor. The calculations for the soft start time (10% to 90%) are shown in 方程式 5. The voltage reference (V_{REF}) is 0.8 V and the soft start current (I_{SS}) is 1.7 μA. The soft start capacitor should remain lower than 0.47 μF and greater than 0.47 nF.

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref\ (V) \times 0.8} \tag{5}$$

At power up, the TPS54561 will not start switching until the soft start pin is discharged to less than 54 mV to ensure a proper power up, see 图 7-3.

Also, during normal operation, the TPS54561 will stop switching and the SS/TR must be discharged to 54 mV, when the VIN UVLO is exceeded, EN pin pulled below 1.2 V, or a thermal shutdown event occurs.

The FB voltage will follow the SS/TR pin voltage with a 42-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see 图 6-23). The SS/TR voltage will ramp linearly until clamped at 2.7 V typically as shown in 图 7-3.

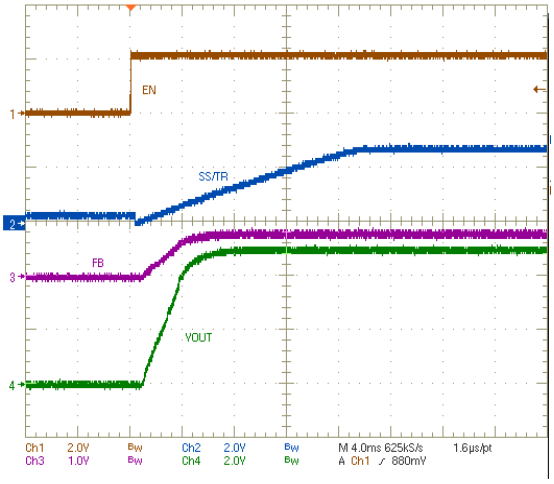


图 7-3. Operation of SS/TR Pin when Starting

7.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins. The sequential method can be implemented using an open drain output of a power on reset pin of another device. The sequential method is illustrated in 图 7-4 using two TPS54561 devices. The power good is Connected to the EN pin on the TPS54561 which will enable the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply will provide a 1-ms start up delay. 图 7-5 shows the results of 图 7-4.

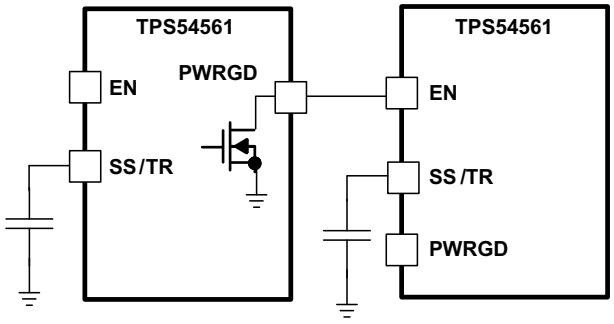


图 7-4. Schematic for Sequential Start-Up Sequence

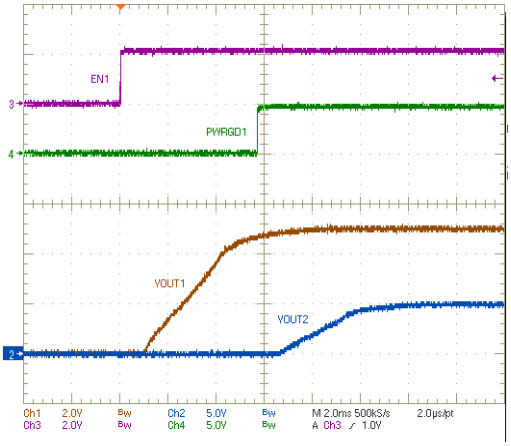


图 7-5. Sequential Startup using EN and PWRGD

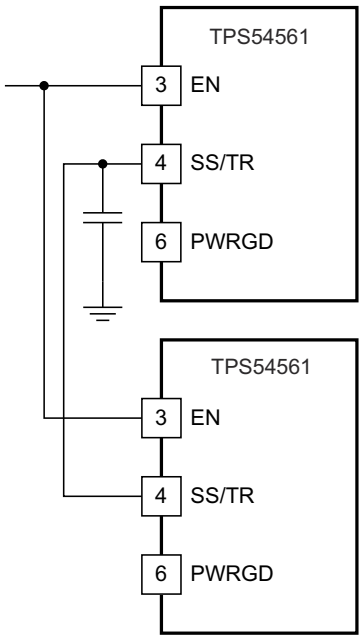


图 7-6. Schematic for Ratio-Metric Start-Up Sequence

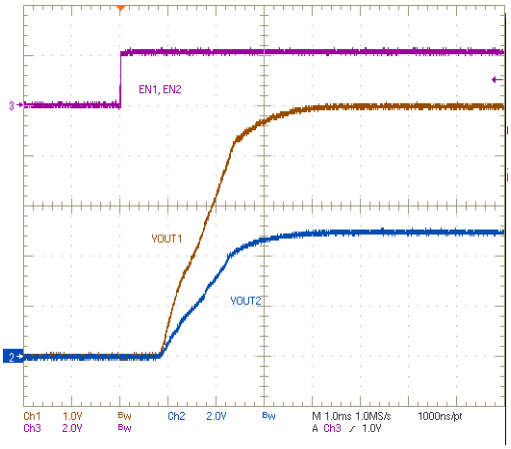


图 7-7. Ratio-Metric Startup using Coupled SS/TR pins

图 7-6 shows a method for ratio-metric start up sequence by connecting the SS/TR pins together. The regulator outputs will ramp up and reach regulation at the same time. When calculating the soft start time the pull up current source must be doubled in 方程式 5. 图 7-7 shows the results of 图 7-6.

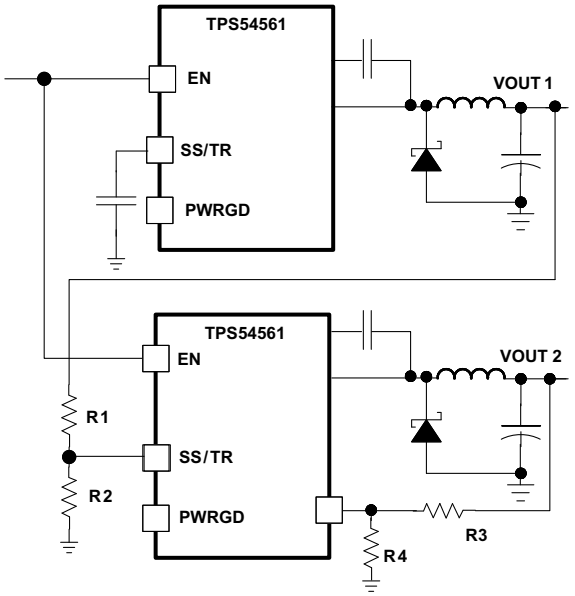


图 7-8. Schematic for Ratio-Metric and Simultaneous Start-Up Sequence

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in 图 7-8 to the output of the power supply that needs to be tracked or another voltage reference source. Using 方程式 6 and 方程式 7, the tracking resistors can be calculated to initiate the Vout2 slightly before, after or at the same time as Vout1. 方程式 8 is the voltage difference between Vout1 and Vout2 at the 95% of nominal output regulation.

The deltaV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to FB offset ($V_{SSOFFSET}$) in the soft start circuit and the offset created by the pullup current source (Iss) and tracking resistors, the $V_{SSOFFSET}$ and I_{SS} are included as variables in the equations.

To design a ratio-metric start up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in 方程式 6 through 方程式 8 for deltaV. 方程式 8 will result in a positive number for applications which the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved.

Since the SS/TR pin must be pulled below 54 mV before starting after an EN, UVLO or thermal shutdown fault, careful selection of the tracking resistors ensures that the device will restart after a fault. The calculated R1 value from 方程式 6 must be greater than the value calculated in 方程式 9 to ensure the device recovers from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage the $V_{SSOFFSET}$ becomes larger as the soft start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 1.5 V for a complete handoff to the internal voltage reference.

$$R1 = \frac{Vout2 + deltaV}{VREF} \times \frac{Vssoffset}{Iss} \tag{6}$$

$$R2 = \frac{VREF \times R1}{Vout2 + deltaV - VREF} \tag{7}$$

$$deltaV = Vout1 - Vout2 \tag{8}$$

$$R1 > 2800 \times Vout1 - 180 \times deltaV \tag{9}$$

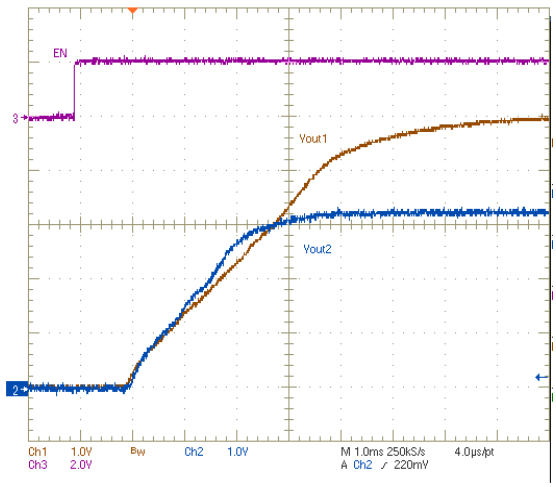


图 7-9. Ratio-Metric Startup with Tracking Resistors

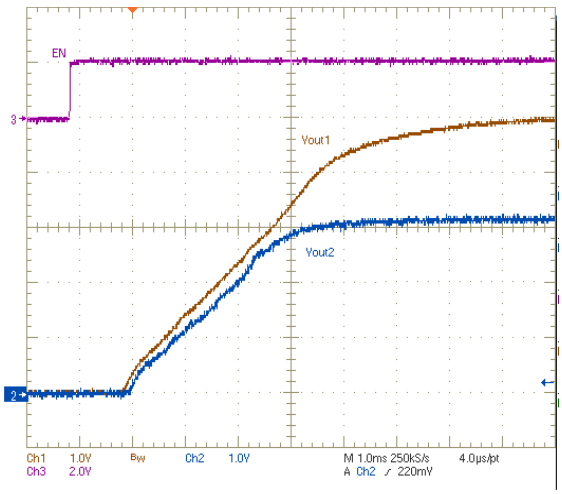


图 7-10. Ratio-Metric Startup with Tracking Resistors

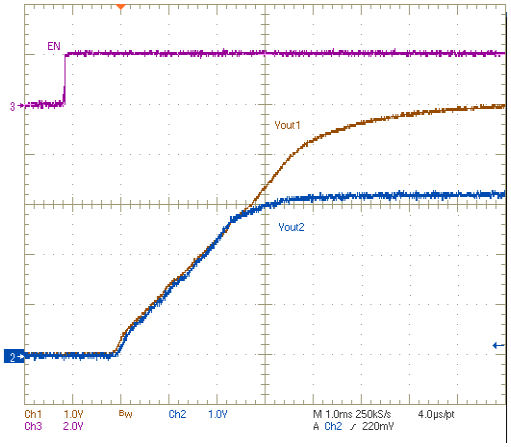


图 7-11. Simultaneous Startup with Tracking Resistor

7.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK) Pin)

The switching frequency of the TPS54561 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use 方程式 10 or 方程式 11 or the curves in 图 6-5 and 图 6-6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 135 ns which limits the maximum operating frequency in applications with high input to output step down ratios. The maximum switching frequency is also limited by the frequency foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$R_T\ (k\Omega) = \frac{101756}{f\text{sw}\ (kHz)^{1.008}} \tag{10}$$

$$f\text{sw}\ (kHz) = \frac{92417}{RT\ (k\Omega)^{0.991}} \tag{11}$$

7.3.11 Maximum Switching Frequency

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54561 implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The TPS54561 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current may exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. 方程式 13 calculates the maximum switching frequency at which the inductor current will remain under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency should not exceed the calculated value.

方程式 12 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output at maximum input voltage.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right) \tag{12}$$

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right) \tag{13}$$

I_O	Output current
I_{CL}	Current limit
R_{dc}	Inductor resistance
V_{IN}	Maximum input voltage
V_{OUT}	Output voltage
$V_{OUT(SC)}$	Output voltage during short
V_d	Diode voltage drop
$R_{DS(on)}$	Switch on resistance
t_{ON}	Controllable on time
f_{DIV}	Frequency divide equals (1, 2, 4, or 8)

7.3.12 Synchronization to RT/CLK Pin

The RT/CLK pin can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature connect a square wave to the RT/CLK pin through either circuit network shown in 图 7-12. The square wave applied to the RT/CLK pin must switch lower than 0.5 V and higher than 2 V and have a pulse width greater than 15 ns. The synchronization frequency range is 160 kHz to 2300 kHz. The rising edge of the SW will be synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed such that the default frequency set resistor is connected from the RT/CLK pin to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor is connected in parallel with an ac coupling capacitor to a termination resistor (that is, 50 Ω) as shown in 图 7-12. The two resistors in series provide the default frequency setting resistance when the signal source is turned off. The sum of the resistance should set the switching frequency close to the external CLK frequency. AC coupling the synchronization signal through a 10-pF ceramic capacitor to RT/CLK pin is recommended.

The first time the RT/CLK is pulled above the PLL threshold the TPS54561 switches from the RT resistor free-running frequency mode to the PLL synchronized mode. The internal 0.5 V voltage source is removed and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 microseconds. During the transition from the PLL mode to the resistor programmed mode, the switching frequency will fall to 150 kHz and then increase or decrease to the resistor programmed frequency when the 0.5-V bias voltage is reapplied to the RT/CLK resistor.

The switching frequency is divided by 8, 4, 2, and 1 as the FB pin voltage ramps from 0 to 0.8 V. The device implements a digital frequency foldback to enable synchronizing to an external clock during normal start-up and fault conditions. 图 7-13, 图 7-14, and 图 7-15 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse skip mode (Eco-Mode).

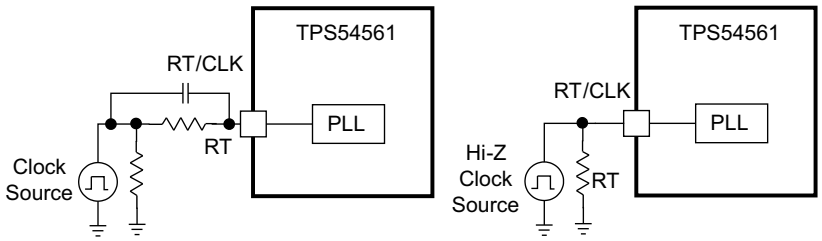


图 7-12. Synchronizing to a System Clock

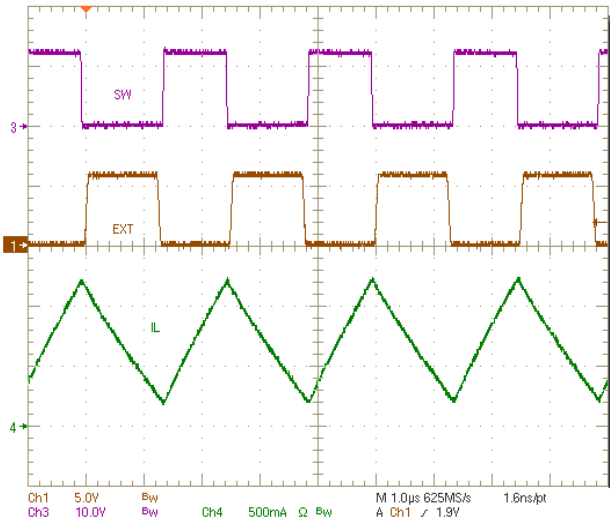


图 7-13. Plot of Synchronizing in CCM

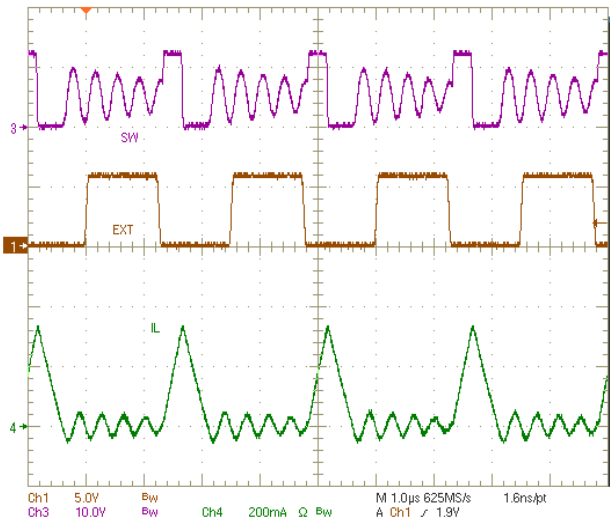


图 7-14. Plot of Synchronizing in DCM

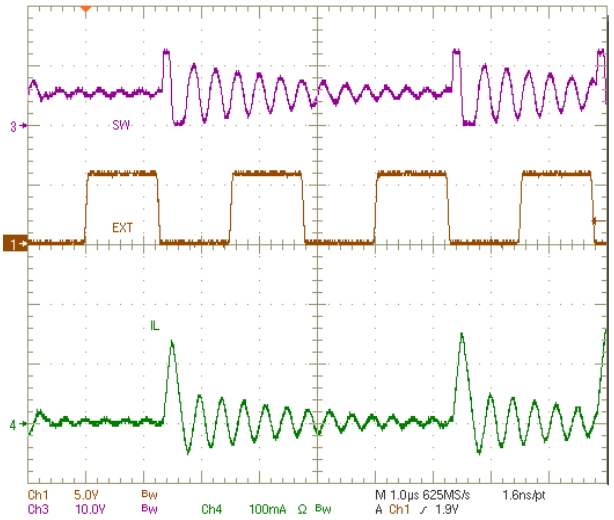


图 7-15. Plot of Synchronizing in Eco-mode

7.3.13 Accurate Current Limit Operation

The TPS54561 implements peak current mode control in which the COMP pin voltage controls the peak current of the high side MOSFET. A signal proportional to the high side switch current and the COMP pin voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP pin high. The error amplifier output is clamped internally at a level which sets the peak switch current limit. The TPS54561 provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay will result in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in 图 7-16.

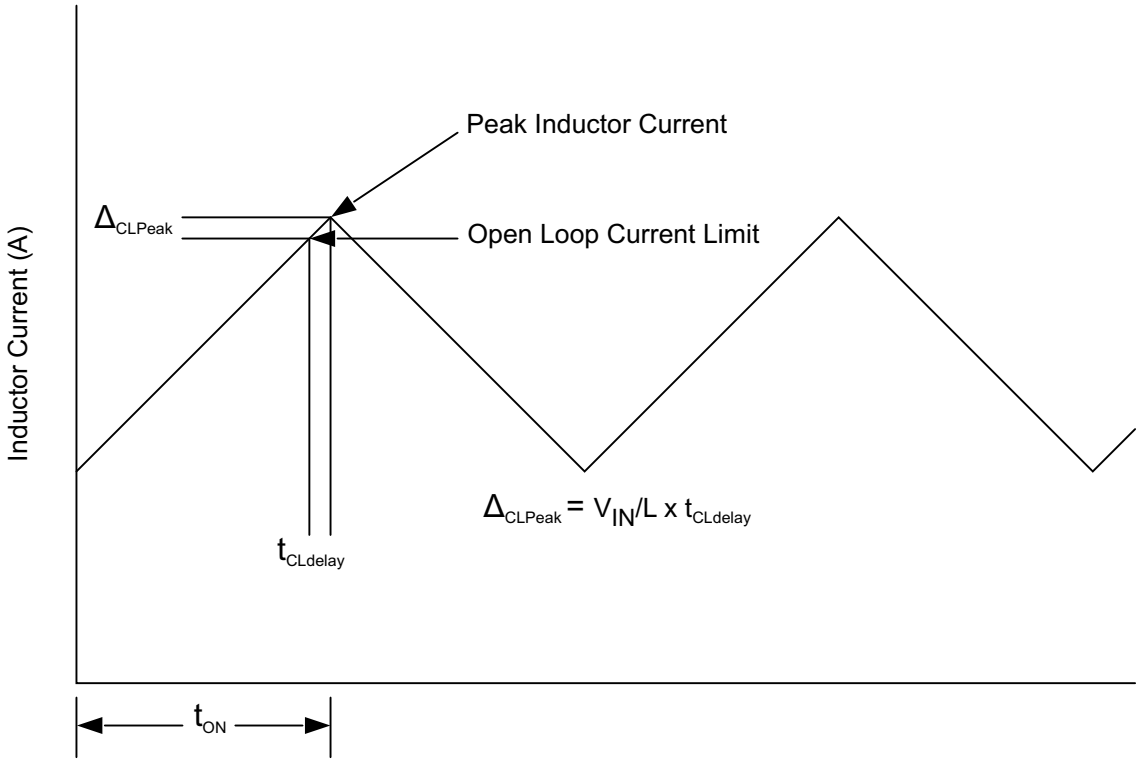


图 7-16. Current Limit Delay

7.3.14 Power Good (PWRGD Pin)

The PWRGD pin is an open drain output. Once the FB pin is between 93% and 106% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. A pull-up resistor of 1 kΩ to a voltage source that is 5.5 V or less is recommended. A higher pull-up resistance reduces the amount of current drawn from the pull-up voltage source when the PWRGD pin is asserted low. A lower pull-up resistance reduces the switching noise seen on the PWRGD signal. The PWRGD is in a defined state once the VIN input voltage is greater than 2 V but with reduced current sinking capability. The PWRGD will achieve full current sinking capability as VIN input voltage approaches 3 V.

The PWRGD pin is pulled low when the FB is lower than 90% or greater than 108% of the nominal internal reference voltage. Also, PWRGD is pulled low, if UVLO or thermal shutdown are asserted or the EN pin pulled low.

7.3.15 Overvoltage Protection

The TPS54561 incorporates an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will increase to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 108% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high side MOSFET resumes normal operation.

7.3.16 Thermal Shutdown

The TPS54561 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power up sequence controlled by discharging the SS/TR pin.

7.3.17 Small Signal Model for Loop Response

图 7-17 shows a simplified equivalent model for the TPS54561 control loop which can be simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 350 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open loop gain and frequency response of the amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a provides the small signal response of the frequency compensation. Plotting a/b provides the small signal response of the overall loop. The dynamic loop response can be evaluated by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode (CCM) operation.

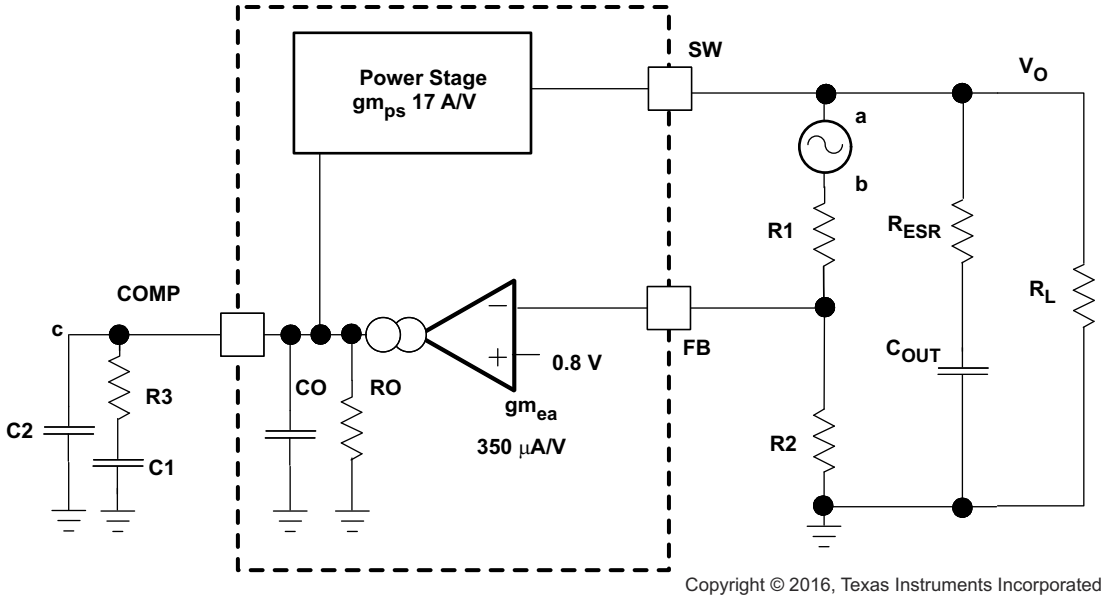


图 7-17. Small Signal Model for Loop Response

7.3.18 Simple Small Signal Model for Peak Current Mode Control

图 7-18 describes a simple small signal model that can be used to design the frequency compensation. The TPS54561 power stage can be approximated by a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in 方程式 14 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in 图 7-17) is the power stage transconductance, gm_{PS}. The gm_{PS} for the TPS54561 is 17 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in 方程式 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see 方程式 16). The combined effect is highlighted by the dashed line in the right half of 图 7-18. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum

electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor (see 方程式 17).

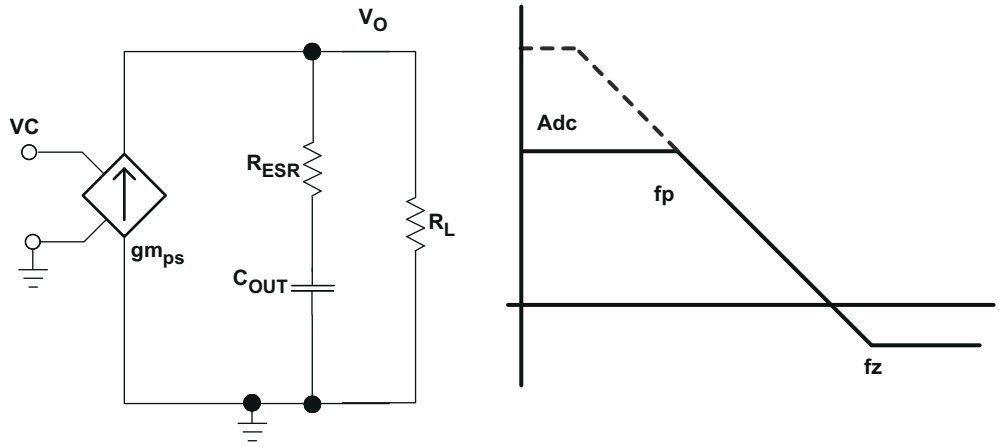


图 7-18. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

7.3.19 Small Signal Model for Frequency Compensation

The TPS54561 uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in 图 7-19. Type 2 circuits are typically implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. 方程式 18 and 方程式 19 relate the frequency response of the amplifier to the small signal model in 图 7-19. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in 图 7-19. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

方程式 18 through 方程式 27 are provided as a reference. An alternative is to use WEBENCH software tools to create a design based on the power supply requirements.

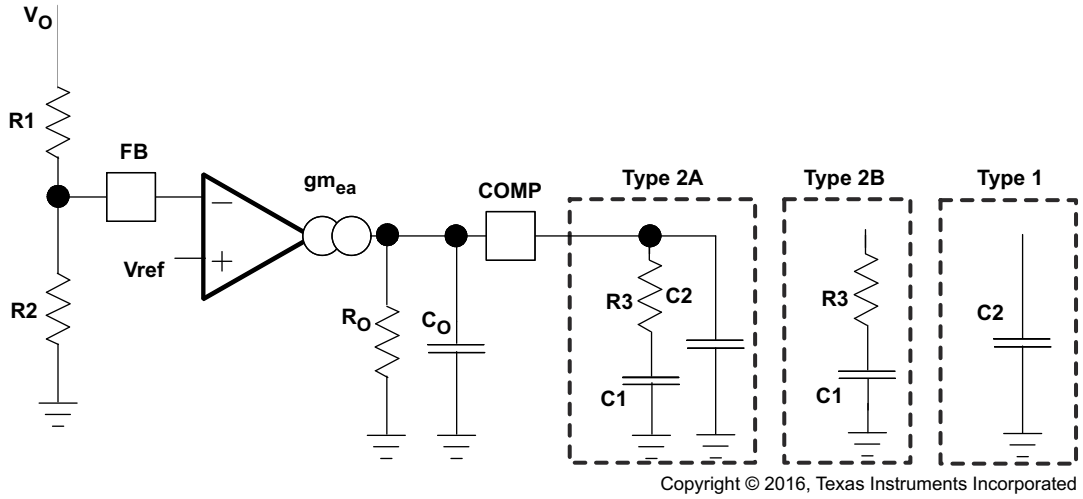


图 7-19. Types of Frequency Compensation

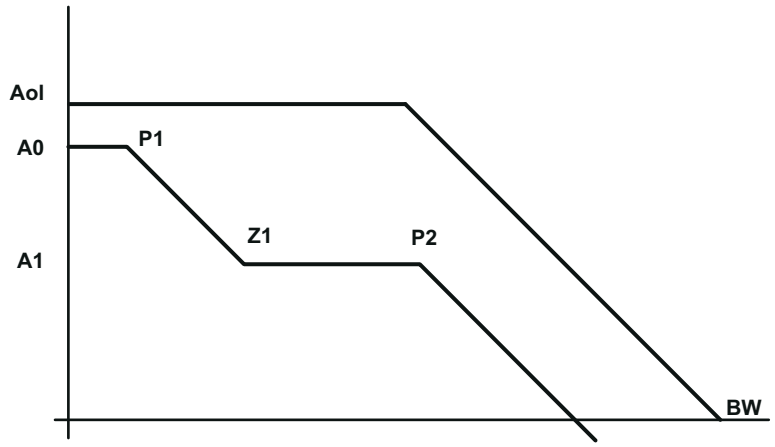


图 7-20. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$Ro = \frac{AoI(V/V)}{gm_{ea}} \tag{18}$$

$$C_O = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \tag{19}$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \tag{20}$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \tag{21}$$

$$A1 = gm_{ea} \times Ro \| R3 \times \frac{R2}{R1 + R2} \tag{22}$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \quad (23)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R_O \times (C2 + C_O)} \text{ type 2a} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R_O \times C_O} \text{ type 2b} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ type 1} \quad (27)$$

7.4 Device Functional Modes

The TPS54561 is designed to operate with input voltages above 4.5 V. When the VIN voltage is above the 4.3 V typical rising UVLO threshold and the EN voltage is above the 1.2 V typical threshold the device is active. If the VIN voltage falls below the typical 4-V UVLO turn off threshold the device stops switching. If the EN voltage falls below the 1.2-V threshold the device stops switching and enters a shutdown mode with low supply current of 2 µA typical.

The TPS54561 will operate in CCM when the output current is enough to keep the inductor current above 0 A at the end of each switching period. As a non-synchronous converter it will enter DCM at low output currents when the inductor current falls to 0 A before the end of a switching period. At very low output current the COMP voltage will drop to the pulse skipping threshold and the device operates in a pulse-skipping Eco-mode. In this mode the high-side MOSFET does not switch every switching period. This operating mode reduces power loss while keeping the output voltage regulated. For more information on Eco-mode see 节 *7.3.3*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS54561 device is a 60-V, 5-A, step-down regulator with an integrated high-side MOSFET. This device typically converts a higher dc voltage to a lower dc voltage with a maximum available output current of 5 A. Example applications are: 12-V, 24-V, and 48-V industrial, automotive and communication power systems. Use the following design procedure to select component values for the TPS54561 device. The Excel® spreadsheet (SLVC452) located on the product page can help on all calculations. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an interactive design procedure and accesses a comprehensive database of components when generating a design.

8.2 Typical Applications

8.2.1 Buck Converter for 7-V to 60-V Input to 5-V at 5-A Output

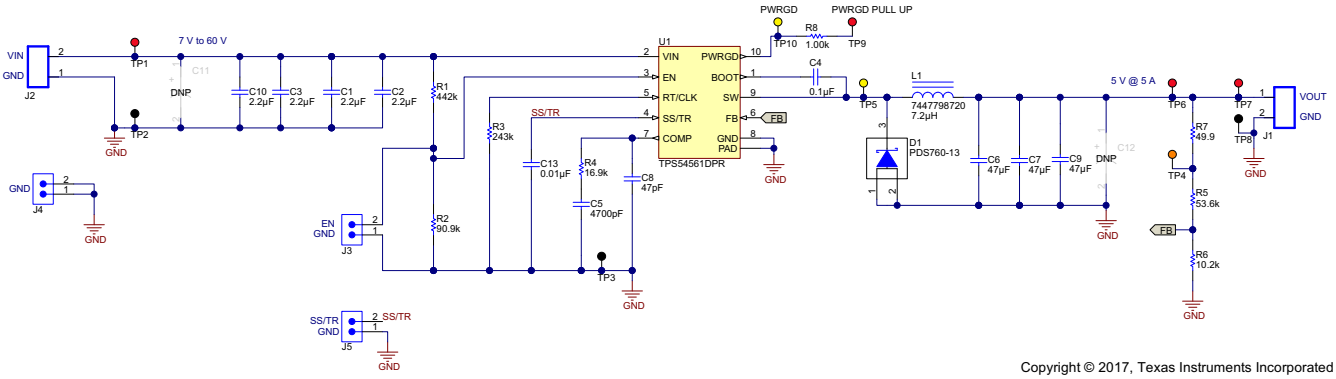


图 8-1. 5-V Output TPS54561 Design Example

8.2.1.1 Design Requirements

图 8-1 illustrates the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. Calculations can be done with the aid of WEBENCH or the excel spreadsheet (SLVC452) located on the product page. This example is designed to the following known parameters:

表 8-1. Design Parameters

PARAMETER	VALUE
Output Voltage	5 V
Transient response 1.25 A to 3.75 A load step	ΔV_{OUT} = 4 %
Maximum output current	5 A
Input voltage	12 V nom. 7 V to 60 V
Output voltage ripple	0.5% of V_{OUT}
Start input voltage (rising VIN)	6.5 V
Stop input voltage (falling VIN)	5 V

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54561 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible since this produces the smallest solution size. High switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage and the frequency foldback protection.

方程式 12 and 方程式 13 should be used to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 135 ns for the TPS54561. For this example, the output voltage is 5 V and the maximum input voltage is 60 V, which allows for a maximum switch frequency up to 708 kHz to avoid pulse skipping from 方程式 12. To ensure overcurrent runaway is not a concern during short circuits use 方程式 13 to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 60 V, assuming a diode voltage of 0.7 V, inductor resistance of 11 mΩ, switch resistance of 87 mΩ, a current limit value of 6 A and short circuit output voltage of 0.1 V, the maximum switching frequency is 855 kHz.

For this design, a lower switching frequency of 400 kHz is chosen to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use 方程式 10 or the curve in 图 6-6. The switching frequency is set by resistor R_3 shown in 图 8-1. For 400-kHz operation, the closest standard value resistor is 243 kΩ.

$$f_{SW(max\,skip)} = \frac{1}{135\ ns} \times \left(\frac{5\ A \times 11\ m\Omega + 5\ V + 0.7\ V}{60\ V - 5\ A \times 87\ m\Omega + 0.7\ V} \right) = 708\ kHz \quad (28)$$

$$f_{SW(shift)} = \frac{8}{135\ ns} \times \left(\frac{6\ A \times 11\ m\Omega + 0.1\ V + 0.7\ V}{60\ V - 6\ A \times 87\ m\Omega + 0.7\ V} \right) = 855\ kHz \quad (29)$$

$$R_T\ (k\Omega) = \frac{101756}{400\ (kHz)^{1.008}} = 242\ k\Omega \quad (30)$$

8.2.1.2.3 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use 方程式 31.

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to

or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be desirable. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Since the inductor ripple current is part of the current mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, it is best to choose relatively large inductor ripple current. This provides sufficienct ripple current with the input voltage at the minimum.

For this design example, K_{IND} = 0.3 and the inductor value is calculated to be 7.6 μH. The nearest standard value is 7.2 μH. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from 方程式 33 and 方程式 34. For this design, the RMS inductor current is 5 A and the peak inductor current is 5.8 A. The chosen inductor is a WE 7447798720, which has a saturation current rating of 7.9 A and an RMS current rating of 6 A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54561 which is nominally 7.5 A.

$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} = \frac{60\ V\ -\ 5\ V}{5\ A\ x\ 0.3} \times \frac{5\ V}{60\ V\ \times\ 400\ kHz} = 7.6\ \mu H \tag{31}$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} = \frac{5\ V\ x\ (60\ V\ -\ 5\ V)}{60\ V\ x\ 7.2\ \mu H\ x\ 400\ kHz} = 1.591\ A \tag{32}$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_O \times f_{SW}} \right)^2} = \sqrt{(5\ A)^2 + \frac{1}{12} \times \left(\frac{5\ V\ \times\ (60\ V\ -\ 5\ V)}{60\ V\ \times\ 7.2\ \mu H\ \times\ 400\ kHz} \right)^2} = 5\ A \tag{33}$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 5\ A + \frac{1.591\ A}{2} = 5.797\ A \tag{34}$$

8.2.1.2.4 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to

supply the difference in current for 2 clock cycles to maintain the output voltage within the specified range. 方程式 35 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, $f$sw is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 1.25 A to 3.75 A. Therefore, ΔI_{OUT} is 3.75 A - 1.25 A = 2.5 A and ΔV_{OUT} = 0.04 × 5 = 0.2 V. Using these numbers gives a minimum capacitance of 62.5 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator cannot sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. A typical load step response is shown in 图 8-6. The excess energy absorbed in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. 方程式 36 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage, and Vi is the initial voltage. For this example, the worst case load step will be from 3.75 A to 1.25 A. The output voltage increases during this load transition and the stated maximum in our specification is 4 % of the output voltage. This makes V_f = 1.04 × 5 = 5.2. Vi is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in 方程式 36 yields a minimum capacitance of 44.1 µF.

方程式 37 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where $f$sw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. 方程式 37 yields 19.9 µF.

方程式 38 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. 方程式 38 indicates the ESR should be less than 15.7 mΩ.

The most stringent criteria for the output capacitor is 62.5 µF required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature and dc bias increases this minimum value. For this example, 3 x 47 µF, 10-V ceramic capacitors with 5 mΩ of ESR will be used. The derated capacitance is 87.4 µF, well above the minimum required capacitance of 62.5 µF.

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. 方程式 39 can be used to calculate the RMS ripple current that the output capacitor must support. For this example, 方程式 39 yields 459 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 2.5\ A}{400\ kHz \times 0.2\ V} = 62.5\ \mu F \tag{35}$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_I)^2\right)} = 7.2\ \mu H \times \frac{\left(3.75\ A^2 - 1.25\ A^2\right)}{\left(5.2\ V^2 - 5\ V^2\right)} = 44.1\ \mu F \tag{36}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{ORIPPLE}}{I_{RIPPLE}}\right)} = \frac{1}{8 \times 400\ kHz} \times \frac{1}{\left(\frac{25\ mV}{1.591\ A}\right)} = 19.9\ \mu F \tag{37}$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{25\ mV}{1.591\ A} = 15.7\ m\Omega \tag{38}$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{5\ V \times (60\ V - 5\ V)}{\sqrt{12} \times 60\ V \times 7.2\ \mu H \times 400\ kHz} = 459\ mA \quad (39)$$

8.2.1.2.5 Catch Diode

The TPS54561 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60 V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the TPS54561.

For the example design, the PDS760 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS760 is 0.52 V at 5 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. 方程式 40 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The PDS760 diode has a junction capacitance of 180 pF. Using 方程式 40, the total loss in the diode at the nominal input voltage is 1.65 Watts.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times Vfd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + Vfd\right)^2}{2} =$$

$$\frac{(12\ V - 5\ V) \times 5\ A \times 0.52\ V}{12\ V} + \frac{180\ pF \times 400\ kHz \times (12\ V + 0.52\ V)^2}{2} = 1.65\ W \quad (40)$$

8.2.1.2.6 Input Capacitor

The TPS54561 requires a high quality ceramic type X5R or X7R input decoupling capacitor with at least 3 μF of effective capacitance. Some applications will benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54561. The input ripple current can be calculated using 方程式 41.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the dc bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 60 V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V. For this example, four 2.2 μF, 100 V capacitors in parallel are used. 表 8-2 shows several choices of high voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 方程式 42. Using the design example values, I_{OUT} = 5 A, C_{IN} = 8.8 µF, $f$sw = 400 kHz, yields an input voltage ripple of 355 mV and a rms input ripple current of 2.26 A.

$$I_{CI(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 5\ A \sqrt{\frac{5\ V}{7\ V} \times \frac{(7\ V - 5\ V)}{7\ V}} = 2.26\ A \tag{41}$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{5\ A \times 0.25}{8.8\ \mu F \times 400\ kHz} = 355\ mV \tag{42}$$

表 8-2. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100 V	X7R	GRM32 series
	1 to 4.7		50 V		
	1	1206	100 V		GRM31 series
	1 to 2.2		50 V		
Vishay	1 to 1.8	2220	50 V		VJ X7R series
	1 to 1.2		100 V		
	1 to 3.9	2225	50 V		
	1 to 1.8		100 V		
TDK	1 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1 to 2.2	1210	100 V		C series C3225
	1 to 3.3		50 V		
AVX	1 to 4.7	1210	50 V		X7R dielectric series
	1		100 V		
	1 to 4.7	1812	50 V		
	1 to 2.2		100 V		

8.2.1.2.7 Slow Start Capacitor

The slow start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54561 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. 方程式 43 can be used to find the minimum slow start time, tss, necessary to charge the output capacitor, Cout, from 10% to 90% of the output voltage, Vout, with an average slow start current of Issavg. In the example, to charge the effective output capacitance of 87 µF up to 5 V with an average current of 1 A requires a 0.3 ms slow start time.

Once the slow start time is known, the slow start capacitor value can be calculated using 方程式 5. For the example circuit, the slow start time is not too critical since the output capacitor value is 3 x 47 µF which does not require much current to charge to 5 V. The example circuit has the slow start time set to an arbitrary value of 3.5 ms which requires a 9.3-nF slow start capacitor calculated by 方程式 44. For this design, the next larger standard value of 10 nF is used.

$$tss > \frac{Cout \times Vout \times 0.8}{Issavg} \quad (43)$$

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref\ (V) \times 0.8} = \frac{3.5\ ms \times 1.7\ \mu A}{(0.8\ V \times 0.8)} = 9.3\ nF \quad (44)$$

8.2.1.2.8 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10 V or higher voltage rating.

8.2.1.2.9 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54561. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 6.5 V (UVLO start). After the regulator starts switching, it should continue to do so until the input voltage falls below 5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor divider of R_{UVLO1} and R_{UVLO2} between Vin and ground connected to the EN pin. 方程式 3 and 方程式 4 calculate the resistance values necessary. For the example application, a 442 kΩ between V_{IN} and EN (R_{UVLO1}) and a 90.9 kΩ between EN and ground (R_{UVLO2}) are required to produce the 6.5 V and 5 V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{6.5\ V - 5\ V}{3.4\ \mu A} = 441\ k\Omega \quad (45)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2\ V}{\frac{6.5\ V - 1.2\ V}{442\ k\Omega} + 1.2\ \mu A} = 90.9\ k\Omega \quad (46)$$

8.2.1.2.10 Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using 方程式 2, R5 is calculated as 53.5 kΩ. The nearest standard 1% resistor is 53.6 kΩ. Due to the input current of the FB pin, the current flowing through the feedback network should be greater than 1 μA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} = 10.2\ k\Omega \times \left(\frac{5\ V - 0.8\ V}{0.8\ V}\right) = 53.5\ k\Omega \quad (47)$$

8.2.1.2.11 Compensation

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual crossover frequency will be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} must be calculated using 方程式 48 and 方程式 49. For C_{OUT}, use a derated value of 87.4 μF. Use equations 方程式 50 and 方程式 51 to estimate a starting point for the crossover frequency, $f$co. For the example design, $f_{p(mod)}$ is 1821 Hz and $f_{z(mod)}$ is 1100 kHz. 方程式 49 is the geometric mean of the modulator pole and the ESR zero and 方程式 51 is the mean of modulator pole and half of the switching frequency. 方程式 50 yields 44.6 kHz and 方程式 51 gives 19.1 kHz. Use the

geometric mean value of 方程式 50 and 方程式 51 for an initial crossover frequency. For this example, after lab measurement, the crossover frequency target was increased to 30 kHz for an improved transient response.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{5\ A}{2 \times \pi \times 5\ V \times 87.4\ \mu F} = 1821\ Hz \quad (48)$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 1.67\ m\Omega \times 87.4\ \mu F} = 1100\ kHz \quad (49)$$

$$f_{co1} = \sqrt{f_{p(mod)} \times f_{z(mod)}} = \sqrt{1821\ Hz \times 1100\ kHz} = 44.6\ kHz \quad (50)$$

$$f_{co2} = \sqrt{f_{p(mod)} \times \frac{f_{SW}}{2}} = \sqrt{1821\ Hz \times \frac{400\ kHz}{2}} = 19.1\ kHz \quad (51)$$

To determine the compensation resistor, R4, use 方程式 52. Assume the power stage transconductance, gmps, is 17 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5 V, 0.8 V, and 350 μA/V, respectively. R4 is calculated to be 16.8 kΩ and a standard value of 16.9 kΩ is selected. Use 方程式 53 to set the compensation zero to the modulator pole frequency. 方程式 53 yields 5172 pF for compensating capacitor C5. 4700 pF is used for this design.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{gmps}\right) \times \left(\frac{V_{OUT}}{V_{REF} \times gmea}\right) = \left(\frac{2 \times \pi \times 29.2\ kHz \times 87.4\ \mu F}{17\ A/V}\right) \times \left(\frac{5V}{0.8\ V \times 350\ \mu A/V}\right) = 16.8\ k\Omega \quad (52)$$

$$C5 = \frac{1}{2 \times \pi \times R4 \times f_{p(mod)}} = \frac{1}{2 \times \pi \times 16.9\ k\Omega \times 1821\ Hz} = 5172\ pF \quad (53)$$

A compensation pole can be implemented if desired by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from 方程式 54 and 方程式 55 for C8 to set the compensation pole. The selected value of C8 is 47 pF for this design example.

$$C8 = \frac{C_{OUT} \times R_{ESR}}{R4} = \frac{87.4\ \mu F \times 1.67\ m\Omega}{16.9\ k\Omega} = 8.64\ pF \quad (54)$$

$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} = \frac{1}{16.9\ k\Omega \times 400\ kHz \times \pi} = 47.1\ pF \quad (55)$$

8.2.1.2.12 Power Dissipation Estimate

The following formulas show how to estimate the TPS54561 power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is operating in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current (P_Q). Example calculations are shown with the 12-V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) = 5\ A^2 \times 87\ m\Omega \times \frac{5\ V}{12\ V} = 0.958\ W \quad (56)$$

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12\ V \times 400\ kHz \times 5\ A \times 4.9\ ns = 0.118\ W \quad (57)$$

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12\ V \times 3nC \times 400\ kHz = 0.014\ W \quad (58)$$

$$P_Q = V_{IN} \times I_Q = 12\ V \times 146\ \mu A = 0.0018\ W \quad (59)$$

Where:

I_{OUT} is the output current (A).
$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
V_{OUT} is the output voltage (V).
V_{IN} is the input voltage (V).
fsw is the switching frequency (Hz).
t_{rise} is the SW pin voltage rise time and can be estimated by trise = V_{IN} x 0.16 ns/V + 3 ns
Q_G is the total gate charge of the internal MOSFET
I_Q is the operating nonswitching supply current

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.958\ W + 0.118\ W + 0.014\ W + 0.0018\ W = 1.092\ W \quad (60)$$

For given T_A,

$$T_J = T_A + R_{TH} \times P_{TOT} \quad (61)$$

For given T_{JMAX} = 150°C

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT} \quad (62)$$

Where:

P_{tot} is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
R_{TH} is the thermal resistance from junction to ambient for a given PCB layout (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and PCB trace resistance impacting the overall efficiency of the regulator.

8.2.1.2.13 Safe Operating Area

The safe operating area (SOA) of a typical design is shown in 图 8-2, through 图 8-5 for 3.3-V, 5-V and 12-V outputs and varying amounts of forced air flow. The temperature derating curves represent the conditions at which the internal components and external components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a double-sided PCB with 2 oz. copper, similar to the EVM. Careful attention must be paid to the other components chosen for the design, especially the catch diode. In most applications the thermal performance will be limited by the catch diode. When operating with high duty cycles, higher input voltage or at higher switching frequency the TPS54561's thermal performance can become the limiting factor.

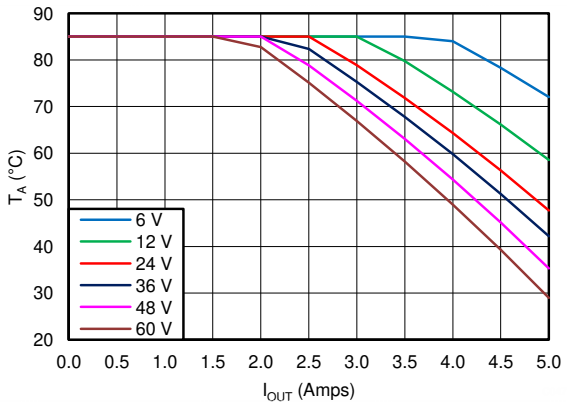


图 8-2. 3.3-V Output with 400-kHz Switching Frequency

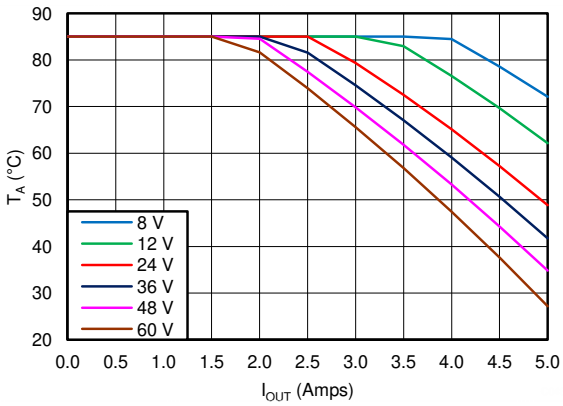


图 8-3. 5-V Output with 400-kHz Switching Frequency

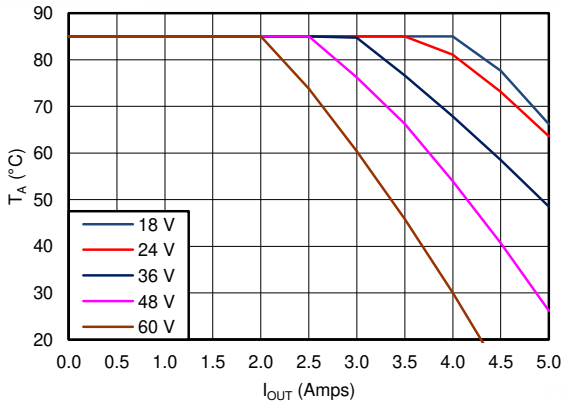
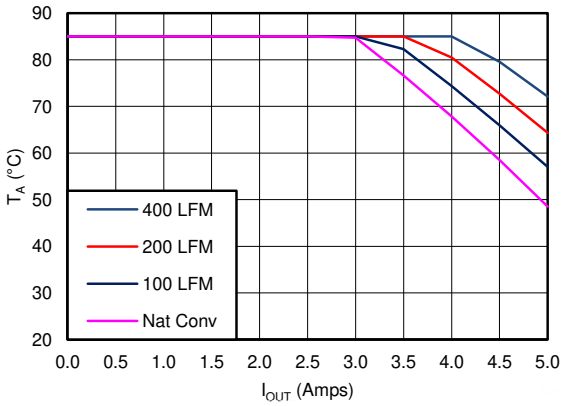


图 8-4. 12-V Output with 800-kHz Switching Frequency



V_{IN} = 36 V V_O = 12 V fsw = 800 kHz

图 8-5. Air Flow Conditions

8.2.1.2.14 Discontinuous Conduction Mode and Eco-mode Boundary

With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 410 mA. The power supply enters Eco-mode when the output current is lower than 25 mA. The input current draw is 280 μA with no load.

8.2.1.3 Application Curves

Measurements are taken with standard EVM using a 12-V input, 5-V output, and 5-A load unless otherwise noted.

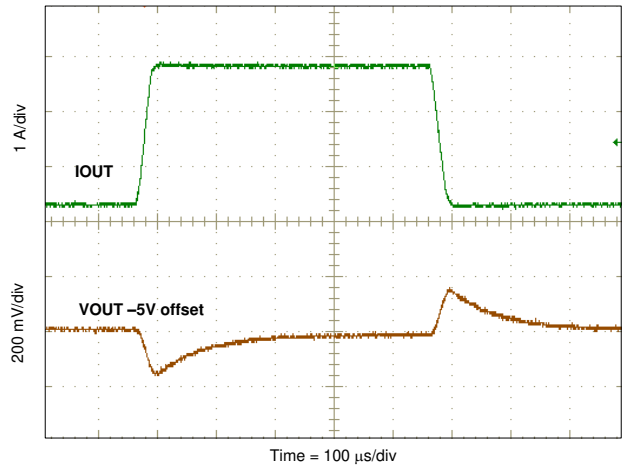


图 8-6. Load Transient

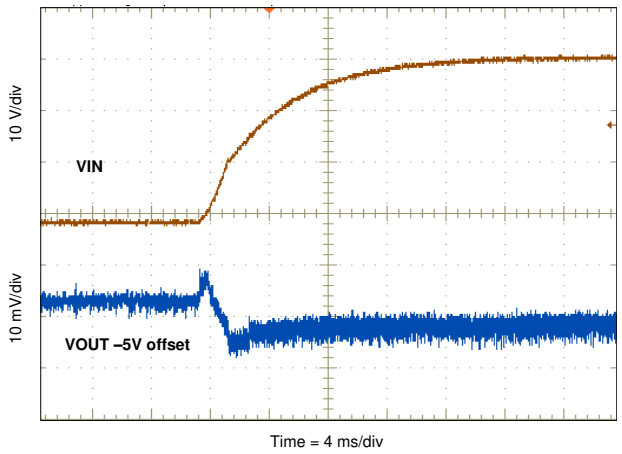


图 8-7. Line Transient (8 V to 40 V)

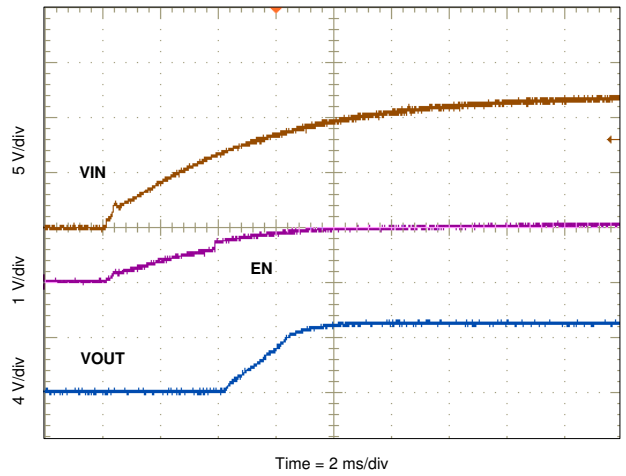


图 8-8. Start-up With VIN

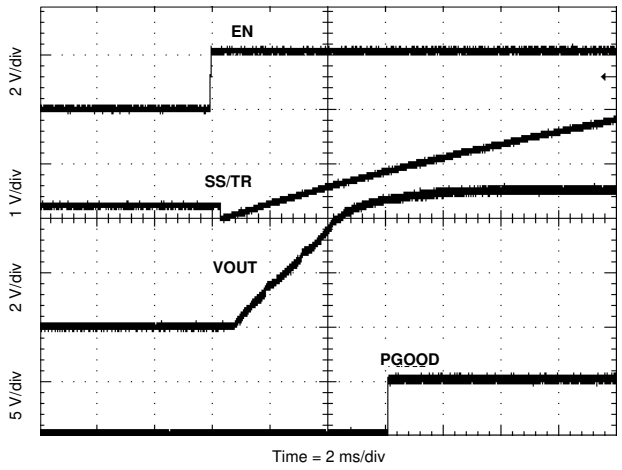


图 8-9. Start-up With EN

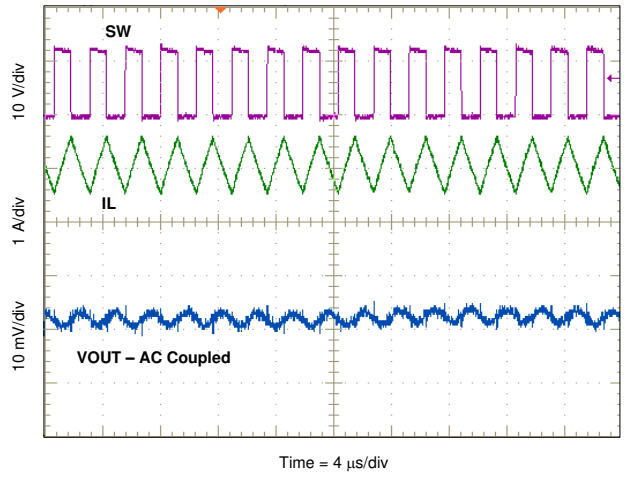


图 8-10. Output Ripple CCM

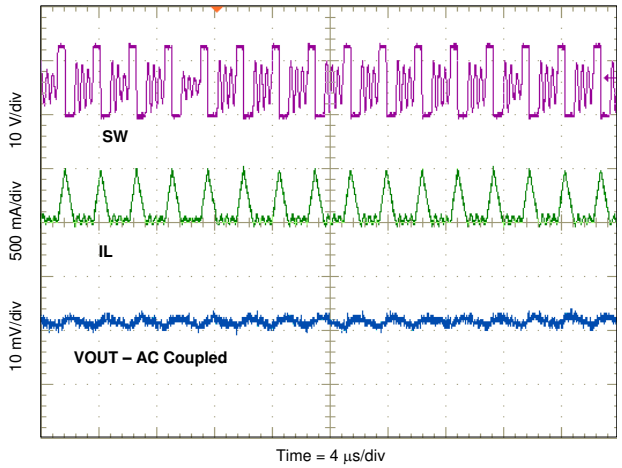


图 8-11. Output Ripple DCM

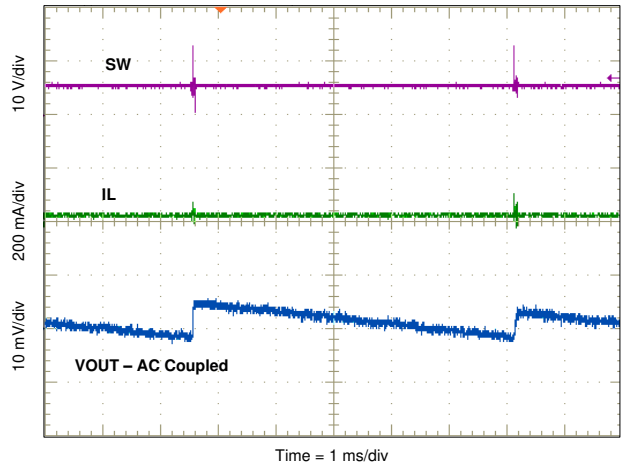


图 8-12. Output Ripple PSM

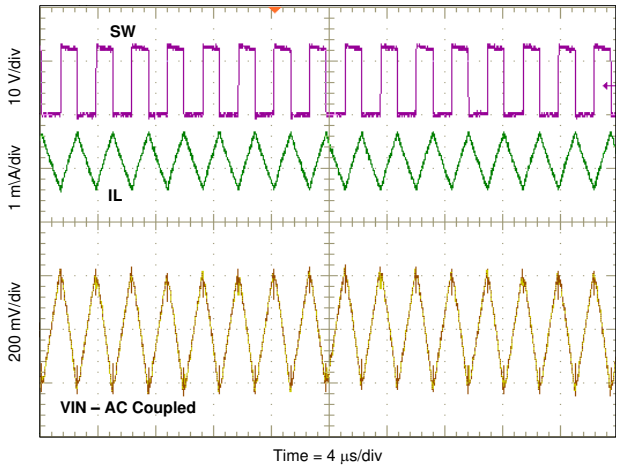


图 8-13. Input Ripple CCM

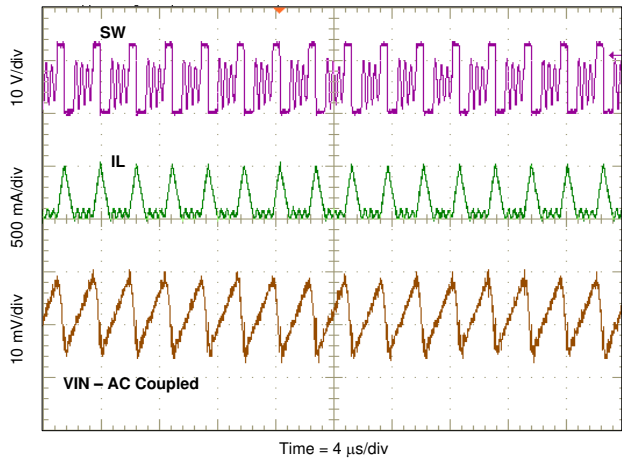


图 8-14. Input Ripple DCM

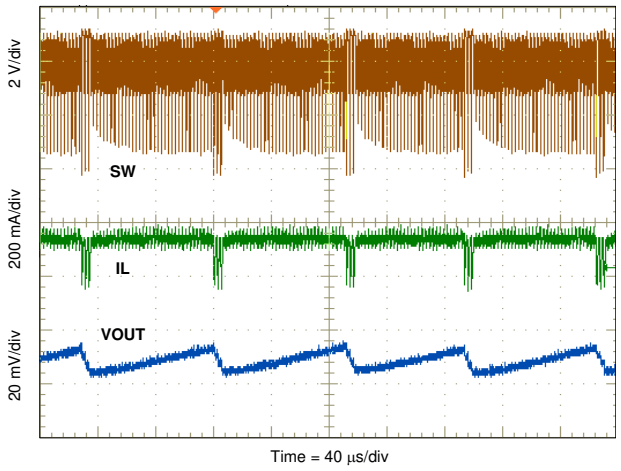


图 8-15. Low Dropout Operation

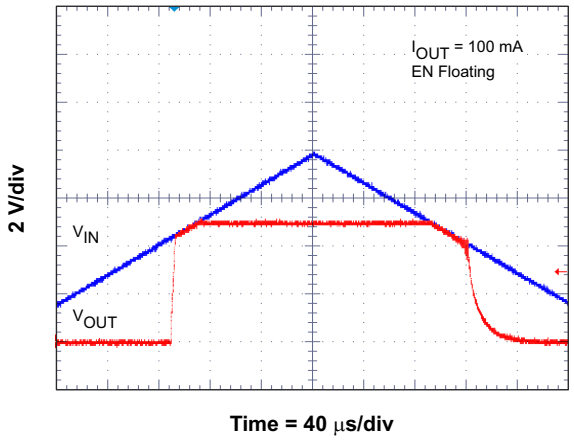


图 8-16. Low Dropout Operation

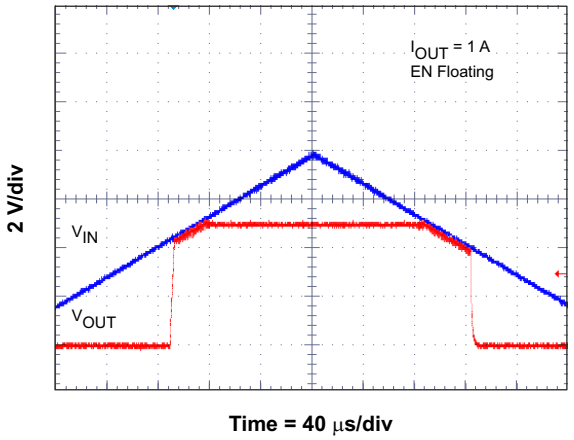


图 8-17. Low Dropout Operation

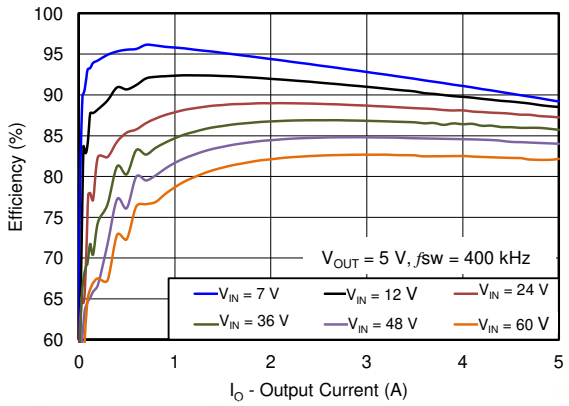


图 8-18. Efficiency vs Load Current

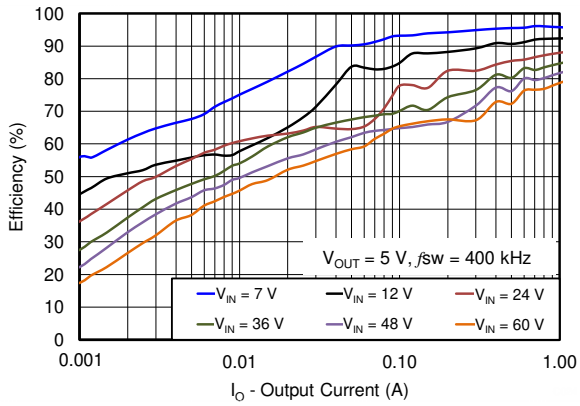


图 8-19. Light Load Efficiency

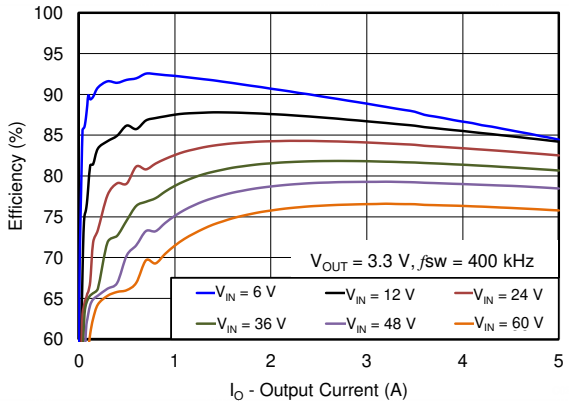


图 8-20. Efficiency vs Load Current

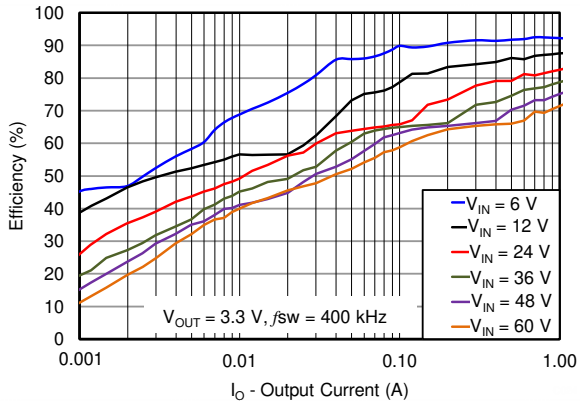
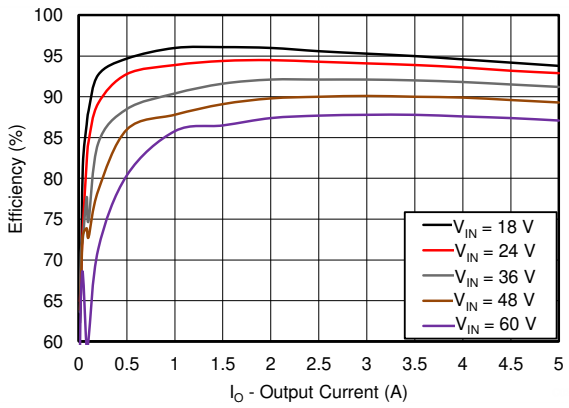


图 8-21. Light Load Efficiency



V_{OUT} = 12 V fsw = 800 kHz

图 8-22. Efficiency vs Output Current

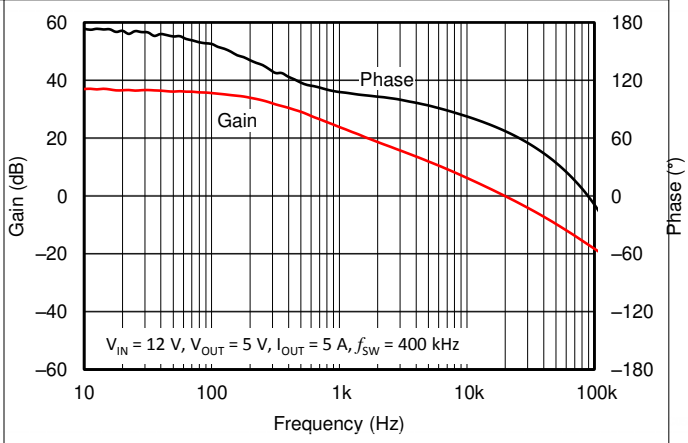


图 8-23. Overall Loop Frequency Response

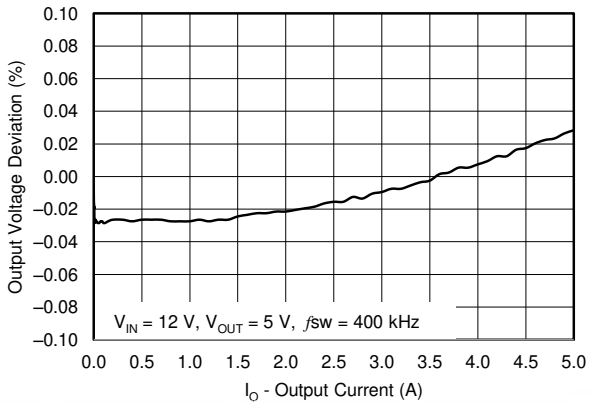


图 8-24. Regulation vs Load Current

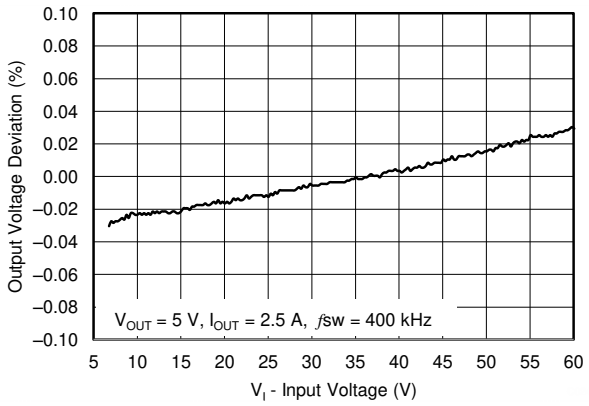


图 8-25. Regulation vs Input Voltage

8.2.2 Inverting Buck-Boost Topology for Positive Input to Negative Output

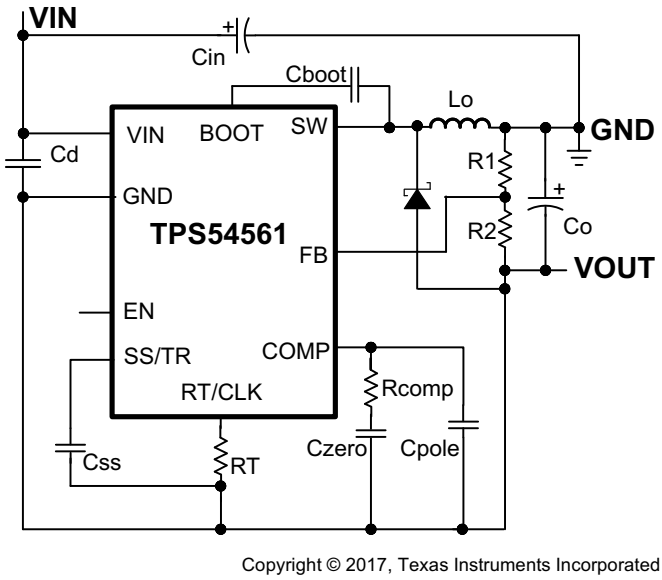


图 8-26. TPS54561 Inverting Power Supply From Application Note

8.2.3 Split-Rail Topology for Positive Input to Negative and Positive Output

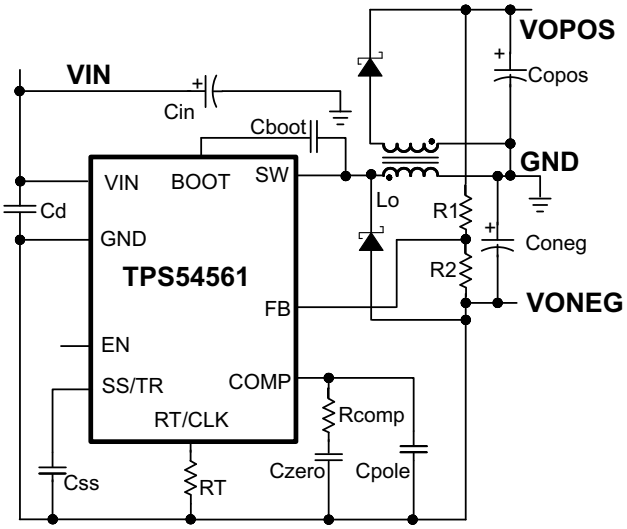


图 8-27. TPS54561 Split Rail Power Supply Based on the Application Note

9 Power Supply Recommendations

The design of the device is for operation from an power supply range between 4.5 V and 60 V. Good regulation of this power supply is essential. If the power supply is more distant than a few inches from the TPS54561 converter, the circuit may require additional bulk capacitance besides the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. To reduce parasitic effects, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See 图 10-1 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC.

The thermal pad should be connected to internal PCB ground planes using multiple vias directly under the IC. The SW pin should be routed to the cathode of the catch diode and to the output inductor. Since the SW connection is the switching node, the catch diode and output inductor should be located close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

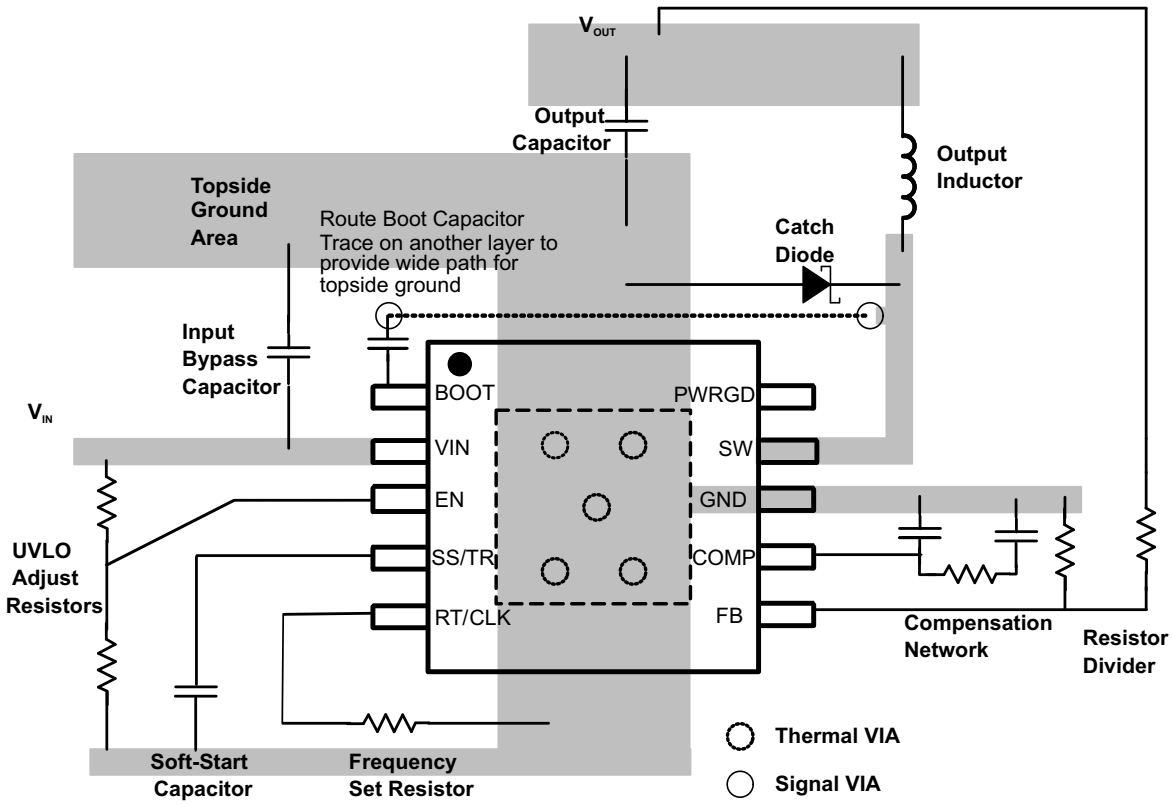


图 10-1. PCB Layout Example

10.3 Estimated Circuit Area

Boxing in the components in the design of 图 8-1 the estimated printed circuit board area is 1.025 in^2 (661 mm^2). This area does not include test points or connectors.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For the TPS54560, TPS54561, and TPS54561-Q1 family Excel design tool, see SLVC452.

11.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54561 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Create an Inverting Power Supply From a Step-Down Regulator,* SLVA317
- *Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator,* SLVA369
- *Evaluation Module for the TPS54561 Step-Down Converter,* SLVU993
- *Creating a Universal Car Charger for USB Devices From the TPS54240 and TPS2511,* SLVA464
- *Creating GSM /GPRS Power Supply from TPS54260,* SLVA412)

11.3 接收文档更新通知

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11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54561DPRR	ACTIVE	WSON	DPR	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 54561	Samples
TPS54561DPRT	ACTIVE	WSON	DPR	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 54561	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS54561 :

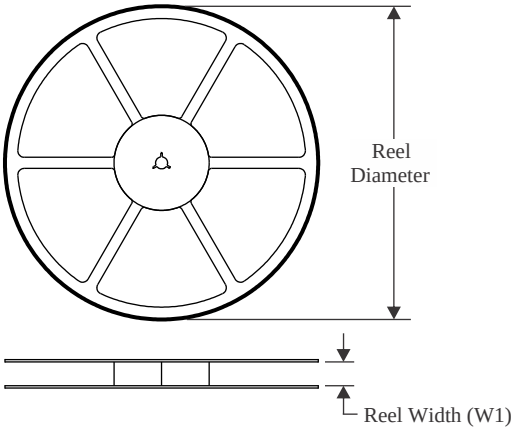
- Automotive : TPS54561-Q1

NOTE: Qualified Version Definitions:

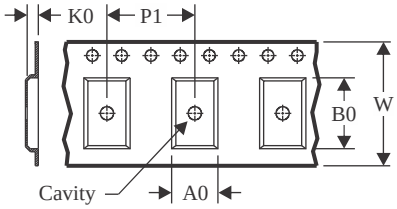
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

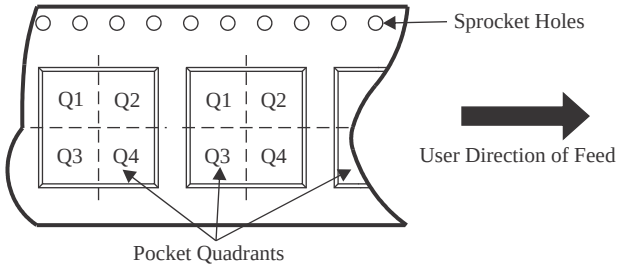


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

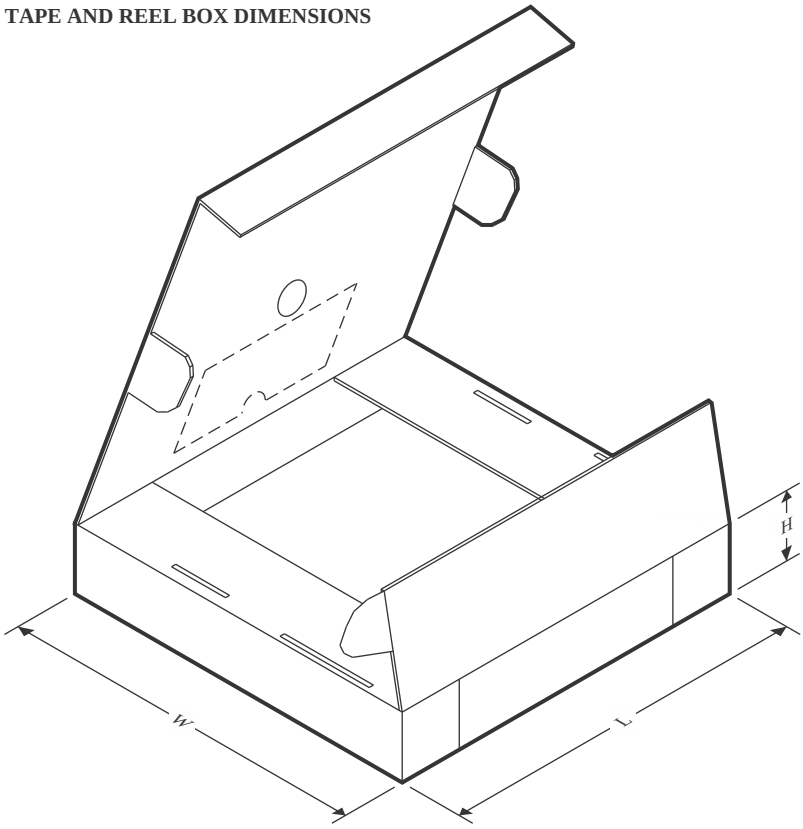
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54561DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54561DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

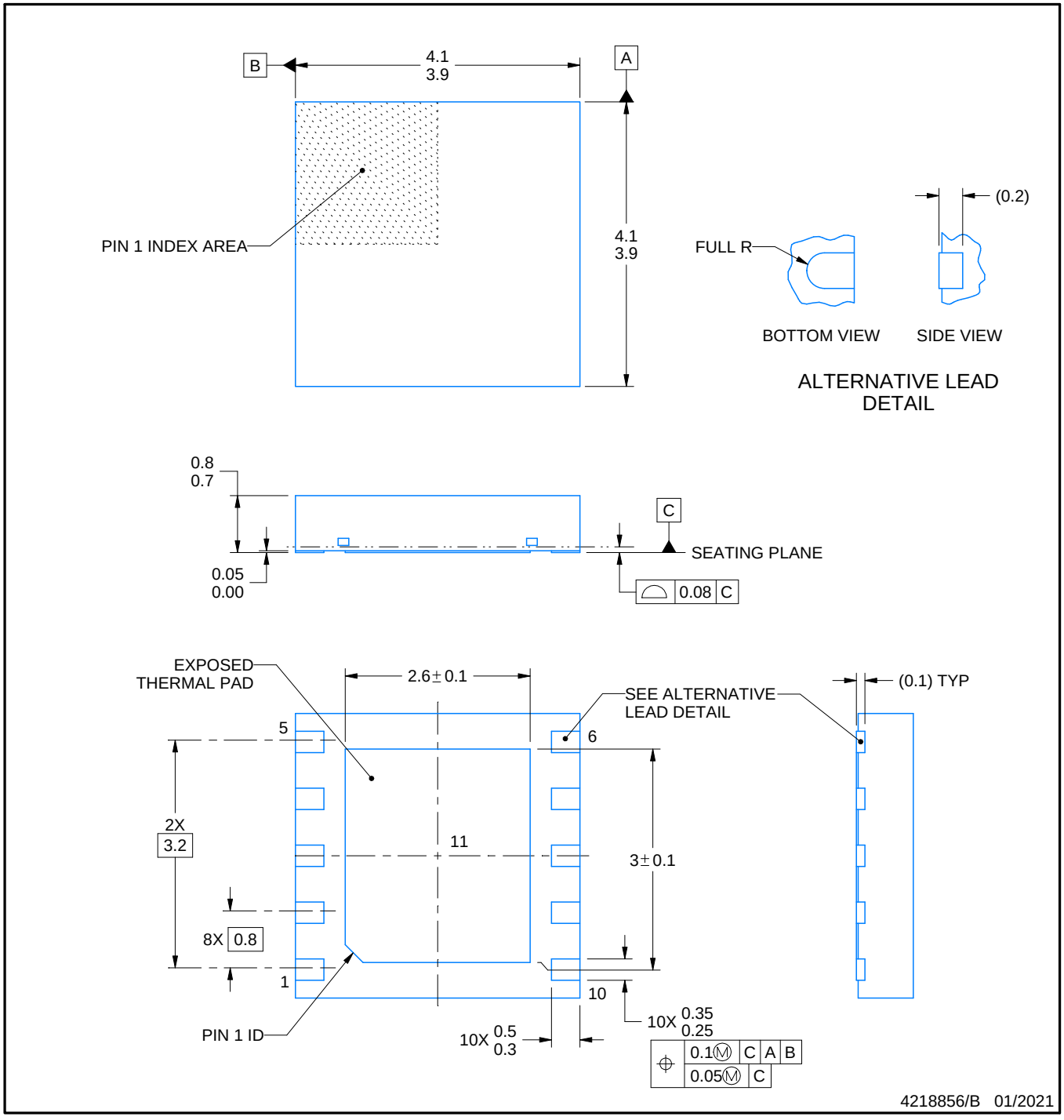
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54561DPRR	WSON	DPR	10	3000	346.0	346.0	33.0
TPS54561DPRT	WSON	DPR	10	250	182.0	182.0	20.0

PACKAGE OUTLINE

DPR0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

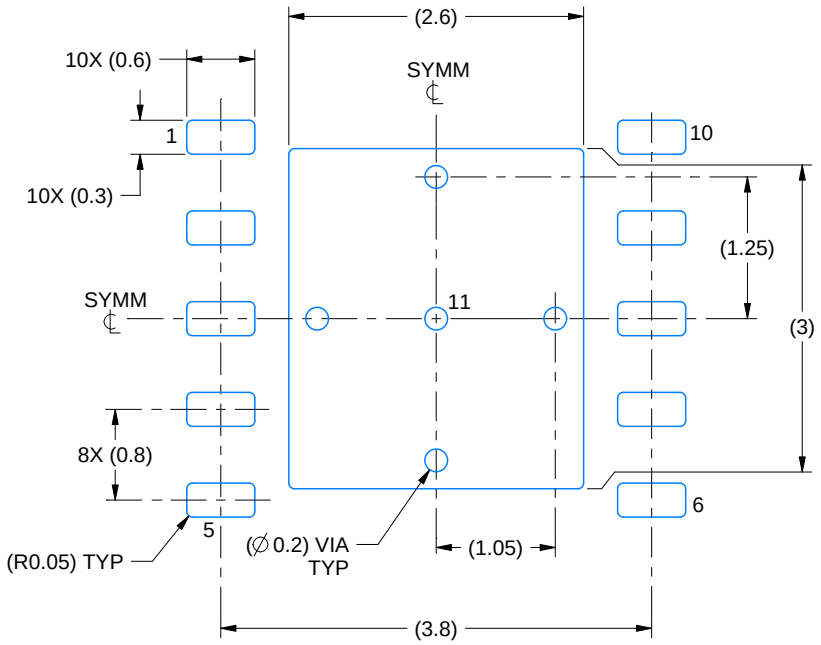
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

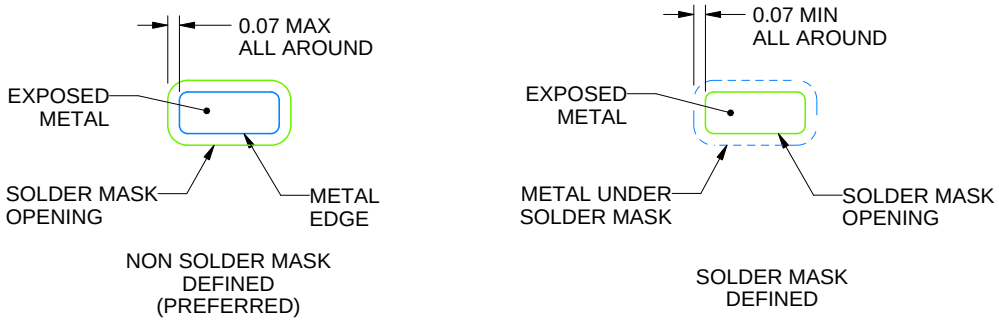
DPR0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

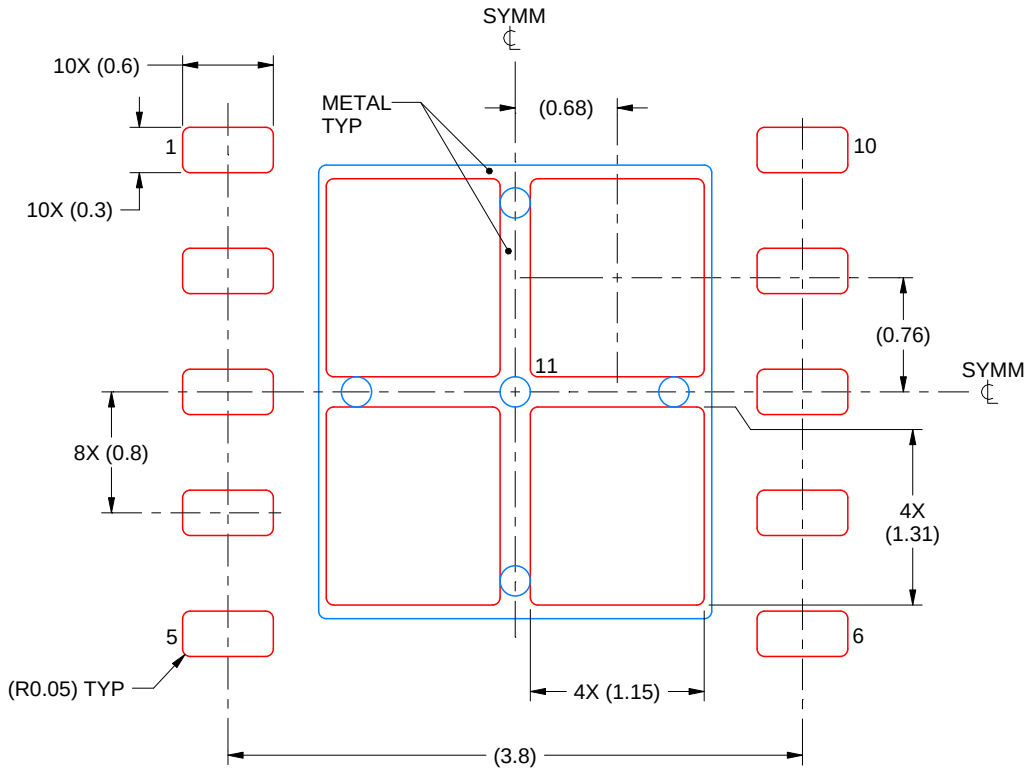
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPR0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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