TPS6594-Q1 Power Management IC (PMIC) for Processors with 5 Bucks and 4 LDOs

1 器件概述

1.1 特性

- 符合汽车类 应用要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：–40°C 至 +125°C 的环境工作温度范围
  - 器件 HBM 分类等级 2
  - 器件 CDM 分类等级 C4A
- SafeTI ™半导体组件
  - 设计用于功能安全 应用
  - 根据 ISO 26262 标准的要求开发
  - 支持 ASIL-D 系统 (SEooC)
  - 输入电源监控和过压保护
  - 窗口式电压和过流监控器
  - 集成式 Q&A 或触发模式看门狗模块
  - 双通道或 PWM 错误信号监控 (ESM) 支持具有集成式安全 MCU 的处理器
  - 具有高温报警和热关断功能的温度监控
  - 带有运行或保持上电序列以及复位释放选项的 NVM 位完整性错误检测
- 低功耗
  - 关断电流典型值为 2µA
  - 在仅备用电源模式下典型值为 7µA
  - 在低功耗待机模式下典型值为 20µA
- 五个降压开关模式电源降压稳压器：
  - 输入电压范围：2.8V 至 5.5V
  - 输出电压范围：0.3V 至 3.34V（电压阶跃为 5mV、10mV 或 20mV）
  - 四个降压稳压器电流为 3.5A，单轨的灵活多相拉电流高达 14A。其中一个降压稳压器单相电流为 4A
  - 一个降压稳压器电流为 2A
  - 具有短路和过流保护
  - 内部软启动可限制浪涌电流
  - 开关频率为 2.2MHz/4.4MHz
  - 可与外部时钟输入同步
- 三个具有可配置旁路模式的低压降 (LDO) 线性稳压器
  - LDO 模式下的输入电压范围：1.2V 至 5.5V
  - 旁路模式下的输入电压范围：1.7V 至 3.6V
  - 输出电压范围：0.6V 至 3.3V（电压阶跃为 50mV）
  - 具有 500mA 电流、短路和过流保护
- 一个具有低噪声的低压降 (LDO) 线性稳压器
  - 输入电压范围：2.2V 至 5.5V
  - 输出电压范围：1.2V 至 3.3V（电压阶跃为 25mV）
  - 具有 300mA 电流、短路和过流保护
- 电源序列控制：
  - 可配置上电和断电序列 (NVM)
  - 睡眠和激活状态转换之间的可配置序列 (NVM)
  - 数字输出信号可添加至启动序列
- 32kHz 晶体振荡器，可输出缓冲式 32kHz 时钟输出
- 具有警报和定期唤醒机制的实时时钟 (RTC)
- 具有一个 SPI 或两个 I^2C 控制接口，且第二个 I^2C 接口专用于 Q&A 看门狗通信
- 封装选项：
  - 8mm × 8mm 56 引脚 VQFNP，间距为 0.5mm

1.2 应用

- 汽车信息娱乐系统和数字仪表组
- 汽车高级驾驶辅助系统 (ADAS)
- 汽车导航系统
- 汽车远程信息处理
- 工业控制和自动化

1.3 说明

TPS6594-Q1 是一款适用于汽车和工业 应用的集成式电源管理器件。该器件提供五个降压转换器，其中四个是灵活多相可配置降压转换器，每相电流为 3.5A；另一个降压转换器的电流为 2A。所有降压转换器均可与内部 2.2MHz 或 4.4MHz 时钟信号和外部 1MHz、2MHz 或 4MHz 时钟信号同步。为改善该器件的 EMC 性能，可对同步的降压开关时钟信号进行集成式扩频调制，也可通过 GPIO 输出引脚对外部器件进行集成式扩频调制。该器件提供四个 LDO，其中三个可配置为负载开关，电流为 500mA；另一个电流为 300mA，具有低噪声。

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非易失性存储器 (NVM) 用于控制默认的电源序列和诸如输出电压和 GPIO 配置等默认配置。NVM 经过出厂编程，无需外部编程即可启动。多数默认静态设置可通过 SPI 或 I^2C 寄存器进行更改，从而根据多种不同系统需求配置器件。在安全功能方面，NVM 还具备比特完整性错误检测功能，可在检测到错误时停止上电序列，防止系统在未知状态下启动。

TPS6594-Q1 包含 32kHz 晶体振荡器，为集成式 RTC 模块提供精确的 32kHz 时钟。备用电池管理功能可在主电源发生功率损耗时，利用纽扣电池或超级电容为晶体振荡器和 RTC 模块供电。

TPS6594-Q1 器件包含可监控软件锁定情况的 Q&A 看门狗，以及可监控随附 SoC 或 MCU 所产生错误信号且具有故障注入选项的 2 个系统错误监控输入。该器件还具有保护和诊断机制，如短路保护、热监测和关断。PMIC 可通过中断处理程序向处理器报告这些事件，以便处理器采取相关措施进行响应。

表 1-1. 器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS6594-Q1	VQFNP (56)	8.00mm x 8.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

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1.4 功能图

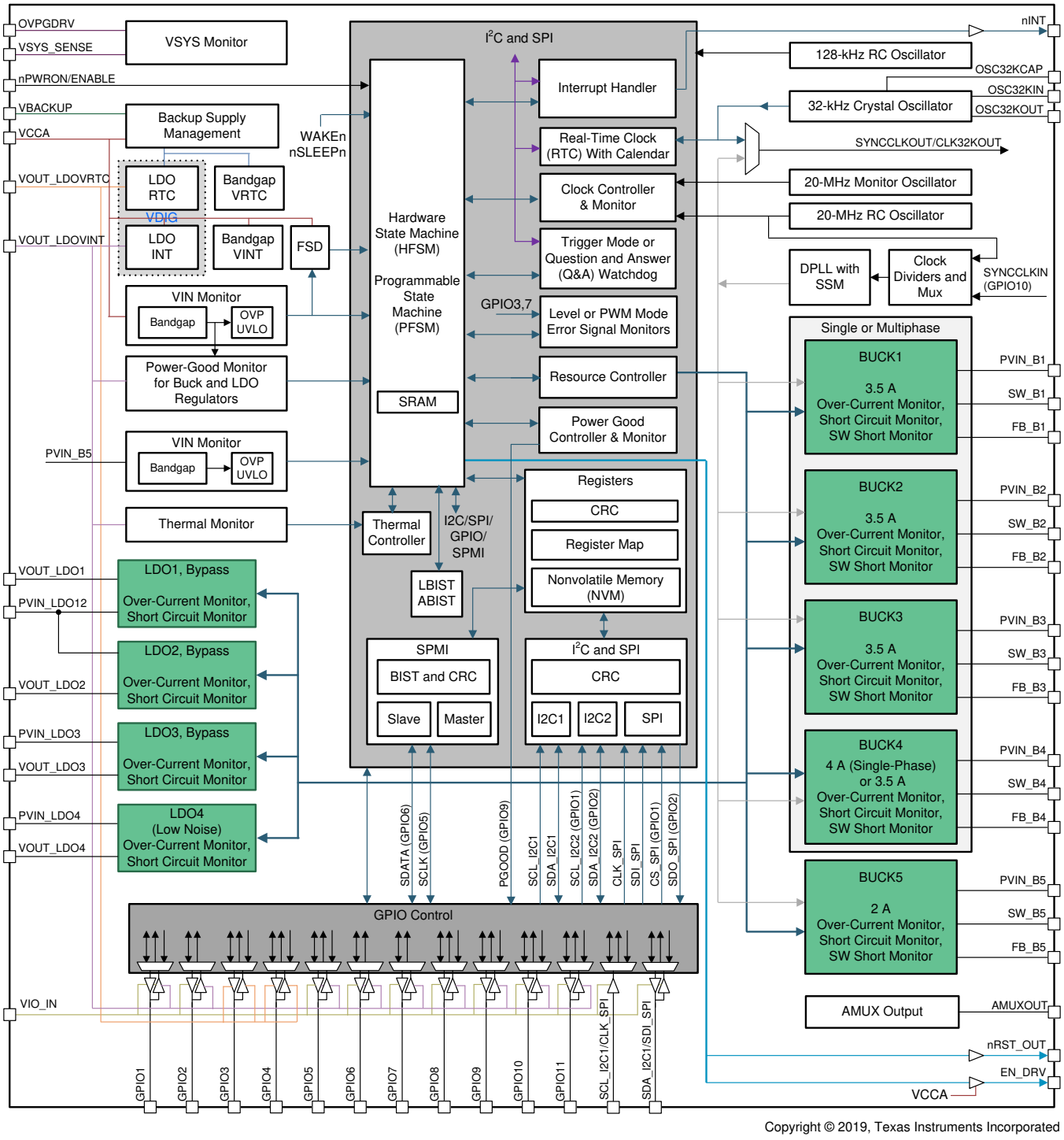

图 **1-1.** 功能图

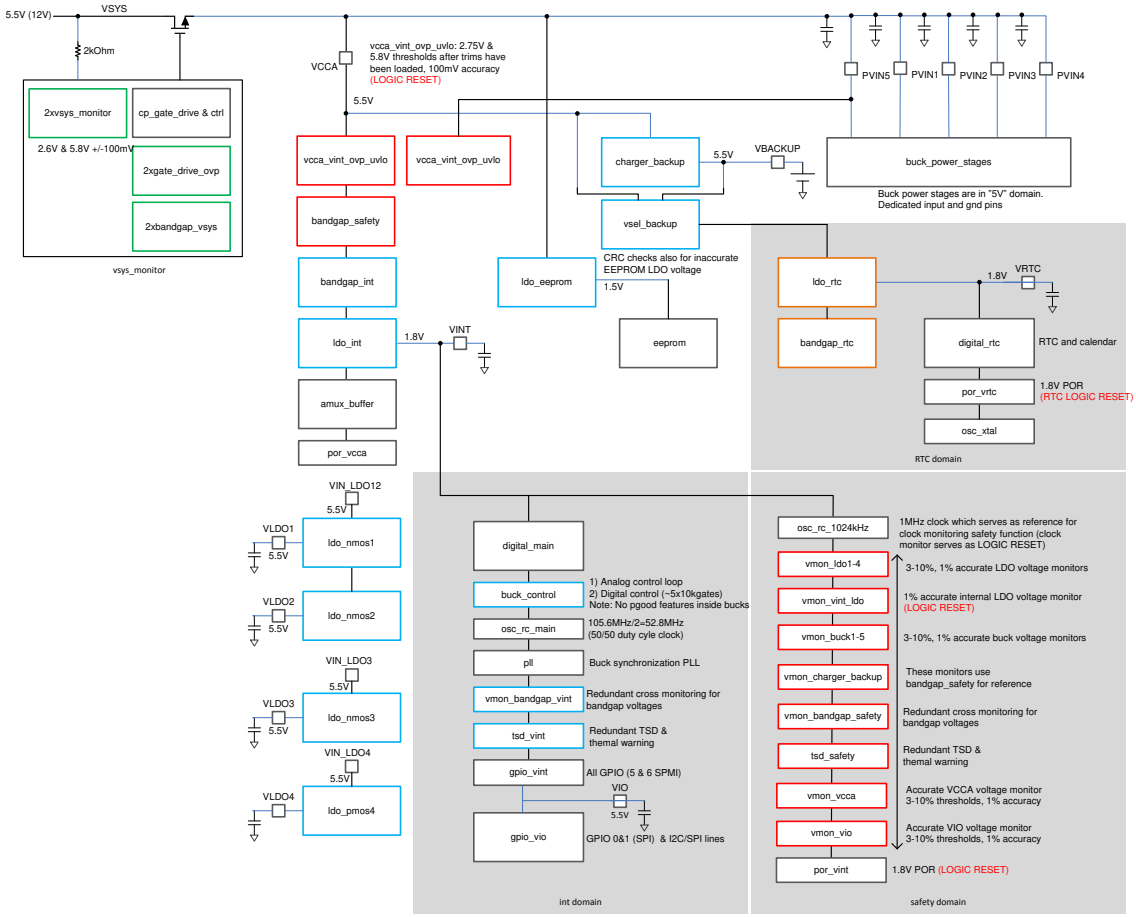

图 **1-2.** 内部电源树图

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 11 月	*	初始发行版。

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3 Pin Configuration and Functions

Figure 3-1 shows the 56-pin RWE plastic quad-flatpack no-lead (VQFN) pin assignments and thermal pad.

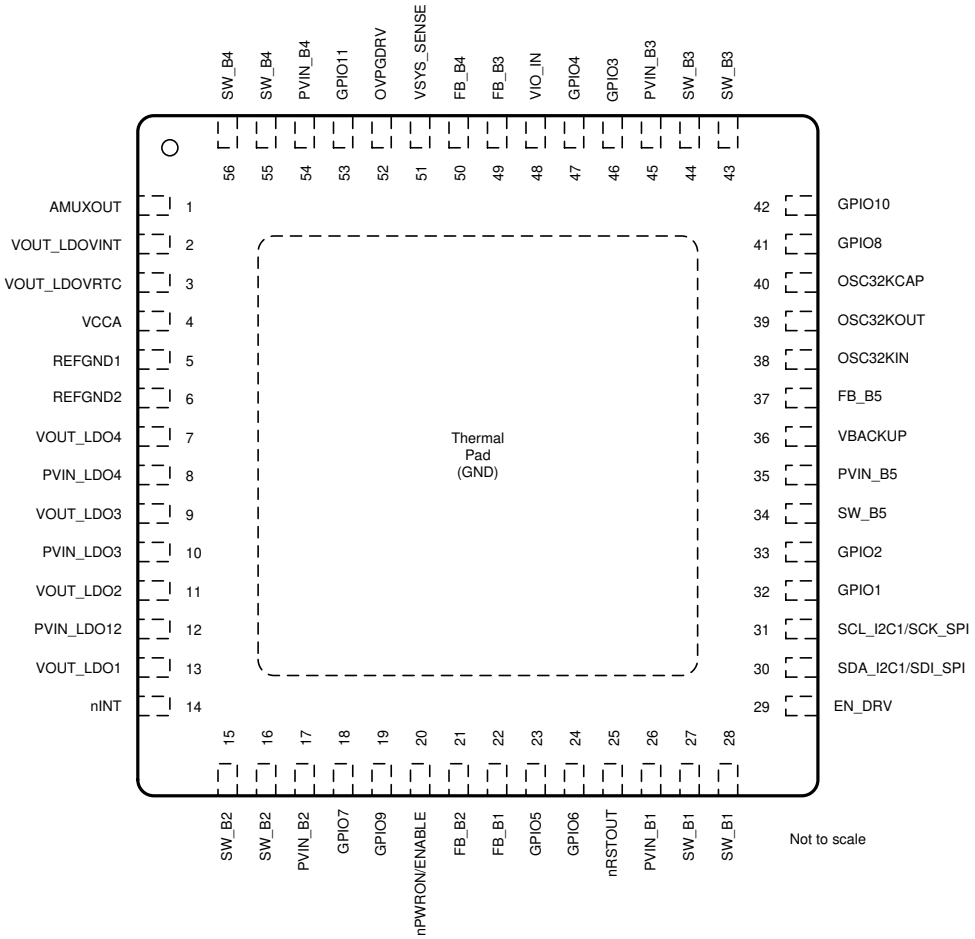

Figure 3-1. 56-Pin RWE (VQFN) Package, 0.5-mm Pitch, With Thermal Pad (Top View)

3.1 Pin Attributes

Pin Attributes

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
STEP-DOWN CONVERTERS (BUCKs)				
PVIN_B1	26	I	Power input for BUCK1	VCCA
FB_B1	22	I	Output voltage-sense (feedback) input for BUCK1 or differential voltage-sense (feedback) positive input for BUCK12/123/1234 in multi-phase configuration	Ground
SW_B1	27	O	Switch node of BUCK1	Floating
SW_B1	28	O	Switch node of BUCK1	Floating
PVIN_B2	17	I	Power input for BUCK2	VCCA
FB_B2	21	I	Output voltage-sense (feedback) input for BUCK2 or differential voltage-sense (feedback) negative input for BUCK12/123/1234 in multi-phase configuration	Ground
SW_B2	15	O	Switch node of BUCK2	Floating
SW_B2	16	O	Switch node of BUCK2	Floating

Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
PVIN_B3	45	I	Power input for BUCK3	VCCA
FB_B3	49	I	Output voltage-sense (feedback) input for BUCK3 or differential voltage-sense (feedback) positive input for BUCK34 in dual-phase configuration	Ground
SW_B3	43	O	Switch node of BUCK3	Floating
SW_B3	44	O	Switch node of BUCK3	Floating
PVIN_B4	54	I	Power input for BUCK4	VCCA
FB_B4	50	I	Output voltage-sense (feedback) input for BUCK4 or differential voltage-sense (feedback) negative input for BUCK34 in dual-phase configuration	Ground
SW_B4	55	O	Switch node of BUCK4	Floating
SW_B4	56	O	Switch node of BUCK4	Floating
PVIN_B5	35	I	Power input for BUCK5	VCCA
FB_B5	37	I	Output voltage-sense (feedback) input for BUCK5	Ground
SW_B5	34	O	Switch node of BUCK5	Floating
LOW-DROPOUT REGULATORS				
PVIN_LDO12	12	I	Power input voltage for LDO1 regulator	VCCA
VOUT_LDO1	13	O	LDO1 output voltage	Floating
VOUT_LDO2	11	O	LDO2 output voltage	Floating
PVIN_LDO3	10	I	Power input voltage for LDO3 regulator	VCCA
VOUT_LDO3	9	O	LDO3 output voltage	Floating
PVIN_LDO4	8	I	Power input voltage for LDO4 regulator	VCCA
VOUT_LDO4	7	O	LDO4 output voltage	Floating
LOW-DROPOUT REGULATORS (INTERNAL)				
VOUT_LDOVRTC	3	O	LDOVRTC output voltage.	—
VOUT_LDOVINT	2	O	LDOVINT output voltage	—
CRYSTAL OSCILLATOR				
OSC32KIN	38	I	32-KHz crystal oscillator input	Ground
OSC32KOUT	39	O	32-KHz crystal oscillator output	Floating
OSC32KCAP	40	O	Filtering capacitor for the 32 KHz crystal Oscillator	Floating
SYSTEM CONTROL				
GPIO1	32	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I	Alternative function: SCL_I2C2, which is the Q&A WatchDog I^2C serial clock (external pull-up)	Ground
		I	Alternative function: CS_SPI, which is the SPI chip enable signal	Ground
		O	Alternative function: nRSTOUT_SoC, which is the SoC reset or power on output (Active Low)	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground

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(1) Default option.

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Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
GPIO2	33	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I/O	Alternative function: SDA_I2C2, which is the Q&A WatchDog I^2C serial bidirectional data (external pull-up)	Ground
		O	Alternative function: SDO_SPI, which is the SPI output data signal	Floating
		I	Alternative function: TRIG_WDOG, which is the watchdog trigger input signal for Watchdog Trigger mode.	Ground
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground
GPIO3	46	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I	Alternative function: nERR_SoC, which is the system error count down input signal from the SoC (Active Low)	Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: LP_WKUP1 or LP_WKUP2, which are capable of processing a wake-up request for the device to go to higher power states while the device is in LP STANDBY state. They can also be used as regular WKUP1 or WKUP2 pins while the device is in mission states	Ground
GPIO4	47	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: LP_WKUP1 or LP_WKUP2, which are capable of processing a wake-up request for the device to go to higher power states while the device is in LP STANDBY state. They can also be used as regular WKUP1 or WKUP2 pins while the device is in mission states	Ground
GPIO5	23	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I/O	Alternative function: SCLK_SPMI, which is the Multi-PMIC SPMI serial interface clock signal. It's an output pin for the master SPMI device, and an input pin for the slave SPMI device	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground
GPIO6	24	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I/O	Alternative function: SDATA_SPMI, which is the Multi-PMIC SPMI serial interface bidirectional data signal	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground

Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
GPIO7	18	I/O	Primary function: General-purpose input (1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I	Alternative function: nERR_MCU, which is the system error count down input signal from the MCU (Active Low)	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground
GPIO8	41	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		O	Alternative function: SYNCCLKOUT, which is a clock output synchronized to the switching clock signals for the bucks in the device	Floating
		I	Alternative function: DISABLE_WDOG, which is the input to disable the watchdog monitoring function	Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground
GPIO9	19	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		O	Alternative function: PGOOD, which is the indication signal for valid regulator output voltages	Floating
		O	Alternative function: SYNCCLKOUT, which is the internal fallback switching clock for BUCK	Floating
		I	Alternative function: DISABLE_WDOG, which is the input to disable the watchdog monitoring function	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground
GPIO10	42	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I	Alternative function: SYNCCLKIN, which is the external switching clock input for BUCK	Floating
		O	Alternative function: SYNCCLKOUT, which is the internal fallback switching clock for BUCK	Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground

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Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
GPIO11	53	I/O	Primary function: General-purpose input(1) and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator	Input: Ground Output: Floating
		I	Alternative function: TRIG_WDOG, which is the watchdog trigger input signal for Watchdog Trigger mode.	Ground
		O	Alternative function: nRSTOUT_SoC, which is the SoC reset or power on output (Active Low)	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low)	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states	Ground
SCL_I2C1/SCK_SPI	31	I	I2C_SPI_SEL = '0': SCL_I2C1 - I^2C serial clock (external pullup)	Ground
		I	I2C_SPI_SEL = '1': CLK_SPI - SPI clock signal	Ground
SDA_I2C1/SDI_SPI	30	I/O	I2C_SPI_SEL = '0': SDA_I2C1 - I^2C serial bidirectional data (external pullup)	Ground
		I	I2C_SPI_SEL = '1': SDI_SPI - SPI input data signal	Ground
nPWRON/ENABLE	20	I	NPWRON_SEL = '0': nPWRON - Active low edge sensitive button press pin to power up the device	Floating
		I	NPWRON_SEL = '1': ENABLE- Level sensitive input pin to power up the device, with programable polarity	Ground
nRSTOUT	25	O	System reset or power on reset output (low = reset, high = active or sleep)	Floating
AMUXOUT	1	O	Buffered bandgap output	Floating
nINT	14	O	Maskable interrupt output request to the host processor	Floating
EN_DRV	29	O	Enable Drive output pin to indicate the device entering safe state (set low when ENABLE_DRV bit is '0')	Floating
OVPGDRV	52	O	Gate drive output for input over voltage protection FET	Floating
POWER SUPPLIES AND REFERENCE GROUN5				
VIO_IN	48	I	Digital supply input for GPIOs and I/O supply voltage	—
VCCA	4	I	Analog input voltage for the internal LDOs and other internal blocks	—
VBACKUP	36	I	Backup power source input pin	Ground
VSYS_SENSE	51	I	Analog input sense pin	Floating
REFGND1	5	—	System reference ground	—
REFGND2	6	—	System reference ground	—
PGND/ThermalPad	—	—	Power Ground, which is also the thermal pad of the package. Connect to PCB ground planes with multiple vias	—

3.2 Digital Signal Descriptions

Table 3-1. Signal Descriptions

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD(1)	RECOMMENDED EXTERNAL PU/PD(1)	Control Registers
			Power Domain	DEGLITCH TIME(2)	Power Domain	Push-pull/Open-drain(3)			
nPWRON (Selectable function of nPWRON/ENABLE pin)(4)	Input	$V_{IL(VCCA)}$, $V_{IH(VCCA)}$	VRTC	50 ms			400 kΩ PU to VCCA	None	NPWRON_SEL
ENABLE (Selectable function of nPWRON/ENABLE pin)(4)	Input	$V_{IL(VCCA)}$, $V_{IH(VCCA)}$	VRTC	8 µs			400 kΩ SPU to VCCA, or 400 kΩ SPD to GND	None	NPWRON_SEL ENABLE_POL ENABLE_DEGLITCH_EN ENABLE_PU_PD_EN ENABLE_PU_SEL
EN_DRV	Output	$V_{OL(EN\_DRV)}$			VCCA/ PVIN_B1	PP	10 kΩ High-side to VCCA	None	ENABLE_DRV
SCL_I2C1 (Selectable function of SCL_I2C1/SCK_SPI pin)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	High-speed mode: 10 ns All other modes: 50 ns			None	PU to VIO	I2C_SPI_SEL I2C1_HS
SDA_I2C1 (Selectable function of SDA_I2C1/SDI_SPI pin)(4)	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)\_20mA}$	VINT	High-speed mode: 10 ns All other modes: 50 ns	VIO	OD	None	PU to VIO	I2C_SPI_SEL I2C1_HS
SCL_I2C2 (Selectable function of GPIO1)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	High-speed mode: 10 ns All other modes: 50 ns			None	PU to VIO	I2C_SPI_SEL I2C2_HS GPIO1_SEL

(1) PU = Pullup, PD = Pulldown, SPU = Software-configurable pullup, SPD = Software-configurable pulldown.
(2) Deglitch time is only applicable when option is enabled
(3) PP = Push-pull, OD = Open-drain
(4) Configurable function through NVM register setting

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Table 3-1. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD(1)	RECOMMENDED EXTERNAL PU/PD(1)	Control Registers
			Power Domain	DEGLITCH TIME(2)	Power Domain	Push-pull/Open-drain(3)			
SDA_I2C2 (Selectable function of GPIO2)(4)	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)\_20mA}$	VINT	High-speed mode: 10 ns All other modes: 50 ns	VIO	OD	None	PU to VIO	I2C_SPI_SEL I2C2_HS GPIO1_SEL
SCK_SPI (Selectable function of SCL_I2C1/SCK_SPI pin)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			None	None	I2C_SPI_SEL
SDI_SPI (Selectable function of SDA_I2C1/SDI_SPI pin)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			None	None	I2C_SPI_SEL
CS_SPI (Selectable function of GPIO1)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			None	None	I2C_SPI_SEL GPIO1_SEL
SDO_SPI (Selectable function of GPIO2)(4)	Output	$V_{OL(VIO)\_20mA}$, $V_{OH(VIO)}$			VIO	PP / HiZ	None	None	I2C_SPI_SEL GPIO1_SEL
SCLK_SPMI (Configurable function of GPIO5)(4)	Input in Slave Mode Output in Master Mode	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)\_20mA}$, $V_{OH(DIG)}$	VINT	None	VINT	PP	400 kΩ PD to GND	None	GPIO5_SEL GPIO5_PU_PD_EN
SDATA_SPMI (Configurable function of GPIO6)(4)	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)\_20mA}$, $V_{OH(DIG)}$	VINT	None	VINT	PP / HiZ	400 kΩ PD to GND	None	GPIO5_SEL GPIO5_PU_PD_EN
nINT	Output	$V_{OL(nINT)}$			VCCA	OD	None	PU to VCCA	
nRSTOUT	Output	$V_{OL(nRSTOUT)}$			VCCA/ VIO	PP or OD	10 kΩ Pull-Up to VIO if configured as Push-Pull	PU to VIO if Open-drain (driven low if no VIO)	NRSTOUT_OD

Table 3-1. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD[1]	RECOMMENDED EXTERNAL PU/PD[1]	Control Registers
			Power Domain	DEGLITCH TIME[2]	Power Domain	Push-pull/Open-drain[3]			
nRSTOUT_SoC (Configurable function of GPIO1 & GPIO11)[4]	Output	$V_{OL(nRSTOUT)}$			VCCA/ VIO	PP or OD	10 kΩ Pull-Up to VIO if configured as Push-Pull	PU to VIO if Open-drain (driven low if no VIO)	GPIO1_SEL GPIO1_OD GPIO11_SEL GPIO11_OD
PGOOD (Configurable function of GPIO9)[4]	Output	$V_{OL(VIO)}$, $V_{OH(VIO)}$			VIO	PP or OD	None	PU to VIO if Open-drain	GPIO9_SEL GPIO9_OD PGOOD_POL PGOOD_WINDOW PGOOD_SEL_x
nERR_MCU (Configurable function of GPIO7)[4]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	8 µs			400 kΩ PD to GND	None	GPIO9_SEL
nERR_SoC (Configurable function of GPIO3)[4]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VRTC	15 µs			400 kΩ PD to GND	None	GPIO7_SEL
DISABLE_WDOG (Configurable function of GPIO8 & GPIO9)[4]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	30 µs			400 kΩ PD to GND	None	GPIO8_SEL GPIO9_SEL
TRIG_WDOG (Configurable function of GPIO2 & GPIO11)[4]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	30 µs			400 kΩ SPD to GND	None	GPIO2_SEL GPIO2_PU_PD_EN GPIO11_SEL GPIO11_PU_PD_EN
nSLEEP1 (Configurable function of all GPIO pins)[4]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	GPIO3 or 4: VRTC other GPIOs: VINT	8 µs			GPIO3 or 4: 400 kΩ SPU to VRTC GPIO5 or 6: 400 kΩ SPU to VINT all other GPIOs: 400 kΩ SPU to VIO	None	GPIOn_SEL GPIOn_PU_PD_EN NSLEEP1B
nSLEEP2 (Configurable function of all GPIO pins)[4]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	GPIO3 or 4: VRTC other GPIOs: VINT	8 µs			GPIO3 or 4: 400 kΩ SPU to VRTC GPIO5 or 6: 400 kΩ SPU to VINT all other GPIOs: 400 kΩ SPU to VIO	None	GPIOn_SEL GPIOn_PU_PD_EN NSLEEP2B

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Table 3-1. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD(1)	RECOMMENDED EXTERNAL PU/PD(1)	Control Registers
			Power Domain	DEGLITCH TIME(2)	Power Domain	Push-pull/Open-drain(3)			
WKUP1 (Configurable function of all GPIO pins except GPIO3 & GPIO4)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	8 µs			GPIO5 or 6: 400 kΩ SPU to VINT or 400 kΩ SPD to GND all other GPIOs: 400 kΩ SPU to VIO or 400 kΩ SPD to GND	None	GPIOn_SEL GPIOn_DEGLITCH_EN GPIOn_PU_PD_EN GPIOn_PU_SEL
WKUP2 (Configurable function of all GPIO pins except GPIO3 & GPIO4)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	8 µs			GPIO5 or 6: 400 kΩ SPU to VINT or 400 kΩ SPD to GND all other GPIOs: 400 kΩ SPU to VIO or 400 kΩ SPD to GND	None	GPIOn_SEL GPIOn_DEGLITCH_EN GPIOn_PU_PD_EN GPIOn_PU_SEL
LP_WKUP1 (Configurable function of GPIO3 & GPIO4)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VRTC	8 µs, no degltch in LP_STANDBY state			400 kΩ SPU to VRTC, or 400 kΩ SPD to GND	None	GPIO3,4_SEL GPIO3,4_DEGLITCH_EN GPIO3,4_PU_PD_EN GPIO3,4_PU_SEL
LP_WKUP2 (Configurable function of GPIO3 & GPIO4)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VRTC	8 µs, no degltch in LP_STANDBY state			400 kΩ SPU to VRTC, or 400 kΩ SPD to GND	None	GPIO3,4_SEL GPIO3,4_DEGLITCH_EN GPIO3,4_PU_PD_EN GPIO3,4_PU_SEL
GPIO1	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)\_20mA}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO1_DEGLITCH_EN GPIO1_PU_PD_EN GPIO1_PU_SEL Output: GPIO1_OD GPIO1_DIR
GPIO2	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)\_20mA}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO2_DEGLITCH_EN GPIO2_PU_PD_EN GPIO2_PU_SEL Output: GPIO2_OD GPIO2_DIR

Table 3-1. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD(1)	RECOMMENDED EXTERNAL PU/PD(1)	Control Registers
			Power Domain	DEGLITCH TIME(2)	Power Domain	Push-pull/Open-drain(3)			
GPIO3	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VRTC	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO3_DEGLITCH_EN GPIO3_PU_PD_EN GPIO3_PU_SEL Output: GPIO3_OD GPIO3_DIR
GPIO4	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VRTC	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO4_DEGLITCH_EN GPIO4_PU_PD_EN GPIO4_PU_SEL Output: GPIO4_OD GPIO4_DIR
GPIO5	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)\_20mA}$, $V_{OH(VIO)}$	VINT	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO5_DEGLITCH_EN GPIO5_PU_PD_EN GPIO5_PU_SEL Output: GPIO5_OD GPIO5_DIR
GPIO6	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)\_20mA}$, $V_{OH(VIO)}$	VINT	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO6_DEGLITCH_EN GPIO6_PU_PD_EN GPIO6_PU_SEL Output: GPIO6_OD GPIO6_DIR
GPIO7	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO7_DEGLITCH_EN GPIO7_PU_PD_EN GPIO7_PU_SEL Output: GPIO7_OD GPIO7_DIR
GPIO8	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO8_DEGLITCH_EN GPIO8_PU_PD_EN GPIO8_PU_SEL Output: GPIO8_OD GPIO8_DIR

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Table 3-1. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD(1)	RECOMMENDED EXTERNAL PU/PD(1)	Control Registers
			Power Domain	DEGLITCH TIME(2)	Power Domain	Push-pull/Open-drain(3)			
GPIO9	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO9_DEGLITCH_EN GPIO9_PU_PD_EN GPIO9_PU_SEL Output: GPIO9_OD GPIO9_DIR
GPIO10	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO10_DEGLITCH_EN GPIO10_PU_PD_EN GPIO10_PU_SEL Output: GPIO10_OD GPIO10_DIR
GPIO11	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VINT	8 µs	VIO	PP or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	Input: GPIO11_DEGLITCH_EN GPIO11_PU_PD_EN GPIO11_PU_SEL Output: GPIO11_OD GPIO11_DIR
SYNCCLKIN (Configurable function of GPIO10)(4)	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			400 kΩ SPD to GND	None	GPIO10_PU_PD_EN
SYNCCLKOUT (Configurable function of GPIO8, GPIO9, & GPIO10)(4)	Output	$V_{OL(VIO)}$, $V_{OH(VIO)}$			VIO	PP	None	None	
CLK32KOUT (Configurable function of GPIO3, GPIO4, GPIO8, & GPIO10)(4)	Output	GPIO3 or 4: $V_{OL(DIG)}$, $V_{OH(DIG)}$ GPIO8 or 10: $V_{OL(VIO)}$, $V_{OH(VIO)}$			GPIO3 or 4: VRTC GPIO8 or 10: VIO	PP	None	None	

4 Specifications

4.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.(1)

POS			MIN	MAX	UNIT
M1.1	Voltage on power supply sense pin	VSYS_SENSE	–0.3	12.5	V
M1.2	Voltage on overvoltage (OV) gate drive	OVPGDRV	–0.3	12.5	V
M1.3	Voltage on OV protected supply input pin	VCCA	–0.3	6	V
M1.4	Voltage on all buck supply voltage input pins	PVIN_Bx	–0.3	6	V
M1.4a	Voltage difference between supply input pins	Between VCCA and each PVIN_Bx	–0.5	0.5	V
M1.5a	Voltage on all buck switch nodes	SW_Bx pins	–2	PVIN_Bx + 0.3 V, up to 6 V	V
M1.5b		SW_Bx pins, 10-ns transient	–2	10	V
M1.6	Voltage on all buck voltage sense nodes	FB_Bx	–0.3	6	V
M1.7	Voltage on all LDO supply voltage input pins	PVIN_LDOx	–0.3	6	V
M1.8	Voltage on all LDO output pins	VOUT_LDOx	–0.3	PVIN_LDOx + 0.3 V, up to 6 V	V
M1.9	Voltage on internal LDO output pins	VOUT_LDOVINT, VOUT_LDOVRTC	–0.3	2	V
M1.10	Voltage on I/O supply pin	VIO_IN with respect to ground pad	–0.3	VCCA + 0.3 V, up to 6 V	V
M1.11	Voltage on logic pins (input or output) in VIO domain	I^2C and SPI pins, nRSTOUT, and nINT pins, and all GPIO output buffers except GPO5 & GPO6	–0.3	6	V
M1.12	Voltage on logic pins (input or output) in LDOVINT domain	GPO5 & GPO6, and all GPIO input buffers except GPI3 & GPI4	–0.3	6	V
M1.13	Voltage on logic pins (input) in LDOVRTC domain	GPI3 & GPI4	–0.3	6	V
M1.14	Voltage on logic pins (input or output) in VCCA domain	nPWRON/ENABLE & EN_DRV	–0.3	6	V
M1.15	Voltage on analog mux output pin	AMUXOUT	–0.3	VCCA + 0.3 V, up to 6 V	V
M1.16	Voltage on back-up power supply input	VBACKUP	–0.3	6	V
M1.17	Voltage on crystal oscillator pins	OSC32KIN, OSC32KOUT, & OSC32KCAP	–0.3	2	V
M1.18	Voltage on REFGND pins	REFGND1 & REFGND2	–0.3	0.3	V
M2.2	Current through input protection FET	Between VSYS_SENSE & VCCA		15	A
M3	Junction temperature, T_J		–45	150	°C
M4	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

POS				VALUE	UNIT
M5	$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
M6	$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

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4.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS			MIN	NOM	MAX	UNIT
R1.1	Voltage on power supply sense pin	VSYS_SENSE	2.8	5	5.5	V
R1.2	Voltage on OV gate drive	OVPGDRV	0	11.5	12	V
R1.3	Voltage on OV protected supply input pin	VCCA	2.8		5.5	V
R1.4	Voltage on all buck supply input pins	PVIN_Bx	2.6	3.8	5.5	V
R1.4a	Voltage difference between supply input pins	Between VCCA and each PVIN_Bx	–0.2		0.2	V
R1.5	Voltage on all buck switch nodes	SW_Bx pins		3.3	5.5	V
R1.6	Voltage on all buck voltage sense nodes(1)	FB_Bx	0		$V_{OUT(BUCKx)max}$	V
R1.7a	Voltage on all LDO supply voltage input pins	PVIN_LDO12, PVIN_LDO3	1.2	3.3	VCCA	V
R1.7b		PVIN_LDO4	2.2	3.3	VCCA	V
R1.8	Voltage on all LDO output pins(1)	VOUT_LDOx	0		$V_{OUT(LDOx)\ max}$	V
R1.9	Voltage on internal LDO output pins	VOUT_LDOVINT, VOUT_LDOVRTC	1.65		1.95	V
R1.10	Voltage on reference ground pins	REFGNDx	–0.3		0.3	V
R1.11	Voltage on I/O supply pin	V_{VIO_IN} = 1.8 V	1.7	1.8	1.9	V
R1.12		V_{VIO_IN} = 3.3 V	3.135	3.3	VCCA, up to 3.465V	
R1.13	Voltage on logic pins (input or output) in VIO domain	I^2C and SPI pins, nRSTOUT & nRSTOUT_SoC pins, GPIO1, GPIO2, GPIO7, GPIO8, GPIO9, GPIO10, and GPIO11 pins	0	V_{VIO}	VIO_{max}	V
R1.14	Voltage on backup supply pin	VBACKUP	0		5.5	V
R1.15	Voltage on crystal oscillator pins	OSC32KIN, OSC32KOUT, OSC32KCAP	0		$V_{OUT(LDOinternal)max}$	V
R1.16	Voltage on logic pins (input or output) in LDOVRTC domain	With fail-safe: GPIO3 & GPIO4	0	$V_{OUT(LDOinternal)}$	$V_{OUT(LDOinternal)max}$	V
R1.17	Voltage on logic pins (input or output) in LDOVINT domain	With fail-safe: GPIO5 to GPIO6	0	$V_{OUT(LDOinternal)}$	$V_{OUT(LDOinternal)max}$	V
R1.18	Voltage on logic pins (input or output) in VCCA domain	nPWRON/ENABLE, EN_DRV	0		V_{VCCA}	V
R1.19	Operating free-air temperature(2)		–40	25	125	°C
R1.20	Junction temperature, T_J	Operational	–40	25	150	°C

(1) The maximum output voltage of BUCK1 to BUCK5 and LDO1 to LDO4 can be reduced by an NVM setting to adopt the maximum voltage to the requirements (or maximum ratings) of the load. This protects the processor from exceeding the maximum ratings of the core voltage. The value is set at TI upon customer request in nonvolatile memory (NVM).
(2) Additional cooling strategies may be necessary to keep junction temperature at recommended limits.

4.4 Thermal Information

THERMAL METRIC(1)		TPS6594-Q1 RVJ (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

4.5 General Purpose Low Drop-Out Regulators (LDO1, LDO2, LDO3)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
1.1a	$C_{IN(LDOx)}$	Input filtering capacitance (1)	Connected from PVIN_LDOx to GND, Shared input tank capacitance (depending on platform requirements)	1	2.2		µF
1.1b	$C_{OUT(LDOx)}$	Output filtering effective capacitance (2)	Connected from VOUT_LDOx to GND	1	2.2	4	µF
1.1c	C_{ESR} (LDOx)	Filtering capacitor ESR (3)	1 MHz ≤ f ≤ 10 MHz			20	mΩ
1.1d	C_{OUT_TOTAL} (LDOx)	Total capacitance at output (Local + POL) (4)	1 MHz ≤ f ≤ 10 MHz			20	µF
1.2a	$V_{IN(LDOx)}$	LDO Input voltage	LDO mode	1.2		VCCA	V
1.2b	$V_{IN(LDOx)\_bypass}$	LDO Input voltage in bypass mode	Bypass mode	1.7		VCCA, upto 3.6 V	V
1.3	$V_{OUT(LDOx)}$	LDO output voltage programmable	LDO mode, with 50-mV steps	0.6		3.3	V
1.4a	$T_{DCOV(LDOx)}$	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperation variations	LDO mode, $V_{IN(LDOx)}$ - $V_{OUT(LDOx)}$ > 300 mV, $V_{OUT(LDOx)}$ ≥ 1V	–1%		1%	
1.4b			LDO mode, $V_{IN(LDOx)}$ - $V_{OUT(LDOx)}$ > 300 mV, $V_{OUT(LDOx)}$ < 1V	–10		10	mV
1.6	$I_{OUT(LDOx)}$	Output current	$V_{IN(LDOx)min}$ ≤ $V_{IN(LDOx)}$ ≤ $V_{IN(LDOx)max}$			500	mA
1.7	$I_{SHORT(LDOx)}$	LDO current limitation	LDO mode and bypass mode	750		1500	mA
1.8a	$I_{IN\_RUSH(LDOx)}$	LDO inrush current	LDOx_BYPASS = 0			1500	mA
			LDOx_BYPASS = 1, with maximum 50-µF load connected to VOUT_LDOx			1500	
1.9	$DC_{LDR(LDOx)}$	DC load regulation, ΔV_{OUT}	1 mA ≤ I_{OUT} ≤ I_{OUTmax} at VOUT_LDOx pin, $V_{IN(LDOx)}$ - $V_{OUT(LDOx)}$ > 300 mV	-1%		1%	
1.10	$DC_{LNR(LDOx)}$	DC line regulation, ΔV_{OUT} / V_{OUT}	V_{INmin} ≤ V_{IN} ≤ V_{INmax}, I_{OUT} = I_{OUTmax}, $V_{IN(LDOx)}$ - $V_{OUT(LDOx)}$ > 300 mV	-1%		1%	
1.11a	$R_{DIS(LDOx)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOx_PLDN = '00'	35	50	65	kΩ
1.11b	$R_{DIS(LDOx)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOx_PLDN = '01'	60	125	200	Ω
1.11c	$R_{DIS(LDOx)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOx_PLDN = '10'	120	250	400	Ω
1.11d	$R_{DIS(LDOx)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOx_PLDN = '11'	240	500	800	Ω
1.12a	$PSRR_{VIN(LDOx)}$	Power supply ripple rejection from $V_{IN(LDOx)}$	f = 1 kHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA	50	60		dB
1.12b			f = 10 kHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA	37	50		
1.12c			f = 100 kHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA	25	35		
1.12d			f = 1 MHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA	25	33		
1.13	$I_{Qoff(LDOx)}$	Quiescent current, off mode	For LDO1, LDO2, & LDO3, VCCA = $V_{IN(LDOx)}$ = 3.3 V, T_J = 25°C			2	µA
1.14a	$I_{Qon(LDOx)}$	Quiescent current, on mode	LDOx_BYPASS = 0, I_{LOAD} = 0 mA , T_J = 25°C			70	µA
1.14b			LDOx_BYPASS = 1, I_{LOAD} = 0 mA , T_J = 25°C			60	
1.15	$T_{LDR(LDOx)}$	Transient load regulation, ΔV_{OUT} (5)	LDOx_BYPASS = 0, I_{OUT} = 20% to 80% of I_{OUTmax}, t_r = t_f = 1 µs		25		mV
1.16	$T_{BYPASS\_to\_LDO(LDOx)}$	Transient regulation due to Bypass Mode to Linear Mode Transition	$V_{IN(LDOx)}$ = 3.3V, I_{OUT}=$I_{OUT(LDOx)max}$, LDOx_BYPASS bit switches between 1 and 0		-2		mV

(1) Input capacitors must be placed as close as possible to the device pins.
(2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
(3) Ceramic capacitors recommended
(4) Additional capacitance, including local and POL, beyond the specifiied value can cause the LDO to become unstable
(5) Load transient voltage must be considered when selecting UV/OV threshold levels for the LDO output

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General Purpose Low Drop-Out Regulators (LDO1, LDO2, LDO3) *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.17	$V_{NOISE(LDOx)}$	RMS Noise	100 Hz < f ≤ 100 kHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 300 mA		250		μV_{RMS}
1.18		Ripple	From the internal charge pump			5	mV_{PP}
1.19a	$R_{BYPASS(LDOx)}$	Bypass resistance	3.1 V ≤ $V_{IN(LDOx)}$ ≤ 3.5 V, PVIN_LDOx ≤ VCCA, I_{OUT} = 500 mA, LDOx_BYPASS = 1			200	mΩ
1.19c			1.7 V ≤ $V_{IN(LDOx)}$ ≤ 1.9 V, I_{OUT} = 500 mA, LDOx_BYPASS = 1			250	
1.20	$V_{TH\_SC\_RV(LDOx)}$	Threshold voltage for Short Circuit and Residual Voltage Detection	LDOx_EN = 0	140	150	160	mV
Timing Requirements							
19.1	$t_{on(LDOx)}$	Turnon time	Time between enable of the LDOx to within OV/UV monitor level			500	µs
19.2		Ramp up slew rate	VOUT from 0.3 V to 90% of LDOx_VSET			25	mV/µs
19.3a	$t_{delay\_OC(LDOx)}$	Over-current detection delay	Detection singal delay when I_{OUT} > ILIM			35	µs
19.3b	$t_{deglitch\_OC(LDOx)}$	Over-current detection signal deglitch time	Digital deglitch time for the over-current detection signal	38		44	µs
19.4	$t_{latency\_OC(LDOx)}$	Over-current signal total latency time	Total delay from I_{out} > ILIM to interrupt or PFSM trigger			79	µs

4.6 Low Noise Low Drop-Out Regulator (LDO4)

Over operating free-air temperature range (unlessotherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
2.1a	$C_{IN(LDO4)}$	Input filtering capacitance(1)	Connected from PVIN_LDO4 to GND, Shared input tank capacitance (depending on platform requirements)	1	2.2		µF
2.1b	$C_{OUT(LDO4)}$	Output filtering capacitance(2)	Connected from VOUT_LDO4 to GND	1	2.2	4	µF
2.1c	$C_{ESR(LDO4)}$	Input and output capacitor ESR(3)	1 MHz ≤ f ≤ 10 MHz			20	mΩ
2.1d	$C_{OUT\_TOTAL(LDO4)}$	Total capacitance at output (Local + POL)(4)	1 MHz ≤ f ≤ 10 MHz			30	µF
2.2	$V_{IN(LDO4)}$	LDO Input voltage		2.2		5.5	V
2.3	$V_{OUT(LDO4)}$	LDO output voltage programmable range	with 25-mV steps	1.2		3.3	V
2.5	$T_{DCOV(LDO4)}$	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperature	$V_{IN(LDO4)}$ - $V_{OUT(LDO4)}$ > 300 mV	–1%		1%	
2.7	$I_{OUT(LDO4)}$	Output current	$V_{IN(LDO4)min}$ ≤ $V_{IN(LDO4)}$ ≤ $V_{IN(LDO4)max}$			300	mA
2.8	$I_{SHORT(LDO4)}$	LDO current limit		400		900	mA
2.9	$I_{IN\_RUSH(LDO4)}$	LDO inrush current	V_{IN} = 3.3V when LDO is enabled			500	mA
2.10	$DC_{LDR(LDO4)}$	DC load regulation, ΔV_{OUT}	1 mA ≤ I_{OUT} ≤ I_{OUTmax} at VOUT_LDO4 pin			1%	
2.11	$DC_{LNR(LDO4)}$	DC line regulation, ΔV_{OUT} / V_{OUT}	$V_{IN(LDO4)min}$ ≤ $V_{IN(LDO4)}$ ≤ $V_{IN(LDO4)max}$, $I_{OUT(LDO4)}$ = $I_{OUT(LDO4)max}$			1%	

(1) Input capacitors must be placed as close as possible to the device pins.
(2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
(3) Ceramic capacitors recommended
(4) Additional capacitance, including local and POL, beyond the specifiied value can cause the LDO to become unstable

ADVANCE INFORMATION

Low Noise Low Drop-Out Regulator (LDO4) *(continued)*

Over operating free-air temperature range (unlessotherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.13a	$PSRR_{(LDO4)}$	Power supply ripple rejection	f = 1 kHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA	65	70		dB
2.13b			f = 10 kHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA	50	70		
2.13c			f = 100 kHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA	40	62		
2.13d			f = 1 MHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA	20	38		
2.12a	$R_{DIS(LDO4)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled, LDO4_PLDN = '00'	35	50	65	kΩ
2.12b			Active only when converter is disabled, LDO4_PLDN = '01'	60	125	200	Ω
2.12c			Active only when converter is disabled, LDO4_PLDN = '10'	120	250	400	Ω
2.12d			Active only when converter is disabled, LDO4_PLDN= '11'	240	500	800	Ω
2.14	$I_{Qoff(LDO4)}$	Leackage current in off mode	For all LDO regulators, VCCA = $V_{IN(LDO4)}$ = 3.8 V, T_J = 25℃			2	µA
2.15	$I_{Qon(LDO4)}$	Quiescent current	I_{LOAD} = 0 mA ,LDO4 under valid operating condition, T_J = 25℃			30	µA
2.16	$T_{LDR(LDO4)}$	Transient load regulation, ΔV_{OUT}	$V_{IN(LDO4)}$ = 3.3V, $V_{OUT(LDO4)}$ = 2.80V, I_{OUT} = 20% of I_{OUT_MAX} to 80% of I_{OUT_MAX} in 1us, $C_{OUT(LDO4)}$ = 2.2uF	–25		25	mV
2.17	$T_{LNR(LDO4)}$	Transient line regulation, ΔV_{OUT} / V_{OUT}	On mode, not under dropout condition, V_{IN} step = 600 mV_{PP}, t_r = t_f = 10 µs	-25		25	mV
2.18	$V_{NOISE(LDO4)}$	RMS Noise	100 Hz < f ≤ 100 kHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 300 mA		15	20	$µV_{RMS}$
2.19	$V_{TH\_SC\_RV(LDO4)}$	Threshold voltage for Short Circuit and Residual Voltage Detection	LDO4_EN = 0	140	150	160	mV
Timing Requirements							
19.11a	$t_{START(LDO4)}$	Start Time	Time from completion of enable command to output voltage at 0.5 V			150	µs
19.12a	$t_{RAMP(LDO4)}$	Ramp Time	Measured from 0.5 V to 90% of LDO4_VSET			350	µs
19.12b	$t_{RAMP\_SLEW(LDO4)}$	Ramp up slew rate	VOUT from 0.5 V to 90% of LDO4_VSET			27	mV/µs
19.13a	$t_{delay\_OC(LDO4)}$	Over-current detection delay	Detection singal delay when I_{OUT} > ILIM			35	µs
19.13b	$t_{deglitch\_OC(LDO4)}$	Over-current detection signal deglitch time	Digital deglitch time for the over-current detection signal	38		44	µs
19.14	$t_{latency\_OC(LDO4)}$	Over-current signal total latency time	Total delay from I_{out} > ILIM to interrupt or PFSM trigger			79	µs

4.7 Internal Low Drop-Out Regulators (LDOVRTC, LDOVINT)

Over operating free-air temperature range (unlessotherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
3.1	$C_{OUT(LDOinternal)}$	Output filtering capacitance(1)	Connected from VOUT_LDOx to GND	1	2.2	4	µF
3.2ai	$V_{IN(LDOVRTC)}$	LDO input voltage	LDOVRTC	1.65		5.5	V
3.2bi	$V_{IN(LDOVINT)}$		LDOVINT	2.7		5.5	V

(1) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.

ADVANCE INFORMATION

Internal Low Drop-Out Regulators (LDOVRTC, LDOVINT) *(continued)*

Over operating free-air temperature range (unlessotherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3a	$V_{OUT(LDOVRTC)}$	LDO output voltage	LDOVRTC		1.8		V
3.3b	$V_{OUT(LDOVINT)}$		LDOVINT		1.8		V
3.4ai	$T_{DCOV(PVIN\_LDOVRTC)}$	Total DC output voltage accuracy for internal LDOs	LDOVRTC_OUT, V_{IN} > 2.7 V	–1		1	%
3.4bi	$T_{DCOV(PVIN\_LDOVINT)}$		LDOVINT_OUT, V_{IN} > 2.7 V	–1		1	%
3.5i	$I_{OUT(LDO\_INT)}$	Output current, internal LDOs	LDOVINT in active mode			50	mA
3.6ai	$I_{OUT(LDO\_RTC)}$	Output current, internal LDOs	$V_{IN(LDOVRTC)}$ ≥ VCCA_UVLO			10	mA
3.6bi			$V_{IN(LDOVRTC)}$ < VCCA_UVLO			1	mA
3.7a	$I_{Qoff(LDOinternal)}$	Leakage current, off mode	LDOVRTC, VCCA = 3.3 V, T_J = 25℃			2	µA
3.7b			LDOVINT, VCCA = 3.3 V, T_J = 25℃			2	
3.8a	$I_{Qon(LDOinternal)}$	Quiescent current, on mode	LDOVRTC under valid operating condition, I_{LOAD} = 0 mA		3	10	µA
3.8b			LDOVINT under valid operating condition, I_{LOAD} = 0 mA		3	10	
3.9	$R_{DIS(LDOinterna;)}$	Pulldown discharge resistance at LDO output	LDOx disabled	60	125	190	Ω
3.10ai	$V_{UVLO(LDOVINT)}$	LDOVINT UVLO threshold	LDOVINT output step from 1.8 V → 1.6 V, t_f = 100 mV/µs	1.62	1.64	1.665	V
3.10bi	$V_{UVLO(LDOVRTC)}$	LDOVRTC UVLO threshold	LDOVRTC output step from 1.8 V → 1.6 V, t_f = 100 mV/µs	1.62	1.64	1.665	V
3.11ai	$V_{OVP(LDOVINT)}$	LDOVINT OVP threshold	LDOVINT output step from 1.8 V → 2.0 V, t_r = 100 mV/µs	1.93	1.96	1.98	V

4.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics - Output Voltage							
4.1a	V_{VOUT_Bx}	Output voltage programmable range	1-phase output	0.3		3.34	V
4.1b			Multi-phase output	0.3		1.9	V
4.2a	$V_{VOUT\_Bx\_Step}$	Output voltage programmable step size	0.3 V ≤ V_{VOUT_Bx} < 0.6 V		20		mV
4.2b			0.6 V ≤ V_{VOUT_Bx} < 1.1 V		5		mV
4.2c			1.1 V ≤ V_{VOUT_Bx} < 1.66 V		10		mV
4.2d			1.66 V ≤ V_{VOUT_Bx} < 3.34 V		20		mV
4.3a	$V_{OUT\_DC\_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.3b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.3c			V_{VOUT_Bx} < 1 V, PFM mode	–10		30	mV
4.3d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1%		3%	
4.4		Input and output voltage difference	Minimum voltage between PVIN_Bx and VOUT_Bx to fulfill the electrical characteristics	0.7			V

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.5a		Output voltage slew-rate programmable range(1)(2)	BUCKn_SLEW_RATE[2:0] = 000b		33.3		mV/µs
4.5b			BUCKn_SLEW_RATE[2:0] = 001b		20		mV/µs
4.5c			BUCKn_SLEW_RATE[2:0] = 010b		10		mV/µs
4.5d			BUCKn_SLEW_RATE[2:0] = 011b		5		mV/µs
4.5e			BUCKn_SLEW_RATE[2:0] = 100b		2.5		mV/µs
4.5f			BUCKn_SLEW_RATE[2:0] = 101b		1.25		mV/µs
4.5g			BUCKn_SLEW_RATE[2:0] = 110b		0.625		mV/µs
4.5h			BUCKn_SLEW_RATE[2:0] = 111b		0.3125		mV/µs
4.6		Output voltage slew-rate accuracy(1)	During voltage programming. Voltage step ≥ 500mV	-10%	0	10%	
Electrical Characteristics - Output Current, Limits and Thresholds							
4.7a	I_{OUT_Bx}	Output current(3)(4)	1-phase, BUCK5			2	A
4.7b			1-phase, BUCK4			4	A
4.7c			1-phase, BUCK1, BUCK2, BUCK3			3.5	A
4.7d			2-phase			7	A
4.7e			3-phase			10.5	A
4.7f			4-phase			14	A
4.8a		Current balancing for multi-phase output	Mismatch between phase current and average phase current, 1A/phase < I_{OUT_Bx} ≤ 2A / phase			20%	
4.8b			Mismatch between phase current and average phase current, I_{OUT_Bx} > 2 A / phase			10%	
4.9a	$I_{LIM\ FWD\ PEAK\ Range}$	Forward current limit (peak during each switching cycle) Programmable range	BUCK5	2.5		3.5	A
4.9b			BUCK1, BUCK2, BUCK3, BUCK4	2.5		5.5	A
4.10	$I_{LIM\ FWD\ PEAK\ Step}$	Forward current limit step Size			1		A
4.11a	$I_{LIM\ FWD\ PEAK\ Accuracy}$	Forward current limit accuracy	I_{LIM} = 3.5 A, 4.5 V ≤ V_{PVIN_Bx} ≤ 5.5 V, BUCK5	–15%		15%	
4.11b			I_{LIM} = 3.5 A, 3.0 V ≤ V_{PVIN_Bx} ≤ 3.6 V, BUCK5	–15%		15%	
4.11c			I_{LIM} = 4.5 A or 5.5 A, 4.5 V ≤ V_{PVIN_Bx} ≤ 5.5 V, BUCK1, BUCK2, BUCK3, BUCK4	–10%		10%	
4.11d			I_{LIM} = 4.5 A or 5.5 A, 3.0 V ≤ V_{PVIN_Bx} ≤ 3.6 V, BUCK1, BUCK2, BUCK3, BUCK4	–15%		10%	
4.12	$I_{LIM\ NEG}$	Negative current limit (peak during each switching cycle)		1.5	2	2.5	A
4.13	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode		600		mA
4.14	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode		300		mA

(1) SLEW_RATEx[2:0] regsiter default comes from NVM memory, and can be re-programed by software. Output capacitance, forward and negative current limits and load current may limit the maximum and minimum slew rates.
(2) The 33.3 mV/µs slew-rate setting is not recommended for L_{Bx} ≥ 1 µH, as this may may trigger OV detection due to larger overshoot at the buck output.
(3) The maximum output current can be limited by the forward current limit ILIM FWD. The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length ofthe current pulse, efficiency, board and ambient temperature.
(4) Advance thermal design is required to avoid thermal shutdown.
(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependent on the output voltage, input voltage, and the inductor current level.

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.14a	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode		300		mA
4.15a	I_{ADD}	Phase adding level (multi-phase rails)	From 1-phase to 2-phase		2.0		A
4.15b			From 2-phase to 3-phase		4.0		A
4.15c			From 3-phase to 4-phase		6.0		A
4.16a	I_{SHED}	Phase shedding level (multi-phase rails)	From 2-phase to 1-phase		0.8		A
4.16b			From 3-phase to 2-phase		1.8		A
4.16c			From 4-phase to 3-phase		2.4		A
4.16d	I_{SHED_Hyst}	Phase shedding hysteresis (multi-phase rails)	Hysteresis from 2-phase to 1-phase		1.2		A
4.16e			Hysteresis from 3-phase to 2-phase		2.2		A
4.16f			Hysteresis from 4-phase to 3-phase		3.6		A
Electrical Characteristics - Current Consumption, On-Resistance, and Output Pulldown Resistance							
4.17	I_{off}	Shutdown current, BUCKx disabled			1		µA
4.18a	I_{Q_AUTO}	Auto mode quiescent current	I_{OUT_Bx} = 0 mA, not switching, master phase		40		µA
4.18b			I_{OUT_Bx} = 0 mA, not switching, slave phase		40		µA
4.19a	$R_{DS(ON)\ HS\ FET}$	On-resistance, high-side FET	I_{OUT_Bx} = 1 A, BUCK5		55	110	mΩ
4.19b			I_{OUT_Bx} = 1 A, BUCK1, BUCK2, BUCK3, BUCK4		52	100	mΩ
4.20a	$R_{DS(ON)\ LS\ FET}$	On-resistance, low-side FET	I_{OUT_Bx} = 1 A, BUCK5		41	70	mΩ
4.20b			I_{OUT_Bx} = 1 A, BUCK1, BUCK2, BUCK3, BUCK4		30	55	mΩ
4.21	R_{DIS_Bx}	Output pulldown discharge resistance	Regulator disabled, per phase, BUCKx_PLDN = 1	50	100	150	Ω
4.22	R_{SW_SC}	Short circuit detection resistance threshold at the SW pin		2	4.5	20	Ω
Electrical Characteristics - 4.4 MHz V_{OUT} Less than 1.9 V, Multiphase or High C_{OUT} Single Phase							
4.31	V_{PVIN_Bx}	Input voltage range		3.0	3.3	5.5	V
4.32	V_{VOUT_Bx}	Output voltage programmable range		0.3		1.9	V
4.33a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.33b	$C_{OUT-Local(Buckx)}$	Output capacitance, local(7)	Per phase	10	22		µF
4.33c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)	Per phase	50		250	µF
4.34a	L_{Bx}	Power inductor	Inductance	154	220	286	nH
4.34b			DCR		10		mΩ
4.35	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA		17		mA
4.36		Efficiency	V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V, I_{OUT_Bx} = 2A		83%		

(6) Input capacitors must be placed as close aspossible to the device pins.
(7) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.37a	T_{LDSR_MP}	Transient load step response(8)	0.3 V ≤ V_{VOUT_Bx} < 0.6 V, I_{OUT_Bx} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		15	20	mV
4.37b			0.6 V ≤ V_{VOUT_Bx} < 1.5 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		15	30	mV
4.37c			1.5 V ≤ V_{VOUT_Bx} ≤ 1.9 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		1.5%	2.5%	
4.38	T_{LNSR}	Transient line response	V_{PVIN_Bx} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bx} = $I_{OUT(max)}$	-20	±5	20	mV
4.39a	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode, 1-phase		3	5	mV_{PP}
4.39b			PFM mode		15	25	mV_{PP}
4.40	$V_{TH\_SC\_RV(Bx)}$	Threshold voltage for Short Circuit and Residual Voltage Detection	Bx_EN = 0	140	150	160	mV
4.101	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0 V		600		mA
4.102	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0 V		300		mA
4.103	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0 V		300		mA
Electrical Characteristics - 4.4 MHz V_{OUT} Less than 1.9 V, Multiphase or High C_{OUT} Single Phase, Internal							
40.1i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.2i			load transient up			250	µs
40.3i			load transient down			250	µs
40.4i			Voltage programming			250	µs
40.5i			Phase adding and shedding			250	µs
40.6i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			100	µs
40.7i			load transient up			100	µs
40.8i			load transient down			100	µs
40.9i			Voltage programming			100	µs
40.10i			Phase adding and shedding			100	µs
40.11i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.12i			PWM			4	A
40.13i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.14i			Voltage programming			30	mV
40.15ai			Phase adding and shedding			10	mV
40.15bi			PFM entry and exit			15	mV
40.16i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.17i			Voltage programming			3	%
40.18ai			Phase adding and shedding			1	%
40.18bi			PFM entry and exit			1	%
40.19i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.20i			Voltage programming			30	mV
40.21ai			Phase adding and shedding			10	mV
40.21bi			PFM entry and exit			15	mV

(8) Please refer to the applications section of the datasheet regarding the power delievery networlk (PDN) used for the transient load step and output ripple test conditions. All ripple specs are defined across POL capacitor in the decribed PDN.

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.22i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.23i			Voltage programming			3	%
40.24ai			Phase adding and shedding			1	%
40.24bi			PFM entry and exit			1	%
40.25i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.26i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.27i			load transient up			25	MHz
40.28i			load transient down			25	MHz
40.29i			Phase adding and shedding			25	MHz
40.30i	T_{Jitter}	Cycle by cycle jitter in steady state				25	ns
Electrical Characteristics - DDR VTT Termination, 4.4 MHz Single Phase Onl							
4.41	V_{PVIN_Bx}	Input voltage range		2.6	3.3	5.5	V
4.42	$I_{OUT\_Bx\_SINK}$	Current sink		–1			A
4.43	V_{VOUT_Bx}	Output voltage programmable range		0.5		0.7	V
4.44a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.44b	$C_{OUT-Local(Buckx)}$	Output capacitance, local(7)		10	22		µF
4.44c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)		25		50	µF
4.45a	L_{Bx}	Power inductor	Inductance	329	470	611	nH
4.45b			DCR		10		mΩ
4.46a	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA, BUCK1, BUCK2, BUCK3, BUCK4		17		mA
4.46b			I_{OUT_Bx} = 0 mA, BUCK5		17		mA
4.47a		Efficiency	V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 0.6 V, I_{OUT_Bx} = -1 A BUCK1, BUCK2, BUCK3, BUCK4		76%		
4.47b			V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 0.6 V, I_{OUT_Bx} = -1 A BUCK5		74%		
4.48	T_{LDSR_MP}	Transient load step response(8)	0.5 V ≤ V_{VOUT_Bx} ≤ 0.7 V, I_{OUT_Bx} = -1 mA to -1000 mA, t_r = t_f = 1 µs, PWM mode		15	30	mV
4.49	T_{LNSR}	Transient line response	V_{PVIN_Bx} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bx} = $I_{OUT\_Bx(max)}$	-20	±5	20	mV
4.50	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode		3	5	mV_{PP}
Electrical Characteristics - DDR VTT Termination, 4.4 MHz Single Phase Only, Internal							
40.31i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.32i			load transient up			250	µs
40.33i			load transient down			250	µs
40.34i			Voltage programming			250	µs
40.35i			Phase adding and shedding			250	µs

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.36i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			100	µs
40.37i			load transient up			100	µs
40.38i			load transient down			100	µs
40.39i			Voltage programming			100	µs
40.40i			Phase adding and shedding			100	µs
40.41i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.42i			PWM			2	A
40.43i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.44i			Voltage programming			30	mV
40.45ai			Phase adding and shedding			10	mV
40.45bi			PFM entry and exit			15	mV
40.46i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.47i			Voltage programming			3	%
40.48ai			Phase adding and shedding			1	%
40.48bi			PFM entry and exit			1	%
40.49i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.50i			Voltage programming			30	mV
40.51ai			Phase adding and shedding			10	mV
40.51bi			PFM entry and exit			15	mV
40.52i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.53i			Voltage programming			3	%
40.54ai			Phase adding and shedding			1	%
40.54bi			PFM entry and exit			1	%
40.55i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.56i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.57i			load transient up			25	MHz
40.58i			load transient down			25	MHz
40.59i			Phase adding and shedding			25	MHz
40.60i	T_{Jitter}	Cycle by cycle jitter in steady state				25	ns
Electrical Characteristics - 4.4 MHz V_{OUT} Less than 1.9 V, Low C_{OUT}, Single Phase Only							
4.51	V_{PVIN_Bx}	Input voltage range		3.0	3.3	5.5	V
4.52	V_{VOUT_Bx}	Output voltage programmable range		0.3		1.9	V
4.53a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.53b	$C_{OUT-Local(Buckx)}$	Output capacitance, local(7)		10	22		µF
4.53c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)		25		100	µF
4.54a	L_{Bx}	Power inductor	Inductance	154	220	286	nH
4.54b			DCR		10		mΩ
4.55a	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA, BUCK1, BUCK2, BUCK3, BUCK4		17		mA
4.55b			I_{OUT_Bx} = 0 mA, BUCK5		17		mA

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.56a		Efficiency	V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V, I_{OUT_Bx} = 2A, BUCK1, BUCK2, BUCK3, BUCK4		83%		
4.56b			V_{PVIN_Bx} = 3.3V, V_{VOUT_Bx} = 1.0V, I_{OUT_Bx} = 1A, BUCK5		85%		
4.57a	T_{LDSR_MP}	Transient load step response(8)	0.3 V ≤ V_{VOUT_Bx} < 0.6 V, I_{OUT_Bx} = 1 mA to 200 mA / phase, t_r = t_f = 1 µs, PWM mode		15	20	mV
4.57b			0.6 V ≤ V_{VOUT_Bx} < 1.5 V, I_{OUT_Bx} = 1 mA to 1 A / phase, t_r = t_f = 1 µs, PWM mode		15	30	mV
4.57c			1.5 V ≤ V_{VOUT_Bx} ≤ 1.9 V, I_{OUT_Bx} = 1 mA to 1 A / phase, t_r = t_f = 1 µs, PWM mode		1.5%	2%	
4.58	T_{LNSR}	Transient line response	V_{PVIN_Bxx} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bx}= $I_{OUT\_Bx(max)}$	-20	±5	20	mV
4.59a	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode		5	8	mV_{PP}
4.59b			PFM mode		15	50	mV_{PP}
4.111	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0 V		600		mA
4.112	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0 V		200		mA
4.113	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0 V		300		mA
Electrical Characteristics - 4.4 MHz V_{OUT} Less than 1.9 V, Low C_{OUT}, Single Phase Only, Internal							
40.61i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.62i			load transient up			250	µs
40.63i			load transient down			250	µs
40.64i			Voltage programming			250	µs
40.65i			Phase adding and shedding			250	µs
40.66i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			250	µs
40.67i			load transient up			100	µs
40.68i			load transient down			100	µs
40.69i			Voltage programming			100	µs
40.70i			Phase adding and shedding			100	µs
40.71i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.72i			PWM			4	A
40.73i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.74i			Voltage programming			30	mV
40.75ai			Phase adding and shedding			10	mV
40.75bi			PFM entry and exit			15	mV
40.76i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.77i			Voltage programming			3	%
40.78ai			Phase adding and shedding			1	%
40.78bi			PFM entry and exit			1	%
40.79i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.80i			Voltage programming			30	mV
40.81ai			Phase adding and shedding			10	mV
40.81bi			PFM entry and exit			15	mV

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.82i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.83i			Voltage programming			3	%
40.84ai			Phase adding and shedding			1	%
40.84bi			PFM entry and exit			1	%
40.85i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.86i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.87i			load transient up			25	MHz
40.88i			load transient down			25	MHz
40.89i			Phase adding and shedding			25	MHz
40.90i	T_{Jitter}	Cycle by cycle jitter in steady state				20	ns
Electrical Characteristics - 4.4 MHz V_{OUT} Greater than 1.7 V, Single Phase Only							
4.61	V_{PVIN_Bx}	Input voltage range		4.5	5	5.5	V
4.62	$I_{OUT\_Bx\_4.4\_HVOUT}$	Output current				2.5	A
4.63	V_{VOUT_Bx}	Output voltage programmable range		1.7		3.34	V
4.64a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.64b	$C_{OUT-Local\_Bx}$	Output capacitance, local(7)		10	22		µF
4.64c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)		50		150	µF
4.65a	L_{Bx}	Power inductor	Inductance	329	470	611	nH
4.65b			DCR		10		mΩ
4.66a	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA, BUCK1, BUCK2, BUCK3, BUCK4		17		mA
4.66b			I_{OUT_Bx} = 0 mA, BUCK5		17		mA
4.67		Efficiency	V_{PVIN_Bx} = 5.0 V, V_{VOUT_Bx} = 1.8V, I_{OUT_Bx} = 1.25A BUCK1, BUCK2, BUCK3, BUCK4		91%		
4.68	T_{LDSR_SP}	Transient load step response(8)	1.7 V ≤ V_{VOUT_Bx} ≤ 3.34 V, I_{OUT_Bx} = 1 mA to 1 A/phase, t_r = t_f = 1 µs, PWM mode		1.5%	2.2%	
4.69	T_{LNSR}	Transient line response	V_{PVIN_Bxx} stepping from 4.7 V to 5.2 V, t_r = t_f = 10 µs, I_{OUT_Bx} = $I_{OUT\_Bx(max)}$	-20	±5	20	mV
4.70a	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode		3	7	mV_{PP}
4.70b			PFM mode		15	25	mV_{PP}
4.121	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 5 V, V_{VOUT_Bx} = 1.8 V		600		mA
4.122	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 5 V, V_{VOUT_Bx} = 1.8 V		200		mA
4.123	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bx} = 5 V, V_{VOUT_Bx} = 1.8 V		300		mA
Electrical Characteristics - 4.4 MHz V_{OUT} Greater than 1.7 V, Single Phase Only, Internal							

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.91i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.92i			load transient up			250	µs
40.93i			load transient down			250	µs
40.94i			Voltage programming			250	µs
40.95i			Phase adding and shedding			250	µs
40.96i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			100	µs
40.97i			load transient up			100	µs
40.98i			load transient down			100	µs
40.99i			Voltage programming			100	µs
40.100i			Phase adding and shedding			100	µs
40.101i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.102i			PWM			4	A
40.103i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.104i			Voltage programming			30	mV
40.105ai			Phase adding and shedding			10	mV
40.105bi			PFM entry and exit			15	mV
40.106i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.107i			Voltage programming			3	%
40.108ai			Phase adding and shedding			1	%
40.108bi			PFM entry and exit			1	%
40.109i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.110i			Voltage programming			30	mV
40.111ai			Phase adding and shedding			10	mV
40.111bi			PFM entry and exit			15	mV
40.112i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.113i			Voltage programming			3	%
40.114ai			Phase adding and shedding			1	%
40.114bi			PFM entry and exit			1	%
40.115i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.116i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.117i			load transient up			25	MHz
40.118i			load transient down			25	MHz
40.119i			Phase adding and shedding			25	MHz
40.120i	T_{Jitter}	Cycle by cycle jitter in steady state				20	ns
Electrical Characteristics - 2.2 MHz Full V_{OUT} Range and V_{IN} Greater than 4.5 V, Single Phase Only							
4.71	V_{PVIN_Bx}	Input voltage range		4.5	5	5.5	V
4.72	V_{VOUT_Bx}	Output voltage programmable range		0.3		3.34	V
4.73a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.73b	$C_{OUT-Local\_Bx}$	Output capacitance, local(7)		10	22		µF
4.73c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)		100		1000	µF

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.74a	L_{Bx}	Power inductor	Inductance	700	1000	1300	nH
4.74b			DCR		10		mΩ
4.75	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA		10		mA
4.76		Efficiency	V_{PVIN_Bx} = 5.0 V, V_{VOUT_Bx} = 1.0 V, I_{OUT_Bx} = 2 A		88%		
4.77a	T_{LDSR_MP}	Transient load step response(8)	0.3 V ≤ V_{VOUT_Bx} < 0.6 V, I_{OUT_Bx} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		15	20	mV
4.77b			0.6 V ≤ V_{VOUT_Bx} < 1.5 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		15	30	mV
4.77c			1.5 V ≤ V_{VOUT_Bx} ≤ 3.34 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		1.5%	2%	
4.78	T_{LNSR}	Transient line response	V_{PVIN_Bx} stepping from 4.7 V to 5.2 V, t_r = t_f = 10 µs, I_{OUT_Bx}= $I_{OUT\_Bx(max)}$	-20	±5	20	mV
4.79a	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode		3	5	mV_{PP}
4.79b			PFM mode		15	25	mV_{PP}
4.131	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 5 V, V_{VOUT_Bx} = 1.0V		600		mA
4.132	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 5 V, V_{VOUT_Bx} = 1.0V		200		mA
4.133	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bx} = 5 V, V_{VOUT_Bx} = 1.0V		300		mA
Electrical Characteristics - 2.2 MHz Full V_{OUT} Range and V_{IN} Greater than 4.5 V, Single Phase Only, Internal							
40.121i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.122i			load transient up			250	µs
40.123i			load transient down			250	µs
40.124i			Voltage programming			250	µs
40.125i			Phase adding and shedding			250	µs
40.126i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			100	µs
40.127i			load transient up			100	µs
40.128i			load transient down			100	µs
40.129i			Voltage programming			100	µs
40.130i			Phase adding and shedding			100	µs
40.131i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.132i			PWM			4	A
40.133i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.134i			Voltage programming			30	mV
40.135ai			Phase adding and shedding			10	mV
40.135bi			PFM entry and exit			15	mV
40.136i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.137i			Voltage programming			3	%
40.138ai			Phase adding and shedding			1	%
40.138bi			PFM entry and exit			1	%

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.139i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.140i			Voltage programming			30	mV
40.141ai			Phase adding and shedding			10	mV
40.141bi			PFM entry and exit			15	mV
40.142i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.143i			Voltage programming			3	%
40.144ai			Phase adding and shedding			1	%
40.144bi			PFM entry and exit			1	%
40.145i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.146i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.147i			load transient up			25	MHz
40.148i			load transient down			25	MHz
40.149i			Phase adding and shedding			25	MHz
40.150i	T_{Jitter}	Cycle by cycle jitter in steady state				50	ns
Electrical Characteristics - 2.2 MHz V_{OUT} Less than 1.9 V Multiphase or Single Phase							
4.81	V_{PVIN_Bx}	Input voltage range		3.0	3.3	5.5	V
4.82	V_{VOUT_Bx}	Output voltage programmable range		0.3		1.9	V
4.83a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.83b	$C_{OUT-Local\_Bx}$	Output capacitance, local(7)	Per phase	10	22		µF
4.83c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)	Per phase	100		1000	µF
4.84a	LBx	Power inductor	Inductance	329	470	611	nH
4.84b			DCR		10		mΩ
4.85	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA		10		mA
4.86		Efficiency	V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V, I_{OUT} = 2A		87%		
4.87a	T_{LDSR_MP}	Transient load step response(8)	0.3 V ≤ V_{VOUT_Bx} < 0.6 V, I_{OUT_Bx} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		15	20	mV
4.87b			0.6 V ≤ V_{VOUT_Bx} < 1.5 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		15	30	mV
4.87c			1.5 V ≤ V_{VOUT_Bx} ≤ 1.9 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		1.5%	2%	
4.88	T_{LNSR}	Transient line response	V_{PVIN_Bx} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bx} = $I_{OUT\_Bx(max)}$	-20	±5	20	mV
4.89a	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode, 1-phase		3	5	mV_{PP}
4.89b			PFM mode		15	25	mV_{PP}
4.141	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V		600		mA
4.142	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V		300		mA
4.143	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V		300		mA
Electrical Characteristics - 2.2 MHz V_{OUT} Less than 1.9 V Multiphase or Single Phase, Internal							

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.151i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.152i			load transient up			250	µs
40.153i			load transient down			250	µs
40.154i			Voltage programming			2000	µs
40.155i			Phase adding and shedding			250	µs
40.156i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			100	µs
40.157i			load transient up			100	µs
40.158i			load transient down			100	µs
40.159i			Voltage programming			100	µs
40.160i			Phase adding and shedding			100	µs
40.161i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.162i			PWM			4	A
40.163i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.164i			Voltage programming			30	mV
40.165ai			Phase adding and shedding			10	mV
40.165bi			PFM entry and exit			15	mV
40.166i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.167i			Voltage programming			3	%
40.168ai			Phase adding and shedding			1	%
40.168bi			PFM entry and exit			1	%
40.169i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.170i			Voltage programming			30	mV
40.171ai			Phase adding and shedding			10	mV
40.171bi			PFM entry and exit			15	mV
40.172i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.173i			Voltage programming			3	%
40.174ai			Phase adding and shedding			1	%
40.174bi			PFM entry and exit			1	%
40.175i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.176i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.177i			load transient up			25	MHz
40.178i			load transient down			25	MHz
40.179i			Phase adding and shedding			25	MHz
40.180i	T_{Jitter}	Cycle by cycle jitter in steady state				50	ns
Electrical Characteristics - 2.2 MHz Full V_{OUT} and Full V_{IN} Range, Single Phase Only							
4.91	V_{PVIN_Bx}	Input voltage range		2.6	3.3	5.5	V
4.92	V_{VOUT_Bx}	Output voltage programmable range		0.3		3.34	V
4.93a	C_{IN_Bx}	Input filtering capacitance(6)		3	22		µF
4.93b	$C_{OUT-Local\_Bx}$	Output capacitance, local(7)		10	22		µF
4.93c	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(7)		100		500	µF

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.94a	L_{Bx}	Power inductor	Inductance	700	1000	1300	nH
4.94b			DCR		10		mΩ
4.95	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bx} = 0 mA, BUCK1, BUCK2, BUCK3, BUCK4		10		mA
4.96		Efficiency	V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V, I_{OUT} = 2A		87%		
4.97a	T_{LDSR_SP}	Transient load step response(8)	0.3 V ≤ V_{VOUT_Bx} < 0.6 V, I_{OUT_Bx} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		35	40	mV
4.97b			0.6 V ≤ V_{VOUT_Bx} < 1.0 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		35	40	mV
4.97c			1.0 V ≤ V_{VOUT_Bx} ≤ 3.34 V, I_{OUT_Bx} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		3.5%	4%	
4.98	T_{LNSR}	Transient line response	V_{PVIN_Bx} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bx} = $I_{OUT\_Bx(max)}$	-20	±5	20	mV
4.99a	V_{OUT_Ripple}	Ripple voltage(8)	PWM mode		3	5	mV_{PP}
4.99b			PFM mode		15	25	mV_{PP}
4.151	$I_{PFM-PWM}$	PFM to PWM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V		600		mA
4.152	$I_{PWM-PFM}$	PWM to PFM switch current threshold(5)	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V		200		mA
4.153	$I_{PWM-PFM\_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bx} = 3.3 V, V_{VOUT_Bx} = 1.0V		300		mA
Electrical Characteristics - 2.2 MHz Full V_{OUT} and Full V_{IN} Range, Single Phase Only, Internal							
40.181i	t_{SETTLE_FSW}	Settling time for fsw (3% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			1000	µs
40.182i			load transient up			250	µs
40.183i			load transient down			250	µs
40.184i			Voltage programming			2000	µs
40.185i			Phase adding and shedding			250	µs
40.186i	t_{SETTLE_Vout}	Settling time for Vout (10mV or 1% from target, 10µs within window)	Max slew rate, no spread spectrum, startup			100	µs
40.187i			load transient up			100	µs
40.188i			load transient down			100	µs
40.189i			Voltage programming			100	µs
40.190i			Phase adding and shedding			100	µs
40.191i	I_{Ripple_L}	Inductor current ripple pp	PFM			5	A
40.192i			PWM			4	A
40.193i	V_{OS_LVout}	Overshoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.194i			Voltage programming			30	mV
40.195ai			Phase adding and shedding			10	mV
40.195bi			PFM entry and exit			15	mV
40.196i	V_{OS_HVout}	Overshoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.197i			Voltage programming			3	%
40.198ai			Phase adding and shedding			1	%
40.198bi			PFM entry and exit			1	%

ADVANCE INFORMATION

BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
40.199i	V_{US_LVout}	Undershoot, 0.3 ≤ VOUT_Bx < 1.0	Startup			30	mV
40.200i			Voltage programming			30	mV
40.201ai			Phase adding and shedding			10	mV
40.201bi			PFM entry and exit			15	mV
40.202i	V_{US_HVout}	Undershoot, 1.0 ≤ VOUT_Bx	Startup			3	%
40.203i			Voltage programming			3	%
40.204ai			Phase adding and shedding			1	%
40.204bi			PFM entry and exit			1	%
40.205i	V_{SW_STOP}	Vout when switching stops after shutdown				140	mV
40.206i	f_{SW_Cycle}	Cycle by cycle switching frequency	Max slew rate, no spread spectrum, startup			25	MHz
40.207i			load transient up			25	MHz
40.208i			load transient down			25	MHz
40.209i			Phase adding and shedding			25	MHz
40.210i	T_{Jitter}	Cycle by cycle jitter in steady state				50	ns
Switching Characteristics							
20.1a	f_{SW}	Switching frequency, PWM mode NVM programmable	2.2 MHz setting, internal clock	2	2.2	2.4	MHz
20.1b			4.4 MHz setting, internal clock	4	4.4	4.8	MHz
20.1d			2.2 MHz setting, internal clock, spread spectrum	1.8	2.2	2.6	MHz
20.1e			4.4 MHz setting, internal clock, spread spectrum	3.5	4.4	5.3	MHz
20.1f			2.2 MHz setting, synchronized to external clock	1.8	2.2	2.6	MHz
20.1g			4.4 MHz setting, synchronized to external clock	3.5	4.4	5.3	MHz
20.2a	f_{SW_max}	Automatic maximum switching frequency scaling in PWM mode	0.6 V ≤ V_{VOUT_Bx}		4.4		MHz
20.2b			0.3 V ≤ V_{VOUT_Bx} < 0.6 V		2.2		MHz
Timing Requirements							
20.3	t_{settle_Bx}	Settling time after voltage scaling				100	µs
20.4	$t_{startup\_Bx}$	Start-up delay	From enable to start of output voltage rise	205		218	µs
20.5a	t_{delay_OC}	Over-current detection delay	Peak current limit triggering during every switching cycle			2	µs
20.5b	$t_{deglitch\_OC}$	Over-current detection signal deglitch time	Digital deglitch time for detected signal. Time duration to filter out short positive and negative pulses	19		23	µs
20.6	$t_{latency\_OC}$	Over-current signal latency time from detection	Total delay from over-current detection to interrupt or PFSM trigger			25	µs

4.9 Reference Generator (Band Gap)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
5.1		Max capacitance at AMUX pin	Capacitance between AMUXOUT pin and thernal/ground pad			100	pF
5.2		Output voltage	Measured at the AMUXOUT pin	1.17	1.2	1.23	V
5.4		Quiescent current	T_J = 25°C		3	5	µA

ADVANCE INFORMATION

Reference Generator (Band Gap) *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing Requirements							
21.1	t_{SU_REF}	Start-up time	From AMUXOUT_EN=1 to the time bandgap voltage settles		1		ms

4.10 Monitoring Functions

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: BUCK REGULATORS OUTPUT							
7.1a	$V_{BUCK\_OV\_TH}$	Overvoltage monitoring for buck output, programable threshold accuracy, V_{OUT_Bx} ≥ 1 V(1)	BUCKn_OV_THR = 0x0	2%	3%	4%	
7.1b			BUCKn_OV_THR = 0x1	2.5%	3.5%	4.5%	
7.1c			BUCKn_OV_THR = 0x2	3%	4%	5%	
7.1d			BUCKn_OV_THR = 0x3	4%	5%	6%	
7.1e			BUCKn_OV_THR = 0x4	5%	6%	7%	
7.1f			BUCKn_OV_THR = 0x5	6%	7%	8%	
7.1g			BUCKn_OV_THR = 0x6	7%	8%	9%	
7.1h			BUCKn_OV_THR = 0x7	9%	10%	11%	
7.2a	$V_{BUCK\_OV\_TH\_mv}$	Overvoltage monitoring for buck output, programable threshold accuracy, V_{OUT_Bx} < 1 V(1)	BUCKn_OV_THR = 0x0	20	30	40	mV
7.2b			BUCKn_OV_THR = 0x1	25	35	45	
7.2c			BUCKn_OV_THR = 0x2	30	40	50	
7.2d			BUCKn_OV_THR = 0x3	40	50	60	
7.2e			BUCKn_OV_THR = 0x4	50	60	70	
7.2f			BUCKn_OV_THR = 0x5	60	70	80	
7.2g			BUCKn_OV_THR = 0x6	70	80	90	
7.2h			BUCKn_OV_THR = 0x7	90	100	110	
7.3a	$V_{BUCK\_UV\_TH}$	Undervoltage monitoring for buck output, programable threshold accuracy, V_{OUT_Bx} ≥ 1 V(1)	BUCKn_UV_THR = 0x0	–4%	–3%	–2%	
7.3b			BUCKn_UV_THR = 0x1	–4.5%	–3.5%	–2.5%	
7.3c			BUCKn_UV_THR = 0x2	–5%	–4%	–3%	
7.3d			BUCKn_UV_THR = 0x3	–6%	–5%	–4%	
7.3e			BUCKn_UV_THR = 0x4	–7%	–6%	–5%	
7.3f			BUCKn_UV_THR = 0x5	–8%	–7%	–6%	
7.3g			BUCKn_UV_THR = 0x6	–9%	–8%	–7%	
7.3h			BUCKn_UV_THR = 0x7	–11%	–10%	–9%	
7.4a	$V_{BUCK\_UV\_TH\_mv}$	Undervoltage monitoring for buck output, programable threshold accuracy, V_{OUT_Bx} < 1 V(1)	BUCKn_UV_THR = 0x0	–40	–30	–20	mV
7.4b			BUCKn_UV_THR = 0x1	–45	–35	–25	
7.4c			BUCKn_UV_THR = 0x2	–50	–40	–30	
7.4d			BUCKn_UV_THR = 0x3	–60	–50	–40	
7.4e			BUCKn_UV_THR = 0x4	–70	–60	–50	
7.4f			BUCKn_UV_THR = 0x5	–80	–70	–60	
7.4g			BUCKn_UV_THR = 0x6	–90	–80	–70	
7.4h			BUCKn_UV_THR = 0x7	–110	–100	–90	
Electrical Characteristics: LDO REGULATOR OUTPUTS							

(1) The default values of BUCKn_OV_THR & BUCKn_UV_THR registers come from the NVM memory, and can be re-programmed by software.

ADVANCE INFORMATION

Monitoring Functions

(continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.5a	$V_{LDO\_OV\_TH}$	Overvoltage monitoring for LDO output, programable threshold accuracy, $V_{OUT\_LDOx} \geq 1$ V(2)	LDOn_OV_THR = 0x0	2%	3%	4%	
7.5b			LDOn_OV_THR = 0x1	2.5%	3.5%	4.5%	
7.5c			LDOn_OV_THR = 0x2	3%	4%	5%	
7.5d			LDOn_OV_THR = 0x3	4%	5%	6%	
7.5e			LDOn_OV_THR = 0x4	5%	6%	7%	
7.5f			LDOn_OV_THR = 0x5	6%	7%	8%	
7.5g			LDOn_OV_THR = 0x6	7%	8%	9%	
7.5h			LDOn_OV_THR = 0x7	9%	10%	11%	
7.6a	$V_{LDO\_OV\_TH\_mv}$	Overvoltage monitoring for LDO output, programable threshold accuracy, $V_{OUT\_LDOx} < 1$ V(2)	LDOn_OV_THR = 0x0	20	30	40	mV
7.6b			LDOn_OV_THR = 0x1	25	35	45	
7.6c			LDOn_OV_THR = 0x2	30	40	50	
7.6d			LDOn_OV_THR = 0x3	40	50	60	
7.6e			LDOn_OV_THR = 0x4	50	60	70	
7.6f			LDOn_OV_THR = 0x5	60	70	80	
7.6g			LDOn_OV_THR = 0x6	70	80	90	
7.6h			LDOn_OV_THR = 0x7	90	100	110	
7.7a	$V_{LDO\_UV\_TH}$	Undervoltage monitoring for LDO output, programable threshold accuracy, $V_{OUT\_LDOx} \geq 1$ V(2)	LDOn_UV_THR = 0x0	–4%	–3%	–2%	
7.7b			LDOn_UV_THR = 0x1	–4.5%	–3.5%	–2.5%	
7.7c			LDOn_UV_THR = 0x2	–5%	–4%	–3%	
7.7d			LDOn_UV_THR = 0x3	–6%	–5%	–4%	
7.7e			LDOn_UV_THR = 0x4	–7%	–6%	–5%	
7.7f			LDOn_UV_THR = 0x5	–8%	–7%	–6%	
7.7g			LDOn_UV_THR = 0x6	–9%	–8%	–7%	
7.7h			LDOn_UV_THR = 0x7	–11%	–10%	–9%	
7.8a	$V_{LDO\_UV\_TH\_mv}$	Undervoltage monitoring for LDO output, programable threshold accuracy, $V_{OUT\_LDOx} < 1$ V(2)	LDOn_UV_THR = 0x0	–40	–30	–20	mV
7.8b			LDOn_UV_THR = 0x1	–45	–35	–25	
7.8c			LDOn_UV_THR = 0x2	–50	–40	–30	
7.8d			LDOn_UV_THR = 0x3	–60	–50	–40	
7.8e			LDOn_UV_THR = 0x4	–70	–60	–50	
7.8f			LDOn_UV_THR = 0x5	–80	–70	–60	
7.8g			LDOn_UV_THR = 0x6	–90	–80	–70	
7.8h			LDOn_UV_THR = 0x7	–110	–100	–90	
Electrical Characteristics: VCCA INPUT							
7.9a	$VCCA_{OV\_TH}$	Overvoltage monitoring for VCCA input, programable threshold accuracy(3)	VCCA_OV_THR = 0x0	2%	3%	4%	
7.9b			VCCA_OV_THR = 0x1	2.5%	3.5%	4.5%	
7.9c			VCCA_OV_THR = 0x2	3%	4%	5%	
7.9d			VCCA_OV_THR = 0x3	4%	5%	6%	
7.9e			VCCA_OV_THR = 0x4	5%	6%	7%	
7.9f			VCCA_OV_THR = 0x5	6%	7%	8%	
7.9g			VCCA_OV_THR = 0x6	7%	8%	9%	
7.9h			VCCA_OV_THR = 0x7	9%	10%	11%	

(2) The default values of LDOn_OV_THR & LDOn_UV_THR registers come from the NVM memory, and can be re-programmed by software.
(3) The default values of VCCA_OV_THR & VCCA_UV_THR registers come from the NVM memory, and can be re-programmed by software.

ADVANCE INFORMATION

Monitoring Functions

(continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.10a	$VCCA_{UV\_TH}$	Undervoltage monitoring for VCCA input, programable threshold accuracy(3)	VCCA_UV_THR = 0x0	-4%	-3%	-2%	
7.10b			VCCA_UV_THR = 0x1	-4.5%	-3.5%	-2.5%	
7.10c			VCCA_UV_THR = 0x2	-5%	-4%	-3%	
7.10d			VCCA_UV_THR = 0x3	-6%	-5%	-4%	
7.10e			VCCA_UV_THR = 0x4	-7%	-6%	-5%	
7.10f			VCCA_UV_THR = 0x5	-8%	-7%	-6%	
7.10g			VCCA_UV_THR = 0x6	-9%	-8%	-7%	
7.10h			VCCA_UV_THR = 0x7	-11%	-10%	-9%	
Timing Requirements							
26.30a	$t_{delay\_OV\_UV}$	BUCK and LDO OV/UV detection delay	Detection delay with 5 mV (V_{in} < 1 V) or 0.5% (V_{in} ≥ 1 V) over/underdrive			8	µs
26.30b	$t_{delay\_OV\_UV}$	VCCA OV/UV detection delay	Detection delay with 30 mV iver/underdrive			8	µs
26.31a	$t_{deglitch1\_OV\_UV}$	VCCA, BUCK, and LDO OV/UV signal deglitch time	VMON_DEGLITCH_SEL = 0: Digital deglitch time for detected signal	3.4	3.8	4.2	µs
26.31b	$t_{deglitch2\_OV\_UV}$		VMON_DEGLITCH_SEL = 1: Digital deglitch time for detected signal	18	20	22	µs
26.32a	$t_{latency1\_OV\_UV}$	BUCK and LDO OV/UV signal latency time	VMON_DEGLITCH_SEL = 0: Total delay from 5mV (V_{in} < 1 V) or 0.5% (V_{in} ≥ 1 V) over/underdrive to interrupt or PFSM trigger			13	µs
26.32b	$t_{latency2\_OV\_UV}$		VMON_DEGLITCH_SEL = 1: Total delay from 5mV (V_{in} < 1 V) or 0.5% (V_{in} ≥ 1 V) over/underdrive to interrupt or PFSM trigger			30	µs
26.32b	$t_{latency1\_VCCA\_OV\_UV}$	VCCA OV/UV signal latency time	VMON_DEGLITCH_SEL = 0: Total delay from 30 mV over/underdrive to interrupt or PFSM trigger			13	µs
26.32b	$t_{latency2\_VCCA\_OV\_UV}$		VMON_DEGLITCH_SEL = 1: Total delay from 30 mV over/underdrive to interrupt or PFSM trigger			30	µs
26.33a	$t_{deglitch\_PGOOD\_rise}$	PGOOD signal degltich time	Internal logic signal transitions from invalid to valid(4)	9.5		10.5	µs
26.33b	$t_{deglitch\_PGOOD\_fall}$		Internal logic signal transitions from valid to invalid(4)		0		µs

(4) Interrupt status signal is input signal for PGOOD deglitch logic.

4.11 Clocks, Oscillators, and PLL

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: CRYSTAL							
6.1		Crystal frequency			32768		Hz
6.2		Crystal frequency tolerance	Parameter of crystal, T_J = 25°C	–20		20	ppm
6.4		Crystal series resistance	At fundamental frequency			90	kΩ
6.5		Oscillator drive power	The power dissipated in the crystal during oscillator operation		0.1	0.5	µW
6.6		Crystal Load capacitance(1)	Corresponding to crystal frequency, including parasitic capacitances	6		12.5	pF
6.7		Crystal shunt capacitance	Parameter of crystal		1.4	2.6	pF
ELectrical Characteristics: 32-kHz CRYSTAL OSCILLATOR EXTERNAL COMPONENTS							

(1) Customer must use the XTAL_SEL bit to select the corresponding crystal based on its load capacitance.

ADVANCE INFORMATION

Clocks, Oscillators, and PLL *(continued)*

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.7a		Load capacitance on OSC32KIN and OSC32KOUT (parallel mode, including parasitic of PCB for external capacitor)(2)	External Capacitors	0		13	pF
6.7b			Internal Capacitors	9.5	12	14.5	pF
Switching Characteristics: 32-kHz CRYSTAL OSCILLATOR CLOCK							
23.1		Crystal Oscillator output frequency	Typical with specified load capacitors		32768		Hz
23.2		Crystal Oscillator Output duty cycle	Parameter of crystal, T_J = 25°C	40%	50%	60%	
23.3		Crystal Oscillator rise and fall time	10% to 90%, with 10 pF load capacitance		10	20	ns
23.4		Crystal Oscillator Settling time				200	ms
Electrical Characteristics: 20-MHz and 128-kHz RC OSCILLATOR CLOCK							
6.8a		20 MHz RC Oscillator active current consumption	T_J = 25°C		4	8	µA
6.8b		20 MHz RC Oscillator power down current	T_J = 25°C			30	nA
6.9a		128 kHz RC Oscillator active current consumption	T_J = 25°C			2	µA
6.9b		128 kHz RC Oscillator power down current				30	nA
Switching Characteristics: 20-MHz and 128-kHz RC OSCILLATOR CLOCK							
23.10		20 MHz RC Oscillator output frequency	After trimming at T_J = 25°C	19	20	21	MHz
23.11		20 MHz RC Oscillator output duty cycle		40%	50%	60%	
23.12		128 kHz RC Oscillator output frequency	After trimming at T_J = 25°C	121	128	135	kHz
23.13		128 kHz RC Oscillator output duty cycle		40%	50%	60%	
Switching Characteristics: DPLL, SYNCCLKIN, and SYNCCLKOUT							
22.1a		External input clock nominal frequency	EXT_CLK_FREQ = 0x0		1.1		MHz
22.1b			EXT_CLK_FREQ = 0x1		2.2		
22.1c			EXT_CLK_FREQ = 0x2		4.4		
22.2a		External input clock required accuracy from nominal frequency	SS_DEPTH = 0x0	–18%		18%	
22.2b			SS_DEPTH = 0x1	–12%		12%	
22.2c			SS_DEPTH = 0x2	–10%		10%	
22.2d			SS_DEPTH = 0x3	–8%		8%	
22.3		External clock detection delay for missing clock detection				1.8	µs
22.4		External clock input debounce time for clock detection				20	µs
22.5		Clock change delay (internal to external)	From valid clock detection to use of external clock		600		µs
22.7a		SYNCCLKOUT clock nominal frequency	SYNCCLKOUT_FREQ_SEL = 0x1		1.1		MHz
22.7b			SYNCCLKOUT_FREQ_SEL = 0x2		2.2		MHz
22.7c			SYNCCLKOUT_FREQ_SEL = 0x3		4.4		MHz
22.8		SYNCCLKOUT duty-cycle	Cycle-to-cycle	40%	50%	60%	
22.9		SYNCCLKOUT output buffer external load		5	35	50	pF
22.10		DPLL clock output frequency		42.24	52.8	63.36	MHz

ADVANCE INFORMATION

(2) External capacitors must be used if cyrstal load capacitance > 6 pF.

Clocks, Oscillators, and PLL *(continued)*

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
22.11 a		Spread spectrum variation for nominal switching frequency	SS_DEPTH = 0x1		6.3%		
22.11 b			SS_DEPTH = 0x2		8.4%		
22.11 c			SS_DEPTH = 0x3		10.5%		
22.12		Internal clock spread spectrum modulation steps	f_{SSM_STEP}/f_{SW}		2.1%		
Timing Requirements: Clock Monitors							
26.7a	$t_{latency\_CLKfail}$	Clock Monitor Failure signal latency from occurance of error	Failure on 20MHz system clock			10	µs
26.7b			Failure on 128KHz monitoring clock			40	µs
26.8	$t_{latency\_CLKdrift}$	Clock Monitor Drift signal latency from detection				115	µs
26.9	f_{sysclk}	Internal system clock		19	20	21	MHz
26.10	CLKdrift_TH	Threshold for internal system clock frequency drift detection		-20%		20%	
26.11	CLKfail_TH	Threshold for internal system clock stuck at high or stuck at low detection				10	MHz

4.12 Thermal Monitoring and Shutdown

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
8.1a	T_{WARN_0}	Thermal warning rising threshold	TWARN_LEVEL = 0	110	120	130	°C
8.1b	T_{WARN_1}		TWARN_LEVEL = 1	120	130	140	°C
8.1c		Thermal warning hysteresis			10		°C
8.2a	$T_{SD\_orderly}$	Thermal orderly shutdown rising threshold		130	140	150	°C
8.2b		Thermal orderly shutdown hysteresis			10		°C
8.3a	T_{SD_imm}	Thermal immediate shutdown rising threshold		140	150	160	°C
8.3b		Thermal immediate shutdown hysteresis			10		°C
Timing Requirements							
26.6	$t_{latancy\_TSD}$	TSD signal latency from detection				400	µs
26.6a i	t_{delay_TSD}	TSD signal analog comparator delay	With 5-mV overdrive			5	µs
26.6b i	$t_{deglitch\_TSD}$	TSD signal deglitch time				4	µs

4.13 System Control Thresholds

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
9.1	$V_{POR\_Falling}$	VCCA UVLO/POR falling threshold	Measured on VCCA pin, trimmed	2.7	2.75	2.8	V
9.2	V_{POR_Rising}	VCCA UVLO/POR rising threshold	Measured on VCCA pin, untrimmed	2.7		3	V
9.3	V_{POR_Hyst}	VCCA UVLO/POR hysteresis			100		mV
9.5a	$V_{VCCA\_OVP\_Rising}$	VCCA OVP rising threshold	Measured on VCCA pin, trimmed	5.6	5.7	5.8	V

ADVANCE INFORMATION

System Control Thresholds *(continued)*

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.5b	$V_{VCCA\_OVP\_Hyst}$	VCCA OVP hysteresis			50		mV
9.7	$V_{VSYS\_OVP\_Rising}$	VSYS OVP rising threshold	Measured on VSYS_SENSE pin, untrimmed	5.6	5.9	6.2	V
9.8	$V_{VSYS\_OVP\_Rising\_Trim}$	VSYS OVP rising threshold, trimmed	Measured on VSYS_SENSE pin, trimmed	5.8	5.9	6	V
9.9	$V_{OVPGDRV\_OFF}$	Output voltage at OVPGDRV pin when external FET is switched off	Measured after OVPGDRV pin has reached steady state voltage			0.4	V
9.10	$V_{OVPGDRV\_On}$	Output voltage at OVPGDRV pin when external FET is switched on	Measured after OVPGDRV pin has reached steady state voltage			12	V
9.12	$V_{OVPGDRV\_OV\_TH}$	Over-voltage threshold level at OVPGDRV pin when external FET is switched on				12.5	V
26.20	$t_{VSYSOVP\_INIT}$	Start up time for OVPGDRV output	V_{SYS_SENSE} >3 V, and $V_{OVPGDRV}$ has reached 90% of its final value			5	ms
Timing Requirements							
26.2	$t_{latency\_VSYSOVP}$	OVPGDRV latency from VSYS OVP detection	Measured time from the detection of V_{VSYS_SENSE} > $V_{VSYS\_OVP\_Rising}$ with ≤ 100mV/µs slope, to when $V_{OVPGDRV}$ = VCCA (external FET is switched off)			15	µs
26.3	$t_{latency\_VCCAOVP}$	OVPGDRV latency from VCCA OVP detection	Measured time between the detection of $V_{VCCA\_OVP\_Rising}$ < V_{VCCA} < 6 V, with ≤100mV/µs slope, to when $V_{OVPGDRV}$ = VCCA (external FET is switched off)			15	µs
26.3ai	$t_{latency\_VCCAOVP\_analog}$	Analog comparator latency from VCCA OVP detection	With voltage ramp forced at the VCCA pin, measured time from the detection of V_{VCCA} rising from 5 V to 6 V with ≤ 100mv/µs slope, to the time when $V_{OVPGDRV}$ ≤ V_{VCCA}			10	µs
26.3bi	$t_{deglitch\_VCCAOVP}$	VCCA_OVP digital deglitch filtering				15	µs
26.4	$t_{latency\_VCCAUVLO}$	VCCA_UVLO signal latency from detection				10	µs
26.4ai	$t_{latency\_VCCAUVLO\_analog}$	Analog comparator latency from VCCA_UVLO detection	Measured time between V_{VCCA} falling from 3.3 V to 2.7 V with ≤ 100mv/µs slope, to the detection of VCCA_UVLO signal			10	µs
26.5	$t_{latency\_VINT}$	LDOVINT OVP and UVLO signal latency from detection				10	µs
26.5ai	t_{delay_VINT}	LDOVINT OVP and UVLO analog comparator delay	With 25-mV overdrive			10	µs
26.14	$t_{ABISTrun}$	Run time for ABIST				1	ms
26.15	$t_{LBISTrun}$	Run time for LBIST				5	ms
26.16	$t_{INIT\_NVM\_ANALOG}$	Device initialization time to load default values for NVM programmable registers, and start up analog circuits				2	ms
26.17	$t_{INIT\_REF\_CLK\_LDO}$	Device initialization time for reference bandgaps, system clock, and internal LDOs				1	ms

4.14 Current Consumption

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
10.1	I_{NO_SUPPLY}	No Supply leackage current	From VSYS_SENSE pin, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. PWRON/ENABLE deactivated. VCCA = PVIN_Bx = PVIN_LDOx = 0 V. T_J = 25℃		2	4	µA

ADVANCE INFORMATION

Current Consumption *(continued)*

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10.2	I_{BACKUP_RTC}	Backup current consumption, regulators disabled	From VBACKUP pin. PWRON/ENABLE deactivated. Device powered by the backup battery source. Only 32-kHz crystal oscillator and RTC counters are functioning. T_J = 25℃. VSYS_OVP function deactivated.		7	10	µA
10.3a	$I_{LP\_STANDBY\_noOVP}$	Low Power Standby current consumption, regulators disabled	From VCCA pins. PWRON/ENABLE deactivated. VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. 32-kHz crystal oscillator and RTC digital is functioning. GPI pins in LDOVRTC domain are active. T_J = 25℃. VSYS OVP function deactivated		20	24	µA
10.3b	$I_{LP\_STANDBY}$	Low Power Standby current consumption, regulators disabled	From VSYS_SENSE pin, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. PWRON/ENABLE deactivated. VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. 32-kHz crystal oscillator and RTC digital is functioning. GPI pins in LDOVRTC domain are active. T_J = 25℃. VSYS_OVP function activated		29	34	µA
10.4	I_{ACTIVE}	Active current consumption during PWM operation	From VSYS_SENSE pin, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. PWRON/ENABLE activated. VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. All buck and LDO regulators are powered up to 1.8 V output voltage with no load. Buck regulators are in single phase, forced PWM mode with 2.2MHz switching frequency. All buck and VCCA OV/UV monitoring enabled. VSYS_OVP function activated. T_J = 25℃.		40	45	mA
10.5	$I_{STANDBY}$	Standby current consumption	From VSYS_SENSE pin, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. PWRON/ENABLE deactivated. VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. T_J = 25℃. VSYS_OVP function activated		55	62	µA

4.15 Backup Battery Charger

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
27.1a	I_{charge}	Charging current	VBACKUP = 1 V, BB_ICHR = 0x0		100		µA
27.1b			VBACKUP = 1 V, BB_ICHR = 0x1		500		
27.2a	V_{EOC}	End of charge voltage	BB_VEOC = 0x0	2.4	2.5	2.6	V
27.2b			BB_VEOC = 0x1	2.7	2.8	2.9	
27.2c			BB_VEOC = 0x2	2.9	3	3.1	
27.2d			BB_VEOC = 0x3	3.2	3.3	3.4	
27.3	I_{q_CHGR}	Quiescent current of backup battery charger	End of charge, charger enabled		5	9	µA
27.4a	$I_{q\_CHGR\_OFF}$	Off current of backup battery charger	Charger disabled. Device not in BACKUP state. Tj < 125°C		10	50	nA
27.4b			Charger disabled. Device not in BACKUP state. 125°C < Tj < 150°C			100	
27.5	C_{BKUP}	Backup battery capacitance with additional capacitor	Additional capacitor added when backup battery ESR > 20 Ω	1	2.2	4	µF
27.6a	R_{BKUP_ESR}	Backup battery sereies resistance	Without additional capacitor in parallel			20	Ω
27.6b			With additional capacitor in parallel			1000	

ADVANCE INFORMATION

4.16 Digital Input Signal Parameters

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device. VIO refers to the VIO_IN pin, VCCA refers to the VCCA pin.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: nPWRON/ENABLE							
11.1	$V_{IL(VCCA)}$	Low-level input voltage		-0.3	0	0.54	V
11.2	$V_{IH(VCCA)}$	High-level input voltage		1.26			V
11.3		Hysteresis		150			mV
Electrical Characteristics: I2C/SPI Pins and Input Signals through all GPIO pins							
11.4	$V_{IL(DIG)}$	Low-level input voltage		-0.3	0	0.54	V
11.5	$V_{IH(DIG)}$	High-level input voltage		1.26			V
11.6		Hysteresis		150			mV
Timing Requirements: nPWRON/ENABLE							
24.1a	t_{LPK_TIME}	nPWRON Long Press Key time			8		s
24.1b	t_{degl_PWRON}	nPWRON button deglitch time		48	50	52	ms
24.2	t_{degl_ENABLE}	ENABLE signal deglitch time(1)	exclude when activated under LP_STANDBY state while the system clock is not available	6	8	10	µs
24.3a	t_{WKUP_LP}	Time from valid GPIx assertion until device wakes up from LP_STANDBY state to ACTIVE or MCU ONLY states	FAST_BIST=0			10	ms
24.3b			FAST_BIST=1			5	ms
Timing Requirements: GPIx, nSLEEPx, nERRx, and other digital input signals							
25.1a	t_{degl_GPIx}	GPIx and nSLEEPx signal deglitch time		6	8	10	µs
25.1b	t_{degl_ESMx}	nERRx signal deglitch time		12	15	18	µs
25.2a	$t_{STARTUP}$	Time from receiving nPWRON/ENABLE trigger in STANDBY state to nRSTOUT assertion				5	ms
25.2b		Time from valid GPIx assertion until device wakes up from Deep Sleep or STANDBY state to ACTIVE or MCU ONLY states				1.5	ms
25.3	t_{SLEEP}	Time from nSLEEPx assertion until device goes to SLEEP or DEEP SLEEP state				1.5	ms
25.4a	$t_{WK\_PW\_MIN}$	Minimum valid input pulse width for the WKUP input signals	input through LP_WKUP1 and LP_WKUP2 (GPIO3 or GPIO4) pins while the device is in LP_STANDBY state	40			ns
25.4b			input through WKUP1, WKUP2, LP_WKUP1 and LP_WKUP2 pins while the device is in mission states	200			ns
25.5a	t_{WD_DIS}	DISABLE_WDOG input signal deglitch time		24	30	36	µs
25.5b	t_{WD_pulse}	TRIG_WDOG input signal deglitch time		24	30	36	µs

(1) ENABLE signal deglitch is not available when device is activated from the LP_STANDBY state while the deglitching clock is not available.

4.17 Digital Output Signal Parameters

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device. VIO refers to the VIO_IN pin, VCCA refers to the VCCA pin.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: SDA_I2C1, and Output Signals through GPO1 and GPO2 pins							
12.11	$V_{OL(VIO)\_20mA}$	Low-level output voltage, push-pull and open-drain	I_{OL} = 20 mA			0.4	V
12.12	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	VIO – 0.4			V

ADVANCE INFORMATION

Digital Output Signal Parameters

(continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the thermal/ground pad of the device. VIO refers to the VIO_IN pin, VCCA refers to the VCCA pin.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12.12 ai	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA, V_{VIO} = 1.8 V	1.4			V
12.12 bi	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA, V_{VIO} = 3.3 V	2.9			V
Electrical Characteristics: Output Signals through GPO3 and GPO4 pins							
12.13	$V_{OL(DIG)}$	Low-level output voltage, push-pull	I_{OL} = 3 mA			0.4	V
12.14	$V_{OH(DIG)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	1.4			V
Electrical Characteristics: Output Signals through GPO5 and GPO6 pins							
12.4	$V_{OL(DIG)\_20mA}$	Low-level output voltage, push-pull	I_{OL} = 20 mA			0.4	V
12.5	$V_{OH(DIG)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	1.4			V
Electrical Characteristics: Output Signals through GPO7, GPO8, GPO9, GPO10, and GPO11 pins							
12.1	$V_{OL(VIO)}$	Low-level output voltage, push-pull and open-drain	I_{OL} = 3 mA			0.4	V
12.2	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	VIO – 0.4			V
12.2a i	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA, V_{VIO} = 1.8 V	1.4			V
12.2b i	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA, V_{VIO} = 3.3 V	2.9			V
12.3		Supply for external pullup resistor, open drain				VIO	V
Electrical Characteristics: EN_DRV, nINT, nRSTOUT							
12.6	$V_{OL(EN\_DRV)}$	Low-level output voltage for EN_DRV pin	I_{OL} =20 mA			0.4	V
12.7	$V_{OL(nINT)}$	Low-level output voltage for nINT pin	I_{OL} = 20 mA			0.4	V
12.8	$V_{OL(nRSTOUT)}$	Low-level output voltage for nRSTOUT and nRSTOUT_SoC pin	I_{OL} = 20 mA			0.4	V

4.18 I/O Pullup and Pulldown Resistance

Over operating free-air temperature range, VIO refers to the VIO_IN pin, VSYS refersto the VSYS_SENSE pin (unless otherwise noted).

POS	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics						
13.1	nPWRON/ENABLE pullup and pulldown resistance	nPWRON/ENALBE IO buffer internal pull up to VCCA supply and pull down to ground	280	400	520	kΩ
13.2	IO signals pullup resistance	SDA_I2C1/SDI_SPI, and GPIO1 -11 pins configured as input with internal pullup	280	400	520	kΩ
13.3	IO signals pulldown resistance	GPIO1 - 11 pins configured as inputs with internal pulldown	280	400	520	kΩ
13.4	nRSTOUT and nRSTOUT_SoC pullup resistance	Internal pullup to VIO supply when output driven high	8	10	12	kΩ
13.5	EN_DRV pullup resistance	Internal pullup to VCCA supply when output driven high	8	10	12	kΩ

4.19 I^2C Interface

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

POS	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics						

ADVANCE INFORMATION

I²C Interface *(continued)*

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
14.1	C_B	Capacitive load for SDA and SCL				400	pF
Timing Requirements							
16.1a	f_{SCL}	Serial clock frequency	Standard mode			100	kHz
16.1b			Fast mode			400	
16.1c			Fast mode+			1	MHz
16.1d			High-speed mode, C_b = 100 pF			3.4	
16.1e			High-speed mode, C_b = 400 pF			1.7	
16.2a	t_{LOW}	SCL low time	Standard mode	4.7			µs
16.2b			Fast mode	1.3			
16.2c			Fast mode+	0.5			
16.2d			High-speed mode, C_b = 100 pF	160			ns
16.2e			High-speed mode, C_b = 400 pF	320			
16.3a	t_{HIGH}	SCL high time	Standard mode	4			µs
16.3b			Fast mode	0.6			
16.3c			Fast mode+	0.26			
16.3d			High-speed mode, C_b = 100 pF	60			ns
16.3e			High-speed mode, C_b = 400 pF	120			
16.4a	$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
16.4b			Fast mode	100			
16.4c			Fast mode+	50			
16.4d			High-speed mode	10			
16.5a	$t_{HD;DAT}$	Data hold time	Standard mode	10		3450	ns
16.5b			Fast mode	10		900	
16.5c			Fast mode+	10			
16.5d			High-speed mode, C_b = 100 pF	10		70	ns
16.5e			High-speed mode, C_b = 400 pF	10		150	
16.6a	$t_{SU;STA}$	Setup time for a start or a REPEATED START condition	Standard mode	4.7			µs
16.6b			Fast mode	0.6			
16.6c			Fast mode+	0.26			
16.6d			High-speed mode	160			ns
16.7a	$t_{HD;STA}$	Hold time for a start or a REPEATED START condition	Standard mode	4			µs
16.7b			Fast mode	0.6			
16.7c			Fast mode+	0.26			
16.7d			High-speed mode	160			ns
16.8a	t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
16.8b			Fast mode	1.3			
16.8c			Fast mode+	0.5			
16.9a	$t_{SU;STO}$	Setup time for a STOP condition	Standard mode	4			µs
16.9b			Fast mode	0.6			
16.9c			Fast mode+	0.26			
16.9d			High-speed mode	160			ns

ADVANCE INFORMATION

I²C Interface *(continued)*

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16.10 a	t_{rDA}	Rise time of SDA signal	Standard mode			1000	ns
16.10 b			Fast mode	20		300	
16.10 c			Fast mode+			120	
16.10 d			High-speed mode, C_b = 100 pF	10		80	
16.10 e			High-speed mode, C_b = 400 pF	20		160	
16.11 a	t_{fDA}	Fall time of SDA signal	Standard mode			300	ns
16.11 b			Fast mode	1.4		300	
16.11 c			Fast mode+	6.5		120	
16.11 d			High-speed mode, C_b = 100 pF	10		80	
16.11 e			High-speed mode, C_b = 400 pF	13		160	
16.12 a	t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
16.12 b			Fast mode	20		300	
16.12 c			Fast mode+			120	
16.12 d			High-speed mode, C_b = 100 pF	10		40	
16.12 e			High-speed mode, C_b = 400 pF	20		80	
16.13 a	t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	High-speed mode, C_b = 100 pF	10		80	ns
16.13 b			High-speed mode, C_b = 400 pF	20		160	
16.14 a	t_{fCL}	Fall time of SCL signal	Standard mode			300	ns
16.14 b			Fast mode	6.5		300	
16.14 c			Fast mode+	6.5		120	
16.14 d			High-speed mode, C_b = 100 pF	10		40	
16.14 e			High-speed mode, C_b = 400 pF	20		80	
16.15 a	t_{SP}	Pulse width of spike suppressed (SCL and SDA spikes that are less than the indicated width are suppressed)	Standard mode, fast mode, and fast mode+			50	ns
16.15 b			High-speed mode			10	

4.20 System Power Management Interface (SPMI)

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
15.2	C_b	Bus capacitance				50	pF
Timing Requirements							
18.1	t_{SCLKOH}	SCLK output high time		66			ns
18.2	$t_{SCLKIOL}$	SCLK output low time		66			ns

ADVANCE INFORMATION

System Power Management Interface (SPMI) *(continued)*

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
18.3	$t_{SCLKOTR}$	SCLK output transition (Rise/Fall) time		0.9		24	ns
18.5	t_D	SDATA output valid from SCLK rising edge		0		60	ns
18.6	$t_{SDATAOTR}$	SDATA output transition (Rise/Fall) time		0.9		24	ns
18.7	t_{SDATAZ}	SDARA drive release time				54	ns
18.8	t_S	SDATA receiver setup time		6			ns
18.9	t_H	SDATA receiver hold time		15			ns
18.10	t_{CYCLE}	SCLK cycle time		200			ns

4.21 Serial Peripheral Interface (SPI)

These specifications are ensured by design, V_{IO} = 1.8 V(unless otherwise noted).

POS	PARAMETERS		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Electrical Characteristics							
15.1		Capacitive load on pin SDO				30	pF
Timing Requirements							
17.1	1	Cycle time		200			ns
17.2	2	Enable lead time		150			ns
17.3	3	Enable lag time		150			ns
17.4	4	Clock low time		60			ns
17.5	5	Clock high time		60			ns
17.6	6	Data setup time		15			ns
17.7	7	Data hold time		15			ns
17.8	8	Output data valid after SCLK falling		4			ns
17.9	9	New output data valid after SCLK falling				60	ns
17.10	10	Disable time				30	ns
17.11	11	CS inactive time		100			ns

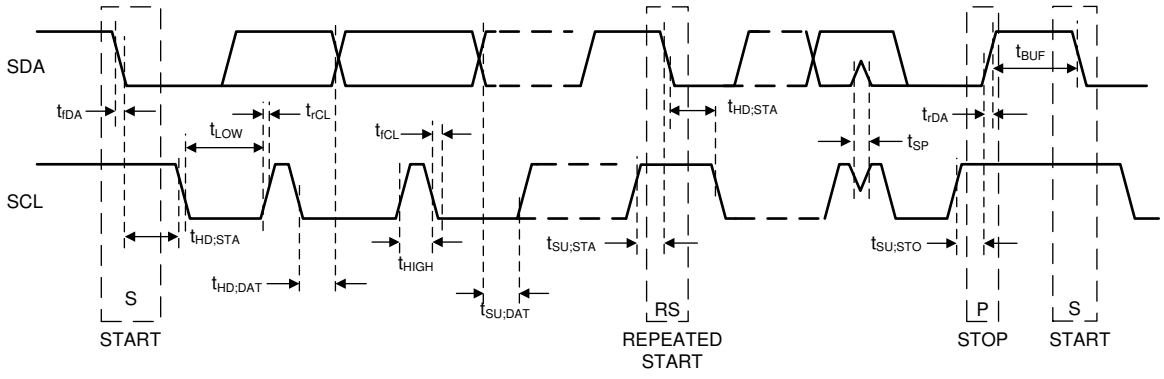

图 4-1. I²C Timing

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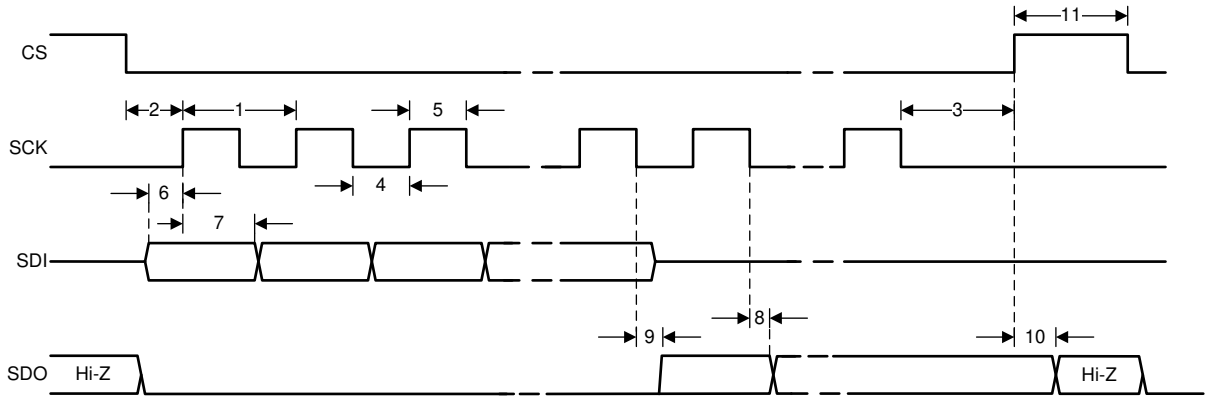

图 4-2. SPI Timing

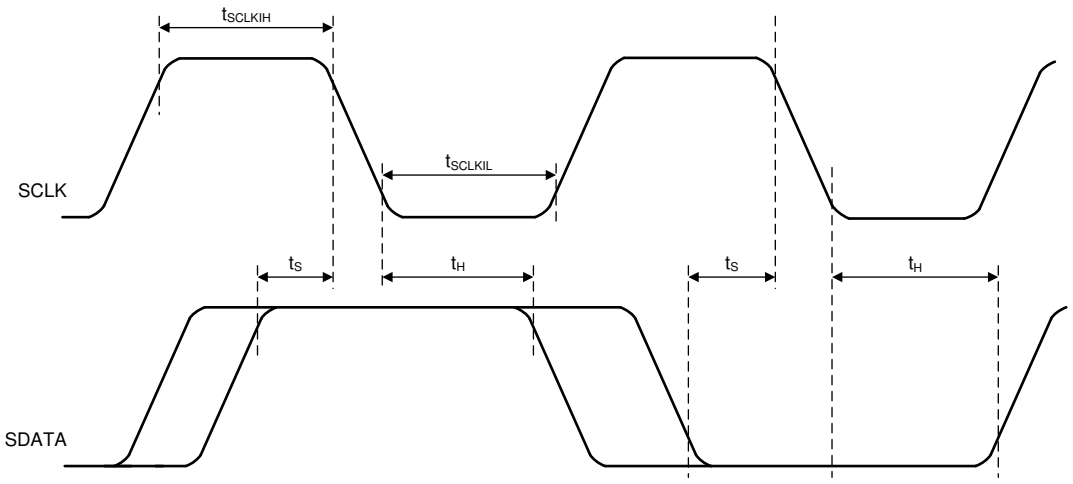

图 4-3. SPMI Receive Timing

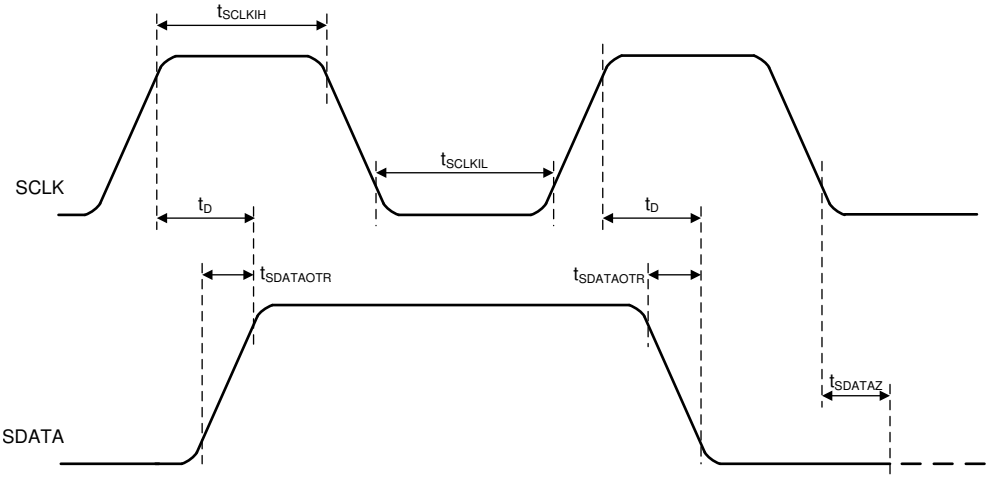

图 4-4. SPMI Transmit Timing

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4.22 Typical Characteristics

5 Detailed Description

5.1 Overview

The TPS6594-Q1 device is a power-management integrated circuit (PMIC), available in a 56-pin, 0.5-mm pitch, 8-mm × 8-mm QFN package. It is designed for powering embedded systems or system on chip (SoC) in Automotive or Industrial applications. It provides five configurable buck converter rails, with four of the rails having the ability to combine outputs in multi-phase mode. BUCK4 has the ability to supply up to 4 A in single-phase mode, while BUCK1, BUCK2, and BUCK3 have the ability to supply up to 3.5 A in single-phase mode. When working in multi-phase mode, each BUCK1, BUCK2, BUCK3, and BUCK4 can supply up to 3.5 A per phase, adding up to 14 A in four-phase configuration. BUCK5 is a single-phase only buck converter which supports up to 2 A current load. All five of the BUCK converters has the capability to sink up to 1 A, and support dynamic voltage scaling. Double buffered voltage scaling registers enable each BUCK to transition to a different voltages during operation by SPI or I^2C. A DPLL enables the BUCK converters to synchronizing to an external clock input, with phase delays between the outputs rails.

The TPS6594-Q1 device also provides three LDO rails which can supply up to 500 mA per rail and can be configured in bypass mode to be used as a load switch. One additional low-noise LDO rail can supply up to 300 mA. The 500 mA LDOs support 0.6 V to 3.3 V output with 50 mV step. The 300 mA low-noise LDO supports 1.2 V to 3.3 V output with 25 mV step. The output voltages of the LDOs can be pre-configured through the SPI or I^2C interfaces.

Two I^2C interface channels or one SPI channel can be used to configure the power rails and the power state of the TPS6594-Q1 device. I^2C channel 1 (I2C1) is the main channel with access to the registers which control the configurable power sequencer, the states and the outputs of power rails (including DVFS), the device operating states, and the RTC registers. I^2C channel 2 (I2C2), which is available through GPIO1 and GPIO2 pins, is dedicated for accessing the Q&A Watchdog communication registers. When the SPI is configured instead of the two I^2C interfaces, the SPI can access all of the registers, including the Q&A Watchdog registers. An NVM option is available to enable I2C1 to access all of the registers as well, including the Q&A Watchdog registers.

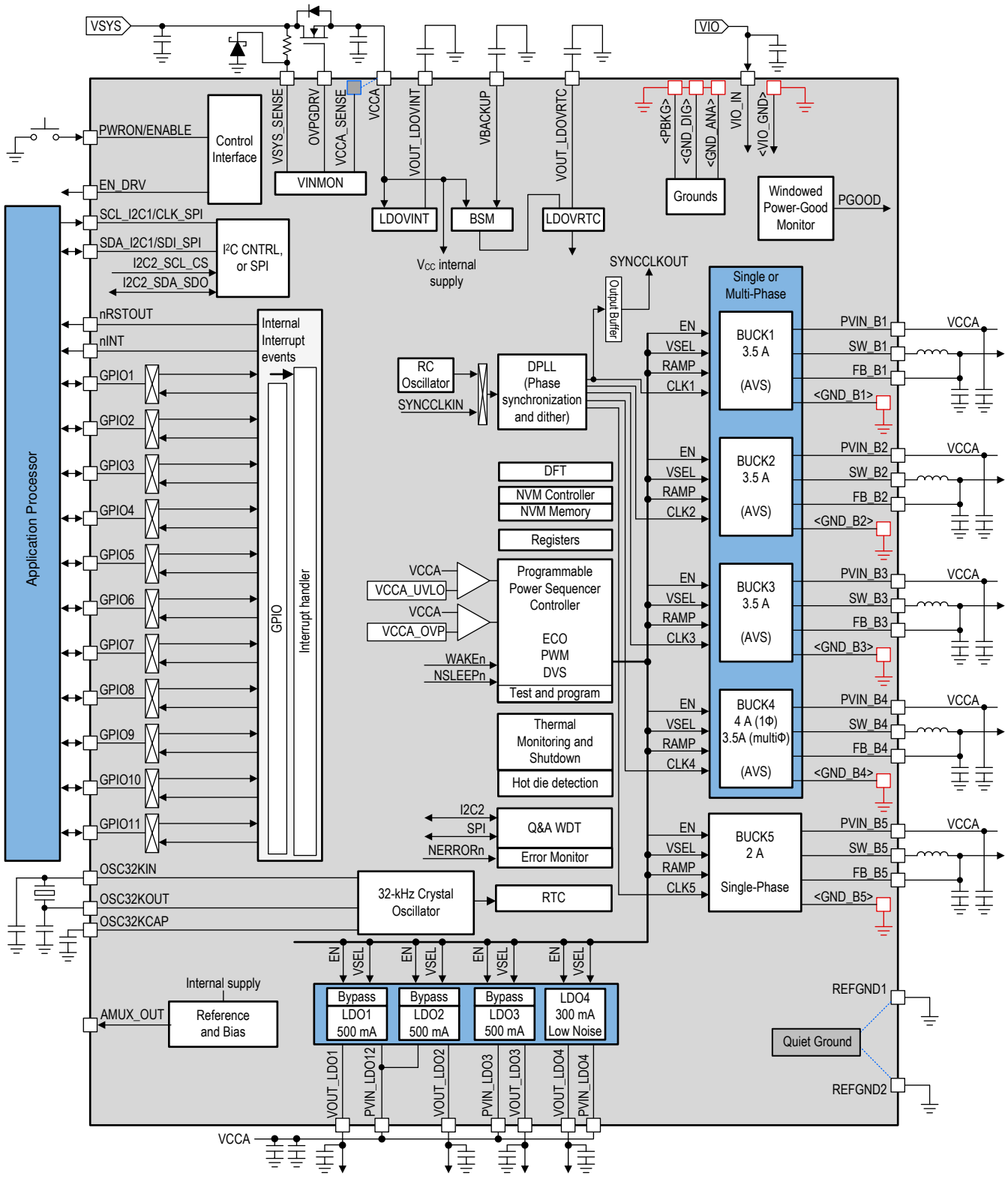
The TPS6594-Q1 device includes an internal RC oscillator to sequence all resources during power up and power down. Two internal LDOs (LDOVINT and LDOVRTC) generate the supply for the entire digital circuitry of the device as soon as the external input supply is available through the VCCA input. A backup battery supply input can also be used to power the RTC block and a 32 kHz Crystal Oscillator clock generator in the event of a power loss from the main supply

TPS6594-Q1 device has eleven GPIOs each with multiple functions and configurable features. All of the GPIOs, when configured as a general purpose output pin, can be included in the power-up and power-down sequence and used as enable signals for external resources. In addition, each GPIO can be configured as a wake-up input or a sleep mode trigger. The default configuration of the GPIO port comes from the NVM memory, and can be re-programmed by system software if the external connection permits.

The TPS6594-Q1 device includes a Q&A watchdog to monitor software lockup, and two system error monitoring inputs with fault injection options to monitor the lock-step signal of the attached SoC or MCU. The device includes protection and diagnostic mechanisms such as short-circuit protection, thermal monitoring and shutdown. The PMIC can notify the processor of these events through the interrupt signal open-drain output, allowing the processor to take action in response.

An SPMI interface is included in the TPS6594-Q1 device to distribute power state information to satellite PMICs, thus enabling synchronous power state transition across multiple PMICs in the application system. This feature allows the consolidation of IO control signals required between the application processor or MCU and any number of PMICs in the system into TPS6594-Q1 only.

5.2 Functional Block Diagram



* These red squares are internal pads for down-bonds to the package thermal/ground pad.

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5.3 Feature Description

5.3.1 System Voltage Monitor and Over-voltage Protection

The TPS6594-Q1 device includes an over-voltage protection mechanism through a 12 V compliant input monitor at the VSYS_SENSE pin. When an over-voltage is detected at the VSYS_SENSE pin, OVPGDRV pin is pulled low to disable the external high voltage load switch which connects the VSYS supply to the VCCA pin. To protect VSYS_SENSE pin from over-voltage condition due to possible short at the pre-regulator output, we recommend connecting a 10 V zener diode to ground at the VSYS_SENSE pin, as well as series resistor(s) between the VSYS_SENSE pin and the output of the pre-regulator to limit the current surge. The voltage slew rate at the VSYS_SENSE pin must be limited to ≤100 mV/µs to prevent possible damage to the device

In case the TPS6594-Q1 device detects a VCCA over voltage condition, the VCCA domain will be unpowered and no longer able to signal the over voltage condition to the VSYS over-voltage protection module. Therefore, a dead-lock mechanism is implemented in the VSYS domain by setting a latch to keep the external high voltage load switch (between VSYS and VCCA) open once the Leo device has detected a VCCA over voltage condition.

The comparator module which monitors the voltage on the VCCA pins controls the power state machine of the TPS6594-Q1 device. VCCA voltage detection outputs determine the power states of the device as following:

VCCA_UVLO When the voltage on the VCCA pin rises above VCCA_UV during initial power up, the device transitions from the NO SUPPLY state to the INIT state. When the supply at the VCCA pin falls below the VCCA_UVLO threshold, the device returns to the BACKUP state. During BACKUP state LDOVRTC is powered by the output of the Backup Supply Management (BSM) module. When the input supply of the LDOVRTC falls below the operating range, the device returns to the NO SUPPLY state and is completely shutdown. The device will not return to the BACKUP state from the NO SUPPLY state.

VCCA_OVP While the device is in operation, if the voltage on VCCA pin rises above the VCCA_OVP threshold despite the OVPGDRV mechanism, the device will clear the ENABLE_DRV bit and start the immediate shutdown sequence to protect itself from over-voltage input condition.

When VCCA is expected to be 5 V or 3.3 V, a separate voltage comparator can be enabled to monitor whether or not the VCCA voltage is within the expected PGOOD range. Please refer to 节 5.3.4 for additional detail on the operation of the PGOOD monitor function.

The 图 5-1 shows a block diagram of the system input monitoring and over-voltage protection mechanism, and the generation of the VCCAUVLO and VCCA_OVP power state control signals.

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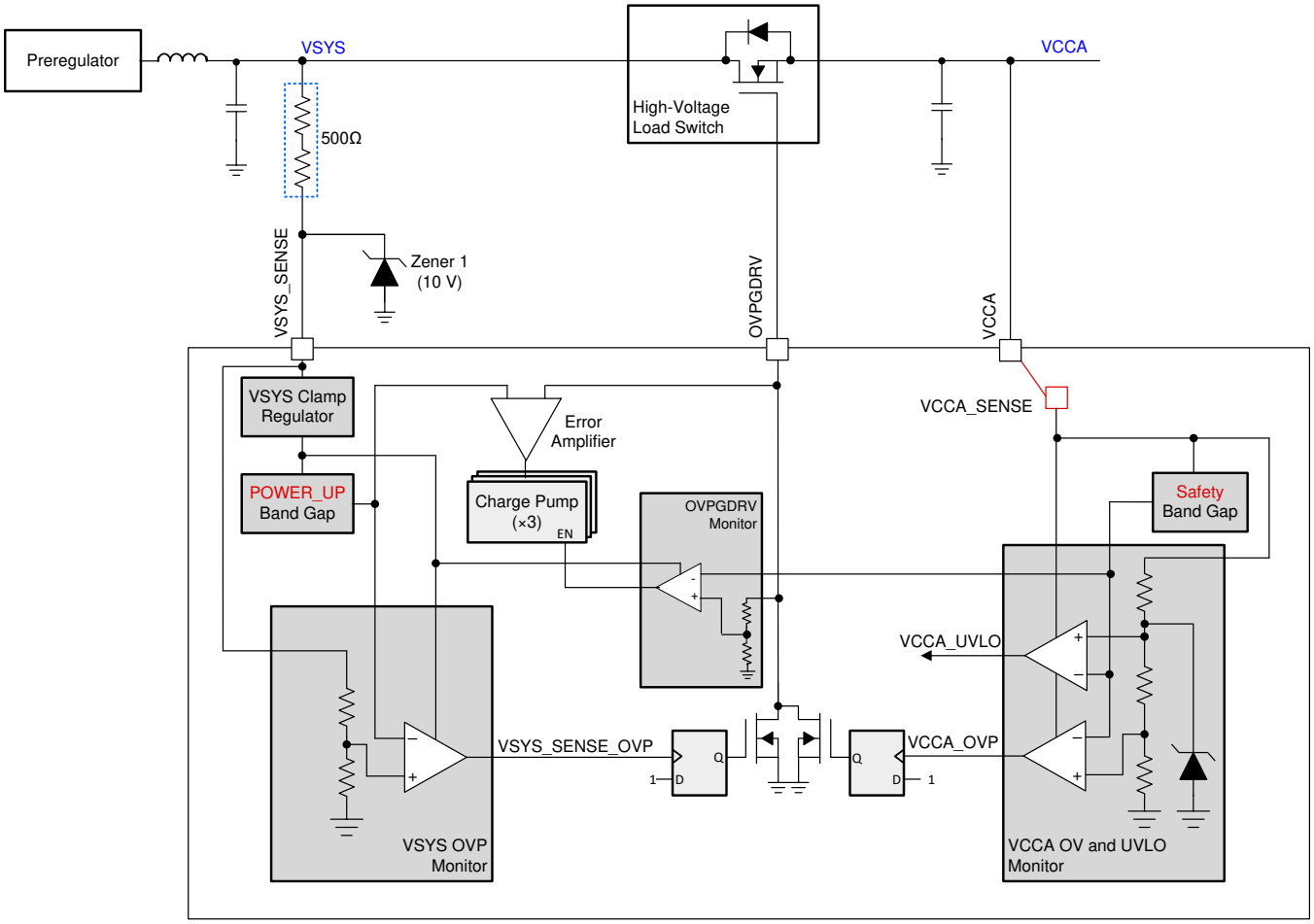

图 5-1. VSYS Monitor and OVPGDRV Output Generation

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5.3.2 Power Resources (Bucks and LDOs)

The power resources provided by the TPS6594-Q1 device include inductor-based bucks and linear LDOs. These supply resources provide the required power to the external processor cores, external components, and to modules embedded in the device. The supply of the bucks, the PVIN_Bx pins, must connect to the VCCA pin externally. The supply of the LDOs, the PVIN_LDOx pins, may connect to the VCCA pin or a buck output which is at a lower voltage level than the VCCA.

The voltage output of each power resources are continuously monitored by a dedicated analog monitor on an independent reference voltage domain. An un-used regulator can also be used as a voltage monitor for an external rail by connected the external rail to the FB_Bn or the VOUT_LDOn pin. A residual voltage checking option is also available for each power resource to ensure the output voltage has dropped below 150 mV before it can be powered up again.

表 5-1 lists the power resources provided by the TPS6594-Q1 device.

表 5-1. Power Resources

RESOURCE	TYPE	VOLTAGE	CURRENT CAPABILITY	COMMENTS
BUCK1, BUCK2, BUCK3	BUCK	0.3 to 0.6 V, 20-mV steps 0.6 to 1.1 V, 5-mV steps 1.1 to 1.66 V, 10-mV steps 1.66 to 3.34 V, 20-mV steps	3.5 A	Can be configured in multi-phase mode or stand-alone in single-phase mode
BUCK4	BUCK	0.3 to 0.6 V, 20-mV steps 0.6 to 1.1 V, 5-mV steps 1.1 to 1.66 V, 10-mV steps 1.66 to 3.34 V, 20-mV steps	4 A in single-phase mode 3.5 A in multi-phase mode	Can be configured in multi-phase mode or stand-alone in single-phase mode
BUCK5	BUCK	0.3 to 0.6 V, 20-mV steps 0.6 to 1.1 V, 5-mV steps 1.1 to 1.66 V, 10-mV steps 1.66 to 3.34 V , 20-mV steps	2 A	Only in single-phase mode
LDO1, LDO2, LDO3	LDO	0.6 V to 3.3 V, 50-mV steps	500 mA	Bypass mode configurable
LDO4	LDO	1.2 V to 3.3 V, 25-mV steps	300 mA	Low-noise performance

5.3.2.1 Buck Regulators

5.3.2.1.1 Overview

The TPS6594-Q1 includes five synchronous buck converters, with four of which can combine outputs in multi-phase configuration. All of the buck converters support the following features:

- Automatic mode control based on the loading (PFM or PWM mode) or Forced-PWM mode operation
- External clock synchronization option to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Soft start
- AVS support with configurable slew-rate
- Windowed Power Good Monitor with configurable threshold
- Windowed voltage monitor for external supply when the buck converter is disabled

When the outputs of converters are combined in multi-phase configuration, it also supports the following features:

- Current balancing between the phases of the converter
- Differential voltage sensing from point of the load
- Phase shifted outputs for EMI reduction
- Optional dynamic phase shedding/adding

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There are two modes of operation for the converter, depending on the output current required: pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption. When forced-PWM mode is selected, the device avoids pulse skipping and allows easy filtering of the switch noise by external filter components. The drawback of this mode is the higher quiescent current at low output current levels.

When operating in PWM mode the phases of a multi-phase regulator are automatically added/shed based on the load current level. The forced multi-phase mode can be enabled for lower ripple at the output.

A multi-phase synchronous BUCK converter offers several advantages over a single power stage converter. For application processor power delivery, lower ripple on the input and output currents and faster transient response to load steps are the most significant advantages. The even distribution of the load current in multi-phase output configuration, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. The physical size of the output inductor shrinks significantly due to this heat reduction. A block diagram of a single core is shown in Figure 5-2.

Interleaving switching action of the multi-phase converters is shown in Figure 5-3.

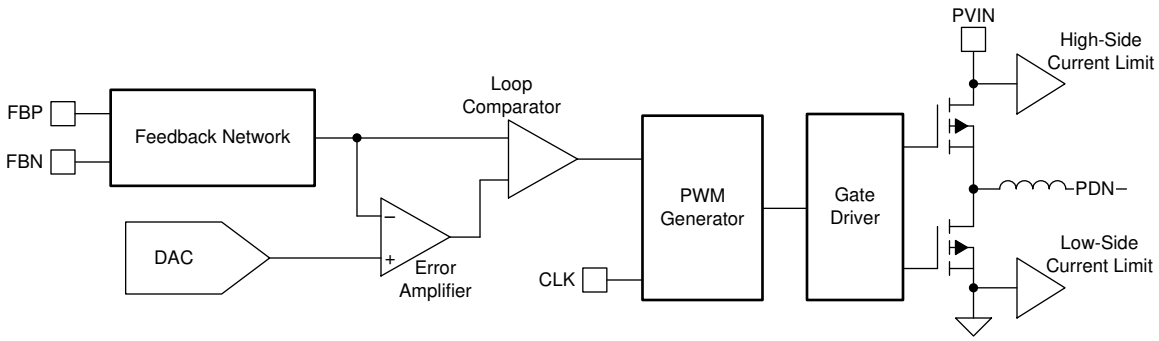

Figure 5-2. Buck Core Block Diagram

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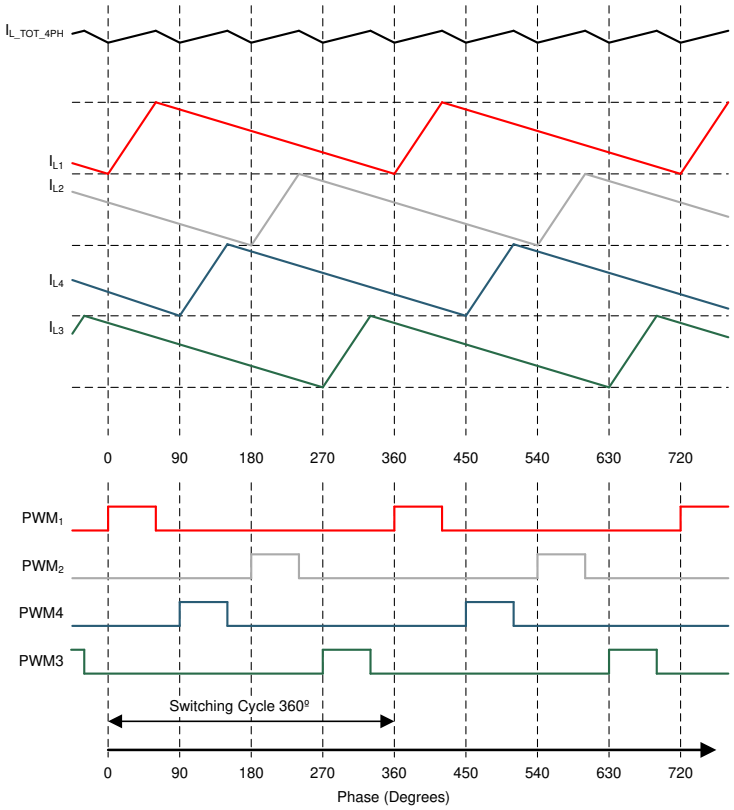

Figure 5-3. Example of PWM Timings, Inductor Current Waveforms, and Total Output Current in 4-Phase Configuration. (1)

5.3.2.1.2 Multi-Phase Operation and Phase-Adding/Shedding

Under heavy load conditions, the 4-phase converters Buck1/2/3/4 switches each channel 90° apart. As a result, the 4-phase converter has an effective ripple frequency four times greater than the switching frequency of any one phase. In the same way 3-phase converter has an effective ripple frequency three times greater and 2-phase converter has an effective ripple frequency two times greater than the switching frequency of any one phase. However, the parallel operation decreases the efficiency at light load conditions. In order to overcome this operational inefficiency, the TPS6594-Q1 can change the number of active phases to optimize efficiency for the variations of the load. This is called phase adding/shedding. The concept is shown in Figure 5-4.

The converter can be forced to multi-phase operation by the BUCKn_FPWM_MP bit in BUCKn_CTRL1 register. If the regulator operates in forced multi-phase mode (two phases in the dual-phase configuration, three phases in three-phase configuration and four phases in a four-phase configuration) the forced-PWM operation is automatically used. If the multi-phase operation is not forced, the number of phases are added and shedded automatically to follow the required output current.

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(1) Graph is not in scale and is for illustrative purposes only.

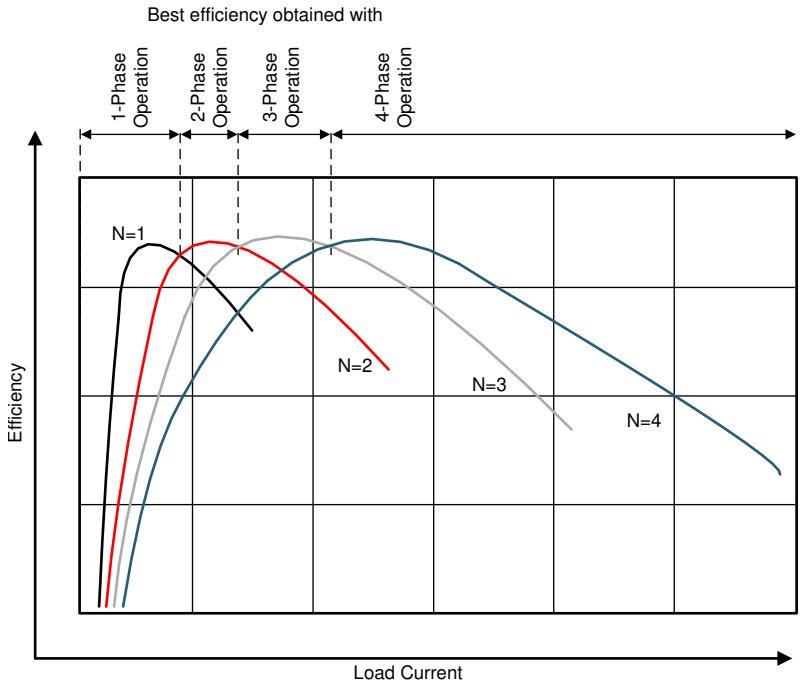

Figure 5-4. Multiphase Buck Converter Efficiency vs Number of Phases (Converters in PWM Mode) (1)

5.3.2.1.3 Transition Between PWM and PFM Modes

Force PWM mode operation with phase-adding/shedding optimizes efficiency at mid-to-full load. The TPS6594-Q1 converter operates in PWM mode at load current of about 600 mA or higher. At lighter load-current levels the device automatically switches into PFM mode for reduced current consumption when forced-PWM mode is disabled (AUTO-mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load-current range.

5.3.2.1.4 Multi-Phase Buck Regulator Configurations

In the multi-phase configuration the control of the multi-phase regulator settings is done using the control registers of the master buck. The following slave registers are ignored:

- BUCKn_CTRL register, except BUCKn_VMON_EN and BUCKn_RV_SEL
- BUCKn_CONF register
- BUCKn_VOUT_1 and BUCKn_VOUT_2 registers
- BUCKn_PG_WINDOW register
- interrupt bits related to the slave buck, except BUCKn_ILIM_INT, BUCKn_ILIM_MASK and BUCKn_ILIM_STAT

Table 5-2 shows the supported Multi-Phase buck regulator configurations and the assigned master buck in each configuration.

Table 5-2. Master Buck Assignment for Supported Multi-phase Configuration

Supported Multi-Phase Buck Regulator Configuration	Master Buck Assignment
4-Phase: BUCK1 + BUCK2 + BUCK3 + BUCK4	BUCK1
3-Phase: BUCK1 + BUCK2 + BUCK3	BUCK1
2-Phase: BUCK1 + BUCK2	BUCK1
2-Phase: BUCK3 + BUCK4	BUCK3

(1) Graph is not in scale and is for illustrative purposes only.

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When the bucks are configured in 3-phase or 4-phase configurations, there are exceptions to the above list of slave registers which are ignored. The configuration registers for the voltage monitor function on Buck3 and Buck4 in a 4-phase configuration, and Buck3 in a 3-phase configuration, are user configurable. This is because the FB_Bn pins of these bucks can be used as voltage monitor pins for external supplies. The following list of registers and register bits for Buck3 and Buck4 can be used to enable and set the target voltage for the external voltage monitoring function under such configuration:

- BUCKn_VMON_EN bit
- BUCKn_RV_SEL bit
- BUCKn_VSEL bit
- BUCKn_VOUT_1 and BUCKn_VOUT_2 registers
- BUCKn_PG_WINDOW register

Customer is responsible for setting the correct values in these registers when using Buck3 or Buck4 to monitor an external supply under the 3-phase or 4-phase configuration. If the voltage monitor function is not used under such scenario, the FB_Bn pins must be connected to the reference ground, and the BUCKn_VMON_EN and BUCKn_RV_SEL bits must be set to '0'.

5.3.2.1.5 Spread-Spectrum Mode

The TPS6594-Q1 device supports spread-spectrum modulation of the switching clocks of the buck regulators. Three factory-selectable modulation modes are available. The first mode is modulation from external input clock at the SYNCCLKIN pin. The second mode is modulating the input clock at the SYNCCLKIN pin using the DPLL. The third mode is modulating the internal 20 MHz RC Oscillator clock using the DPLL.

This is a fixed NVM option and switch-over between different modulation modes is not possible as a functional feature.

The modulation frequency range is limited by the DPLL bandwidth. The max frequency spread for the input clock to the DPLL is +/-18% to secure parametric compliance of the buck output performance.

The internal modulation is disabled by default and can be enabled and configured after power up. Internal modulation is activated by setting the SS_EN control bit. The internal modulation must be disabled (SS_EN = 0) when changing the following parameter:

- SS_DEPTH[1:0] - Spread Spectrum modulation depth
- SS_PARAM1[3:0] - Spread Spectrum parameter 1 for selecting modulation dwell time
- SS_PARAM2[3:0] - Spread Spectrum parameter 2 for selecting modulation dwell time
- SS_MODE[1:0] - Spread Spectrum modulation scheme

When internal modulation is enabled and configured, it can be disabled by the system MCU during operation. The device transition to different mission states does not impact internal modulation when it is enabled and configured.

There are 3 different modulation schemes than can be selected using the SS_MODE[1:0] EEPROM mapped bits. Additional EEPROM bits, SS_PARAM1[3:0] and SS_PARAM2[3:0], are used to set minimum and maximum dwell times

- Mixed Dwell (triangular modulation with pseudo random fm)
- Ramp Dwell (triangular modulation with triangular modulated fm)
- Blind LFSR

Traditional triangular modulation will generate a tone at f_m. Ramp Dwell and Mixed Dwell are used to attenuate the tone at f_m.

Table 5-3. MODCLK Modulation Options

MODULATION OPTION	SS_MODE[1:0]	SS_PARAM2[3:0]	SS_PARAM1[3:0]
No modulation	00b	X	X

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Table 5-3. MODCLK Modulation Options (continued)

MODULATION OPTION	SS_MODE[1:0]	SS_PARAM2[3:0]	SS_PARAM1[3:0]
Mixed dwell	01b	Maximum dwell	Minimum dwell
Blind LFSR	10b	Fixed dwell	Maximum step
Ramp dwell	11b	Maximum dwell	Minimum dwell

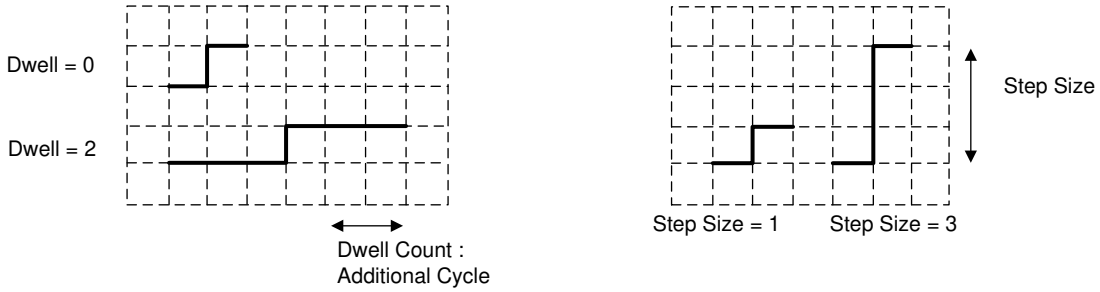

Figure 5-5. Internal Spread-Spectrum Configuration Options (Controlled through EEPROM-Mapped Bits)

5.3.2.1.5.1 Mixed Dwell Spread-Spectrum Modulation

- In this scheme, frequency will change in a triangular fashion through varying the spread spectrum DAC.
- he time interval between each DAC code is determined based on maximum dwell and minimum dwell.
- The dwell count only changes after one complete cycle of DAC codes (0->F->0)
- At the start of each cycle, pick a new dwell count between maximum dwell and minimum dwell based on an LFSR counter.

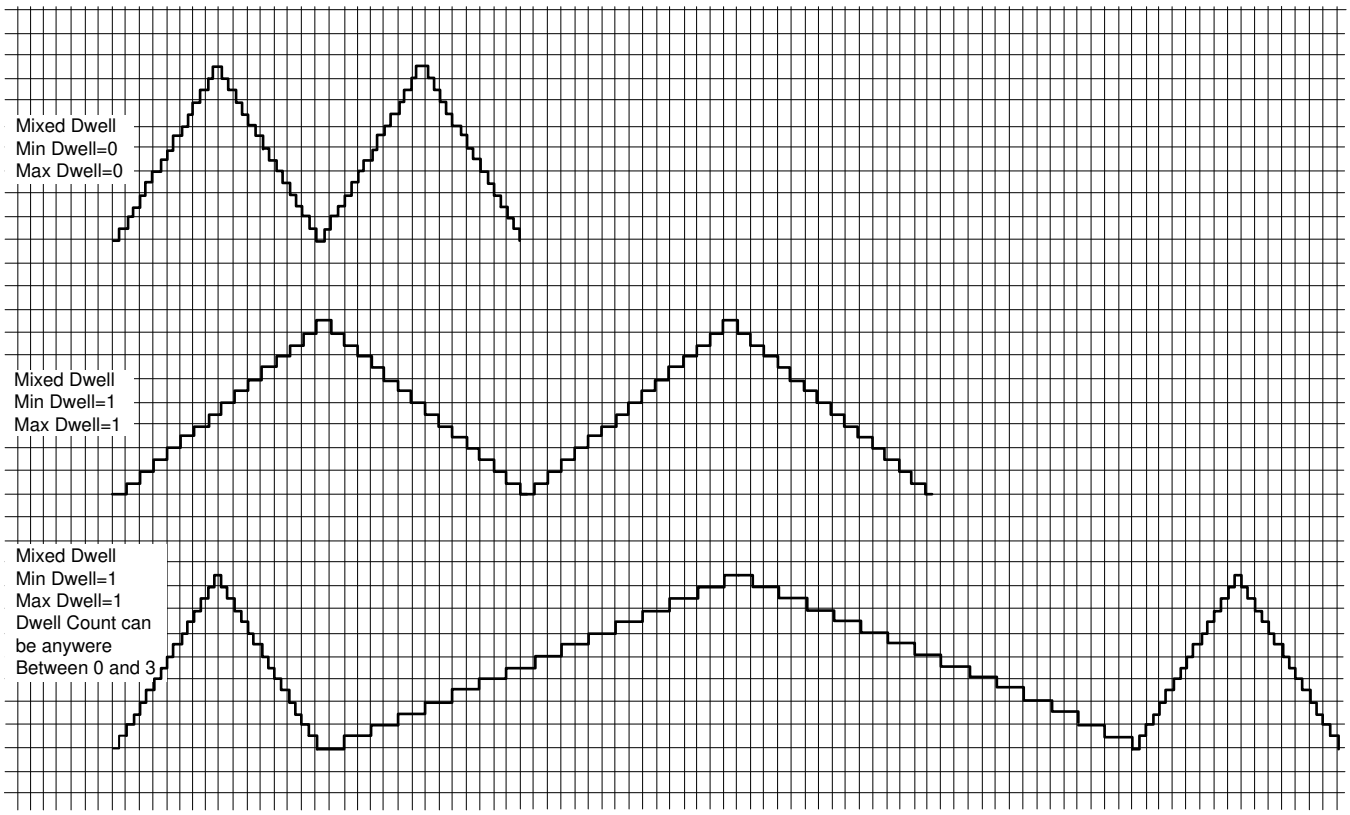

Figure 5-6. Mixed-Dwell SSM (DAC Code-Cycles Example)

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5.3.2.1.5.2 Ramp Dwell Spread Spectrum Modulation

- In this scheme, frequency changes in a triangular fashion through varying the spread spectrum DAC.
- The time interval between each DAC code is determined based on maximum dwell and minimum dwell
- The dwell count changes in a triangular fashion. In other words, the next dwell count is current dwell count + 1 until the maximum dwell count is reached. When the maximum dwell count is reached, the direction changes and next dwell count is current dwell count -1 until it the minimum dwell count is reached. This cycle repeats.
- The dwell count only changes after one complete cycle of DAC codes (0->F->0)

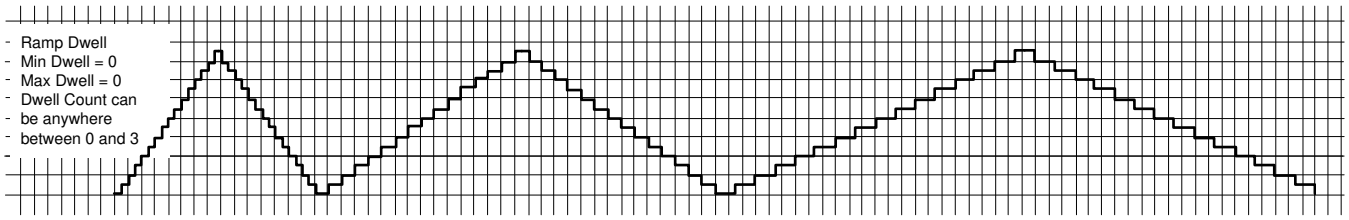

Figure 5-7. Ramp Dwell SSM (DAC Code-Cycles Example)

5.3.2.1.5.3 Blind LFSR Spread-Spectrum Modulation

This scheme uses the LFSR to pick the next DAC code. The new DAC code is within the “max_step” of the previous value. A new DAC code is picked each “fixed_step” number of clocks set by SS_2_CFG[7:4] EEPROM bits

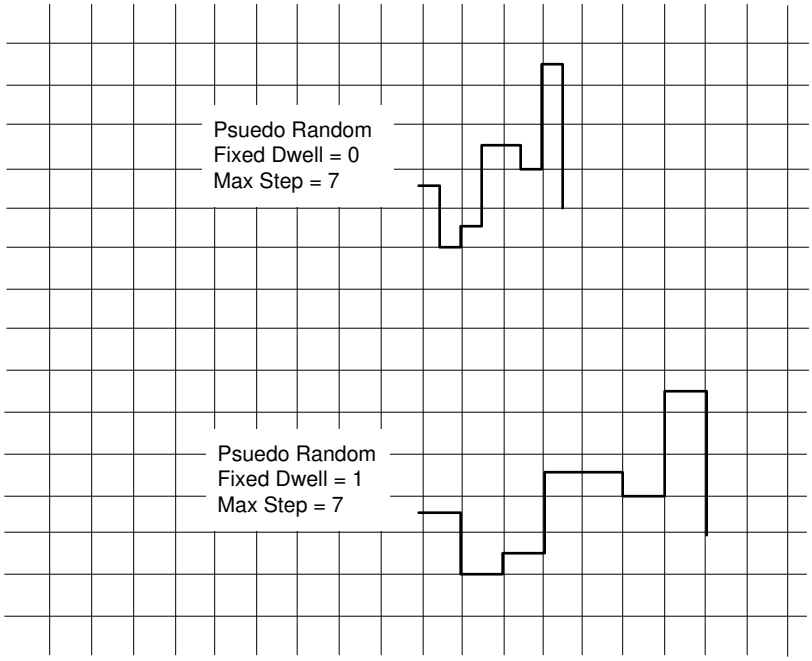

Figure 5-8. Blind LFSR SSM (DAC Code-Cycles Example)

5.3.2.1.6 Adaptive Voltage Scaling (AVS) and Dynamic Voltage Scaling (DVS) Support

An AVS or a DVS voltage value can be configured by the attached MCU after the buck regular is powered up to the default output voltage selected in register BUCKn_VSET1, which loads its default value from NVM. The purpose of the AVS/DVS voltage is to set the buck output voltage to enable optimal efficiency and performance of the attached SoC.

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All of bucks on the TPS6594-Q1 device support AVS and DVS voltage scaling changes. Once the AVS/DVS voltage value is written into the BUCKn_VSET1 or BUCKn_VSET2 register, and the MCU sets the BUCKn_VSEL register to select the AVS/DVS voltage, the output of the buck will maintain the AVS/DVS voltage level instead of the default voltage from NVM until any one of the following event occurs:

- Error that causes the device to re-initialize itself through a power cycle after reaching the SAFE RECOVERY state
- Error that causes the device to execute warm reset
- MCU configures the device to enter the LP STANDBY state

Figure 5-9 shows the arbitration scheme for loading the buck output level from the AVS register using the BUCKn_VSET control registers.

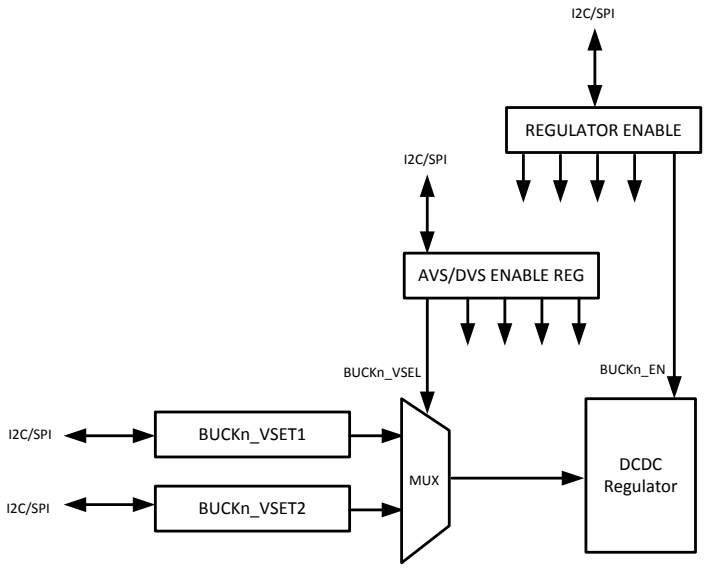

Figure 5-9. AVS/DVS Configuration Register Arbitration Diagram

During the AVS or DVS voltage change , the OV and UV threshold of the buck output voltage monitor will be updated automatically by the digital control block. When the output voltage is increased, the OV threshold is updated at the same time the BUCKn_VSETx is updated to the AVS voltage level, while the UV threshold is updated after a delay calculated by Equation 1.

When the output voltage is decreased, the UV threshold is updated at the same time the BUCKn_VSETx is updated to the AVS voltage level, while the OV threshold is updated after a delay calculated by Equation 1.

$$t_{PG\_OV\_UV\_DELAY} = (dV / BUCKn\_SLEW\_RATE) + t_{settle\_Bx} \quad (1)$$

In order to prevent erroneous voltage monitoring, the digital block also temporarily mask the results of the OV and UV monitor from the regulator output when the buck is enabled and the voltage is rising to the BUCKn_VSETx level. The duration of the mask starts from the time the buck is enabled. The buck OV monitor output is masked for a fixed delay time of $t_{PG\_OV\_GATE}$, which is approximately 115 µs - 128 µs. The UV monitor output is masked for the time duration calculated by Equation 2. The 370 µs additional delay time in the formula includes the start-up delay of the buck, the fixed delay after the ramp, and the time for the BIST operation of the OV and UV monitors.

$$t_{PG\_UV\_GATE} = (BUCKn\_VSEL / BUCKn\_SLEW\_RATE) + 370\ \mu s \quad (2)$$

Figure 5-10 and Figure 5-11 are timing diagrams illustrating the voltage change for AVS and DVS enabled bucks and the corresponding OV and UV monitor threshold changes.

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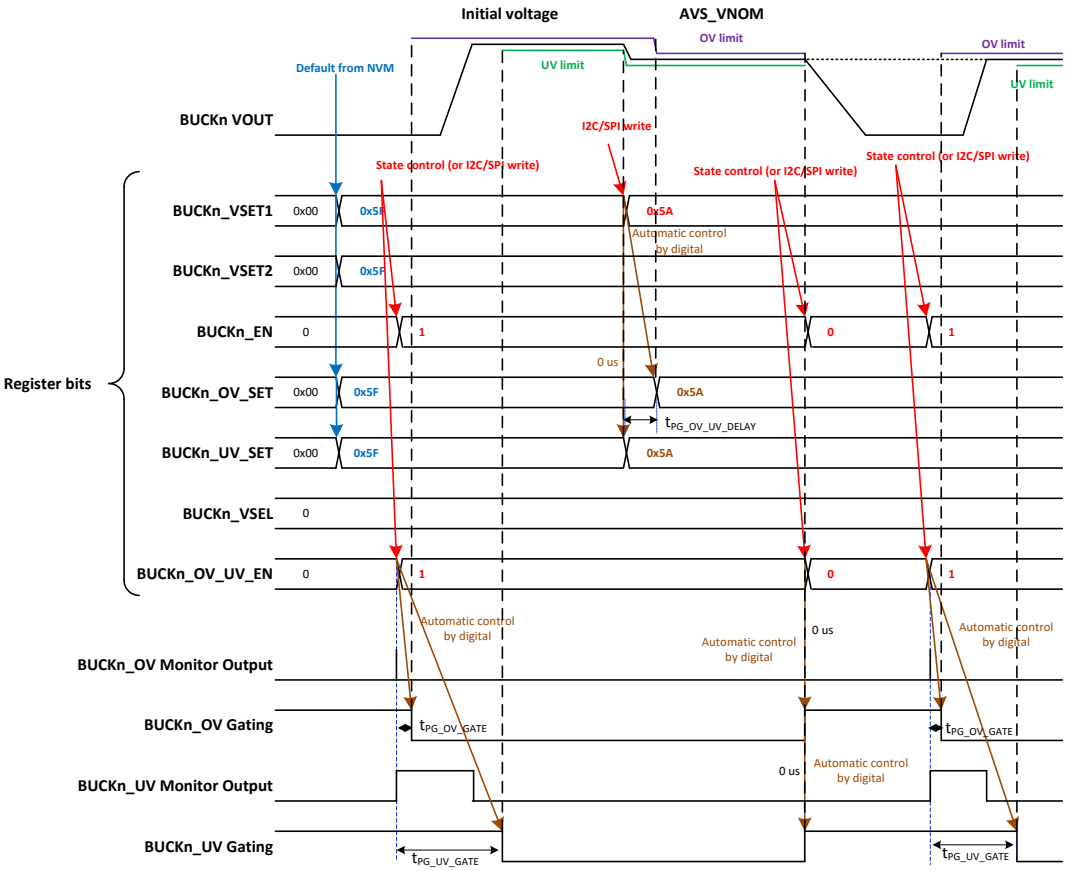

Figure 5-10. AVS Voltage and OV UV Threshold Level Change Timing Diagram

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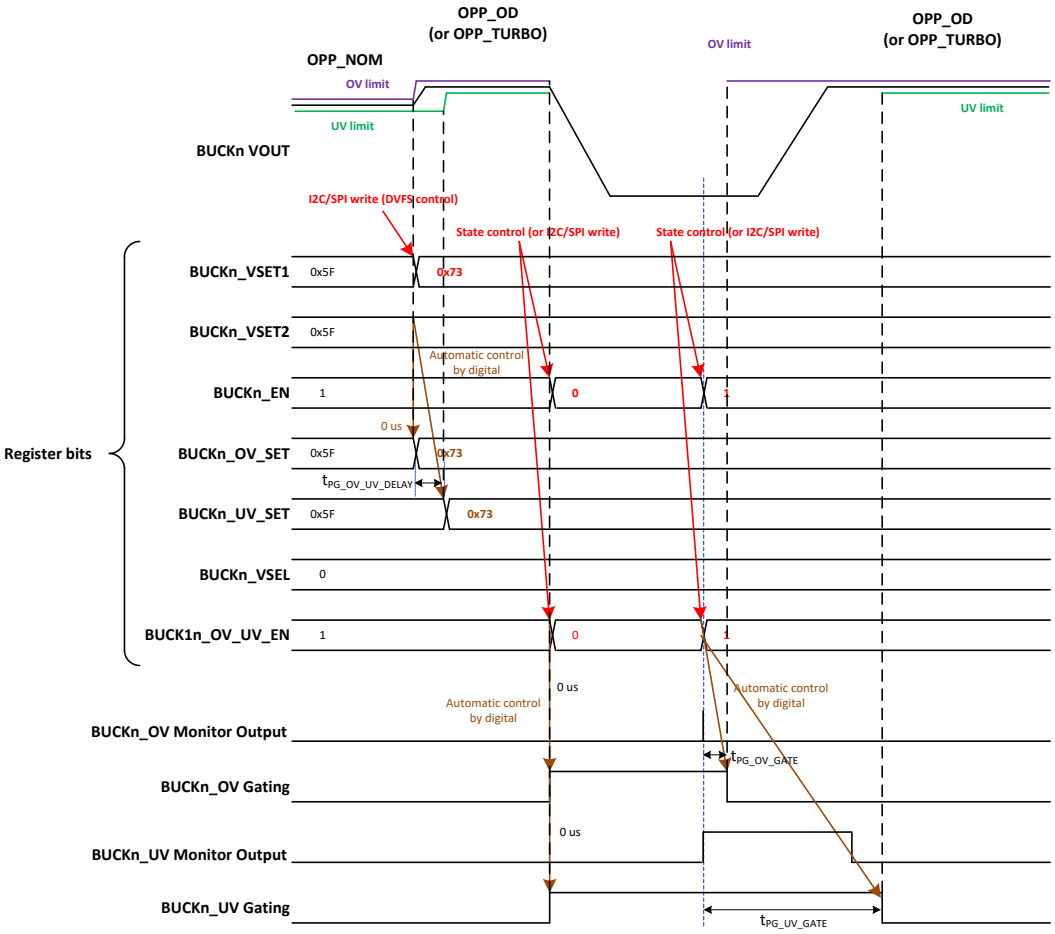

Figure 5-11. DVS Voltage and OV UV Threshold Level Change Timing Diagram

5.3.2.1.7 Buck Output Voltage Setting

The buck output voltage is selected using the coding shown in Table 5-4.

Table 5-4. Output Voltage Selection for Buck Regulators

BUCKn_ VSETn	Output Voltage [V] 20 mV steps	BUCKn_ VSETn	Output Voltage [V] 5 mV steps	BUCKn_ VSETn	Output Voltage [V] 5 mV steps	BUCKn_ VSETn	Output Voltage [V] 10 mV steps	BUCKn_ VSETn	Output Voltage [V] 20 mV steps	BUCKn_ VSETn	Output Voltage [V] 20 mV steps
0x00	0.3	0x0F	0.6	0x41	0.85	0x73	1.1	0xAB	1.66	0xD6	2.52
0x01	0.32	0x10	0.605	0x42	0.855	0x74	1.11	0xAC	1.68	0xD7	2.54
0x02	0.34	0x11	0.61	0x43	0.86	0x75	1.12	0xAD	1.7	0xD8	2.56
0x03	0.36	0x12	0.615	0x44	0.865	0x76	1.13	0xAE	1.72	0xD9	2.58
0x04	0.38	0x13	0.62	0x45	0.87	0x77	1.14	0xAF	1.74	0xDA	2.6
0x05	0.4	0x14	0.625	0x46	0.875	0x78	1.15	0xB0	1.76	0xDB	2.62
0x06	0.42	0x15	0.63	0x47	0.88	0x79	1.16	0xB1	1.78	0xDC	2.64
0x07	0.44	0x16	0.635	0x48	0.885	0x7A	1.17	0xB2	1.8	0xDD	2.66
0x08	0.46	0x17	0.64	0x49	0.89	0x7B	1.18	0xB3	1.82	0xDE	2.68
0x09	0.48	0x18	0.645	0x4A	0.895	0x7C	1.19	0xB4	1.84	0xDF	2.7
0x0A	0.5	0x19	0.65	0x4B	0.9	0x7D	1.2	0xB5	1.86	0xE0	2.72
0x0B	0.52	0x1A	0.655	0x4C	0.905	0x7E	1.21	0xB6	1.88	0xE1	2.74
0x0C	0.54	0x1B	0.66	0x4D	0.91	0x7F	1.22	0xB7	1.9	0xE2	2.76

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Table 5-4. Output Voltage Selection for Buck Regulators (continued)

BUCKn_ VSETn	Output Voltage [V] 20 mV steps	BUCKn_ VSETn	Output Voltage [V] 5 mV steps	BUCKn_ VSETn	Output Voltage [V] 5 mV steps	BUCKn_ VSETn	Output Voltage [V] 10 mV steps	BUCKn_ VSETn	Output Voltage [V] 20 mV steps	BUCKn_ VSETn	Output Voltage [V] 20 mV steps
0x0D	0.56	0x1C	0.665	0x4E	0.915	0x80	1.23	0xB8	1.92	0xE3	2.78
0x0E	0.58	0x1D	0.67	0x4F	0.92	0x81	1.24	0xB9	1.94	0xE4	2.8
		0x1E	0.675	0x50	0.925	0x82	1.25	0xBA	1.96	0xE5	2.82
		0x1F	0.68	0x51	0.93	0x83	1.26	0xBB	1.98	0xE6	2.84
		0x20	0.685	0x52	0.935	0x84	1.27	0xBC	2	0xE7	2.86
		0x21	0.69	0x53	0.94	0x85	1.28	0xBD	2.02	0xE8	2.88
		0x22	0.695	0x54	0.945	0x86	1.29	0xBE	2.04	0xE9	2.9
		0x23	0.7	0x55	0.95	0x87	1.3	0xBF	2.06	0xEA	2.92
		0x24	0.705	0x56	0.955	0x88	1.31	0xC0	2.08	0xEB	2.94
		0x25	0.71	0x57	0.96	0x89	1.32	0xC1	2.1	0xEC	2.96
		0x26	0.715	0x58	0.965	0x8A	1.33	0xC2	2.12	0xED	2.98
		0x27	0.72	0x59	0.97	0x8B	1.34	0xC3	2.14	0xEE	3.0
		0x28	0.725	0x5A	0.975	0x8C	1.35	0xC4	2.16	0xEF	3.02
		0x29	0.73	0x5B	0.98	0x8D	1.36	0xC5	2.18	0xF0	3.04
		0x2A	0.735	0x5C	0.985	0x8E	1.37	0xC6	2.2	0xF1	3.06
		0x2B	0.74	0x5D	0.99	0x8F	1.38	0xC7	2.22	0xF2	3.08
		0x2C	0.745	0x5E	0.995	0x90	1.39	0xC8	2.24	0xF3	3.1
		0x2D	0.75	0x5F	1.0	0x91	1.4	0xC9	2.26	0xF4	3.12
		0x2E	0.755	0x60	1.005	0x92	1.41	0xCA	2.28	0xF5	3.14
		0x2F	0.76	0x61	1.01	0x93	1.42	0xCB	2.3	0xF6	3.16
		0x30	0.765	0x62	1.015	0x94	1.43	0xCC	2.32	0xF7	3.18
		0x31	0.77	0x63	1.02	0x95	1.44	0xCD	2.34	0xF8	3.2
		0x32	0.775	0x64	1.025	0x96	1.45	0xCE	2.36	0xF9	3.22
		0x33	0.78	0x65	1.03	0x97	1.46	0xCF	2.38	0xFA	3.24
		0x34	0.785	0x66	1.035	0x98	1.47	0xD0	2.4	0xFB	3.26
		0x35	0.79	0x67	1.04	0x99	1.48	0xD1	2.42	0xFC	3.28
		0x36	0.795	0x68	1.045	0x9A	1.49	0xD2	2.44	0xFD	3.3
		0x37	0.8	0x69	1.05	0x9B	1.5	0xD3	2.46	0xFE	3.32
		0x38	0.805	0x6A	1.055	0x9C	1.51	0xD4	2.48	0xFF	3.34
		0x39	0.81	0x6B	1.06	0x9D	1.52	0xD5	2.5		
		0x3A	0.815	0x6C	1.065	0x9E	1.53				
		0x3B	0.82	0x6D	1.07	0x9F	1.54				
		0x3C	0.825	0x6E	1.075	0xA0	1.55				
		0x3D	0.83	0x6F	1.08	0xA1	1.56				
		0x3E	0.835	0x70	1.085	0xA2	1.57				
		0x3F	0.84	0x71	1.09	0xA3	1.58				
		0x40	0.845	0x72	1.095	0xA4	1.59				
						0xA5	1.6				
						0xA6	1.61				
						0xA7	1.62				
						0xA8	1.63				
						0xA9	1.64				
						0xAA	1.65				

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5.3.2.2 Sync Clock Functionality

The TPS6594-Q1 device contains a SYNCCLKIN (GPIO10) input to synchronize switching clock of the buck regulator with the external clock. The block diagram of the clocking and PLL module is shown in 图 5-12. The external clock is selected when the external clock is available, and SEL_EXT_CLK = '1'. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[1:0] bits in the NVM and it can be 1.1 MHz, 2.2 MHz, or 4.4 MHz. The external SYNCCLKIN clock must be inside accuracy limits (–18%/+18%) of the typical input frequency for valid clock detection.

The EXT_CLK_INT interrupt is generated in cases the external clock is expected (SEL_EXT_CLK = 1), but it is not available or the clock frequency is not within the valid range.

The TPS6594-Q1 device can also generate clock SYNCCLKOUT for external device use. The SYNCCLKOUT is available through GPIO8, GPIO9, or GPIO10.

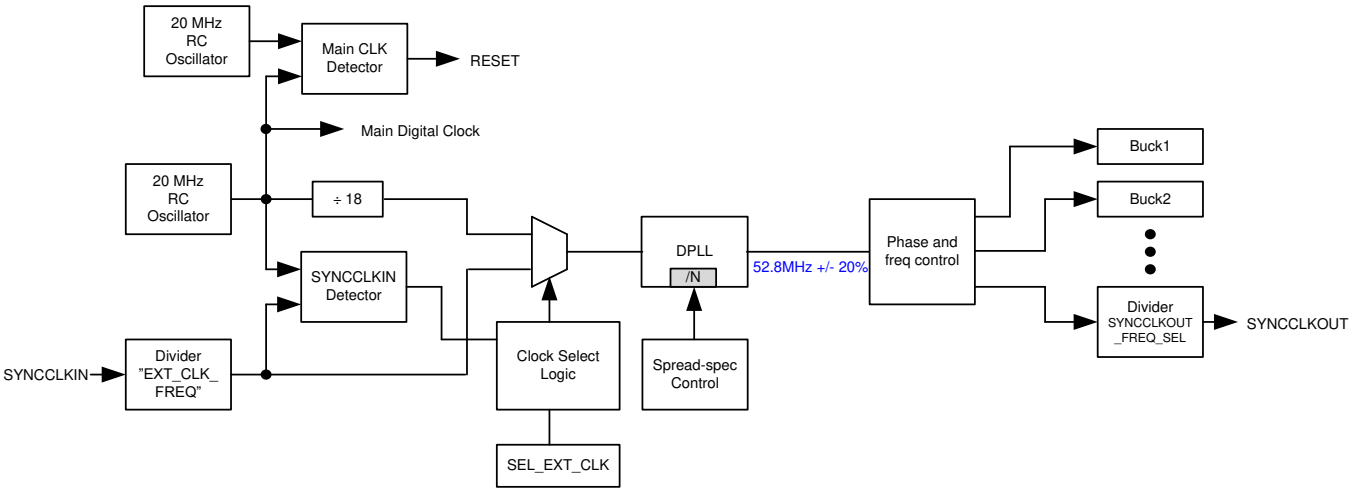

图 5-12. Sync Clock and DPLL Module

5.3.2.3 Low Dropout Regulators (LDOs)

All of the LDO regulators in the TPS6594-Q1 device can be supplied by the system supply or another pre-regulated voltage source which are within the specified VIN range. The PVIN_LDOn voltage level must be equal or less than the VCCA voltage level to ensure proper operation of the LDOs. The default output voltages of all LDOs are loaded from the NVM memory and can be configured by the LDOn_VSET[7:0]. There is no hardware protection to prevent software from selecting an improper output voltage if the minimum level of PVIN_LDOn is lower than the dropout voltage of the LDO regulator in addition to the configured LDO output voltage. In such conditions, the output voltage will droop to near the PVIN_LDOn level. Writing a "RESERVED" value to the LDOn_VSET[7:0] register bits will trigger a LDOn_OV_INT or LDOn_UV_INT interrupt.

If an LDO is not needed, it can be used as a voltage monitor for an external rail by connecting it to the VOUT_LDOn pin. The voltage output level to be monitored must be within the PGOOD monitor range of the LDOn_VSET[7:0] of the LDO. If external resistor divider is necessary in this case, the user must take into account of the input impedance at the VOUT_LDOn pin as shown in 图 5-13, and adjust the resistor values to compensate for the voltage shift.

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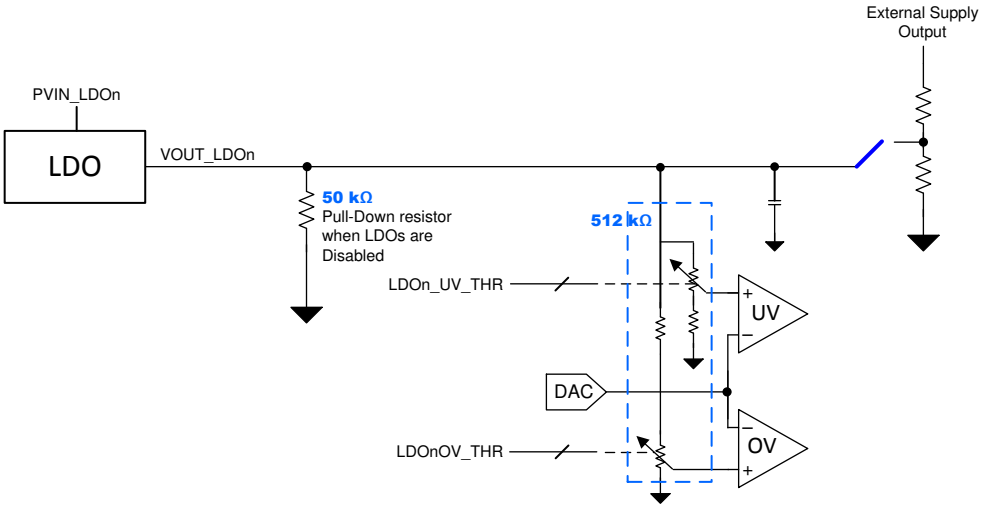

图 5-13. Impedance at the VOUT_LDOn pins

5.3.2.3.1 LDOVINT

The LDOVINT voltage regulator is dedicated to supply the digital and analog functions of the TPS6594-Q1 device which are not required to be always-on and can be turned-off when the device is in low power states, such as various monitoring circuits. The LDOVINT regulator is automatically enabled and disabled as needed. The automatic control optimizes the overall current consumption when the device is in low power LP_STANDBY state.

5.3.2.3.2 LDOVRTC

The LDOVRTC regulator supplies always-on functions, such as wake-up functions. This power resource is active as soon as a valid energy source is present.

This resource runs in normal mode or backup mode. The LDOVRTC regulator functions in normal mode when supplied from the main system power rail and is able to supply the GPIO, the digital components, the crystal and the RTC calendar module of the TPS6594-Q1 device. The LDOVRTC regulator remains on in BACKUP state when VCCA is below the VCCA_UVLO level, and the backup power source is above the LDOVRTC_UVLO level.

In BACKUP state, only the 32 kHz crystal and the RTC counter are activation. In the LP STANDBY state, the RTC calendar function will remain active, but the interrupt functions are reduced to maintaining the wake up functions only. In the ACTIVE and MCU_ONLY/SLEEP states, the RTC calendar and interrupt functions are fully activated.

Customer has the option to enable the *shelf mode* by setting the LDORTC_DIS bit to 1 while the device is in MISSION state and the I2C bus is in operation, and ramp down VCCA to 0V immediately after the I2C write has completed. This bit will force the device to skip the BACKUP state and enters the NO SUPPLY state under VCCA_UVLO condition. This mode is useful to prevent the continual draining of the back up power source when the 32 KHz crystal and RTC counter functions are no longer needed.

5.3.2.3.3 LDO1, LDO2, and LDO3

The LDO1, LDO2 and LDO3 regulators can deliver up to 500 mA of current, with a configurable output range of 0.6 V to 3.3 V in 50 mV steps. These 3 LDO regulators also support bypass mode, which allows an input voltage at the PVIN_LDOn to show up at the VOUT_LDOn pin. This feature allows the LDOs to be configured as load switches with power sequencing control. As also in 节 5.3.2.3, an un-used regulator can also be used as a voltage monitor for an external rail by connected the external rail to the VOUT_LDOn pin.

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The bypass capability to connect the input voltage to the output in bypass mode is supported when the input voltage is within the 1.7 V to 3.5 V range. As an SD card I/O supply, this bypass capability also allows the LDO to switch from 3.3 V in bypass mode to 1.8 V in LDO mode, or switch from 1.8 V in LDO mode to 3.3 V in bypass mode.

When changing the LDO output voltage setting, it is important to wait until the LDO has settle on the target voltage from the previous change. The worst case voltage scaling time for LDO1, LDO2, and LDO3 is 63 µs x (7 + the number of 50 mV steps to the new target voltage).

The output voltage for LDO1, LDO2, and LDO3 is selected using the coding shown in 表 5-5

表 5-5. Output Voltage Selection for LDO1, LDO2, and LDO3

LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]
0x00	Reserved	0x10	1.20	0x20	2.00	0x30	2.80
0x01	Reserved	0x11	1.25	0x21	2.05	0x31	2.85
0x02	Reserved	0x12	1.30	0x22	2.10	0x32	2.90
0x03	Reserved	0x13	1.35	0x23	2.15	0x33	2.95
0x04	0.60	0x14	1.40	0x24	2.20	0x34	3.00
0x05	0.65	0x15	1.45	0x25	2.25	0x35	3.05
0x06	0.70	0x16	1.50	0x26	2.30	0x36	3.10
0x07	0.75	0x17	1.55	0x27	2.35	0x37	3.15
0x08	0.80	0x18	1.60	0x28	2.40	0x38	3.20
0x09	0.85	0x19	1.65	0x29	2.45	0x39	3.25
0x0A	0.90	0x1A	1.70	0x2A	2.50	0x3A	3.30
0x0B	0.95	0x1B	1.75	0x2B	2.55	0x3B	Reserved
0x0C	1.00	0x1C	1.80	0x2C	2.60	0x3C	Reserved
0x0D	1.05	0x1D	1.85	0x2D	2.65	0x3D	Reserved
0x0E	1.10	0x1E	1.90	0x2E	2.70	0x3E	Reserved
0x0F	1.15	0x1F	1.95	0x2F	2.75	0x3F	Reserved

5.3.2.3.4 Low-Noise LDO (LDO4)

The LDO4 regulator can deliver up to 300 mA of current, with a configurable output range of 1.2 V to 3.3 V in 25 mV steps. This LDO is specifically designed to supply noise sensitive circuits. This supply can be used to power circuits such as PLLs, oscillators, or other analog modules that require low noise on the supply. LDO4 does not support bypass mode. However it can also be used as a external voltage monitor if its regulator function is not needed.

The output voltage for LDO4 is elected using the coding shown in 表 5-6

表 5-6. Output Voltage Selection for LDO4

LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]
0x00	Reserved	0x20	1.200	0x40	2.000	0x60	2.800
0x01	Reserved	0x21	1.225	0x41	2.025	0x61	2.825
0x02	Reserved	0x22	1.250	0x42	2.050	0x62	2.850
0x03	Reserved	0x23	1.275	0x43	2.075	0x63	2.875
0x04	Reserved	0x24	1.300	0x44	2.100	0x64	2.900
0x05	Reserved	0x25	1.325	0x45	2.125	0x65	2.925
0x06	Reserved	0x26	1.350	0x46	2.150	0x66	2.950
0x07	Reserved	0x27	1.375	0x47	2.175	0x67	2.975
0x08	Reserved	0x28	1.400	0x48	2.200	0x68	3.000

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表 5-6. Output Voltage Selection for LDO4 (continued)

LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]
0x09	Reserved	0x29	1.425	0x49	2.225	0x69	3.025
0x0A	Reserved	0x2A	1.450	0x4A	2.250	0x6A	3.050
0x0B	Reserved	0x2B	1.475	0x4B	2.275	0x6B	3.075
0x0C	Reserved	0x2C	1.500	0x4C	2.300	0x6C	3.100
0x0D	Reserved	0x2D	1.525	0x4D	2.325	0x6D	3.125
0x0E	Reserved	0x2E	1.550	0x4E	2.350	0x6E	3.150
0x0F	Reserved	0x2F	1.575	0x4F	2.375	0x6F	3.175
0x10	Reserved	0x30	1.600	0x50	2.400	0x70	3.200
0x11	Reserved	0x31	1.625	0x51	2.425	0x71	3.225
0x12	Reserved	0x32	1.650	0x52	2.450	0x72	3.250
0x13	Reserved	0x33	1.675	0x53	2.475	0x73	3.275
0x14	Reserved	0x34	1.700	0x54	2.500	0x74	3.300
0x15	Reserved	0x35	1.725	0x55	2.525	0x75	Reserved
0x16	Reserved	0x36	1.750	0x56	2.550	0x76	Reserved
0x17	Reserved	0x37	1.775	0x57	2.575	0x77	Reserved
0x18	Reserved	0x38	1.800	0x58	2.600	0x78	Reserved
0x19	Reserved	0x39	1.825	0x59	2.625	0x79	Reserved
0x1A	Reserved	0x3A	1.850	0x5A	2.650	0x7A	Reserved
0x1B	Reserved	0x3B	1.875	0x5B	2.675	0x7B	Reserved
0x1C	Reserved	0x3C	1.900	0x5C	2.700	0x7C	Reserved
0x1D	Reserved	0x3D	1.925	0x5D	2.725	0x7D	Reserved
0x1E	Reserved	0x3E	1.950	0x5E	2.750	0x7E	Reserved
0x1F	Reserved	0x3F	1.975	0x5F	2.775	0x7F	Reserved

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5.3.3 Residual Voltage Checking

The residual voltage (RV) checking feature ensures the voltage level at the buck or LDO regulators is below $V_{TH\_SC\_RV}$ before it can be ramped up the target output voltage. If BUCKn/LDOn_RV_SEL=1 by default, residual voltage is also checked before the device enters BOOT_BIST state. If the residual voltage at the output of the regulators is greater than $V_{TH\_SC\_RV}$, the device waits until voltage goes below $V_{TH\_SC\_RV}$ before starting BOOT_BIST or the voltage ramp up.

This feature is enabled by the BUCKn_VMON_EN and BUCKn_RV_SEL bits for each buck regulators, and by the LDOn_VMON_EN and LDOn_RV_SEL bits for each LDO regulators. When this feature is enabled, the VMON of the corresponding regulator will remain on after the regulator is disabled, and remain on for the RV Timeout period. After the RV Timeout period elapses the output voltage of the regulator will be compared to the SC threshold of $V_{TH\_SC\_RV}$, and assert the corresponding BUCKn_SC_INT or LDOn_SC_INT interrupt bits if the residual voltage is still higher than the threshold voltage. The RV timeout period for the BUCK regulators is automatically calculated by the digital controller inside the device by 公式 3. The RV timeout period of the LDO regulator is configured by the LDOn_RV_TIMEOUT[3:0].

$$t_{BUCK\_RV\_TIMEOUT} = BUCKn\_VSET / BUCKn\_SLEW\_RATE + 100\ \mu s \quad (3)$$

The residual voltage check can also be performed on external rails when they are connected to unused LDO regulator outputs.

图 5-14 shows the timing diagram of the residual voltage checking operation which results in pass or fail results.

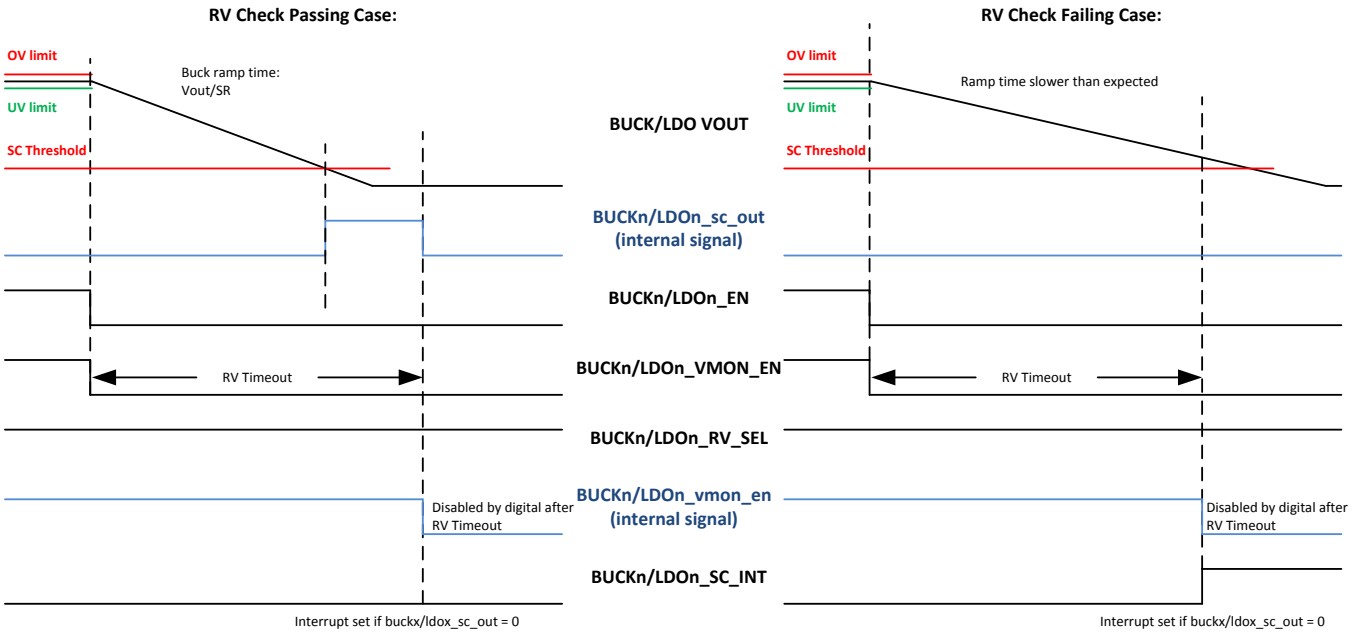

图 5-14. Residual Voltage Check Timing Diagram

5.3.4 Output Voltage Monitor and PGOOD Generation

The TPS6594-Q1 device monitors the UV and OV conditions of the output voltage of the bucks and LDOs, as well as VCCA when it is expected to be 5 V or 3.3 V, and indicate result with PGOOD signal. Thermal warning can also be included in the result of the PGOOD monitor if it is not masked. Either voltage and current monitoring or a voltage monitoring only can be selected for PGOOD indication. This selection is set by the PGOOD_SEL_BUCKn register bits for each buck regulator (select master phase for multi-phase regulator), and is set by the PGOOD_SEL_LDOn register bits for each LDO regulator. When both voltage and current are monitored, PGOOD signal active indicates that the regulator output is inside the Power-Good voltage window and that load current is below the current limit. If only voltage is monitored, then the current monitoring is ignored for the PGOOD signal.

When a buck or a LDO is not needed as a regulated output, it can be used as a voltage monitor for an extern rail. For buck converters, if the BUCKn_VMON_EN bit remains '1' while the BUCKn_EN bit is '0', it can be used as a voltage monitor for an external rail which is connected to the buck converter's FB_Bn pin. For LDO regulators, if the LDOn_VMON_EN bit remains '1' while the LDOn_EN bit is '0', it can be used as a voltage monitor for an external rail which is connected to the VOUT_LDOn pin. External resistor dividers may be necessary in this case to ensure the external voltage is equal to or within the PGOOD monitor range of the active BUCKn_VSETn[7:0] of the buck, selected by the BUCKn_VSEL register bit, or LDOn_VSET[7:0] of the LDO.

When the monitor for a buck or a LDO regulator is disabled, the output of the corresponding monitor is automatically masked to prevent it from forcing PGOOD inactive. This allows connecting PGOOD signals from various devices together when open-drain outputs are used.

An NVM option is available to gate the PGOOD output with the nRSTOUT and the nRSTOUT_SoC signals. When PGOOD_SEL_NRSTOUT = '1', the PGOOD pin is gated by the nRSTOUT signal. When PGOOD_SEL_NRSTOUT_SOC = '1', the PGOOD pin is gated by the nRSTOUT_SoC signal. This option allows the PGOOD output to be used as an enable/reset signal for external peripherals.

The monitoring from all the output rails are combined, and PGOOD is active only if all the sources shows active status.

The type of output voltage monitoring for PGOOD signal is selected by PGOOD_WINDOW bit. If the bit is 0, only undervoltage is monitored; if the bit is 1, both undervoltage and over-voltage are monitored.

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The polarity and the output type (push-pull or open-drain) are selected by PGOOD_POL and GPIO9_OD bits.

The Power-Good generation block diagram is shown in Figure 5-15. The Power-Good waveforms are shown in Figure 5-16.

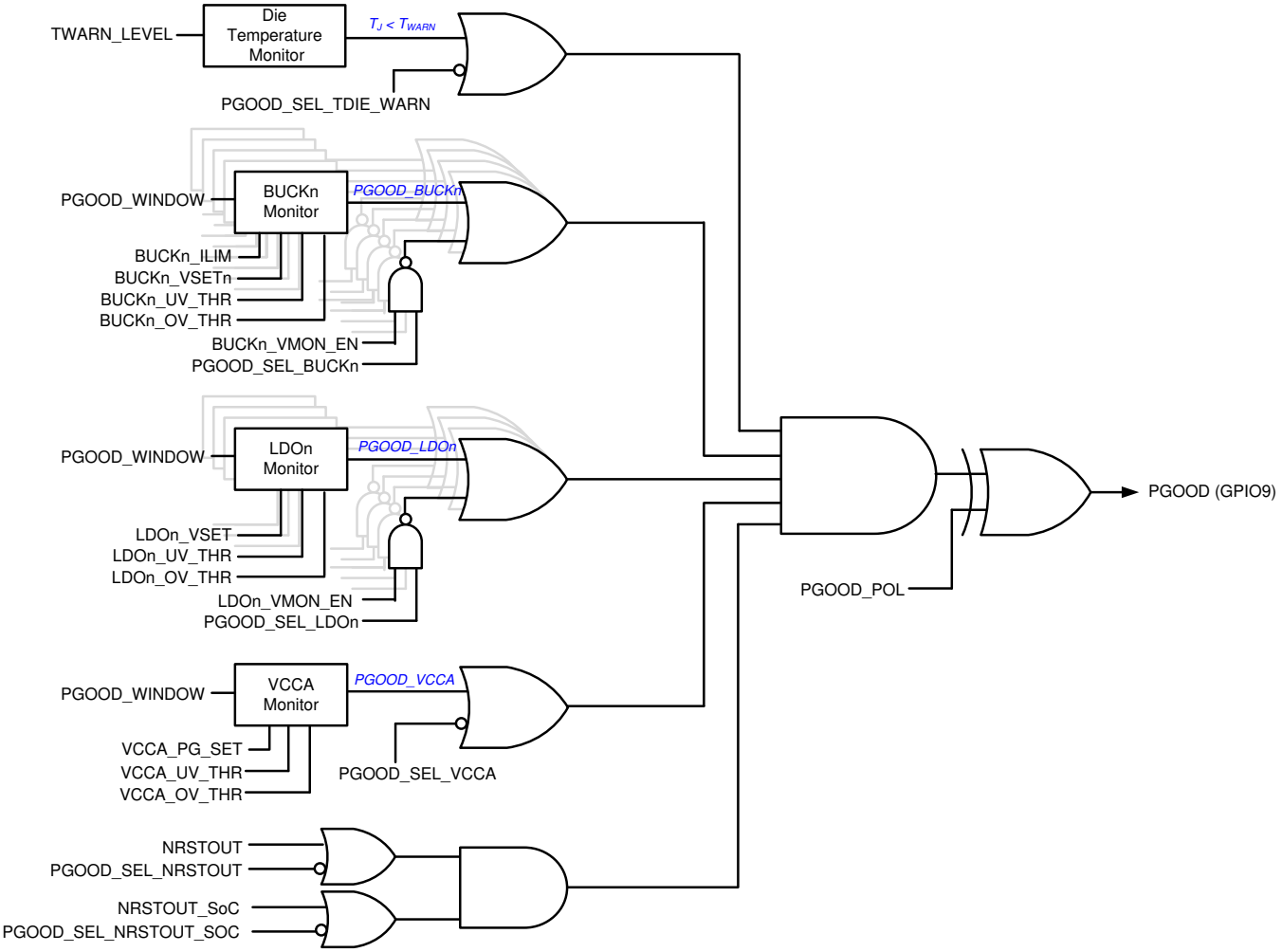

Figure 5-15. PGOOD Block Diagram

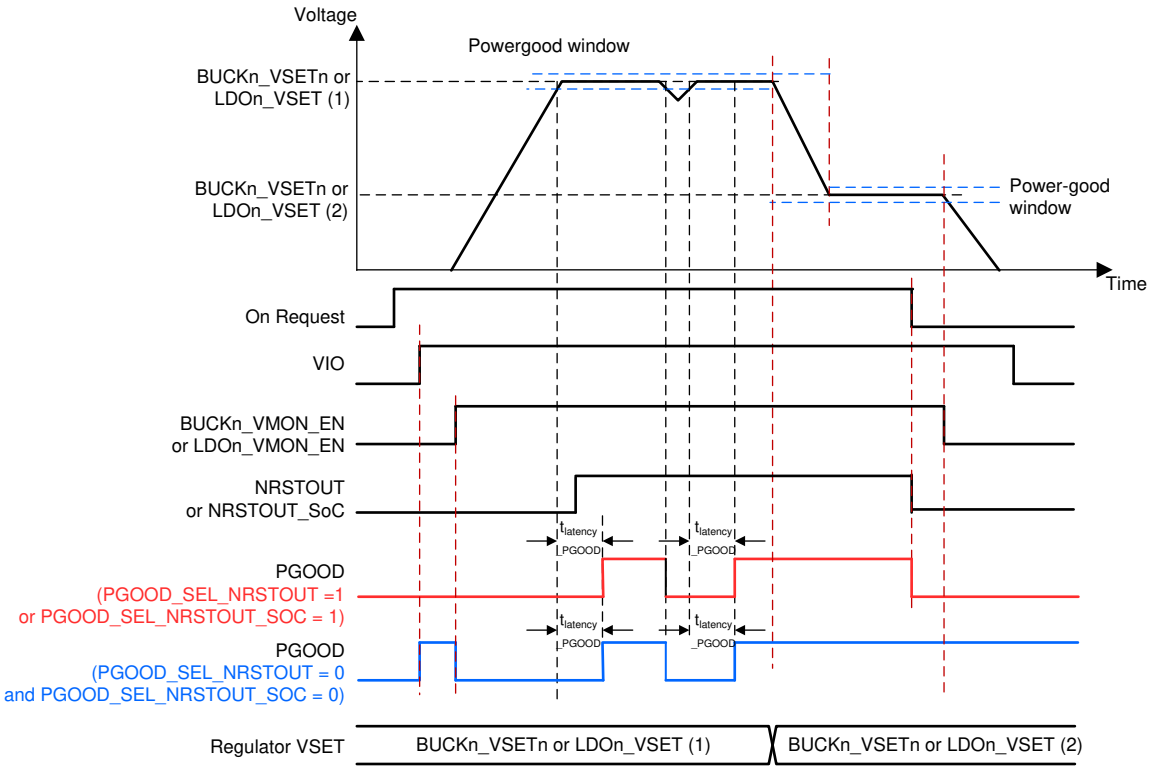

Figure 5-16. PGOOD Waveforms

The OV and UV threshold of the buck and LDO output voltage monitor are updated automatically by the digital control block when the output voltage setting changes. When the output voltage is increased, the OV threshold is updated at the same time the VSET of the regulator is changed. The UV threshold is updated after a delay calculated by the delta voltage change and the slew rate of the regulator output. When the output voltage is decreased, the UV threshold is updated at the same time the VSET of the regulator is changed. The OV threshold is updated after a delay calculated by the delta voltage change and the slew rate of the regulator output. The OV and UV threshold of the buck and LDO output voltage monitors are calculated based on the target output voltage set by the corresponding BUCKn_VSET1, BUCKn_VSET2 , or LDOn_VSET registers, and the deviation from the target output voltage set by the corresponding BUCKn_UV_THR, BUCKn_OV_THR, LDOn_UV_THR, and the LDOn_OV_THR registers.

It is important to note that when a regulator is enabled, a voltage monitor self test is perform to ensure proper operation. The monitoring function is disabled/gated during this time. Figure 5-17 shows the timing diagram of the buck regulator UV/OV self test. Figure 5-18 shows the timing diagram of the LDO UV/OV self test. The monitoring function will become effective after the gating period.

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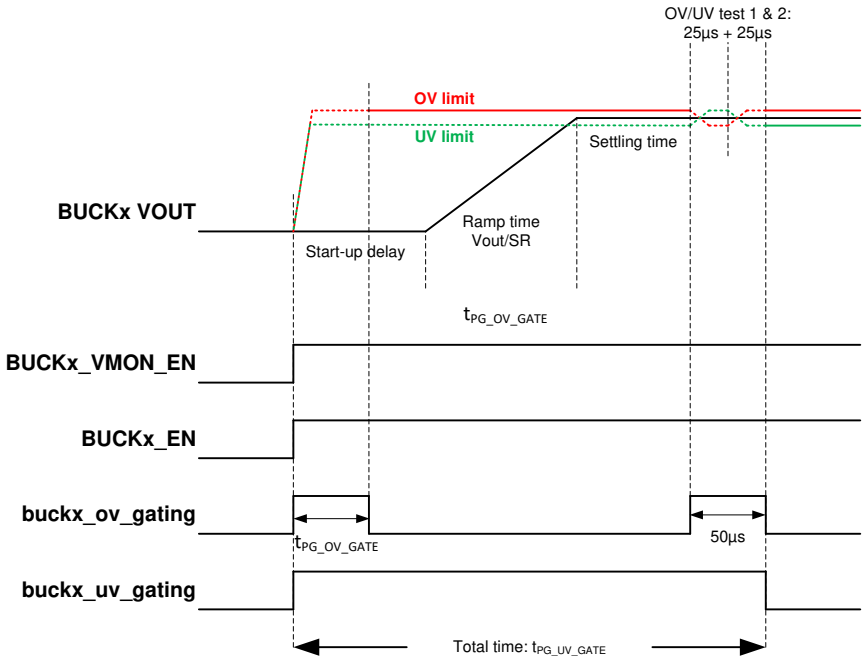

Figure 5-17. Timing of Buck Regulator UV/OV Self Test

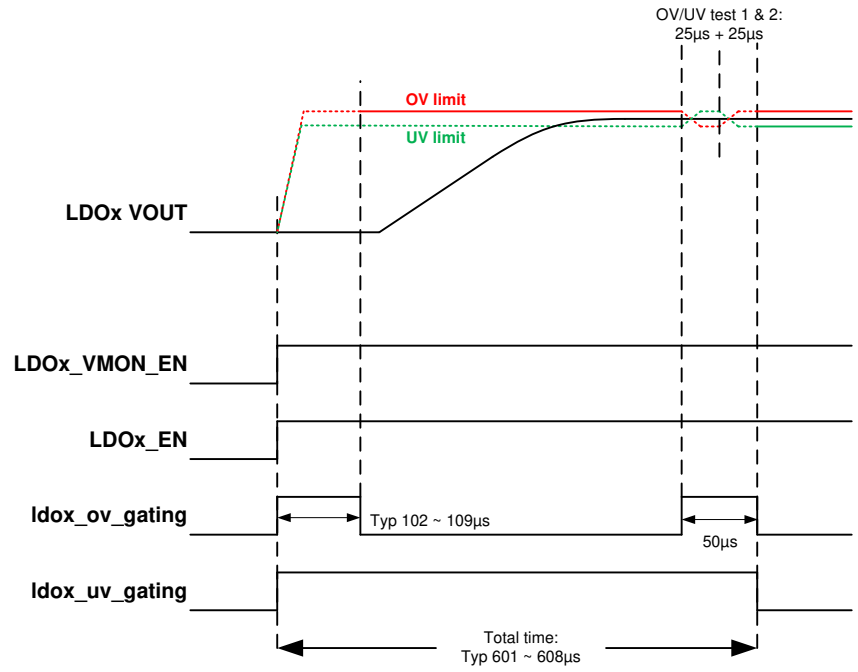

Figure 5-18. Timing of LDO Regulator UV/OV Self Test

5.3.5 Thermal Monitoring

The TPS6594-Q1 device includes several thermal monitoring functions for internal thermal protection of the PMIC.

The TPS6594-Q1 device integrates thermal detection modules to monitor the temperature of the die. These modules are placed on opposite sides of the device and close to the LDO and BUCK modules. An over-temperature condition at either module first generates a warning to the system and then, if the temperature continues to rise, a switch-off of the PMIC device can occur before damage to the die.

Two thermal protection levels are available. One of these protections is a thermal warning function described in Section 5.3.5.1, which sends an interrupt to software. Software is expected to close any noncritical running tasks to reduce power. The second protection is a thermal shutdown (TS) function described in Section 5.3.5.2, which immediately begins device switch-off.

Thermal monitoring is automatically enabled when any one of the external regulator output is enabled under the mission states. It is disabled in all power states, including the LP_STANDBY state, when only the internal regulators are regulator is enabled, to minimize the device power consumption. Indication of a thermal warning event is written to the TWARN_INT register.

The current consumption of the thermal monitoring can be decreased in mission states when the low power dissipation is important. If TSD_LP_EN bit is set and the temperature is below thermal warning level in all thermal detection modules, only one thermal detection module is monitored. If the temperature rises in that module, monitoring of all modules is started.

If the die temperature of the PMIC device rises further, an orderly or an immediate shutdown occurs. Indication of a thermal shutdown event is written to the TSD_ORD_INT register bit for orderly shutdown, or the TSD_IMM_INT register bit for the immediate shutdown. The system cannot restart until the temperature falls below the thermal warning threshold.

5.3.5.1 Thermal Warning Function

The thermal monitor provides a warning to the host processor through the interrupt system when the temperature reaches a critical value. The threshold value must be set to less than the thermal shutdown threshold. Hysterisis is added to the thermal warning detection to avoid generating multiple interrupts.

The integrated thermal warning function provides the host PM software with an early warning over-temperature condition. This monitoring system is connected to the interrupt controller and can send an interrupt when the temperature is higher than the preset threshold. The TPS6594-Q1 device uses the TWARN_LEVEL register bit to set the thermal warning junction temperature at 120°C or 130°C. The hysterisis of the thermal warning level is 10°C in typical conditions.

When the power-management software triggers an interrupt, immediate action must be taken to reduce the amount of power drawn from the PMIC device (for example, noncritical applications must be closed).

5.3.5.2 Thermal Shutdown

The thermal shutdown detector monitors the temperature on the die. If the junction reaches a temperature at which damage can occur, a switch-off transition is initiated and a thermal shutdown event is written into a status register. There are two levels of thermal shutdown threshold. When the die temperature reaches the $T_{SD\_orderly}$ level, an orderly shutdown of the TPS6594-Q1 device will take place. If the die temperature raises rapidly and reaches the T_{SD_imm} level before the orderly shutdown process completes, an immediate shutdown of the device will take place to turn off all of the power resources as rapidly as possible. After the thermal shutdown takes place, the system cannot restart until the die temperature falls below the thermal warning threshold.

5.3.6 Backup Supply Power-Path

LDOVRTC are supplied from either the VBACKUP (backup supply from either coin-cell or super-cap) input or VCCA. The power-path is designed to prioritize VCCA to maximize the life of the backup supply. Whenever the PMIC is powered-up from NO SUPPLY state, the power-path is forced to select the VCCA input.

When VCCA drops below the VCCA_UVLO threshold, the device shuts down all rails except LDOVRTC and enters BACKUP mode. At this point the Backup Supply Power-Path (BSPP) selects the supply for the LDOVRTC based on on the level of VCCA. If VCCA falls below the VCCA_UVLO threshold, the power-path switches to the VBACKUP as the input of LDOVRTC. When the voltage of VCCA returns to level above the VCCA_UVLO threshold level, the power-path switches the input of LDOVRTC back to VCCA.

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When both the VCCA voltage drop below the VCCA_UVLO threshold, and the VBACKUP voltage drops below the RTC_LDO_UVLO threshold, LDOVRTC is turned OFF and the digital core is reset, forcing the device into NO SUPPLY state.

5.3.7 General-Purpose I/Os (GPIO Pins)

The TPS6594-Q1 device integrates eleven configurable general-purpose I/Os that are multiplexed with alternative features as listed in Section 3.1.

For GPIOs characteristics, refer to Electrical characteristics tabled for Digital Input Signal Parameters and Digital Output Signal Parameters.

When configured as primary functions, all GPIOs are controlled through the following set of registers bits under the individual GPIOn_CONF register.

- GPIOn_DEGLITCH_EN: Enables the 8 µs deglitch time for each GPIO pin (input)
- GPIOn_PU_PD_EN: Enables the internal pull up or pull down resistor connected to each GPIO pin
- GPIOn_PU_SEL: Selects the pull up or the pull down resistor to be connected when GPIOn_PU_PD_EN = '1'. '1' = pull-up resistor selected, '0' = pull-down resistor selected
- GPIOn_OD: Configures the GPIO pin (output) as: '1' = open drain, '0' = push-pull
- GPIOn_DIR: Configures the input or output direction of each GPIO pin

Each GPIO event can generate an interrupt on a rising edge, falling edge, or both, configured through the GPIOn_FALL_MASK and the GPIOn_RISE_MASK register bits. A GPIO-interrupt applies when the primary function (general-purpose I/O) has been selected and also for the following alternative functions:

- nRSTOUT
- nRSTOUT_SOC
- PGOOD
- nERR_MCU
- nERR_SoC
- TRIG_WDOG
- DISABLE_WDOG
- NSLEEP1, NSLEEP2
- WKUP1, WKUP2
- LP_WKUP2, LP_WKUP2

The GPIOn_SEL[2:0] register bits under the GPIOn_CONF registers control the selection between a primary and an alternative functions. When a pre-defined function is selected, some predetermined IO characteristics (such as pullup, pulldown, push-pull or open drain) for the pin will be enforced regardless the settings of the associated GPIO configuration register. Please note that if the GPIOn_SEL[2:0] is changed during device operation, a signal glitch may occur which may cause digital malfunction, especially if it involves a clock signal such as SCL_I2C2, CLK32KOUT, SCL_SPMI, SYNCCLKIN, or SYNCCLKOUT. Please refer to Section 3.2 for more detail on the predetermined IO characteristics for each pre-defined digital interface function.

All GPIOs can be configured as a wake-up input when it is configured as a WKUP1 or a WKUP2 signal. Only GPIO3 and GPIO4 can be configured as LP_WKUP1 or LP_WKUP2 signal so that they can be used to wake up the device from LP_STANDBY state. All GPIOs can also be configured as a NSLEEP1 or a NSLEEP2 input. For more information regarding the usage of the NSLEEPx pins and the WKUPx pins, please refer to Section 5.4.1.2.2.2.1 and Section 5.4.1.2.2.2.2.

Any of the GPIO pin can also be configured as part of the power-up sequence to enable external devices such as external BUCKs when it is configured as a general-purpose output port.

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5.3.8 Interrupts

The interrupt registers in the device are organized in hierarchical fashion. The are grouped in to the following categories:

BUCK ERROR These interrupts indicate over-voltage (OV), under-voltage (UV), short-circuit (SC), residual voltage (SC) and over-current (ILIM) error conditions found on the Buck regulators

LDO ERROR These interrupts indicate OV, UV, and SC error conditions found on the LDO regulators, as well as OV and UV error conditions found on the VCCA supply

SEVERE ERROR These errors indicate severe device error conditions, such as thermal shutdown, PFSM sequencing and execution error and pre-regulator over-voltage failure, which caused the device to execute immediate shutdown of all digital outputs, external voltage rails and monitors, and proceed to the Safe Recovery State

MODERATE ERROR These interrupts provide warnings to the system to indicate detection of multiple WDOG Errors or ESM errors exceeding the allowed recovery count, detection of long press nPWRON button, SPMI communication error, register CRC error, BIST failure, or thermal reaching orderly shutdown level. These warning causes the device to execute orderly shutdown of all digital outputs, external voltage rails and monitors, and proceed to the Safe Recovery State

MISCELLANEOUS WARNING These interrupts provides information to the system to indicate detection of WDOG or ESM errors, die temperature crossing thermal warning threshold, external sync clock available, or device passing BIST test

STARTUP SOURCE These interrupts provides information to the system the mechanism which caused the device to start up, which includes FSD, RTC alarm or timer interrupts, the activation of the ENABLE pin or the nPRWON pin button detection

GPIO DETECTION These interrupts indicates the High/Rising-Edge or the Low/Falling-Edge detection at the GPIO1 through GPIO11 pins.

FSM ERROR INTERRUPT There interrupts indicate the detection of an error which causes the device mission state changes.

All interrupts are logically combined on a single output pin, nINT (active low). The host processor can read the INT_TOP register to find the interrupt registers to find out the source of the interrupt, and write '1' to the corresponding interrupt register bit to clear the interrupt. This mechanism ensures when a new interrupt occurs while the nINT pin is still active, all of the corresponding interrupt register bit will retain the interrupt source information until it is cleared by the host.

Any interrupt source can be masked by setting the corresponding mask register to '1'. When an interrupt is masked, the interrupt bit is not updated when the associated event occurs, the nINT line will not be affected, and the event is not recorded. If an interrupt is masked after the event occurred, the interrupt register bit will reflect the event until the bit is cleared. While the event is masked, the interrupt register bit will not be over-written when a new event occurs.

Figure 5-19 shows the hierarchical structure of the interrupt registers according to the categories described above. The purpose of this register structure is to reduce the number of interrupt register read cycles the host has to perform in order to identify the source of the interrupt. Table 5-7 summarizes the trigger and the clearing mechanism for all of the interrupt signals. More detail descriptions of each interrupt registers can be found in 节 5.7.

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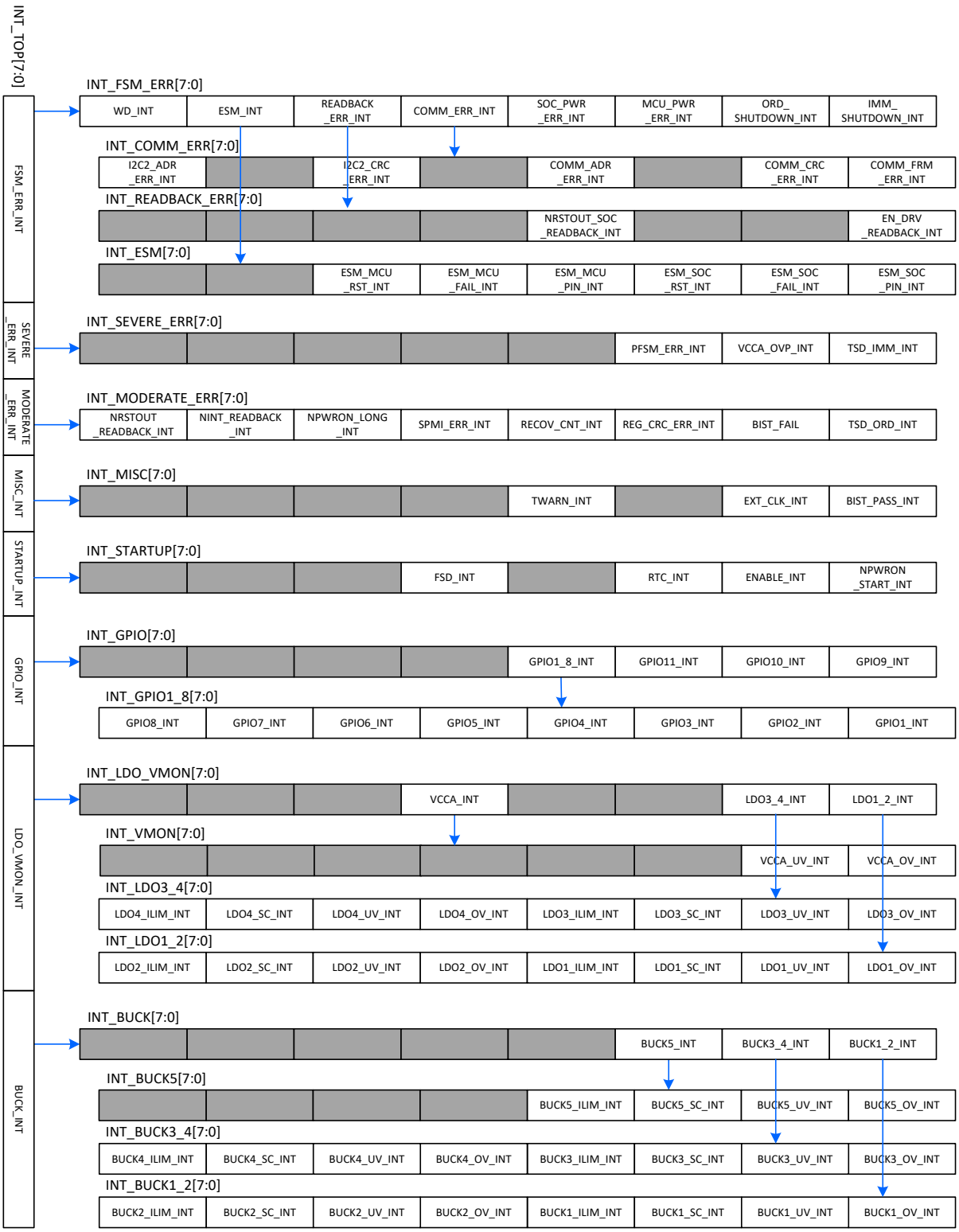

Figure 5-19. Hierarchical Structure of Interrupt Registers

Table 5-7. Summary of Interrupt Signals

EVENT	TRIGGER FOR FSM	RESULT	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Buck regulator forward current limit triggered	**EN_ILIM_FSM_CTRL=1:** According to BUCKn_GRP_SEL and x_RAIL_TRIG bits **EN_ILIM_FSM_CTRL=0:** N/A	**EN_ILIM_FSM_CTRL=1:** Transition according to FSM trigger and interrupt **EN_ILIM_FSM_CTRL=0:** Interrupt only	Depends on FSM configuration, see FSM transition diagram	BUCKn_ILIM_INT = 1	BUCKn_ILIM_MASK	BUCKn_ILIM_STAT	Write 1 to BUCKn_ILIM_INT bit Interrupt is not cleared if current limit violation is active
LDO regulator current limit triggered	**EN_ILIM_FSM_CTRL=1:** According to LDOn_GRP_SEL and x_RAIL_TRIG bits **EN_ILIM_FSM_CTRL=0:** N/A	**EN_ILIM_FSM_CTRL=1:** Transition according to FSM trigger and interrupt **EN_ILIM_FSM_CTRL=0:** Interrupt only	Depends on FSM configuration, see FSM transition diagram	LDOn_ILIM_INT = 1	LDOn_ILIM_MASK	LDOn_ILIM_STAT	Write 1 to LDOn_ILIM_INT bit Interrupt is not cleared if current limit violation is active
Buck output or switch short circuit detected	According to BUCKn_GRP_SEL and x_RAIL_TRIG bits	Regulator disable and transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	BUCKn_SC_INT = 1	N/A	N/A	Write 1 to BUCKn_SC_INT bit
LDO output short circuit detected	According to LDOn_GRP_SEL and x_RAIL_TRIG bits	Regulator disable and transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	LDOn_SC_INT = 1	N/A	N/A	Write 1 to LDOn_SC_INT bit
Buck output residual voltage violation	**BUCKn_RV_SEL = 1** According to BUCKn_GRP_SEL and x_RAIL_TRIG bits **BUCKn_RV_SEL = 0** N/A	**BUCKn_RV_SEL = 1** Regulator disable and transition according to FSM trigger and interrupt **BUCKn_RV_SEL = 0** N/A	Depends on FSM configuration, see FSM transition diagram	BUCKn_SC_INT = 1	N/A	N/A	Write 1 to BUCKn_SC_INT bit
LDO output residual voltage violation	**LDOn_RV_SEL = 1** According to LDOn_GRP_SEL and x_RAIL_TRIG bits **LDOn_RV_SEL = 0** N/A	**LDOn_RV_SEL = 1** Regulator disable and transition according to FSM trigger and interrupt **LDOn_RV_SEL = 0** N/A	Depends on FSM configuration, see FSM transition diagram	LDOn_SC_INT = 1	N/A	N/A	Write 1 to LDOn_SC_INT bit
Buck regulator overvoltage	According to BUCKn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	BUCKn_OV_INT = 1	BUCKn_OV_MASK	BUCKn_OV_STAT	Write 1 to BUCKn_OV_INT bit Interrupt is not cleared if it is active
Buck regulator undervoltage	According to BUCKn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	BUCKn_UV_INT = 1	BUCKn_UV_MASK	BUCKn_UV_STAT	Write 1 to BUCKn_UV_INT bit Interrupt is not cleared if it is active
LDO regulator overvoltage	According to LDOn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	LDOn_OV_INT = 1	LDOn_OV_MASK	LDOn_OV_STAT	Write 1 to LDOn_OV_INT bit Interrupt is not cleared if it is active
LDO regulator undervoltage	According to LDOn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	LDOn_UV_INT = 1	LDOn_UV_MASK	LDOn_UV_STAT	Write 1 to LDOn_UV_INT bit Interrupt is not cleared if it is active
VCCA input overvoltage monitoring	According to VCCA_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	VCCA_OV_INT = 1	VCCA_OV_MASK	VCCA_OV_STAT	Write 1 to VCCA_OV_INT bit Interrupt is not cleared if it is active
VCCA input undervoltage monitoring	According to VCCA_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	VCCA_UV_INT = 1	VCCA_UV_MASK	VCCA_UV_STAT	Write 1 to VCCA_UV_INT bit Interrupt is not cleared if it is active
VMONx input overvoltage monitoring	According to VMONx_GRP_SEL and X_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	VMONx_OV_INT = 1	VMONx_OV_MASK	VMONx_OV_STAT	Write 1 to VMONx_OV_INT bit Interrupt is not cleared if it is active
VMONx input undervoltage monitoring	According to VMONx_GRP_SEL and X_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	VMONx_UV_INT = 1	VMONx_UV_MASK	VMONx_UV_STAT	Write 1 to VMONx_UV_INT bit Interrupt is not cleared if it is active

Table 5-7. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Thermal warning	N/A	Interrupt only	Not valid	TWARN_INT = 1	TWARN_MASK	TWARN_STAT	Write 1 to TWARN_INT bit Interrupt is not cleared if temperature is above thermal warning level
Thermal shutdown, orderly sequenced	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence and interrupt	Automatic startup to STARTUP_DEST[1:0] state after temperature is below TWARN level	TSD_ORD_INT = 1	N/A	TSD_ORD_STAT	Write 1 to TSD_ORD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
Thermal shutdown, immediate	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt	Automatic startup to STARTUP_DEST[1:0] state after temperature is below TWARN level	TSD_IMM_INT = 1	N/A	TSD_IMM_STAT	Write 1 to TSD_IMM_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
BIST error	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low immediately and interrupt	Automatic startup to STARTUP_DEST[1:0] state	BIST_FAIL_INT = 1	BIST_FAIL_MASK	N/A	Write 1 to BIST_FAIL_INT bit
Register CRC error	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low immediately and interrupt	Automatic startup to STARTUP_DEST[1:0] state	REG_CRC_ERR_INT = 1	REG_CRC_ERR_MASK	N/A	Write 1 to REG_CRC_ERR_INT bit
SPMI communication error	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low immediately and interrupt	Automatic startup to STARTUP_DEST[1:0] state	SPMI_ERR_INT = 1	SPMI_ERR_MASK	N/A	Write 1 to SPMI_ERR_INT bit
SPI frame error	N/A	Interrupt only	Not valid	COMM_FRM_ERR_INT = 1	COMM_FRM_ERR_MASK	N/A	Write 1 to COMM_FRM_ERR_INT bit
I2C1 or SPI CRC error	N/A	Interrupt only	Not valid	COMM_CRC_ERR_INT = 1	COMM_CRC_ERR_MASK	N/A	Write 1 to COMM_CRC_ERR_INT bit
I2C1 or SPI address error	N/A	Interrupt only	Not valid	COMM_ADR_ERR_INT = 1	COMM_ADR_ERR_MASK	N/A	Write 1 to COMM_ADR_ERR_INT bit
I2C2 CRC error	N/A	Interrupt only	Not valid	I2C2_CRC_ERR_INT = 1	I2C2_CRC_ERR_MASK	N/A	Write 1 to I2C2_CRC_ERR_INT bit
I2C2 address error	N/A	Interrupt only	Not valid	I2C2_ADR_ERR_INT = 1	I2C2_ADR_ERR_MASK	N/A	Write 1 to I2C2_ADR_ERR_INT bit
PFSM error	N/A	Interrupt only	Not valid	PFSM_ERR_INT = 1	PFSM_ERR_MASK	N/A	Write 1 to PFSM_ERR_INT bit
EN_DRV pin readback error (monitoring high and low states)	N/A	Interrupt and ENABLE_DRV = 0	Not valid	EN_DRV_READBACK_INT = 1	EN_DRV_READBACK_MASK	EN_DRV_READBACK_STAT	Write 1 to EN_DRV_READBACK_INT bit Interrupt is not cleared if it is active
NINT pin readback error (monitoring low state)	N/A	Interrupt and ENABLE_DRV = 0	Not valid	NINT_READBACK_INT = 1	NINT_READBACK_MASK	NINT_READBACK_STAT	Write 1 to NINT_READBACK_INT bit Interrupt is not cleared if it is active
NRSTOUT pin readback error (monitoring low state)	N/A	Interrupt and ENABLE_DRV = 0	Not valid	NRSTOUT_READBACK_INT = 1	NRSTOUT_READBACK_MASK	NRSTOUT_READBACK_STAT	Write 1 to NRSTOUT_READBACK_INT bit Interrupt is not cleared if it is active
NRSTOUT_SOC pin readback error (monitoring low state)	N/A	Interrupt only	Not valid	NRSTOUT_SOC_READBACK_INT = 1	NRSTOUT_SOC_READBACK_MASK	NRSTOUT_SOC_READBACK_STAT	Write 1 to NRSTOUT_SOC_READBACK_INT bit Interrupt is not cleared if it is active
Fault detected by SOC ESM (level mode: low level detected, PWM mode: PWM signal timing violation)	N/A	Interrupt only	Not valid	ESM_SOC_PIN_INT = 1	ESM_SOC_PIN_MASK	N/A	Write 1 to ESM_SOC_PIN_INT bit

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Table 5-7. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Fault detected by SOC ESM (level mode: low level longer than DELAY1 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1time)	N/A	Interrupt and ENABLE_DRV = 0 (configurable)	Not valid	ESM_SOC_FAIL_INT = 1	ESM_SOC_FAIL_MASK	N/A	Write 1 to ESM_SOC_FAIL_INT bit
Fault detected by SOC ESM (level mode: low level longer than DELAY1+DELAY2 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1+DELAY2 time)	ESM_SOC_RST	Interrupt, and NRSTOUT_SOC toggle	Automatically returns to the current operating state after the completion of SoC warm reset	ESM_SOC_RST_INT = 1	ESM_SOC_RST_MASK	N/A	Write 1 to ESM_SOC_RST_INT bit
Fault detected by MCU ESM (level mode: low level detected, PWM mode: PWM signal timing violation	N/A	Interrupt only	Not valid	ESM_MCU_PIN_INT = 1	ESM_MCU_PIN_MASK	N/A	Write 1 to ESM_MCU_PIN_INT bit
Fault detected by MCU ESM (level mode: low level longer than DELAY1 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1 time)	N/A	Interrupt and ENABLE_DRV = 0 (configurable)	Not valid	ESM_MCU_FAIL_INT = 1	ESM_MCU_FAIL_MASK	N/A	Write 1 to ESM_MCU_FAIL_INT bit
Fault detected by MCU ESM (level mode: low level longer than DELAY1+DELAY2 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1+DELAY2 time)	ESM_MCU_RST	Interrupt and Warm Reset (ENABLE_DRV = 0 and NRSTOUT and NRSTOUT_SOC toggle)	Automatically returns to the current operating state after the completion of warm reset	ESM_MCU_RST_INT = 1	ESM_MCU_RST_MASK	N/A	Write 1 to ESM_MCU_RST_INT bit
External clock is expected, but it is not available or the frequency is not in the valid range	N/A	Interrupt only	Not valid	EXT_CLK_INT = 1(1)	EXT_CLK_MASK	EXT_CLK_STAT	Write 1 to EXT_CLK_INT bit
BIST completed successfully	N/A	Interrupt only	Not valid	BIST_PASS_INT = 1	BIST_PASS_MASK	N/A	Write 1 to BIST_PASS_INT bit
Watchdog fail counter above fail threshold	N/A	Interrrupt and ENABLE_DRV = 0	Clear interrupt and WD_FAIL_CNT < WD_FAIL_TH	WD_FAIL_INT = 1	N/A	N/A	Write 1 to WD_FAIL_INT bit
Watchdog fail counter above reset threshold	WD_RST (if WD_RST_EN = 1)	Interrupt and Warm Reset if WD_RST_EN = 1 (ENABLE_DRV = 0 and NRSTOUT and NRSTOUT_SOC toggle)	Automatically returns to the current operating state after the completion of warm reset	WD_RST_INT = 1	N/A	N/A	Write 1 to WD_RST_INT bit
Watchdog long window timeout	WD_RST	Interrupt and Warm Reset (ENABLE_DRV = 0 and NRSTOUT and NRSTOUT_SOC toggle)	Automatically returns to the current operating state after the completion of warm reset	WD_LONGWIN_TIMEOUT_INT = 1	N/A	N/A	Write 1 to WD_LONGWIN_TIMEOUT_INT bit
RTC alarm wake-up	TRIGGER_SU_x	Startup to STARTUP_DEST[1:0] state and interrupt	Not valid	ALARM = 1	IT_ALARM = 0	N/A	Write 1 to ALARM bit
RTC timer wake-up	TRIGGER_SU_x	Startup to STARTUP_DEST[1:0] state and interrupt	Not valid	TIMER = 1	IT_TIMER = 0	N/A	Write 1 to TIMER bit
Low state in NPWRON pin	TRIGGER_SU_x	Startup to STARTUP_DEST[1:0] state and interrupt	Not valid	NPWRON_START_INT = 1	NPWRON_START_MASK	NPWRON_IN	Write 1 to NPWRON_START_INT bit
Long low state in NPWRON pin	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence and interrupt	Valid power-on request	NPWRON_LONG_INT = 1	NPWRON_LONG_MASK	NPWRON_IN	Write 1 to NPWRON_LONG_INT bit

(1) Interrupt is generated during clock detector operation and in case clock is not available when clock detector is enabled.

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Table 5-7. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Low state in ENABLE pin	TRIGGER_FORCE_STANDBY/TRIGGER_FORCE_LP_STANDBY	Transition to STANDBY or LP_STANDBY depending on the LP_STANDBY_SEL bit setting	ENABLE pin rise	N/A	N/A	N/A	N/A
ENABLE pin rise	TRIGGER_SU_x	Startup to STARTUP_DEST[1:0] state and interrupt	Not valid	ENABLE_INT = 1	ENABLE_MASK	ENABLE_STAT	Write 1 to ENABLE_INT bit
Fault causing orderly shutdown	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence and interrupt	Automatic startup to STARTUP_DEST[1:0] state	ORD_SHUTDOWN_INT	ORD_SHUTDOWN_MASK	N/A	Write 1 to ORD_SHUTDOWN_INT
Fault causing immediate shutdown	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt	Automatic startup to STARTUP_DEST[1:0] state	IMM_SHUTDOWN_INT	IMM_SHUTDOWN_MASK	N/A	Write 1 to IMM_SHUTDOWN_INT
Power supply error for MCU	MCU_POWER_ERROR	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	MCU_PWR_ERR_INT	MCU_PWR_ERR_MASK	N/A	Write 1 to MCU_PWR_ERR_INT
Power supply error for SOC	SOC_POWER_ERROR	Transition according to FSM trigger and interrupt	Depends on FSM configuration, see FSM transition diagram	SOC_PWR_ERR_INT	SOC_PWR_ERR_MASK	N/A	Write 1 to SOC_PWR_ERR_INT
VCCA over-voltage ($VCCA_{OVP}$)	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt	Automatic startup to STARTUP_DEST[1:0] state after VCCA voltage is below $VCCA_{OVP}$	VCCA_OVP_INT = 1	N/A	VCCA_OVP_STAT	Write 1 to INT_OVP_INT bit Interrupt is not cleared if VCCA voltage is above $VCCA_{OVP}$ level
GPIO interrupt	According to GPIOx_FSM_MASK and GPIOx_FSM_MASK_POL bits	Transition according to FSM trigger and interrupt	Not valid	GPIOx_INT = 1	GPIOx_RISE_MASK GPIOx_FALL_MASK	GPIOx_IN	Write 1 to GPIOx_INT bit
WKUP1 and LP_WKUP1 signals	WKUP1	Transition to ACTIVE state and interrupt	Not valid	N/A	GPIOx_RISE_MASK GPIOx_FALL_MASK	GPIOx_IN	Write 1 to GPIOx_INT bit
WKUP2 and LP_WKUP2 signals	WKUP2	Transition to MCU ONLY state and interrupt	Not valid	N/A	GPIOx_RISE_MASK GPIOx_FALL_MASK	GPIOx_IN	Write 1 to GPIOx_INT bit
NSLEEP1 signal, NSLEEP1B bit	According to NSLEEP1 and NSLEEP2	State transition based on NSLEEP1 and NSLEEP2	Not valid	N/A	NSLEEP1_MASK	GPIOx_IN	N/A
NSLEEP2 signal, NSLEEP2B bit	According to NSLEEP1 and NSLEEP2	State transition based on NSLEEP1 and NSLEEP2	Not valid	N/A	NSLEEP2_MASK	GPIOx_IN	N/A
LDOVINT over- or undervoltage	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately	Valid LDOVINT voltage	N/A	N/A	N/A	N/A
Main clock outside valid frequency	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately	VCCA power cycle	N/A	N/A	N/A	N/A
Recovery counter limit exceeded	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence	VCCA power cycle	N/A	N/A	N/A	N/A
VCCA supply falling below $VCCA_{UVLO}$	IMMEDIATE_SHUTDOWN	Immediate shutdown	VCCA voltage rising	N/A	N/A	N/A	N/A
First supply detection, VCCA supply rising above $VCCA_{UVLO}$	TRIGGER_SU_x	Startup to STARTUP_DEST[1:0] state and interrupt	Not valid	FSD_INT = 1	FSD_MASK	N/A	Write 1 to FSD_INT bit

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5.3.9 RTC

5.3.9.1 General Description

The RTC is driven by the 32-kHz oscillator and it provides the alarm and time-keeping functions.

The main functions of the RTC block are:

- Time information (seconds, minutes, hours) in binary-coded decimal (BCD) code
- Calendar information (day, month, year, day of the week) in BCD code up to year 2099
- Configurable interrupts generation; the RTC can generate two types interrupts which can be enabled and masked individually:
  - Timer interrupts periodically (1-second, 1-minute, 1-hour, or 1-day periods)
  - Alarm interrupt at a precise time of the day (alarm function)
- Oscillator frequency calibration and time correction with 1/32768 resolution

图 5-20 shows the RTC block diagram.

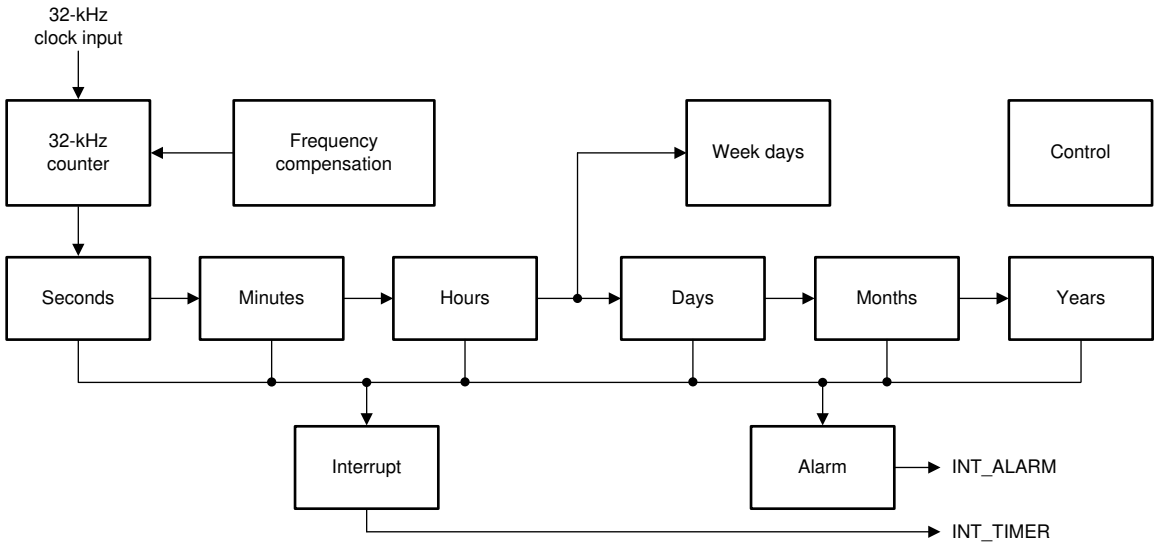

图 5-20. RTC Block Diagram

5.3.9.2 Time Calendar Registers

All the time and calendar information is available in the time calendar (TC) dedicated registers: SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, WEEKS_REG, MONTHS_REG, and YEARS_REG. The TC register values are written in BCD code.

- Year data ranges from 00 to 99.
  - Leap Year = Year divisible by four (2000, 2004, 2008, 2012, and so on)
  - Common Year = Other years
- Month data ranges from 01 to 12.
- Day value ranges:
  - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
  - 1 to 30 when months are 4, 6, 9, 11
  - 1 to 29 when month is 2 and year is a leap year
  - 1 to 28 when month is 2 and year is a common year
- Weekday value ranges from 0 to 6.
- Hour value ranges from 0 to 23 in 24-hour mode and ranges from 1 to 12 in AM or PM mode.
- Minutes value ranges from 0 to 59.

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- Seconds value ranges from 0 to 59.

Example: Time is 10H54M36S PM (PM_AM mode set), 2008 September 5; previous registers values are listed in 表 5-8:

表 5-8. RTC Time Calendar Registers Example

REGISTER	CONTENT
RTC_SECONDS	0x36
RTC_MINTURES	0x54
RTC_HOURS	0x10
RTC_DAYS	0x05
RTC_MONTHS	0x09
RTC_YEARS	0x08
RTC_WEEKS	0x06

The user can round to the closest minute, by setting the ROUND_30S register bit in the RTC_CTRL_REG register. TC values are set to the closest minute value at the next second. The ROUND_30S bit is automatically cleared when the rounding time is performed.

Example:

- If current time is 10H59M45S, round operation changes time to 11H00M00S
- If current time is 10H59M29S, round operation changes time to 10H59M00S

5.3.9.2.1 TC Registers Read Access

TC registers read accesses can be done in two ways:

- A direct read to the TC registers. In this case, there can be a discrepancy between the final time read and the real time because the RTC keeps running because some of the registers can toggle in between register accesses. Software must manage the register change during the reading.
- Read access to shadowed TC registers. These registers are at the same addresses as the normal TC registers. They are selected by setting the GET_TIME bit in the RTC_CTRL_REG register. When this bit is set, the content of all TC registers is transferred into shadow registers so they represent a coherent timestamp, avoiding any possible discrepancy between them. When processing the read accesses to the TC registers, the value of the shadowed TC registers is returned so it is completely transparent in terms of register access.

[For test mode only] The content of the TC registers will be available for read access only 50 µs after the 20MHz oscillator clock is started.

5.3.9.2.2 TC Registers Write Access

TC registers write accesses can be done while RTC is stopped. Software can stop the RTC by the clearing the STOP_RTC bit of the control register and checking the RUN bit of the status to be sure that RTC is frozen. It then updates the TC values and restarts the RTC by setting the STOP_RTC bit, which ensures that the final written values are aligned with the targeted values.

5.3.9.3 RTC Alarm

RTC alarm registers (ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, and ALARM_YEARS_REG) are used to set the alarm time or date to the corresponding generated ALARM interrupts. These register values are written in BCD code, with the same data range as described for the TC registers (see 节 5.3.9.2).

5.3.9.4 RTC Interrupts

The RTC supports two types of interrupts:

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- ALARM interrupt. This interrupt is generated when the configured date or time in the corresponding ALARM registers is reached. This interrupt is enabled and disabled by setting the IT_ALARM bit.
- TIMER interrupt. This interrupt is generated when the periodic time (day, hour, minute, second) set in the EVERY bits of the RTC_INTERRUPTS register is reached. This interrupt is enabled and disabled by setting the IT_TIMER bit. The first of the periodic interrupt will occur when the RTC counter reaches the next day, hour, minute, or second counter value. For example, if a timer interrupt is set for every hour at 2:59 AM, the first interrupt will occur at 3:00 AM instead of 3:59 AM.

Both types of the RTC interrupts can be used to wake up the device from the STANDBY state or the LP_STANDBY state when they are not masked.

5.3.9.5 RTC 32-kHz Oscillator Drift Compensation

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers are used to compensate for any inaccuracy of the 32-kHz clock output from the 32-kHz crystal oscillator. To compensate for any inaccuracy, software must perform an external calibration of the oscillator frequency, calculate the drift compensation needed versus one time hour period, and load the compensation registers with the drift compensation value.

The compensation mechanism is enabled by the AUTO_COMP_EN bit in the RTC_CTRL_REG register. The process happens after the first second of each hour. The time between second 1 to second 2 (T_ADJ) is adjusted based on the settings of the two RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers. These two registers form a 16-bit, 2 s complement value COMP_REG (from –32767 to 32767) that is subtracted from the 32-kHz counter as per the following formula to adjust the length of T_ADJ: $\left(\frac{32768 - \text{COMP\_REG}}{32768}\right)$. It is therefore possible to adjust the compensation with a 1/32768-second time unit accuracy per hour and up to 1 second per hour.

Software must ensure that these registers are updated before each compensation process (there is no hardware protection). For example, software can load the compensation value into these registers after each hour event, during second 0 to second 1, just before the compensation period, happening from second 1 to second 2.

It is also possible to preload the internal 32-kHz counter with the content of the RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers when setting the SET_32_COUNTER bit in the RTC_CTRL_REG register. This must be done when the RTC is stopped.

图 5-21 shows the RTC compensation scheduling.

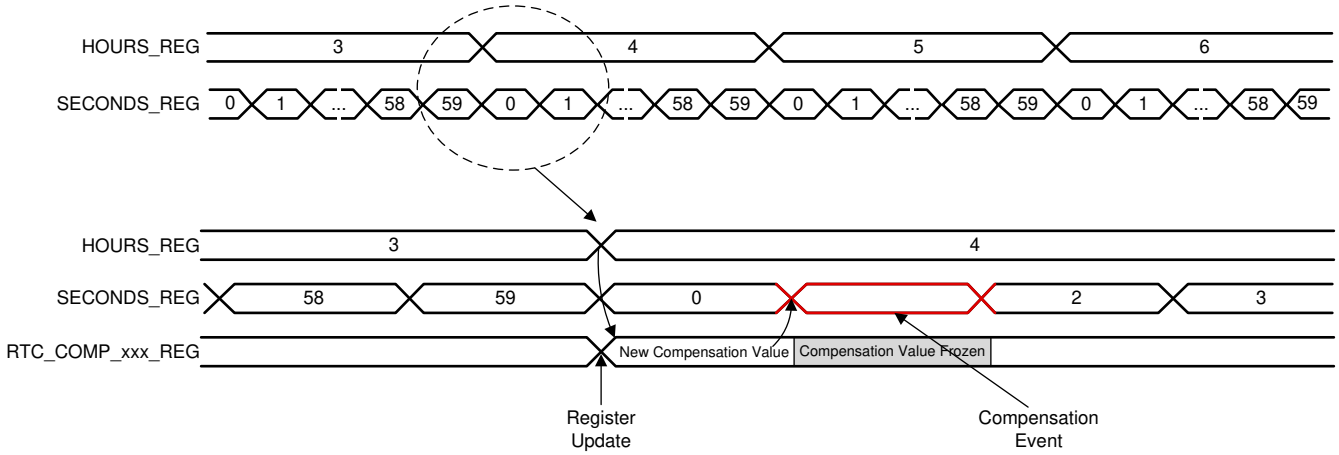

图 5-21. RTC Compensation Scheduling

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5.3.10 Watchdog (WD)

The watchdog monitors the correct operation of the MCU. This watchdog requires specific messages from the MCU in specific time intervals to detect correct operation of the MCU. The MCU can control the logic-level of the EN_DRV pin when the watchdog detects correct operation of the MCU. When the watchdog detects incorrect operation of the MCU, the TPS6594-Q1 device pulls the EN_DRV pin low. This EN_DRV pin can be used in the application as a control-signal to deactivate the power output stages, for example a motor driver, in case of incorrect operation of the MCU.

The watchdog has two different modes which are defined as follows:

Trigger mode In trigger mode, the MCU applies a pulse signal with a minimum pulse width of t_{WD_pulse} on the pre-assigned GPIO input pin to send the required watchdog trigger. To select this mode, the MCU must clear bit WD_MODE_SELECT. More details are available in Section 5.3.10.6

Q&A (question and answer) mode In Q&A mode, the MCU sends watchdog answers through the I2C bus or SPI bus. To select this mode, the MCU must set bit WD_MODE_SELECT. More details are available in Section 5.3.10.7.1

The watchdog will operate in Q&A per default after device powers-up from the NO SUPPLY state.

5.3.10.1 Watchdog Fail Counter and Status

The watchdog includes a watchdog fail counter WD_FAIL_CNT[3:0] that increments because of *bad events* or decrements because of *good events*. Furthermore, the watchdog includes two programmable thresholds:

1. Fail-threshold (programmable through bits WD_FAIL_TH[2:0])
2. Reset-threshold (programmable through bits WD_RST_TH[2:0])

When the WD_FAIL_CNT[3:0] counter value is less than or equal to the configured Watchdog-Fail threshold (WD_FAIL_TH[2:0]) and bit WD_FIRST_OK=1, the MCU can set the ENABLE_DRV bit when no other error-flags are set.

When the WD_FAIL_CNT[3:0] counter value is greater than the configured Watchdog-Fail threshold (WD_FAIL_CNT[3:0] > WD_FAIL_TH[2:0]), the device clears the ENABLE_DRV bit, sets the error-flag WD_FAIL_INT, and pulls the nINT pin low.

When the WD_FAIL_CNT[3:0] counter value is greater than the configured Watchdog-Fail plus Watchdog-Reset threshold (WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0])) and the watchdog-reset function is enabled (configuration bit WD_RST_EN=1), the device goes through a warm reset, sets the error-flag WD_RST_INT, and pulls the nINT pin low.

The device clears the WD_FAIL_CNT[3:0] each time the watchdog enters the Long Window. The status bits WD_FAIL_INT and WD_RST_INT are latched until the MCU writes a '1' to these bits.

Table Table 5-9 gives an overview of the Watchdog Fail Counter value ranges and the corresponding device status.

Table 5-9. Overview of Watchdog Fail Counter value ranges and corresponding device status

Watchdog Fail Counter value WD_FAIL_CNT[3:0]	Device Status
WD_FAIL_CNT[3:0] ≤ WD_FAIL_TH[2:0]	MCU can set the ENABLE_DRV bit if WD_FIRST_OK=1 and no other error-flags are set
WD_FAIL_TH[2:0] < WD_FAIL_CNT[3:0] ≤ (WD_FAIL_TH[2:0] + WD_RST_TH[2:0])	The deviceclears the ENABLE_DRV bit, sets error-flag WD_FAIL_INT and pulls the nINT pin low
WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0])	If configuration bit WD_RST_EN=1, device goes through a warm reset, sets the error-flag WD_RST_INT, and pulls the nINT pin low. See Interrupt handling for WD_RTS in Table 5-7.

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The WD_FAIL_CNT[3:0] counter responds as follows:

- When the Watchdog is in the Long-Window, the WD_FAIL_CNT[3:0] is cleared to 4'b0000
- A good event decrements the WD_FAIL_CNT[3:0] by one before the start of the next Window-1
- A bad event increments the WD_FAIL_CNT[3:0] by one before the start of the next Window-1

For definitions of good event and bad event, please refer to Section 5.3.10.6 and Section 5.3.10.7.1 respectively.

5.3.10.2 Watchdog Start-up and Configuration

When the device releases the nRSTOUT pin, the watchdog starts with the Long Window. This Long Window has a time interval (t_{LONG_WINDOW}) which is has a default value of 12 minutes set in bits WD_LONGWIN[7:0] (default value 0xFF).

As long as the watchdog is in the Long Window, the MCU can either clear bit WD_EN to disable to watchdog, or configure the watchdog through the following register bits:

- WD_LONGWIN[7:0] to configure the duration of the Long-Window time-interval
- WD_MODE_SELECT to select the Watchdog mode (Trigger mode or Q&A Mode)
- WD_PWRHOLD to activate the Watchdog Disable function (more detail in Section 5.3.10.4)
- WD_RETURN_LONGWIN to return to Long-Window after completion of the current watchdog sequence (more detail in Section 5.3.10.4)
- WD_WIN1[6:0] to configure the duration of the Window-1 time-interval
- WD_WIN2[6:0] to configure the duration of the Window-2 time-interval
- WD_RST_EN to enable/disable the watchdog-reset function
- WD_EN to enable/disable the watchdog
- WD_FAIL_TH[2:0] to configure the Watchdog-Fail threshold
- WD_RST_TH[2:0] to configure the Watchdog-Reset threshold
- WD_QA_FDBK[1:0] to configure the settings for the reference answer-generation
- WD_QA_LFSR[1:0] to configure the settings for the question-generation
- WD_QUESTION_SEED[3:0] to configure the starting-point for the 1st question-generation
- WD_QA_CFG for watchdog in Q&A Mode

The device will keep the above register bit values configured by the MCU as long as the device is powered.

The MCU can configure the time interval of the Long Window (t_{LONG_WINDOW}) with the WD_LONGWIN[7:0] bits. When WD_LONGWIN[7:0] = 0x00, $t_{LONG\_WINDOW\_MIN}$ = 95 ms, and $t_{LONG\_WINDOW\_MAX}$ = 105 ms.

Use Equation 4 and Equation 5 to calculate the minimum and maximum values for the Long Window (t_{LONG_WINDOW}) time interval when WD_LONGWIN[7:0] > 0x00:

$$t_{LONG\_WINDOW\_MIN} = WD\_LONGWIN[7:0] \times 3 \text{ seconds} \times 0.95 \quad (4)$$

$$t_{LONG\_WINDOW\_MAX} = WD\_LONGWIN[7:0] \times 3 \text{ seconds} \times 1.05 \quad (5)$$

When the MCU clears bit WD_EN, the watchdog goes out of the Long Window and disables the watchdog. When the watchdog is disabled in this way, the MCU can control the ENABLE_DRV bit when no other error-flags are set. The MCU can set bit WD_EN back to '1' to enable the watchdog again. When the MCU sets bit WD_EN back to '1', the watchdog starts with the Long Window.

The watchdog locks the following configuration register bits when it goes out of the Long Window and start the first watchdog sequence:

- WD_WIN1[6:0]
- WD_WIN2[6:0]
- WD_LONGWIN[7:0]
- WD_MODE_SELECT

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- WD_QA_FDBK[1:0], WD_QA_LFSR[1:0] and WD_QUESTION_SEED[3:0]
- WD_RST_EN, WD_EN, WD_FAIL_TH[2:0] and WD_RST_TH[2:0]

5.3.10.3 MCU to Watchdog Synchronization

In order to go out of the Long Window and start the first watchdog sequence, the MCU must do the following:

- Clear bits WD_PWRHOLD to de-activate the Watchdog Disable function (more detail in Section 5.3.10.4)
- Apply a pulse signal with a minimum pulse-width t_{WD_pulse} on the pre-assigned GPIO pin in the case the watchdog is configured for Trigger mode, or
- Write four times to WD_ANSWER[7:0] in the case the watchdog is configured for Q&A mode

When the MCU fails to get the watchdog out of the Long Window before the configured Long Window ti me interval (t_{LONG_WINDOW}) elapses, the device goes through a warm reset, and sets the WD_LONGWIN_TIMEOUT_INT. This bit latched until the MCU writes a '0' to it'1' to clear it.

5.3.10.4 Watchdog Disable function

The watchdog in the TPS6594-Q1 device has a Watchdog Disable function to prevent an unwanted MCU reset in case the MCU is un-programmed or needs to be reprogrammed. In order to activate this Watchdog Disable function for an un-programmed MCU, DISABLE_WDOG pin must be asserted to a logic-high level for a time-interval longer than t_{WD_DIS} prior to the moment the device releases the nRSTOUT pin. If the Watchdog Disable function is activated in this way, the device sets bit WD_PWRHOLD to keep the watchdog in the Long Window. The watchdog stays in the Long Window until the MCU clears the WD_PWRHOLD bit.

In case the MCU needs to be reprogrammed while the watchdog monitors the correct operation of the MCU, the MCU can set bit WD_RETURN_LONGWIN to put the watchdog back in the Long Window. When the MCU set this bit, the watchdog returns to the Long Window after the current Watchdog Sequence completes. In order to make the watchdog stay in the Long Window as long as needed the MCU can either re-configure the Long Window (t_{LONG_WINDOW}) time interval, or set the WD_PWRHOLD bit. Once the MCU starts the first watchdog sequence (as described in Section 5.3.10.3), the MCU must clear bit WD_RETURN_LONGWIN before the end of the first Watchdog Sequence.

5.3.10.5 Watchdog Sequence

Once the watchdog is out of the Long Window, each watchdog sequence starts with a Window-1 followed by a Window-2. The watchdog ends the current sequence and starts a next sequence when one of the events below occurs:

- The configured Window-2 time period elapses
- The watchdog detects a pulse signal with a minimum pulse-width t_{WD_pulse} on the pre-assigned GPIO pin in case the watchdog is used in Trigger mode
- The watchdog detects four times a write access to WD_ANSWER[7:0] in case the watchdog is used in Q&A mode

The MCU can configure the time periods of the Window-1 ($t_{WINDOW1}$) and Window-2 ($t_{WINDOW2}$) with the bits WD_WIN1[6:0] and WD_WIN2[6:0] respectively.

Use Equation 6 and Equation 7 to calculate the minimum and maximum values for the $t_{WINDOW1}$ time interval.

$$t_{WINDOW1\_MIN} = (WD\_WIN1[6:0] + 1) \times 0.55 \times 0.95 \text{ ms} \quad (6)$$

$$t_{WINDOW1\_MAX} = (WD\_WIN1[6:0] + 1) \times 0.55 \times 1.05 \text{ ms} \quad (7)$$

Use Equation 8 and Equation 9 to calculate the minimum and maximum values for the $t_{WINDOW-2}$ time interval.

$$t_{WINDOW2\_MIN} = (WD\_WIN2[6:0] + 1) \times 0.55 \times 0.95 \text{ ms} \quad (8)$$

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$t_{WINDOW2\_MAX}$ = (WD_WIN2[6:0] + 1) × 0.55 × 1.05 ms (9)

5.3.10.6 Watchdog Trigger Mode (Default Mode)

When the TPS6594-Q1 device is configured to use the Watchdog Trigger Mode, the watchdog receives the watchdog-triggers from the MCU on the pre-assigned GPIO pin. A rising edge on this GPIO pin, followed by a stable logic-high level on that pin for more than the maximum pulse time, $t_{WD\_pulse(max)}$, is a watchdog-trigger. The watchdog uses a deglitch filter with a t_{WD_pulse} filter time and an internal system clock to create the internally-generated trigger pulse from the watchdog-trigger on the pre-assigned GPIO pin.

The watchdog detects a *good event* when the watchdog-trigger comes in Window-2. The rising edge of the watchdog-trigger on the pre-assigned GPIO pin must occur for at least the t_{WD_pulse} time before the end of Window-2 to generate such a good event.

The watchdog detects a *bad event* when one of the following events occurs:

- The watchdog-trigger comes in Window-1. The rising edge of the watchdog-trigger on the pre-assigned GPIO pin must occur for at least the t_{WD_pulse} time before the end of Window-1 to generate such a bad event. In case of this bad event, the device sets bits WD_TRIG_EARLY and WD_BAD_EVENT
- No watchdog-trigger comes in Window-2. In case of this bad event (also referred to as time-out event), the device sets bits WD_TIMEOUT and WD_BAD_EVENT.

Please consider that the minimum WD-pulse duration needs to meet the maximum deglitch time $t_{WD\_pulse(max)}$

The status bit WD_BAD_EVENT is read-only. The watchdog clears the WD_BAD_EVENT status bit at the end of the watchdog-sequence.

Figure 5-22 shows the flow-chart of the watchdog in Trigger mode

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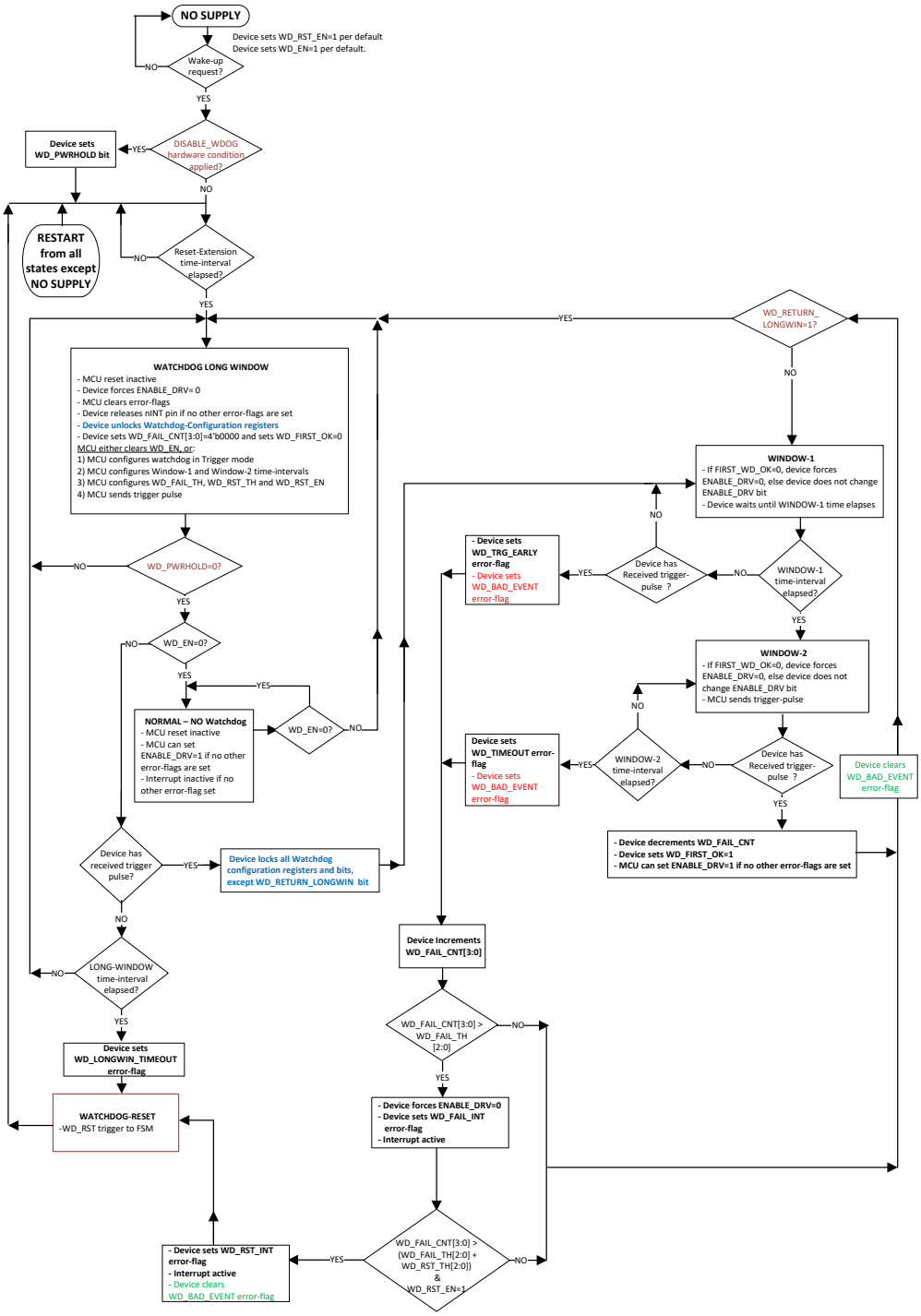

Figure 5-22. Flow Chart for WatchDog Monitor in Trigger Mode

Figure 5-23, Figure 5-24, Figure 5-25,Figure 5-26, and Figure 5-27 give examples of watchdog is trigger mode with good and bad events after device startup.

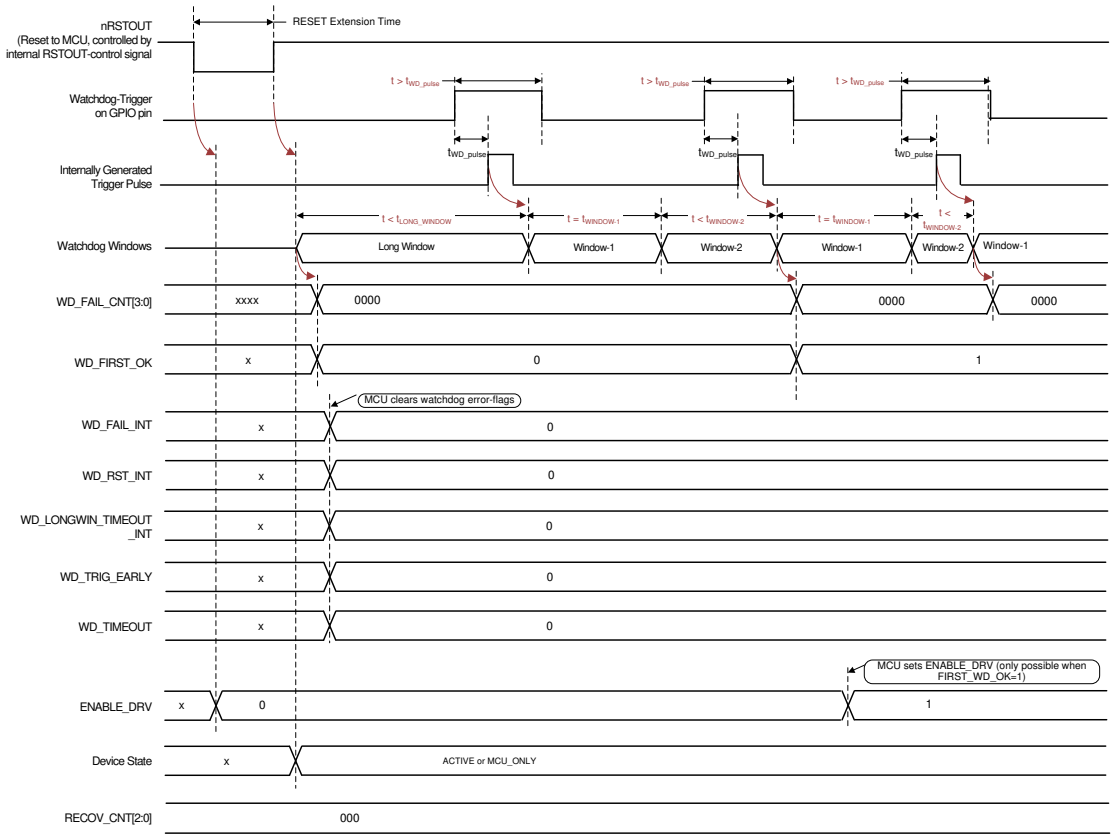

Figure 5-23. Watchdog in Trigger mode - normal MCU startup with correct watchdog-triggers

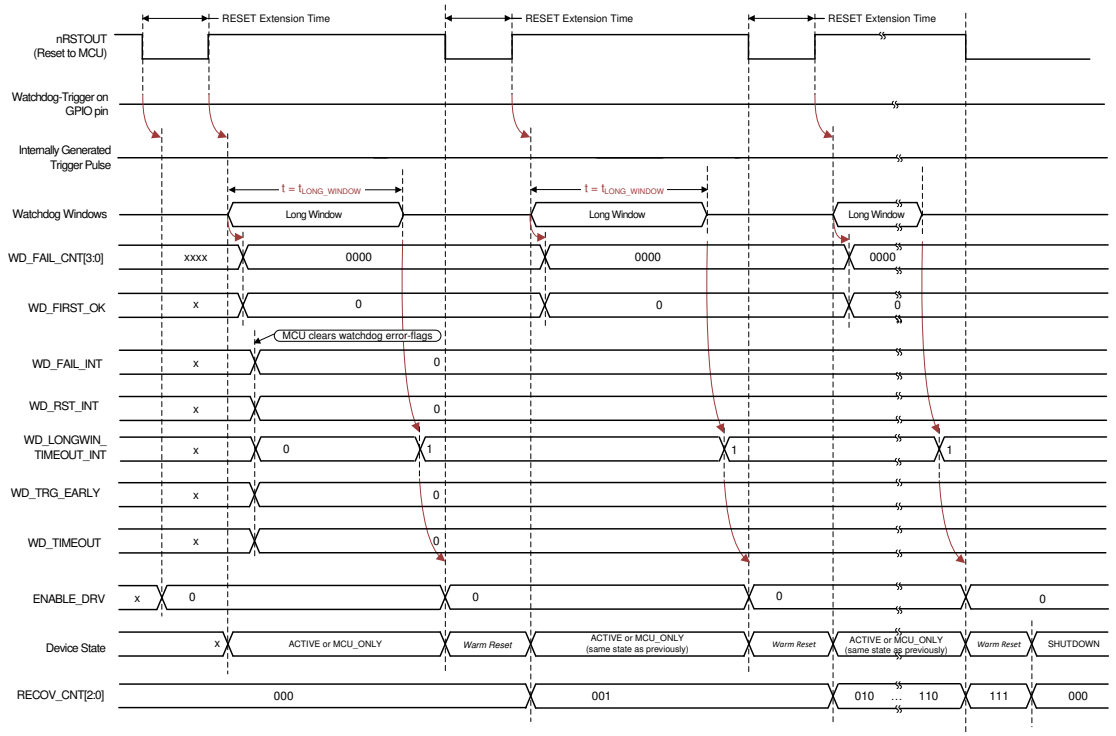

Figure 5-24. Watchdog in Trigger mode - MCU does not send watchdog-triggers after startup

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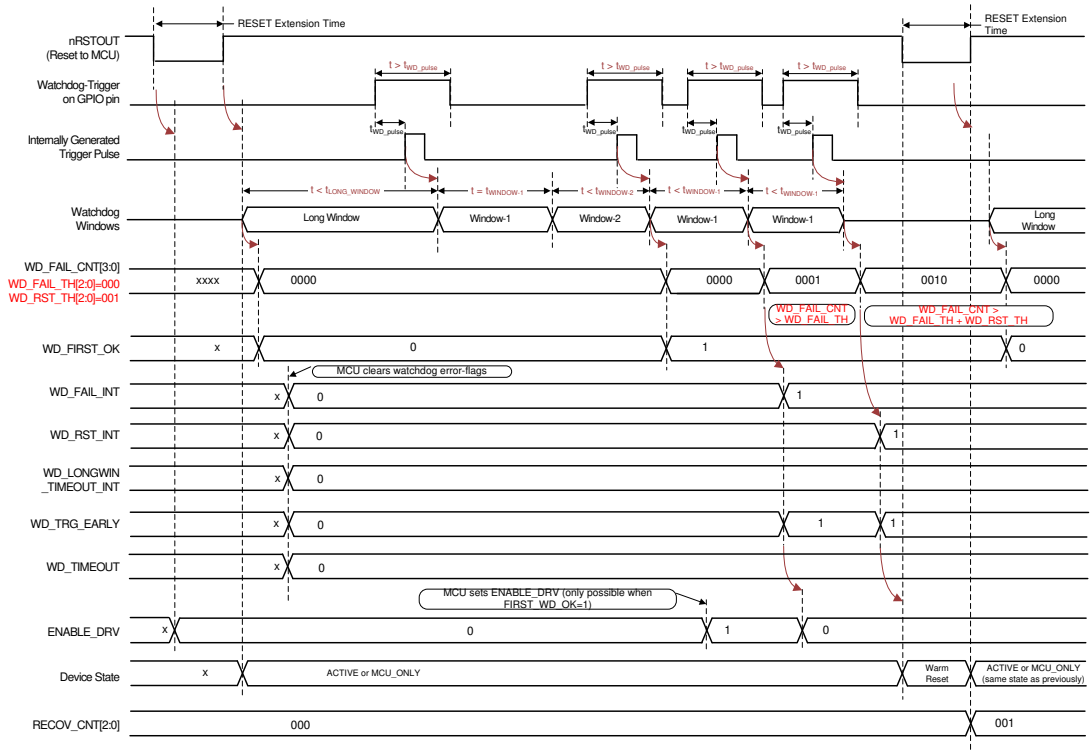

Figure 5-25. Watchdog in Trigger mode – bad event (watchdog-triggers in Window-1) after startup

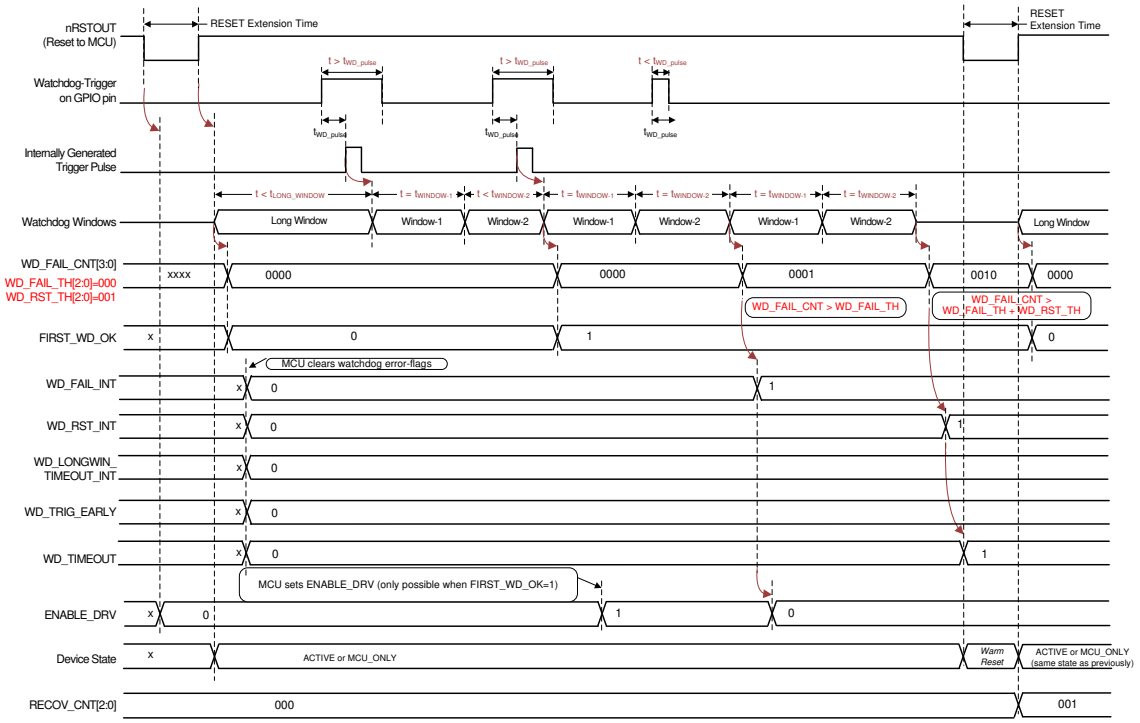

Figure 5-26. Watchdog in Trigger mode - bad events (too short or no trigger in Window-2) after startup

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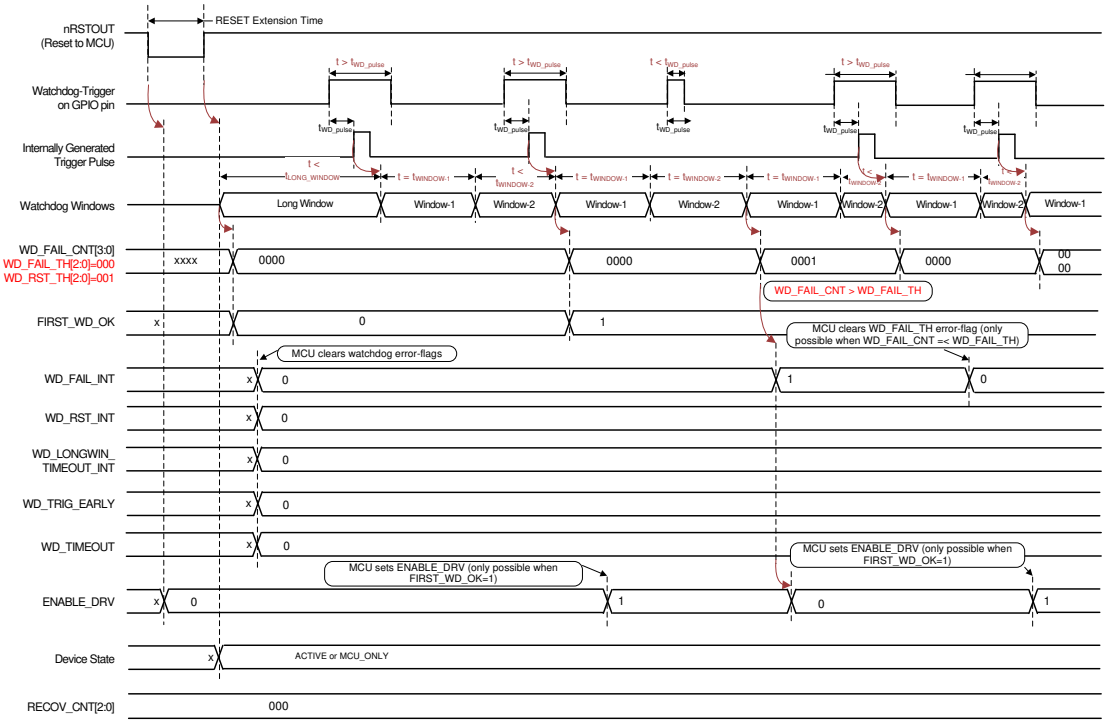

Figure 5-27. Watchdog in Trigger mode – good events (correct watchdog-triggers) after startup, followed by a bad-event (no watchdog-trigger in Window-2) and after that followed by a good event.

5.3.10.7 Watchdog Question-Answer Mode

When the TPS6594-Q1 device is configured to use the Watchdog Question Answer mode, the watchdog requires specific messages from the MCU in specific time intervals to detect correct operation of the MCU.

During operation, the device provides a question for the MCU in WD_QUESTION[3:0]. The MCU performs a fixed series of arithmetic operations on this question to calculate the required 32-bit answer. This answer is split into four answer bytes: Answer-3, Answer-2, Answer-1, and Answer-0. The MCU writes these answer bytes one byte at a time into WD_ANSWER[7:0] from the SPI or the dedicated I^2C2 interface, mapped to GPIO1 and GPIO2 pins.

A good event occurs when the MCU sends the correct answer-bytes calculated for the current question in the correct watchdog window and in the correct sequence.

A bad event occurs when one of the events that follows occur:

- The MCU sends the correct answer-bytes, but not in the correct watchdog window.
- The MCU sends incorrect answer-bytes.
- The MCU returns correct answer-bytes, but in the incorrect sequence.

If the MCU stops providing answer-bytes for the duration of the watchdog time-period, the watchdog detects a time-out event. This time-out event sets the WD_TIMEOUT status bit, increments the WD_FAIL_CNT[3:0] counter, and starts a new watchdog sequence.

5.3.10.7.1 Watchdog Q&A Related Definitions

A question and answer are defined as follows:

Question A question is a 4-bit word (see Section 5.3.10.7.2).

The watchdog provides the question to the MCU when the MCU reads the WD_QUESTION[3:0] bits.

The MCU can request each new question at the start of the watchdog sequence, but this is not required to calculate the answer. The MCU can also have a software implementation

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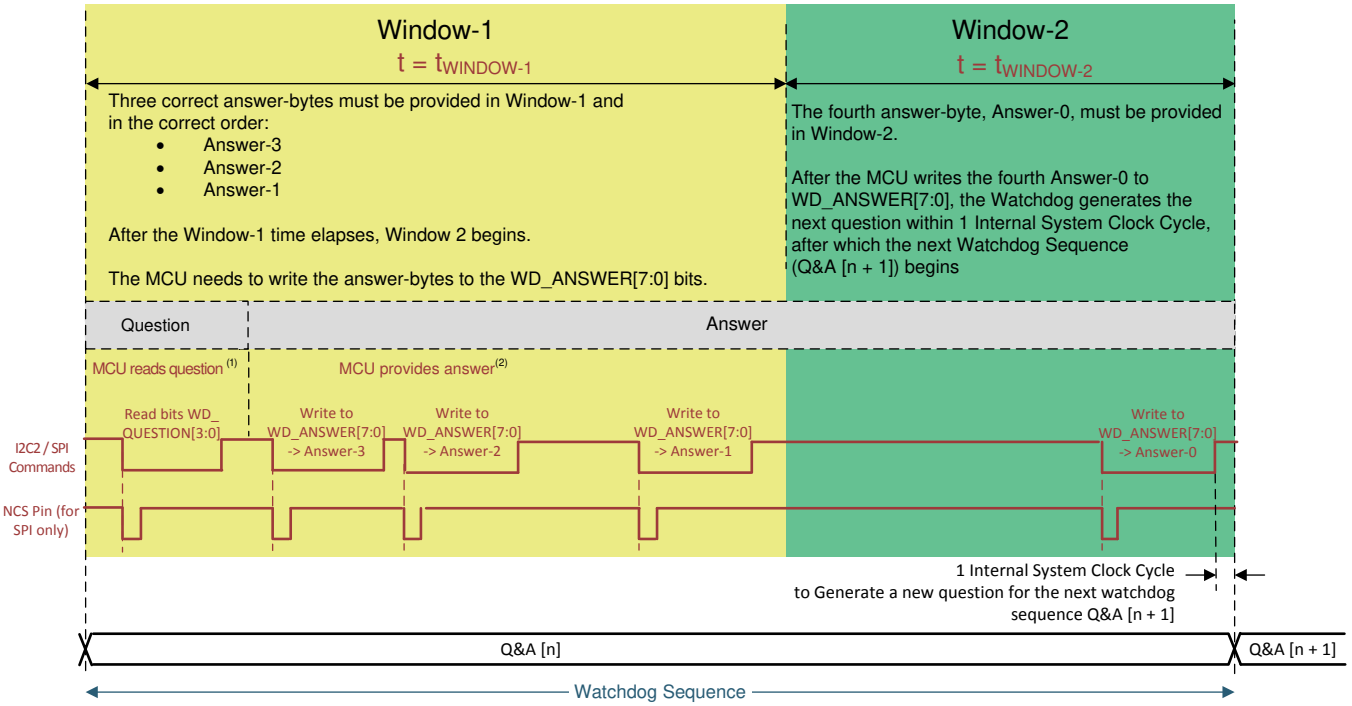
which generates the question according the circuit as shown in Figure 5-30. Nevertheless, the answer and therefore the answer-bytes are always based on the question generated inside the watchdog of the device. So if the MCU generates an incorrect question and gives answer-bytes calculated from this incorrect question, the watchdog detects a bad event

Answer An answer is a 32-bit word that is split into four answer bytes: Answer-3, Answer-2, Answer-1, and Answer-0.

The watchdog receives an answer-byte when the MCU writes to the WD_ANSWER[7:0] bits. For each question, the watchdog requires four correct answer-bytes from the MCU in the correct timing and order (Answer-3, Answer-2, and Answer-1 in Window 1 in the correct sequence, and Answer-0 in Window 2) to detect a good event.

The watchdog sequence in Q&A mode ends after the MCU writes the fourth answer byte (Answer-0), or after a time-out event when the Window-2 time-interval elapses..



(1)) The MCU is not required to read the question. The MCU can give correct answer-bytes Answer-3, Answer-2, Answer-1 as soon as Window-1 starts. The next watchdog sequence always starts in 1 system clock cycle after the watchdog receives the final Answer-0

(2) The MCU can put other I^2C or SPI commands in-between the write-commands to WD_ANSWER[7:0] (even re-requesting the question). This has no influence on the detection of a good event, as long as the three correct answer-bytes in Window-1 are in the correct sequence, and the fourth correct answer-byte is provided before the configured Window-2 time-interval elapses.

Figure 5-28. Watchdog Sequence in Q&A Mode

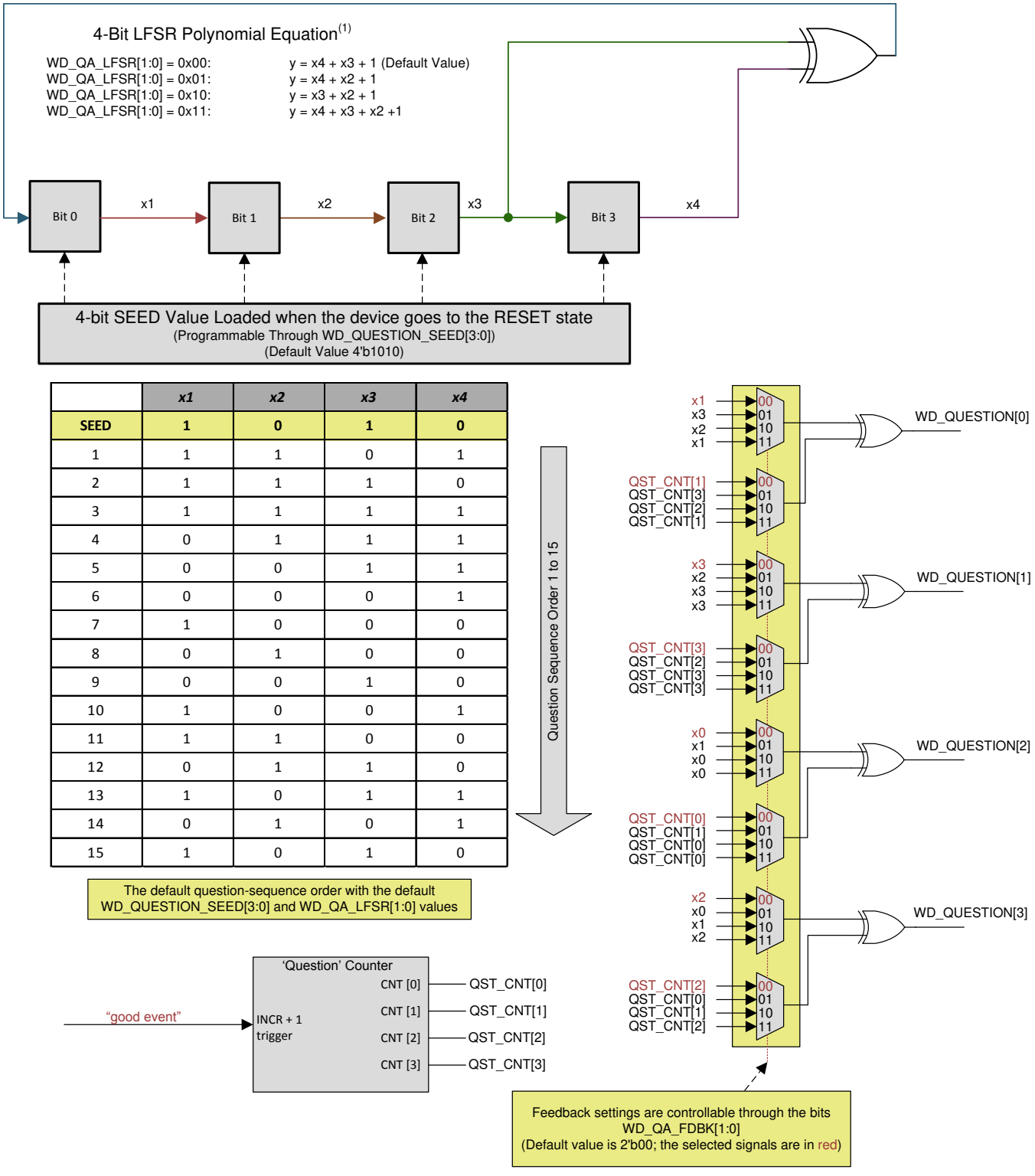
5.3.10.7.2 Question Generation

The watchdog uses a 4-bit *question counter* (QST_CNT[3:0] bits in Figure 5-29), and a 4-bit Markov chain to generate a 4-bit question. The MCU can read this question in the WD_QUESTION[3:0] bits. The watchdog generates a new question when the question counter increments, which only occurs when the watchdog detects a good event. The watchdog does not generate a new question when it detects a bad event or a time-out event.

The question-counter provides a clock pulse to the Markov chain when it transitions from 4'b1111 to 4'b0000. The question counter and the Markov chain are set to the default value of 4'b0000 when the watchdog goes out of the Long Window.

Figure 5-29 shows the logic combination for the WD_QUESTION[3:0] generation.

The logic combination of the question-counter with the WD_ANSW_CNT[1:0] status bits generates the reference answer-bytes as shown in Figure 5-30.



	x1	x2	x3	x4
SEED	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

(1) If current, the y value is 0000, the next y value will be 0001, and any further question generation begins from this value.

Figure 5-29. Watchdog Question Generation

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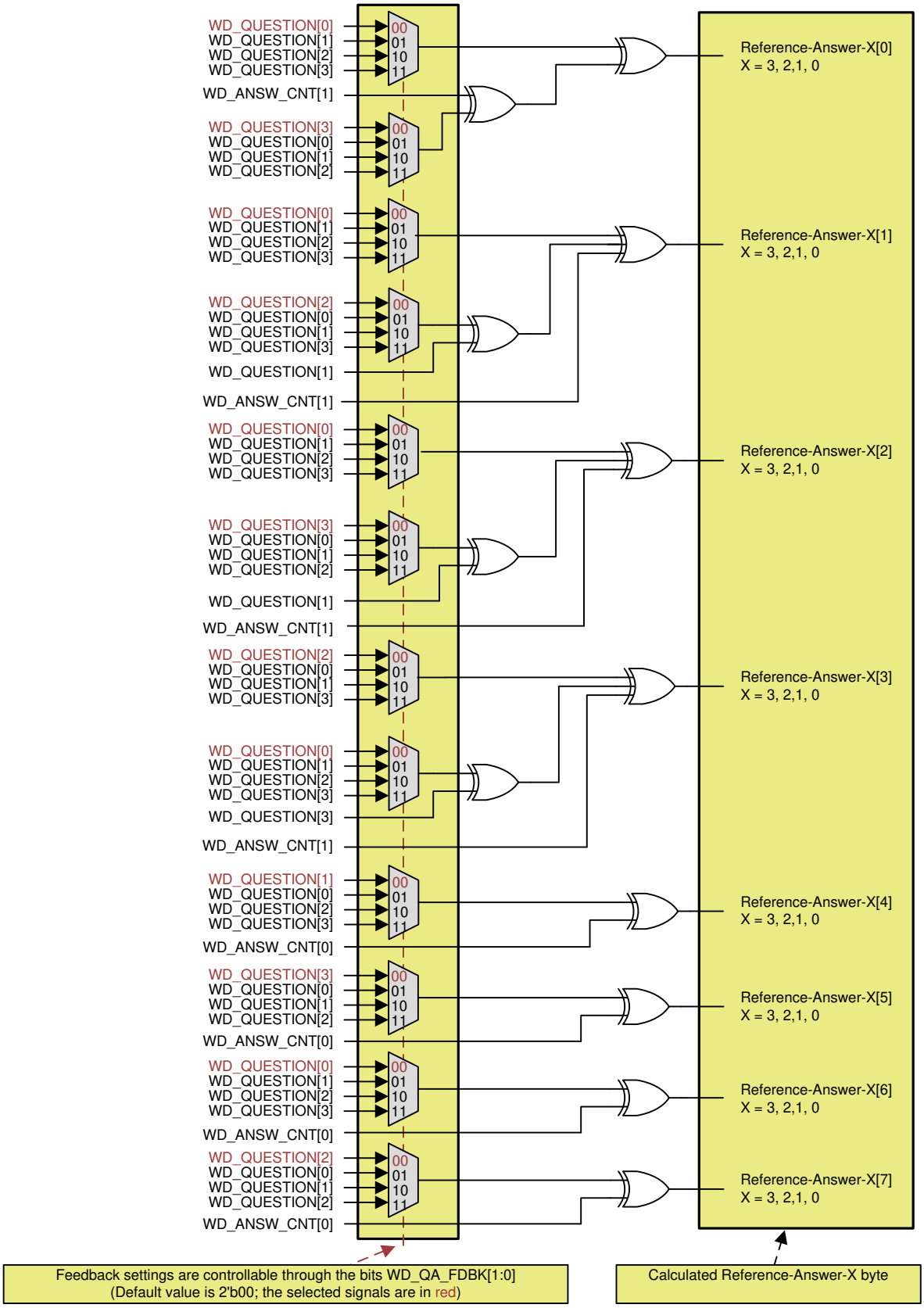

Figure 5-30. Watchdog Reference Answer Calculation

Table 5-10. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER				COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT	
0 answers	0 answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	No answers
0 answers	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Total WD_ANSW_CNT[1:0] = 4
0 answers	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Total WD_ANSW_CNT[1:0] = 4
0 answers	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer						
2 CORRECT answer	1 CORRECT answer						
0 answers	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer						
2 CORRECT answers	1 INCORRECT answer						
0 answers	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answers						
2 CORRECT answers	2 CORRECT answers						
0 answers	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answers						
2 CORRECT answers	2 INCORRECT answers						
0 answers	3 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	
2 INCORRECT answers	1 CORRECT answer						
0 answers	3 INCORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answer						
2 INCORRECT answer	1 INCORRECT answer						
0 answers	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answers		1b	0b	1b	0b	
2 INCORRECT answers	2 CORRECT answers						
0 answers	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answers						
2 INCORRECT answers	2 INCORRECT answers						
3 CORRECT answers	0 answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	0b	0b	0b	1b	Less than 4 CORRECT ANSW in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answers	0 answers		0b	0b	1b	1b	
1 CORRECT answers	0 answers						
3 CORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	0b	0b	0b	CORRECT SEQUENCE

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Table 5-10. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A (continued)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER				COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT	
3 CORRECT answers	1 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answers	0 answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	1b	Total WD_ANSW_CNT[1:0] < 4
3 INCORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	Total WD_ANSW_CNT[1:0] = 4
4 CORRECT answers	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	0b	0b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
3 CORRECT answers + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	0b	0b	
2 CORRECT answers + 2 INCORRECT answers	Not applicable						
1 CORRECT answer + 3 INCORRECT answers	Not applicable						

5.3.10.7.3 Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in Figure 5-30. At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 2'b11 to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_ANSWER[7:0].

The device sets the WD_ANSW_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a '1' to this bit.

5.3.10.7.3.1 Sequence of the 2-bit Watchdog Answer Counter

The sequence of the 2-bit, watchdog answer-counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 2'b11:
  1. The watchdog calculates the reference Answer-3.
  2. A write access occurs. The MCU writes the Answer-3 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 2b'10 and sets the WD_ANSW_ERR status bit to 1 if the Answer-3 byte was incorrect.
- WD_ANSW_CNT[1:0] = 2b'10:
  1. The watchdog calculates the reference Answer-2.
  2. A write access occurs. The MCU writes the Answer-2 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_ANSWER[7:0]..
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 2b'01 and sets the WD_ANSW_ERR status bit to 1 if the Answer-2 byte was incorrect.

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- WD_ANSW_CNT[1:0] = 2b‘01:
  1. The watchdog calculates the reference Answer-1.
  2. A write access occurs. The MCU writes the Answer-1 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_ANSWER[7:0]..
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 2b‘00 and sets the WD_ANSW_ERR status bit to 1 if the Answer-1 byte was incorrect.
- WD_ANSW_CNT[1:0] = 2b‘00:
  1. The watchdog calculates the reference Answer-0.
  2. A write access occurs. The MCU writes the Answer-0 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_ANSWER[7:0].
  4. The watchdog sets the WD_ANSW_ERR status bit to 1 if the Answer-0 byte was incorrect.
  5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 2‘b11’.

  The MCU needs to clear the bit by writing a '1' to the WD_ANSW_ERR bit.

Table 5-11. Set of Questions and Corresponding Answer-Bytes Using the Default Setting of WD_QA_CFG Register

WD QUESTION	ANSWER-BYTES (EACH BYTE TO BE WRITTEN INTO WD_ANSWER[7:0])			
	ANSWER-3	ANSWER-2	ANSWER-1	ANSWER-0
WD_QUESTION[3:0]	WD_ANSW_CNT [1:0] = 2'b11	WD_ANSW_CNT [1:0] = 2'b10	WD_ANSW_CNT [1:0] = 2'b01	WD_ANSW_CNT [1:0] = 2'b00
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

5.3.10.7.4 Watchdog Sequence Events and Status Updates

The watchdog sequence events are as follows for the different scenarios listed:

- A good event occurs when all answer bytes are correct in value and timing. After such a good event, following events will occur:
  1. The WD_FAIL_CNT[2:0] counter decrements by one at the end of the watchdog-sequence
  2. The question-counter increments by one and the watchdog generates a new question
- A bad event occurs when all answer-bytes are correct in value but not in correct timing. After such a bad event, following events will occur:
  1. The WD_SEQ_ERR and WD_BAD_EVENT status bits are set if Window-1 time-interval elapses before watchdog has received Answer-3, Answer-2 and Answer-1
  2. The WD_ANSW_EARLY and WD_BAD_EVENT status bits are set if watchdog receives all four answers in Window-1
  3. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence
  4. The question-counter does not change, and hence the watchdog does not generate a new question
- A bad event occurs when one or more of the answer-bytes are not correct in value but in correct timing. After such a bad event, following events will occur:
  1. The WD_ANSW_ERR and WD_BAD_EVENT status bits are set as soon as the watchdog detects an incorrect answer-byte
  2. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence
  3. The question-counter does not change, and hence the watchdog does not generate a new question

- A bad event occurs when one or more of the answer-bytes are not correct in value and not in correct timing. After such a bad event, following events will occur:
  1. The WD_ANSW_ERR and WD_BAD_EVENT status bits are set as soon as the watchdog detects an incorrect answer-byte
  2. The WD_SEQ_ERR and WD_BAD_EVENT status bits are set if Window-1 time-interval elapses before watchdog has received Answer-3, Answer-2 and Answer-1
  3. The WD_ANSW_EARLY and WD_BAD_EVENT status bits are set if watchdog receives all four answer-bytes in Window-1
  4. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence
  5. The question-counter does not change, and hence the watchdog does not generate a new question
- A time-out event occurs when the device receives less than 4 answer-bytes before Window-2 time-interval elapses. After a time-out event occurs, following events will occur:
  1. WD_SEQ_ERR and WD_BAD_EVENT status bits are set if Window-1 time-interval elapses before watchdog has received Answer-3, Answer-2 and Answer-1
  2. The WD_TIMEOUT and WD_BAD_EVENT status bits are set at the end of the watchdog-sequence
  3. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence
  4. The question-counter does not change, and hence the watchdog does not generate a new question

The status bit WD_BAD_EVENT is read-only. The watchdog clears the WD_BAD_EVENT status bit at the end of the watchdog-sequence.

The status bits WD_SEQ_ERR, WD_ANSW_EARLY, and WD_TIMEOUT are latched until the MCU writes a ‘1’ to these bits. If one or more of these status bits are set, the watchdog can still detect a good event in the next watchdog-sequence. These status bits are read-only. The watchdog clears the WD_BAD_EVENT status bit at the end of the watchdog-sequence.

Figure 5-31 shows the flow-chart of the watchdog in Q&A mode.

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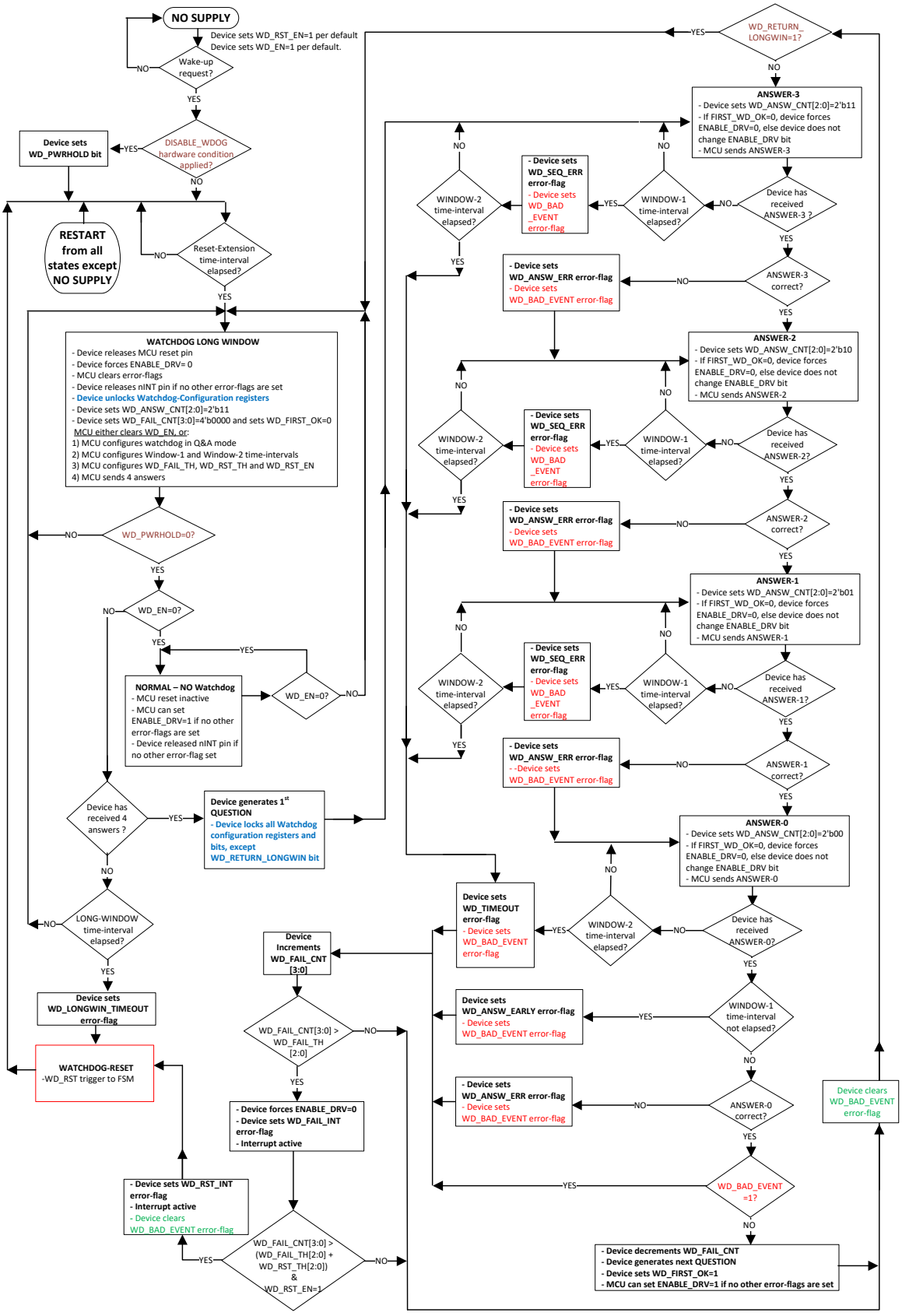

Figure 5-31. Flow Chart for WatchDog in Q&A Mode

5.3.11 Error Signal Monitor (ESM)

The TPS6594-Q1 device has two Error Signal Monitor (ESMs): one ESM_MCU to monitor the MCU error output signal at the nERR_MCU input pin, and one ESM_SoC to monitor the SoC error output signal at the nERR_SoC input pin.

By default, each ESM is enabled at start-up of the TPS6594-Q1 device. To start each ESM, the MCU sets the start bits ESM_MCU_START or ESM_SOC_START for the respective ESM through software after the system is powered up and the initial software configuration is completed. If the MCU clears a start bit, the prospective ESM stops monitoring its input pin. The MCU can set the ENABLE_DRV bit only when the MCU has either started or disabled the ESM. When the prospective ESM is started, the following configuration registers are write protected and can only be read:

Configuration registers write-protected by the ESM_MCU_START register bit:

- ESM_MCU_DELAY1_REG
- ESM_MCU_DELAY2_REG
- ESM_MCU_MODE_CFG
- ESM_MCU_HMAX_REG
- ESM_MCU_HMIN_REG
- ESM_MCU_LMAX_REG
- ESM_MCU_LMIN_REG

Configuration registers write-protected by the ESM_SOC_START register bit:

- ESM_SOC_DELAY1_REG
- ESM_SOC_DELAY2_REG
- ESM_SOC_MODE_CFG
- ESM_SOC_HMAX_REG
- ESM_SOC_HMIN_REG
- ESM_SOC_LMAX_REG
- ESM_SOC_LMIN_REG

ESM uses a deglitch-filter with deglitch-time t_{degl_ESMx} to monitor its related input pin.

The MCU can configure the ESM in two different modes which are defined as follows:

Level Mode the ESM detects an ESM-error when the input pin remains low for a time equal to or longer than the deglitch-time t_{degl_ESMx}.

To select this mode for the ESM_MCU, the MCU must clear bit ESM_MCU_MODE. To select this mode for the ESM_SoC, the MCU must clear bit ESM_SOC_MODE. See Section 5.3.11.2 for further detail

PWM Mode the ESM monitors a PWM signal at its input pin. The ESM detects a bad-event when the frequency or duty cycle of the PWM input signal deviates from the expected signal. The ESM detects a good-event when both frequency and duty cycle of the PWM signal match with the expected signal for one signal period.

The ESM has an error-counter (ESM_MCU_ERR_CNT[4:0] or ESM_SOC_ERR_CNT[4:0]), which increments with +2 after each bad-event, and decrements with -1 after each good-event. The ESM detects an ESM-error when the error-counter value is more than its related threshold value.

To select this mode for the ESM_MCU, the MCU must set bit ESM_MCU_MODE. To select this mode for the ESM_SoC, the MCU must set bit ESM_SOC_MODE. See Section 5.3.11.3 for further details.

The MCU can configure each ESM as long as its related start bit is cleared to 0 (bit ESM_MCU_START or ESM_SOC_START). As soon as the MCU sets a start bit, the device sets a write-protection on the configuration registers of the related ESM except the related start bits ESM_MCU_START and ESM_SOC_START.

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5.3.11.1 ESM Error-Handling Procedure

Each ESM has two of its own configurable delay-timers, which are reset at when the device clears the respective ESM_x_START bit. When an ESM detects an ESM-error, the ESM starts the following procedure:

1. The device sets interrupt bit ESM_MCU_PIN_INT or ESM_SOC_PIN_INT, and pulls the nINT pin low.
2. The ESM starts the delay-1 timer (configurable through related ESM_MCU_DELAY1[7:0] or ESM_SOC_DELAY1[7:0] bits)
3. If the ESM-error is no longer present and MCU has cleared the related interrupt bit ESM_MCU_PIN_INT or ESM_SOC_PIN_INT before the delay-1 timer elapses, the device will release the nINTpin, the ESM will reset the delay-1 and delay-2 timers and continues to monitor its input pin.
4. If the ESM-error is still present and the delay-1 timer elapses, then the ESM clears the ENABLE_DRV bit if bit ESM_MCU_ENDRV=1 or if bit ESM_SOC_ENDRV=1
5. If the delay-2 timer (configurable through related ESM_MCU_DELAY2[7:0] or ESM_SOC_DELAY2[7:0] bits) is set to 0, then the ESM skips steps 6 of this list, and performs step 7.
6. If the delay-2 timer is not set to 0, then:
   a. For ESM_MCU, the device sets interrupt bit ESM_MCU_FAIL_INT and pulls the nINT pin low and starts the delay-2 timer
   b. For ESM_SOC: the device sets interrupt bit ESM_SOC_FAIL_INT, pulls the nINT pin low and starts the delay-2 timer
7. If the ESM-error is no longer present and the MCU has cleared the related interrupt bits listed below before the delay-2 timer elapses, the device will release the nINTpin, the ESM will reset the delay-1 and delay-2 timers and continues to monitor its input pin:
   – ESM_MCU_PIN_INT (and ESM_MCU_FAIL_INT if set in step 6), or
   – ESM_SOC_PIN_INT (and ESM_SOC_FAIL_INT if set in step 6)
8. If the ESM-error is still present and the delay-2 timer elapses, then:
   a. For ESM_MCU, the device:
      i. clears the ESM_MCU_START BIT
      ii. sets interrupt bit ESM_MCU_RST_INT, which the device handles as an ESM_MCU_RST trigger for FSM, described in Table 5-7
      iii. After this trigger handling completes, the device re-initializes the ESM_MCU
   b. For ESM_SoC, the device:
      i. clears the ESM_SOC_START bit
      ii. sets interrupt bit ESM_SOC_RST_INT, which the device handles as an ESM_SOC_RST trigger for FSM, described in Table 5-7
      iii. After this trigger handling completes, the device re-initializes the ESM_SoC

ESM_MCU_DELAY1[7:0] and ESM_SOC_DELAY1[7:0] set the delay-1 time-interval ($t_{DELAY-1}$) for the related ESM_MCU or ESM_SoC. Use Equation 10 and Equation 11 to calculate the worst-case values for the $t_{DELAY-1}$:

Min. $t_{DELAY-1}$ = (ESM_x_DELAY1[7:0] × 2.048 ms) × 0.95 (10)

Max. $t_{DELAY-1}$ = (ESM _x_DELAY1[7:0] × 2.048 ms) × 1.05 (11)

, in which x stands for either MCU or SoC.

ESM_MCU_DELAY2[7:0] or ESM_SOC_DELAY2[7:0] bits set the delay-2 time-interval ($t_{DELAY-2}$) for the related ESM_MCU or ESM_SoC. Use Equation 12 and Equation 13 to calculate the worst-case values for the $t_{DELAY-2}$:

Min. $t_{DELAY-2}$ = (ESM_x_DELAY2[7:0] × 2.048 ms) × 0.95 (12)

Max. $t_{DELAY-2}$ = (ESM _x_DELAY2[7:0] × 2.048 ms) × 1.05 (13)

, in which x stands for either MCU or SoC.

5.3.11.2 Level Mode

In Level Mode, after MCU has set the start bit (bit ESM_MCU_START or bit ESM_SOC_START), the ESM monitors its nERR_MCU or nERR_SoC input pin. Each ESM detects an ESM-error when the voltage level on its input pin remains low for a time equal or longer than the deglitch-time t_{degli_ESMx}. When an ESM detects an ESM-error, it starts the ESM Error-Handling procedure as described in Section 5.3.11.1. If the voltage level on its input pin remains high for a time equal or longer than the deglitch-time t_{degli_ESMx} before the elapse of the configured delay-1 or delay-2 time-intervals, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 5.3.11.1.

For a complete overview on how the ESM works in Level Mode, please refer to the flow-chart in Figure 5-32. Figure 5-33, Figure 5-34, Figure 5-35, and Figure 5-36 show example wave forms for several error-cases for the ESM in Level Mode. In these examples, only the ESM_MCU is shown.

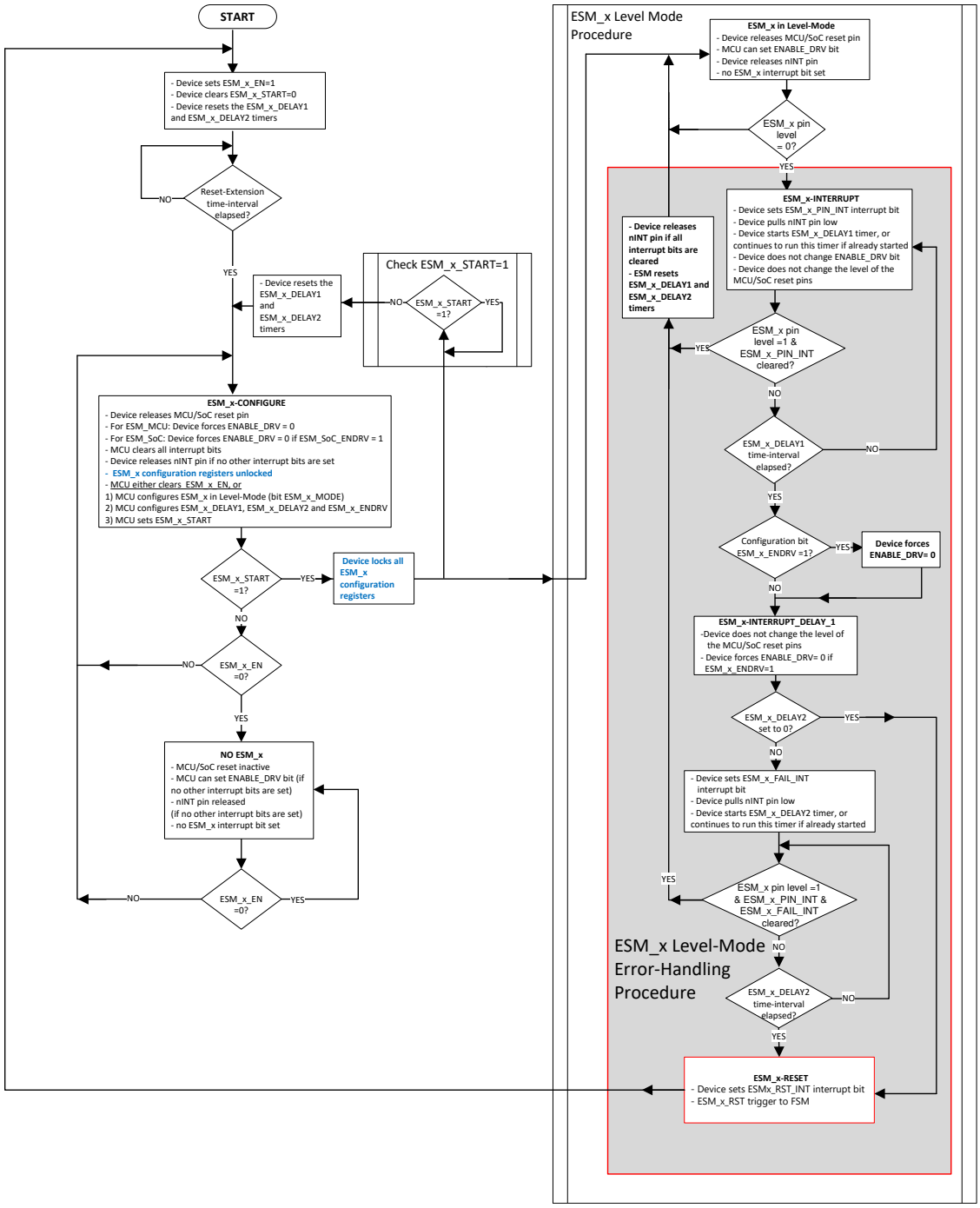

Figure 5-32. Flow Chart for Error Detection in Level Mode

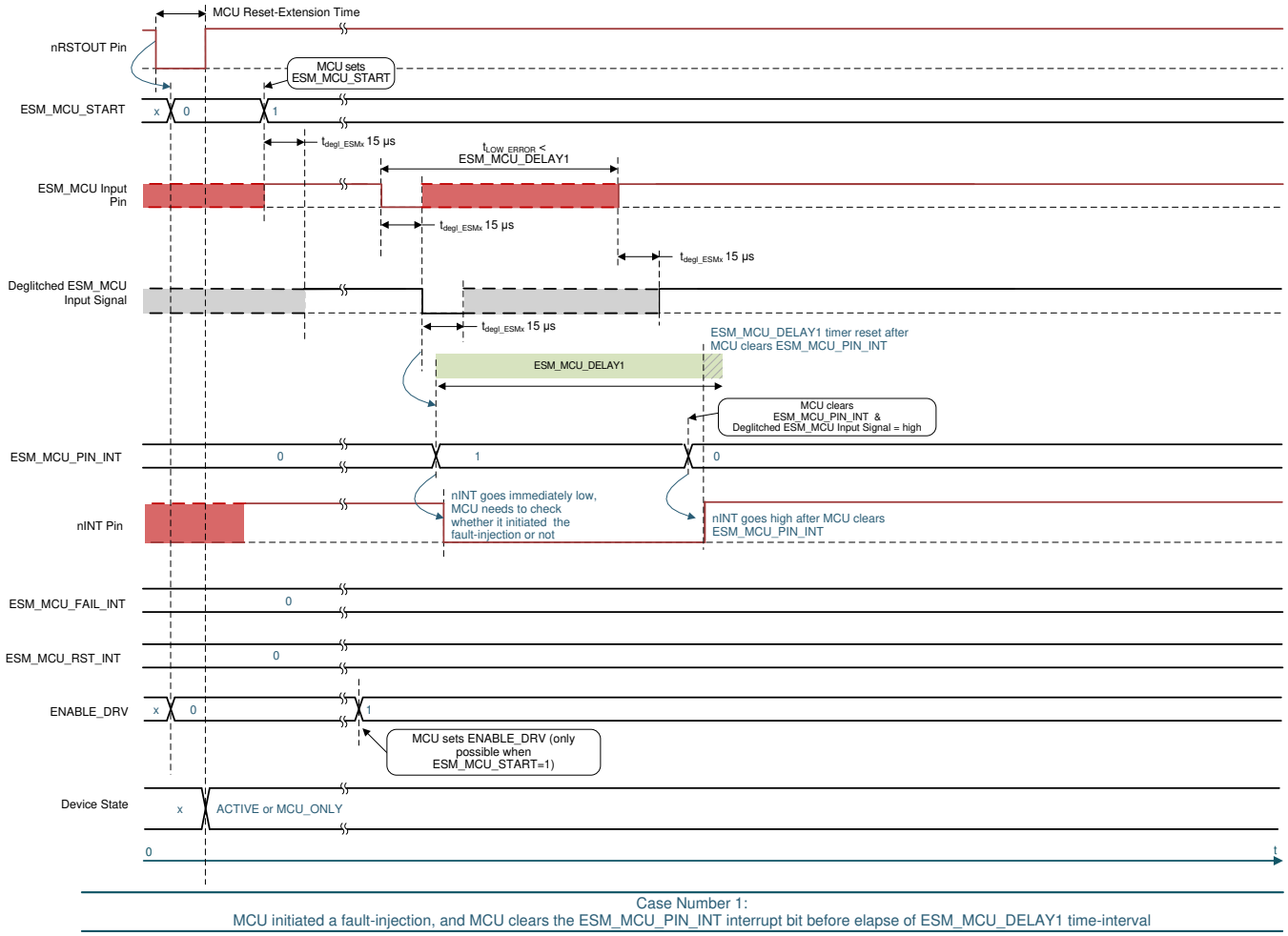

Figure 5-33. Example Waveform for ESMx in Level Mode - Case Number 1: ESM_MCU Signal Recovers Before Elapse of Delay-1 time-interval

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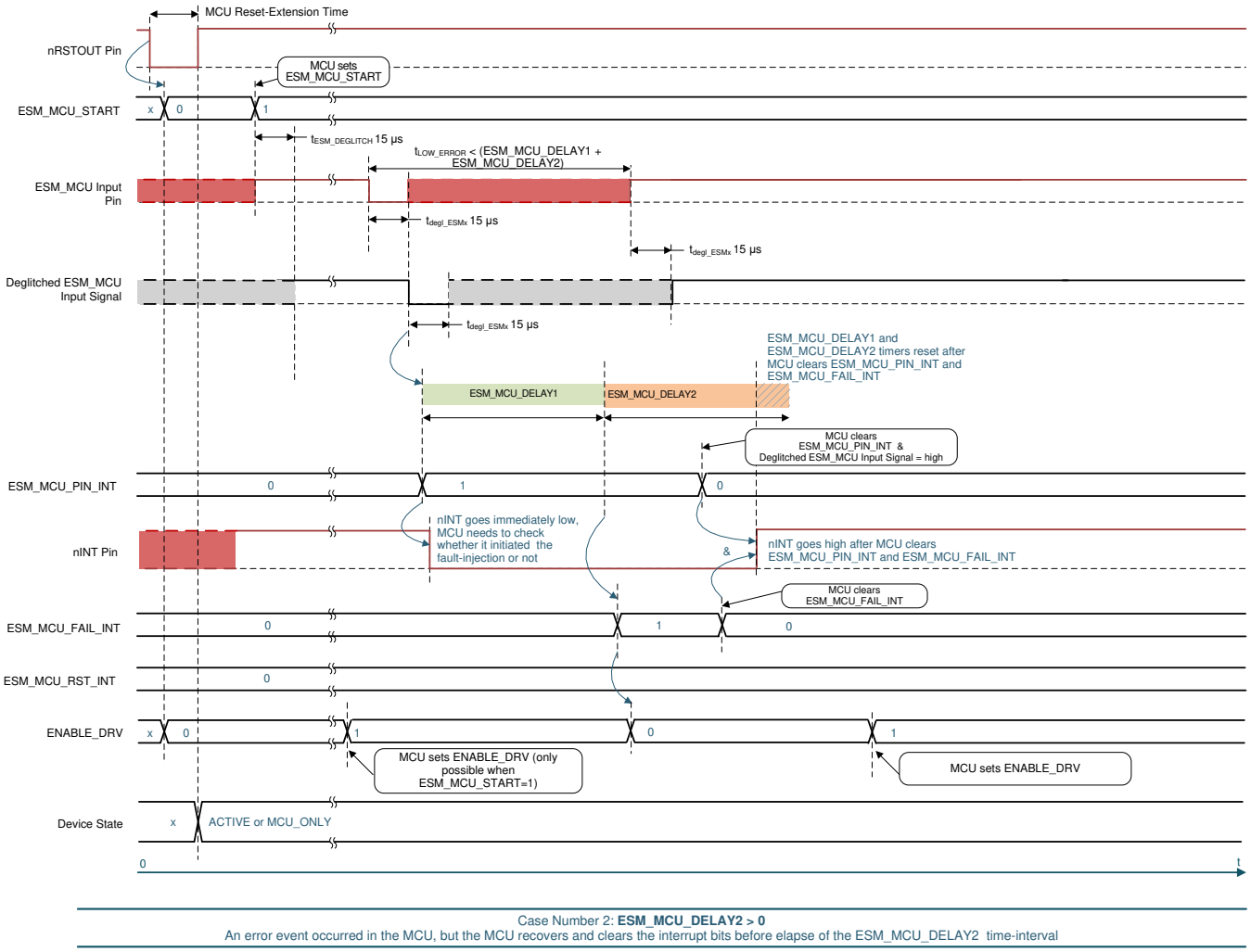

Case Number 2: **ESM_MCU_DELAY2 > 0**
An error event occurred in the MCU, but the MCU recovers and clears the interrupt bits before elapse of the ESM_MCU_DELAY2 time-interval

Figure 5-34. Example Waveform for ESM in Level Mode - Case Number 2: Delay-2 not set to 0 and ESM_MCU_ENDRV=1, ESM_MCU Signal Recovers Elapse of Delay-2 time-interval

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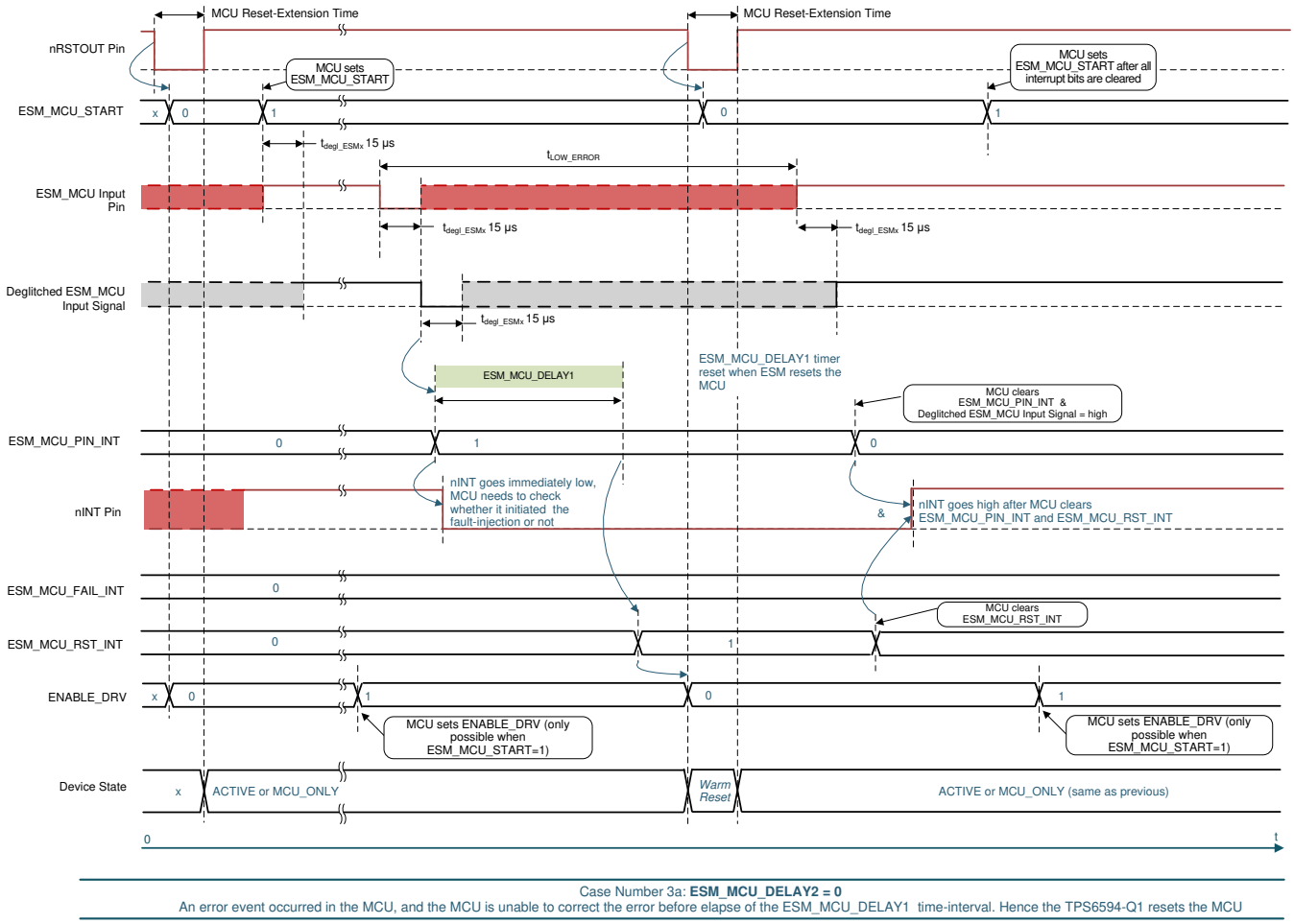

Figure 5-35. Example Waveform for ESM in Level Mode - Case Number 3a: Delay-2 set to 0 and ESM_MCU_ENDRV=1, ESM_MCU input signal recovers too late and MCU-reset occurs

ADVANCE INFORMATION

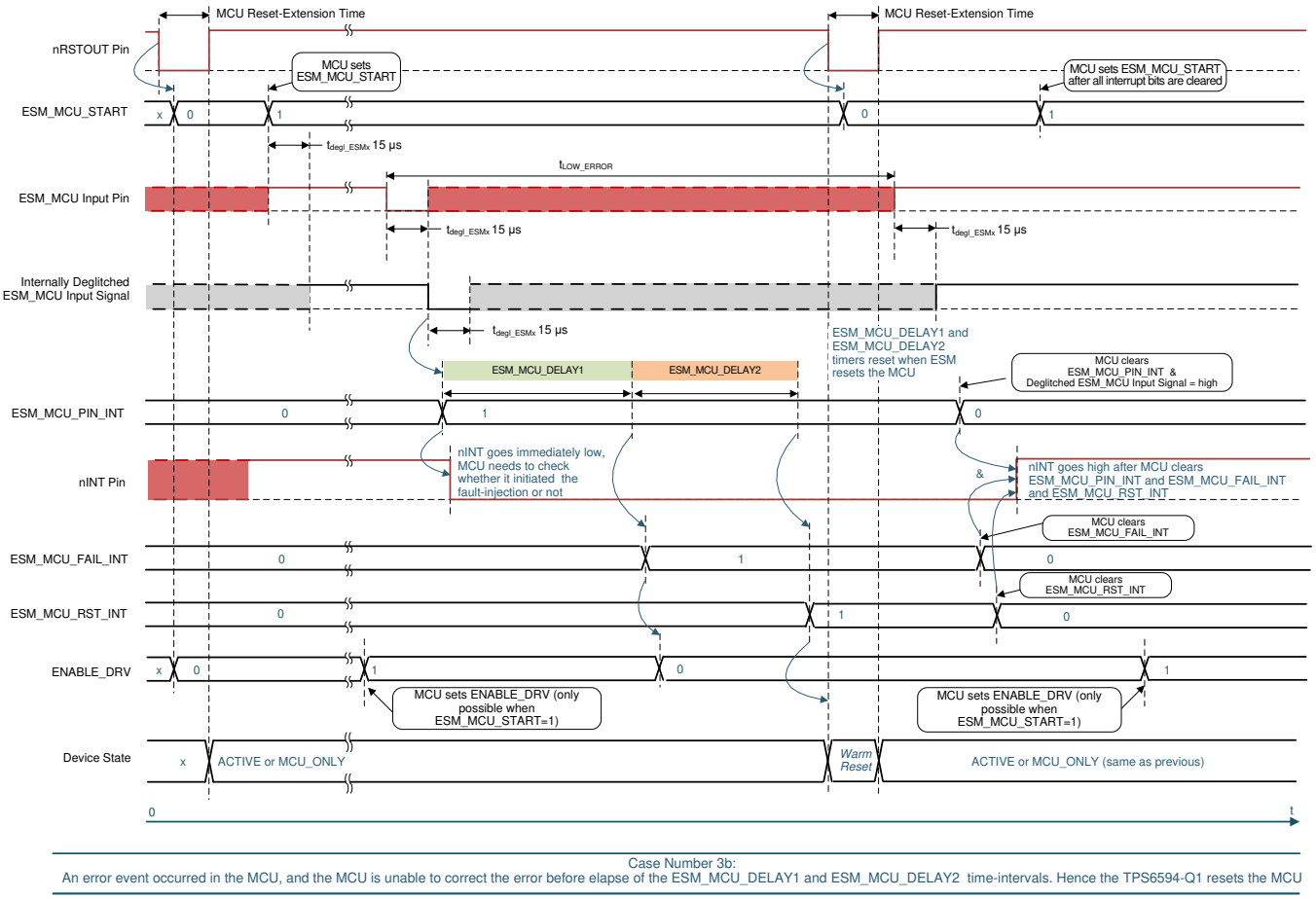

Figure 5-36. Example Waveform for ESM in Level Mode - Case Number 3b: Delay-2 not set to 0 and ESM_MCU_ENDRV=1, ESM_MCU input signal recovers too late and MCU-reset occurs

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5.3.11.3 PWM Mode

5.3.11.3.1 Good-Events and Bad-Events

In PWM mode, each ESM monitors the high-pulse and low-pulse duration times its PWM inputs signal as follows:

- after a falling edge, the ESM starts monitoring the low-pulse time-duration. If the input signal remains low after exceeding the maximum low-pulse time-threshold ($t_{LOW\_MAX\_TH}$), the ESM detects a bad event and the low-pulse duration counter reinitializes. Each time the signal further exceeds the maximum threshold, the ESM detects a bad event. On the next rising edge on the input signal, the ESM starts the high-pulse time-duration monitoring
- after a rising edge, the ESM starts monitoring the high-pulse time-duration. If the input signal remains high after exceeding the maximum high-pulse time-threshold ($t_{HIGH\_MAX\_TH}$), the ESM detects a bad event and the high-pulse duration counter reinitializes. Each time the signal further exceeds the maximum threshold, the ESM detects a bad event. On the next falling edge on the input signal, the ESM starts the low-pulse time-duration monitoring.

In addition, each ESM detects a bad-event in PWM mode if one of the events that follow occurs on the deglitched signal of the related input pin nERR_MCU or nERR_SoC:

- A high-pulse time-duration which is longer than the maximum high-pulse time-threshold ($t_{HIGH\_MAX\_TH}$) that is configured in corresponding ESM_MCU_HMAX[7:0] or ESM_SOC_HMAX[7:0].
- A high-pulse time-duration which is shorter than the minimum high-pulse time-threshold ($t_{HIGH\_MIN\_TH}$) that is configured in corresponding ESM_MCU_HMIN[7:0] or ESM_SOC_HMIN[7:0].
- A low-pulse time-duration which is longer than the maximum low-pulse time-threshold ($t_{LOW\_MAX\_TH}$) that is configured in corresponding ESM_MCU_LMAX[7:0] or ESM_SOC_LMAX[7:0].
- A low-pulse time-duration which is less than the minimum low-pulse time-threshold ($t_{LOW\_MIN\_TH}$) that is configured in corresponding ESM_MCU_LMIN[7:0] or ESM_SOC_LMIN[7:0].

The ESM detects a good-event in PWM mode if one of the events that follow occurs on the deglitched signal of the related input pin nERR_MCU or nERR_SoC:

- a low-pulse time-duration within the minimum and maximum low-pulse time-thresholds is followed by a high-pulse time-duration within the minimum and maximum high-pulse time-thresholds, or
- a high-pulse duration within the minimum and maximum high-pulse time-thresholds is followed by a low-pulse duration within the minimum and maximum low-pulse time-thresholds

ESM_MCU_HMAX[7:0] and ESM_SOC_HMAX[7:0] set the maximum high-pulse time-threshold ($t_{HIGH\_MAX\_TH}$) for the related ESM. Use Equation 14 and Equation 15 to calculate the worst-case values for the $t_{HIGH\_MAX\_TH}$:

$$\text{Min. } t_{HIGH\_MAX\_TH} = (15\ \mu s + \text{ESM\_x\_HMAX[7:0]} \times 15\ \mu s) \times 0.95 \quad (14)$$

$$\text{Max. } t_{HIGH\_MAX\_TH} = (15\ \mu s + \text{ESM\_x\_HMAX[7:0]} \times 15\ \mu s) \times 1.05 \quad (15)$$

, in which x stands for either MCU or SoC.

ESM_MCU_HMIN[7:0] and ESM_SOC_HMIN[7:0] set the minimum high-pulse time-threshold ($t_{HIGH\_MIN\_TH}$) for the related ESM. Use Equation 16 and Equation 17 to calculate the worst-case values for the $t_{HIGH\_MIN\_TH}$:

$$\text{Min. } t_{HIGH\_MIN\_TH} = (15\ \mu s + \text{ESM\_x\_HMIN[7:0]} \times 15\ \mu s) \times 0.95 \quad (16)$$

$$\text{Max. } t_{HIGH\_MIN\_TH} = (15\ \mu s + \text{ESM\_x\_HMIN[7:0]} \times 15\ \mu s) \times 1.05 \quad (17)$$

, in which x stands for either MCU or SoC.

ESM_MCU_LMAX[7:0] and ESM_SOC_LMAX[7:0] set the maximum low-pulse time-threshold ($t_{LOW\_MAX\_TH}$) for the related ESM. Use Equation 18 and Equation 19 to calculate the worst-case values for the $t_{LOW\_MAX\_TH}$:

$$\text{Min. } t_{LOW\_MAX\_TH} = (15\ \mu s + \text{ESM\_x\_LMAX[7:0]} \times 15\ \mu s) \times 0.95 \quad (18)$$

$$\text{Max. } t_{LOW\_MAX\_TH} = (15\ \mu s + \text{ESM\_x\_LMAX[7:0]} \times 15\ \mu s) \times 1.05 \quad (19)$$

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, in which x stands for either MCU or SoC.

ESM_MCU_LMIN[7:0] and ESM_SOC_LMIN[7:0] set the minimum low-pulse time-threshold ($t_{LOW\_MIN\_TH}$) for the related ESM. Use Equation 20 and Equation 21 to calculate the worst-case values for the $t_{LOW\_MIN\_TH}$:

Min. $t_{LOW\_MIN\_TH}$ = (15 µs +ESM_x_LMIN[7:0] × 15 µs) × 0.95 (20)

Max. $t_{LOW\_MIN\_TH}$ = (15 µs +ESM_x_LMIN[7:0] × 15 µs) × 1.05 (21)

, in which x stands for either MCU or SoC.

Please note that when setting up the minimum and the maximum low/high-pulse time-thresholds need to be configured such that clock tolerances from the TPS6594-Q1 and from the processor are incorporated. Equation 22, , Equation 24, and Equation 25are a guideline on how to incorporate these clock-tolerances:

ESM_x_HMIN[7:0] < 0.5 × (ESM_x_HMAX[7:0] + ESM_x_HMIN[7:0]) × 0.95 × (1 - MCU/SoC clock tolerance) (22)

ESM_x_HMAX[7:0] > 0.5 × (ESM_x_HMAX[7:0] + ESM_x_HMIN[7:0]) × 1.05 × (1 + MCU/SoC clock tolerance) (23)

ESM_x_LMIN[7:0] < 0.5 × (ESM_x_LMAX[7:0] + ESM_x_LMIN[7:0]) × 0.95 × (1 - MCU/SoC clock tolerance) (24)

ESM_x_LMAX[7:0] > 0.5 × (ESM_x_LMAX[7:0] + ESM_x_LMIN[7:0]) × 1.05 × (1 + MCU/SoC clock tolerance) (25)

5.3.11.3.2 ESM Error-Counter

If an ESM detects a bad-event, it increments its related error-counter (bits ESM_MCU_ERR_CNT[4:0] or bits ESM_SOC_ERR_CNT[4:0]) by 2. If an ESM detects a good-event, it decrements its related error-counter (bits ESM_MCU_ERR_CNT[4:0] or bits ESM_SOC_ERR_CNT[4:0]) by 1.

The device clears each error counter when ESM_x_START=0. Furthermore, the device clears the error-counter ESM_SOC_ERR[4:0] when it resets the SoC.

Each error-counter has a related threshold (bits ESM_MCU_ERR_CNT_TH[3:0] or bits ESM_SOC_ERR_CNT_TH[3:0]) which the MCU can configure if the related ESM start-bit is 0. If the error-counter value is above its configured threshold, the related ESM has detected a so-called ESM-error and starts the Error-Handling Procedure as described in Section 5.3.11.1. If the error-counter reached a value equal or less its configured threshold before the elapse of the configured delay-1 or delay-2 time-intervals, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 5.3.11.1.

5.3.11.3.2.1 ESM Start-Up in PWM Mode

After MCU has set the start bit of an ESM (bit ESM_MCU_START or bit ESM_SOC_START), there are two possible scenarios:

A. The deglitched signal of the monitored input pin has a low level at the moment the MCU sets the start bit. In this scenario, the related ESM starts the following procedure:
   1. Start a timer with a time-length according the value configured in correspondig ESM_MCU_LMAX[7:0] or ESM_SOC_LMAX[7:0].
   2. Wait for a first rising edge on its deglitched input signal.
   3. If the rising edge comes before the configured time-length elapses, the ESM skips the next step and starts to monitor the high-pulse duration time. Hereafter, the ESM detects good-events or bad-events as described in Section 5.3.11.3.1. Figure 5-38 shows an example this scenario as Case Number 1.
   4. If the configured time-length (configured in corresponding ESM_MCU_LMAX[7:0] or ESM_SOC_LMAX[7:0]) elapses, the ESM detects a bad-event and increments the related error-counter with +2. Hereafter, the ESM detects good-events or bad-events as described in Section 5.3.11.3.1. Figure 5-40 shows an example this scenario as Case Number 3.
   5. If the error-counter value is above its configured threshold, the related ESM has detected a so-called ESM-error and starts the Error-Handling Procedure as described inSection 5.3.11.3.1.
   6. During this Error-Handling Procedure, the ESM continues to monitor its related input pin, and updates the error-counter accordingly when it detects good-events or bad-events, until the Error-

Handling Procedure reaches the step in which the device resets the MCU or SoC. Figure 5-41 shows a scenario in which the device resets the MCU or SoC as Case Number 4.

7. If the error-counter reaches a value equal or less its configured threshold before the elapse of the configured delay-1 or delay-2 time-intervals, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 5.3.11.3.1.

B. The deglitched signal monitored input pin has a high level at the moment the MCU sets the start bit. In this scenario, the related ESM starts the following procedure:

1. Start a timer with a time-length according the value configured in corresponding ESM_MCU_HMAX[7:0] or ESM_SOC_HMAX[7:0].
2. Wait for a first falling edge on its deglitched input signal.
3. If the falling edge comes before the configured time-length elapses, the ESM skips the next step and starts to monitor the low-pulse duration time. Hereafter, the ESM detects good-events or bad-events as described in Section 5.3.11.3.1. Figure 5-39 shows an example this scenario as Case Number 2.
4. If the configured time-length (configured in corresponding ESM_MCU_HMAX[7:0] or ESM_SOC_HMAX[7:0]) elapses, the ESM detects a bad-event and increments the related error-counter with +2. Hereafter, the ESM detects good-events or bad-events as described in Section 5.3.11.3.1.
5. If the error-counter value is above its configured threshold, the related ESM has detected a so-called ESM-error and starts the Error-Handling Procedure as described inSection 5.3.11.3.1.
6. During this Error-Handling Procedure, the ESM continues to monitor its related input pin, and updates the error-counter accordingly when it detects good-events or bad-events, until the Error-Handling Procedure reaches the step in which the device resets the MCU or SoC as Case Number 4.
7. If the error-counter reaches a value equal or less its configured threshold before the elapse of the configured delay-1 or delay-2 time-intervals, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 5.3.11.3.1.

For a complete overview on how the ESM works in PWM Mode, please refer to the flow-chart in Figure 5-37. Figure 5-38, Figure 5-39, Figure 5-40, and Figure 5-41 show example waveforms for several error-cases for the ESM in PWM Mode.

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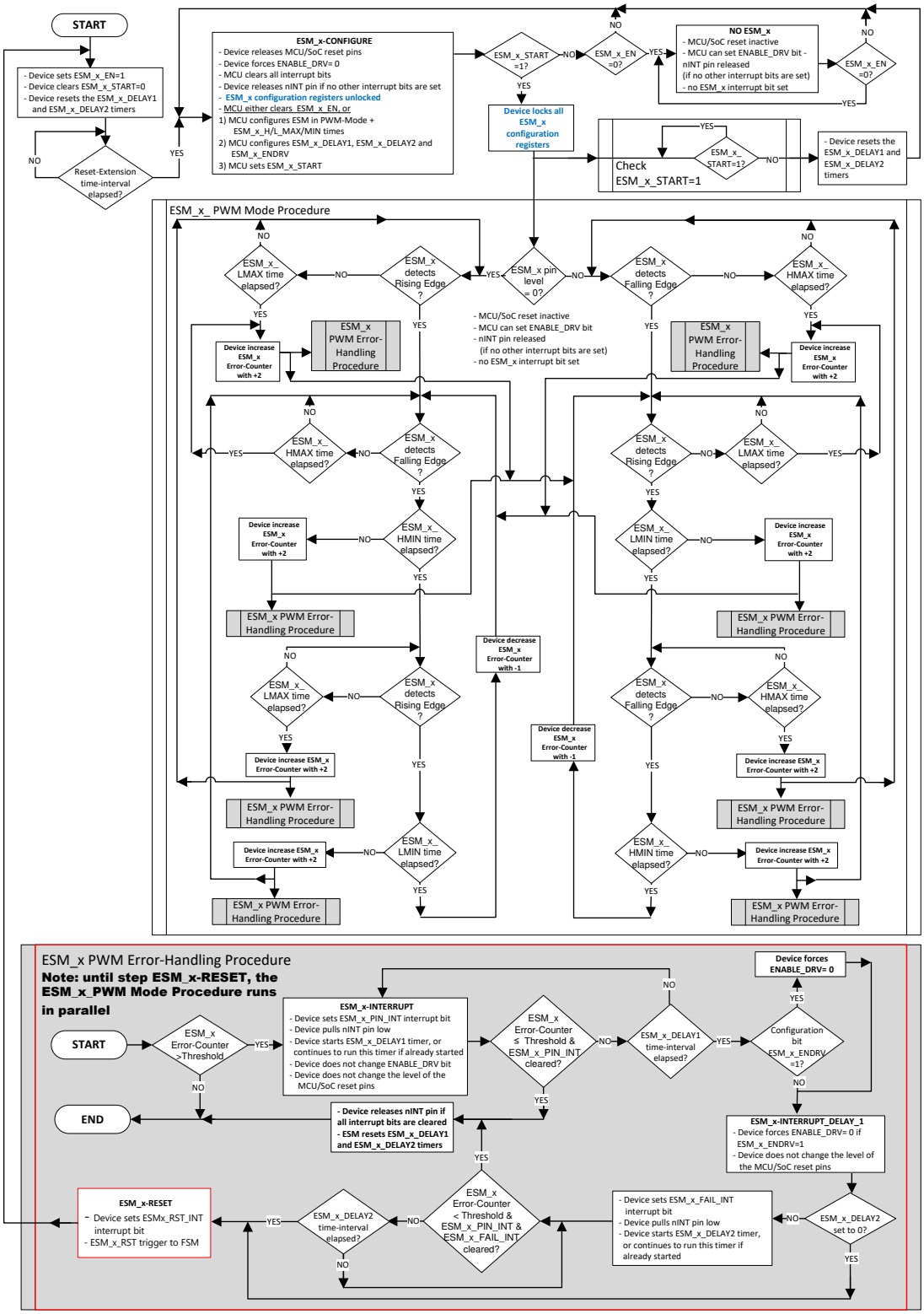

Figure 5-37. Flow-chart for ESM_MCU and ESM_SoC in PWM Mode

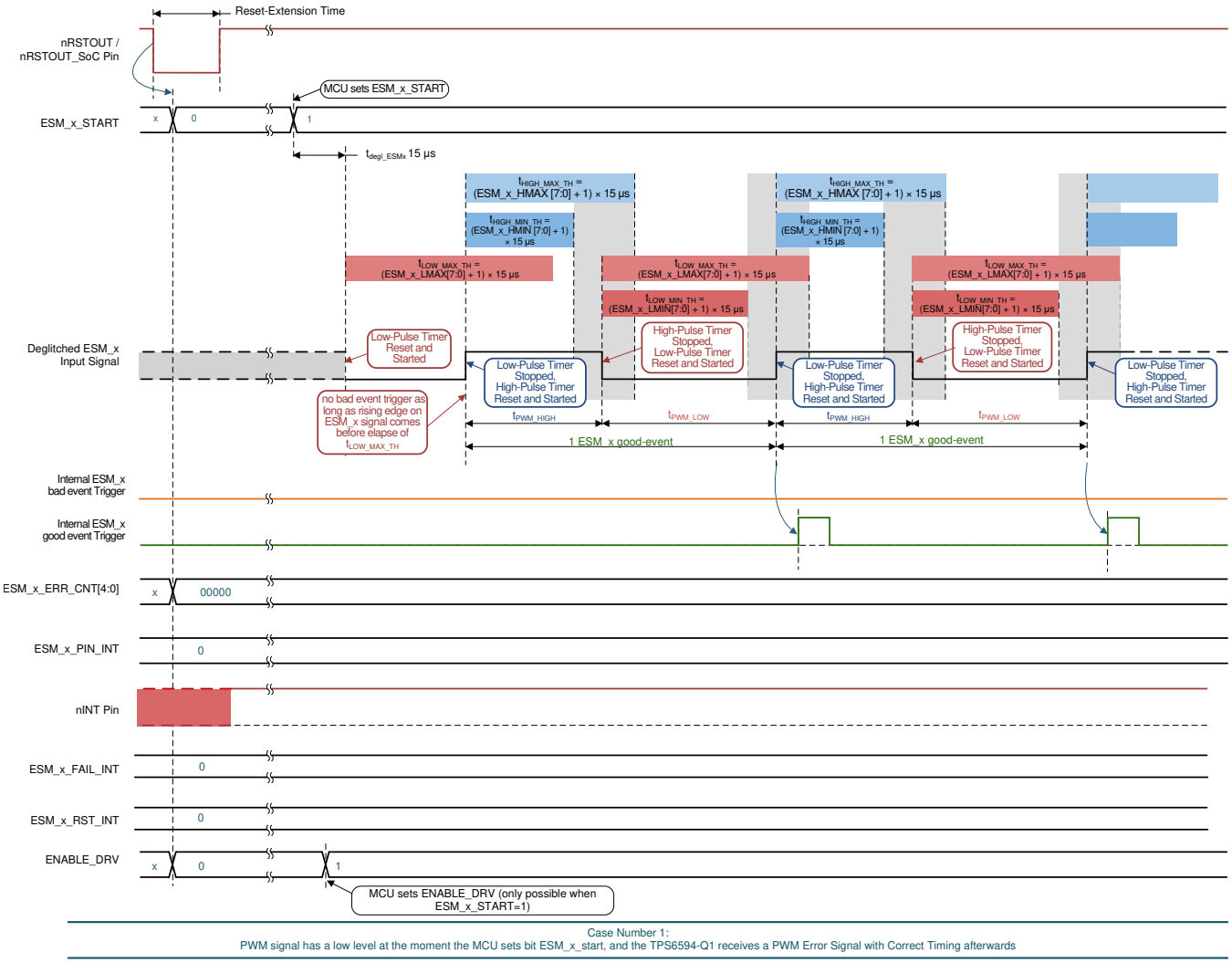

Figure 5-38. Example Waveform for ESM in PWM Mode - Case Number 1: ESM starts with low-level at deglitched input signal, and receives correct PWM signal afterwards

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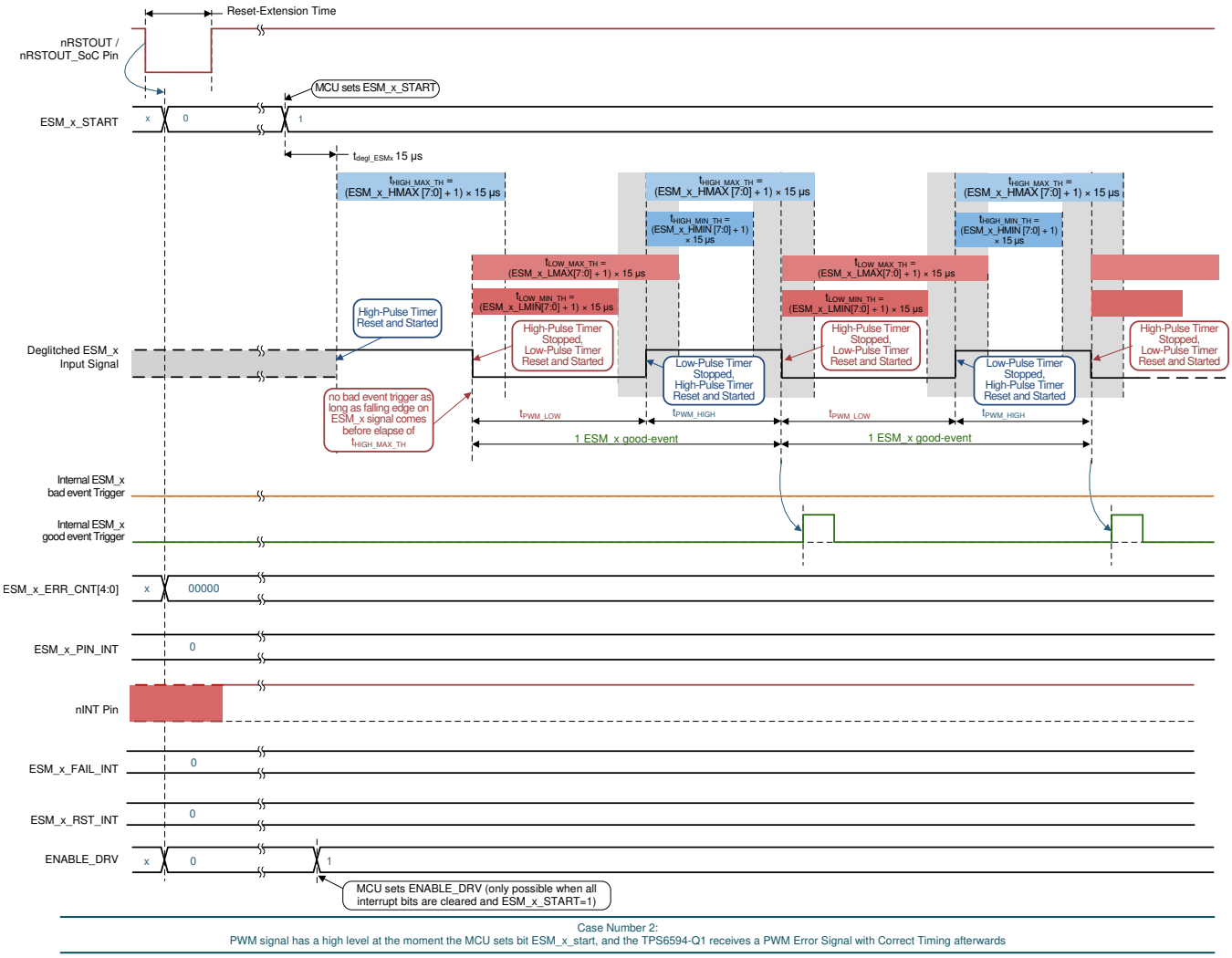

Figure 5-39. Example Waveform for ESM in PWM Mode - Case Number 2: ESM starts with high-level at deglitched input signal, and receives correct PWM signal afterwards

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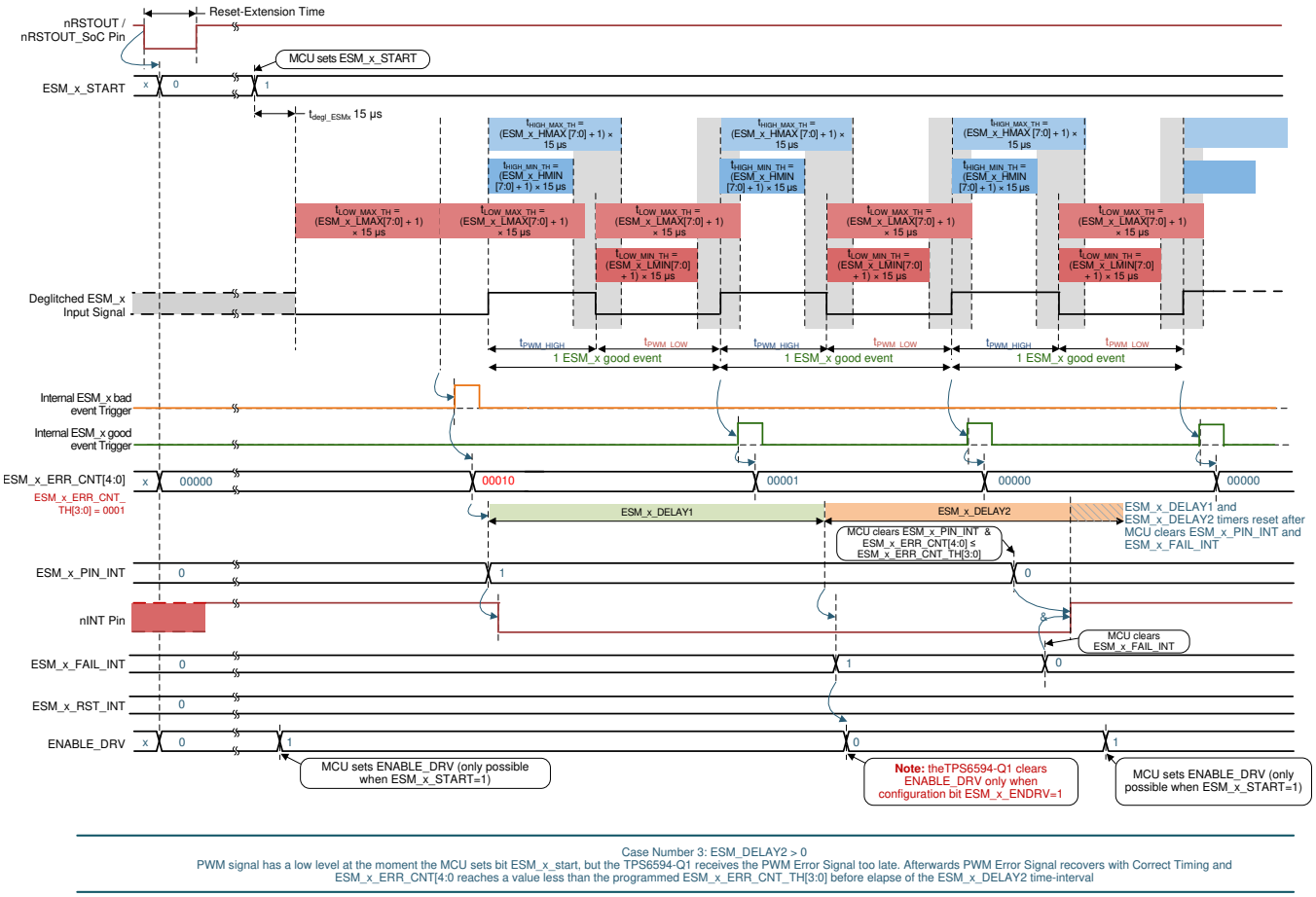

Case Number 3: ESM_DELAY2 > 0
PWM signal has a low level at the moment the MCU sets bit ESM_x_start, but the TPS6594-Q1 receives the PWM Error Signal too late. Afterwards PWM Error Signal recovers with Correct Timing and ESM_x_ERR_CNT[4:0 reaches a value less than the programmed ESM_x_ERR_CNT_TH[3:0] before elapse of the ESM_x_DELAY2 time-interval

Figure 5-40. Example Waveform for ESM in PWM Mode - Case Number 3: ESM starts with low-level at deglitched input signal, but receives too late a correct PWM signal afterwards

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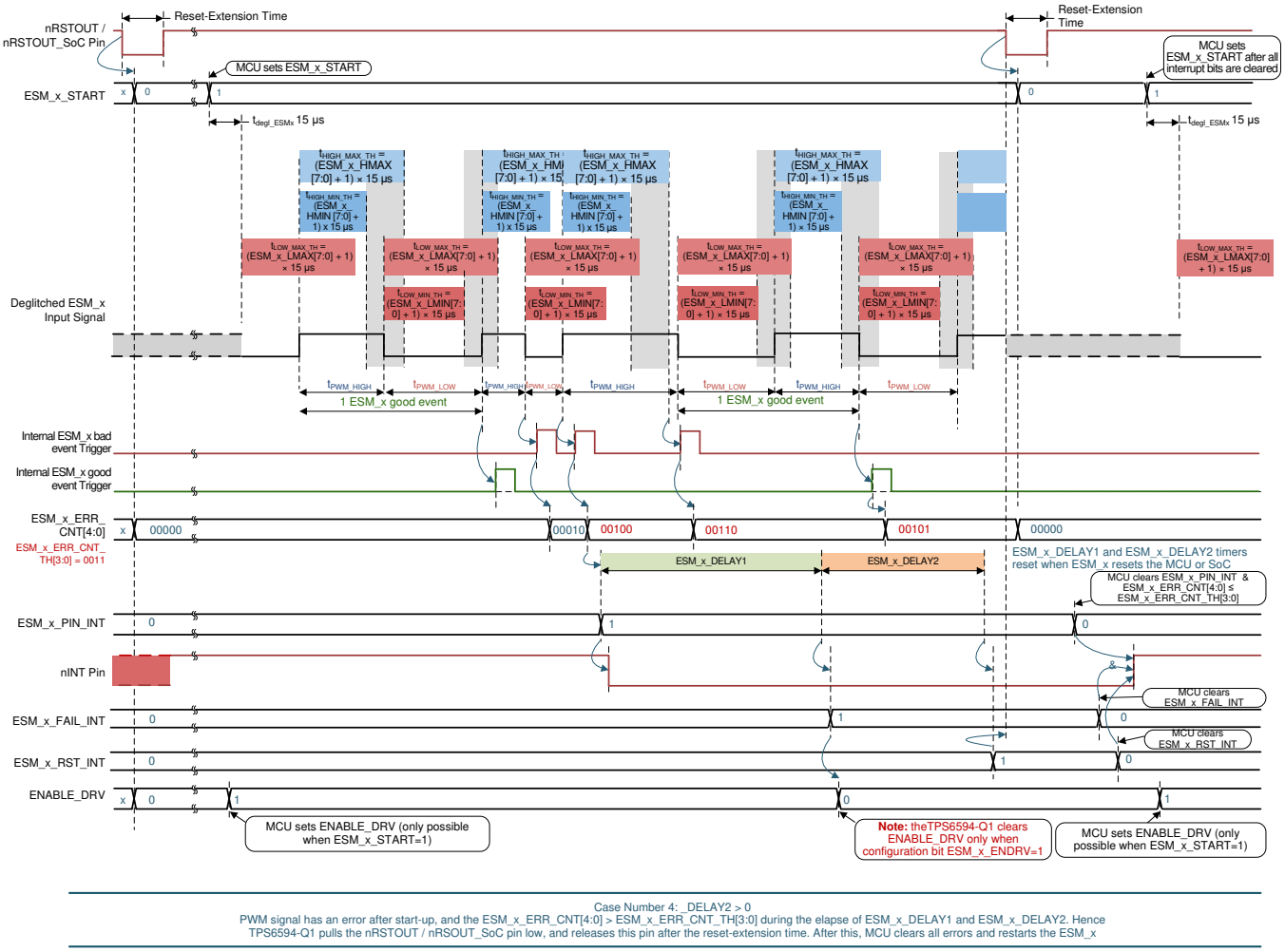

Case Number 4: _DELAY2 > 0
PWM signal has an error after start-up, and the ESM_x_ERR_CNT[4:0] > ESM_x_ERR_CNT_TH[3:0] during the elapse of ESM_x_DELAY1 and ESM_x_DELAY2. Hence TPS6594-Q1 pulls the nRSTOUT / nRSOUT_SoC pin low, and releases this pin after the reset-extension time. After this, MCU clears all errors and restarts the ESM_x

Figure 5-41. Example Waveform for ESM in PWM Mode - Case Number 4: ESM starts with low-level at deglitched input signal and receives a correct PWM signal. Afterwards the ESM detects bad events, and the PWM signal recovers too late which leads to a reset of the MCU or SoC

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5.4 Device Functional Modes

5.4.1 Device State Machine

The TPS6594-Q1 device integrates an finite state machine (FSM) engine which manages the state of the device during operating state transitions. It supports EEPROM configurable mission states with configurable input triggers for transitions between states. Any resources, including the 5 bucks, 4 LDOs, and all of the digital IO pins including the 11 GPIO pins on the device, can be controlled during power sequencing. When a resource is not controlled or configured through a power sequence, the resource is left in the default state as pre-configured by the NVM.

Each resource can be pre-configured through the NVM configuration, or re-configured through register bits. Therefore, the user can statically control the resource through the control interfaces (I^2C or SPI), or the FSM can automatically control the resource during state sequences.

The FSM is powered by an internal LDO which is automatically enabled when VCCA supply is available to the device. Ensuring that the VCCA supply, which is the protected input supply connected to VSYS_SENSE via the external high voltage load switch, is the first supply available to the device is important to ensure proper operation of all the power resources as well as the control interface and device IOs.

There are 3 parts of the FSM which control the operational modes of the TPS6594-Q1 device:

- Hardware Device Power States (HFSM)
- Pre-Configurable Mission States (PFSM)
- Error Handling Operations

The PFSM works in concert with a traditional HFSM in order to draw from the strengths of both designs and to reduce the high cost of a completely configurable FSM. The PFSM provides configurable rail sequencing utilizing instructions in configuration memory. This flexibility enables customers to alter power-up sequences on a platform basis. The HFSM handles the majority of fixed functionality that is internally mandated and common to all platforms.

5.4.1.1 Hardware Device Power States

The Hardware Device Power States portion of the FSM engine (HFSM) manages to power up the device before the power rails are fully enabled and ready to power external loadings, and to power down the device when in the events of insufficient power supply or device/system error conditions. While the device is in one of the Hardware Device Powers states, the ENABLE_DRV bit remains low.

The definitions and transition triggers of the Device Power States are fixed and cannot be reconfigured.

Following are the definitions of the Device Power states:

NO SUPPLY The device is not powered by a valid energy source on the system power rail. The device is completely powered off.

BACKUP (RTC backup battery) The device is not powered by a valid supply on the system power rail (VCCA < VCCA_UVLO). However a backup power source is present and is within the operating range of the LDOVRTC. The RTC clock counter remains active in this state if it has been previously activated by appropriate register enable bit. The calendar function of the RTC block is not activated in this state. Customer has the option to enable the *shelf mode* by setting the LDORTC_DIS bit to 1 while the I2C is in operation. This bit will force the device to skip the BACKUP state and enters the NO SUPPLY state under VCCA_UVLO condition.

LP_STANDBY The device can enter this state from a mission state after receiving a valid OFF request or an I2C trigger, and the LP_STANDBY_SEL= 1. When the device is in this state, the RTC clock counter and the RTC Alarm or Timer Wake up functions are active if they have been previously activated by appropriate register enable bit. Low Power Wake-up input monitor in the LDOVRTC domain (LP_WKUP secondary function through GPIO3 or GPIO4) and the on request monitors are also enabled in this state. When a logic level transition from high-to-low or low-to-high with a minimum pulse length of t_{LP_WKUP} is detection on the assigned LP_WKUP pin, or if the device detects an valid on-request or a wake up signal from the RTC block, the device will proceed to execute the power up sequence and reach the default

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mission state. More details regarding the LP_WAKE function can be found in Section 5.4.1.2.2.3.

INIT The device is powered by a valid supply on the system power rail (VCCA ≥ VCCA_UV) and have received an external wake-up signal such as CAN WAKE-UP, the RTC alarm or timer wake-up signal, or an On Request from the nPWRON/ENABLE pin. Device digital and monitor circuits are powered up. The PMIC reads its internal NVM memory in this state and configures default values to registers, IO configuration and FSM accordingly.

BOOT BIST The device is running the built-in self test routine which includes both the LBIST (around 3ms run time) and the ABIST/CRC (around 100µs run time). An option is available to shorten the device power up time from the NO_SUPPLY state by setting the NVM bit FAST_BOOT_BIST = '1" to skip the LBIST. Software can also set the FAST_BIST = '1' to skip LBIST after the device wakes up from the LP STANDBY state. When the device arrives this state from the SAFE_RECOVERY state, LBIST is automatically skipped if it has not previously failed. If LBIST failed, but passed after multiple re-tries before exceeding the recovery counter limit, the device will be powered up normally. The following NVM bits are additional options which can be set to disable parts of the ABIST/CRC tests if further sequence time reduction is required. Note that the BIST tests are executed as parallel processes, and the longest process determines the total BIST duration. Therefore the following options does not guarantee a certain amount of time saving from the total BIST duration:

- REG_CRC_EN = '0': disables the register map and SRAM CRC check
- VMON_ABIST_EN = '0': disables the ABIST for the VMON OV/UV function
- SPMI_WD_EN = '0': disables the SPMI Watchdog operation for the SPMI WD function

RUNTIME BIST A request was received from the MCU to exercise runtime BIST on the device. No rails are modified and all external signals, include all I^2C or SPI interface communications, are ignored during BIST. If the device passed BIST, it will resume the previous operation. if the device failed BIST, it will shut down all of the regulator outputs and proceed to the SAFE RECOVERY state. In order to avoid a register CRC error, all register write must be avoid after the request for the BIST operation until an interrupt is asserted to indicate the completion of BIST. The results of the BIST are indicated by the BIST_PASS_INT or the BIST_FAIL_INT bits.

SAFE RECOVERY The device meets the qualified error condition for immediate or ordered shutdown request. If the error is recovered within the recovery time interval, the device will increment the recovery count, and return to INIT state if the recovery count does not exceeded the threshold of the counter. If the recovery count exceeded the threshold or if the error cannot be recovered, such as the die temperature cannot be reduced to < T_{WARN}, or if VCCA stays above OVP threshold, the device will stay in SAFE RECOVERY state until supply power cycle occurs.

When multiple system conditions occur simultaneously which demands power state arbitration, the device will go to the higher priority state according to the following priority order:

1. NO SUPPLY
2. BACKUP
3. SAFE_RECOVERY
4. LP_STANDBY
5. MISSION STATES

Figure 5-42 shows the power trasition states of the FSM engine.

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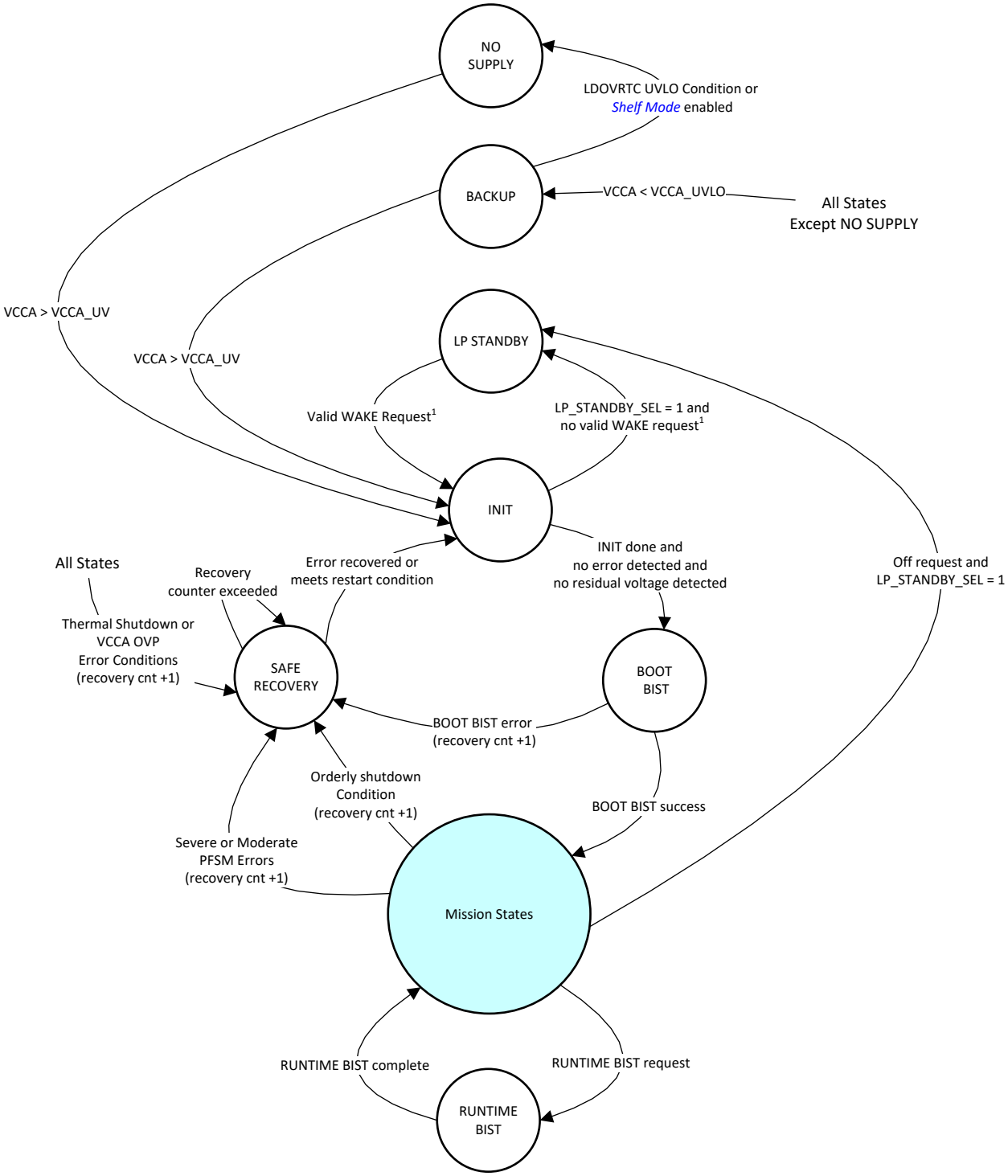

[1] A valid WAKE request consist of:

- nPWRON/ENABLE on request detection if the device arrived the LP_STANDBY state through the long key-press of the nPWRON pin or by disabling the ENABLE pin, or
- RTC Alarm, RTC Timer, LP_WKUP1 or LP_WKUP2 detection if the device arrived the LP_STANDBY state through writing to a TRIGGER_I2C_0 bit.

Figure 5-42. State Diagram for Device Power States

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5.4.1.2 Pre-Configurable Mission States

When the device arrives a mission state, all rail sequencing is controlled by the pre-configurable FSM engine (PFSM) through the configuration memory. The configuration memory allows configurations of the triggers and the operation states which together form the configurable sub state machine within the scope of mission states. This sub state machine could be used to control and sequence the different voltage outputs as well as any GPIO outputs that can be used as enable for external rails. Various forms of register writes provide the means of controlling the external environment. When the device is in a mission state, it has the capacity to supply the processor and other platform modules depending on the power rail configuration. The definitions and transition triggers of the mission states are configurable via NVM configuration.

When the device is in any one of the Mission States, the state with the higher power level has the higher priority. For instance, if the Mission States consist of ACTIVE, MCU ONLY, DEEP SLEEP, S2R, STANDBY states, the priority order of these states should be in the following order:

1. ACTIVE
2. MCU ONLY
3. DEEP SLEEP / S2R
4. STANDBY

5.4.1.2.1 Mission State Configuration

The Mission States portion of the FSM engine manages the power sequence of the power rails in state such as ACTIVE, MCU ONLY, DEEP SLEEP, etc. The device must be powered by a valid supply on the system power rail (VCCA > VCCA_UV) and has received a start-up event before it can reach a mission state. Figure 5-43 is an example state machine which can be configured through configuration memory.

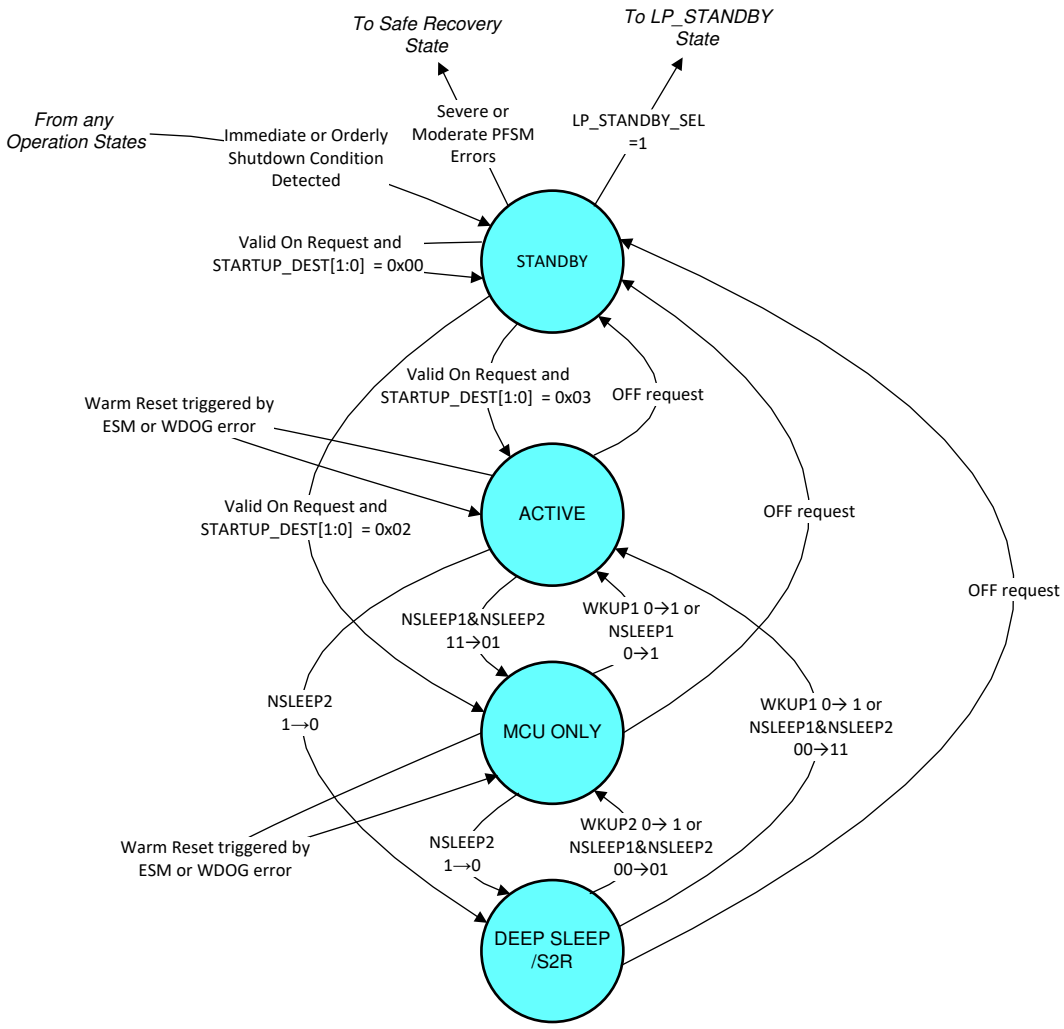

Figure 5-43. Example of a Mission State-Machine

When the device reaches any mission state, the rail sequencing defined in the state (colored in light blue in Figure 5-43) can be configured in the configuration memory. When the PMIC determines that a transition to another operation state is necessary, it will read the configuration memory to determine what sequencing is needed for the state transition.

The trigger signals for each state transition can come from a variety of GPIO inputs or potential error sources. In order to processes all of the possible error sources inside the PFSM engine, a hierarchical mask system is applied to filter out the common errors which can be handled by interrupt only, and categorize the other error sources as Severe Global Error, Moderate Global Error, and other errors as show in Figure 5-44. The filtered and categorized triggers are send into the PFSM engine, which then determines the entry and exit condition for each configured mission state.

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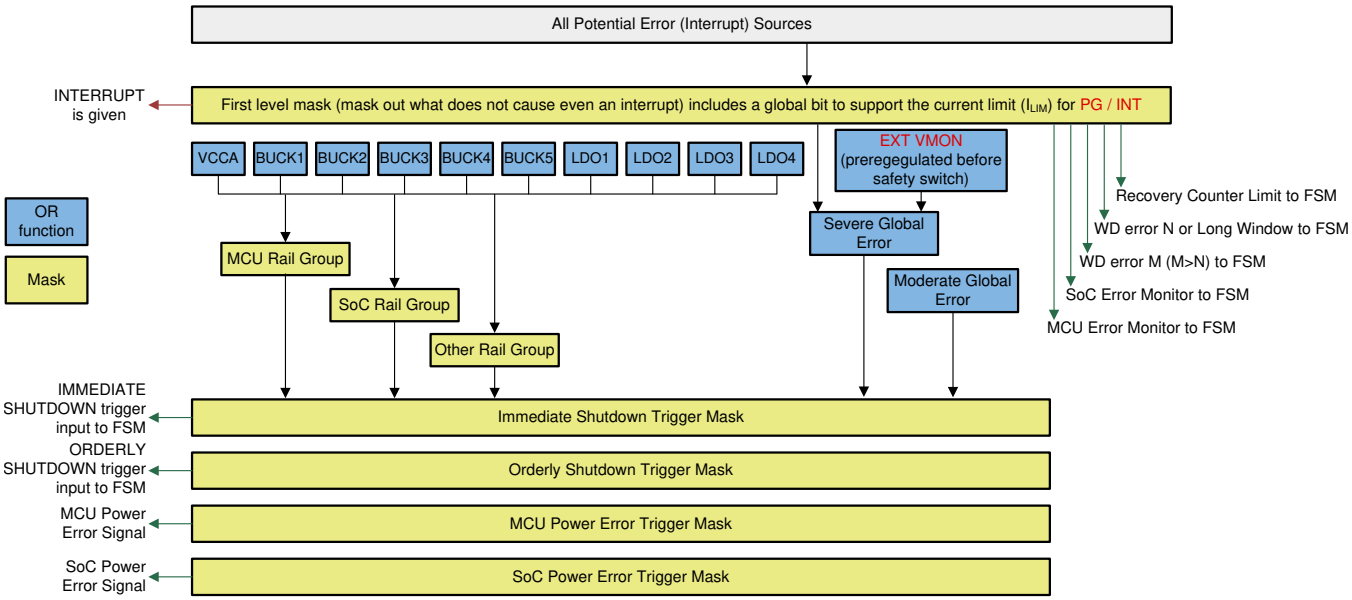

Figure 5-44. Error Source Hierarchical Mask System

The PFSM engine utilizes instructions to execute the configured device state transitions. Table 5-12shows the code and description of each command in the instruction set.

Table 5-12. Configurable FSM Instruction set

Command Opcode	Command	Command Description
"0000"	REG_WRITE_MASK_PAGE0_IMM	Write the specified data, except the masked bits, to the specified page 0 register address
"0001"	REG_WRITE_IMM	Write the specified data to the specified register address
"0010"	REG_WRITE_MASK_IMM	Write the specified data, except the masked bits, to the specified register address
"0011"	REG_WRITE_VOUT_IMM	Write the target voltage of a specified regulator after a specified delay
"0100"	REG_WRITE_VCTRL_IMM	Write the operation mode of a specified regulator after a specified delay
"0101"	REG_WRITE_MASK_SREG	Write the data from a scratch register, except the masked bits, to the specified register address
"0110"	SREG_READ_REG	Write scratch register (REG0-3) with data from a specified address
"0111"	WAIT	Execution is paused until the specified type of the condition is met or timed out
"1000"	DELAY_IMM	Delay the execution by a specified time
"1001"	DELAY_SREG	Delay the execution by a time value stored in the specified scratch register
"1010"	TRIG_SET	Set a trigger destination address for a given input signal or condition
"1011"	TRIG_MASK	Sets a trigger mask that determines which triggers are active.
"1100"	END	Mark the final instruction in a sequential task
"1101"	REG_WRITE_BIT_PAGE0_IMM	Write the specified data to the BIT_SEL location of the specified page 0 register address
"1110"	REG_WRITE_WIN_PAGE0_IMM	Write the specified data to the SHIFT location of the specified page 0 register address
"1111"	SREG_WRITE_IMM	Write the specified data to the scratch register (REG0-3)

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5.4.1.2.1.1 REG_WRITE_IMM Command

Table 5-13 shows the format of the REG_WRITE_IMM commands

Table 5-13. REG_WRITE_IMM Command Format

Bits[21:14]	Bits[13:4]	Bits[3:0]
DATA	ADDR	CMD
8 bits	10 bits	4 bits

Description: Write the specified data to the specified register address

Fields:

- CMD: Command opcode (0x1)
- ADDR: Address of register to be written
- DATA: Data to be written

Assembly command: **REG_WRITE_IMM [ADDR=]<Address> [DATA=]<Data>**

Address and Data can be in any literal integer format (decimal, hex, etc.).

'ADDR=' and 'DATA=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_IMM 0x1D 0x55** - Write value 0x55 to address 0x1D
- **REG_WRITE_IMM ADDR=0x10 DATA=0xFF** - Write value 0xFF to address 0x10
- **REG_WRITE_IMM DATA=0xFF ADDR=0x10** - Write value 0xFF to address 0x10

5.4.1.2.1.2 REG_WRITE_MASK_IMM Command

Table 5-14 shows the format of the REG_WRITE_MASK_IMM commands

Table 5-14. REG_WRITE_MASK_IMM Command Format

Bits[29:22]	Bits[21:14]	Bits[13:4]	Bits[3:0]
MASK	DATA	ADDR	CMD
8 bits	8 bits	10 bits	4 bits

Description: Write the specified data, except the masked bits, to the specified register address

Fields:

- CMD: Command opcode (0x2)
- ADDR: Address of register to be written
- DATA: Data to be written
- MASK: Mask used to select bits to be modified. Only bits with mask=0 are modified

Assembly command: **REG_WRITE_MASK_IMM [ADDR=]<Address> [DATA=]<Data> [MASK=]<Mask>**

Address, Data, and Mask can be in any literal integer format (decimal, hex, etc.).

'ADDR=', 'DATA=', and 'MASK=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_MASK_IMM 0x1D 0x80 0xF0** - Write 0b1000 to the upper 4 bits of the register at address 0x1D
- **REG_WRITE_MASK_IMM ADDR=0x10 DATA=0x0F MASK=0xF0** - Write 0b1111 to the lower 4 bits of the register at address 0x10
- **REG_WRITE_MASK_IMM DATA=0x0F MASK=0xF0 ADDR=0x10** - Write 0b1111 to the lower 4 bits of the register at address 0x10

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5.4.1.2.1.3 REG_WRITE_MASK_PAGE0_IMM Command

Table 5-14 shows the format of the REG_WRITE_MASK_PAGE0_IMM commands

Table 5-15. REG_WRITE_MASK_PAGE0_IMM Command Format

Bits[27:20]	Bits[19:12]	Bits[11:4]	Bits[3:0]
MASK	DATA	ADDR	CMD
8 bits	8 bits	8 bits	4 bits

Description: Write the specified data, except the masked bits, to the specified page 0 register address

Fields:

- CMD: Command opcode (0x0)
- ADDR: Page 0 address of register to be written
- DATA: Data to be written
- MASK: Mask used to select bits to be modified. Only bits with mask=0 are modified

Assembly command: **REG_WRITE_MASK_PAGE0_IMM [ADDR=]<Address> [DATA=]<Data> [MASK=]<Mask>**

Address, Data, and Mask can be in any literal integer format (decimal, hex, etc.).

'ADDR=', 'DATA=', and 'MASK=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_MASK_PAGE0_IMM 0x1D 0x80 0xF0** - Write 0b1000 to the upper 4 bits of the register at address 0x1D
- **REG_WRITE_MASK_PAGE0_IMM ADDR=0x10 DATA=0x0F MASK=0xF0** - Write 0b1111 to the lower 4 bits of the register at address 0x10
- **REG_WRITE_MASK_PAGE0_IMM DATA=0x0F MASK=0xF0 ADDR=0x10** - Write 0b1111 to the lower 4 bits of the register at address 0x10

5.4.1.2.1.3.1 REG_WRITE_BIT_PAGE0_IMM Command

Table 5-14 shows the format of the REG_WRITE_BIT_PAGE0_IMM commands

Table 5-16. REG_WRITE_BIT_PAGE0_IMM Command Format

Bits[15:13]	Bits[12]	Bits[11:4]	Bits[3:0]
BIT_SEL	DATA	ADDR	CMD
3 bits	1 bits	8 bits	4 bits

Description: Write the specified data to the BIT_SEL location of the specified page 0 register address

Fields:

- CMD: Command opcode (0xD)
- ADDR: Page 0 address of register to be written
- DATA: Data to be written
- BIT_SEL: Bit location within the register to be written

Assembly command: **REG_WRITE_BIT_PAGE0_IMM [ADDR=]<Address> [BIT=]<Bit> [DATA=]<Data>**

Address, Bit, and Data can be in any literal integer format (decimal, hex, etc.).

'ADDR=', 'BIT=', and 'DATA=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_BIT_PAGE0_IMM 0x1D 7 0** - Write '0' to bit 7 of the register at address 0x1D

- **REG_WRITE_BIT_PAGE0_IMM ADDR=0x10 BIT=3 DATA=1** - Write 0b1 to bit 3 of the register at address 0x10

5.4.1.2.1.3.2 REG_WRITE_WIN_PAGE0_IMM Command

Table 5-14 shows the format of the REG_WRITE_WIN_PAGE0_IMM commands

Table 5-17. REG_WRITE_WIN_PAGE0_IMM Command Format

Bits[23:22]	Bits[21:17]	Bits[16:12]	Bits[11:4]	Bits[3:0]
BYTE_SEL	MASK	DATA	ADDR	CMD
2 bits	5 bits	5 bits	8 bits	4 bits

Description: Write the specified data to the SHIFT location of the specified page 0 register address

Fields:

- CMD: Command opcode (0xE)
- ADDR: Page 0 address of register to be written
- DATA: Data to be written
- MASK: Mask used to select bits to be modified. Only bits with mask=0 are modified
- SHIFT: Data and mask will be left shifted by this amount

Assembly command: **REG_WRITE_WIN_PAGE0_IMM [ADDR=]<Address> [DATA=]<Data> [MASK=]<Mask> [SHIFT=]<Shift>**

Address, Data, Mask, and Shift can be in any literal integer format (decimal, hex, etc.).

'ADDR=', 'DATA=', 'MASK=', and 'SHIFT=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_WIN_PAGE0_IMM ADDR=0x1D DATA=0x8 MASK=0x13 SHIFT=2** - Write bits 5:4 to 0b10 to the register at address 0x1D. Data and mask give 5-bit value 0bx10xx. This is then left shifted 2 bits to give full byte value of 0bxx10xxxx, hence sets bits 5:4 to 0b10.

5.4.1.2.1.4 REG_WRITE_VOUT_IMM Command

Table 5-18 shows the format of the REG_WRITE_VOUT_IMM commands

Table 5-18. REG_WRITE_VOUT_IMM Command Format

Bits[23:18]	Bits[17:10]	Bits[9:8}	Bits[7:4]	Bits[3:0]
DELAY	VOUT	SEL	RAIL	CMD
6 bits	8 bits	2 bits	4 bits	4 bits

Description: Write the target voltage of a specified regulator after a specified delay. This is a spin-off of the REG_WRITE_IMM command with the intention to save instruction bits.

Fields:

- CMD: Command opcode (0x3)
- RAIL: Regulator ID to be configured. Valid values are 0-4: Buck1-5, and 8-11: LDO1-4
- SEL: Selection of BUCKn_VSET1 or BUCKn_VSET2 if RAIL is 0-4
- VOUT: Target voltage for the regulator. Set the value of the BUCK<X>_VOUT<Y> or the LDO<X>_VOUT registers. Variable X is determined by the RAIL selection, and variable Y (only for BUCK regulations) is determined by the BUCK<X>_VSEL value
- DELAY: Delay before modifying the regulator output voltage. This delay represents a threshold count for a counter running a step size specified in register PFSM_DELAY_STEP

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Assembly command: **REG_WRITE_VOUT_IMM [REGULATOR=]<Regulator ID> [SEL=]<VSEL> [VOUT=]<Vout> [DELAY=]<Delay>**

'REGULATOR=', ''SEL=', 'VOUT=', and 'DELAY=' are options. When included, the parameters can be in any order.

Regulator ID = BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, LDO1, LDO2, LDO3, or LDO4.

VSEL selects the BUCKn_VSET1 or BUCKn_VSET2 bits which the command will write to if Regulator ID is BUCK1-5. It is defined as: '0': BUCKn_VSET1, '1': BUCKn_VSET2, '2': Currently Active BUCKn_VSET, '3': Currently Inactive BUCKn_VSET. If Regulator ID is LDO1-4, VSEL value is ignored.

VOUT = output voltage in mV or V. Unit must be listed.

DELAY = delay time in ns, µs, ms, or s. If there is no units, it must be an integer value between 0-63, which will become the threshold count for the counter running a step size specified in the register PFSM_DELAY_STEP. Delay value will be rounded to the nearest achievable delay time based on the current step size. Current step size will default to the NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler will report an error if the step size is too large or too small to meet the delay.

Examples:

- **REG_WRITE_VOUT_IMM BUCK3 2 1.05V 100µs** - Sets BUCK3 to 1.05 V by updating the active BUCK3_VSET register after 100 µs
- **REG_WRITE_VOUT_IMM REGULATOR=LDO1 SEL=0 VOUT=700mV DELAY=6ms** - Sets LDO1 to 700 mV after 6 ms.

5.4.1.2.1.5 REG_WRITE_VCTRL_IMM Command

Table 5-19 shows the format of the REG_WRITE_VCTRL_IMM commands

Table 5-19. REG_WRITE_VCTRL_IMM Command Format

Bits[31:26]	Bits[25:18]	Bits[17:10]	Bits[9:8]	Bits[7:4]	Bits[3:0]
DELAY	MASK	VCTRL	DLY_MODE	RAIL	CMD
6 bits	8 bits	8 bits	2 bits	4 bits	4 bits

Description: Write the operation mode of a specified regulator after a specified delay. This is a spin-off of the REG_WRITE_IMM command with the intention to save instruction bits.

Fields:

- CMD: Command opcode (0x4)
- RAIL: Regulator ID of a rail to be configured. Valid values are 0-4: Buck1-5, and 8-11: LDO1-4
- DLY_MODE: 0:Delay if vctrl enable bit mismatches 1:Delay if any vctrl bits mismatch 2:Delay always 3: Reserved
- VCTRL: Data to write to the following regulator control fields: BUCKs: BUCKn_PLDN, BUCKn_VMON_EN, BUCKn_VSEL, BUCKn_FPWM_MP, BUCKn_FPWM, and BUCKn_EN. LDOs: LDOn_PLDN, LDOn_VMON_EN, 0, 0, LDOn_EN
- MASK: Mask used to select bits to be modified. Only bits with mask=0 are modified
- DELAY: Delay before modifying the regulator operation mode. This delay represents a threshold count for a counter running a step size specified in register PFSM_DELAY_STEP

Assembly command: **REG_WRITE_VCTRL_IMM [REGULATOR=]<Regulator ID> [VCTRL=]<VCTRL> [MASK=]<Mask> [DELAY=]<Delay> [DELAY_MODE=]<Delay Mode>**

'REGULATOR=', 'VCTRL=', 'MASK=', and 'DELAY=' are options. When included, the parameters can be in any order.

Regulator ID = BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, LDO1, LDO2, LDO3, or LDO4.

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VCTRL = 0-15, in hex, decimal, or binary format. Data to write to the following regulator control fields: BUCKs: BUCKn_PLDN, BUCKn_VMON_EN, BUCKn_VSEL, BUCKn_FPWM_MP, BUCKn_FPWM, and BUCKn_EN. LDOs: LDOn_PLDN, LDOn_VMON_EN, 0, 0, LDOn_EN

DELAY = delay time in ns, µs, ms, or s. If there is no units, it must be an integer value between 0-63, which will become the threshold count for the counter running a step size specified in the register PFSM_DELAY_STEP. Delay value will be rounded to the nearest achievable delay time based on the current step size. Current step size will default to the NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler will report an error if the step size is too large or too small to meet the delay.

Delay Mode must be one of the below options: MATCH_EN = 0 (Delay if vctrl enable bit mismatches) MATCH_ALL = 1 (Delay if any vctrl bits mismatch) ALWAYS = 2 (Delay always)

Examples:

- **REG_WRITE_VCTRL_IMM BUCK3 0x00 0xE0 100µs** - Sets BUCK3 to OFF (VCTRL bits = 0b00000) after 100 µs
- **REG_WRITE_VCTRL_IMM REGULATOR=LDO1 VCTRL=0x09 MASK=0x36 DELAY=10ms** - Set LDO1_VMON and LDO1_EN to '1' after 10ms

5.4.1.2.1.6 REG_WRITE_MASK_SREG Command

Table 5-20 shows the format of the REG_WRITE_MASK_SREG commands

Table 5-20. REG_WRITE_MASK_SREG Command Format

Bits[23:16]	Bits[15:14]	Bits[13:4]	Bits[3:0]
MASK	REG	ADDR	CMD
8 bits	2 bits	10 bits	4 bits

Description: Write the data from a scratch register, except the masked bits, to the specified register address

Fields:

- CMD: Command opcode (0x5)
- ADDR: Address of register to be written
- REG: Scratch register where the data will be copied from
- MASK: Mask used to select bits to be modified. Only bits with mask=0 are modified

Assembly command: **REG_WRITE_MASK_SREG [REG=]<Scratch Register> [ADDR=]<Address> [MASK=]<Mask>**

'REG=', 'ADDR=', and 'MASK=' are options. When included, the parameters can be in any order.

Scratch Register can be R0, R1, R2, or R3.

Address and Mask can be in any literal integer format (decimal, hex, etc.).

Examples:

- **REG_WRITE_MASK_SREG R2 0x22 0x00** - Write the content of scratch register 2 to address 0x22
- **REG_WRITE_MASK_SREG REG=R0 ADDR=0x054 MASK=0xF0** - Write the lower 4 bits of scratch register 0 to address 0x54

5.4.1.2.1.7 SREG_READ_REG Command

Table 5-21 shows the format of the SREG_READ_REG commands

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Table 5-21. SREG_READ_REG Command Format

Bits[15:14]	Bits[13:4]	Bits[3:0]
REG	ADDR	CMD
2 bits	10 bits	4 bits

Description: Write scratch register (REG0-3) with data from a specified address

Fields:

- CMD: Command opcode (0x6)
- ADDR: Address of register to be read
- REG: Destination scratch register where the read data will be placed

Assembly command: **SREG_READ_REG [REG=]<Scratch Register> [ADDR=]<Address>**

'REG=' and 'ADDR=' are options. When included, the parameters can be in any order.

Scratch Register can be R0, R1, R2, or R3.

Address can be in any literal integer format (decimal, hex, etc.).

Examples:

- **SREG_READ_REG R2 0x15** - Read the content of address 0x15 and write the data to scratch register 2
- **SREG_READ_REG ADDR=0x077 REG=R3** - Read the content of address 0x77 and write the data to scratch register 3

5.4.1.2.1.7.1 SREG_WRITE_IMM Command

Table 5-21 shows the format of the SREG_WRITE_IMM commands

Table 5-22. SREG_WRITE_IMM Command Format

Bits[13:6]	Bits[5:4]	Bits[3:0]
DATA	SREG	CMD
8 bits	2 bits	4 bits

Description: Write the specified data to the scratch register (REG0-3)

Fields:

- CMD: Command opcode (0xF)
- DATA: Data to be written to th scratch register
- SREG: Destination scratch register where the data will be written to

Assembly command: **SREG_WRITE_IMM [REG=]<Register> [DATA=]<Data>**

Data can be in any literal integer format (decimal, hex, etc.).

Register can be R0, R1, R2, or R3.

'REG=' and 'DATA=' are options. When included, the parameters can be in any order.

Examples:

- **SREG_WRITE_IMM R2 0x15** - Write 0x15 to scratch register 2
- **SREG_WRITE_IMM ADDR=0x077 REG=R3** - Read 0x77 to scratch register 3

5.4.1.2.1.8 WAIT Command

Table 5-23 shows the format of the WAIT commands

Table 5-23. WAIT Command Format

Bits[23:18]	Bits[17:12]	Bits[11:10]	Bits[9:4]	Bits[3:0]
SKIP_CNT	TIMEOUT	COND_TYPE	COND_SEL	CMD
6 bits	6 bits	2 bits	6 bits	4 bits

Description: Wait upon a condition of a given type. Execution is paused until the specified type of the condition is met or timed out

Fields:

- CMD: Command opcode (0x7)
- COND_SEL: Selects the condition list in below in Table 5-24
- COND_TYPE: Condition type to monitor - 0x0: LOW, 0x1: HIGH, 0x2: Rising Edge, 0x3: Falling Edge
- TIMEOUT: Maximum time to wait for the condition. This timeout represents a threshold count for a counter running a step size specified in register PFSM_DELAY_STEP
- SKIP_CNT: Number of consecutive instructions that will become NOOPs if timeout occurs

Assembly command: **WAIT [COND=]<Condition> [TYPE=]<Type> [TIMEOUT=]<Timeout> [DEST=]<Destination>**

Alternative assembly command: **JUMP [DEST=]<Destination>**

'COND=', 'TYPE=', 'TIMEOUT=', and 'DEST=' are options. When included, the parameters can be in any order.

Condition are listed in Table 5-24 . Examples: GPIO1, BUCK1_PG, I2C_1

Type = LOW, HIGH, RISE, or FALL

Timeout = timeout value in ns, µs, ms, or s. If there is no units, it must be an integer value between 0-63. Timeout value will be rounded to the nearest achievable time based on the current step size. Current step size will default to the NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler will report an error if the step size is too large or too small to meet the delay.

Destination = Label to jump to if when timeout occurs. Destination must be after the WAIT statement in memory.

Memory space can be either '0' or '1'. '0' indicates the destination address is in the PFSM memory space. '1' indicates the destination address is external and represents a FSM state ID.

When using the jump command, this will be an unconditional jump. The command will be compiled as "WAIT COND=63 TYPE=LOW TIMEOUT=0 DEST=<Destination>". Condition 63 is a hardcoded 1, so the condition is never satisfied and will always timeout. Therefore the command will always jump to the destination.

Examples:

- **WAIT GPIO4 RISE 1s <Destination> 0** - Wait to execute the command at the specified SRAM address when a rise edge is detected at GPIO4, or after 1 second
- **WAIT COND=BUCK1_PG TYPE=HIGH TIMEOUT=500us DEST=<mcu2act_seq>** - Wait to execute the commands at <mcu2act_seq> address as soon as BUCK1 output is within power_good range, or after 500 µs

Table 5-24. WAIT Command Conditions

COND_SEL	Condition Name	COND_SEL	Condition Name	COND_SEL	Condition Name	COND_SEL	Condition Name
0	GPIO1	16	LDO1_PG	32	I2C_0	48	LP_STANDBY_SEL
1	GPIO2	17	LDO2_PG	33	I2C_1	49	N/A
2	GPIO3	18	LDO3_PG	34	I2C_2	50	N/A

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Table 5-24. WAIT Command Conditions (continued)

COND_SEL	Condition Name	COND_SEL	Condition Name	COND_SEL	Condition Name	COND_SEL	Condition Name
3	GPIO4	19	LDO4_PG	35	I2C_3	51	N/A
4	GPIO5	20	PGOOD	36	I2C_4	52	N/A
5	GPIO6	21	TWARN_EVENT	37	I2C_5	53	N/A
6	GPIO7	22	INTERRUPT_PIN	38	I2C_6	54	N/A
7	GPIO8	23	N/A	39	I2C_7	55	N/A
8	GPIO9	24	N/A	40	SREG0	56	N/A
9	GPIO10	25	N/A	41	SREG1	57	N/A
10	GPIO11	26	N/A	42	SREG2	58	N/A
11	BUCK1_PG	27	N/A	43	SREG3	59	N/A
12	BUCK2_PG	28	N/A	44	SREG4	60	N/A
13	BUCK3_PG	29	N/A	45	SREG5	61	N/A
14	BUCK4_PG	30	N/A	46	SREG6	62	0
15	BUCK5_PG	31	N/A	47	SREG7	63	1

5.4.1.2.1.9 DELAY_IMM Command

Table 5-25 shows the format of the DELAY_IMM commands

Table 5-25. DELAY_IMM Command Format

Bits[11:4]	Bits[3:0]
DELAY	CMD
8 bits	4 bits

Description: Delay the execution by a specified time

Fields:

- CMD: Command opcode (0x8)
- DELAY: The delay time to wait before execution continues. The delay represents a threshold count for a counter running a step size specified in register PFSM_DELAY_STEP

Assembly command: **DELAY_IMM <Delay>**

Delay = delay time in ns, µs, ms, or s. If there is no units, it must be an integer value between 0-63. Delay value will be rounded to the nearest achievable time based on the current step size. Current step size will default to the NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler will report an error if the step size is too large or too small to meet the delay.

Examples:

- **DELAY_IMM 100us** - Delay execution by 100 µs
- **DELAY_IMM 10ms** - Delay execution by 10 ms
- **DELAY_IMM 8** - Delay execution by 8 ticks of the current PFSM time step

5.4.1.2.1.10 DELAY_SREG Command

Table 5-25 shows the format of the DELAY_SREG commands

Table 5-26. DELAY_SREG Command Format

Bits[5:4]	Bits[3:0]
REG	CMD
2 bits	4 bits

Description: Delay the execution by a time value stored in the specified scratch register

Fields:

- CMD: Command opcode (0x9)
- REG: The scratch register where the delay time is specified to wait before execution continues. The delay time represents a threshold count for a counter running a step size specified in register PFSM_DELAY_STEP

Assembly command: **DELAY_SREG <Register>**

Register can be R0, R1, R2, or R3.

Examples:

- **DELAY_SREG R0** - Delay execution by the time value stored in scratch register0

5.4.1.2.1.11 TRIG_SET Command

Table 5-27 shows the format of the TRIG_SET commands

Table 5-27. TRIG_SET Command Format

Bits[31:20]	Bit [19]	Bit[18]	Bit[17]	Bits[16:15]	Bits[14:9]	Bits[8:4]	Bits[3:0]
ADDR	REENTRANT	EXT	IMM	TRIG_TYPE	TRIG_SEL	TRIG_ID	CMD
12 bits	1 bit	1 bit	1 bit	2bits	6 bits	5 bits	4 bits

Description: Set a trigger destination address for a given input signal or condition. These commands must be defined at the beginning of PFSM configuration memory.

Fields:

- CMD: Command opcode (0xA)
- TRIG_ID: The ID of the hardware trigger module to be configured (Value range 0-27). They must be defined in numeric order based on the priority of the trigger.
- TRIG_SEL: Selection of the trigger signal to be associated with the TRIG_ID. Selections are listed in Table 5-28
- TRIG_TYPE: Trigger type to monitor - 0x0: LOW, 0x1: HIGH, 0x2: Rising Edge, 0x3: Falling Edge
- IMM: 0x0: Trigger is not activated until the END command of a given task, 0x1: Trigger is activated immediately and can abort a sequence
- REENTRANT: Permits a trigger to repeatedly execute active sequence. When EXT=1, this bit is used as bit 0 of the external FSM state. This bit must be 0 when IMM=1
- EXT: 0x0: Destination is an address in the PFSM memory space, 0x1: Destination is external and the address represents a FSM state ID
- ADDR: The destination address or state ID for the trigger event. The assembler will automatically create this address based upon labels

Assembly command: **TRIG_SET [DEST=]<Destination> [ID=]<Trig_ID> [SEL=]<Trig_sel> [TYPE=]<Trig_type> [IMM=]<IMM> [EXT=]<Memory space>**

'DEST=', 'ID=', 'SEL='. 'TYPE=', 'IMM=', and 'EXT=' are options. When included, the parameters can be in any order.

Destination is the label where this trigger should start executing

Trig_ID is the ID of the hardware trigger module to be configured (Value range 0-27). They must be defined in numeric order based on the priority of the trigger.

Trig_Sel is the "Trigger Name' from Table 5-28. This is the trigger signal to be associated with the specified TRIG_ID

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Trig_type = LOW, HIGH, RISE, or FALL

IMM can be either '0' or '1'. = '0' if the trigger is not activated until the END command of a given task; '1' if the trigger is activated immediately and can abort a sequence

REEMTRANT can be either '0' or '1'. '1' permits a trigger to repeatedly execute active sequence

Memory space can be either '0' or '1'. '0' indicates the destination address is in the PFSM memory space. '1' indicates the destination address is external and represents a FSM state ID.

Examples:

- **TRIG_SET seq1 20 GPIO_1 LOW 0 0** - Set trigger 20 to be GPIO_1=Low, not immediate. When triggered, start executing at ‘seq1’ label.
- **TRIG_SET DEST=seq2 ID=15 SEL=ESM_MCU_ERROR TYPE=RISE IMM=0 EXT=0**- Set trigger 15 to be rising ESM_MCU_ERROR trigger, not immediate. When triggered, start executing at ‘seq2’ label.

Table 5-28. PFSM Trigger Selections

TRIG_SEL	Trigger Name	TRIG_SEL	Trigger Name	TRIG_SEL	Trigger Name	TRIG_SEL	Trigger Name
0	IMMEDIATE_SHUTDOWN	16	C	32	I2C_0	48	LP_STANDBY_SEL
1	MCU_POWER_ERROR	17	D	33	I2C_1	49	N/A
2	ORDERLY_SHUTDOWN	18	SU_STANDBY	34	I2C_2	50	N/A
3	RESERVED	19	SU_X	35	I2C_3	51	N/A
4	FORCE_STANDBY	20	WAIT_TIMEOUT	36	I2C_4	52	N/A
5	FORCE_LP_STANDBY	21	GPIO1	37	I2C_5	53	N/A
6	ESM_MCU_ERROR	22	GPIO2	38	I2C_6	54	N/A
7	WD_ERROR	23	GPIO3	39	I2C_7	55	N/A
8	SOC_POWER_ERROR	24	GPIO4	40	SREG_0	56	N/A
9	ESM_SOC_ERROR	25	GPIO5	41	SREG_1	57	N/A
10	A	26	GPIO6	42	SREG_2	58	N/A
11	WKUP1	27	GPIO7	43	SREG_3	59	N/A
12	SU_ACTIVE	28	GPIO8	44	SREG_4	60	N/A
13	B	29	GPIO9	45	SREG_5	61	N/A
14	WKUP2	30	GPIO10	46	SREG_6	62	0
15	SU_MCU_ONLY	31	GPIO11	47	SREG_7	63	1

5.4.1.2.1.12 TRIG_MASK Command

Table 5-29 shows the format of the TRIG_MASK commands

Table 5-29. TRIG_MASK Command Format

Bits[31:28]	Bits[27:20]	Bits[19:12]	Bits[11:4]	Bits[3:0]
DATA4	DATA3	DATA2	DATA1	CMD
4 bits	8 bits	8 bits	8 bits	4 bits

Description: Sets a trigger mask that determines which triggers are active. Setting a ‘0’ enables the trigger, setting a ‘1’ disables (masks) the trigger.

Fields:

- CMD: Command opcode (0xB)
- DATA1: The mask for triggers 7-0
- DATA2: The mask for triggers 15-8
- DATA3: The mask for triggers 23-16

- DATA4: The mask for triggers 27-24

Assembly command: **TRIG_MASK <Mask value>**

Mask Value = 28-bit mask in any literal integer format (decimal, hex, etc.).

Examples:

- **TRIG_MASK 0x5FF82F0** - Set the trigger mask to 0x5FF82F0

5.4.1.2.1.13 END

Table 5-30 shows the format of the END commands

Table 5-30. END Command Format

Bit[3:0]
CMD
4 bits

Description: Marks the final instruction in a sequential task

Fields:

- CMD: Command opcode (0xC)

Assembly command: **END**

5.4.1.2.1.14 Configuration Memory Organization and Sequence Execution

The configuration memory is loaded from EEPROM into an SRAM. Figure 5-45shows an example configuration memory with only two configured sequences.

ADDRESS	CONTENT
1	Trigger Type (up to 11 triggers, 2 bits per trigger)
2	TRIG_MAP(trig_sel, start_addr, dest_state)
3	TRIG_MAP(trig_sel, start_addr, dest_state)
4	TRIG_MAP(trig_sel, start_addr, dest_state)
5	TRIG_MAP(trig_sel, start_addr, dest_state)
6	END(delay, seq_state)
7	
8	VR_WRITE(addr, data, delay, cond)
9	VR_WRITE(addr, data, delay, cond)
10	VR_WRITE(addr, data, delay, cond)
11	VR_WRITE(addr, data, delay, cond)
12	VR_WRITE(addr, data, delay, cond)
13	VR_WRITE(addr, data, delay, cond)
14	VR_WRITE(addr, data, delay, cond)
15	RR_WRITE(addr, data, mask)
16	TRIG_MAP(trig_sel, start_addr, dest_state)
17	TRIG_MAP(trig_sel, start_addr, dest_state)
18	END(delay, seq_state)
19	
20	VR_WRITE(addr, data, delay, cond)
21	VR_WRITE(addr, data, delay, cond)
22	VR_WRITE(addr, data, delay, cond)
23	VR_WRITE(addr, data, delay, cond)
24	VR_WRITE(addr, data, delay, cond)
25	VR_WRITE(addr, data, delay, cond)
26	VR_WRITE(addr, data, delay, cond)
27	RR_WRITE(addr, data, mask)
28	TRIG_MAP(trig_sel, start_addr, dest_state)
29	END(delay, seq_state)

The first address in the configuration memory is special. This address is used to define the trigger type of all 11 triggers. Defining the trigger type is a total of 22 bits, 2 bits per trigger. These bits define the active state of each trigger.

0h = active low (level sensitive)
1h = active high (level sensitive)
2h = active low (edge sensitive)
3h = active high (edge sensitive)

Figure 5-45. Configuration Memory Script Example [TO BE UPDATED]

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The actual memory organization can be modified later to optimize bit usage based on the SRAM options available.

As soon as the PMIC state reaches the mission states, it will start reading from the configuration memory until it hits the first END command. The contents in this first section would include the global trigger type selections, which is always stored in the first address of the configuration memory, as well as the first set of trigger configurations. The trigger configurations are read and mapped to an internal lookup table. The lookup table can be used to lookup the start address associated with each trigger (or start address associated with each valid DEST_STATE if a DEST_STATE is received from serial interface). From that point on the configured triggers control the sequencing.

If one of the triggers in the first set of trigger configurations is activated, then the execution engine looks up the starting address associated with that trigger and starts executing commands until it hits an END command. The last few commands before END will contain the new set of trigger configurations.

Again, the execution engine waits until any of the new triggers is activated, at which point it starts executing from the address associated with the activated trigger.

The above sequence of waiting for triggers and executing the sequence associated with an activated trigger is the normal operating condition of the execution engine when the main PMIC state machine is in ACTIVE/MISSION state. Any time an event occurs that requires a transition from ACTIVE/MISSION state of the PMIC to any of the other PMIC states, the PMIC state machine will take over control from the execution engine. But any sequencing required for IMMEDIATE_SHUTDOWN, ORDERLY_SHUTDOWN or SAFE states will be determined from what is configured in configuration memory using the TRIG_MAP command (see details of the TRIG_MAP command)

The internal lookup table created from the TRIG_MAP commands is cleared out as soon as a trigger (or DEST_STATE from serial interface) is received that starts a sequence. The table is re-populated at the end of the sequence through new set of TRIG_MAP commands at the end of each sequence. Essentially the lookup table cleared out at the beginning of each sequence and is re-populated at the end of each sequence.

5.4.1.2.2 State Transition Requests

5.4.1.2.2.1 ON Requests

ON requests are used to switch on the device, which transitions the device from the STANDBY or the LP_STANDBY to the state specified by STARTUP_DEST[1:0].

After the device arrives the corresponding STARTUP_DEST[1:0] operation state, the MCU must setup the NSLEEP1 and NSLEEP2 signals accordingly before clearing the STARTUP_INT interrupt. Once the interrupt is cleared, the device will stay or move to the next state corresponding to the NSLEEP signals state assignment as specified in Table 5-34.

Table 5-31 lists the available ON requests.

Table 5-31. ON Requests

EVENT	MASKABLE	COMMENT	DEBOUNCE
nPWRON (pin)	Yes	Edge sensitive	50 ms
ENABLE (pin)	Yes	Level sensitive	8 µs
First Supply Detection (FSD)	Yes	VCCA > VCCA_UV and FSD unmasked	N/A
RTC ALARM Interrupt	Yes		N/A
RTC TIMER Interrupt	Yes		N/A
WKUP1 or WKUP2 Detection	Yes	Edge sensitive	8 µs
LP_WKUP1 or LP_WKUP2 Detection	Yes	Edge sensitive	N/A

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Table 5-31. ON Requests (continued)

EVENT	MASKABLE	COMMENT	DEBOUNCE
Recovery from Immediate and Orderly Shutdown	Yes	Recover from system errors which caused immediate or orderly shut down of the device	N/A

If one of the events listed in Table 5-31 occurs, the event powers on the device unless one of the gating conditions listed in Table 5-32 is present.

Table 5-32. ON Requests Gating Conditions

EVENT	MASKABLE	COMMENT
VCCA_OVP (event)	No	VCCA_SENSE > VCCA_OVP, VSYS_DEAD_LOCK_EN = 1
VCCA_UVLO (event)	No	VCCA < VCCA_UVLO
VINT_OVP (event)	No	LDOVINT > 1.98 V
VINT_UVLO (event)	No	LDOVINT < 1.62 V
TSD and TWARN (event)	No	Device temperature exceeds the Thermal Warning level

The NPWRON_SEL NVM register bit determines whether the nPWRON/ENABLE pin should be treated as a power on press button or a level sensitive enable switch. When this pin is configured as the nPWRON button, a short button press detection will be latched internally as a device enable signal until the NPWRON_START_INT is cleared, or a long press key event is detected. The short button press detection occurs when an falling edge is detected at the nPWRON pin.

When the pin is configured as an ENABLE pin, it is a level sensitive pin, and an assertion will enable the device until the pin is released.

5.4.1.2.2.2 OFF Requests

OFF request is used to orderly switch off the device. OFF requests initiate transition from any other mission state to the STANDBY state or the LP_STANDBY state depending on the setting of the LP_STANDBY_SEL bit.Table 5-33 lists the conditions to generate the OFF requests and the corresponding destination state.

Table 5-33. OFF Requests

EVENT	DEBOUNCE	LP_STANDBY_SEL bit setting	Destination State
nPWRON (pin) (long press key event)	8 s	LP_STANDBY_SEL = 0	STANDBY
		LP_STANDBY_SEL = 1	LP_STANDBY
ENABLE (pin)	8 µs	LP_STANDBY_SEL = 0	STANDBY
		LP_STANDBY_SEL = 1	LP_STANDBY
I2C_TRIGGER_0	NA	LP_STANDBY_SEL = 0	STANDBY
		LP_STANDBY_SEL = 1	LP_STANDBY

The long press key event occurs when the nPWRON pin stays low for longer than t_{LPK_TIME} while the device is in a mission state.

5.4.1.2.2.2.1 NSLEEP1 and NSLEEP2 Functions

The SLEEP requests are activated through the assertion of nSLEEP1 or nSLEEP2 pins, which are the secondary functions of the 11 GPIO pins and can be selected through GPIO configuration using the GPIOx_SEL register bits. If the nSLEEP1 or nSLEEP2 pins are not available, the NSLEEP1B and NSLEEP2B register bits can be configured in place for their functions. The input of nSLEEP1 pin and the state of the NSLEEP1B register bit are combined to create the NSLEEP1 signal through an "OR" function. Similarly for the input of the nSLEEP2 pin and the NSLEEP2B register bit as they are combined to create the NSLEEP2 signal.

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A 1 → 0 logic level transition of the NSLEEP signal generates a sleep request, while a 0 → 1 logic level transition reverses the sleep request. When a NSLEEPn signal transitions from 1 → 0, it generates a sleep request to go from a higher power state to a lower power state. When the signal transitions from 0 → 1, it reverses the sleep request and returns the device to the higher power state.

The NSLEEPn_MASK bit can be used to mask the sleep request associated with the corresponding NSLEEPn signal. When the NSLEEPn_MASK = 1, the corresponding NSLEEPn signal will be ignored. The combination of the NSLEEPn signals and NSLEEPn_MASK bits creates triggers A/B/C/D to the FSM to control the power state of the device as shown in Table 5-34.

The states of the resources during ACTIVE, SLEEP, and DEEP SLEEP/S2R states are defined in the LDOn_CTRL and BUCKn_CTRL registers. For each resource, a transition to the MCU ONLY or the DEEP SLEEP/S2R states is controlled by the FSM when the resource is associated to the SLEEP or DEEP SLEEP/S2R states.

Table 5-34 shows the corresponding state assignment based on the state of the NSLEEPn and their corresponding mask signals.

Table 5-34. NSLEEPn Transitions and Mission State Assignments

Current State	NSLEEP1	NSLEEP2	NSLEEP1 MASK	NSLEEP2 MASK	Trigger to FSM	Next State
DEEP SLEEP/S2R	0	0 → 1	0	0	TRIGGER B	MCU ONLY
DEEP SLEEP/S2R	0 → 1	0 → 1	0	0	TRIGGER A	ACTIVE
DEEP SLEEP/S2R	Don't care	0 → 1	1	0	TRIGGER A	ACTIVE
DEEP SLEEP/S2R or MCU ONLY	0 → 1	Don't care	0	1	TRIGGER A	ACTIVE
MCU ONLY	0 → 1	1	0	0	TRIGGER A	ACTIVE
MCU ONLY	0	1 → 0	0	0	TRIGGER D	DEEP SLEEP or S2R
MCU ONLY	Don't care	1 → 0	1	0	TRIGGER D	DEEP SLEEP or S2R
ACTIVE	1 → 0	1	0	0	TRIGGER B	MCU ONLY
ACTIVE	1 → 0	1 → 0	0	0	TRIGGER D	DEEP SLEEP or S2R
ACTIVE	Don't care	1 → 0	1	0	TRIGGER D	DEEP SLEEP or S2R
ACTIVE	1 → 0	Don't care	0	1	TRIGGER B	MCU ONLY

5.4.1.2.2.2 WKUP1 and WKUP2 Functions

The WKUP1 and WKUP2 functions are activated through the edge detection of all GPIO pins. Any one of these GPIO pins when configured as an input pin can be configured to wake up the device by setting GPIOn_SEL bit to select the WKUP1 or WKUP2 functions. When a GPIO pin is configured as a WKUP1 pin, a rising or falling edge detected at the input of this pin (configurable by the GPIOn_FALL_MASK and the GPIOn_RISE_MASK bits) will wake up the device to the ACTIVE state. Likewise if a GPIO pin is configured as a WKUP2 pin, an detected edge will wake up the device to the MCU ONLY state. If multiple edge detections of WKUP signals occur simultaneous, the device will go to the state in the following priority order:

1. ACTIVE
2. MCU ONLY

When a valid edge is detected at a WKUP pin, an interrupt will be generated by the nINT pin to signal the MCU of the wake-up event, and the GPIOx_INT interrupt bit will be set. The wake request will remain active until the GPIOx_INT bit is cleared by the MCU. While the wake request is executing, the device will ignore any sleep request to go to a lower power state until the corresponding GPIOx_INT interrupt bit is cleared to deactivate the wake request. After the wake request is deactivated, the device will return to the state indicated by the NSLEEP1 and NSLEEP2 signals as shown in Table 5-34

5.4.1.2.2.2.3 LP_WKUP Pins for Waking Up from LP STANDBY

The LP_WKUP functions are activated through the edge detection of LP_WKUP pins, configurable as secondary functions of GPIO3 and GPIO4. They are specially designed to wake the device up from the LP STANDBY state when a high speed wake up signal is detected. Similar to the WKUP1 and WKUP2 pins, when GPIO3 or GPIO4 pin is configured as a LP_WKUP1 pin, an rising or falling edge detected at the input of this pin (configurable by the GPIOn_FALL_MASK and the GPIOn_RISE_MASK bits) will wake up the device to the ACTIVE state. Likewise if the pin is configured as a LP_WKUP2 pin, a detected edge will wake up the device to the MCU ONLY state. If multiple edge detections of LP_WKUP signals occur simultaneous, the device will go to the state in the following priority order:

1. ACTIVE
2. MCU ONLY

The TPS6594-Q1 device supports limited CAN Wake-up capability through the LP_WKUP1/2 pins. When an input signal (without deglitch) with logic level transition from high-to-low or low-to-high with a minimum pulse width of $t_{WK\_PW\_MIN}$ is detection on the assigned LP_WKUP1/2 pins, the device will wake up asynchronously and execute the power up sequence. CAN-transceiver RXD- or INH-outputs can be connected to the LP_WKUP pin. If RXD-output is used it is assumed the transceiver RXD-pin IO is powered by the transceiver itself from an external supply when TPS6594-Q1 is in LP_STANDBY state. If INH-signal is used it has to be scaled down to recommenced GPIO input voltage level specified in the electrical characteristics table.

The device can wake up from the LP_STANDBY state through the detection of LP_WKUP pins only if it enters the LP_STANDBY state by writing to the TRIGGER_I2C0 bit. Once a valid wake-up signal is detected at the LP_WKUP pin, it is handled as a WAKE request. An interrupt will be generated by the nINT pin to signal the MCU of the wake-up event, and the corresponding GPIOx_INT interrupt bit will be set. The wake request will remain active until the interrupt bit is cleared by the MCU.

Figure 5-46 illustrates the valid wake-up signal at the LP_WKUP1/2 pins, and the generation and clearing of the internal wake-up signal.

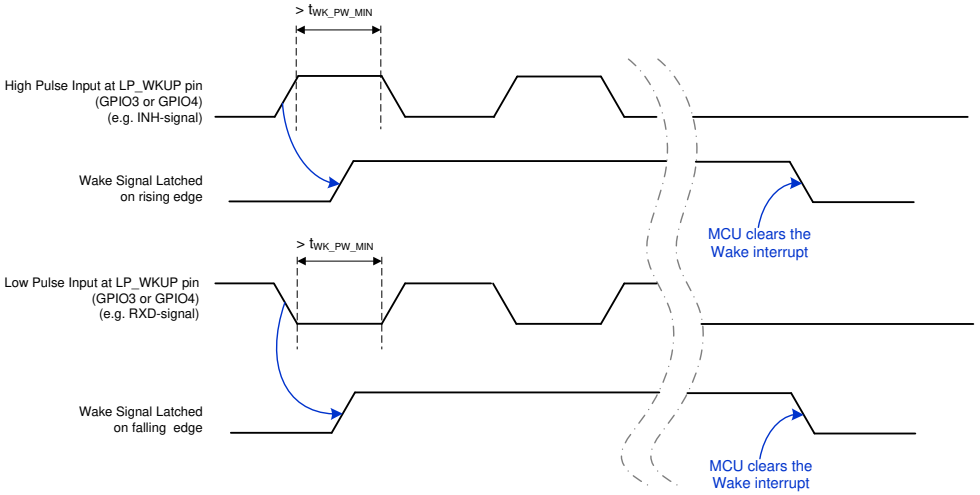

Figure 5-46. CAN Wake-up Timing Diagram

5.4.1.3 Error Handling Operations

The FSM engine of the TPS6594-Q1 device is designed to handle the following types of errors throughout the operation:

- Power Rail Output Error
- Boot BIST Error
- Runtime BIST Error

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- Catastrophic Error
- Watchdog Error
- Error Signal Monitor (ESM) Error
- Warnings

5.4.1.3.1 Power Rail Output Error

Power rail output error occurs when error condition is detected from the output rails of the device which are used to power the attached MCU or SoC. These errors includes rails not reaching or maintaining within the power good voltage level threshold, a short condition is detected at a regulator output, or the load current has exceeded the forward current limit.

The BUCKn_GRP_SEL, LDOn_GRP_SEL, and VCCA_GRP_SEL registers are used to configure the rail group for all of the Bucks and LDOs, as well as the voltage monitors which are available for external rails. The selectable rail groups are MCU rail group, SoC rail group, or other rail group. The TPS6594-Q1 device is designed to react differently when an error is detected from a power resource assigned to the different rail groups.

The SOC_RAIL_TRIG[1:0], MCU_RAIL_TRIG[1:0], and OTHER_RAIL_TRIG[1:0] registers are used as the "Immediate Shutdown Trigger Mask", "Orderly Shutdown Trigger Mask", "MCU Power Error Trigger Mask", or the "SoC Power Error Trigger Mask" shown in Figure 5-44. The settings of these register bits determine the error handling sequence which the assigned groups of rails should take in an event of output error. The PFSM engine can be configure to execute the appropriate error handling sequence to be taken for the following error handling sequence options: "immediate shutdown", "orderly shutdown", "MCU power error", or "SOC power error". For example, if an "immediate shutdown" sequence is assigned to the MCU rail group through the MCU_RAIL_TRIG[1:0], any failure detected in this group of rails will cause the device to execute the immediate shutdown sequence and enter the SAFE RECOVERY state. The device will immediately reset both the attached MCU and SoC by de-asserting the nRSTOUT and nRSTOUT_SoC (GPO1) pins. All of the power resources assigned to both the MCU and the SOC will be shutdown immediately without sequencing order. The EN_DRV pin will be forced low, and the nINT pin will signal a MCU_PWR_ERR_INT interrupt event has occurred. If the error is recoverable within the recovery time interval, the device will increment the recovery count, return to INIT state and re-attempt the power up sequence if the recovery count has not exceeded the counter threshold. If the recovery count was already exceeded the threshold, the device will stay in the SAFE RECOVERY state until VCCA voltage is below the VCCA_UVLO threshold and the device is power cycled.

The power resource assigned to the SoC rail group are typically assigned to the SOC power error handling sequence. When a power resource in this group is detected, the PFSM will typically cause the device to execute the shutdown of all the resources assigned to the SoC rail group, and the device will enter the MCU ONLY state. The device will immediately reset the attached SoC by toggling the nRSTOUT_SoC (GPO1) pins. The reset output to the MCU and the resources assigned to the MCU rail group will remain unchanged. The EN_DRV pin will also remain unchanged, and the nINT pin will signal a SOC_PWR_ERR_INT interrupt event has occurred.

5.4.1.3.2 Boot BIST Error

Boot BIST error occurs when the device is not able to pass the BOOT BIST during device power up. Every failure of the BOOT BIST attemp will cause the recovery count to increment as the device enters the SAFE RECOVERY state. If the count value has not exceeded the counter threshold, the device will attempt to enter the INIT state again and re-attempt the BOOT BIST until the recovery count reaches the maximum threshold. When this occurs the device will stay in SAFE RECOVERY state until VCCA voltage is below the VCCA_UVLO threshold and the device is power cycled.

5.4.1.3.3 Runtime BIST Error

Runtime BIST error occurs when the device is not able to pass the Runtime BIST while the device is in an operation state. This error creates an immediate shutdown condition, which will cause the device to execute the immediate shutdown sequence and enter the SAFE RECOVERY state. The device will immediately reset both the attached MCU and SoC by de-asserting the nRSTOUT and nRSTOUT_SoC (GPO1 or GPIO11)) pins. All of the power resources assigned to both the MCU and the SOC will be immediately shutdown. The EN_DRV pin will be forced low, and the nINT pin will be de-asserted to signal an interrupt event has occurred.

5.4.1.3.4 Catastrophic Error

Catastrophic errors are errors that affect multiple power resources such as errors detected in supply voltage, LDOVINT supply for control logic, clocks monitors, as well as device temperature passing the thermal shutdown threshold, or error detected in the SPMI communication network. These error creates an immediate or orderly shutdown condition, which will cause the device to execute the immediate or orderly shutdown sequence and enter the SAFE RECOVERY state. The device will reset both the attached MCU and SoC by de-asserting the nRSTOUT and nRSTOUT_SoC (GPO1 or GPIO11) pins. All of the power resources assigned to both the MCU and the SOC will be shutdown. The EN_DRV pin will be forced low, and the nINT pin will be de-asserted to signal an interrupt event has occurred.

5.4.1.3.5 Watchdog (WDOG) Error

Watchdog (WDOG) errors detection mechanisms are described in detail under 节 5.3.10.

5.4.1.3.6 Error Signal Monitor (ESM) Error

There are two Error Signal Monitors (ESM) available for the TPS6594-Q1 device, one designed to detect and handle the error signals received from the attached SoC, while the other one for the attached MCU. The error detection mechanisms for both monitors are described in detail under 节 5.3.11.

5.4.1.3.7 Warnings

Warning are non-catastrophic errors. When such an error occurs while the device is in the operating states, the device detects the error and handles the error through the interrupt handler. These are errors such as thermal warnings, I2C, or SPI communication errors, or power resource over current limit detection while the output voltage still maintains within the power good threshold. When these errors occur, the PFSM will pull the nINT pin low to signal an interrupt event has occurred. The device will remain in the operation state and no changes will be applied to the power resources, the reset outputs, nor the state of the EN_DRV pin.

5.4.1.4 Device Startup Timing

Figure 5-47 shows the timing diagram of the TPS6594-Q1 after the first supply detection.

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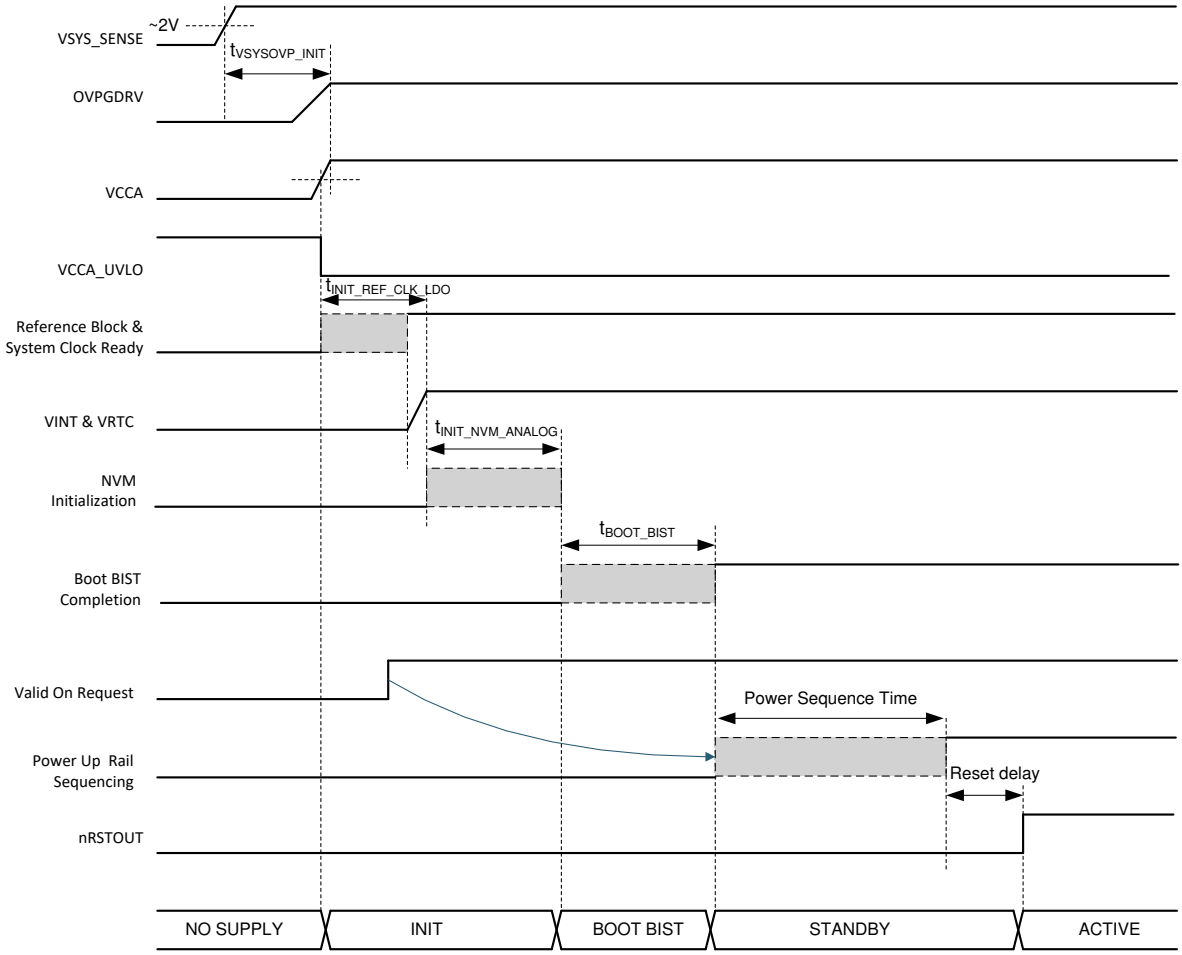

Figure 5-47. Device Startup Timing Diagram

$t_{VSYSOVP\_INIT}$ is the time between VSYS detection and when the VSYS Over Voltage Protection Module is in operation and the external protection FET connects the VSYS_SENSE to VCCA and the PVINx pins.

$t_{SU\_REFCLK\_LDO}$ is the start up time for the reference block. $t_{INIT\_NVM\_ANALOG}$ is the time for the device to load the default values of the NVM configurable registers from the NVM memory, and the start up time for the analog circuits in the device. Both t_{SU_REF} and $t_{INIT\_NVM\_ANALOG}$ are defined in the electrical characterization table.

t_{BOOT_BIST} is the sum of $t_{ABISTrun}$ and $t_{LBISTrun}$, which are defined in the electrical characterization tables.

The Power Sequence time is the total time for the device to complete the power up sequence. Please refer to Section 5.4.1.5 for more detail.

The Reset delay time is a configurable wait time for the nRSTOUT and the nRSTOUT_SoC release after the power up sequence is completed.

5.4.1.5 Power Sequences

A power sequence is an automatic preconfigured sequence the TPS6594-Q1 device configures its resources, which include the states of the BUCKs, LDOs, 32-kHz clock, and part of the GPIOs (REGENn signals). For a detailed description of the GPIOs signals, please refer to 节 5.3.7.

Figure 5-48 shows an example of a power up transition followed by a power down transition. The power up sequence is triggered through a valid on request, and the power down sequence is trigger by a valid off request. The resources controlled (for this example) are: BUCK3, LDO1, BUCK2, LDO2, REGEN1, LDO4, and LDO3. The time between each resource enable and disable (TinstX) is also part of the preconfigured sequence definition.

When a resource is not assigned to any power sequence, it remains in off mode. The user (through software) can enable and configure this resource independently when the power sequence completes.

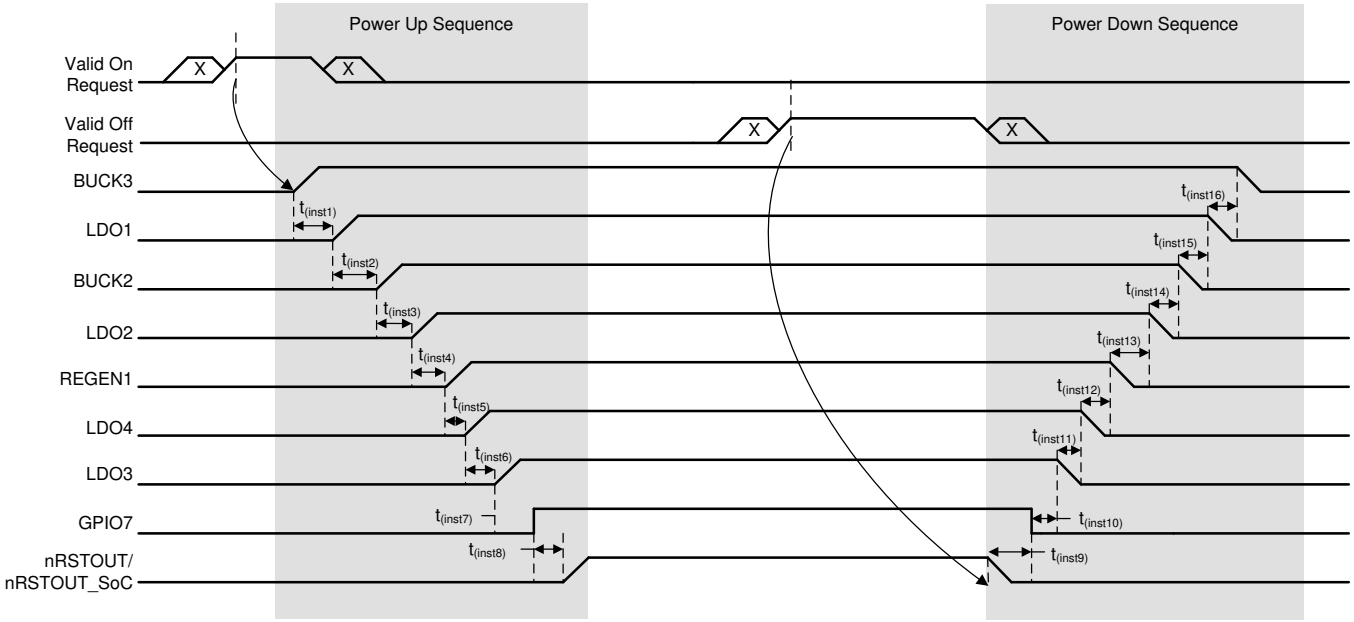

Figure 5-48. Power Sequence Example

As the power sequences of the TPS6594-Q1 device are defined according to the processor requirements, the total time for the completion of the power sequence will vary across various system definitions.

5.4.1.6 First Supply Detection

TheTPS6594-Q1 device can be configured to automatic start up from a first supply-detection (FSD) event detection. This feature is enabled by setting the FSD_MASK register bit to '0', and setting the NPWRON_SEL[1:0] registers bits to '10' or '11' to mask the functionality of nPWRON/ENABLE pin.

When the FSD feature is enabled, the PMIC powers up to an operation state automatically from the NO SUPPLY state to the destination state configured by STARTUP_DEST[1:0] bits when VCCA > VCCA_UV.

After the device arrives the corresponding STARTUP_DEST[1:0] operation state, the MCU must setup the NSLEEP1 and NSLEEP2 signals accordingly before clearing the FSD_INT interrupt. Once the interrupt is cleared, the device will stay or move to the destination state according to the state of the NSLEEP1/2 signals as specified in Table 5-34.

The FSD feature is managed through the configuration of an NVM register, which can be overwritten through I2C/SPI configuration after the device is in operation. When the device is power up from the NO SUPPLY state, the FSD detection is validated after the NVM default for this feature is loaded into the device memory.

5.4.1.7 Register Power Domains and Reset Levels

The TPS6594-Q1 registers are defined by the following categories:

- LDOVINT registers
- LDOVRTC registers

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LDOVINT registers The LDOVINT registers are powered by the internal LDOVINT, and retains their values until the devices enters LP_STANDBY state or the BACKUP state after the device was fully powered up and in operation. When this occurs LDOVINT is powered off, and the content of all LDOVINT registers will be lost, including the VSET registers which stores the default output voltage levels for all of the external power rails. As the device re-enters the INIT state from a wake up signal or an On-request, the registers powered by the LDOVINT will be re-written with the default values. All registers in the device except the LDOVRTC registers are powered by LDOVINT.

LDOVRTC registers The LDOVRTC registers retains their values until a Power-On-Reset (POR) occurs. POR occurs when the device lost supply power and enters the NO SUPPLY state. When this occurs LDOVRTC is powered off, and the content of all LDOVRTC registers will be lost.

Following are the LDOVRTC registers:

- All RTC registers
- RTC and Crystal Oscillator bypass bits
- Status registers for the following events: TSD and RTC reset
- Control registers for PWRON/ENABLE, GPIO3, and GPIO4 pins (for wake signal monitor during LP_STANDBY state)
- Following interrupt registers:
  - FSD_INT
  - RECOV_CNT_INT
  - TSD_ORD_INT
  - TSD_IMM_INT
  - PFSM_ERR_INT
  - VCCA_OVP_INT
  - ESM_MCU_RST_INT
  - ESM_SOC_RST_INT
  - WD_RST_INT
  - WD_LONGWIN_TIMEOUT_INT
  - NPWRON_LONG_INT

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5.4.2 Multi-PMIC Synchronization

A multi-PMIC synchronization scheme is implemented in the TPS6594-Q1 device to synchronize the power state changes with external PMIC devices. This feature consolidates and simplifies the IO control signals required between the application processor or the micro controller and multiple PMICs in the system. The control interface consists of an SPMI protocol which communicates the next power state information from the TPS6594-Q1 device to up to 5 slave PMICs, and receives feedback signal from the slave PMICs to indicate any error condition. Figure 5-49 is the block diagram of the power state synchronisation scheme. The TPS6594-Q1 is represented as the primary PMIC in this block diagram, which is responsible for broadcasting the synchronous system power state data, and processing the error feedback signals from the slave PMICs. It is the master device in the SPMI interface bus.

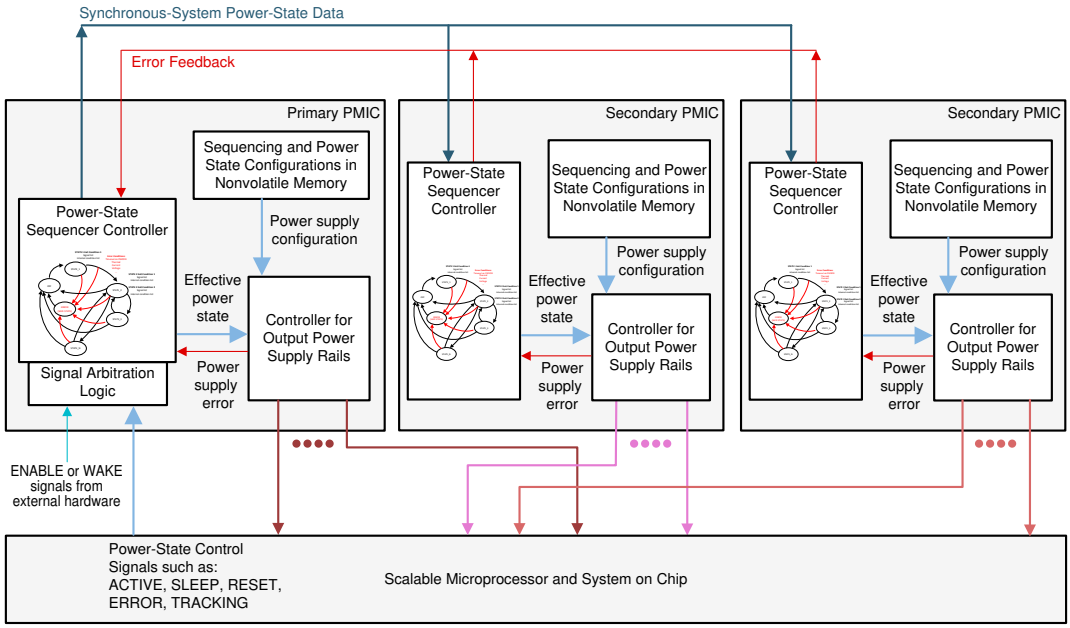

Figure 5-49. Multi-PMIC Power State Synchronization Block Diagram

In this scheme each primary and secondary PMIC runs on its on system clock, and maintains it's own I2C register set. Each PMIC will monitor it's own activities and pull down the open-drain output of nINT or PGOOD pin when errors are detected. The microprocessor will need to read the status bits on each PMIC device to find out the source of error being reported.

To synchronize the timing when entering and exiting from the LP_STANDBY state, the VOUT_LDOVINT of the TPS6594-Q1 device must be connected to the ENABLE input of the secondary PMICs, which are the slave devices in the SPMI interface bus. Figure 5-50 illustrates the pin connections between the primary, the secondary, and the application processor or the System on Chip.

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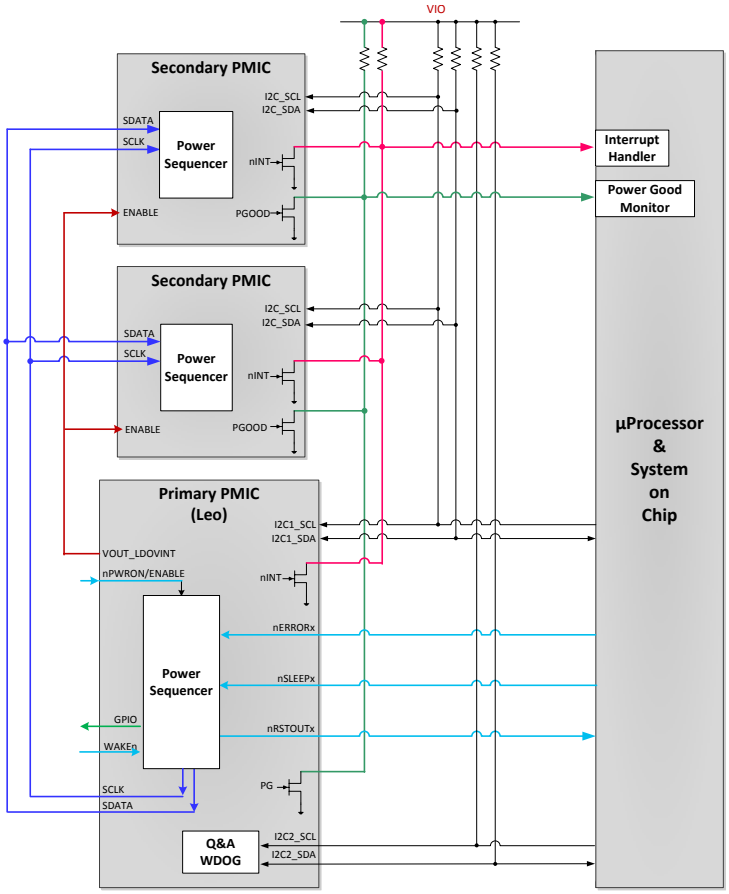

Figure 5-50. Multi-PIMC Pin Connections

The power sequencer of the multiple PMICs are synchronized at the beginning of each power up and power down sequence. However, due to the +/- 5% clock accuracy of the independent system clocks on the primary and secondary PMICs, a variation in the sequence timing is still possible. The worst case sequence timing variation from different PMIC rails is up to +/- 10% of the target delay time. Figure 5-51 illustrates the creation of this timing variation between PMICs.

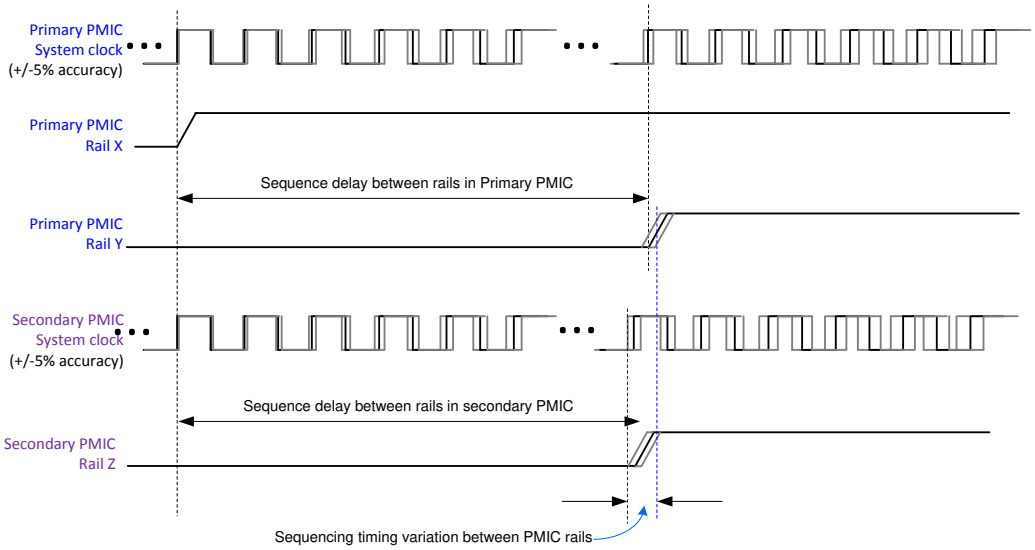

Figure 5-51. Multi-PMIC Rail Sequencing Timing Variation

5.4.2.1 SPMI Interface System Setup

An SPMI interface in the TPS6594-Q1 device is utilized to communicate the power state transition across multiple PMICs in the system. The interface block contains a SPMI master block and a SPMI slave block. There is only one SPMI master device in any given system. The TPS6594-Q1 device is generally the SPMI master in the system with both master and slave blocks enabled. As the SPMI master it initiates SPMI interface BIST and executes periodic checking of the SPMI bus health.

The SPMI master ID (MID) of the TPS6594-Q1 device is 1. TPS6594-Q1 will also contain a logical SPMI slave interface in order to receive SPMI communications from the SPMI slave devices. The TPS6594-Q1 as the SPMI master device will contain the logical (SID) = 0101.

All of the slave devices on this SPMI network will only have the slave interface enabled. There cannot be more than 5 slave devices in the system. The SIDs for the five slave devices are:

- 1st slave device: 0011
- 2nd slave device: 1100
- 3rd slave device: 1001
- 4th slave device: 0110
- 5th slave device: 1010

All devices in the SPMI network will listen to Group Slave ID (GSID): 1111. This address is used to communicate all power state transition information in broadcast mode to all connected devices in parallel.

5.4.2.2 Transmission Protocol and CRC

The communication between the devices on the network utilizes Extended Register Write command to GSID address “1111” with byte length of 2. Sequence format complies with MIPI SPMI 2.0 specification. First data frame carries the data payload of 5 bits and 3 filler bits.

Communication over the SPMI interface may contain information regarding the power state transition of the slave device with the NVM ID during the periodic testing for the SPMI bus. In the case of power state information the data payload contains 5 bits of Trigger ID information and 3 additional '0' bits. In the case of NVM ID information all 8 bits contain the NVM ID of the slave device.

Second data frame carries 8 bits of CRC information. CRC polynomial used is $X^8 + X^2 + X + 1$. CRC is calculated over the SPMI command frame, the address frame and the first data frame which contains the payload, excluding the parity bits in these three frames.

Figure 5-52 shows the data format of the SPMI Extended Register Write Command.

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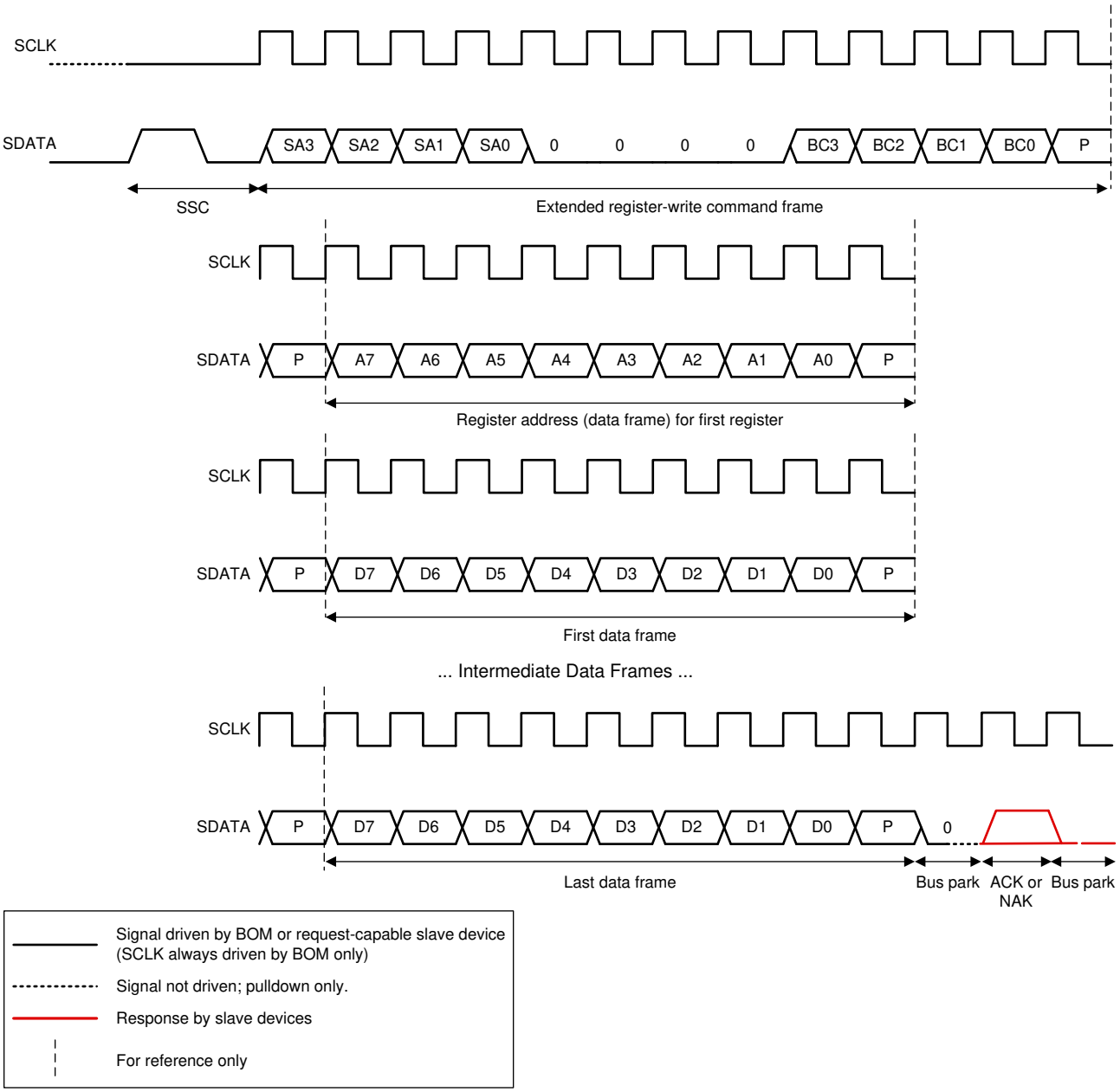

Figure 5-52. SPMI Extended Register Write Command

5.4.2.2.1 Operation with Transmission Errors

If the receiving device detects a parity or CRC error in the incoming sequence it will respond with negative ACK/NACK per SPMI standard.

If the transmitting device sees NACK response, it will try to resend the message as many times as indicated by SPMI_RETRY_LIMIT register bits. After that it will consider SPMI bus inoperable, sets SPMI_ERR_INT interrupt and goes to the safe recovery state and executes an orderly shutdown. Bus arbitration requests do not count as failed attempts if a slave device loses bus arbitration. SPMI_RETRY_LIMIT counter will be reset after each successful transmission by the device.

If a slave device has determined that SPMI does not work reliably it will not respond to any SPMI commands anymore until power-on-reset event has occurred. This is to prevent continued operation in a situation where SPMI is unreliable. This will force the TPS6594-Q1 device to detect a missing secondary device on the network during the periodic testing of SPMI bus. The slave device will then internally handle the SPMI error condition per error handling rules set for the device (in general executing an orderly shutdown). SPMI block signals to the device that SPMI bus error has occurred after the retry limit has been exceeded.

5.4.2.2.2 Transmitted Information

SPMI bus will be used to carry two types of information:

- PFSM Trigger ID between the SPMI master and slave devices
- NVM ID from SPMI slave devices to SPMI master device

The SPMI master device reads the NVM ID of the slave devices periodically to check the health of the interface. Exchanging Trigger IDs for the power state transition is sufficient to keep the PFSMs of all the devices on the SPMI network in synchronization. Notifications which do not cause power state transitions are still communicated to the rest of the system via interrupts, not via SPMI.

5.4.2.3 SPMI Slave Communication to SPMI Master

An SPMI slave device communicates to the SPMI master device and any other SPMI slave devices only if there is an internal error which is not SPMI related. The slave device initiates the error communication using Slave Arbitration Request with A-bit as defined in the SPMI 2.0 specification. SPMI 2.0 protocol manages the situation with multiple slave devices requesting error communication at the same time. This is resolved using the slave arbitration process as described in SPMI 2.0 specification. Once the SPMI slave device wins the Slave Arbitration using A-bit protocol it will perform Extended Register Write command to Group Slave ID address “1111” with using the protocol described earlier in this document for communicating PFSM trigger ID.

5.4.2.3.1 Incomplete Communication from SPMI Slave to SPMI Master

In case the TPS6594-Q1 device as the SPMI master detects Slave Arbitration Request on the SPMI interface, but the received sequence has an error or is incomplete, it will immediately perform SPMI interface BIST. If this fails, SPMI master will execute error handling for the SPMI error. If the SPMI interface BIST is successfully executed, TPS6594-Q1 will resume normal operation.

5.4.2.4 SPMI BIST Overview

The BIST operation is implemented both during BIST state and regularly during runtime operation. Figure 5-53 below illustrates how SPMI BIST operates during device power-up.

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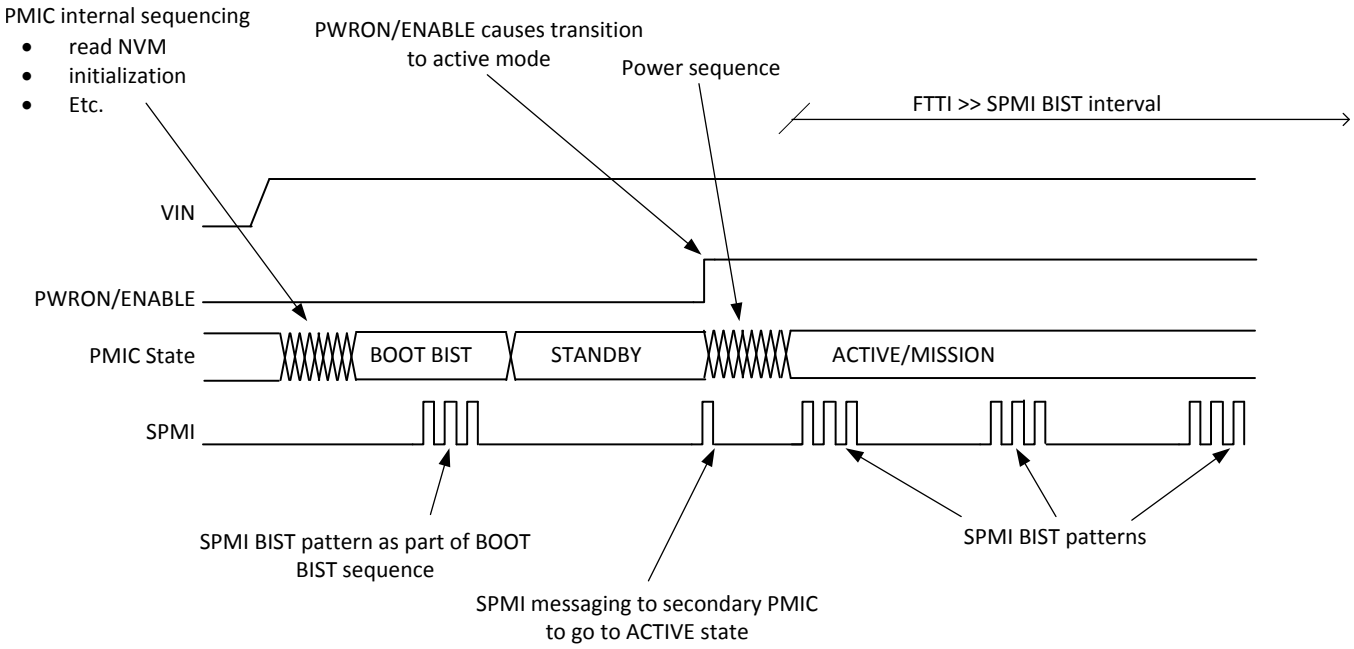

Figure 5-53. SPMI BIST Operation

After input power is detected and verified to be at the correct level, TPS6594-Q1 will initialize itself by reading NVM and performing any actions needed to prepare for operation. TPS6594-Q1 will then enter BOOT BIST state in which internal logic will sequence a series of tests to verify TPS6594-Q1 and the system are OK. As part of this test the SPMI interface BIST is performed. After it is successfully completed the device goes to standby state and wait further signals from the system to initiate the power-up sequence of the processor.

A valid on request initiates the processor power-up sequence. TPS6594-Q1 as the SPMI master will communicate this event via SPMI to all of the slave devices in the system. The power-up sequence will then be executed and TPS6594-Q1 will then enter the active state or any mission states.

5.4.2.4.1 SPMI Bus Boot BIST

Boot BIST will include both LBIST of the SPMI logic and an interface BIST. LBIST is performed first before the interface BIST during BOOT BIST or RUNTIME BIST. Interface BIST is implemented by reading NVM ID from each slave device into the TPS6594-Q1 device, and comparing this against reference values stored in the NVM memory. This ensures that

- All slave device(s) are present in the system as expected
- Each slave device has the right NVM settings
- The SPMI logic blocks are working on the master and all of the slave devices
- The pins and wires on the ICs and PCB are in working order

The SPMI interface BIST is initiated by the SPMI master device by writing a request to the slave devices (using GSID) requesting the slave devices to send their NVM IDs to the master device. Upon receiving this command from SPMI master the slave devices will request SPMI bus arbitration using SR-bit protocol; and upon winning the bus arbitration the slave devices will transmit their NVM ID into the logical slave of the SPMI master device.

The TPS6594-Q1 device contains a list of all SPMI slave devices on the SPMI bus and their NVM IDs in the register set. As the master device TPS6594-Q1 will read the NVM_ID register in each SID and compare the result with the stored NVM ID for the corresponding slave ID. The master device has to ensure that every non-zero slave NVM ID on its list is returned. This is important for use cases where there are two or more identical slave devices in the system. In these cases it is mandatory that correct number of the same NVM ID is returned. If no identical devices are to be used, then return of the same NVM ID multiple times is an error due to incorrect assembly of identical devices onto the PCB. An all-zero NVM ID stored in the register indicates the slave device is not present in the system.

Table 5-35 is the look-up table of corresponding slave ID for each NVM ID.

Table 5-35. SPMI SLAVE NVM ID Register Address and Corresponding Slave ID

REGISTER NAME	REGISTER ADRESS	SID of SLAVE DEVICE
SLAVE_NVM_ID_1	0x118	0011
SLAVE_NVM_ID_2	0x119	1100
SLAVE_NVM_ID_3	0x11A	1001
SLAVE_NVM_ID_4	0x11B	0110
SLAVE_NVM_ID_5	0x11C	1010

5.4.2.4.2 Periodic Checking of the SPMI

The TPS6594-Q1device as SPMI master automatically executes the SPMI interface BIST periodically while device is operating. Frequency of SPMI interface BIST is set by the SPMI_WD_BOOT_INTERVAL[3:0] register bits during the device boot time, and by SPMI_WD_RUNTIME_INTERVAL[3:0] after the device reaches mission states. The setting of the SPMI_WD_x_INTERVAL[3:0] bits should be the same for all the devices on the same SPMI network. Slave devices should expect that the master device polls NVM ID within 1.5x the period of SPMI_WD_x_INTERVAL[3:0]. This provides enough margins for clock uncertainty.

During mission state operation, master device expects the slave devices to respond to NVM ID request within the polling period set by the SPMI_WD_RESPONSE_TIMEOUT[3:0] register bits. In other words, from the polling start command the slaves must responded within the time interval set by SPMI_WD_RESPONSE_TIMEOUT[3:0].

During boot time or when the device enters Safe Recovery state, to prevent the SPMI master from polling the slave devices too often while the slave device is recovering from a system error such as a thermal shutdown event, the SPMI_WD_AUTO_BOOT_TIMEOUT[7:0] register bits sets a longer timeout period for the slave devices to respond to the master device before the master device reports an error.

Violating either the SPMI_WD_RESPONSE_TIMEOUT[3:0] period or the SPMI_WD_AUTO_BOOT_TIMEOUT[7:0] period will cause the triggering of SPMI error.

5.4.2.4.3 SPMI Message Priorities

SPMI bus will use the protocol priority levels listed in Table 5-36 for each message type of communications.

Table 5-36. SPMI Message Types and Priorities

SPMI protocol priority level	Name of priority level in SPMI standard	Message types
Highest	Slave A-bit arbitration	State transition messages from slave(s) to master
	Master priority arbitration	State transition messages from master to slave(s)
	Slave SR-bit arbitration	Slave NVM ID to master
Lowest	Master secondary arbitration	Master request of NVM IDs from slave(s)

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5.5 Control Interfaces

The device has two, exclusive selectable (from factory settings) interfaces. The first selection is two high-speed I^2C interfaces (I2C_SPI_SEL=0). The second selection is one SPI interface (I2C_SPI_SEL=1). Both the SPI and the I2C1 interfaces are used to fully control and configure the device and have access to all of the configuration registers, as well as the Watchdog registers. During normal operating mode, when the I^2C configuration is selected, and GPIO1 and GPIO2 pins are configured as the SCL_I2C2 and SDA_I2C2 pins, I2C2 interface will become the dedicated interface for the Q&A Watchdog communication channel, while I2C1 interface will no longer have access to the Watchdog registers. When the device enters EEPROM programing mode or test mode, I2C2 interface is automatically disabled, and I2C1 interface will have access to all of the registers, including the Watchdog registers.

5.5.1 CRC Calculation for I^2C and SPI Interface Protocols

For safety applications, the TPS6594-Q1device supports read and write protocols with embedded CRC data fields. Both the master and slave devices use a standard CRC-8 polynomial to calculate the checksum value: $X^8 + X^2 + X + 1$.The CRC algorithm details are as follows:

- Initial value for the remainder is all 1s.
- Big-endian bit stream order
- Result inversion is enabled.

For I^2C Interface, the TPS6594-Q1 device uses this polynomial to calculate the checksum value on every bit except the ACK and NACK bits it receives from the MCU during a write protocol. The device compares this calculated checksum with the MCRC checksum value which the device receives from the MCU. The device also uses this polynomial to calculate the SCRC checksum value based on every bit except the ACK and NACK bits which the device transmits to the MCU during a read protocol. The master device (MCU) must use this same polynomial to calculate the checksum value based on the bits which the MCU receives from the device. The MCU must compare this calculated checksum with the SCRC checksum value which it receives from the device.

For the SPI interface, the TPS6594-Q1 device uses this polynomial to calculate the checksum value on every bit it receives from the MCU during a write protocol. The device compares this calculated checksum with the MCRC checksum value which the device receives from the MCU. The device also uses this polynomial to calculate the SCRC checksum value based on every bit which the device transmits to the MCU during a read protocol. The master device (MCU) must use this same polynomial to calculate the checksum value based on the bits which the MCU receives from the device. The MCU must compare this calculated checksum with the SCRC checksum value which it receives from the device.

Figure 5-54 and Figure 5-55 are examples for the 4-bit MCRC and the SCRC calculation from 16-bit databus.

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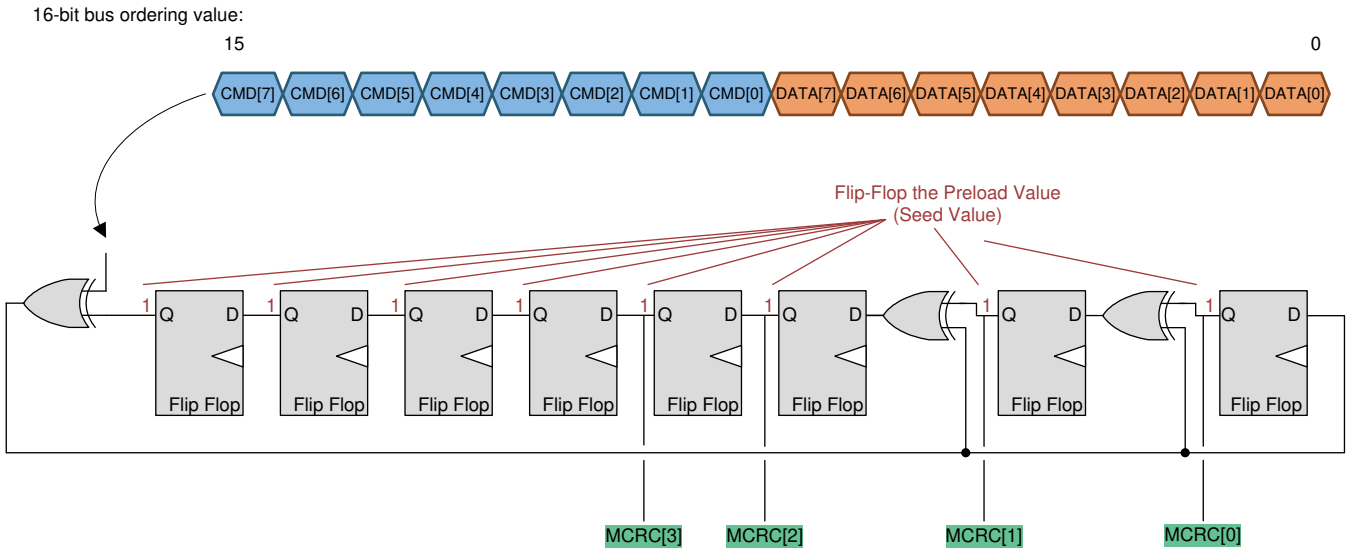

Figure 5-54. Calculation of 4-Bit Master CRC (MCRC) Output

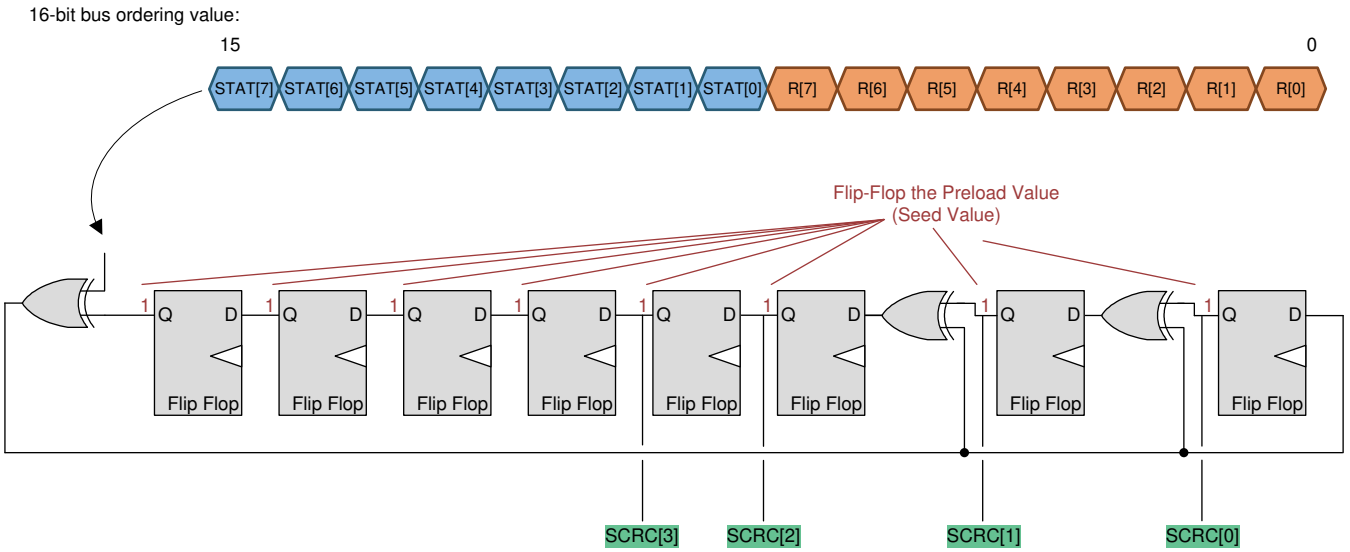

Figure 5-55. Calculation of 4-Bit Slave CRC (SCRC) Input

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5.5.2 I^2C-Compatible Interface

The default I^2C1 7-bit slave device address of the TPS6594-Q1 device is set to 0x48 (0b1001000 in binary), while the two least-significant bits can be changed for alternative page selection listed under Section 5.6.1. The default 7-bit slave device address for the Q&A WatchDog I^2C2 interface is set to 0x12. The I2C1_ID and I2C2_ID register bits can be used to reconfigure the 7-bit default slave address for the corresponding I^2C interface.

The I^2C-compatible synchronous serial interface provides access to the configurable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode plus (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

5.5.2.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

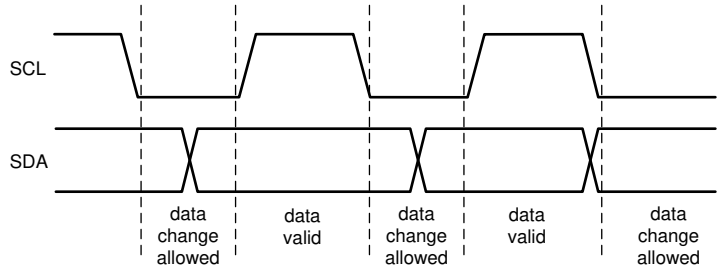

Figure 5-56. Data Validity Diagram

5.5.2.2 Start and Stop Conditions

The device is controlled through an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as the SDA signal going from HIGH to LOW while the SCL signal is HIGH. A STOP condition is defined as the SDA signal going from LOW to HIGH while the SCL signal is HIGH. The I²C master device always generates the START and STOP conditions.

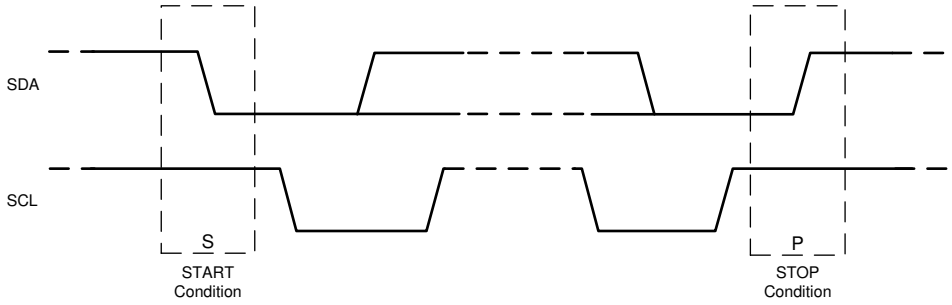

Figure 5-57. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. Figure 5-58 shows the SDA and SCL signal timing for the I²C-compatible bus. For timing values, see the *Specification* section.

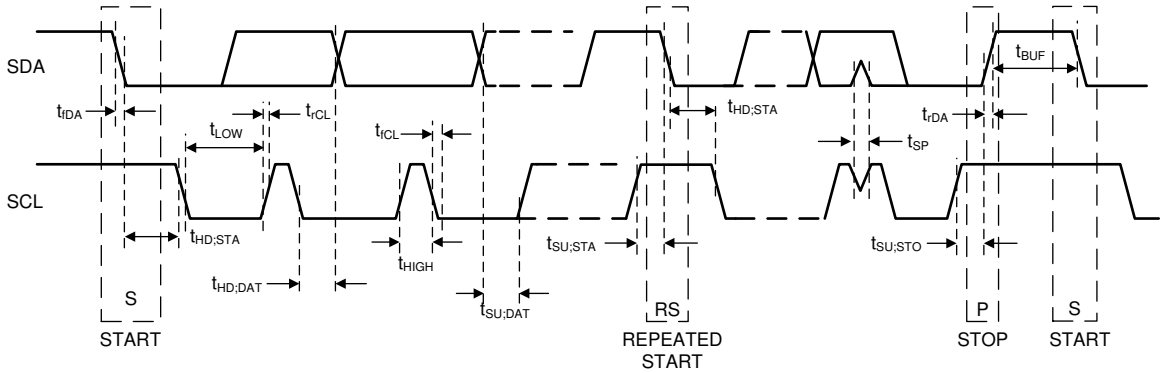

Figure 5-58. I²C-Compatible Timing

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5.5.2.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register. Figure 5-59 shows an example bit format of device address 110000-Bin = 60Hex.

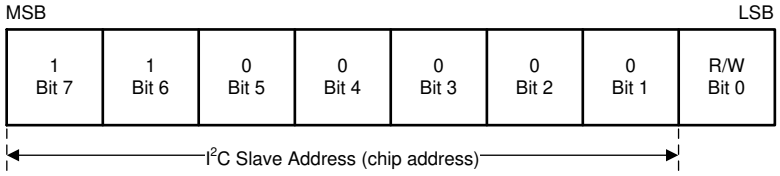

Figure 5-59. Example Device Address

In case the MCU attempts to write to a register-address that does not exist, the device sets the COMM_ADR_ERR_INT (for I2C1) or I2C2_ADR_ERR_INT (for I2C2) bit, unless the COMM_ADR_ERR_MASK or I2C2_ADR_ERR_MASK bit is set. The MCU must clear this bit by writing a '1' to the COMM_ADR_ERR_INT (for I2C1) or I2C2_ADR_ERR_INT (for I2C2) bit.

For safety applications, the device supports read and write protocols with embedded CRC data fields. In a write cycle, the I^{2}C master should provide the 8-bit CRC value after sending the write data bits and receiving the ACK from the slave. The CRC value should be calculated from every bit included in the write protocol except the ACK bits from the slave. In a read cycle, the I^{2}C slave should provide the 8-bit CRC value after sending the read data bits and receiving the NACK from the master. The CRC value should be calculated from every bit included in the read protocol except the ACK and NACK bits.

The embedded CRC field can be enabled or disabled from the protocol by setting the I2C1_SPI_CRC_EN (for I2C1) or I2C2_CRC_EN (for I2C2) register bit to '1' - enabled, '0' - disabled. The default of this bit is configurable through the NVM.

In case the calculated CRC-value does not match the received CRC-check-sum, an I^{2}C-CRC-error is detected, the COMM_CRC_ERR_INT (for I2C1) or I2C2_CRC_ERR_INT (for I2C2) bit is set, unless it is masked by the COMM_CRC_ERR_MASK or I2C2_CRC_ERR_MASK bit. The MCU must clear this bit by writing a '1' to the COMM_CRC_ERR_INT (for I2C1) or I2C2_CRC_ERR_INT (for I2C2) bit.

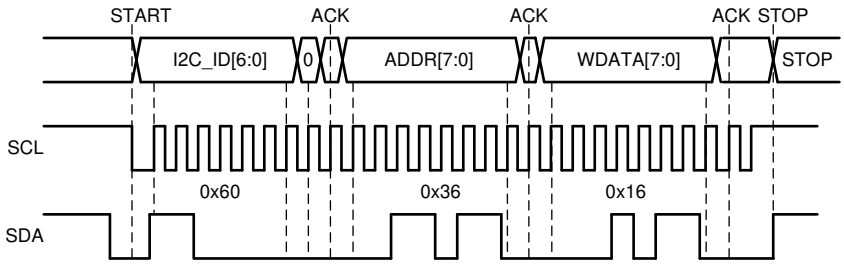

Figure 5-60. I^{2}C Write Cycle without CRC

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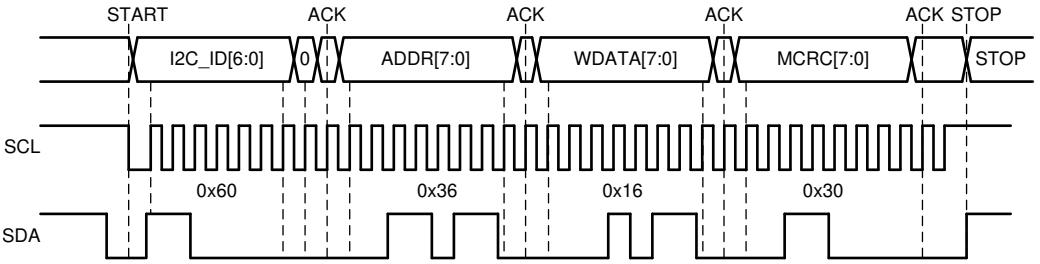
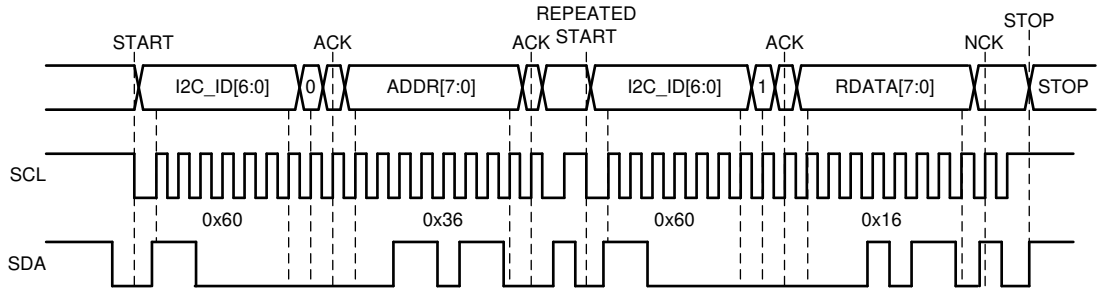


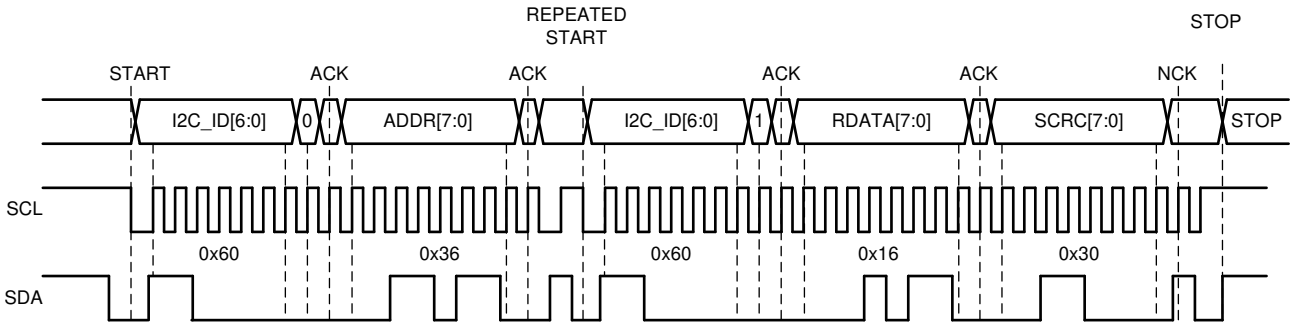
Master provides MCRC[7:0], which is calculated from the I2C_ID, R/W, ADDR, and the WDATA bits (24 bits).

Figure 5-61. I²C Write Cycle with CRC



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 5-62. I²C Read Cycle without CRC



Slave provides SCRC[7:0], which is calculated from the I2C_ID, R/W, ADDR, I2C_ID, R/W, and the RDATA bits (32 bits).

Figure 5-63. I²C READ Cycle with CRC

5.5.2.4 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the device, the internal address index counter is incremented by one and the next register is written. Table 5-37 lists the writing sequence to two consecutive registers. Note that auto increment feature does not support CRC protocol.

Table 5-37. Auto-Increment Example

MASTER ACTION	START	DEVICE ADDRESS = 0x60	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
PMIC device				ACK		ACK		ACK		ACK	

5.5.3 *Serial Peripheral Interface (SPI)*

The device supports SPI serial-bus interface and it operates as a slave. A single read and write transmissions consist of 24-bit write and read cycles (32-bit if CRC is enabled) in the following order:

- Bits 1-8: ADDR[7:0], Register address

- Bits 9-11: PAGE[2:0], Page address for register
- Bit 12: Read/Write definition, 0 = WRITE, 1 = READ.
- Bits 13-16: RESERVED[4:0], Reserved, use all zeros.
- For Write: Bits 17-24: WDATA[7:0], write data
- For Write with CRC enabled: Bits 25-32: MCRC[7:0], CRC error code for bits 1-24, sent by master
- For Read: Bits 17-24: RDATA[7:0], read data
- For Read with CRC enabled: Bits 25-32: SCRC[7:0], CRC error code for bits 1-24, sent by slave

The embedded CRC filed can be enabled or disabled from the protocol by setting the I2C1_SPI_CRC_EN register bit to '1' - enabled, '0' - disabled. The default of this bit is configurable through the NVM.

The SDO output is in a high-impedance state when the CS pin is high. When the CS pin is low, the SDO output is always driven low except when the RDATA or SCRC bits are sent. When the RDATA or SCRC bits are sent, the SDO output is driven accordingly.

The address, page, data, and CRC are transmitted MSB first. The slave-select signal, CS, must be low during the cycle transmission. The CS signal resets the interface when it is high, and must be taken high between successive cycles. Data is clocked in on the rising edge of the SCLK clock signal and it is clocked out on the falling edge of SCLK clock signal

The *SPI Timing* diagram shows the timing information for these signals.

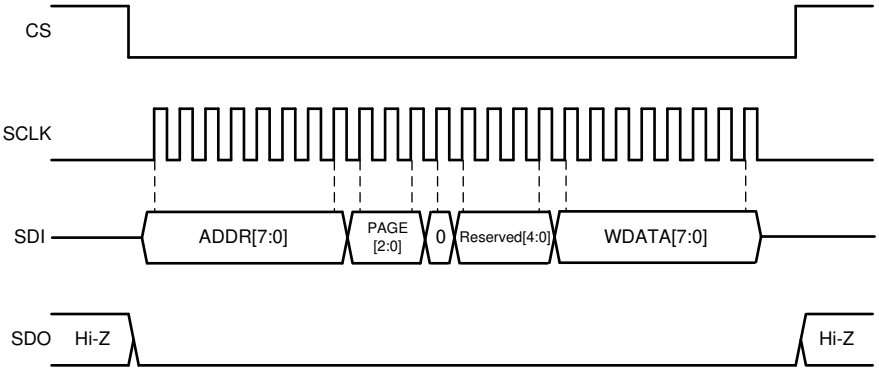


Figure 5-64. SPI Write Cycle

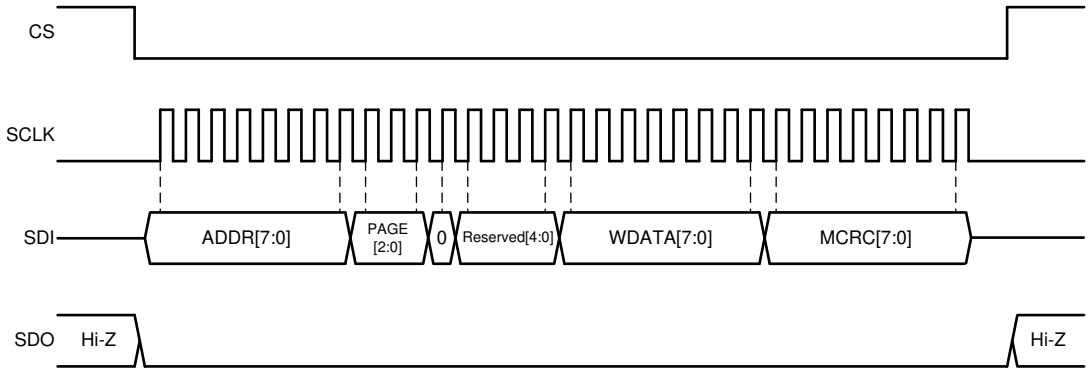


Figure 5-65. SPI Write Cycle with Master CRC

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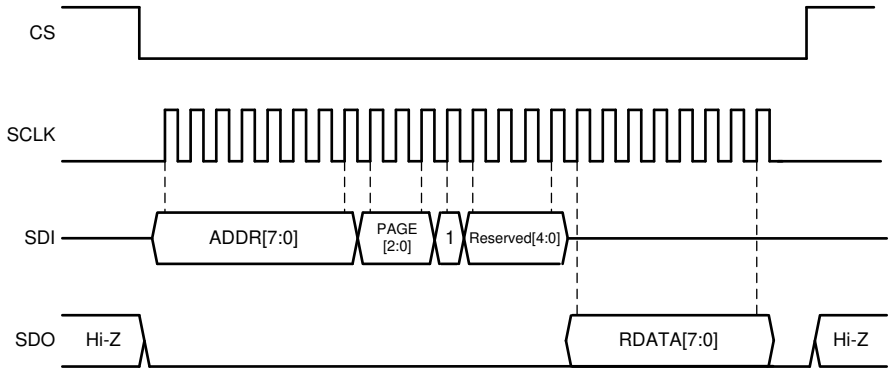

Figure 5-66. SPI Read Cycle

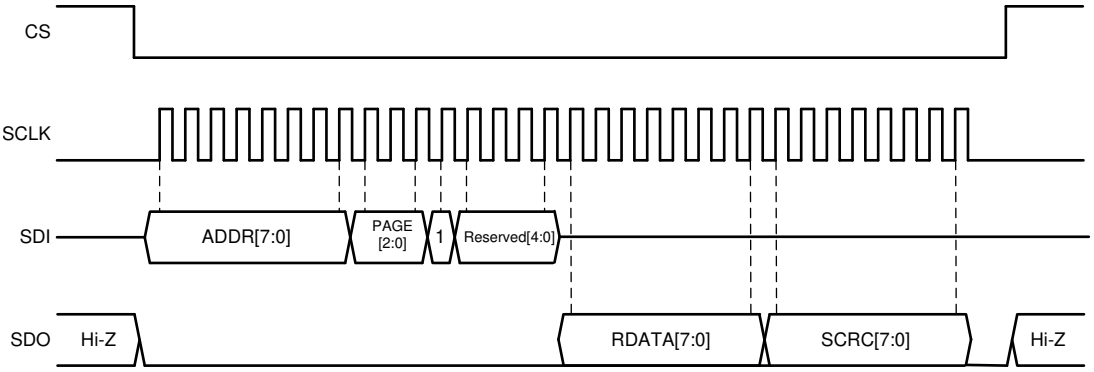

Figure 5-67. SPI Read Cycle with Slave CRC

5.6 Configurable Registers

5.6.1 Register Page Partitioning

The registers in the TPS6594-Q1 device are organized into five internal pages of 256 bytes each. The first 3 bits of the 11-bit register address offset indicates one of the following pages which the register belongs to:

- Page 0: User Registers
- Page 1: NVM Control, Configuration, and Test Registers
- Page 2: Trim Registers
- Page 3: SRAM for PFSM Registers
- Page 4: WatchDog Registers

5.6.2 CRC Protection for Configuration, Control, and Test Registers

The CRC-8 engine continuously checks the control registers on the device. The expected CRC-8 value is stored in the NVM. Anytime a mismatch between the calculated and expected CRC-8 values is detected, the interrupt bit REG_CRC_ERR_INT is set and the device will force a orderly shutdown sequence to return to the SAFE RECOVERY state. The device NVM control, configuration, and test registers in page 1 are protected against read or write access when the device is in normal functional mode. The CRC8 protection for the NVM registers is configured and enabled only when the device is in DFT/DEBUG operating mode.

The CRC-8 engine uses a standard CRC-8 polynomial to calculate the internal known-good checksum-value which is $X^8 + X^2 + X + 1$.

The initial value for the remainder of the polynomial is all 1s and is in big-endian bit-stream order. The inversion of the calculated result is enabled.

NOTE

The CRC-8 engine assume the value of '0' for all undefined or reserved bits in all control registers. Therefore the software MUST NOT write the value of '1' to any of these undefined or reserved bits. If the value of '1 is written to any undefined or reserved bit of a writeable register, a mismatch between the calculated and expected CRC-8 values will be detected, a REG_CRC_ERR interrupt will be set, and the device will force a orderly shutdown sequence to return to the SAFE RECOVERY state.

5.6.3 Register Write Protection

For safety application, in order to prevent unintentional writes to the control registers, the TPS6594-Q1 device implements locking and unlocking mechanisms to many of its configuration/control registers described in the following subsections.

5.6.3.1 ESM and WDOG Configuration Registers

The configuration registers for the watchdog and the ESM modules are locked when their monitoring functions are in operation. The timing and the list of the watchdog registers which will locked is described under Section 5.3.10.2. The list of ESM registers locked after the start of each ESM module is described under 节 5.3.11

5.6.3.2 User Registers

User registers in page 0, except the ESM and the WDOG configuration registers described in Section 5.6.3.1, and the interrupt registers, are write protected by a dedicated lock. User must write '0x9B' to the REGISTER_LOCK register to unlock the register. Writing any value other than '0x9B' will activate the lock again. To check the register lock status, user should read the REGISTER_LOCK_STATUS bit. When this bit is '0', it indicates the user registers are unlocked. When this bit is '1', the user registers are locked. During startup sequence such as powering up for the first time, waking up from LP_STANDBY, or recovering from SAFE_RECOVERY, the user registers will be unlocked automatically.

As an extra measure of protection to prevent the accidental change of the buck frequency while the buck is in operation, the BUCKn_FREQ_SEL register bits are locked by the REGISTER_LOCK register as well as the FREQ_SEL_UNCLOCK bit. Users must set the FREQ_SEL_UNLOCK bit to '1' in addition to writing '0x9B' to the REGISTER_LOCK register in order to change the BUCKn_FREQ_SEL bit setting. The default setting of the FREQ_SEL_UNLOCK bit comes from the NVM register setting. User is advised against changing the buck frequency while the buck is in operation.

5.6.3.3 NVM Control and Configuration Registers

The NVM registers can be unlocked for reconfiguration by first writing '0x98', '0xB8', '0x13', and '0x7D' in sequence to the USER_EE_PROG_UNLOCK_SEQ bits. Writing these value out of sequence or writing any other value will lock the NVM registers from write access. After the sequence write, the device enters user EEPROM programing mode and I2C2 is disabled. User can use I2C1 to access all of the regsiters including the WDOG registers in page4. User can also gain write access to the USER_PROG_UNLOCK_CODE bits, where user can write a customized unlock code. The default value of the USER_PROG_UNLOCK_CODE is trimmed during the initial NVM configuration.

5.6.3.4 Test and Trim Registers

The test and trim register are only writeable in test mode. To enter test mode, user must set the voltage at the AMUXOUT pin to 2 V above VCCA, and write *4 TBD* values to the TM_UNLOCK_CODE regsiter bits. When the device enters test mode, FFSM and PFSM will not operate. I2C2 will be disabled and I2C1 will have access to all registers include the WDOG register in page4.

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5.7 Register Maps

5.7.1 TPS6594x_map Registers

Table 5-38 lists the TPS6594x_map registers. All register offset addresses not listed in Table 5-38 should be considered as reserved locations and the register contents should not be modified.

Table 5-38. TPS6594X_MAP Registers

Offset	Acronym	Register Name	Section
0x1	DEV_REV		Section 5.7.1.1
0x2	NVM_CODE_1		Section 5.7.1.2
0x3	NVM_CODE_2		Section 5.7.1.3
0x4	BUCK1_CTRL		Section 5.7.1.4
0x5	BUCK1_CONF		Section 5.7.1.5
0x6	BUCK2_CTRL		Section 5.7.1.6
0x7	BUCK2_CONF		Section 5.7.1.7
0x8	BUCK3_CTRL		Section 5.7.1.8
0x9	BUCK3_CONF		Section 5.7.1.9
0xA	BUCK4_CTRL		Section 5.7.1.10
0xB	BUCK4_CONF		Section 5.7.1.11
0xC	BUCK5_CTRL		Section 5.7.1.12
0xD	BUCK5_CONF		Section 5.7.1.13
0xE	BUCK1_VOUT_1		Section 5.7.1.14
0xF	BUCK1_VOUT_2		Section 5.7.1.15
0x10	BUCK2_VOUT_1		Section 5.7.1.16
0x11	BUCK2_VOUT_2		Section 5.7.1.17
0x12	BUCK3_VOUT_1		Section 5.7.1.18
0x13	BUCK3_VOUT_2		Section 5.7.1.19
0x14	BUCK4_VOUT_1		Section 5.7.1.20
0x15	BUCK4_VOUT_2		Section 5.7.1.21
0x16	BUCK5_VOUT_1		Section 5.7.1.22
0x17	BUCK5_VOUT_2		Section 5.7.1.23
0x18	BUCK1_PG_WINDOW		Section 5.7.1.24
0x19	BUCK2_PG_WINDOW		Section 5.7.1.25
0x1A	BUCK3_PG_WINDOW		Section 5.7.1.26
0x1B	BUCK4_PG_WINDOW		Section 5.7.1.27
0x1C	BUCK5_PG_WINDOW		Section 5.7.1.28
0x1D	LDO1_CTRL		Section 5.7.1.29
0x1E	LDO2_CTRL		Section 5.7.1.30
0x1F	LDO3_CTRL		Section 5.7.1.31
0x20	LDO4_CTRL		Section 5.7.1.32
0x21	LDOINT_CTRL		Section 5.7.1.33
0x22	LDORTC_CTRL		Section 5.7.1.34
0x23	LDO1_VOUT		Section 5.7.1.35
0x24	LDO2_VOUT		Section 5.7.1.36
0x25	LDO3_VOUT		Section 5.7.1.37
0x26	LDO4_VOUT		Section 5.7.1.38
0x27	LDO1_PG_WINDOW		Section 5.7.1.39
0x28	LDO2_PG_WINDOW		Section 5.7.1.40

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x29	LDO3_PG_WINDOW		Section 5.7.1.41
0x2A	LDO4_PG_WINDOW		Section 5.7.1.42
0x2B	VCCA_VMON_CTRL		Section 5.7.1.43
0x2C	VCCA_PG_WINDOW		Section 5.7.1.44
0x31	GPIO1_CONF		Section 5.7.1.45
0x32	GPIO2_CONF		Section 5.7.1.46
0x33	GPIO3_CONF		Section 5.7.1.47
0x34	GPIO4_CONF		Section 5.7.1.48
0x35	GPIO5_CONF		Section 5.7.1.49
0x36	GPIO6_CONF		Section 5.7.1.50
0x37	GPIO7_CONF		Section 5.7.1.51
0x38	GPIO8_CONF		Section 5.7.1.52
0x39	GPIO9_CONF		Section 5.7.1.53
0x3A	GPIO10_CONF		Section 5.7.1.54
0x3B	GPIO11_CONF		Section 5.7.1.55
0x3C	NPWRON_CONF		Section 5.7.1.56
0x3D	GPIO_OUT_1		Section 5.7.1.57
0x3E	GPIO_OUT_2		Section 5.7.1.58
0x3F	GPIO_IN_1		Section 5.7.1.59
0x40	GPIO_IN_2		Section 5.7.1.60
0x41	RAIL_SEL_1		Section 5.7.1.61
0x42	RAIL_SEL_2		Section 5.7.1.62
0x43	RAIL_SEL_3		Section 5.7.1.63
0x44	FSM_TRIG_SEL_1		Section 5.7.1.64
0x45	FSM_TRIG_SEL_2		Section 5.7.1.65
0x46	FSM_TRIG_MASK_1		Section 5.7.1.66
0x47	FSM_TRIG_MASK_2		Section 5.7.1.67
0x48	FSM_TRIG_MASK_3		Section 5.7.1.68
0x49	MASK_BUCK1_2		Section 5.7.1.69
0x4A	MASK_BUCK3_4		Section 5.7.1.70
0x4B	MASK_BUCK5		Section 5.7.1.71
0x4C	MASK_LDO1_2		Section 5.7.1.72
0x4D	MASK_LDO3_4		Section 5.7.1.73
0x4E	MASK_VMON		Section 5.7.1.74
0x4F	MASK_GPIO1_8_FALL		Section 5.7.1.75
0x50	MASK_GPIO1_8_RISE		Section 5.7.1.76
0x51	MASK_GPIO9_11		Section 5.7.1.77
0x52	MASK_STARTUP		Section 5.7.1.78
0x53	MASK_MISC		Section 5.7.1.79
0x54	MASK_MODERATE_ERR		Section 5.7.1.80
0x56	MASK_FSM_ERR		Section 5.7.1.81
0x57	MASK_COMM_ERR		Section 5.7.1.82
0x58	MASK_READBACK_ERR		Section 5.7.1.83
0x59	MASK_ESM		Section 5.7.1.84
0x5A	INT_TOP		Section 5.7.1.85
0x5B	INT_BUCK		Section 5.7.1.86
0x5C	INT_BUCK1_2		Section 5.7.1.87

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x5D	INT_BUCK3_4		Section 5.7.1.88
0x5E	INT_BUCK5		Section 5.7.1.89
0x5F	INT_LDO_VMON		Section 5.7.1.90
0x60	INT_LDO1_2		Section 5.7.1.91
0x61	INT_LDO3_4		Section 5.7.1.92
0x62	INT_VMON		Section 5.7.1.93
0x63	INT_GPIO		Section 5.7.1.94
0x64	INT_GPIO1_8		Section 5.7.1.95
0x65	INT_STARTUP		Section 5.7.1.96
0x66	INT_MISC		Section 5.7.1.97
0x67	INT_MODERATE_ERR		Section 5.7.1.98
0x68	INT_SEVERE_ERR		Section 5.7.1.99
0x69	INT_FSM_ERR		Section 5.7.1.100
0x6A	INT_COMM_ERR		Section 5.7.1.101
0x6B	INT_READBACK_ERR		Section 5.7.1.102
0x6C	INT_ESM		Section 5.7.1.103
0x6D	STAT_BUCK1_2		Section 5.7.1.104
0x6E	STAT_BUCK3_4		Section 5.7.1.105
0x6F	STAT_BUCK5		Section 5.7.1.106
0x70	STAT_LDO1_2		Section 5.7.1.107
0x71	STAT_LDO3_4		Section 5.7.1.108
0x72	STAT_VMON		Section 5.7.1.109
0x73	STAT_STARTUP		Section 5.7.1.110
0x74	STAT_MISC		Section 5.7.1.111
0x75	STAT_MODERATE_ERR		Section 5.7.1.112
0x76	STAT_SEVERE_ERR		Section 5.7.1.113
0x77	STAT_READBACK_ERR		Section 5.7.1.114
0x78	PGOOD_SEL_1		Section 5.7.1.115
0x79	PGOOD_SEL_2		Section 5.7.1.116
0x7A	PGOOD_SEL_3		Section 5.7.1.117
0x7B	PGOOD_SEL_4		Section 5.7.1.118
0x7C	PLL_CTRL		Section 5.7.1.119
0x7D	CONFIG_1		Section 5.7.1.120
0x7E	CONFIG_2		Section 5.7.1.121
0x80	ENABLE_DRV_REG		Section 5.7.1.122
0x81	MISC_CTRL		Section 5.7.1.123
0x82	ENABLE_DRV_STAT		Section 5.7.1.124
0x83	RECOV_CNT_REG_1		Section 5.7.1.125
0x84	RECOV_CNT_REG_2		Section 5.7.1.126
0x85	FSM_I2C_TRIGGERS		Section 5.7.1.127
0x86	FSM_NSLEEP_TRIGGERS		Section 5.7.1.128
0x87	BUCK_RESET_REG		Section 5.7.1.129
0x88	SPREAD_SPECTRUM_1		Section 5.7.1.130
0x8A	FREQ_SEL		Section 5.7.1.131
0x8B	FSM_STEP_SIZE		Section 5.7.1.132
0x8C	LDO_RV_TIMEOUT_REG_1		Section 5.7.1.133
0x8D	LDO_RV_TIMEOUT_REG_2		Section 5.7.1.134

Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x8E	USER_SPARE_REGS		Section 5.7.1.135
0x8F	ESM_MCU_START_REG		Section 5.7.1.136
0x90	ESM_MCU_DELAY1_REG		Section 5.7.1.137
0x91	ESM_MCU_DELAY2_REG		Section 5.7.1.138
0x92	ESM_MCU_MODE_CFG		Section 5.7.1.139
0x93	ESM_MCU_HMAX_REG		Section 5.7.1.140
0x94	ESM_MCU_HMIN_REG		Section 5.7.1.141
0x95	ESM_MCU_LMAX_REG		Section 5.7.1.142
0x96	ESM_MCU_LMIN_REG		Section 5.7.1.143
0x97	ESM_MCU_ERR_CNT_REG		Section 5.7.1.144
0x98	ESM_SOC_START_REG		Section 5.7.1.145
0x99	ESM_SOC_DELAY1_REG		Section 5.7.1.146
0x9A	ESM_SOC_DELAY2_REG		Section 5.7.1.147
0x9B	ESM_SOC_MODE_CFG		Section 5.7.1.148
0x9C	ESM_SOC_HMAX_REG		Section 5.7.1.149
0x9D	ESM_SOC_HMIN_REG		Section 5.7.1.150
0x9E	ESM_SOC_LMAX_REG		Section 5.7.1.151
0x9F	ESM_SOC_LMIN_REG		Section 5.7.1.152
0xA0	ESM_SOC_ERR_CNT_REG		Section 5.7.1.153
0xA1	REGISTER_LOCK		Section 5.7.1.154
0xA2	USER_EE_CTRL_1		Section 5.7.1.155
0xA3	USER_EE_CTRL_2		Section 5.7.1.156
0xA4	SRAM_ADDR_CTRL		Section 5.7.1.157
0xA5	RECOV_CNT_PFSM_INCR		Section 5.7.1.158
0xA6	MANUFACTURING_VER		Section 5.7.1.159
0xA7	CUSTOMER_NVM_ID_REG		Section 5.7.1.160
0xB5	RTC_SECONDS		Section 5.7.1.161
0xB6	RTC_MINUTES		Section 5.7.1.162
0xB7	RTC_HOURS		Section 5.7.1.163
0xB8	RTC_DAYS		Section 5.7.1.164
0xB9	RTC_MONTHS		Section 5.7.1.165
0xBA	RTC_YEARS		Section 5.7.1.166
0xBB	RTC_WEEKS		Section 5.7.1.167
0xBC	ALARM_SECONDS		Section 5.7.1.168
0xBD	ALARM_MINUTES		Section 5.7.1.169
0xBE	ALARM_HOURS		Section 5.7.1.170
0xBF	ALARM_DAYS		Section 5.7.1.171
0xC0	ALARM_MONTHS		Section 5.7.1.172
0xC1	ALARM_YEARS		Section 5.7.1.173
0xC2	RTC_CTRL_1		Section 5.7.1.174
0xC3	RTC_CTRL_2		Section 5.7.1.175
0xC4	RTC_STATUS		Section 5.7.1.176
0xC5	RTC_INTERRUPTS		Section 5.7.1.177
0xC6	RTC_COMP_LSB		Section 5.7.1.178
0xC7	RTC_COMP_MSB		Section 5.7.1.179
0xC8	RTC_RESET_STATUS		Section 5.7.1.180
0xC9	SCRATCH_PAD_REG_1		Section 5.7.1.181

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0xCA	SCRATCH_PAD_REG_2		Section 5.7.1.182
0xCB	SCRATCH_PAD_REG_3		Section 5.7.1.183
0xCC	SCRATCH_PAD_REG_4		Section 5.7.1.184
0xCD	PFSM_DELAY_REG_1		Section 5.7.1.185
0xCE	PFSM_DELAY_REG_2		Section 5.7.1.186
0xCF	PFSM_DELAY_REG_3		Section 5.7.1.187
0xD0	PFSM_DELAY_REG_4		Section 5.7.1.188
0xEF	CRC_CALC_CONTROL		Section 5.7.1.189
0xF0	CRC_1		Section 5.7.1.190
0xF1	CRC_2		Section 5.7.1.191
0xF2	CRC_3		Section 5.7.1.192
0xF3	CRC_4		Section 5.7.1.193
0xF4	CRC_5		Section 5.7.1.194
0xF5	CRC_6		Section 5.7.1.195
0xF6	CRC_7		Section 5.7.1.196
0xF7	CRC_8		Section 5.7.1.197
0xF8	CRC_9		Section 5.7.1.198
0xF9	CRC_10		Section 5.7.1.199
0xFA	CRC_11		Section 5.7.1.200
0xFB	CRC_12		Section 5.7.1.201
0xFE	CRC_15		Section 5.7.1.202
0xFF	CRC_16		Section 5.7.1.203
0x100	BUCK_CONFIG_ANALOG_0		Section 5.7.1.204
0x101	BUCK_CONFIG_ANALOG_1		Section 5.7.1.205
0x102	BUCK_CONFIG_ANALOG_2		Section 5.7.1.206
0x103	BUCK_CONFIG_ANALOG_3		Section 5.7.1.207
0x104	BUCK_CONFIG_ANALOG_4		Section 5.7.1.208
0x105	BUCK_CONFIG_ANALOG_5		Section 5.7.1.209
0x106	BUCK_CONFIG_ANALOG_6		Section 5.7.1.210
0x107	BUCK_CONFIG_ANALOG_7		Section 5.7.1.211
0x108	BUCK_CONFIG_ANALOG_8		Section 5.7.1.212
0x109	BUCK_CONFIG_RADAR		Section 5.7.1.213
0x10A	BUCK_CONFIG_DIGITAL_0		Section 5.7.1.214
0x10B	BUCK_CONFIG_DIGITAL_1		Section 5.7.1.215
0x10C	BUCK_CONFIG_DIGITAL_2		Section 5.7.1.216
0x10D	BUCK_CONFIG_DIGITAL_3		Section 5.7.1.217
0x10E	BUCK_CONFIG_DIGITAL_4		Section 5.7.1.218
0x10F	BUCK_CONFIG_DIGITAL_5		Section 5.7.1.219
0x110	BUCK_CONFIG_DIGITAL_6		Section 5.7.1.220
0x111	BUCK_CONFIG_DIGITAL_7		Section 5.7.1.221
0x112	BUCK_CONFIG_DIGITAL_8		Section 5.7.1.222
0x113	BUCK_CONFIG_DIGITAL_9		Section 5.7.1.223
0x114	BUCK_CONFIG_DIGITAL_10		Section 5.7.1.224
0x115	BUCK_CONFIG_DIGITAL_11		Section 5.7.1.225
0x116	BUCK_CONFIG_DIGITAL_12		Section 5.7.1.226
0x117	GENERAL_REG_0		Section 5.7.1.227
0x118	GENERAL_REG_1		Section 5.7.1.228

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x119	GENERAL_REG_2		Section 5.7.1.229
0x11A	SERIAL_IF_CONFIG		Section 5.7.1.230
0x11B	SPMI_CONFIG_1		Section 5.7.1.231
0x11C	SPMI_CONFIG_2		Section 5.7.1.232
0x11D	SPMI_CONFIG_3		Section 5.7.1.233
0x11E	SPMI_CONFIG_4		Section 5.7.1.234
0x11F	SPMI_CONFIG_5		Section 5.7.1.235
0x120	SPMI_CONFIG_6		Section 5.7.1.236
0x121	SPMI_ID		Section 5.7.1.237
0x122	I2C1_ID_REG		Section 5.7.1.238
0x123	I2C2_ID_REG		Section 5.7.1.239
0x124	CLOCK_REQS		Section 5.7.1.240
0x125	PHASE_CONFIG		Section 5.7.1.241
0x126	SPMI_SLAVE_COUNT		Section 5.7.1.242
0x12C	XCOORD_REG		Section 5.7.1.243
0x12D	YCOORD_REG		Section 5.7.1.244
0x12E	WAFERNUM_REG		Section 5.7.1.245
0x12F	WAFERLOTNUM_REG_1		Section 5.7.1.246
0x130	WAFERLOTNUM_REG_2		Section 5.7.1.247
0x131	WAFERLOTNUM_REG_3		Section 5.7.1.248
0x132	WAFERFAB_REG		Section 5.7.1.249
0x133	BUCK_CONFIG_DIGITAL_13		Section 5.7.1.250
0x134	BUCK_CONFIG_DIGITAL_14		Section 5.7.1.251
0x135	BUCK_CONFIG_DIGITAL_15		Section 5.7.1.252
0x13F	SPREAD_SPECTRUM_CONFIG_1		Section 5.7.1.253
0x140	SPREAD_SPECTRUM_CONFIG_2		Section 5.7.1.254
0x141	USER_EE_PROG_UNLOCK		Section 5.7.1.255
0x142	INT_CONFIG_0		Section 5.7.1.256
0x143	SAFETY_CONFIG_0		Section 5.7.1.257
0x144	VM_VSYS_CONFIG_0		Section 5.7.1.258
0x145	RTC_CONFIG_0		Section 5.7.1.259
0x146	LDO1_3_FILT_CONFIG_0		Section 5.7.1.260
0x147	LDO1_CONFIG_0		Section 5.7.1.261
0x148	LDO2_CONFIG_0		Section 5.7.1.262
0x149	LDO3_CONFIG_0		Section 5.7.1.263
0x14A	LDO4_CONFIG_0		Section 5.7.1.264
0x160	TEST_MODE_LOCK		Section 5.7.1.265
0x161	TEST_MODE_STATUS		Section 5.7.1.266
0x162	TEST_SET_SCAN_MODE		Section 5.7.1.267
0x163	DMUX1_CTRL_1		Section 5.7.1.268
0x164	DMUX1_CTRL_2		Section 5.7.1.269
0x165	DMUX2_CTRL_1		Section 5.7.1.270
0x166	DMUX2_CTRL_2		Section 5.7.1.271
0x167	DMUX3_CTRL_1		Section 5.7.1.272
0x168	DMUX3_CTRL_2		Section 5.7.1.273
0x169	DMUX4_CTRL_1		Section 5.7.1.274
0x16A	DMUX4_CTRL_2		Section 5.7.1.275

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x16B	DMUX5_CTRL_1		Section 5.7.1.276
0x16C	DMUX5_CTRL_2		Section 5.7.1.277
0x16D	TEST_REG_8		Section 5.7.1.278
0x16E	TEST_REG_9		Section 5.7.1.279
0x16F	TEST_REG_10		Section 5.7.1.280
0x170	TEST_REG_11		Section 5.7.1.281
0x171	TEST_REG_12		Section 5.7.1.282
0x172	TEST_REG_13		Section 5.7.1.283
0x173	TEST_REG_14		Section 5.7.1.284
0x174	TEST_REG_15		Section 5.7.1.285
0x175	TEST_REG_16		Section 5.7.1.286
0x176	TEST_SPMI_1		Section 5.7.1.287
0x177	TEST_SPMI_2		Section 5.7.1.288
0x179	TEST_SPMI_5		Section 5.7.1.289
0x17A	TEST_SPMI_6		Section 5.7.1.290
0x17B	TEST_SPMI_7		Section 5.7.1.291
0x17C	TEST_PFSM_0		Section 5.7.1.292
0x17D	TEST_PFSM_1		Section 5.7.1.293
0x17E	TEST_PFSM_2		Section 5.7.1.294
0x17F	TEST_PFSM_3		Section 5.7.1.295
0x180	TEST_FFSM_1		Section 5.7.1.296
0x181	TEST_FFSM_2		Section 5.7.1.297
0x182	TEST_REG_29		Section 5.7.1.298
0x183	TEST_REG_30		Section 5.7.1.299
0x184	TEST_SRAM_1		Section 5.7.1.300
0x188	TEST_RTC_CAL_0		Section 5.7.1.301
0x18A	TEST_PADRING_0		Section 5.7.1.302
0x18B	TEST_PADRING_1		Section 5.7.1.303
0x18C	TEST_PADRING_3		Section 5.7.1.304
0x18D	TEST_PADRING_4		Section 5.7.1.305
0x18E	TEST_PADRING_5		Section 5.7.1.306
0x18F	TEST_PADRING_6		Section 5.7.1.307
0x190	TEST_PADRING_7		Section 5.7.1.308
0x191	TEST_VMVCCA_0		Section 5.7.1.309
0x192	TEST_VMPVIN_0		Section 5.7.1.310
0x193	TEST_INT_0		Section 5.7.1.311
0x194	TEST_INT_1		Section 5.7.1.312
0x195	TEST_SAFETY_0		Section 5.7.1.313
0x196	TEST_SAFETY_1		Section 5.7.1.314
0x197	TEST_SAFETY_2		Section 5.7.1.315
0x198	TEST_VM_VSYS_0		Section 5.7.1.316
0x199	TEST_RTC_0		Section 5.7.1.317
0x19A	TEST_RTC_1		Section 5.7.1.318
0x19B	TEST_LDO1_3_FILT_0		Section 5.7.1.319
0x19C	TEST_LDO1_0		Section 5.7.1.320
0x19D	TEST_LDO1_1		Section 5.7.1.321
0x19E	TEST_LDO2_0		Section 5.7.1.322

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x19F	TEST_LDO2_1		Section 5.7.1.323
0x1A0	TEST_LDO3_0		Section 5.7.1.324
0x1A1	TEST_LDO3_1		Section 5.7.1.325
0x1A2	TEST_LDO4_0		Section 5.7.1.326
0x1A3	TEST_EE_LDO_0		Section 5.7.1.327
0x1A4	TEST_BB_0		Section 5.7.1.328
0x1A5	BUCK1_ATEST_REG_0		Section 5.7.1.329
0x1A6	BUCK1_ATEST_REG_1		Section 5.7.1.330
0x1A7	BUCK1_ATEST_REG_2		Section 5.7.1.331
0x1A8	BUCK1_DTEST_REG_0		Section 5.7.1.332
0x1A9	BUCK1_DTEST_REG_1		Section 5.7.1.333
0x1AA	BUCK1_DTEST_REG_2		Section 5.7.1.334
0x1AB	BUCK1_DTEST_REG_3		Section 5.7.1.335
0x1AC	BUCK1_DTEST_REG_4		Section 5.7.1.336
0x1AE	BUCK2_ATEST_REG_0		Section 5.7.1.337
0x1AF	BUCK2_ATEST_REG_1		Section 5.7.1.338
0x1B0	BUCK2_ATEST_REG_2		Section 5.7.1.339
0x1B1	BUCK2_DTEST_REG_0		Section 5.7.1.340
0x1B2	BUCK2_DTEST_REG_1		Section 5.7.1.341
0x1B3	BUCK2_DTEST_REG_2		Section 5.7.1.342
0x1B4	BUCK2_DTEST_REG_3		Section 5.7.1.343
0x1B5	BUCK2_DTEST_REG_4		Section 5.7.1.344
0x1B7	BUCK3_ATEST_REG_0		Section 5.7.1.345
0x1B8	BUCK3_ATEST_REG_1		Section 5.7.1.346
0x1B9	BUCK3_ATEST_REG_2		Section 5.7.1.347
0x1BA	BUCK3_DTEST_REG_0		Section 5.7.1.348
0x1BB	BUCK3_DTEST_REG_1		Section 5.7.1.349
0x1BC	BUCK3_DTEST_REG_2		Section 5.7.1.350
0x1BD	BUCK3_DTEST_REG_3		Section 5.7.1.351
0x1BE	BUCK3_DTEST_REG_4		Section 5.7.1.352
0x1C0	BUCK4_ATEST_REG_0		Section 5.7.1.353
0x1C1	BUCK4_ATEST_REG_1		Section 5.7.1.354
0x1C2	BUCK4_ATEST_REG_2		Section 5.7.1.355
0x1C3	BUCK4_DTEST_REG_0		Section 5.7.1.356
0x1C4	BUCK4_DTEST_REG_1		Section 5.7.1.357
0x1C5	BUCK4_DTEST_REG_2		Section 5.7.1.358
0x1C6	BUCK4_DTEST_REG_3		Section 5.7.1.359
0x1C7	BUCK4_DTEST_REG_4		Section 5.7.1.360
0x1C9	BUCK5_ATEST_REG_0		Section 5.7.1.361
0x1CA	BUCK5_ATEST_REG_1		Section 5.7.1.362
0x1CB	BUCK5_ATEST_REG_2		Section 5.7.1.363
0x1CC	BUCK5_DTEST_REG_0		Section 5.7.1.364
0x1CD	BUCK5_DTEST_REG_1		Section 5.7.1.365
0x1CE	BUCK5_DTEST_REG_2		Section 5.7.1.366
0x1CF	BUCK5_DTEST_REG_3		Section 5.7.1.367
0x1D0	BUCK5_DTEST_REG_4		Section 5.7.1.368
0x1D2	BUCK1_STATE		Section 5.7.1.369

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x1D3	BUCK2_STATE		Section 5.7.1.370
0x1D4	BUCK3_STATE		Section 5.7.1.371
0x1D5	BUCK4_STATE		Section 5.7.1.372
0x1D6	BUCK5_STATE		Section 5.7.1.373
0x1D7	BUCK1_INTEGRATOR		Section 5.7.1.374
0x1D8	BUCK2_INTEGRATOR		Section 5.7.1.375
0x1D9	BUCK3_INTEGRATOR		Section 5.7.1.376
0x1DA	BUCK4_INTEGRATOR		Section 5.7.1.377
0x1DB	BUCK5_INTEGRATOR		Section 5.7.1.378
0x1DC	BUCK_STATUS		Section 5.7.1.379
0x1E0	EEPROM_CONTROL_1	The TM_EE_CFG_* bits provide configuration information that will effect TM_EE_CMD_* operation.	Section 5.7.1.380
0x1E1	EEPROM_CONTROL_2	Any disabled banks will be skipped during automated command load and program operations Note this bit has no value for a single bank and the corresponding bit can be safely tied low.	Section 5.7.1.381
0x1E2	EEPROM_CONTROL_3		Section 5.7.1.382
0x1E7	EEPROM_CONTROL_8	EEPROM data for prog and read	Section 5.7.1.383
0x1E8	EEPROM_CONTROL_9	EEPROM data for prog and read	Section 5.7.1.384
0x1E9	EEPROM_CONTROL_10	EEPROM data for prog and read	Section 5.7.1.385
0x1EA	EEPROM_CONTROL_11	EEPROM data for prog and read	Section 5.7.1.386
0x1EB	EEPROM_CONTROL_12		Section 5.7.1.387
0x1EC	EEPROM_CONTROL_13		Section 5.7.1.388
0x1ED	EEPROM_CONTROL_14		Section 5.7.1.389
0x1EE	EEPROM_CONTROL_15		Section 5.7.1.390
0x1EF	EEPROM_CONTROL_16	The TM_EE_CMD_* bits execute commands that are carried out by the digital Eeprom controller. These bits are all WriteSelfClear, such that they are only high for 1 cycle to initiate the operation. If multiple commands are set together they will execute in the order 1)TM_EE_CMD_READ 2)TM_EE_CMD_ERASE 3)TM_EE_CMD_PROG.	Section 5.7.1.391
0x1F0	EEPROM_CONTROL_17	Directly force Eeprom control signals (Corresponding name) and thereby bypassing the use of the Eeprom controller. Note these register bits are ORed with Eeprom controller driver, so it is imperative that they are used separately. For detailed description of Eeprom control signals see Synopsys Design Ware NVM Databook (https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.33756.60785).	Section 5.7.1.392
0x1F1	EEPROM_CONTROL_18	Directly drive Eeprom test signals (Corresponding name) and thereby bypassing the use of the Eeprom controller. Be aware that some of these signals are also utilized by Eeprom controller to achieve higher level functionality (See TM_EE_CFG_*). For detailed description of Eeprom control signals see Synopsys Design Ware NVM Databook (https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.33756.60785).	Section 5.7.1.393
0x1F2	EEPROM_CONTROL_19		Section 5.7.1.394
0x1F3	EEPROM_CONTROL_20		Section 5.7.1.395
0x200	TRIM_VMVCCA_0		Section 5.7.1.396
0x201	TRIM_VMVCCA_1		Section 5.7.1.397
0x202	TRIM_VMVCCA_2		Section 5.7.1.398

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x204	TRIM_VMPVIN_0		Section 5.7.1.399
0x205	TRIM_VMPVIN_1		Section 5.7.1.400
0x207	TRIM_INT_0		Section 5.7.1.401
0x208	TRIM_INT_1		Section 5.7.1.402
0x209	TRIM_INT_2		Section 5.7.1.403
0x20A	TRIM_INT_3		Section 5.7.1.404
0x20B	TRIM_INT_4	trim_osc_20mhz is separated from int_trim_ocore bus, so that it can be located to RTC domain. The reason for moving it to RTC domain is to speed up startup from LP_STANDBY. RTC domain stays powered up in LP_STANDBY so counting the 100us NVM_LDO startup delay is done with correct trim value. trim_osc_20mhz is routed through INT domain to LEO_FS_DIGITAL output, so the output will be INT domain signal (since it goes throug level shifters).	Section 5.7.1.405
0x20C	TRIM_INT_5		Section 5.7.1.406
0x20D	TRIM_INT_6		Section 5.7.1.407
0x20E	TRIM_INT_7		Section 5.7.1.408
0x20F	TRIM_INT_8		Section 5.7.1.409
0x212	TRIM_SAFETY_0		Section 5.7.1.410
0x213	TRIM_SAFETY_1		Section 5.7.1.411
0x214	TRIM_SAFETY_2		Section 5.7.1.412
0x215	TRIM_SAFETY_3		Section 5.7.1.413
0x216	TRIM_SAFETY_4		Section 5.7.1.414
0x217	TRIM_SAFETY_5		Section 5.7.1.415
0x218	TRIM_SAFETY_6		Section 5.7.1.416
0x219	TRIM_SAFETY_7		Section 5.7.1.417
0x21A	TRIM_SAFETY_8		Section 5.7.1.418
0x21B	TRIM_SAFETY_9		Section 5.7.1.419
0x21C	TRIM_SAFETY_10		Section 5.7.1.420
0x21D	TRIM_SAFETY_11		Section 5.7.1.421
0x21E	TRIM_SAFETY_12		Section 5.7.1.422
0x21F	TRIM_SAFETY_13		Section 5.7.1.423
0x220	TRIM_SAFETY_14		Section 5.7.1.424
0x221	TRIM_SAFETY_15		Section 5.7.1.425
0x222	TRIM_SAFETY_16		Section 5.7.1.426
0x223	TRIM_SAFETY_17		Section 5.7.1.427
0x224	TRIM_SAFETY_18		Section 5.7.1.428
0x225	TRIM_SAFETY_19		Section 5.7.1.429
0x226	TRIM_SAFETY_20		Section 5.7.1.430
0x227	TRIM_SAFETY_21		Section 5.7.1.431
0x228	TRIM_SAFETY_22		Section 5.7.1.432
0x229	TRIM_SAFETY_23		Section 5.7.1.433
0x22A	TRIM_SAFETY_24		Section 5.7.1.434
0x22B	TRIM_SAFETY_25		Section 5.7.1.435
0x22C	TRIM_SAFETY_26		Section 5.7.1.436
0x22D	TRIM_SAFETY_27		Section 5.7.1.437
0x22E	TRIM_SAFETY_28		Section 5.7.1.438
0x22F	TRIM_SAFETY_29		Section 5.7.1.439

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x230	TRIM_SAFETY_30		Section 5.7.1.440
0x231	TRIM_SAFETY_31		Section 5.7.1.441
0x232	TRIM_SAFETY_32		Section 5.7.1.442
0x233	TRIM_SAFETY_33		Section 5.7.1.443
0x234	TRIM_SAFETY_34		Section 5.7.1.444
0x235	TRIM_SAFETY_35		Section 5.7.1.445
0x236	TRIM_SAFETY_36		Section 5.7.1.446
0x237	TRIM_SAFETY_37		Section 5.7.1.447
0x238	TRIM_SAFETY_38		Section 5.7.1.448
0x23A	TRIM_VM_VSYS_0		Section 5.7.1.449
0x23B	TRIM_VM_VSYS_1		Section 5.7.1.450
0x23D	TRIM_RTC_0		Section 5.7.1.451
0x23E	TRIM_RTC_1		Section 5.7.1.452
0x23F	TRIM_RTC_2		Section 5.7.1.453
0x245	TRIM_DPLL_0		Section 5.7.1.454
0x247	TRIM_LDO1_0		Section 5.7.1.455
0x248	TRIM_LDO1_1		Section 5.7.1.456
0x249	TRIM_LDO1_2		Section 5.7.1.457
0x24A	TRIM_LDO1_3		Section 5.7.1.458
0x24C	TRIM_LDO2_0		Section 5.7.1.459
0x24D	TRIM_LDO2_1		Section 5.7.1.460
0x24E	TRIM_LDO2_2		Section 5.7.1.461
0x24F	TRIM_LDO2_3		Section 5.7.1.462
0x251	TRIM_LDO3_0		Section 5.7.1.463
0x252	TRIM_LDO3_1		Section 5.7.1.464
0x253	TRIM_LDO3_2		Section 5.7.1.465
0x254	TRIM_LDO3_3		Section 5.7.1.466
0x256	TRIM_LDO4_0		Section 5.7.1.467
0x257	TRIM_LDO4_1		Section 5.7.1.468
0x258	TRIM_LDO4_2		Section 5.7.1.469
0x260	BUCK1_TRIM_REG_0		Section 5.7.1.470
0x261	BUCK1_TRIM_REG_1		Section 5.7.1.471
0x262	BUCK1_TRIM_REG_2		Section 5.7.1.472
0x263	BUCK1_TRIM_REG_3		Section 5.7.1.473
0x264	BUCK1_TRIM_REG_4		Section 5.7.1.474
0x265	BUCK1_TRIM_REG_5		Section 5.7.1.475
0x266	BUCK1_TRIM_REG_6		Section 5.7.1.476
0x267	BUCK1_TRIM_REG_7		Section 5.7.1.477
0x268	BUCK1_TRIM_REG_8		Section 5.7.1.478
0x269	BUCK1_TRIM_REG_9		Section 5.7.1.479
0x26A	BUCK1_TRIM_REG_10		Section 5.7.1.480
0x26B	BUCK1_TRIM_REG_11		Section 5.7.1.481
0x26C	BUCK1_TRIM_REG_12		Section 5.7.1.482
0x26D	BUCK1_TRIM_REG_13		Section 5.7.1.483
0x280	BUCK2_TRIM_REG_0		Section 5.7.1.484
0x281	BUCK2_TRIM_REG_1		Section 5.7.1.485
0x282	BUCK2_TRIM_REG_2		Section 5.7.1.486

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x283	BUCK2_TRIM_REG_3		Section 5.7.1.487
0x284	BUCK2_TRIM_REG_4		Section 5.7.1.488
0x285	BUCK2_TRIM_REG_5		Section 5.7.1.489
0x286	BUCK2_TRIM_REG_6		Section 5.7.1.490
0x287	BUCK2_TRIM_REG_7		Section 5.7.1.491
0x288	BUCK2_TRIM_REG_8		Section 5.7.1.492
0x289	BUCK2_TRIM_REG_9		Section 5.7.1.493
0x28A	BUCK2_TRIM_REG_10		Section 5.7.1.494
0x28B	BUCK2_TRIM_REG_11		Section 5.7.1.495
0x28C	BUCK2_TRIM_REG_12		Section 5.7.1.496
0x28D	BUCK2_TRIM_REG_13		Section 5.7.1.497
0x2A0	BUCK3_TRIM_REG_0		Section 5.7.1.498
0x2A1	BUCK3_TRIM_REG_1		Section 5.7.1.499
0x2A2	BUCK3_TRIM_REG_2		Section 5.7.1.500
0x2A3	BUCK3_TRIM_REG_3		Section 5.7.1.501
0x2A4	BUCK3_TRIM_REG_4		Section 5.7.1.502
0x2A5	BUCK3_TRIM_REG_5		Section 5.7.1.503
0x2A6	BUCK3_TRIM_REG_6		Section 5.7.1.504
0x2A7	BUCK3_TRIM_REG_7		Section 5.7.1.505
0x2A8	BUCK3_TRIM_REG_8		Section 5.7.1.506
0x2A9	BUCK3_TRIM_REG_9		Section 5.7.1.507
0x2AA	BUCK3_TRIM_REG_10		Section 5.7.1.508
0x2AB	BUCK3_TRIM_REG_11		Section 5.7.1.509
0x2AC	BUCK3_TRIM_REG_12		Section 5.7.1.510
0x2AD	BUCK3_TRIM_REG_13		Section 5.7.1.511
0x2C0	BUCK4_TRIM_REG_0		Section 5.7.1.512
0x2C1	BUCK4_TRIM_REG_1		Section 5.7.1.513
0x2C2	BUCK4_TRIM_REG_2		Section 5.7.1.514
0x2C3	BUCK4_TRIM_REG_3		Section 5.7.1.515
0x2C4	BUCK4_TRIM_REG_4		Section 5.7.1.516
0x2C5	BUCK4_TRIM_REG_5		Section 5.7.1.517
0x2C6	BUCK4_TRIM_REG_6		Section 5.7.1.518
0x2C7	BUCK4_TRIM_REG_7		Section 5.7.1.519
0x2C8	BUCK4_TRIM_REG_8		Section 5.7.1.520
0x2C9	BUCK4_TRIM_REG_9		Section 5.7.1.521
0x2CA	BUCK4_TRIM_REG_10		Section 5.7.1.522
0x2CB	BUCK4_TRIM_REG_11		Section 5.7.1.523
0x2CC	BUCK4_TRIM_REG_12		Section 5.7.1.524
0x2CD	BUCK4_TRIM_REG_13		Section 5.7.1.525
0x2E0	BUCK5_TRIM_REG_0		Section 5.7.1.526
0x2E1	BUCK5_TRIM_REG_1		Section 5.7.1.527
0x2E2	BUCK5_TRIM_REG_2		Section 5.7.1.528
0x2E3	BUCK5_TRIM_REG_3		Section 5.7.1.529
0x2E4	BUCK5_TRIM_REG_4		Section 5.7.1.530
0x2E5	BUCK5_TRIM_REG_5		Section 5.7.1.531
0x2E6	BUCK5_TRIM_REG_6		Section 5.7.1.532
0x2E7	BUCK5_TRIM_REG_7		Section 5.7.1.533

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Table 5-38. TPS6594X_MAP Registers (continued)

Offset	Acronym	Register Name	Section
0x2E8	BUCK5_TRIM_REG_8		Section 5.7.1.534
0x2E9	BUCK5_TRIM_REG_9		Section 5.7.1.535
0x2EA	BUCK5_TRIM_REG_10		Section 5.7.1.536
0x2EB	BUCK5_TRIM_REG_11		Section 5.7.1.537
0x2EC	BUCK5_TRIM_REG_12		Section 5.7.1.538
0x2ED	BUCK5_TRIM_REG_13		Section 5.7.1.539
0x401	WD_ANSWER_REG		Section 5.7.1.540
0x402	WD_QUESTION_ANSW_CNT		Section 5.7.1.541
0x403	WD_WIN1_CFG		Section 5.7.1.542
0x404	WD_WIN2_CFG		Section 5.7.1.543
0x405	WD_LONGWIN_CFG		Section 5.7.1.544
0x406	WD_MODE_REG		Section 5.7.1.545
0x407	WD_QA_CFG		Section 5.7.1.546
0x408	WD_ERR_STATUS		Section 5.7.1.547
0x409	WD_THR_CFG		Section 5.7.1.548
0x40A	WD_FAIL_CNT_REG		Section 5.7.1.549

Complex bit access types are encoded to fit into small table cells. Table 5-39 shows the codes that are used for access types in this section.

Table 5-39. TPS6594x_map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WSelfClrF	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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5.7.1.1 DEV_REV Register (Offset = 0x1) [reset = 0x0]

DEV_REV is shown in Figure 5-68 and described in Table 5-40.

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Figure 5-68. DEV_REV Register

7	6	5	4	3	2	1	0
TI_DEVICE_ID							
R/W-0b							

Table 5-40. DEV_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TI_DEVICE_ID	R/W	0b	TI_DEVICE_ID[7:2] = Device GPN TI_DEVICE_ID[1]: 0 - QM 1 - ASIL TI_DEVICE_ID[0]: 0 - Industrial 1 - Auto

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5.7.1.2 NVM_CODE_1 Register (Offset = 0x2) [reset = 0x0]

NVM_CODE_1 is shown in Figure 5-69 and described in Table 5-41.

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Figure 5-69. NVM_CODE_1 Register

7	6	5	4	3	2	1	0
TI_NVM_ID							
R/W-0b							

Table 5-41. NVM_CODE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TI_NVM_ID	R/W	0b	0x00 - 0xF0 are reserved for TI manufactured NVM variants 0xF1 - 0xFF are reserved for special use 0xF1 = Engineering sample, blank NVM [trim and basic defaults only], customer programmable for engineering use only 0xF2 = Production unit, blank NVM [trim and basic defaults only], customer programmable in volume production 0xF3-FF = Reserved, do not use

5.7.1.3 NVM_CODE_2 Register (Offset = 0x3) [reset = 0x0]

NVM_CODE_2 is shown in Figure 5-70 and described in Table 5-42.

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Figure 5-70. NVM_CODE_2 Register

7	6	5	4	3	2	1	0
TI_NVM_REV							
R/W-0b							

Table 5-42. NVM_CODE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TI_NVM_REV	R/W	0b	NVM revision of the IC

5.7.1.4 BUCK1_CTRL Register (Offset = 0x4) [reset = 0x22]

BUCK1_CTRL is shown in Figure 5-71 and described in Table 5-43.

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Figure 5-71. BUCK1_CTRL Register

7	6	5	4	3	2	1	0
BUCK1_RV_SEL	RESERVED	BUCK1_PLDN	BUCK1_VMON_EN	BUCK1_VSEL	BUCK1_FPWM_MP	BUCK1_FPWM	BUCK1_EN
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b

Table 5-43. BUCK1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_RV_SEL	R/W	0b	Select residual voltage checking for BUCK1 feedback pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6	RESERVED	R/W	0b	
5	BUCK1_PLDN	R/W	1b	Enable output pull-down resistor when BUCK1 is disabled: (Default from NVM memory) 0b = Pull-down resistor disabled 1b = Pull-down resistor enabled
4	BUCK1_VMON_EN	R/W	0b	Enable BUCK1 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0b = OV, UV, SC and ILIM comparators are disabled 1b = OV, UV, SC and ILIM comparators are enabled
3	BUCK1_VSEL	R/W	0b	Select output voltage register for BUCK1: (Default from NVM memory) 0b = BUCK1_VOUT_1 1b = BUCK1_VOUT_2
2	BUCK1_FPWM_MP	R/W	0b	Forces the BUCK1 regulator to operate always in multi-phase and forced PWM operation mode: (Default from NVM memory) 0b = Automatic phase adding and shedding. 1b = Forced to multi-phase operation, all phases in the multi-phase configuration.
1	BUCK1_FPWM	R/W	1b	Forces the BUCK1 regulator to operate in PWM mode: (Default from NVM memory) 0b = Automatic transitions between PFM and PWM modes (AUTO mode). 1b = Forced to PWM operation.
0	BUCK1_EN	R/W	0b	Enable BUCK1 regulator: (Default from NVM memory) 0b = BUCK regulator is disabled 1b = BUCK regulator is enabled

5.7.1.5 BUCK1_CONF Register (Offset = 0x5) [reset = 0x22]

BUCK1_CONF is shown in Figure 5-72 and described in Table 5-44.

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Figure 5-72. BUCK1_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_ILIM			BUCK1_SLEW_RATE		
R/W-0b		R/W-100b			R/W-10b		

Table 5-44. BUCK1_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK1_ILIM	R/W	100b	Sets the switch peak current limit of BUCK1. Can be programmed at any time during operation: (Default from NVM memory) 0b = Reserved 1b = Reserved 10b = 2.5 A 11b = 3.5 A 100b = 4.5 A 101b = 5.5 A 110b = Reserved 111b = Reserved
2:0	BUCK1_SLEW_RATE	R/W	10b	Sets the output voltage slew rate for BUCK1 regulator (rising and falling edges): (Default from NVM memory) 0b = 33 mV/µs 1b = 20 mV/µs 10b = 10 mV/µs 11b = 5.0 mV/µs 100b = 2.5 mV/µs 101b = 1.3 mV/µs 110b = 0.63 mV/µs 111b = 0.31 mV/µs

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5.7.1.6 BUCK2_CTRL Register (Offset = 0x6) [reset = 0x22]

BUCK2_CTRL is shown in Figure 5-73 and described in Table 5-45.

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Figure 5-73. BUCK2_CTRL Register

7	6	5	4	3	2	1	0
BUCK2_RV_SEL	RESERVED	BUCK2_PLDN	BUCK2_VMON_EN	BUCK2_VSEL	RESERVED	BUCK2_FPWM	BUCK2_EN
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b

Table 5-45. BUCK2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_RV_SEL	R/W	0b	Select residual voltage checking for BUCK2 feedback pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6	RESERVED	R/W	0b	
5	BUCK2_PLDN	R/W	1b	Enable output pull-down resistor when BUCK2 is disabled: (Default from NVM memory) 0b = Pull-down resistor disabled 1b = Pull-down resistor enabled
4	BUCK2_VMON_EN	R/W	0b	Enable BUCK2 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0b = OV, UV, SC and ILIM comparators are disabled 1b = OV, UV, SC and ILIM comparators are enabled
3	BUCK2_VSEL	R/W	0b	Select output voltage register for BUCK2: (Default from NVM memory) 0b = BUCK2_VOUT_1 1b = BUCK2_VOUT_2
2	RESERVED	R/W	0b	
1	BUCK2_FPWM	R/W	1b	Forces the BUCK2 regulator to operate in PWM mode: (Default from NVM memory) 0b = Automatic transitions between PFM and PWM modes (AUTO mode). 1b = Forced to PWM operation.
0	BUCK2_EN	R/W	0b	Enable BUCK2 regulator: (Default from NVM memory) 0b = BUCK regulator is disabled 1b = BUCK regulator is enabled

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5.7.1.7 BUCK2_CONF Register (Offset = 0x7) [reset = 0x22]

BUCK2_CONF is shown in Figure 5-74 and described in Table 5-46.

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Figure 5-74. BUCK2_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK2_ILIM			BUCK2_SLEW_RATE		
R/W-0b		R/W-100b			R/W-10b		

Table 5-46. BUCK2_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK2_ILIM	R/W	100b	Sets the switch peak current limit of BUCK2. Can be programmed at any time during operation: (Default from NVM memory) 0b = Reserved 1b = Reserved 10b = 2.5 A 11b = 3.5 A 100b = 4.5 A 101b = 5.5 A 110b = Reserved 111b = Reserved
2:0	BUCK2_SLEW_RATE	R/W	10b	Sets the output voltage slew rate for BUCK2 regulator (rising and falling edges): (Default from NVM memory) 0b = 33 mV/µs 1b = 20 mV/µs 10b = 10 mV/µs 11b = 5.0 mV/µs 100b = 2.5 mV/µs 101b = 1.3 mV/µs 110b = 0.63 mV/µs 111b = 0.31 mV/µs

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5.7.1.8 BUCK3_CTRL Register (Offset = 0x8) [reset = 0x22]

BUCK3_CTRL is shown in Figure 5-75 and described in Table 5-47.

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Figure 5-75. BUCK3_CTRL Register

7	6	5	4	3	2	1	0
BUCK3_RV_SEL	RESERVED	BUCK3_PLDN	BUCK3_VMON_EN	BUCK3_VSEL	BUCK3_FPWM_MP	BUCK3_FPWM	BUCK3_EN
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b

Table 5-47. BUCK3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK3_RV_SEL	R/W	0b	Select residual voltage checking for BUCK3 feedback pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6	RESERVED	R/W	0b	
5	BUCK3_PLDN	R/W	1b	Enable output pull-down resistor when BUCK3 is disabled: (Default from NVM memory) 0b = Pull-down resistor disabled 1b = Pull-down resistor enabled
4	BUCK3_VMON_EN	R/W	0b	Enable BUCK3 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0b = OV, UV, SC and ILIM comparators are disabled 1b = OV, UV, SC and ILIM comparators are enabled
3	BUCK3_VSEL	R/W	0b	Select output voltage register for BUCK3: (Default from NVM memory) 0b = BUCK3_VOUT_1 1b = BUCK3_VOUT_2
2	BUCK3_FPWM_MP	R/W	0b	Forces the BUCK3 regulator to operate always in multi-phase and forced PWM operation mode: (Default from NVM memory) 0b = Automatic phase adding and shedding. 1b = Forced to multi-phase operation, all phases in the multi-phase configuration.
1	BUCK3_FPWM	R/W	1b	Forces the BUCK3 regulator to operate in PWM mode: (Default from NVM memory) 0b = Automatic transitions between PFM and PWM modes (AUTO mode). 1b = Forced to PWM operation.
0	BUCK3_EN	R/W	0b	Enable BUCK3 regulator: (Default from NVM memory) 0b = BUCK regulator is disabled 1b = BUCK regulator is enabled

5.7.1.9 BUCK3_CONF Register (Offset = 0x9) [reset = 0x22]

BUCK3_CONF is shown in Figure 5-76 and described in Table 5-48.

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Figure 5-76. BUCK3_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK3_ILIM			BUCK3_SLEW_RATE		
R/W-0b		R/W-100b			R/W-10b		

Table 5-48. BUCK3_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK3_ILIM	R/W	100b	Sets the switch peak current limit of BUCK3. Can be programmed at any time during operation: (Default from NVM memory) 0b = Reserved 1b = Reserved 10b = 2.5 A 11b = 3.5 A 100b = 4.5 A 101b = 5.5 A 110b = Reserved 111b = Reserved
2:0	BUCK3_SLEW_RATE	R/W	10b	Sets the output voltage slew rate for BUCK3 regulator (rising and falling edges): (Default from NVM memory) 0b = 33 mV/µs 1b = 20 mV/µs 10b = 10 mV/µs 11b = 5.0 mV/µs 100b = 2.5 mV/µs 101b = 1.3 mV/µs 110b = 0.63 mV/µs 111b = 0.31 mV/µs

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5.7.1.10 BUCK4_CTRL Register (Offset = 0xA) [reset = 0x22]

BUCK4_CTRL is shown in Figure 5-77 and described in Table 5-49.

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Figure 5-77. BUCK4_CTRL Register

7	6	5	4	3	2	1	0
BUCK4_RV_SEL	RESERVED	BUCK4_PLDN	BUCK4_VMON_EN	BUCK4_VSEL	RESERVED	BUCK4_FPWM	BUCK4_EN
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b

Table 5-49. BUCK4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_RV_SEL	R/W	0b	Select residual voltage checking for BUCK4 feedback pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6	RESERVED	R/W	0b	
5	BUCK4_PLDN	R/W	1b	Enable output pull-down resistor when BUCK4 is disabled: (Default from NVM memory) 0b = Pull-down resistor disabled 1b = Pull-down resistor enabled
4	BUCK4_VMON_EN	R/W	0b	Enable BUCK4 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0b = OV, UV, SC and ILIM comparators are disabled 1b = OV, UV, SC and ILIM comparators are enabled
3	BUCK4_VSEL	R/W	0b	Select output voltage register for BUCK4: (Default from NVM memory) 0b = BUCK4_VOUT_1 1b = BUCK4_VOUT_2
2	RESERVED	R/W	0b	
1	BUCK4_FPWM	R/W	1b	Forces the BUCK4 regulator to operate in PWM mode: (Default from NVM memory) 0b = Automatic transitions between PFM and PWM modes (AUTO mode). 1b = Forced to PWM operation.
0	BUCK4_EN	R/W	0b	Enable BUCK4 regulator: (Default from NVM memory) 0b = BUCK regulator is disabled 1b = BUCK regulator is enabled

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5.7.1.11 BUCK4_CONF Register (Offset = 0xB) [reset = 0x22]

BUCK4_CONF is shown in Figure 5-78 and described in Table 5-50.

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Figure 5-78. BUCK4_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK4_ILIM			BUCK4_SLEW_RATE		
R/W-0b		R/W-100b			R/W-10b		

Table 5-50. BUCK4_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK4_ILIM	R/W	100b	Sets the switch peak current limit of BUCK4. Can be programmed at any time during operation: (Default from NVM memory) 0b = Reserved 1b = Reserved 10b = 2.5 A 11b = 3.5 A 100b = 4.5 A 101b = 5.5 A 110b = Reserved 111b = Reserved
2:0	BUCK4_SLEW_RATE	R/W	10b	Sets the output voltage slew rate for BUCK4 regulator (rising and falling edges): (Default from NVM memory) 0b = 33 mV/µs 1b = 20 mV/µs 10b = 10 mV/µs 11b = 5.0 mV/µs 100b = 2.5 mV/µs 101b = 1.3 mV/µs 110b = 0.63 mV/µs 111b = 0.31 mV/µs

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5.7.1.12 BUCK5_CTRL Register (Offset = 0xC) [reset = 0x22]

BUCK5_CTRL is shown in Figure 5-79 and described in Table 5-51.

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Figure 5-79. BUCK5_CTRL Register

7	6	5	4	3	2	1	0
BUCK5_RV_SEL	RESERVED	BUCK5_PLDN	BUCK5_VMON_EN	BUCK5_VSEL	RESERVED	BUCK5_FPWM	BUCK5_EN
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b

Table 5-51. BUCK5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK5_RV_SEL	R/W	0b	Select residual voltage checking for BUCK5 feedback pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6	RESERVED	R/W	0b	
5	BUCK5_PLDN	R/W	1b	Enable output pull-down resistor when BUCK5 is disabled: (Default from NVM memory) 0b = Pull-down resistor disabled 1b = Pull-down resistor enabled
4	BUCK5_VMON_EN	R/W	0b	Enable BUCK5 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0b = OV, UV, SC and ILIM comparators are disabled 1b = OV, UV, SC and ILIM comparators are enabled
3	BUCK5_VSEL	R/W	0b	Select output voltage register for BUCK5: (Default from NVM memory) 0b = BUCK5_VOUT_1 1b = BUCK5_VOUT_2
2	RESERVED	R/W	0b	
1	BUCK5_FPWM	R/W	1b	Forces the BUCK5 regulator to operate in PWM mode: (Default from NVM memory) 0b = Automatic transitions between PFM and PWM modes (AUTO mode). 1b = Forced to PWM operation.
0	BUCK5_EN	R/W	0b	Enable BUCK5 regulator: (Default from NVM memory) 0b = BUCK regulator is disabled 1b = BUCK regulator is enabled

5.7.1.13 BUCK5_CONF Register (Offset = 0xD) [reset = 0x22]

BUCK5_CONF is shown in Figure 5-80 and described in Table 5-52.

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Figure 5-80. BUCK5_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK5_ILIM			BUCK5_SLEW_RATE		
R/W-0b		R/W-100b			R/W-10b		

Table 5-52. BUCK5_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK5_ILIM	R/W	100b	Sets the switch peak current limit of BUCK5. Can be programmed at any time during operation: (Default from NVM memory) 0b = Reserved 1b = Reserved 10b = 2.5 A 11b = 3.5 A 100b = Reserved 101b = Reserved 110b = Reserved 111b = Reserved
2:0	BUCK5_SLEW_RATE	R/W	10b	Sets the output voltage slew rate for BUCK5 regulator (rising and falling edges): (Default from NVM memory) 0b = 33 mV/µs 1b = 20 mV/µs 10b = 10 mV/µs 11b = 5.0 mV/µs 100b = 2.5 mV/µs 101b = 1.3 mV/µs 110b = 0.63 mV/µs 111b = 0.31 mV/µs

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5.7.1.14 BUCK1_VOUT_1 Register (Offset = 0xE) [reset = 0x0]

BUCK1_VOUT_1 is shown in Figure 5-81 and described in Table 5-53.

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Figure 5-81. BUCK1_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK1_VSET1							
R/W-0b							

Table 5-53. BUCK1_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK1_VSET1	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

5.7.1.15 BUCK1_VOUT_2 Register (Offset = 0xF) [reset = 0x0]

BUCK1_VOUT_2 is shown in Figure 5-82 and described in Table 5-54.

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Figure 5-82. BUCK1_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK1_VSET2							
R/W-0b							

Table 5-54. BUCK1_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK1_VSET2	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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5.7.1.16 BUCK2_VOUT_1 Register (Offset = 0x10) [reset = 0x0]

BUCK2_VOUT_1 is shown in Figure 5-83 and described in Table 5-55.

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Figure 5-83. BUCK2_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK2_VSET1							
R/W-0b							

Table 5-55. BUCK2_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK2_VSET1	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

5.7.1.17 BUCK2_VOUT_2 Register (Offset = 0x11) [reset = 0x0]

BUCK2_VOUT_2 is shown in Figure 5-84 and described in Table 5-56.

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Figure 5-84. BUCK2_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK2_VSET2							
R/W-0b							

Table 5-56. BUCK2_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK2_VSET2	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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5.7.1.18 BUCK3_VOUT_1 Register (Offset = 0x12) [reset = 0x0]

BUCK3_VOUT_1 is shown in Figure 5-85 and described in Table 5-57.

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Figure 5-85. BUCK3_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK3_VSET1							
R/W-0b							

Table 5-57. BUCK3_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK3_VSET1	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

5.7.1.19 BUCK3_VOUT_2 Register (Offset = 0x13) [reset = 0x0]

BUCK3_VOUT_2 is shown in Figure 5-86 and described in Table 5-58.

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Figure 5-86. BUCK3_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK3_VSET2							
R/W-0b							

Table 5-58. BUCK3_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK3_VSET2	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

ADVANCE INFORMATION

5.7.1.20 BUCK4_VOUT_1 Register (Offset = 0x14) [reset = 0x0]

BUCK4_VOUT_1 is shown in Figure 5-87 and described in Table 5-59.

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Figure 5-87. BUCK4_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK4_VSET1							
R/W-0b							

Table 5-59. BUCK4_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK4_VSET1	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

5.7.1.21 BUCK4_VOUT_2 Register (Offset = 0x15) [reset = 0x0]

BUCK4_VOUT_2 is shown in Figure 5-88 and described in Table 5-60.

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Figure 5-88. BUCK4_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK4_VSET2							
R/W-0b							

Table 5-60. BUCK4_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK4_VSET2	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

ADVANCE INFORMATION

5.7.1.22 BUCK5_VOUT_1 Register (Offset = 0x16) [reset = 0x0]

BUCK5_VOUT_1 is shown in Figure 5-89 and described in Table 5-61.

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Figure 5-89. BUCK5_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK5_VSET1							
R/W-0b							

Table 5-61. BUCK5_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK5_VSET1	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

5.7.1.23 BUCK5_VOUT_2 Register (Offset = 0x17) [reset = 0x0]

BUCK5_VOUT_2 is shown in Figure 5-90 and described in Table 5-62.

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Figure 5-90. BUCK5_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK5_VSET2							
R/W-0b							

Table 5-62. BUCK5_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BUCK5_VSET2	R/W	0b	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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5.7.1.24 BUCK1_PG_WINDOW Register (Offset = 0x18) [reset = 0x0]

BUCK1_PG_WINDOW is shown in Figure 5-91 and described in Table 5-63.

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Figure 5-91. BUCK1_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_UV_THR			BUCK1_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-63. BUCK1_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK1_UV_THR	R/W	0b	Powergood low threshold level for BUCK1: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	BUCK1_OV_THR	R/W	0b	Powergood high threshold level for BUCK1: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

5.7.1.25 BUCK2_PG_WINDOW Register (Offset = 0x19) [reset = 0x0]

BUCK2_PG_WINDOW is shown in Figure 5-92 and described in Table 5-64.

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Figure 5-92. BUCK2_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK2_UV_THR			BUCK2_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-64. BUCK2_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK2_UV_THR	R/W	0b	Powergood low threshold level for BUCK2: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	BUCK2_OV_THR	R/W	0b	Powergood high threshold level for BUCK2: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

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5.7.1.26 BUCK3_PG_WINDOW Register (Offset = 0x1A) [reset = 0x0]

BUCK3_PG_WINDOW is shown in Figure 5-93 and described in Table 5-65.

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Figure 5-93. BUCK3_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK3_UV_THR			BUCK3_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-65. BUCK3_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK3_UV_THR	R/W	0b	Powergood low threshold level for BUCK3: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	BUCK3_OV_THR	R/W	0b	Powergood high threshold level for BUCK3: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

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5.7.1.27 BUCK4_PG_WINDOW Register (Offset = 0x1B) [reset = 0x0]

BUCK4_PG_WINDOW is shown in Figure 5-94 and described in Table 5-66.

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Figure 5-94. BUCK4_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK4_UV_THR			BUCK4_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-66. BUCK4_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK4_UV_THR	R/W	0b	Powergood low threshold level for BUCK4: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	BUCK4_OV_THR	R/W	0b	Powergood high threshold level for BUCK4: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

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5.7.1.28 BUCK5_PG_WINDOW Register (Offset = 0x1C) [reset = 0x0]

BUCK5_PG_WINDOW is shown in Figure 5-95 and described in Table 5-67.

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Figure 5-95. BUCK5_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK5_UV_THR			BUCK5_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-67. BUCK5_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	BUCK5_UV_THR	R/W	0b	Powergood low threshold level for BUCK5: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	BUCK5_OV_THR	R/W	0b	Powergood high threshold level for BUCK5: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

5.7.1.29 LDO1_CTRL Register (Offset = 0x1D) [reset = 0x60]

LDO1_CTRL is shown in Figure 5-96 and described in Table 5-68.

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Figure 5-96. LDO1_CTRL Register

7	6	5	4	3	2	1	0
LDO1_RV_SEL	LDO1_PLDN		LDO1_VMON_EN	RESERVED			LDO1_EN
R/W-0b	R/W-11b		R/W-0b	R/W-0b			R/W-0b

Table 5-68. LDO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO1_RV_SEL	R/W	0b	Select residual voltage checking for LDO1 output pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6:5	LDO1_PLDN	R/W	11b	Enable output pull-down resistor when LDO1 is disabled: (Default from NVM memory) 0b = 50 kOhm 1b = 125 Ohm 10b = 250 Ohm 11b = 500 Ohm
4	LDO1_VMON_EN	R/W	0b	Enable LDO1 OV and UV comparators: (Default from NVM memory) 0b = OV and UV comparators are disabled 1b = OV and UV comparators are enabled.
3:1	RESERVED	R/W	0b	
0	LDO1_EN	R/W	0b	Enable LDO1 regulator: (Default from NVM memory) 0b = LDO1 regulator is disabled 1b = LDO1 regulator is enabled.

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5.7.1.30 LDO2_CTRL Register (Offset = 0x1E) [reset = 0x60]

LDO2_CTRL is shown in Figure 5-97 and described in Table 5-69.

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Figure 5-97. LDO2_CTRL Register

7	6	5	4	3	2	1	0
LDO2_RV_SEL	LDO2_PLDN		LDO2_VMON_EN	RESERVED			LDO2_EN
R/W-0b	R/W-11b		R/W-0b	R/W-0b			R/W-0b

Table 5-69. LDO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_RV_SEL	R/W	0b	Select residual voltage checking for LDO2 output pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6:5	LDO2_PLDN	R/W	11b	Enable output pull-down resistor when LDO2 is disabled: (Default from NVM memory) 0b = 50 kOhm 1b = 125 Ohm 10b = 250 Ohm 11b = 500 Ohm
4	LDO2_VMON_EN	R/W	0b	Enable LDO2 OV and UV comparators: (Default from NVM memory) 0b = OV and UV comparators are disabled 1b = OV and UV comparators are enabled.
3:1	RESERVED	R/W	0b	
0	LDO2_EN	R/W	0b	Enable LDO2 regulator: (Default from NVM memory) 0b = LDO1 regulator is disabled 1b = LDO1 regulator is enabled.

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5.7.1.31 LDO3_CTRL Register (Offset = 0x1F) [reset = 0x60]

LDO3_CTRL is shown in Figure 5-98 and described in Table 5-70.

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Figure 5-98. LDO3_CTRL Register

7	6	5	4	3	2	1	0
LDO3_RV_SEL	LDO3_PLDN		LDO3_VMON_EN	RESERVED			LDO3_EN
R/W-0b	R/W-11b		R/W-0b	R/W-0b			R/W-0b

Table 5-70. LDO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO3_RV_SEL	R/W	0b	Select residual voltage checking for LDO3 output pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6:5	LDO3_PLDN	R/W	11b	Enable output pull-down resistor when LDO3 is disabled: (Default from NVM memory) 0b = 50 kOhm 1b = 125 Ohm 10b = 250 Ohm 11b = 500 Ohm
4	LDO3_VMON_EN	R/W	0b	Enable LDO3 OV and UV comparators: (Default from NVM memory) 0b = OV and UV comparators are disabled 1b = OV and UV comparators are enabled.
3:1	RESERVED	R/W	0b	
0	LDO3_EN	R/W	0b	Enable LDO3 regulator: (Default from NVM memory) 0b = LDO1 regulator is disabled 1b = LDO1 regulator is enabled.

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5.7.1.32 LDO4_CTRL Register (Offset = 0x20) [reset = 0x60]

LDO4_CTRL is shown in Figure 5-99 and described in Table 5-71.

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Figure 5-99. LDO4_CTRL Register

7	6	5	4	3	2	1	0
LDO4_RV_SEL	LDO4_PLDN		LDO4_VMON_EN	RESERVED			LDO4_EN
R/W-0b	R/W-11b		R/W-0b	R/W-0b			R/W-0b

Table 5-71. LDO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_RV_SEL	R/W	0b	Select residual voltage checking for LDO4 output pin. (Default from NVM memory) 0b = Disabled 1b = Enabled
6:5	LDO4_PLDN	R/W	11b	Enable output pull-down resistor when LDO4 is disabled: (Default from NVM memory) 0b = 50 kOhm 1b = 125 Ohm 10b = 250 Ohm 11b = 500 Ohm
4	LDO4_VMON_EN	R/W	0b	Enable LDO4 OV and UV comparators: (Default from NVM memory) 0b = OV and UV comparators are disabled 1b = OV and UV comparators are enabled.
3:1	RESERVED	R/W	0b	
0	LDO4_EN	R/W	0b	Enable LDO4 regulator: (Default from NVM memory) 0b = LDO1 regulator is disabled 1b = LDO1 regulator is enabled.

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5.7.1.33 LDOINT_CTRL Register (Offset = 0x21) [reset = 0x0]

LDOINT_CTRL is shown in Figure 5-100 and described in Table 5-72.

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Figure 5-100. LDOINT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							LDOINT_DIS
R/W-0b							R/WSelfClrF-0b

Table 5-72. LDOINT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	LDOINT_DIS	R/WSelfClrF	0b	Disable LDOINT regulator: 0b = LDOINT regulator is enabled 1b = LDOINT regulator is disabled

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5.7.1.34 LDORTC_CTRL Register (Offset = 0x22) [reset = 0x0]

LDORTC_CTRL is shown in Figure 5-101 and described in Table 5-73.

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Figure 5-101. LDORTC_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							LDORTC_DIS
R/W-0b							R/W-0b

Table 5-73. LDORTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	LDORTC_DIS	R/W	0b	Disable LDORTC regulator: 0b = LDORTC regulator is enabled 1b = LDORTC regulator is disabled

5.7.1.35 LDO1_VOUT Register (Offset = 0x23) [reset = 0x0]

LDO1_VOUT is shown in Figure 5-102 and described in Table 5-74.

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Figure 5-102. LDO1_VOUT Register

7	6	5	4	3	2	1	0
LDO1_BYPASS	LDO1_VSET						RESERVED
R/W-0b	R/W-0b						R/W-0b

Table 5-74. LDO1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO1_BYPASS	R/W	0b	Set LDO1 to bypass mode: (Default from NVM memory) 0b = LDO is set to linear regulator mode. 1b = LDO is set to bypass mode.
6:1	LDO1_VSET	R/W	0b	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)
0	RESERVED	R/W	0b	

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5.7.1.36 LDO2_VOUT Register (Offset = 0x24) [reset = 0x0]

LDO2_VOUT is shown in Figure 5-103 and described in Table 5-75.

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Figure 5-103. LDO2_VOUT Register

7	6	5	4	3	2	1	0
LDO2_BYPASS	LDO2_VSET						RESERVED
R/W-0b	R/W-0b						R/W-0b

Table 5-75. LDO2_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_BYPASS	R/W	0b	Set LDO2 to bypass mode: (Default from NVM memory) 0b = LDO is set to linear regulator mode. 1b = LDO is set to bypass mode.
6:1	LDO2_VSET	R/W	0b	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)
0	RESERVED	R/W	0b	

5.7.1.37 LDO3_VOUT Register (Offset = 0x25) [reset = 0x0]

LDO3_VOUT is shown in Figure 5-104 and described in Table 5-76.

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Figure 5-104. LDO3_VOUT Register

7	6	5	4	3	2	1	0
LDO3_BYPASS	LDO3_VSET						RESERVED
R/W-0b	R/W-0b						R/W-0b

Table 5-76. LDO3_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO3_BYPASS	R/W	0b	Set LDO3 to bypass mode: (Default from NVM memory) 0b = LDO is set to linear regulator mode. 1b = LDO is set to bypass mode.
6:1	LDO3_VSET	R/W	0b	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)
0	RESERVED	R/W	0b	

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5.7.1.38 LDO4_VOUT Register (Offset = 0x26) [reset = 0x0]

LDO4_VOUT is shown in Figure 5-105 and described in Table 5-77.

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Figure 5-105. LDO4_VOUT Register

7	6	5	4	3	2	1	0
RESERVED	LDO4_VSET						
R/W-0b	R/W-0b						

Table 5-77. LDO4_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	LDO4_VSET	R/W	0b	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)

5.7.1.39 LDO1_PG_WINDOW Register (Offset = 0x27) [reset = 0x0]

LDO1_PG_WINDOW is shown in Figure 5-106 and described in Table 5-78.

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Figure 5-106. LDO1_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO1_UV_THR			LDO1_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-78. LDO1_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	LDO1_UV_THR	R/W	0b	Powergood low threshold level for LDO1: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	LDO1_OV_THR	R/W	0b	Powergood high threshold level for LDO1: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

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5.7.1.40 LDO2_PG_WINDOW Register (Offset = 0x28) [reset = 0x0]

LDO2_PG_WINDOW is shown in Figure 5-107 and described in Table 5-79.

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Figure 5-107. LDO2_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO2_UV_THR			LDO2_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-79. LDO2_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	LDO2_UV_THR	R/W	0b	Powergood low threshold level for LDO2: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	LDO2_OV_THR	R/W	0b	Powergood high threshold level for LDO2: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

5.7.1.41 LDO3_PG_WINDOW Register (Offset = 0x29) [reset = 0x0]

LDO3_PG_WINDOW is shown in Figure 5-108 and described in Table 5-80.

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Figure 5-108. LDO3_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO3_UV_THR			LDO3_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-80. LDO3_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	LDO3_UV_THR	R/W	0b	Powergood low threshold level for LDO3: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	LDO3_OV_THR	R/W	0b	Powergood high threshold level for LDO3: Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

ADVANCE INFORMATION

5.7.1.42 LDO4_PG_WINDOW Register (Offset = 0x2A) [reset = 0x0]

LDO4_PG_WINDOW is shown in Figure 5-109 and described in Table 5-81.

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Figure 5-109. LDO4_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO4_UV_THR			LDO4_OV_THR		
R/W-0b		R/W-0b			R/W-0b		

Table 5-81. LDO4_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:3	LDO4_UV_THR	R/W	0b	Powergood low threshold level for LDO4: (Default from NVM memory) 0b = -3% / -30mV 1b = -3.5% / -35 mV 10b = -4% / -40 mV 11b = -5% / -50 mV 100b = -6% / -60 mV 101b = -7% / -70 mV 110b = -8% / -80 mV 111b = -10% / -100mV
2:0	LDO4_OV_THR	R/W	0b	Powergood high threshold level for LDO4: (Default from NVM memory) 0b = +3% / +30mV 1b = +3.5% / +35 mV 10b = +4% / +40 mV 11b = +5% / +50 mV 100b = +6% / +60 mV 101b = +7% / +70 mV 110b = +8% / +80 mV 111b = +10% / +100mV

5.7.1.43 VCCA_VMON_CTRL Register (Offset = 0x2B) [reset = 0x0]

VCCA_VMON_CTRL is shown in Figure 5-110 and described in Table 5-82.

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Figure 5-110. VCCA_VMON_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		VMON_DEGLITCH_SEL	RESERVED				VCCA_VMON_EN
R/W-0b		R/W-0b	R/W-0b				R/W-0b

Table 5-82. VCCA_VMON_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	VMON_DEGLITCH_SEL	R/W	0b	Deglitch time select for BUCKx_VMON, LDOx_VMON and VCCA_VMON (Default from NVM memory) 0b = 4 us 1b = 20 us
4:1	RESERVED	R/W	0b	
0	VCCA_VMON_EN	R/W	0b	Enable VCCA OV and UV comparators: (Default from NVM memory) 0b = OV and UV comparators are disabled 1b = OV and UV comparators are enabled.

ADVANCE INFORMATION

5.7.1.44 VCCA_PG_WINDOW Register (Offset = 0x2C) [reset = 0x0]

VCCA_PG_WINDOW is shown in Figure 5-111 and described in Table 5-83.

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Figure 5-111. VCCA_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED	VCCA_PG_SET	VCCA_UV_THR			VCCA_OV_THR		
R/W-0b	R/W-0b	R/W-0b			R/W-0b		

Table 5-83. VCCA_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	VCCA_PG_SET	R/W	0b	Powergood level for VCCA pin: (Default from NVM memory) 0b = 3.3 V 1b = 5.0 V
5:3	VCCA_UV_THR	R/W	0b	Powergood low threshold level for VCCA pin: (Default from NVM memory) 0b = -3% 1b = -3.5% 10b = -4% 11b = -5% 100b = -6% 101b = -7% 110b = -8% 111b = -10%
2:0	VCCA_OV_THR	R/W	0b	Powergood high threshold level for VCCA pin: (Default from NVM memory) 0b = +3% 1b = +3.5% 10b = +4% 11b = +5% 100b = +6% 101b = +7% 110b = +8% 111b = +10%

ADVANCE INFORMATION

5.7.1.45 GPIO1_CONF Register (Offset = 0x31) [reset = 0xA]

GPIO1_CONF is shown in Figure 5-112 and described in Table 5-84.

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Figure 5-112. GPIO1_CONF Register

7	6	5	4	3	2	1	0
GPIO1_SEL			GPIO1_DEGLITCH_EN	GPIO1_PU_PD_EN	GPIO1_PU_SEL	GPIO1_OD	GPIO1_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-84. GPIO1_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO1_SEL	R/W	0b	GPIO1 signal function: (Default from NVM memory) 0b = GPIO1 1b = SCL_I2C2/CS_SPI 10b = NRSTOUT_SOC 11b = NRSTOUT_SOC 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO1_DEGLITCH_EN	R/W	0b	GPIO1 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO1_PU_PD_EN	R/W	1b	Control for GPIO1 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO1_PU_SEL	R/W	0b	Control for GPIO1 pin pull-up/pull-down resistor: GPIO1_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO1_OD	R/W	1b	GPIO1 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO1_DIR	R/W	0b	GPIO1 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.46 GPIO2_CONF Register (Offset = 0x32) [reset = 0xA]

GPIO2_CONF is shown in Figure 5-113 and described in Table 5-85.

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Figure 5-113. GPIO2_CONF Register

7	6	5	4	3	2	1	0
GPIO2_SEL			GPIO2_DEGLITCH_EN	GPIO2_PU_PD_EN	GPIO2_PU_SEL	GPIO2_OD	GPIO2_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-85. GPIO2_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO2_SEL	R/W	0b	GPIO2 signal function: (Default from NVM memory) 0b = GPIO2 1b = TRIG_WDOG 10b = SDA_I2C2/SDO_SPI 11b = SDA_I2C2/SDO_SPI 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO2_DEGLITCH_EN	R/W	0b	GPIO2 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO2_PU_PD_EN	R/W	1b	Control for GPIO2 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO2_PU_SEL	R/W	0b	Control for GPIO2 pin pull-up/pull-down resistor: GPIO2_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO2_OD	R/W	1b	GPIO2 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO2_DIR	R/W	0b	GPIO2 signal direction: (Default from NVM memory) 0b = Input 1b = Output

5.7.1.47 GPIO3_CONF Register (Offset = 0x33) [reset = 0xA]

GPIO3_CONF is shown in Figure 5-114 and described in Table 5-86.

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Figure 5-114. GPIO3_CONF Register

7	6	5	4	3	2	1	0
GPIO3_SEL			GPIO3_DEGLITCH_EN	GPIO3_PU_PD_EN	GPIO3_PU_SEL	GPIO3_OD	GPIO3_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-86. GPIO3_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO3_SEL	R/W	0b	GPIO3 signal function: (Default from NVM memory) 0b = GPIO3 1b = CLK32KOUT 10b = NERR_SOC 11b = NERR_SOC 100b = NSLEEP1 101b = NSLEEP2 110b = LP_WKUP1 111b = LP_WKUP2
4	GPIO3_DEGLITCH_EN	R/W	0b	GPIO3 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO3_PU_PD_EN	R/W	1b	Control for GPIO3 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO3_PU_SEL	R/W	0b	Control for GPIO3 pin pull-up/pull-down resistor: GPIO3_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO3_OD	R/W	1b	GPIO3 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO3_DIR	R/W	0b	GPIO3 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.48 GPIO4_CONF Register (Offset = 0x34) [reset = 0xA]

GPIO4_CONF is shown in Figure 5-115 and described in Table 5-87.

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Figure 5-115. GPIO4_CONF Register

7	6	5	4	3	2	1	0
GPIO4_SEL			GPIO4_DEGLITCH_EN	GPIO4_PU_PD_EN	GPIO4_PU_SEL	GPIO4_OD	GPIO4_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-87. GPIO4_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO4_SEL	R/W	0b	GPIO4 signal function: (Default from NVM memory) 0b = GPIO4 1b = CLK32KOUT 10b = CLK32KOUT 11b = CLK32KOUT 100b = NSLEEP1 101b = NSLEEP2 110b = LP_WKUP1 111b = LP_WKUP2
4	GPIO4_DEGLITCH_EN	R/W	0b	GPIO4 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO4_PU_PD_EN	R/W	1b	Control for GPIO4 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO4_PU_SEL	R/W	0b	Control for GPIO4 pin pull-up/pull-down resistor: GPIO4_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO4_OD	R/W	1b	GPIO4 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO4_DIR	R/W	0b	GPIO4 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.49 GPIO5_CONF Register (Offset = 0x35) [reset = 0xA]

GPIO5_CONF is shown in Figure 5-116 and described in Table 5-88.

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Figure 5-116. GPIO5_CONF Register

7	6	5	4	3	2	1	0
GPIO5_SEL			GPIO5_DEGLITCH_EN	GPIO5_PU_PD_EN	GPIO5_PU_SEL	GPIO5_OD	GPIO5_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-88. GPIO5_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO5_SEL	R/W	0b	GPIO5 signal function: (Default from NVM memory) 0b = GPIO5 1b = SCLK_SPMI 10b = SCLK_SPMI 11b = SCLK_SPMI 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO5_DEGLITCH_EN	R/W	0b	GPIO5 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO5_PU_PD_EN	R/W	1b	Control for GPIO5 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO5_PU_SEL	R/W	0b	Control for GPIO5 pin pull-up/pull-down resistor: GPIO5_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO5_OD	R/W	1b	GPIO5 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO5_DIR	R/W	0b	GPIO5 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.50 GPIO6_CONF Register (Offset = 0x36) [reset = 0xA]

GPIO6_CONF is shown in Figure 5-117 and described in Table 5-89.

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Figure 5-117. GPIO6_CONF Register

7	6	5	4	3	2	1	0
GPIO6_SEL			GPIO6_DEGLITCH_EN	GPIO6_PU_PD_EN	GPIO6_PU_SEL	GPIO6_OD	GPIO6_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-89. GPIO6_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO6_SEL	R/W	0b	GPIO6 signal function: (Default from NVM memory) 0b = GPIO6 1b = SDATA_SPMI 10b = SDATA_SPMI 11b = SDATA_SPMI 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO6_DEGLITCH_EN	R/W	0b	GPIO6 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO6_PU_PD_EN	R/W	1b	Control for GPIO6 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO6_PU_SEL	R/W	0b	Control for GPIO6 pin pull-up/pull-down resistor: GPIO6_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO6_OD	R/W	1b	GPIO6 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO6_DIR	R/W	0b	GPIO6 signal direction: (Default from NVM memory) 0b = Input 1b = Output

5.7.1.51 GPIO7_CONF Register (Offset = 0x37) [reset = 0xA]

GPIO7_CONF is shown in Figure 5-118 and described in Table 5-90.

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Figure 5-118. GPIO7_CONF Register

7	6	5	4	3	2	1	0
GPIO7_SEL			GPIO7_DEGLITCH_EN	GPIO7_PU_PD_EN	GPIO7_PU_SEL	GPIO7_OD	GPIO7_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-90. GPIO7_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO7_SEL	R/W	0b	GPIO7 signal function: (Default from NVM memory) 0b = GPIO7 1b = NERR_MCU 10b = NERR_MCU 11b = NERR_MCU 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO7_DEGLITCH_EN	R/W	0b	GPIO7 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO7_PU_PD_EN	R/W	1b	Control for GPIO7 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO7_PU_SEL	R/W	0b	Control for GPIO7 pin pull-up/pull-down resistor: GPIO7_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO7_OD	R/W	1b	GPIO7 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO7_DIR	R/W	0b	GPIO7 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.52 GPIO8_CONF Register (Offset = 0x38) [reset = 0xA]

GPIO8_CONF is shown in Figure 5-119 and described in Table 5-91.

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Figure 5-119. GPIO8_CONF Register

7	6	5	4	3	2	1	0
GPIO8_SEL			GPIO8_DEGLITCH_EN	GPIO8_PU_PD_EN	GPIO8_PU_SEL	GPIO8_OD	GPIO8_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-91. GPIO8_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO8_SEL	R/W	0b	GPIO8 signal function: (Default from NVM memory) 0b = GPIO8 1b = CLK32KOUT 10b = SYNCCLKOUT 11b = DISABLE_WDOG 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO8_DEGLITCH_EN	R/W	0b	GPIO8 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO8_PU_PD_EN	R/W	1b	Control for GPIO8 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO8_PU_SEL	R/W	0b	Control for GPIO8 pin pull-up/pull-down resistor: GPIO8_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO8_OD	R/W	1b	GPIO8 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO8_DIR	R/W	0b	GPIO8 signal direction: (Default from NVM memory) 0b = Input 1b = Output

5.7.1.53 GPIO9_CONF Register (Offset = 0x39) [reset = 0xA]

GPIO9_CONF is shown in Figure 5-120 and described in Table 5-92.

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Figure 5-120. GPIO9_CONF Register

7	6	5	4	3	2	1	0
GPIO9_SEL			GPIO9_DEGLITCH_EN	GPIO9_PU_PD_EN	GPIO9_PU_SEL	GPIO9_OD	GPIO9_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-92. GPIO9_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO9_SEL	R/W	0b	GPIO9 signal function: (Default from NVM memory) 0b = GPIO9 1b = PGOOD 10b = DISABLE_WDOG 11b = SYNCCLKOUT 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO9_DEGLITCH_EN	R/W	0b	GPIO9 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO9_PU_PD_EN	R/W	1b	Control for GPIO9 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO9_PU_SEL	R/W	0b	Control for GPIO9 pin pull-up/pull-down resistor: GPIO9_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO9_OD	R/W	1b	GPIO9 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO9_DIR	R/W	0b	GPIO9 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.54 GPIO10_CONF Register (Offset = 0x3A) [reset = 0xA]

GPIO10_CONF is shown in Figure 5-121 and described in Table 5-93.

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Figure 5-121. GPIO10_CONF Register

7	6	5	4	3	2	1	0
GPIO10_SEL			GPIO10_DEGLITCH_EN	GPIO10_PU_PD_EN	GPIO10_PU_SEL	GPIO10_OD	GPIO10_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-93. GPIO10_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO10_SEL	R/W	0b	GPIO10 signal function: (Default from NVM memory) 0b = GPIO10 1b = SYNCCLKIN 10b = SYNCCLKOUT 11b = CLK32KOUT 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO10_DEGLITCH_EN	R/W	0b	GPIO10 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO10_PU_PD_EN	R/W	1b	Control for GPIO10 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO10_PU_SEL	R/W	0b	Control for GPIO10 pin pull-up/pull-down resistor: GPIO10_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO10_OD	R/W	1b	GPIO10 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO10_DIR	R/W	0b	GPIO10 signal direction: (Default from NVM memory) 0b = Input 1b = Output

5.7.1.55 GPIO11_CONF Register (Offset = 0x3B) [reset = 0xA]

GPIO11_CONF is shown in Figure 5-122 and described in Table 5-94.

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Figure 5-122. GPIO11_CONF Register

7	6	5	4	3	2	1	0
GPIO11_SEL			GPIO11_DEGLITCH_EN	GPIO11_PU_PD_EN	GPIO11_PU_SEL	GPIO11_OD	GPIO11_DIR
R/W-0b			R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b

Table 5-94. GPIO11_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	GPIO11_SEL	R/W	0b	GPIO11 signal function: (Default from NVM memory) 0b = GPIO11 1b = TRIG_WDOG 10b = NRSTOUT_SOC 11b = NRSTOUT_SOC 100b = NSLEEP1 101b = NSLEEP2 110b = WKUP1 111b = WKUP2
4	GPIO11_DEGLITCH_EN	R/W	0b	GPIO11 signal deglitch time when signal direction is input: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 8 us deglitch time.
3	GPIO11_PU_PD_EN	R/W	1b	Control for GPIO11 pin pull-up/pull-down resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	GPIO11_PU_SEL	R/W	0b	Control for GPIO11 pin pull-up/pull-down resistor: GPIO11_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	GPIO11_OD	R/W	1b	GPIO11 signal type when configured to output: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output
0	GPIO11_DIR	R/W	0b	GPIO11 signal direction: (Default from NVM memory) 0b = Input 1b = Output

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5.7.1.56 NPWRON_CONF Register (Offset = 0x3C) [reset = 0x88]

NPWRON_CONF is shown in Figure 5-123 and described in Table 5-95.

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Figure 5-123. NPWRON_CONF Register

7	6	5	4	3	2	1	0
NPWRON_SEL		ENABLE_POL	ENABLE_DEGLITCH_EN	ENABLE_PU_PD_EN	ENABLE_PU_SEL	RESERVED	NRSTOUT_OD
R/W-10b		R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b

Table 5-95. NPWRON_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	NPWRON_SEL	R/W	10b	NPWRON/ENABLE signal function: (Default from NVM memory) 0b = ENABLE 1b = NPWRON 10b = None 11b = None
5	ENABLE_POL	R/W	0b	Control for ENABLE pin polarity: (Default from NVM memory) 0b = Active high 1b = Active low
4	ENABLE_DEGLITCH_EN	R/W	0b	NPWRON/ENABLE signal deglitch time: (Default from NVM memory) 0b = No deglitch, only synchronization. 1b = 10 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.
3	ENABLE_PU_PD_EN	R/W	1b	Control for NPWRON/ENABLE pin pull-up resistor: (Default from NVM memory) 0b = Pull-up/pull-down resistor disabled 1b = Pull-up/pull-down resistor enabled
2	ENABLE_PU_SEL	R/W	0b	Control for NPWRON/ENABLE pin pull-down resistor: ENABLE_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0b = Pull-down resistor selected 1b = Pull-up resistor selected
1	RESERVED	R/W	0b	
0	NRSTOUT_OD	R/W	0b	NRSTOUT signal type: (Default from NVM memory) 0b = Push-pull output 1b = Open-drain output

ADVANCE INFORMATION

5.7.1.57 GPIO_OUT_1 Register (Offset = 0x3D) [reset = 0x0]

GPIO_OUT_1 is shown in Figure 5-124 and described in Table 5-96.

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Figure 5-124. GPIO_OUT_1 Register

7	6	5	4	3	2	1	0
GPIO8_OUT	GPIO7_OUT	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-96. GPIO_OUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_OUT	R/W	0b	Control for GPIO8 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
6	GPIO7_OUT	R/W	0b	Control for GPIO7 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
5	GPIO6_OUT	R/W	0b	Control for GPIO6 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
4	GPIO5_OUT	R/W	0b	Control for GPIO5 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
3	GPIO4_OUT	R/W	0b	Control for GPIO4 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
2	GPIO3_OUT	R/W	0b	Control for GPIO3 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
1	GPIO2_OUT	R/W	0b	Control for GPIO2 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
0	GPIO1_OUT	R/W	0b	Control for GPIO1 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High

ADVANCE INFORMATION

5.7.1.58 GPIO_OUT_2 Register (Offset = 0x3E) [reset = 0x0]

GPIO_OUT_2 is shown in Figure 5-125 and described in Table 5-97.

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Figure 5-125. GPIO_OUT_2 Register

7	6	5	4	3	2	1	0
RESERVED					GPIO11_OUT	GPIO10_OUT	GPIO9_OUT
R/W-0b					R/W-0b	R/W-0b	R/W-0b

Table 5-97. GPIO_OUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	GPIO11_OUT	R/W	0b	Control for GPIO11 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
1	GPIO10_OUT	R/W	0b	Control for GPIO10 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High
0	GPIO9_OUT	R/W	0b	Control for GPIO9 signal when configured to GPIO Output: (Default from NVM memory) 0b = Low 1b = High

ADVANCE INFORMATION

5.7.1.59 GPIO_IN_1 Register (Offset = 0x3F) [reset = 0x0]

GPIO_IN_1 is shown in Figure 5-126 and described in Table 5-98.

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Figure 5-126. GPIO_IN_1 Register

7	6	5	4	3	2	1	0
GPIO8_IN	GPIO7_IN	GPIO6_IN	GPIO5_IN	GPIO4_IN	GPIO3_IN	GPIO2_IN	GPIO1_IN
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-98. GPIO_IN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_IN	R	0b	Level of GPIO8 signal: 0b = Low 1b = High
6	GPIO7_IN	R	0b	Level of GPIO7 signal: 0b = Low 1b = High
5	GPIO6_IN	R	0b	Level of GPIO6 signal: 0b = Low 1b = High
4	GPIO5_IN	R	0b	Level of GPIO5 signal: 0b = Low 1b = High
3	GPIO4_IN	R	0b	Level of GPIO4 signal: 0b = Low 1b = High
2	GPIO3_IN	R	0b	Level of GPIO3 signal: 0b = Low 1b = High
1	GPIO2_IN	R	0b	Level of GPIO2 signal: 0b = Low 1b = High
0	GPIO1_IN	R	0b	Level of GPIO1 signal: 0b = Low 1b = High

ADVANCE INFORMATION

5.7.1.60 GPIO_IN_2 Register (Offset = 0x40) [reset = 0x0]

GPIO_IN_2 is shown in Figure 5-127 and described in Table 5-99.

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Figure 5-127. GPIO_IN_2 Register

7	6	5	4	3	2	1	0
RESERVED				NPWRON_IN	GPIO11_IN	GPIO10_IN	GPIO9_IN
R-0b				R-0b	R-0b	R-0b	R-0b

Table 5-99. GPIO_IN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3	NPWRON_IN	R	0b	Level of NPWRON/ENABLE signal: 0b = Low 1b = High
2	GPIO11_IN	R	0b	Level of GPIO11 signal: 0b = Low 1b = High
1	GPIO10_IN	R	0b	Level of GPIO10 signal: 0b = Low 1b = High
0	GPIO9_IN	R	0b	Level of GPIO9 signal: 0b = Low 1b = High

ADVANCE INFORMATION

5.7.1.61 RAIL_SEL_1 Register (Offset = 0x41) [reset = 0x0]

RAIL_SEL_1 is shown in Figure 5-128 and described in Table 5-100.

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Figure 5-128. RAIL_SEL_1 Register

7	6	5	4	3	2	1	0
BUCK4_GRP_SEL		BUCK3_GRP_SEL		BUCK2_GRP_SEL		BUCK1_GRP_SEL	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-100. RAIL_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BUCK4_GRP_SEL	R/W	0b	Rail group selection for BUCK4: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
5:4	BUCK3_GRP_SEL	R/W	0b	Rail group selection for BUCK3: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
3:2	BUCK2_GRP_SEL	R/W	0b	Rail group selection for BUCK2: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
1:0	BUCK1_GRP_SEL	R/W	0b	Rail group selection for BUCK1: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group

ADVANCE INFORMATION

5.7.1.62 RAIL_SEL_2 Register (Offset = 0x42) [reset = 0x0]

RAIL_SEL_2 is shown in Figure 5-129 and described in Table 5-101.

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Figure 5-129. RAIL_SEL_2 Register

7	6	5	4	3	2	1	0
LDO3_GRP_SEL		LDO2_GRP_SEL		LDO1_GRP_SEL		BUCK5_GRP_SEL	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-101. RAIL_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	LDO3_GRP_SEL	R/W	0b	Rail group selection for LDO3: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
5:4	LDO2_GRP_SEL	R/W	0b	Rail group selection for LDO2: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
3:2	LDO1_GRP_SEL	R/W	0b	Rail group selection for LDO1: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
1:0	BUCK5_GRP_SEL	R/W	0b	Rail group selection for BUCK5: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group

5.7.1.63 RAIL_SEL_3 Register (Offset = 0x43) [reset = 0x0]

RAIL_SEL_3 is shown in Figure 5-130 and described in Table 5-102.

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Figure 5-130. RAIL_SEL_3 Register

7	6	5	4	3	2	1	0
RESERVED				VCCA_GRP_SEL		LDO4_GRP_SEL	
R/W-0b				R/W-0b		R/W-0b	

Table 5-102. RAIL_SEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	VCCA_GRP_SEL	R/W	0b	Rail group selection for VCCA monitoring: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group
1:0	LDO4_GRP_SEL	R/W	0b	Rail group selection for LDO4: (Default from NVM memory) 0b = No group assigned 1b = MCU rail group 10b = SOC rail group 11b = OTHER rail group

ADVANCE INFORMATION

5.7.1.64 FSM_TRIG_SEL_1 Register (Offset = 0x44) [reset = 0x0]

FSM_TRIG_SEL_1 is shown in Figure 5-131 and described in Table 5-103.

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Figure 5-131. FSM_TRIG_SEL_1 Register

7	6	5	4	3	2	1	0
SEVERE_ERR_TRIG		OTHER_RAIL_TRIG		SOC_RAIL_TRIG		MCU_RAIL_TRIG	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-103. FSM_TRIG_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	SEVERE_ERR_TRIG	R/W	0b	Trigger selection for Severe Error: (Default from NVM memory) 0b = Immediate shutdown 1b = Orderly shutdown 10b = MCU power error 11b = SOC power error
5:4	OTHER_RAIL_TRIG	R/W	0b	Trigger selection for OTHER rail group: (Default from NVM memory) 0b = Immediate shutdown 1b = Orderly shutdown 10b = MCU power error 11b = SOC power error
3:2	SOC_RAIL_TRIG	R/W	0b	Trigger selection for SOC rail group: (Default from NVM memory) 0b = Immediate shutdown 1b = Orderly shutdown 10b = MCU power error 11b = SOC power error
1:0	MCU_RAIL_TRIG	R/W	0b	Trigger selection for MCU rail group: (Default from NVM memory) 0b = Immediate shutdown 1b = Orderly shutdown 10b = MCU power error 11b = SOC power error

ADVANCE INFORMATION

5.7.1.65 FSM_TRIG_SEL_2 Register (Offset = 0x45) [reset = 0x0]

FSM_TRIG_SEL_2 is shown in Figure 5-132 and described in Table 5-104.

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Figure 5-132. FSM_TRIG_SEL_2 Register

7	6	5	4	3	2	1	0
RESERVED						MODERATE_ERR_TRIG	
R/W-0b						R/W-0b	

Table 5-104. FSM_TRIG_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	MODERATE_ERR_TRIG	R/W	0b	Trigger selection for Moderate Error: (Default from NVM memory) 0b = Immediate shutdown 1b = Orderly shutdown 10b = MCU power error 11b = SOC power error

ADVANCE INFORMATION

5.7.1.66 FSM_TRIG_MASK_1 Register (Offset = 0x46) [reset = 0x0]

FSM_TRIG_MASK_1 is shown in Figure 5-133 and described in Table 5-105.

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Figure 5-133. FSM_TRIG_MASK_1 Register

7	6	5	4	3	2	1	0
GPIO4_FSM_MASK_POL	GPIO4_FSM_MASK	GPIO3_FSM_MASK_POL	GPIO3_FSM_MASK	GPIO2_FSM_MASK_POL	GPIO2_FSM_MASK	GPIO1_FSM_MASK_POL	GPIO1_FSM_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-105. FSM_TRIG_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO4_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
6	GPIO4_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
5	GPIO3_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
4	GPIO3_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
3	GPIO2_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
2	GPIO2_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
1	GPIO1_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
0	GPIO1_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked

5.7.1.67 FSM_TRIG_MASK_2 Register (Offset = 0x47) [reset = 0x0]

FSM_TRIG_MASK_2 is shown in Figure 5-134 and described in Table 5-106.

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Figure 5-134. FSM_TRIG_MASK_2 Register

7	6	5	4	3	2	1	0
GPIO8_FSM_MASK_POL	GPIO8_FSM_MASK	GPIO7_FSM_MASK_POL	GPIO7_FSM_MASK	GPIO6_FSM_MASK_POL	GPIO6_FSM_MASK	GPIO5_FSM_MASK_POL	GPIO5_FSM_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-106. FSM_TRIG_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
6	GPIO8_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
5	GPIO7_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
4	GPIO7_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
3	GPIO6_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
2	GPIO6_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
1	GPIO5_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
0	GPIO5_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked

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5.7.1.68 FSM_TRIG_MASK_3 Register (Offset = 0x48) [reset = 0x0]

FSM_TRIG_MASK_3 is shown in Figure 5-135 and described in Table 5-107.

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Figure 5-135. FSM_TRIG_MASK_3 Register

7	6	5	4	3	2	1	0
RESERVED		GPIO11_FSM_MASK_POL	GPIO11_FSM_MASK	GPIO10_FSM_MASK_POL	GPIO10_FSM_MASK	GPIO9_FSM_MASK_POL	GPIO9_FSM_MASK
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-107. FSM_TRIG_MASK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	GPIO11_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
4	GPIO11_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
3	GPIO10_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
2	GPIO10_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked
1	GPIO9_FSM_MASK_POL	R/W	0b	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0b = Masking sets signal value to '0' 1b = Masking sets signal value to '1'
0	GPIO9_FSM_MASK	R/W	0b	FSM trigger mask for GPIOx: (Default from NVM memory) 0b = Not masked 1b = Masked

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5.7.1.69 MASK_BUCK1_2 Register (Offset = 0x49) [reset = 0x0]

MASK_BUCK1_2 is shown in Figure 5-136 and described in Table 5-108.

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Figure 5-136. MASK_BUCK1_2 Register

7	6	5	4	3	2	1	0
BUCK2_ILIM_MASK	RESERVED	BUCK2_UV_MASK	BUCK2_OV_MASK	BUCK1_ILIM_MASK	RESERVED	BUCK1_UV_MASK	BUCK1_OV_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-108. MASK_BUCK1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_ILIM_MASK	R/W	0b	Masking for BUCK2 current monitoring interrupt BUCK2_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	RESERVED	R/W	0b	
5	BUCK2_UV_MASK	R/W	0b	Masking of BUCK2 under-voltage detection interrupt BUCK2_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	BUCK2_OV_MASK	R/W	0b	Masking of BUCK2 over-voltage detection interrupt BUCK2_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	BUCK1_ILIM_MASK	R/W	0b	Masking for BUCK1 current monitoring interrupt BUCK1_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	BUCK1_UV_MASK	R/W	0b	Masking of BUCK1 under-voltage detection interrupt BUCK1_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	BUCK1_OV_MASK	R/W	0b	Masking of BUCK1 over-voltage detection interrupt BUCK1_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.70 MASK_BUCK3_4 Register (Offset = 0x4A) [reset = 0x0]

MASK_BUCK3_4 is shown in Figure 5-137 and described in Table 5-109.

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Figure 5-137. MASK_BUCK3_4 Register

7	6	5	4	3	2	1	0
BUCK4_ILIM_MASK	RESERVED	BUCK4_UV_MASK	BUCK4_OV_MASK	BUCK3_ILIM_MASK	RESERVED	BUCK3_UV_MASK	BUCK3_OV_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-109. MASK_BUCK3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_ILIM_MASK	R/W	0b	Masking for BUCK4 current monitoring interrupt BUCK4_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	RESERVED	R/W	0b	
5	BUCK4_UV_MASK	R/W	0b	Masking of BUCK4 under-voltage detection interrupt BUCK4_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	BUCK4_OV_MASK	R/W	0b	Masking of BUCK4 over-voltage detection interrupt BUCK4_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	BUCK3_ILIM_MASK	R/W	0b	Masking for BUCK3 current monitoring interrupt BUCK3_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	BUCK3_UV_MASK	R/W	0b	Masking of BUCK3 under-voltage detection interrupt BUCK3_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	BUCK3_OV_MASK	R/W	0b	Masking of BUCK3 over-voltage detection interrupt BUCK3_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.71 MASK_BUCK5 Register (Offset = 0x4B) [reset = 0x0]

MASK_BUCK5 is shown in Figure 5-138 and described in Table 5-110.

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Figure 5-138. MASK_BUCK5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_ILIM_MASK	RESERVED	BUCK5_UV_MASK	BUCK5_OV_MASK
R/W-0b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-110. MASK_BUCK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	BUCK5_ILIM_MASK	R/W	0b	Masking for BUCK5 current monitoring interrupt BUCK5_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	BUCK5_UV_MASK	R/W	0b	Masking of BUCK5 under-voltage detection interrupt BUCK5_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	BUCK5_OV_MASK	R/W	0b	Masking of BUCK5 over-voltage detection interrupt BUCK5_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.72 MASK_LDO1_2 Register (Offset = 0x4C) [reset = 0x0]

MASK_LDO1_2 is shown in Figure 5-139 and described in Table 5-111.

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Figure 5-139. MASK_LDO1_2 Register

7	6	5	4	3	2	1	0
LDO2_ILIM_MASK	RESERVED	LDO2_UV_MASK	LDO2_OV_MASK	LDO1_ILIM_MASK	RESERVED	LDO1_UV_MASK	LDO1_OV_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-111. MASK_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_ILIM_MASK	R/W	0b	Masking for LDO2 current monitoring interrupt LDO2_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	RESERVED	R/W	0b	
5	LDO2_UV_MASK	R/W	0b	Masking of LDO2 under-voltage detection interrupt LDO2_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	LDO2_OV_MASK	R/W	0b	Masking of LDO2 over-voltage detection interrupt LDO2_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	LDO1_ILIM_MASK	R/W	0b	Masking for LDO1 current monitoring interrupt LDO1_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	LDO1_UV_MASK	R/W	0b	Masking of LDO1 under-voltage detection interrupt LDO1_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	LDO1_OV_MASK	R/W	0b	Masking of LDO1 over-voltage detection interrupt LDO1_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

5.7.1.73 MASK_LDO3_4 Register (Offset = 0x4D) [reset = 0x0]

MASK_LDO3_4 is shown in Figure 5-140 and described in Table 5-112.

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Figure 5-140. MASK_LDO3_4 Register

7	6	5	4	3	2	1	0
LDO4_ILIM_MASK	RESERVED	LDO4_UV_MASK	LDO4_OV_MASK	LDO3_ILIM_MASK	RESERVED	LDO3_UV_MASK	LDO3_OV_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-112. MASK_LDO3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_ILIM_MASK	R/W	0b	Masking for LDO4 current monitoring interrupt LDO4_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	RESERVED	R/W	0b	
5	LDO4_UV_MASK	R/W	0b	Masking of LDO4 under-voltage detection interrupt LDO4_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	LDO4_OV_MASK	R/W	0b	Masking of LDO4 over-voltage detection interrupt LDO4_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	LDO3_ILIM_MASK	R/W	0b	Masking for LDO3 current monitoring interrupt LDO3_ILIM_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	LDO3_UV_MASK	R/W	0b	Masking of LDO3 under-voltage detection interrupt LDO3_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	LDO3_OV_MASK	R/W	0b	Masking of LDO3 over-voltage detection interrupt LDO3_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.74 MASK_VMON Register (Offset = 0x4E) [reset = 0x0]

MASK_VMON is shown in Figure 5-141 and described in Table 5-113.

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Figure 5-141. MASK_VMON Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_UV_MASK	VCCA_OV_MASK
R/W-0b						R/W-0b	R/W-0b

Table 5-113. MASK_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	VCCA_UV_MASK	R/W	0b	Masking of VCCA under-voltage detection interrupt VCCA_UV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	VCCA_OV_MASK	R/W	0b	Masking of VCCA over-voltage detection interrupt VCCA_OV_INT: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

5.7.1.75 MASK_GPIO1_8_FALL Register (Offset = 0x4F) [reset = 0x0]

MASK_GPIO1_8_FALL is shown in Figure 5-142 and described in Table 5-114.

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Figure 5-142. MASK_GPIO1_8_FALL Register

7	6	5	4	3	2	1	0
GPIO8_FALL_MASK	GPIO7_FALL_MASK	GPIO6_FALL_MASK	GPIO5_FALL_MASK	GPIO4_FALL_MASK	GPIO3_FALL_MASK	GPIO2_FALL_MASK	GPIO1_FALL_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-114. MASK_GPIO1_8_FALL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_FALL_MASK	R/W	0b	Masking of interrupt for GPIO8 low state transition: This bit does not affect GPIO8_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	GPIO7_FALL_MASK	R/W	0b	Masking of interrupt for GPIO7 low state transition: This bit does not affect GPIO7_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
5	GPIO6_FALL_MASK	R/W	0b	Masking of interrupt for GPIO6 low state transition: This bit does not affect GPIO6_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	GPIO5_FALL_MASK	R/W	0b	Masking of interrupt for GPIO5 low state transition: This bit does not affect GPIO5_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	GPIO4_FALL_MASK	R/W	0b	Masking of interrupt for GPIO4 low state transition: This bit does not affect GPIO4_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	GPIO3_FALL_MASK	R/W	0b	Masking of interrupt for GPIO3 low state transition: This bit does not affect GPIO3_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
1	GPIO2_FALL_MASK	R/W	0b	Masking of interrupt for GPIO2 low state transition: This bit does not affect GPIO2_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	GPIO1_FALL_MASK	R/W	0b	Masking of interrupt for GPIO1 low state transition: This bit does not affect GPIO1_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.76 MASK_GPIO1_8_RISE Register (Offset = 0x50) [reset = 0x0]

MASK_GPIO1_8_RISE is shown in Figure 5-143 and described in Table 5-115.

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Figure 5-143. MASK_GPIO1_8_RISE Register

7	6	5	4	3	2	1	0
GPIO8_RISE_MASK	GPIO7_RISE_MASK	GPIO6_RISE_MASK	GPIO5_RISE_MASK	GPIO4_RISE_MASK	GPIO3_RISE_MASK	GPIO2_RISE_MASK	GPIO1_RISE_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-115. MASK_GPIO1_8_RISE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_RISE_MASK	R/W	0b	Masking of interrupt for GPIO8 high state transition: This bit does not affect GPIO8_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	GPIO7_RISE_MASK	R/W	0b	Masking of interrupt for GPIO7 high state transition: This bit does not affect GPIO7_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
5	GPIO6_RISE_MASK	R/W	0b	Masking of interrupt for GPIO6 high state transition: This bit does not affect GPIO6_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	GPIO5_RISE_MASK	R/W	0b	Masking of interrupt for GPIO5 high state transition: This bit does not affect GPIO5_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	GPIO4_RISE_MASK	R/W	0b	Masking of interrupt for GPIO4 high state transition: This bit does not affect GPIO4_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	GPIO3_RISE_MASK	R/W	0b	Masking of interrupt for GPIO3 high state transition: This bit does not affect GPIO3_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
1	GPIO2_RISE_MASK	R/W	0b	Masking of interrupt for GPIO2 high state transition: This bit does not affect GPIO2_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	GPIO1_RISE_MASK	R/W	0b	Masking of interrupt for GPIO1 high state transition: This bit does not affect GPIO1_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

5.7.1.77 MASK_GPIO9_11 Register (Offset = 0x51) [reset = 0x0]

MASK_GPIO9_11 is shown in Figure 5-144 and described in Table 5-116.

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Figure 5-144. MASK_GPIO9_11 Register

7	6	5	4	3	2	1	0
RESERVED		GPIO11_RISE_MASK	GPIO10_RISE_MASK	GPIO9_RISE_MASK	GPIO11_FALL_MASK	GPIO10_FALL_MASK	GPIO9_FALL_MASK
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-116. MASK_GPIO9_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	GPIO11_RISE_MASK	R/W	0b	Masking of interrupt for GPIO11 high state transition: This bit does not affect GPIO11_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	GPIO10_RISE_MASK	R/W	0b	Masking of interrupt for GPIO10 high state transition: This bit does not affect GPIO10_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	GPIO9_RISE_MASK	R/W	0b	Masking of interrupt for GPIO9 high state transition: This bit does not affect GPIO9_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	GPIO11_FALL_MASK	R/W	0b	Masking of interrupt for GPIO11 low state transition: This bit does not affect GPIO11_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
1	GPIO10_FALL_MASK	R/W	0b	Masking of interrupt for GPIO10 low state transition: This bit does not affect GPIO10_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	GPIO9_FALL_MASK	R/W	0b	Masking of interrupt for GPIO9 low state transition: This bit does not affect GPIO9_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.78 MASK_STARTUP Register (Offset = 0x52) [reset = 0x0]

MASK_STARTUP is shown in Figure 5-145 and described in Table 5-117.

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Figure 5-145. MASK_STARTUP Register

7	6	5	4	3	2	1	0
RESERVED			FSD_MASK	RESERVED		ENABLE_MASK	NPWRON_START_MASK
R/W-0b			R/W-0b	R/W-0b		R/W-0b	R/W-0b

Table 5-117. MASK_STARTUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	FSD_MASK	R/W	0b	Masking of FSD_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3:2	RESERVED	R/W	0b	
1	ENABLE_MASK	R/W	0b	Masking of ENABLE_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	NPWRON_START_MASK	R/W	0b	Masking of NPWRON_START_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.79 MASK_MISC Register (Offset = 0x53) [reset = 0x0]

MASK_MISC is shown in Figure 5-146 and described in Table 5-118.

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Figure 5-146. MASK_MISC Register

7	6	5	4	3	2	1	0
RESERVED				TWARN_MASK	RESERVED	EXT_CLK_MASK	BIST_PASS_MASK
R/W-0b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-118. MASK_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	TWARN_MASK	R/W	0b	Masking of TWARN_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	EXT_CLK_MASK	R/W	0b	Masking of EXT_CLK_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	BIST_PASS_MASK	R/W	0b	Masking of BIST_PASS_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.80 MASK_MODERATE_ERR Register (Offset = 0x54) [reset = 0x0]

MASK_MODERATE_ERR is shown in Figure 5-147 and described in Table 5-119.

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Figure 5-147. MASK_MODERATE_ERR Register

7	6	5	4	3	2	1	0
NRSTOUT_READBACK_MASK	NINT_READBACK_MASK	NPWRON_LONG_MASK	SPMI_ERR_MASK	RESERVED	REG_CRC_ERR_MASK	BIST_FAIL_MASK	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-119. MASK_MODERATE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NRSTOUT_READBACK_MASK	R/W	0b	Masking of NRSTOUT_READBACK_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	NINT_READBACK_MASK	R/W	0b	Masking of NINT_READBACK_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
5	NPWRON_LONG_MASK	R/W	0b	Masking of NPWRON_LONG_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	SPMI_ERR_MASK	R/W	0b	Masking of SPMI_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	RESERVED	R/W	0b	
2	REG_CRC_ERR_MASK	R/W	0b	Masking of REG_CRC_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
1	BIST_FAIL_MASK	R/W	0b	Masking of BIST_FAIL_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	RESERVED	R/W	0b	

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5.7.1.81 MASK_FSM_ERR Register (Offset = 0x56) [reset = 0x0]

MASK_FSM_ERR is shown in Figure 5-148 and described in Table 5-120.

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Figure 5-148. MASK_FSM_ERR Register

7	6	5	4	3	2	1	0
RESERVED				SOC_PWR_ERR_MASK	MCU_PWR_ERR_MASK	ORD_SHUTDOWN_MASK	IMM_SHUTDOWN_MASK
R/W-0b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-120. MASK_FSM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	SOC_PWR_ERR_MASK	R/W	0b	Masking of SOC_PWR_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	MCU_PWR_ERR_MASK	R/W	0b	Masking of MCU_PWR_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
1	ORD_SHUTDOWN_MASK	R/W	0b	Masking of ORD_SHUTDOWN_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	IMM_SHUTDOWN_MASK	R/W	0b	Masking of IMM_SHUTDOWN_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.82 MASK_COMM_ERR Register (Offset = 0x57) [reset = 0x0]

MASK_COMM_ERR is shown in Figure 5-149 and described in Table 5-121.

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Figure 5-149. MASK_COMM_ERR Register

7	6	5	4	3	2	1	0
I2C2_ADR_ERR_MASK	RESERVED	I2C2_CRC_ERR_MASK	RESERVED	COMM_ADR_ERR_MASK	RESERVED	COMM_CRC_ERR_MASK	COMM_FRM_ERR_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-121. MASK_COMM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C2_ADR_ERR_MASK	R/W	0b	Masking of I2C2_ADR_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
6	RESERVED	R/W	0b	
5	I2C2_CRC_ERR_MASK	R/W	0b	Masking of I2C2_CRC_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	RESERVED	R/W	0b	
3	COMM_ADR_ERR_MASK	R/W	0b	Masking of COMM_ADR_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	RESERVED	R/W	0b	
1	COMM_CRC_ERR_MASK	R/W	0b	Masking of COMM_CRC_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	COMM_FRM_ERR_MASK	R/W	0b	Masking of COMM_FRM_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.83 MASK_READBACK_ERR Register (Offset = 0x58) [reset = 0x0]

MASK_READBACK_ERR is shown in Figure 5-150 and described in Table 5-122.

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Figure 5-150. MASK_READBACK_ERR Register

7	6	5	4	3	2	1	0
RESERVED				NRSTOUT_SOC_READBACK_MASK	RESERVED		EN_DRV_READBACK_MASK
R/W-0b				R/W-0b	R/W-0b		R/W-0b

Table 5-122. MASK_READBACK_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	NRSTOUT_SOC_READBACK_MASK	R/W	0b	Masking of NRSTOUT_SOC_READBACK_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2:1	RESERVED	R/W	0b	
0	EN_DRV_READBACK_MASK	R/W	0b	Masking of EN_DRV_READBACK_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.84 MASK_ESM Register (Offset = 0x59) [reset = 0x0]

MASK_ESM is shown in Figure 5-151 and described in Table 5-123.

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Figure 5-151. MASK_ESM Register

7	6	5	4	3	2	1	0
RESERVED		ESM_MCU_RST_MASK	ESM_MCU_FAIL_MASK	ESM_MCU_PIN_MASK	ESM_SOC_RST_MASK	ESM_SOC_FAIL_MASK	ESM_SOC_PIN_MASK
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-123. MASK_ESM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	ESM_MCU_RST_MASK	R/W	0b	Masking of ESM_MCU_RST_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
4	ESM_MCU_FAIL_MASK	R/W	0b	Masking of ESM_MCU_FAIL_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	ESM_MCU_PIN_MASK	R/W	0b	Masking of ESM_MCU_PIN_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
2	ESM_SOC_RST_MASK	R/W	0b	Masking of ESM_SOC_RST_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
1	ESM_SOC_FAIL_MASK	R/W	0b	Masking of ESM_SOC_FAIL_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
0	ESM_SOC_PIN_MASK	R/W	0b	Masking of ESM_SOC_PIN_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.

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5.7.1.85 INT_TOP Register (Offset = 0x5A) [reset = 0x0]

INT_TOP is shown in Figure 5-152 and described in Table 5-124.

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Figure 5-152. INT_TOP Register

7	6	5	4	3	2	1	0
FSM_ERR_INT	SEVERE_ERR_INT	MODERATE_ERR_INT	MISC_INT	STARTUP_INT	GPIO_INT	LDO_VMON_INT	BUCK_INT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-124. INT_TOP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FSM_ERR_INT	R	0b	Interrupt indicating that INT_FSM_ERR register has pending interrupt. The reason for the interrupt is indicated in INT_FSM_ERR register. This bit is cleared automatically when INT_FSM_ERR register is cleared to 0x00.
6	SEVERE_ERR_INT	R	0b	Interrupt indicating that INT_SEVERE_ERR register has pending interrupt. The reason for the interrupt is indicated in INT_SEVERE_ERR register. This bit is cleared automatically when INT_SEVERE_ERR register is cleared to 0x00.
5	MODERATE_ERR_INT	R	0b	Interrupt indicating that INT_MODERATE_ERR register has pending interrupt. The reason for the interrupt is indicated in INT_MODERATE_ERR register. This bit is cleared automatically when INT_MODERATE_ERR register is cleared to 0x00.
4	MISC_INT	R	0b	Interrupt indicating that INT_MISC register has pending interrupt. The reason for the interrupt is indicated in INT_MISC register. This bit is cleared automatically when INT_MISC register is cleared to 0x00.
3	STARTUP_INT	R	0b	Interrupt indicating that INT_STARTUP register has pending interrupt. The reason for the interrupt is indicated in INT_STARTUP register. This bit is cleared automatically when INT_STARTUP register is cleared to 0x00.
2	GPIO_INT	R	0b	Interrupt indicating that INT_GPIO register has pending interrupt. The reason for the interrupt is indicated in INT_GPIO register. This bit is cleared automatically when INT_GPIO register is cleared to 0x00.
1	LDO_VMON_INT	R	0b	Interrupt indicating that INT_LDO_VMON register has pending interrupt. The reason for the interrupt is indicated in INT_LDO_VMON register. This bit is cleared automatically when INT_LDO_VMON register is cleared to 0x00.
0	BUCK_INT	R	0b	Interrupt indicating that INT_BUCK register has pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.

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5.7.1.86 INT_BUCK Register (Offset = 0x5B) [reset = 0x0]

INT_BUCK is shown in Figure 5-153 and described in Table 5-125.

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Figure 5-153. INT_BUCK Register

7	6	5	4	3	2	1	0
RESERVED					BUCK5_INT	BUCK3_4_INT	BUCK1_2_INT
R-0b					R-0b	R-0b	R-0b

Table 5-125. INT_BUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0b	
2	BUCK5_INT	R	0b	Interrupt indicating that INT_BUCK5 register has pending interrupt. The reason for the interrupt is indicated in INT_BUCK5 register. This bit is cleared automatically when INT_BUCK5 register is cleared to 0x00.
1	BUCK3_4_INT	R	0b	Interrupt indicating that INT_BUCK3_4 register has pending interrupt. This bit is cleared automatically when INT_BUCK3_4 register is cleared to 0x00.
0	BUCK1_2_INT	R	0b	Interrupt indicating that INT_BUCK1_2 register has pending interrupt. This bit is cleared automatically when INT_BUCK1_2 register is cleared to 0x00.

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5.7.1.87 INT_BUCK1_2 Register (Offset = 0x5C) [reset = 0x0]

INT_BUCK1_2 is shown in Figure 5-154 and described in Table 5-126.

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Figure 5-154. INT_BUCK1_2 Register

7	6	5	4	3	2	1	0
BUCK2_ILIM_INT	BUCK2_SC_INT	BUCK2_UV_INT	BUCK2_OV_INT	BUCK1_ILIM_INT	BUCK1_SC_INT	BUCK1_UV_INT	BUCK1_OV_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-126. INT_BUCK1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_ILIM_INT	R/W1C	0b	Latched status bit indicating that BUCK2 output current limit has been triggered. Write 1 to clear.
6	BUCK2_SC_INT	R/W1C	0b	Latched status bit indicating that the BUCK2 output voltage has fallen below 150 mV level during operation or BUCK2 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	BUCK2_UV_INT	R/W1C	0b	Latched status bit indicating that BUCK2 output under-voltage has been detected. Write 1 to clear.
4	BUCK2_OV_INT	R/W1C	0b	Latched status bit indicating that BUCK2 output over-voltage has been detected. Write 1 to clear.
3	BUCK1_ILIM_INT	R/W1C	0b	Latched status bit indicating that BUCK1 output current limit has been triggered. Write 1 to clear.
2	BUCK1_SC_INT	R/W1C	0b	Latched status bit indicating that the BUCK1 output voltage has fallen below 150 mV level during operation or BUCK1 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	BUCK1_UV_INT	R/W1C	0b	Latched status bit indicating that BUCK1 output under-voltage has been detected. Write 1 to clear.
0	BUCK1_OV_INT	R/W1C	0b	Latched status bit indicating that BUCK1 output over-voltage has been detected. Write 1 to clear.

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5.7.1.88 INT_BUCK3_4 Register (Offset = 0x5D) [reset = 0x0]

INT_BUCK3_4 is shown in Figure 5-155 and described in Table 5-127.

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Figure 5-155. INT_BUCK3_4 Register

7	6	5	4	3	2	1	0
BUCK4_ILIM_INT	BUCK4_SC_INT	BUCK4_UV_INT	BUCK4_OV_INT	BUCK3_ILIM_INT	BUCK3_SC_INT	BUCK3_UV_INT	BUCK3_OV_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-127. INT_BUCK3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_ILIM_INT	R/W1C	0b	Latched status bit indicating that BUCK4 output current limit has been triggered. Write 1 to clear.
6	BUCK4_SC_INT	R/W1C	0b	Latched status bit indicating that the BUCK4 output voltage has fallen below 150 mV level during operation or BUCK4 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	BUCK4_UV_INT	R/W1C	0b	Latched status bit indicating that BUCK4 output under-voltage has been detected. Write 1 to clear.
4	BUCK4_OV_INT	R/W1C	0b	Latched status bit indicating that BUCK4 output over-voltage has been detected. Write 1 to clear.
3	BUCK3_ILIM_INT	R/W1C	0b	Latched status bit indicating that BUCK3 output current limit has been triggered. Write 1 to clear.
2	BUCK3_SC_INT	R/W1C	0b	Latched status bit indicating that the BUCK3 output voltage has fallen below 150 mV level during operation or BUCK3 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	BUCK3_UV_INT	R/W1C	0b	Latched status bit indicating that BUCK3 output under-voltage has been detected. Write 1 to clear.
0	BUCK3_OV_INT	R/W1C	0b	Latched status bit indicating that BUCK3 output over-voltage has been detected. Write 1 to clear.

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5.7.1.89 INT_BUCK5 Register (Offset = 0x5E) [reset = 0x0]

INT_BUCK5 is shown in Figure 5-156 and described in Table 5-128.

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Figure 5-156. INT_BUCK5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_ILIM_INT	BUCK5_SC_INT	BUCK5_UV_INT	BUCK5_OV_INT
R/W-0b				R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-128. INT_BUCK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	BUCK5_ILIM_INT	R/W1C	0b	Latched status bit indicating that BUCK5 output current limit has been triggered. Write 1 to clear.
2	BUCK5_SC_INT	R/W1C	0b	Latched status bit indicating that the BUCK5 output voltage has fallen below 150 mV level during operation or BUCK5 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	BUCK5_UV_INT	R/W1C	0b	Latched status bit indicating that BUCK5 output under-voltage has been detected. Write 1 to clear.
0	BUCK5_OV_INT	R/W1C	0b	Latched status bit indicating that BUCK5 output over-voltage has been detected. Write 1 to clear.

ADVANCE INFORMATION

5.7.1.90 INT_LDO_VMON Register (Offset = 0x5F) [reset = 0x0]

INT_LDO_VMON is shown in Figure 5-157 and described in Table 5-129.

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Figure 5-157. INT_LDO_VMON Register

7	6	5	4	3	2	1	0
RESERVED			VCCA_INT	RESERVED		LDO3_4_INT	LDO1_2_INT
R-0b			R-0b	R-0b		R-0b	R-0b

Table 5-129. INT_LDO_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0b	
4	VCCA_INT	R	0b	Interrupt indicating that INT_VMON register has pending interrupt. The reason for the interrupt is indicated in INT_VMON register. This bit is cleared automatically when INT_VMON register is cleared to 0x00.
3:2	RESERVED	R	0b	
1	LDO3_4_INT	R	0b	Interrupt indicating that INT_LDO3_4 register has pending interrupt. This bit is cleared automatically when INT_LDO3_4 register is cleared to 0x00.
0	LDO1_2_INT	R	0b	Interrupt indicating that INT_LDO1_2 register has pending interrupt. This bit is cleared automatically when INT_LDO1_2 register is cleared to 0x00.

5.7.1.91 INT_LDO1_2 Register (Offset = 0x60) [reset = 0x0]

INT_LDO1_2 is shown in Figure 5-158 and described in Table 5-130.

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Figure 5-158. INT_LDO1_2 Register

7	6	5	4	3	2	1	0
LDO2_ILIM_INT	LDO2_SC_INT	LDO2_UV_INT	LDO2_OV_INT	LDO1_ILIM_INT	LDO1_SC_INT	LDO1_UV_INT	LDO1_OV_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-130. INT_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_ILIM_INT	R/W1C	0b	Latched status bit indicating that LDO2 output current limit has been triggered. Write 1 to clear.
6	LDO2_SC_INT	R/W1C	0b	Latched status bit indicating that LDO2 output voltage has fallen below 150 mV level during operation or LDO2 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	LDO2_UV_INT	R/W1C	0b	Latched status bit indicating that LDO2 output under-voltage has been detected. Write 1 to clear.
4	LDO2_OV_INT	R/W1C	0b	Latched status bit indicating that LDO2 output over-voltage has been detected. Write 1 to clear.
3	LDO1_ILIM_INT	R/W1C	0b	Latched status bit indicating that LDO1 output current limit has been triggered. Write 1 to clear.
2	LDO1_SC_INT	R/W1C	0b	Latched status bit indicating that LDO1 output voltage has fallen below 150 mV level during operation or LDO1 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	LDO1_UV_INT	R/W1C	0b	Latched status bit indicating that LDO1 output under-voltage has been detected. Write 1 to clear.
0	LDO1_OV_INT	R/W1C	0b	Latched status bit indicating that LDO1 output over-voltage has been detected. Write 1 to clear.

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5.7.1.92 INT_LDO3_4 Register (Offset = 0x61) [reset = 0x0]

INT_LDO3_4 is shown in Figure 5-159 and described in Table 5-131.

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Figure 5-159. INT_LDO3_4 Register

7	6	5	4	3	2	1	0
LDO4_ILIM_INT	LDO4_SC_INT	LDO4_UV_INT	LDO4_OV_INT	LDO3_ILIM_INT	LDO3_SC_INT	LDO3_UV_INT	LDO3_OV_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-131. INT_LDO3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_ILIM_INT	R/W1C	0b	Latched status bit indicating that LDO4 output current limit has been triggered. Write 1 to clear.
6	LDO4_SC_INT	R/W1C	0b	Latched status bit indicating that LDO4 output voltage has fallen below 150 mV level during operation or LDO4 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	LDO4_UV_INT	R/W1C	0b	Latched status bit indicating that LDO4 output under-voltage has been detected. Write 1 to clear.
4	LDO4_OV_INT	R/W1C	0b	Latched status bit indicating that LDO4 output over-voltage has been detected. Write 1 to clear.
3	LDO3_ILIM_INT	R/W1C	0b	Latched status bit indicating that LDO3 output current limit has been triggered. Write 1 to clear.
2	LDO3_SC_INT	R/W1C	0b	Latched status bit indicating that LDO3 output voltage has fallen below 150 mV level during operation or LDO3 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	LDO3_UV_INT	R/W1C	0b	Latched status bit indicating that LDO3 output under-voltage has been detected. Write 1 to clear.
0	LDO3_OV_INT	R/W1C	0b	Latched status bit indicating that LDO3 output over-voltage has been detected. Write 1 to clear.

5.7.1.93 INT_VMON Register (Offset = 0x62) [reset = 0x0]

INT_VMON is shown in Figure 5-160 and described in Table 5-132.

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Figure 5-160. INT_VMON Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_UV_INT	VCCA_OV_INT
R/W-0b						R/W1C-0b	R/W1C-0b

Table 5-132. INT_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	VCCA_UV_INT	R/W1C	0b	Latched status bit indicating that the VCCA input voltage has decreased below the under-voltage monitoring level. The actual status of the VCCA under-voltage monitoring is indicated by VCCA_UV_STAT bit. Write 1 to clear interrupt.
0	VCCA_OV_INT	R/W1C	0b	Latched status bit indicating that the VCCA input voltage has exceeded the over-voltage detection level. The actual status of the over-voltage is indicated by VCCA_OV_STAT bit. Write 1 to clear interrupt.

ADVANCE INFORMATION

5.7.1.94 INT_GPIO Register (Offset = 0x63) [reset = 0x0]

INT_GPIO is shown in Figure 5-161 and described in Table 5-133.

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Figure 5-161. INT_GPIO Register

7	6	5	4	3	2	1	0
RESERVED				GPIO1_8_INT	GPIO11_INT	GPIO10_INT	GPIO9_INT
R/W-0b				R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-133. INT_GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	GPIO1_8_INT	R	0b	Interrupt indicating that INT_GPIO1_8 has pending interrupt. The reason for the interrupt is indicated in INT_GPIO1_8 register. This bit is cleared automatically when INT_GPIO1_8 register is cleared to 0x00.
2	GPIO11_INT	R/W1C	0b	Latched status bit indicating that GPIO11 has pending interrupt. GPIO11_IN bit in GPIO_IN_2 register shows the status of the GPIO11 signal. Write 1 to clear interrupt.
1	GPIO10_INT	R/W1C	0b	Latched status bit indicating that GPIO10 has pending interrupt. GPIO10_IN bit in GPIO_IN_2 register shows the status of the GPIO10 signal. Write 1 to clear interrupt.
0	GPIO9_INT	R/W1C	0b	Latched status bit indicating that GPIO9 has pending interrupt. GPIO9_IN bit in GPIO_IN_2 register shows the status of the GPIO9 signal. Write 1 to clear interrupt.

5.7.1.95 INT_GPIO1_8 Register (Offset = 0x64) [reset = 0x0]

INT_GPIO1_8 is shown in Figure 5-162 and described in Table 5-134.

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Figure 5-162. INT_GPIO1_8 Register

7	6	5	4	3	2	1	0
GPIO8_INT	GPIO7_INT	GPIO6_INT	GPIO5_INT	GPIO4_INT	GPIO3_INT	GPIO2_INT	GPIO1_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-134. INT_GPIO1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_INT	R/W1C	0b	Latched status bit indicating that GPIO8 has has pending interrupt. GPIO8_IN bit in GPIO_IN_1 register shows the status of the GPIO8 signal. Write 1 to clear interrupt.
6	GPIO7_INT	R/W1C	0b	Latched status bit indicating that GPIO7 has has pending interrupt. GPIO7_IN bit in GPIO_IN_1 register shows the status of the GPIO7 signal. Write 1 to clear interrupt.
5	GPIO6_INT	R/W1C	0b	Latched status bit indicating that GPIO6 has has pending interrupt. GPIO6_IN bit in GPIO_IN_1 register shows the status of the GPIO6 signal. Write 1 to clear interrupt.
4	GPIO5_INT	R/W1C	0b	Latched status bit indicating that GPIO5 has has pending interrupt. GPIO5_IN bit in GPIO_IN_1 register shows the status of the GPIO5 signal. Write 1 to clear interrupt.
3	GPIO4_INT	R/W1C	0b	Latched status bit indicating that GPIO4 has has pending interrupt. GPIO4_IN bit in GPIO_IN_1 register shows the status of the GPIO4 signal. Write 1 to clear interrupt.
2	GPIO3_INT	R/W1C	0b	Latched status bit indicating that GPIO3 has has pending interrupt. GPIO3_IN bit in GPIO_IN_1 register shows the status of the GPIO3 signal. Write 1 to clear interrupt.
1	GPIO2_INT	R/W1C	0b	Latched status bit indicating that GPIO2 has pending interrupt. GPIO2_IN bit in GPIO_IN_1 register shows the status of the GPIO2 signal. Write 1 to clear interrupt.
0	GPIO1_INT	R/W1C	0b	Latched status bit indicating that GPIO1 has pending interrupt. GPIO1_IN bit in GPIO_IN_1 register shows the status of the GPIO1 signal. Write 1 to clear interrupt.

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5.7.1.96 INT_STARTUP Register (Offset = 0x65) [reset = 0x0]

INT_STARTUP is shown in Figure 5-163 and described in Table 5-135.

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Figure 5-163. INT_STARTUP Register

7	6	5	4	3	2	1	0
RESERVED			FSD_INT	RESERVED	RTC_INT	ENABLE_INT	NPWRON_START_INT
R/W-0b			R/W1C-0b	R/W-0b	R-0b	R/W1C-0b	R/W1C-0b

Table 5-135. INT_STARTUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	FSD_INT	R/W1C	0b	Latched status bit indicating that PMIC has started from NO_SUPPLY or BACKUP state (first supply dectection). Write 1 to clear.
3	RESERVED	R/W	0b	
2	RTC_INT	R	0b	Latched status bit indicating that RTC_STATUS register has pending interrupt. This bit is cleared automatically when ALARM and TIMER interrupts are cleared.
1	ENABLE_INT	R/W1C	0b	Latched status bit indicating that ENABLE pin active event has been detected. Write 1 to clear.
0	NPWRON_START_INT	R/W1C	0b	Latched status bit indicating that NPWRON startup event has been detected. Write 1 to clear.

ADVANCE INFORMATION

5.7.1.97 INT_MISC Register (Offset = 0x66) [reset = 0x0]

INT_MISC is shown in Figure 5-164 and described in Table 5-136.

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Figure 5-164. INT_MISC Register

7	6	5	4	3	2	1	0
RESERVED				TWARN_INT	RESERVED	EXT_CLK_INT	BIST_PASS_INT
R/W-0b				R/W1C-0b	R/W-0b	R/W1C-0b	R/W1C-0b

Table 5-136. INT_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	TWARN_INT	R/W1C	0b	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TWARN_STAT bit in STAT_MISC register. Write 1 to clear interrupt.
2	RESERVED	R/W	0b	
1	EXT_CLK_INT	R/W1C	0b	Latched status bit indicating that external clock is not valid. Internal clock is automatically taken into use. Write 1 to clear.
0	BIST_PASS_INT	R/W1C	0b	Latched status bit indicating that BIST has been completed. Write 1 to clear interrupt.

ADVANCE INFORMATION

5.7.1.98 INT_MODERATE_ERR Register (Offset = 0x67) [reset = 0x0]

INT_MODERATE_ERR is shown in Figure 5-165 and described in Table 5-137.

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Figure 5-165. INT_MODERATE_ERR Register

7	6	5	4	3	2	1	0
NRSTOUT_READBACK_INT	NINT_READBACK_INT	NPWRON_LONG_INT	SPMI_ERR_INT	RECOV_CNT_INT	REG_CRC_ERR_INT	BIST_FAIL_INT	TSD_ORD_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-137. INT_MODERATE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NRSTOUT_READBACK_INT	R/W1C	0b	Latched status bit indicating that NRSTOUT readback error has been detected. Write 1 to clear interrupt.
6	NINT_READBACK_INT	R/W1C	0b	Latched status bit indicating that NINT readback error has been detected. Write 1 to clear interrupt.
5	NPWRON_LONG_INT	R/W1C	0b	Latched status bit indicating that NPWRON long press has been detected. Write 1 to clear.
4	SPMI_ERR_INT	R/W1C	0b	Latched status bit indicating that the SPMI communication interface has detected an error. Write 1 to clear interrupt.
3	RECOV_CNT_INT	R/W1C	0b	Latched status bit indicating that RECOV_CNT has reached the limit (RECOV_CNT_THR). Write 1 to clear.
2	REG_CRC_ERR_INT	R/W1C	0b	Latched status bit indicating that the register CRC checking has detected an error. Write 1 to clear interrupt.
1	BIST_FAIL_INT	R/W1C	0b	Latched status bit indicating that the LBIST or ABIST has detected an error. Write 1 to clear interrupt.
0	TSD_ORD_INT	R/W1C	0b	Latched status bit indicating that the die junction temperature has exceeded the thermal level causing a sequenced shutdown. The regulators have been disabled. The regulators cannot be enabled if this bit is active. The actual status of the temperature is indicated by TSD_ORD_STAT bit in STAT_MODERATE_ERR register. Write 1 to clear interrupt.

5.7.1.99 INT_SEVERE_ERR Register (Offset = 0x68) [reset = 0x0]

INT_SEVERE_ERR is shown in Figure 5-166 and described in Table 5-138.

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Figure 5-166. INT_SEVERE_ERR Register

7	6	5	4	3	2	1	0
RESERVED					PFSM_ERR_INT	VCCA_OVP_INT	TSD_IMM_INT
R/W-0b					R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-138. INT_SEVERE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	PFSM_ERR_INT	R/W1C	0b	Latched status bit indicating that the PFSM sequencer has detected an error. Write 1 to clear interrupt.
1	VCCA_OVP_INT	R/W1C	0b	Latched status bit indicating that the VCCA input voltage has exceeded the over-voltage threshold level causing an immediate shutdown. The regulators have been disabled. Write 1 to clear interrupt.
0	TSD_IMM_INT	R/W1C	0b	Latched status bit indicating that the die junction temperature has exceeded the thermal level causing an immediate shutdown. The regulators have been disabled. The regulators cannot be enabled if this bit is active. The actual status of the temperature is indicated by TSD_IMM_STAT bit in THER_CLK_STATUS register. Write 1 to clear interrupt.

ADVANCE INFORMATION

5.7.1.100 INT_FSM_ERR Register (Offset = 0x69) [reset = 0x0]

INT_FSM_ERR is shown in Figure 5-167 and described in Table 5-139.

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Figure 5-167. INT_FSM_ERR Register

7	6	5	4	3	2	1	0
WD_INT	ESM_INT	READBACK_ERR_INT	COMM_ERR_INT	SOC_PWR_ERR_INT	MCU_PWR_ERR_INT	ORD_SHUTDOWN_INT	IMM_SHUTDOWN_INT
R-0b	R-0b	R-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-139. INT_FSM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_INT	R	0b	Interrupt indicating that WD_ERR_STATUS register has pending interrupt. This bit is cleared automatically when WD_RST_INT, WD_FAIL_INT and WD_LONGWIN_TIMEOUT_INT are cleared.
6	ESM_INT	R	0b	Interrupt indicating that INT_ESM has pending interrupt. This bit is cleared automatically when INT_ESM register is cleared to 0x00.
5	READBACK_ERR_INT	R	0b	Interrupt indicating that INT_READBACK_ERR has pending interrupt. This bit is cleared automatically when INT_READBACK_ERR register is cleared to 0x00.
4	COMM_ERR_INT	R	0b	Interrupt indicating that INT_COMM_ERR has pending interrupt. The reason for the interrupt is indicated in INT_COMM_ERR register. This bit is cleared automatically when INT_COMM_ERR register is cleared to 0x00.
3	SOC_PWR_ERR_INT	R/W1C	0b	Latched status bit indicating that SOC power error has been detected. Write 1 to clear.
2	MCU_PWR_ERR_INT	R/W1C	0b	Latched status bit indicating that MCU power error has been detected. Write 1 to clear.
1	ORD_SHUTDOWN_INT	R/W1C	0b	Latched status bit indicating that orderly shutdown has been detected. Write 1 to clear.
0	IMM_SHUTDOWN_INT	R/W1C	0b	Latched status bit indicating that immediate shutdown has been detected. Write 1 to clear.

5.7.1.101 INT_COMM_ERR Register (Offset = 0x6A) [reset = 0x0]

INT_COMM_ERR is shown in Figure 5-168 and described in Table 5-140.

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Figure 5-168. INT_COMM_ERR Register

7	6	5	4	3	2	1	0
I2C2_ADR_ERR_INT	RESERVED	I2C2_CRC_ERR_INT	RESERVED	COMM_ADR_ERR_INT	RESERVED	COMM_CRC_ERR_INT	COMM_FRM_ERR_INT
R/W1C-0b	R/W-0b	R/W1C-0b	R/W-0b	R/W1C-0b	R/W-0b	R/W1C-0b	R/W1C-0b

Table 5-140. INT_COMM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C2_ADR_ERR_INT	R/W1C	0b	Latched status bit indicating that I2C2 write to non-existing, protected or read-only register address has been detected. Write 1 to clear interrupt.
6	RESERVED	R/W	0b	
5	I2C2_CRC_ERR_INT	R/W1C	0b	Latched status bit indicating that I2C2 CRC error has been detected. Write 1 to clear interrupt.
4	RESERVED	R/W	0b	
3	COMM_ADR_ERR_INT	R/W1C	0b	Latched status bit indicating that I2C1/SPI write to non-existing, protected or read-only register address has been detected. Write 1 to clear interrupt.
2	RESERVED	R/W	0b	
1	COMM_CRC_ERR_INT	R/W1C	0b	Latched status bit indicating that I2C1/SPI CRC error has been detected. Write 1 to clear interrupt.
0	COMM_FRM_ERR_INT	R/W1C	0b	Latched status bit indicating that SPI frame error has been detected. Write 1 to clear interrupt.

ADVANCE INFORMATION

5.7.1.102 INT_READBACK_ERR Register (Offset = 0x6B) [reset = 0x0]

INT_READBACK_ERR is shown in Figure 5-169 and described in Table 5-141.

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Figure 5-169. INT_READBACK_ERR Register

7	6	5	4	3	2	1	0
RESERVED				NRSTOUT_SOC_READBACK_INT	RESERVED		EN_DRV_READBACK_INT
R/W-0b				R/W1C-0b	R/W-0b		R/W1C-0b

Table 5-141. INT_READBACK_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	NRSTOUT_SOC_READBACK_INT	R/W1C	0b	Latched status bit indicating that NRSTOUT_SOC readback error has been detected. Write 1 to clear interrupt.
2:1	RESERVED	R/W	0b	
0	EN_DRV_READBACK_INT	R/W1C	0b	Latched status bit indicating that EN_DRV readback error has been detected. Write 1 to clear interrupt.

ADVANCE INFORMATION

5.7.1.103 INT_ESM Register (Offset = 0x6C) [reset = 0x0]

INT_ESM is shown in Figure 5-170 and described in Table 5-142.

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Figure 5-170. INT_ESM Register

7	6	5	4	3	2	1	0
RESERVED		ESM_MCU_RST_INT	ESM_MCU_FAIL_INT	ESM_MCU_PIN_INT	ESM_SOC_RST_INT	ESM_SOC_FAIL_INT	ESM_SOC_PIN_INT
R/W-0b		R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-142. INT_ESM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	ESM_MCU_RST_INT	R/W1C	0b	Latched status bit indicating that MCU ESM reset has been detected. Write 1 to clear interrupt.
4	ESM_MCU_FAIL_INT	R/W1C	0b	Latched status bit indicating that MCU ESM fail has been detected. Write 1 to clear interrupt.
3	ESM_MCU_PIN_INT	R/W1C	0b	Latched status bit indicating that MCU ESM fault has been detected. Write 1 to clear interrupt.
2	ESM_SOC_RST_INT	R/W1C	0b	Latched status bit indicating that SOC ESM reset has been detected. Write 1 to clear interrupt.
1	ESM_SOC_FAIL_INT	R/W1C	0b	Latched status bit indicating that SOC ESM fail has been detected. Write 1 to clear interrupt.
0	ESM_SOC_PIN_INT	R/W1C	0b	Latched status bit indicating that SOC ESM fault has been detected. Write 1 to clear interrupt.

ADVANCE INFORMATION

5.7.1.104 STAT_BUCK1_2 Register (Offset = 0x6D) [reset = 0x0]

STAT_BUCK1_2 is shown in Figure 5-171 and described in Table 5-143.

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Figure 5-171. STAT_BUCK1_2 Register

7	6	5	4	3	2	1	0
BUCK2_ILIM_STAT	RESERVED	BUCK2_UV_STAT	BUCK2_OV_STAT	BUCK1_ILIM_STAT	RESERVED	BUCK1_UV_STAT	BUCK1_OV_STAT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-143. STAT_BUCK1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_ILIM_STAT	R	0b	Status bit indicating that BUCK2 output current is above current limit level.
6	RESERVED	R	0b	
5	BUCK2_UV_STAT	R	0b	Status bit indicating that BUCK2 output voltage is below under-voltage threshold.
4	BUCK2_OV_STAT	R	0b	Status bit indicating that BUCK2 output voltage is above over-voltage threshold.
3	BUCK1_ILIM_STAT	R	0b	Status bit indicating that BUCK1 output current is above current limit level.
2	RESERVED	R	0b	
1	BUCK1_UV_STAT	R	0b	Status bit indicating that BUCK1 output voltage is below under-voltage threshold.
0	BUCK1_OV_STAT	R	0b	Status bit indicating that BUCK1 output voltage is above over-voltage threshold.

5.7.1.105 STAT_BUCK3_4 Register (Offset = 0x6E) [reset = 0x0]

STAT_BUCK3_4 is shown in Figure 5-172 and described in Table 5-144.

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Figure 5-172. STAT_BUCK3_4 Register

7	6	5	4	3	2	1	0
BUCK4_ILIM_STAT	RESERVED	BUCK4_UV_STAT	BUCK4_OV_STAT	BUCK3_ILIM_STAT	RESERVED	BUCK3_UV_STAT	BUCK3_OV_STAT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-144. STAT_BUCK3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_ILIM_STAT	R	0b	Status bit indicating that BUCK4 output current is above current limit level.
6	RESERVED	R	0b	
5	BUCK4_UV_STAT	R	0b	Status bit indicating that BUCK4 output voltage is below under-voltage threshold.
4	BUCK4_OV_STAT	R	0b	Status bit indicating that BUCK4 output voltage is above over-voltage threshold.
3	BUCK3_ILIM_STAT	R	0b	Status bit indicating that BUCK3 output current is above current limit level.
2	RESERVED	R	0b	
1	BUCK3_UV_STAT	R	0b	Status bit indicating that BUCK3 output voltage is below under-voltage threshold.
0	BUCK3_OV_STAT	R	0b	Status bit indicating that BUCK3 output voltage is above over-voltage threshold.

ADVANCE INFORMATION

5.7.1.106 STAT_BUCK5 Register (Offset = 0x6F) [reset = 0x0]

STAT_BUCK5 is shown in Figure 5-173 and described in Table 5-145.

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Figure 5-173. STAT_BUCK5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_ILIM_STAT	RESERVED	BUCK5_UV_STAT	BUCK5_OV_STAT
R-0b				R-0b	R-0b	R-0b	R-0b

Table 5-145. STAT_BUCK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3	BUCK5_ILIM_STAT	R	0b	Status bit indicating that BUCK5 output current is above current limit level.
2	RESERVED	R	0b	
1	BUCK5_UV_STAT	R	0b	Status bit indicating that BUCK5 output voltage is below under-voltage threshold.
0	BUCK5_OV_STAT	R	0b	Status bit indicating that BUCK5 output voltage is above over-voltage threshold.

ADVANCE INFORMATION

5.7.1.107 STAT_LDO1_2 Register (Offset = 0x70) [reset = 0x0]

STAT_LDO1_2 is shown in Figure 5-174 and described in Table 5-146.

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Figure 5-174. STAT_LDO1_2 Register

7	6	5	4	3	2	1	0
LDO2_ILIM_STAT	RESERVED	LDO2_UV_STAT	LDO2_OV_STAT	LDO1_ILIM_STAT	RESERVED	LDO1_UV_STAT	LDO1_OV_STAT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-146. STAT_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_ILIM_STAT	R	0b	Status bit indicating that LDO2 output current is above current limit level.
6	RESERVED	R	0b	
5	LDO2_UV_STAT	R	0b	Status bit indicating that LDO2 output voltage is below under-voltage threshold.
4	LDO2_OV_STAT	R	0b	Status bit indicating that LDO2 output voltage is above over-voltage threshold.
3	LDO1_ILIM_STAT	R	0b	Status bit indicating that LDO1 output current is above current limit level.
2	RESERVED	R	0b	
1	LDO1_UV_STAT	R	0b	Status bit indicating that LDO1 output voltage is below under-voltage threshold.
0	LDO1_OV_STAT	R	0b	Status bit indicating that LDO1 output voltage is above over-voltage threshold.

ADVANCE INFORMATION

5.7.1.108 STAT_LDO3_4 Register (Offset = 0x71) [reset = 0x0]

STAT_LDO3_4 is shown in Figure 5-175 and described in Table 5-147.

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Figure 5-175. STAT_LDO3_4 Register

7	6	5	4	3	2	1	0
LDO4_ILIM_STAT	RESERVED	LDO4_UV_STAT	LDO4_OV_STAT	LDO3_ILIM_STAT	RESERVED	LDO3_UV_STAT	LDO3_OV_STAT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-147. STAT_LDO3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_ILIM_STAT	R	0b	Status bit indicating that LDO4 output current is above current limit level.
6	RESERVED	R	0b	
5	LDO4_UV_STAT	R	0b	Status bit indicating that LDO4 output voltage is below under-voltage threshold.
4	LDO4_OV_STAT	R	0b	Status bit indicating that LDO4 output voltage is above over-voltage threshold.
3	LDO3_ILIM_STAT	R	0b	Status bit indicating that LDO3 output current is above current limit level.
2	RESERVED	R	0b	
1	LDO3_UV_STAT	R	0b	Status bit indicating that LDO3 output voltage is below under-voltage threshold.
0	LDO3_OV_STAT	R	0b	Status bit indicating that LDO3 output voltage is above over-voltage threshold.

5.7.1.109 STAT_VMON Register (Offset = 0x72) [reset = 0x0]

STAT_VMON is shown in Figure 5-176 and described in Table 5-148.

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Figure 5-176. STAT_VMON Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_UV_STAT	VCCA_OV_STAT
R-0b						R-0b	R-0b

Table 5-148. STAT_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0b	
1	VCCA_UV_STAT	R	0b	Status bit indicating that VCCA input voltage is below under-voltage level.
0	VCCA_OV_STAT	R	0b	Status bit indicating that VCCA input voltage is above over-voltage level.

ADVANCE INFORMATION

5.7.1.110 STAT_STARTUP Register (Offset = 0x73) [reset = 0x0]

STAT_STARTUP is shown in Figure 5-177 and described in Table 5-149.

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Figure 5-177. STAT_STARTUP Register

7	6	5	4	3	2	1	0
RESERVED						ENABLE_STAT	RESERVED
R-0b						R-0b	R-0b

Table 5-149. STAT_STARTUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0b	
1	ENABLE_STAT	R	0b	Status bit indicating nPWRON / EN pin status
0	RESERVED	R	0b	

5.7.1.111 STAT_MISC Register (Offset = 0x74) [reset = 0x0]

STAT_MISC is shown in Figure 5-178 and described in Table 5-150.

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Figure 5-178. STAT_MISC Register

7	6	5	4	3	2	1	0
RESERVED				TWARN_STAT	RESERVED	EXT_CLK_STAT	RESERVED
R-0b				R-0b	R-0b	R-0b	R-0b

Table 5-150. STAT_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3	TWARN_STAT	R	0b	Status bit indicating that die junction temperature is above the thermal warning level.
2	RESERVED	R	0b	
1	EXT_CLK_STAT	R	0b	Status bit indicating that external clock is not valid.
0	RESERVED	R	0b	

5.7.1.112 STAT_MODERATE_ERR Register (Offset = 0x75) [reset = 0x0]

STAT_MODERATE_ERR is shown in Figure 5-179 and described in Table 5-151.

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Figure 5-179. STAT_MODERATE_ERR Register

7	6	5	4	3	2	1	0
RESERVED							TSD_ORD_STAT
R-0b							R-0b

Table 5-151. STAT_MODERATE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0b	
0	TSD_ORD_STAT	R	0b	Status bit indicating that the die junction temperature is above the thermal level causing a sequenced shutdown.

5.7.1.113 STAT_SEVERE_ERR Register (Offset = 0x76) [reset = 0x0]

STAT_SEVERE_ERR is shown in Figure 5-180 and described in Table 5-152.

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Figure 5-180. STAT_SEVERE_ERR Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_OVP_STAT	TSD_IMM_STAT
R-0b						R-0b	R-0b

Table 5-152. STAT_SEVERE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0b	
1	VCCA_OVP_STAT	R	0b	Status bit indicating that the VCCA voltage is above overvoltage protection level.
0	TSD_IMM_STAT	R	0b	Status bit indicating that the die junction temperature is above the thermal level causing an immediate shutdown.

ADVANCE INFORMATION

5.7.1.114 STAT_READBACK_ERR Register (Offset = 0x77) [reset = 0x0]

STAT_READBACK_ERR is shown in Figure 5-181 and described in Table 5-153.

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Figure 5-181. STAT_READBACK_ERR Register

7	6	5	4	3	2	1	0
RESERVED				NRSTOUT_SOC_READBACK_STAT	NRSTOUT_READBACK_STAT	NINT_READBACK_STAT	EN_DRV_READBACK_STAT
R-0b				R-0b	R-0b	R-0b	R-0b

Table 5-153. STAT_READBACK_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3	NRSTOUT_SOC_READBACK_STAT	R	0b	Status bit indicating that NRSTOUT_SOC pin output is high and device is driving it low.
2	NRSTOUT_READBACK_STAT	R	0b	Status bit indicating that NRSTOUT pin output is high and device is driving it low.
1	NINT_READBACK_STAT	R	0b	Status bit indicating that NINT pin output is high and device is driving it low.
0	EN_DRV_READBACK_STAT	R	0b	Status bit indicating that EN_DRV pin output is different than driven.

ADVANCE INFORMATION

5.7.1.115 PGOOD_SEL_1 Register (Offset = 0x78) [reset = 0x0]

PGOOD_SEL_1 is shown in Figure 5-182 and described in Table 5-154.

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Figure 5-182. PGOOD_SEL_1 Register

7	6	5	4	3	2	1	0
PGOOD_SEL_BUCK4		PGOOD_SEL_BUCK3		PGOOD_SEL_BUCK2		PGOOD_SEL_BUCK1	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-154. PGOOD_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PGOOD_SEL_BUCK4	R/W	0b	PGOOD signal source control from BUCK4 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit
5:4	PGOOD_SEL_BUCK3	R/W	0b	PGOOD signal source control from BUCK3 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit
3:2	PGOOD_SEL_BUCK2	R/W	0b	PGOOD signal source control from BUCK2 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit
1:0	PGOOD_SEL_BUCK1	R/W	0b	PGOOD signal source control from BUCK1 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit

ADVANCE INFORMATION

5.7.1.116 PGOOD_SEL_2 Register (Offset = 0x79) [reset = 0x0]

PGOOD_SEL_2 is shown in Figure 5-183 and described in Table 5-155.

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Figure 5-183. PGOOD_SEL_2 Register

7	6	5	4	3	2	1	0
RESERVED						PGOOD_SEL_BUCK5	
R/W-0b						R/W-0b	

Table 5-155. PGOOD_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	PGOOD_SEL_BUCK5	R/W	0b	PGOOD signal source control from BUCK5 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit

5.7.1.117 PGOOD_SEL_3 Register (Offset = 0x7A) [reset = 0x0]

PGOOD_SEL_3 is shown in Figure 5-184 and described in Table 5-156.

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Figure 5-184. PGOOD_SEL_3 Register

7	6	5	4	3	2	1	0
PGOOD_SEL_LDO4		PGOOD_SEL_LDO3		PGOOD_SEL_LDO2		PGOOD_SEL_LDO1	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-156. PGOOD_SEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PGOOD_SEL_LDO4	R/W	0b	PGOOD signal source control from LDO4 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit
5:4	PGOOD_SEL_LDO3	R/W	0b	PGOOD signal source control from LDO3 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit
3:2	PGOOD_SEL_LDO2	R/W	0b	PGOOD signal source control from LDO2 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit
1:0	PGOOD_SEL_LDO1	R/W	0b	PGOOD signal source control from LDO1 (Default from NVM memory) 0b = Masked 1b = Powergood threshold voltage 10b = Powergood threshold voltage AND current limit 11b = Powergood threshold voltage AND current limit

ADVANCE INFORMATION

5.7.1.118 PGOOD_SEL_4 Register (Offset = 0x7B) [reset = 0x0]

PGOOD_SEL_4 is shown in Figure 5-185 and described in Table 5-157.

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Figure 5-185. PGOOD_SEL_4 Register

7	6	5	4	3	2	1	0
PGOOD_WINDOW	PGOOD_POL	PGOOD_SEL_NRSTOUT_SOC	PGOOD_SEL_NRSTOUT	PGOOD_SEL_TDIE_WARN	RESERVED		PGOOD_SEL_VCCA
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b		R/W-0b

Table 5-157. PGOOD_SEL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGOOD_WINDOW	R/W	0b	Type of voltage monitoring for PGOOD signal: (Default from NVM memory) 0b = Only undervoltage is monitored 1b = Both undervoltage and overvoltage are monitored
6	PGOOD_POL	R/W	0b	PGOOD signal polarity select: (Default from NVM memory) 0b = PGOOD signal is high when monitored inputs are valid 1b = PGOOD signal is low when monitored inputs are valid
5	PGOOD_SEL_NRSTOUT_SOC	R/W	0b	PGOOD signal source control from nRSTOUT_SOC pin: (Default from NVM memory) 0b = Masked 1b = nRSTOUT_SOC pin low state forces PGOOD signal to low
4	PGOOD_SEL_NRSTOUT	R/W	0b	PGOOD signal source control from nRSTOUT pin: (Default from NVM memory) 0b = Masked 1b = nRSTOUT pin low state forces PGOOD signal to low
3	PGOOD_SEL_TDIE_WARN	R/W	0b	PGOOD signal source control from thermal warning (Default from NVM memory) 0b = Masked 1b = Thermal warning affecting to PGOOD signal
2:1	RESERVED	R/W	0b	
0	PGOOD_SEL_VCCA	R/W	0b	PGOOD signal source control from VCCA monitoring (Default from NVM memory) 0b = Masked 1b = VCCA OV/UV threshold affecting PGOOD signal

ADVANCE INFORMATION

5.7.1.119 PLL_CTRL Register (Offset = 0x7C) [reset = 0x0]

PLL_CTRL is shown in Figure 5-186 and described in Table 5-158.

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Figure 5-186. PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						EXT_CLK_FREQ	
R/W-0b						R/W-0b	

Table 5-158. PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	EXT_CLK_FREQ	R/W	0b	Frequency of the external clock (SYNCCLKIN): See electrical specification for input clock frequency tolerance. (Default from NVM memory) 0b = 1.1 MHz 1b = 2.2 MHz 10b = 4.4 MHz 11b = Reserved

ADVANCE INFORMATION

5.7.1.120 CONFIG_1 Register (Offset = 0x7D) [reset = 0xC0]

CONFIG_1 is shown in Figure 5-187 and described in Table 5-159.

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Figure 5-187. CONFIG_1 Register

7	6	5	4	3	2	1	0
NSLEEP2_MASK	NSLEEP1_MASK	EN_ILIM_FSM_CTRL	I2C2_HS	I2C1_HS	RESERVED		TWARN_LEVEL
R/W-1b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b		R/W-0b

Table 5-159. CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NSLEEP2_MASK	R/W	1b	Masking for NSLEEP2 pin(s) and NSLEEP2B bit: (Default from NVM memory) 0b = NSLEEP2(B) affects FSM state transitions. 1b = NSLEEP2(B) does not affect FSM state transitions.
6	NSLEEP1_MASK	R/W	1b	Masking for NSLEEP1 pin(s) and NSLEEP1B bit: (Default from NVM memory) 0b = NSLEEP1(B) affects FSM state transitions. 1b = NSLEEP1(B) does not affect FSM state transitions.
5	EN_ILIM_FSM_CTRL	R/W	0b	(Default from NVM memory) 0b = Buck/LDO regulators ILIM interrupts do not affect FSM triggers. 1b = Buck/LDO regulators ILIM interrupts affect FSM triggers.
4	I2C2_HS	R/W	0b	Select I2C2 speed (input filter) (Default from NVM memory) 0b = Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code. 1b = Forced to Hs-mode
3	I2C1_HS	R/W	0b	Select I2C1 speed (input filter) (Default from NVM memory) 0b = Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code. 1b = Forced to Hs-mode
2:1	RESERVED	R/W	0b	
0	TWARN_LEVEL	R/W	0b	Thermal warning threshold level. (Default from NVM memory) 0b = 120C 1b = 130C

ADVANCE INFORMATION

5.7.1.121 CONFIG_2 Register (Offset = 0x7E) [reset = 0x0]

CONFIG_2 is shown in Figure 5-188 and described in Table 5-160.

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Figure 5-188. CONFIG_2 Register

7	6	5	4	3	2	1	0
BB_EOC_RDY	RESERVED			BB_VEOC		BB_ICHR	BB_CHARGER_EN
R-0b	R/W-0b			R/W-0b		R/W-0b	R/W-0b

Table 5-160. CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BB_EOC_RDY	R	0b	Backup end of charge indication 0b = Charging active or not enabled 1b = Charger has reached termination voltage set by BB_VEOC register
6:4	RESERVED	R/W	0b	
3:2	BB_VEOC	R/W	0b	End of charge voltage for backup battery charger: (Default from NVM memory) 0b = 2.5V 1b = 2.8V 10b = 3.0V 11b = 3.3V
1	BB_ICHR	R/W	0b	Backup battery charging current: (Default from NVM memory) 0b = 100uA 1b = 500uA
0	BB_CHARGER_EN	R/W	0b	Backup battery charging: 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.122 ENABLE_DRV_REG Register (Offset = 0x80) [reset = 0x0]

ENABLE_DRV_REG is shown in Figure 5-189 and described in Table 5-161.

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Figure 5-189. ENABLE_DRV_REG Register

7	6	5	4	3	2	1	0
RESERVED							ENABLE_DRV
R/W-0b							R/W-0b

Table 5-161. ENABLE_DRV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	ENABLE_DRV	R/W	0b	Control for EN_DRV pin: FORCE_EN_DRV_LOW must be 0 to control EN_DRV pin. Otherwise EN_DRV pin is low. 0b = Low 1b = High

5.7.1.123 MISC_CTRL Register (Offset = 0x81) [reset = 0x0]

MISC_CTRL is shown in Figure 5-190 and described in Table 5-162.

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Figure 5-190. MISC_CTRL Register

7	6	5	4	3	2	1	0
SYNCCLKOUT_FREQ_SEL		SEL_EXT_CLK	AMUXOUT_EN	CLKMON_EN	LPM_EN	NRSTOUT_SOC	NRSTOUT
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-162. MISC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	SYNCCLKOUT_FREQ_SEL	R/W	0b	SYNCCLKOUT enable/frequency select: 0b = SYNCCLKOUT off 1b = 1.1 MHz 10b = 2.2 MHz 11b = 4.4 MHz
5	SEL_EXT_CLK	R/W	0b	Selection of external clock: 0b = Forced to internal RC oscillator. 1b = Automatic external clock use when available, interrupt generated if external clock appears or disappears.
4	AMUXOUT_EN	R/W	0b	Control bandgap voltage to AMUXOUT pin. 0b = Disabled 1b = Enabled
3	CLKMON_EN	R/W	0b	Control of internal clock monitoring. 0b = Disabled 1b = Enabled
2	LPM_EN	R/W	0b	Low power mode control. LPM_EN sets device in a low power mode. Intended use case is for the PFSM to set LPM_EN upon entering a deep sleep state. The end objective is to disable the digital oscillator to reduce power consumption. The following functions are disabled when LPM_EN=1. -TSD cycling of all sensors/thresholds -regmap/SRAM CRC continuous checking -SPMI WD NVM_ID request/response polling -Disable clock monitoring 0b = Low power mode disabled 1b = Low power mode enabled
1	NRSTOUT_SOC	R/W	0b	Control for nRSTOUT_SOC signal: 0b = Low 1b = High
0	NRSTOUT	R/W	0b	Control for nRSTOUT signal: 0b = Low 1b = High

ADVANCE INFORMATION

5.7.1.124 ENABLE_DRV_STAT Register (Offset = 0x82) [reset = 0x8]

ENABLE_DRV_STAT is shown in Figure 5-191 and described in Table 5-163.

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Figure 5-191. ENABLE_DRV_STAT Register

7	6	5	4	3	2	1	0
RESERVED			SPMI_LPM_EN	FORCE_EN_DRV_LOW	NRSTOUT_SOC_IN	NRSTOUT_IN	EN_DRV_IN
R/W-0b			R/W-0b	R/W-1b	R-0b	R-0b	R-0b

Table 5-163. ENABLE_DRV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	SPMI_LPM_EN	R/W	0b	This bit is read/write for PFSM and read-only for I2C/SPI SPMI low power mode control. SPMI_LPM_EN sets SPMI in a low power mode which stops SPMI WD (Bus heartbeat). PMICs should enter SPMI_LPM_EN=1 at similar times to prevent SPMI WD failures. Therefore to mitigate clock variations SPMI_LPM_EN=1 should be done early in the sequence. The following functions are disabled when SPMI_LPM_EN=1. -SPMI WD NVM_ID request/response polling 0b = SPMI low power mode disabled 1b = SPMI low power mode enabled
3	FORCE_EN_DRV_LOW	R/W	1b	This bit is read/write for PFSM and read-only for I2C/SPI 0b = ENABLE_DRV bit can be written by I2C/SPI 1b = ENABLE_DRV bit is forced low and cannot be written high by I2C/SPI
2	NRSTOUT_SOC_IN	R	0b	Level of NRSTOUT_SOC pin: 0b = Low 1b = High
1	NRSTOUT_IN	R	0b	Level of NRSTOUT pin: 0b = Low 1b = High
0	EN_DRV_IN	R	0b	Level of EN_DRV pin: 0b = Low 1b = High

ADVANCE INFORMATION

5.7.1.125 RECOV_CNT_REG_1 Register (Offset = 0x83) [reset = 0x0]

RECOV_CNT_REG_1 is shown in Figure 5-192 and described in Table 5-164.

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Figure 5-192. RECOV_CNT_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED				RECOV_CNT			
R-0b				R-0b			

Table 5-164. RECOV_CNT_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	RECOV_CNT	R	0b	Recovery counter status. Counter value is incremented each time PMIC goes through warm reset.

5.7.1.126 RECOV_CNT_REG_2 Register (Offset = 0x84) [reset = 0x0]

RECOV_CNT_REG_2 is shown in Figure 5-193 and described in Table 5-165.

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Figure 5-193. RECOV_CNT_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			RECOV_CNT_CLR	RECOV_CNT_THR			
R/W-0b			R/WSelfClrF-0b	R/W-0b			

Table 5-165. RECOV_CNT_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	RECOV_CNT_CLR	R/WSelfClrF	0b	Recovery counter clear. Write 1 to clear the counter. This bit is automatically set back to 0.
3:0	RECOV_CNT_THR	R/W	0b	Recovery counter threshold value for immediate power-down of all supply rails. (Default from NVM memory)

ADVANCE INFORMATION

5.7.1.127 FSM_I2C_TRIGGERS Register (Offset = 0x85) [reset = 0x0]

FSM_I2C_TRIGGERS is shown in Figure 5-194 and described in Table 5-166.

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Figure 5-194. FSM_I2C_TRIGGERS Register

7	6	5	4	3	2	1	0
TRIGGER_I2C_7	TRIGGER_I2C_6	TRIGGER_I2C_5	TRIGGER_I2C_4	TRIGGER_I2C_3	TRIGGER_I2C_2	TRIGGER_I2C_1	TRIGGER_I2C_0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/WSelfClrF-0b	R/WSelfClrF-0b	R/WSelfClrF-0b	R/WSelfClrF-0b

Table 5-166. FSM_I2C_TRIGGERS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TRIGGER_I2C_7	R/W	0b	Trigger for PFSM program.
6	TRIGGER_I2C_6	R/W	0b	Trigger for PFSM program.
5	TRIGGER_I2C_5	R/W	0b	Trigger for PFSM program.
4	TRIGGER_I2C_4	R/W	0b	Trigger for PFSM program.
3	TRIGGER_I2C_3	R/WSelfClrF	0b	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.
2	TRIGGER_I2C_2	R/WSelfClrF	0b	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.
1	TRIGGER_I2C_1	R/WSelfClrF	0b	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.
0	TRIGGER_I2C_0	R/WSelfClrF	0b	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.

ADVANCE INFORMATION

5.7.1.128 FSM_NSLEEP_TRIGGERS Register (Offset = 0x86) [reset = 0x0]

FSM_NSLEEP_TRIGGERS is shown in Figure 5-195 and described in Table 5-167.

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Figure 5-195. FSM_NSLEEP_TRIGGERS Register

7	6	5	4	3	2	1	0
RESERVED						NSLEEP2B	NSLEEP1B
R/W-0b						R/W-0b	R/W-0b

Table 5-167. FSM_NSLEEP_TRIGGERS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	NSLEEP2B	R/W	0b	Parallel register bit for NSLEEP2 function: 0b = NSLEEP2 low 1b = NSLEEP2 high
0	NSLEEP1B	R/W	0b	Parallel register bit for NSLEEP1 function: 0b = NSLEEP1 low 1b = NSLEEP1 high

ADVANCE INFORMATION

5.7.1.129 BUCK_RESET_REG Register (Offset = 0x87) [reset = 0x0]

BUCK_RESET_REG is shown in Figure 5-196 and described in Table 5-168.

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Figure 5-196. BUCK_RESET_REG Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_RESET	BUCK4_RESET	BUCK3_RESET	BUCK2_RESET	BUCK1_RESET
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-168. BUCK_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_RESET	R/W	0b	Reset signal for Buck logic.
3	BUCK4_RESET	R/W	0b	Reset signal for Buck logic.
2	BUCK3_RESET	R/W	0b	Reset signal for Buck logic.
1	BUCK2_RESET	R/W	0b	Reset signal for Buck logic.
0	BUCK1_RESET	R/W	0b	Reset signal for Buck logic.

ADVANCE INFORMATION

5.7.1.130 SPREAD_SPECTRUM_1 Register (Offset = 0x88) [reset = 0x0]

SPREAD_SPECTRUM_1 is shown in Figure 5-197 and described in Table 5-169.

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Figure 5-197. SPREAD_SPECTRUM_1 Register

7	6	5	4	3	2	1	0
RESERVED					SS_EN	SS_DEPTH	
R/W-0b					R/W-0b	R/W-0b	

Table 5-169. SPREAD_SPECTRUM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	SS_EN	R/W	0b	Spread spectrum enable. (Default from NVM memory) 0b = Spread spectrum disabled 1b = Spread spectrum enabled
1:0	SS_DEPTH	R/W	0b	Spread spectrum modulation depth. (Default from NVM memory) 0b = No modulation 1b = +/- 6.3% 10b = +/- 8.4% 11b = +/- 10.5%

ADVANCE INFORMATION

5.7.1.131 FREQ_SEL Register (Offset = 0x8A) [reset = 0x0]

FREQ_SEL is shown in Figure 5-198 and described in Table 5-170.

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Figure 5-198. FREQ_SEL Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_FREQ_SEL	BUCK4_FREQ_SEL	BUCK3_FREQ_SEL	BUCK2_FREQ_SEL	BUCK1_FREQ_SEL
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-170. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_FREQ_SEL	R/W	0b	Buck5 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on EEPROM configuration. See TRM for details. (Default from NVM memory) 0b = 2.2 MHz 1b = 4.4 MHz
3	BUCK4_FREQ_SEL	R/W	0b	Buck4 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on EEPROM configuration. See TRM for details. (Default from NVM memory) 0b = 2.2 MHz 1b = 4.4 MHz
2	BUCK3_FREQ_SEL	R/W	0b	Buck3 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on EEPROM configuration. See TRM for details. (Default from NVM memory) 0b = 2.2 MHz 1b = 4.4 MHz
1	BUCK2_FREQ_SEL	R/W	0b	Buck2 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on EEPROM configuration. See TRM for details. (Default from NVM memory) 0b = 2.2 MHz 1b = 4.4 MHz
0	BUCK1_FREQ_SEL	R/W	0b	Buck1 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on EEPROM configuration. See TRM for details. (Default from NVM memory) 0b = 2.2 MHz 1b = 4.4 MHz

ADVANCE INFORMATION

5.7.1.132 FSM_STEP_SIZE Register (Offset = 0x8B) [reset = 0x0]

FSM_STEP_SIZE is shown in Figure 5-199 and described in Table 5-171.

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Figure 5-199. FSM_STEP_SIZE Register

7	6	5	4	3	2	1	0
RESERVED			PFSM_DELAY_STEP				
R/W-0b			R/W-0b				

Table 5-171. FSM_STEP_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	PFSM_DELAY_STEP	R/W	0b	Step size for PFSM sequence counter. Step size is 50ns * $2^{PFSM\_DELAY\_STEP}$. (Default from NVM memory)

5.7.1.133 LDO_RV_TIMEOUT_REG_1 Register (Offset = 0x8C) [reset = 0x0]

LDO_RV_TIMEOUT_REG_1 is shown in Figure 5-200 and described in Table 5-172.

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Figure 5-200. LDO_RV_TIMEOUT_REG_1 Register

7	6	5	4	3	2	1	0
LDO2_RV_TIMEOUT				LDO1_RV_TIMEOUT			
R/W-0b				R/W-0b			

Table 5-172. LDO_RV_TIMEOUT_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	LDO2_RV_TIMEOUT	R/W	0b	LDO residual voltage check timeout select. (Default from NVM memory) 0b = 0.5ms 1b = 1ms 10b = 1.5ms 11b = 2ms 100b = 2.5ms 101b = 3ms 110b = 3.5ms 111b = 4ms 1000b = 2ms 1001b = 4ms 1010b = 6ms 1011b = 8ms 1100b = 10ms 1101b = 12ms 1110b = 14ms 1111b = 16ms

ADVANCE INFORMATION

Table 5-172. LDO_RV_TIMEOUT_REG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	LDO1_RV_TIMEOUT	R/W	0b	LDO residual voltage check timeout select. (Default from NVM memory) 0b = 0.5ms 1b = 1ms 10b = 1.5ms 11b = 2ms 100b = 2.5ms 101b = 3ms 110b = 3.5ms 111b = 4ms 1000b = 2ms 1001b = 4ms 1010b = 6ms 1011b = 8ms 1100b = 10ms 1101b = 12ms 1110b = 14ms 1111b = 16ms

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5.7.1.134 LDO_RV_TIMEOUT_REG_2 Register (Offset = 0x8D) [reset = 0x0]

LDO_RV_TIMEOUT_REG_2 is shown in Figure 5-201 and described in Table 5-173.

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Figure 5-201. LDO_RV_TIMEOUT_REG_2 Register

7	6	5	4	3	2	1	0
LDO4_RV_TIMEOUT				LDO3_RV_TIMEOUT			
R/W-0b				R/W-0b			

Table 5-173. LDO_RV_TIMEOUT_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	LDO4_RV_TIMEOUT	R/W	0b	LDO residual voltage check timeout select. (Default from NVM memory) 0b = 0.5ms 1b = 1ms 10b = 1.5ms 11b = 2ms 100b = 2.5ms 101b = 3ms 110b = 3.5ms 111b = 4ms 1000b = 2ms 1001b = 4ms 1010b = 6ms 1011b = 8ms 1100b = 10ms 1101b = 12ms 1110b = 14ms 1111b = 16ms

ADVANCE INFORMATION

Table 5-173. LDO_RV_TIMEOUT_REG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	LDO3_RV_TIMEOUT	R/W	0b	LDO residual voltage check timeout select. (Default from NVM memory) 0b = 0.5ms 1b = 1ms 10b = 1.5ms 11b = 2ms 100b = 2.5ms 101b = 3ms 110b = 3.5ms 111b = 4ms 1000b = 2ms 1001b = 4ms 1010b = 6ms 1011b = 8ms 1100b = 10ms 1101b = 12ms 1110b = 14ms 1111b = 16ms

ADVANCE INFORMATION

5.7.1.135 USER_SPARE_REGS Register (Offset = 0x8E) [reset = 0x0]

USER_SPARE_REGS is shown in Figure 5-202 and described in Table 5-174.

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Figure 5-202. USER_SPARE_REGS Register

7	6	5	4	3	2	1	0
RESERVED				USER_SPARE_4	USER_SPARE_3	USER_SPARE_2	USER_SPARE_1
R/W-0b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-174. USER_SPARE_REGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	USER_SPARE_4	R/W	0b	
2	USER_SPARE_3	R/W	0b	
1	USER_SPARE_2	R/W	0b	
0	USER_SPARE_1	R/W	0b	

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5.7.1.136 ESM_MCU_START_REG Register (Offset = 0x8F) [reset = 0x0]

ESM_MCU_START_REG is shown in Figure 5-203 and described in Table 5-175.

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Figure 5-203. ESM_MCU_START_REG Register

7	6	5	4	3	2	1	0
RESERVED							ESM_MCU_START
R/W-0b							R/W-0b

Table 5-175. ESM_MCU_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	ESM_MCU_START	R/W	0b	Control bit to start the ESM_MCU: 0b = ESM_MCU not started. Device clears ENABLE_DRV bit when bit ESM_MCU_EN=1 1b = ESM_MCU started.

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5.7.1.137 ESM_MCU_DELAY1_REG Register (Offset = 0x90) [reset = 0x0]

ESM_MCU_DELAY1_REG is shown in Figure 5-204 and described in Table 5-176.

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Figure 5-204. ESM_MCU_DELAY1_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_DELAY1							
R/W-0b							

Table 5-176. ESM_MCU_DELAY1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_MCU_DELAY1	R/W	0b	These bits configure the duration of the ESM_MCU delay-1 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

5.7.1.138 ESM_MCU_DELAY2_REG Register (Offset = 0x91) [reset = 0x0]

ESM_MCU_DELAY2_REG is shown in Figure 5-205 and described in Table 5-177.

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Figure 5-205. ESM_MCU_DELAY2_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_DELAY2							
R/W-0b							

Table 5-177. ESM_MCU_DELAY2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_MCU_DELAY2	R/W	0b	These bits configure the duration of the ESM_MCU delay-2 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

5.7.1.139 ESM_MCU_MODE_CFG Register (Offset = 0x92) [reset = 0x0]

ESM_MCU_MODE_CFG is shown in Figure 5-206 and described in Table 5-178.

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Figure 5-206. ESM_MCU_MODE_CFG Register

7	6	5	4	3	2	1	0
ESM_MCU_MODE	ESM_MCU_EN	ESM_MCU_ENDRV	RESERVED	ESM_MCU_ERR_CNT_TH			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-178. ESM_MCU_MODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ESM_MCU_MODE	R/W	0b	This bit selects the mode for the ESM_MCU: These bits can be only be written when control bit ESM_MCU_START=0. 0b = Level Mode 1b = PWM Mode
6	ESM_MCU_EN	R/W	0b	ESM_MCU enable configuration bit: These bits can be only be written when control bit ESM_MCU_START=0. 0b = ESM_MCU disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared 1b = ESM_MCU enabled. MCU can set ENABLE_DRV bit to 1 if: - bit ESM_MCU_START=1, and - (ESM_MCU_FAIL_INT=0 or ESM_MCU_ENDRV=0), and - ESM_MCU_RST_INT=0, and - all other interrupt bits are cleared
5	ESM_MCU_ENDRV	R/W	0b	Configuration bit to select ENABLE_DRV clear on ESM-error for ESM_MCU: These bits can be only be written when control bit ESM_MCU_START=0. 0b = ENABLE_DRV not cleared when ESM_MCU_FAIL_INT=1 1b = ENABLE_DRV cleared when ESM_MCU_FAIL_INT=1
4	RESERVED	R/W	0b	
3:0	ESM_MCU_ERR_CNT_TH	R/W	0b	Configuration bits for the threshold of the ESM_MCU error-counter. The ESM_MCU starts the Error Handling Procedure (see Error Signal Monitor chapter) if ESM_MCU_ERR_CNT[4:0] > ESM_MCU_ERR_CNT_TH[3:0]. These bits can be only be written when control bit ESM_MCU_START=0.

ADVANCE INFORMATION

5.7.1.140 ESM_MCU_HMAX_REG Register (Offset = 0x93) [reset = 0x0]

ESM_MCU_HMAX_REG is shown in Figure 5-207 and described in Table 5-179.

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Figure 5-207. ESM_MCU_HMAX_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_HMAX							
R/W-0b							

Table 5-179. ESM_MCU_HMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_MCU_HMAX	R/W	0b	These bits configure the the maximum high-pulse time-threshold (tHIGH_MAX_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

5.7.1.141 ESM_MCU_HMIN_REG Register (Offset = 0x94) [reset = 0x0]

ESM_MCU_HMIN_REG is shown in Figure 5-208 and described in Table 5-180.

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Figure 5-208. ESM_MCU_HMIN_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_HMIN							
R/W-0b							

Table 5-180. ESM_MCU_HMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_MCU_HMIN	R/W	0b	These bits configure the the minimum high-pulse time-threshold (tHIGH_MIN_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

5.7.1.142 ESM_MCU_LMAX_REG Register (Offset = 0x95) [reset = 0x0]

ESM_MCU_LMAX_REG is shown in Figure 5-209 and described in Table 5-181.

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Figure 5-209. ESM_MCU_LMAX_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_LMAX							
R/W-0b							

Table 5-181. ESM_MCU_LMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_MCU_LMAX	R/W	0b	These bits configure the the maximum low-pulse time-threshold (tLOW_MAX_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

5.7.1.143 ESM_MCU_LMIN_REG Register (Offset = 0x96) [reset = 0x0]

ESM_MCU_LMIN_REG is shown in Figure 5-210 and described in Table 5-182.

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Figure 5-210. ESM_MCU_LMIN_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_LMIN							
R/W-0b							

Table 5-182. ESM_MCU_LMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_MCU_LMIN	R/W	0b	These bits configure the the minimum low-pulse time-threshold (tLOW_MAX_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

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5.7.1.144 ESM_MCU_ERR_CNT_REG Register (Offset = 0x97) [reset = 0x0]

ESM_MCU_ERR_CNT_REG is shown in Figure 5-211 and described in Table 5-183.

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Figure 5-211. ESM_MCU_ERR_CNT_REG Register

7	6	5	4	3	2	1	0
RESERVED			ESM_MCU_ERR_CNT				
R-0b			R-0b				

Table 5-183. ESM_MCU_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0b	
4:0	ESM_MCU_ERR_CNT	R	0b	Status bits to indicate the value of the ESM_MCU Error-Counter. The device clears these bits when ESM_MCU_START bit is 0, or when the device resets the MCU.

5.7.1.145 ESM_SOC_START_REG Register (Offset = 0x98) [reset = 0x0]

ESM_SOC_START_REG is shown in Figure 5-212 and described in Table 5-184.

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Figure 5-212. ESM_SOC_START_REG Register

7	6	5	4	3	2	1	0
RESERVED							ESM_SOC_START
R/W-0b							R/W-0b

Table 5-184. ESM_SOC_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	ESM_SOC_START	R/W	0b	Control bit to start the ESM_SoC: 0b = ESM_SoC not started. Device clears ENABLE_DRV bit when bit ESM_SOC_EN=1 1b = ESM_SoC started

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5.7.1.146 ESM_SOC_DELAY1_REG Register (Offset = 0x99) [reset = 0x0]

ESM_SOC_DELAY1_REG is shown in Figure 5-213 and described in Table 5-185.

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Figure 5-213. ESM_SOC_DELAY1_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_DELAY1							
R/W-0b							

Table 5-185. ESM_SOC_DELAY1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_SOC_DELAY1	R/W	0b	These bits configure the duration of the ESM_SoC delay-1 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

5.7.1.147 ESM_SOC_DELAY2_REG Register (Offset = 0x9A) [reset = 0x0]

ESM_SOC_DELAY2_REG is shown in Figure 5-214 and described in Table 5-186.

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Figure 5-214. ESM_SOC_DELAY2_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_DELAY2							
R/W-0b							

Table 5-186. ESM_SOC_DELAY2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_SOC_DELAY2	R/W	0b	These bits configure the duration of the ESM_SoC delay-2 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

5.7.1.148 ESM_SOC_MODE_CFG Register (Offset = 0x9B) [reset = 0x0]

ESM_SOC_MODE_CFG is shown in Figure 5-215 and described in Table 5-187.

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Figure 5-215. ESM_SOC_MODE_CFG Register

7	6	5	4	3	2	1	0
ESM_SOC_MODE	ESM_SOC_EN	ESM_SOC_ENDRV	RESERVED	ESM_SOC_ERR_CNT_TH			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-187. ESM_SOC_MODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ESM_SOC_MODE	R/W	0b	This bit selects the mode for the ESM_SoC: These bits can be only be written when control bit ESM_SOC_START=0. 0b = Level Mode 1b = PWM Mode
6	ESM_SOC_EN	R/W	0b	ESM_SoC enable configuration bit: These bits can be only be written when control bit ESM_SOC_START=0. 0b = ESM_SoC disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared 1b = ESM_SoC enabled. MCU can set ENABLE_DRV bit to 1 if: - bit ESM_SOC_START=1, and - (ESM_SOC_FAIL_INT=0 or ESM_SOC_ENDRV=0), and - ESM_SOC_RST_INT=0, and - all other interrupt bits are cleared.
5	ESM_SOC_ENDRV	R/W	0b	Configuration bit to select ENABLE_DRV clear on ESM-error for ESM_SoC: These bits can be only be written when control bit ESM_SOC_START=0 0b = ENABLE_DRV not cleared when ESM_SOC_FAIL_INT=1 1b = ENABLE_DRV cleared when ESM_SOC_FAIL_INT=1.
4	RESERVED	R/W	0b	
3:0	ESM_SOC_ERR_CNT_TH	R/W	0b	Configuration bits for the threshold of the ESM_SoC error-counter The ESM_SoC starts the Error Handling Procedure (see Error Signal Monitor chapter) if ESM_SOC_ERR_CNT[4:0] > ESM_SOC_ERR_CNT_TH[3:0]. These bits can be only be written when control bit ESM_SOC_START=0.

5.7.1.149 ESM_SOC_HMAX_REG Register (Offset = 0x9C) [reset = 0x0]

ESM_SOC_HMAX_REG is shown in Figure 5-216 and described in Table 5-188.

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Figure 5-216. ESM_SOC_HMAX_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_HMAX							
R/W-0b							

Table 5-188. ESM_SOC_HMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_SOC_HMAX	R/W	0b	These bits configure the the maximum high-pulse time-threshold (tHIGH_MAX_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

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5.7.1.150 ESM_SOC_HMIN_REG Register (Offset = 0x9D) [reset = 0x0]

ESM_SOC_HMIN_REG is shown in Figure 5-217 and described in Table 5-189.

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Figure 5-217. ESM_SOC_HMIN_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_HMIN							
R/W-0b							

Table 5-189. ESM_SOC_HMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_SOC_HMIN	R/W	0b	These bits configure the the minimum high-pulse time-threshold (tHIGH_MIN_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

5.7.1.151 ESM_SOC_LMAX_REG Register (Offset = 0x9E) [reset = 0x0]

ESM_SOC_LMAX_REG is shown in Figure 5-218 and described in Table 5-190.

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Figure 5-218. ESM_SOC_LMAX_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_LMAX							
R/W-0b							

Table 5-190. ESM_SOC_LMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_SOC_LMAX	R/W	0b	These bits configure the the maximum low-pulse time-threshold (tLOW_MAX_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

5.7.1.152 ESM_SOC_LMIN_REG Register (Offset = 0x9F) [reset = 0x0]

ESM_SOC_LMIN_REG is shown in Figure 5-219 and described in Table 5-191.

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Figure 5-219. ESM_SOC_LMIN_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_LMIN							
R/W-0b							

Table 5-191. ESM_SOC_LMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ESM_SOC_LMIN	R/W	0b	These bits configure the the minimum low-pulse time-threshold (tLOW_MAX_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

5.7.1.153 ESM_SOC_ERR_CNT_REG Register (Offset = 0xA0) [reset = 0x0]

ESM_SOC_ERR_CNT_REG is shown in Figure 5-220 and described in Table 5-192.

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Figure 5-220. ESM_SOC_ERR_CNT_REG Register

7	6	5	4	3	2	1	0
RESERVED			ESM_SOC_ERR_CNT				
R-0b			R-0b				

Table 5-192. ESM_SOC_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0b	
4:0	ESM_SOC_ERR_CNT	R	0b	Status bits to indicate the value of the ESM_SoC Error-Counter. The device clears these bits when ESM_SOC_START bit is 0, or when the device resets the SoC.

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5.7.1.154 REGISTER_LOCK Register (Offset = 0xA1) [reset = 0x0]

REGISTER_LOCK is shown in Figure 5-221 and described in Table 5-193.

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Figure 5-221. REGISTER_LOCK Register

7	6	5	4	3	2	1	0
RESERVED							REGISTER_LOCK_STATUS
R-0b							R-0b

Table 5-193. REGISTER_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0b	
0	REGISTER_LOCK_STATUS	R	0b	Unlocking registers: write 0x9B to this address. Locking registers: write anything else than 0x9B to this address. Written 8 bit data to this address will not be stored, only lock status can be read. REGISTER_LOCK_STATUS bit shows the lock status: 0b = Registers are unlocked 1b = Registers are locked

5.7.1.155 USER_EE_CTRL_1 Register (Offset = 0xA2) [reset = 0x0]

USER_EE_CTRL_1 is shown in Figure 5-222 and described in Table 5-194.

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Figure 5-222. USER_EE_CTRL_1 Register

7	6	5	4	3	2	1	0
USER_EE_PROG_UNLOCK_SEQ							
R-0b							

Table 5-194. USER_EE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_EE_PROG_UNLOCK_SEQ	R	0b	User EEPROM programming unlock sequence. Write 0x98, 0xB8, 0x13, 0x7D to unlock EEPROM programming. Write anything else to lock EEPROM programming.

5.7.1.156 USER_EE_CTRL_2 Register (Offset = 0xA3) [reset = 0x0]

USER_EE_CTRL_2 is shown in Figure 5-223 and described in Table 5-195.

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Figure 5-223. USER_EE_CTRL_2 Register

7	6	5	4	3	2	1	0
USER_PROG_ALLOWED	USER_PROG_UNLOCKED	RESERVED		EE_PROG_STATUS	EE_PROG_PFSM	EE_PROG_USER	EE_PROG_MODE
R-0b	R-0b	R/W-0b		R-0b	R/WSelfClrF-0b	R/WSelfClrF-0b	R/W-0b

Table 5-195. USER_EE_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	USER_PROG_ALLOWED	R	0b	User EEPROM programming lock status 0b = User is not allowed to program EEPROM (USER_EE_PROG_UNLOCK_CODE != 0xa5) 1b = User is allowed to program EEPROM (USER_EE_PROG_UNLOCK_CODE = 0xa5)
6	USER_PROG_UNLOCKED	R	0b	User EEPROM programming lock status 0b = User EEPROM programming locked 1b = User EEPROM programming unlocked (USER_PROG_ALLOWED=1 and correct code sequence written to USER_EE_PROG_UNLOCK_SEQ)
5:4	RESERVED	R/W	0b	
3	EE_PROG_STATUS	R	0b	EEPROM programming sequence status 0b = EEPROM ready for programming sequence 1b = EEPROM programming sequence busy
2	EE_PROG_PFSM	R/WSelfClrF	0b	Write 1 to start PFSM EEPROM programming. This bit is automatically cleared.
1	EE_PROG_USER	R/WSelfClrF	0b	Write user registers to the state they need to be programmed and write 1 to start user register EEPROM programming. This bit is automatically cleared.
0	EE_PROG_MODE	R/W	0b	EEPROM programming mode select 0b = EEPROM programming mode is not enabled 1b = EEPROM programming mode is enabled and PFSM is not functional

ADVANCE INFORMATION

5.7.1.157 SRAM_ADDR_CTRL Register (Offset = 0xA4) [reset = 0x0]

SRAM_ADDR_CTRL is shown in Figure 5-224 and described in Table 5-196.

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Figure 5-224. SRAM_ADDR_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						SRAM_SEL	
R/W-0b						R/W-0b	

Table 5-196. SRAM_ADDR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	SRAM_SEL	R/W	0b	Select the SRAM address space that can be addressed. 0b = 0x000-0x0FF 1b = 0x100-0x1FF 10b = 0x200-0x2FF 11b = 0x300-0x3FF

ADVANCE INFORMATION

5.7.1.158 RECOV_CNT_PFSM_INCR Register (Offset = 0xA5) [reset = 0x0]

RECOV_CNT_PFSM_INCR is shown in Figure 5-225 and described in Table 5-197.

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Figure 5-225. RECOV_CNT_PFSM_INCR Register

7	6	5	4	3	2	1	0
RESERVED							INCREMENT_RECOV_CNT
R/W-0b							R/WSelfClrF-0b

Table 5-197. RECOV_CNT_PFSM_INCR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	INCREMENT_RECOV_CNT	R/WSelfClrF	0b	Write 1 to increment recovery counter. This bit is accessible only by PFSM, not by I2C/SPI. This bit is automatically cleared.

5.7.1.159 MANUFACTURING_VER Register (Offset = 0xA6) [reset = 0x0]

MANUFACTURING_VER is shown in Figure 5-226 and described in Table 5-198.

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Figure 5-226. MANUFACTURING_VER Register

7	6	5	4	3	2	1	0
SILICON_REV							
R-0b							

Table 5-198. MANUFACTURING_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SILICON_REV	R	0b	SILICON_REV[7:6] - Reserved SILICON_REV[5:3] - ALR SILICON_REV[2:0] - Metal

5.7.1.160 CUSTOMER_NVM_ID_REG Register (Offset = 0xA7) [reset = 0x0]

CUSTOMER_NVM_ID_REG is shown in Figure 5-227 and described in Table 5-199.

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Figure 5-227. CUSTOMER_NVM_ID_REG Register

7	6	5	4	3	2	1	0
CUSTOMER_NVM_ID							
R/W-0b							

Table 5-199. CUSTOMER_NVM_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CUSTOMER_NVM_ID	R/W	0b	Customer defined value if customer programmed part Same value as in TI_NVM_ID register if TI programmed part

5.7.1.161 RTC_SECONDS Register (Offset = 0xB5) [reset = 0x0]

RTC_SECONDS is shown in Figure 5-228 and described in Table 5-200.

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Figure 5-228. RTC_SECONDS Register

7	6	5	4	3	2	1	0
RESERVED	SECOND_1			SECOND_0			
R/W-0b	R/W-0b			R/W-0b			

Table 5-200. RTC_SECONDS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:4	SECOND_1	R/W	0b	Second digit of seconds (range is 0 up to 5)
3:0	SECOND_0	R/W	0b	First digit of seconds (range is 0 up to 9)

ADVANCE INFORMATION

5.7.1.162 RTC_MINUTES Register (Offset = 0xB6) [reset = 0x0]

RTC_MINUTES is shown in Figure 5-229 and described in Table 5-201.

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Figure 5-229. RTC_MINUTES Register

7	6	5	4	3	2	1	0
RESERVED	MINUTE_1			MINUTE_0			
R/W-0b	R/W-0b			R/W-0b			

Table 5-201. RTC_MINUTES Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:4	MINUTE_1	R/W	0b	Second digit of minutes (range is 0 up to 5)
3:0	MINUTE_0	R/W	0b	First digit of minutes (range is 0 up to 9)

5.7.1.163 RTC_HOURS Register (Offset = 0xB7) [reset = 0x0]

RTC_HOURS is shown in Figure 5-230 and described in Table 5-202.

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Figure 5-230. RTC_HOURS Register

7	6	5	4	3	2	1	0
PM_NAM	RESERVED	HOUR_1		HOUR_0			
R/W-0b	R/W-0b	R/W-0b		R/W-0b			

Table 5-202. RTC_HOURS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PM_NAM	R/W	0b	Only used in PM_AM mode (otherwise it is set to 0) 0b = AM 1b = PM
6	RESERVED	R/W	0b	
5:4	HOUR_1	R/W	0b	Second digit of hours(range is 0 up to 2)
3:0	HOUR_0	R/W	0b	First digit of hours (range is 0 up to 9)

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5.7.1.164 RTC_DAYS Register (Offset = 0xB8) [reset = 0x0]

RTC_DAYS is shown in Figure 5-231 and described in Table 5-203.

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Figure 5-231. RTC_DAYS Register

7	6	5	4	3	2	1	0
RESERVED		DAY_1		DAY_0			
R/W-0b		R/W-0b		R/W-0b			

Table 5-203. RTC_DAYS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:4	DAY_1	R/W	0b	Second digit of days (range is 0 up to 3)
3:0	DAY_0	R/W	0b	First digit of days (range is 0 up to 9)

5.7.1.165 RTC_MONTHS Register (Offset = 0xB9) [reset = 0x0]

RTC_MONTHS is shown in Figure 5-232 and described in Table 5-204.

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Figure 5-232. RTC_MONTHS Register

7	6	5	4	3	2	1	0
RESERVED			MONTH_1	MONTH_0			
R/W-0b			R/W-0b	R/W-0b			

Table 5-204. RTC_MONTHS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	MONTH_1	R/W	0b	Second digit of months (range is 0 up to 1)
3:0	MONTH_0	R/W	0b	First digit of months (range is 0 up to 9)

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5.7.1.166 RTC_YEARS Register (Offset = 0xBA) [reset = 0x0]

RTC_YEARS is shown in Figure 5-233 and described in Table 5-205.

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Figure 5-233. RTC_YEARS Register

7	6	5	4	3	2	1	0
YEAR_1				YEAR_0			
R/W-0b				R/W-0b			

Table 5-205. RTC_YEARS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	YEAR_1	R/W	0b	Second digit of years (range is 0 up to 9)
3:0	YEAR_0	R/W	0b	First digit of years (range is 0 up to 9)

5.7.1.167 RTC_WEEKS Register (Offset = 0xBB) [reset = 0x0]

RTC_WEEKS is shown in Figure 5-234 and described in Table 5-206.

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Figure 5-234. RTC_WEEKS Register

7	6	5	4	3	2	1	0
RESERVED					WEEK		
R/W-0b					R/W-0b		

Table 5-206. RTC_WEEKS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	WEEK	R/W	0b	First digit of day of the week (range is 0 up to 6)

ADVANCE INFORMATION

5.7.1.168 ALARM_SECONDS Register (Offset = 0xBC) [reset = 0x0]

ALARM_SECONDS is shown in Figure 5-235 and described in Table 5-207.

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Figure 5-235. ALARM_SECONDS Register

7	6	5	4	3	2	1	0
RESERVED	ALR_SECOND_1			ALR_SECOND_0			
R/W-0b	R/W-0b			R/W-0b			

Table 5-207. ALARM_SECONDS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:4	ALR_SECOND_1	R/W	0b	Second digit of alarm programmation for seconds (range is 0 up to 5)
3:0	ALR_SECOND_0	R/W	0b	First digit of alarm programmation for seconds (range is 0 up to 9)

5.7.1.169 ALARM_MINUTES Register (Offset = 0xBD) [reset = 0x0]

ALARM_MINUTES is shown in Figure 5-236 and described in Table 5-208.

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Figure 5-236. ALARM_MINUTES Register

7	6	5	4	3	2	1	0
RESERVED	ALR_MINUTE_1			ALR_MINUTE_0			
R/W-0b	R/W-0b			R/W-0b			

Table 5-208. ALARM_MINUTES Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:4	ALR_MINUTE_1	R/W	0b	Second digit of alarm programmation for minutes (range is 0 up to 5)
3:0	ALR_MINUTE_0	R/W	0b	First digit of alarm programmation for minutes (range is 0 up to 9)

ADVANCE INFORMATION

5.7.1.170 ALARM_HOURS Register (Offset = 0xBE) [reset = 0x0]

ALARM_HOURS is shown in Figure 5-237 and described in Table 5-209.

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Figure 5-237. ALARM_HOURS Register

7	6	5	4	3	2	1	0
ALR_PM_NAM	RESERVED	ALR_HOUR_1		ALR_HOUR_0			
R/W-0b	R/W-0b	R/W-0b		R/W-0b			

Table 5-209. ALARM_HOURS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALR_PM_NAM	R/W	0b	Only used in PM_AM mode for alarm programmation (otherwise it is set to 0) 0b = AM 1b = PM
6	RESERVED	R/W	0b	
5:4	ALR_HOUR_1	R/W	0b	Second digit of alarm programmation for hours(range is 0 up to 2)
3:0	ALR_HOUR_0	R/W	0b	First digit of alarm programmation for hours (range is 0 up to 9)

ADVANCE INFORMATION

5.7.1.171 ALARM_DAYS Register (Offset = 0xBF) [reset = 0x0]

ALARM_DAYS is shown in Figure 5-238 and described in Table 5-210.

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Figure 5-238. ALARM_DAYS Register

7	6	5	4	3	2	1	0
RESERVED		ALR_DAY_1		ALR_DAY_0			
R/W-0b		R/W-0b		R/W-0b			

Table 5-210. ALARM_DAYS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:4	ALR_DAY_1	R/W	0b	Second digit of alarm programmation for days (range is 0 up to 3)
3:0	ALR_DAY_0	R/W	0b	First digit of alarm programmation for days (range is 0 up to 9)

ADVANCE INFORMATION

5.7.1.172 ALARM_MONTHS Register (Offset = 0xC0) [reset = 0x0]

ALARM_MONTHS is shown in Figure 5-239 and described in Table 5-211.

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Figure 5-239. ALARM_MONTHS Register

7	6	5	4	3	2	1	0
RESERVED			ALR_MONTH_1	ALR_MONTH_0			
R/W-0b			R/W-0b	R/W-0b			

Table 5-211. ALARM_MONTHS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	ALR_MONTH_1	R/W	0b	Second digit of alarm programmation for months (range is 0 up to 1)
3:0	ALR_MONTH_0	R/W	0b	First digit of alarm programmation for months (range is 0 up to 9)

5.7.1.173 ALARM_YEARS Register (Offset = 0xC1) [reset = 0x0]

ALARM_YEARS is shown in Figure 5-240 and described in Table 5-212.

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Figure 5-240. ALARM_YEARS Register

7	6	5	4	3	2	1	0
ALR_YEAR_1				ALR_YEAR_0			
R/W-0b				R/W-0b			

Table 5-212. ALARM_YEARS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	ALR_YEAR_1	R/W	0b	Second digit of alarm programmation for years (range is 0 up to 9)
3:0	ALR_YEAR_0	R/W	0b	First digit of alarm programmation for years (range is 0 up to 9)

5.7.1.174 RTC_CTRL_1 Register (Offset = 0xC2) [reset = 0x0]

RTC_CTRL_1 is shown in Figure 5-241 and described in Table 5-213.

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Figure 5-241. RTC_CTRL_1 Register

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	RESERVED	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-213. RTC_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RTC_V_OPT	R/W	0b	RTC date / time register selection: 0b = Read access directly to dynamic registers (RTC_SECONDS, RTC_MINUTES, RTC_HOURS, RTC_DAYS, RTC_MONTHS, RTC_YEAR, RTC_WEEKS) 1b = Read access to static shadowed registers: (see GET_TIME bit).
6	GET_TIME	R/W	0b	When writing a 1 into this register, the content of the dynamic registers (RTC_SECONDS, RTC_MINUTES, RTC_HOURS, RTC_DAYS, RTC_MONTHS, RTC_YEARS_ and RTC_WEEKS) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (i.e.: reset it to 0 and then rewrite it to 1) Note: Shadowed registers, linked to the GET_TIME feature, are a parallel set of calendar static registers, at the same I2C addresses as the dynamic registers. Note: The GET_TIME feature loads the RTC counter in the shadow registers and make the content of the shadow registers available and stable for reading. Note: The GET_TIME bit has to be set to 0 and again to 1 to get a new timing value. Note: If the time reading is done without GET_TIME, the read value comes directly from the RTC counter and software has to manage the counter change during the reading. Time reading remains always at the same address, with or without using the GET_TIME feature. Note: This bit is not protected by MSECURE.
5	SET_32_COUNTER	R/W	0b	Note: This bit must only be used when the RTC is frozen. 0b = No action 1b = Set the 32kHz counter with RTC_COMP_MSB_REG/RTC_COMP_LSB_REG value
4	RESERVED	R/W	0b	
3	MODE_12_24	R/W	0b	Note: It is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode. 0b = 24 hours mode 1b = 12 hours mode (PM-AM mode)
2	AUTO_COMP	R/W	0b	AUTO_COMP 0b = No auto compensation 1b = Auto compensation enabled

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Table 5-213. RTC_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ROUND_30S	R/W	0b	Note: This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller will read one until the rounding to the closest minute is performed at the next second. 0b = No update 1b = When a one is written, the time is rounded to the closest minute
0	STOP_RTC	R/W	0b	STOP_RTC 0b = RTC is frozen 1b = RTC is running

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5.7.1.175 RTC_CTRL_2 Register (Offset = 0xC3) [reset = 0x0]

RTC_CTRL_2 is shown in Figure 5-242 and described in Table 5-214.

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Figure 5-242. RTC_CTRL_2 Register

7	6	5	4	3	2	1	0
FIRST_STARTUP_DONE	STARTUP_DEST		FAST_BIST	LP_STANDBY_SEL	XTAL_SEL		XTAL_EN
R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b		R/W-0b

Table 5-214. RTC_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIRST_STARTUP_DONE	R/W	0b	This bit controls if EEPROM defaults are loaded to RTC domain reg bits during EEPROM read 0b = EEPROM defaults are loaded to RTC domain bits 1b = EEPROM defaults are not loaded to RTC domain bits
6:5	STARTUP_DEST	R/W	0b	FSM startup destination select. 0b = STANDBY/LP_STANDBY based on LP_STANDBY_SEL 1b = Reserved 10b = MCU_ONLY 11b = ACTIVE
4	FAST_BIST	R/W	0b	FAST_BIST 0b = Logic and analog BIST is run when transitioning from LP_STANDBY to ACTIVE state. 1b = Only analog BIST is run when transitioning from LP_STANDBY to ACTIVE state.
3	LP_STANDBY_SEL	R/W	0b	Control to enter low power standby state: 0b = LDOINT is enabled in standby state. 1b = Low power standby state is used as standby state (LDOINT is disabled).
2:1	XTAL_SEL	R/W	0b	Crystal oscillator type select 0b = 6 pF 1b = 9 pF 10b = 12.5 pF 11b = Reserved
0	XTAL_EN	R/W	0b	This bit is automatically set to "0" if LDORTC OV or UV is detected. This bit must be set to "1" to enable the crystal oscillator. 0b = Crystal oscillator is disabled 1b = Crystal oscillator is enabled

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5.7.1.176 RTC_STATUS Register (Offset = 0xC4) [reset = 0x0]

RTC_STATUS is shown in Figure 5-243 and described in Table 5-215.

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Figure 5-243. RTC_STATUS Register

7	6	5	4	3	2	1	0
POWER_UP	ALARM	TIMER	RESERVED			RUN	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b			R/W-0b	R/W-0b

Table 5-215. RTC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POWER_UP	R/W	0b	Indicates that a reset occurred (bit cleared to 0 by writing 1) and that RTC data are not valid anymore. Note: POWER_UP is set by a reset, is cleared by writing one in this bit. Note: The POWER_UP (RTC_STATUS) and RESET_STATUS (RTC_RESET_STATUS) register bits indicate the same information.
6	ALARM	R/W	0b	Indicates that an alarm interrupt has been generated (bit clear by writing 1). Note: The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of the RTC_STATUS register. Note: The timer interrupt is a low-level pulse (15us duration).
5	TIMER	R/W	0b	Indicates that an timer interrupt has been generated (bit clear by writing 1).
4:2	RESERVED	R/W	0b	
1	RUN	R/W	0b	Note: This bit shows the real state of the RTC, indeed because of STOP_RTC (RTC_CTRL) signal was resynchronized on 32kHz clock, the action of this bit is delayed. 0b = RTC is frozen 1b = RTC is running
0	RESERVED	R/W	0b	

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5.7.1.177 RTC_INTERRUPTS Register (Offset = 0xC5) [reset = 0x0]

RTC_INTERRUPTS is shown in Figure 5-244 and described in Table 5-216.

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Figure 5-244. RTC_INTERRUPTS Register

7	6	5	4	3	2	1	0
RESERVED				IT_ALARM	IT_TIMER	EVERY	
R/W-0b				R/W-0b	R/W-0b	R/W-0b	

Table 5-216. RTC_INTERRUPTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	IT_ALARM	R/W	0b	Enable one interrupt when the alarm value is reached (TC ALARM registers: ALARM_SECONDS, ALARM_MINUTES, ALARM_HOURS, ALARM_DAYS, ALARM_MONTHS, ALARM_YEARS) by the TC registers 0b = interrupt disabled 1b = interrupt enabled
2	IT_TIMER	R/W	0b	Enable periodic interrupt 0b = interrupt disabled 1b = interrupt enabled
1:0	EVERY	R/W	0b	Interrupt period 0b = every second 1b = every minute 10b = every hour 11b = every day

ADVANCE INFORMATION

5.7.1.178 RTC_COMP_LSB Register (Offset = 0xC6) [reset = 0x0]

RTC_COMP_LSB is shown in Figure 5-245 and described in Table 5-217.

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Figure 5-245. RTC_COMP_LSB Register

7	6	5	4	3	2	1	0
COMP_LSB_RTC							
R/W-0b							

Table 5-217. RTC_COMP_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	COMP_LSB_RTC	R/W	0b	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [LSB]

5.7.1.179 RTC_COMP_MSB Register (Offset = 0xC7) [reset = 0x0]

RTC_COMP_MSB is shown in Figure 5-246 and described in Table 5-218.

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Figure 5-246. RTC_COMP_MSB Register

7	6	5	4	3	2	1	0
COMP_MSB_RTC							
R/W-0b							

Table 5-218. RTC_COMP_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	COMP_MSB_RTC	R/W	0b	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [MSB]

5.7.1.180 RTC_RESET_STATUS Register (Offset = 0xC8) [reset = 0x0]

RTC_RESET_STATUS is shown in Figure 5-247 and described in Table 5-219.

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Figure 5-247. RTC_RESET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							RESET_STATUS_RTC
R/W-0b							R/W-0b

Table 5-219. RTC_RESET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b	
0	RESET_STATUS_RTC	R/W	0b	This bit can only be set to one and is cleared when a manual reset or a POR (case of VBAT below the VBAT min) occur. If this bit is reset it means that the RTC has lost its configuration. Note: The RESET_STATUS (RTC_RESET_STATUS) and POWER_UP (RTC_STATUS) register bits indicate the same information.

ADVANCE INFORMATION

5.7.1.181 SCRATCH_PAD_REG_1 Register (Offset = 0xC9) [reset = 0x0]

SCRATCH_PAD_REG_1 is shown in Figure 5-248 and described in Table 5-220.

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Figure 5-248. SCRATCH_PAD_REG_1 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_1							
R/W-0b							

Table 5-220. SCRATCH_PAD_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SCRATCH_PAD_1	R/W	0b	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

5.7.1.182 SCRATCH_PAD_REG_2 Register (Offset = 0xCA) [reset = 0x0]

SCRATCH_PAD_REG_2 is shown in Figure 5-249 and described in Table 5-221.

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Figure 5-249. SCRATCH_PAD_REG_2 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_2							
R/W-0b							

Table 5-221. SCRATCH_PAD_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SCRATCH_PAD_2	R/W	0b	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

ADVANCE INFORMATION

5.7.1.183 SCRATCH_PAD_REG_3 Register (Offset = 0xCB) [reset = 0x0]

SCRATCH_PAD_REG_3 is shown in Figure 5-250 and described in Table 5-222.

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Figure 5-250. SCRATCH_PAD_REG_3 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_3							
R/W-0b							

Table 5-222. SCRATCH_PAD_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SCRATCH_PAD_3	R/W	0b	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

5.7.1.184 SCRATCH_PAD_REG_4 Register (Offset = 0xCC) [reset = 0x0]

SCRATCH_PAD_REG_4 is shown in Figure 5-251 and described in Table 5-223.

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Figure 5-251. SCRATCH_PAD_REG_4 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_4							
R/W-0b							

Table 5-223. SCRATCH_PAD_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SCRATCH_PAD_4	R/W	0b	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

ADVANCE INFORMATION

5.7.1.185 PFSM_DELAY_REG_1 Register (Offset = 0xCD) [reset = 0x0]

PFSM_DELAY_REG_1 is shown in Figure 5-252 and described in Table 5-224.

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Figure 5-252. PFSM_DELAY_REG_1 Register

7	6	5	4	3	2	1	0
PFSM_DELAY1							
R/W-0b							

Table 5-224. PFSM_DELAY_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PFSM_DELAY1	R/W	0b	Generic delay1 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

5.7.1.186 PFSM_DELAY_REG_2 Register (Offset = 0xCE) [reset = 0x0]

PFSM_DELAY_REG_2 is shown in Figure 5-253 and described in Table 5-225.

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Figure 5-253. PFSM_DELAY_REG_2 Register

7	6	5	4	3	2	1	0
PFSM_DELAY2							
R/W-0b							

Table 5-225. PFSM_DELAY_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PFSM_DELAY2	R/W	0b	Generic delay2 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

ADVANCE INFORMATION

5.7.1.187 PFSM_DELAY_REG_3 Register (Offset = 0xCF) [reset = 0x0]

PFSM_DELAY_REG_3 is shown in Figure 5-254 and described in Table 5-226.

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Figure 5-254. PFSM_DELAY_REG_3 Register

7	6	5	4	3	2	1	0
PFSM_DELAY3							
R/W-0b							

Table 5-226. PFSM_DELAY_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PFSM_DELAY3	R/W	0b	Generic delay3 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

5.7.1.188 PFSM_DELAY_REG_4 Register (Offset = 0xD0) [reset = 0x0]

PFSM_DELAY_REG_4 is shown in Figure 5-255 and described in Table 5-227.

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Figure 5-255. PFSM_DELAY_REG_4 Register

7	6	5	4	3	2	1	0
PFSM_DELAY4							
R/W-0b							

Table 5-227. PFSM_DELAY_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PFSM_DELAY4	R/W	0b	Generic delay4 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

5.7.1.189 CRC_CALC_CONTROL Register (Offset = 0xEF) [reset = 0x0]

CRC_CALC_CONTROL is shown in Figure 5-256 and described in Table 5-228.

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Figure 5-256. CRC_CALC_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED						RUN_CRC_UPDATE	RUN_CRC_BIST
R/W-0b						R/WSelfClrF-0b	R/WSelfClrF-0b

Table 5-228. CRC_CALC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	RUN_CRC_UPDATE	R/WSelfClrF	0b	Runs CRC BIST and updates associated expected regmap CRC. This bit is automatically cleared.
0	RUN_CRC_BIST	R/WSelfClrF	0b	Runs CRC BIST and sets CRC error interrupts on failures. This bit is automatically cleared.

ADVANCE INFORMATION

5.7.1.190 CRC_1 Register (Offset = 0xF0) [reset = 0x0]

CRC_1 is shown in Figure 5-257 and described in Table 5-229.

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Figure 5-257. CRC_1 Register

7	6	5	4	3	2	1	0
REGMAP_USER_INCLUDE_PERSIST_CRC16_LOW							
R/W-0b							

Table 5-229. CRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_USER_INCLUDE_PERSIST_CRC16_LOW	R/W	0b	Regmap user space low CRC16 value to be matched against Eeprom load with RTC.

ADVANCE INFORMATION

5.7.1.191 CRC_2 Register (Offset = 0xF1) [reset = 0x0]

CRC_2 is shown in Figure 5-258 and described in Table 5-230.

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Figure 5-258. CRC_2 Register

7	6	5	4	3	2	1	0
REGMAP_USER_INCLUDE_PERSIST_CRC16_HIGH							
R/W-0b							

Table 5-230. CRC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_USER_INCLUDE_PERSIST_CRC16_HIGH	R/W	0b	Regmap user space high CRC16 value to be matched against Eeprom load with RTC.

5.7.1.192 CRC_3 Register (Offset = 0xF2) [reset = 0x0]

CRC_3 is shown in Figure 5-259 and described in Table 5-231.

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Figure 5-259. CRC_3 Register

7	6	5	4	3	2	1	0
REGMAP_USER_EXCLUDE_PERSIST_CRC16_LOW							
R/W-0b							

Table 5-231. CRC_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_USER_EXCLUDE_PERSIST_CRC16_LOW	R/W	0b	Regmap user space low CRC16 value to be matched against Eeprom load without RTC.

5.7.1.193 CRC_4 Register (Offset = 0xF3) [reset = 0x0]

CRC_4 is shown in Figure 5-260 and described in Table 5-232.

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Figure 5-260. CRC_4 Register

7	6	5	4	3	2	1	0
REGMAP_USER_EXCLUDE_PERSIST_CRC16_HIGH							
R/W-0b							

Table 5-232. CRC_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_USER_EXCLUDE_PERSIST_CRC16_HIGH	R/W	0b	Regmap user space high CRC16 value to be matched against Eeprom load without RTC.

5.7.1.194 CRC_5 Register (Offset = 0xF4) [reset = 0x0]

CRC_5 is shown in Figure 5-261 and described in Table 5-233.

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Figure 5-261. CRC_5 Register

7	6	5	4	3	2	1	0
REGMAP_CONFIG_CRC16_LOW							
R/W-0b							

Table 5-233. CRC_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_CONFIG_CRC16_LOW	R/W	0b	Regmap config space CRC16 value.

5.7.1.195 CRC_6 Register (Offset = 0xF5) [reset = 0x0]

CRC_6 is shown in Figure 5-262 and described in Table 5-234.

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Figure 5-262. CRC_6 Register

7	6	5	4	3	2	1	0
REGMAP_CONFIG_CRC16_HIGH							
R/W-0b							

Table 5-234. CRC_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_CONFIG_CRC16_HIGH	R/W	0b	Regmap config space CRC16 value.

5.7.1.196 CRC_7 Register (Offset = 0xF6) [reset = 0x0]

CRC_7 is shown in Figure 5-263 and described in Table 5-235.

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Figure 5-263. CRC_7 Register

7	6	5	4	3	2	1	0
SRAM_BANK0_CRC16_LOW							
R/W-0b							

Table 5-235. CRC_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SRAM_BANK0_CRC16_LOW	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

ADVANCE INFORMATION

5.7.1.197 CRC_8 Register (Offset = 0xF7) [reset = 0x0]

CRC_8 is shown in Figure 5-264 and described in Table 5-236.

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Figure 5-264. CRC_8 Register

7	6	5	4	3	2	1	0
SRAM_BANK0_CRC16_HIGH							
R/W-0b							

Table 5-236. CRC_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SRAM_BANK0_CRC16_HIGH	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

5.7.1.198 CRC_9 Register (Offset = 0xF8) [reset = 0x0]

CRC_9 is shown in Figure 5-265 and described in Table 5-237.

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Figure 5-265. CRC_9 Register

7	6	5	4	3	2	1	0
SRAM_BANK1_CRC16_LOW							
R/W-0b							

Table 5-237. CRC_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SRAM_BANK1_CRC16_LOW	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

ADVANCE INFORMATION

5.7.1.199 CRC_10 Register (Offset = 0xF9) [reset = 0x0]

CRC_10 is shown in Figure 5-266 and described in Table 5-238.

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Figure 5-266. CRC_10 Register

7	6	5	4	3	2	1	0
SRAM_BANK1_CRC16_HIGH							
R/W-0b							

Table 5-238. CRC_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SRAM_BANK1_CRC16_HIGH	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

5.7.1.200 CRC_11 Register (Offset = 0xFA) [reset = 0x0]

CRC_11 is shown in Figure 5-267 and described in Table 5-239.

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Figure 5-267. CRC_11 Register

7	6	5	4	3	2	1	0
SRAM_BANK2_CRC16_LOW							
R/W-0b							

Table 5-239. CRC_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SRAM_BANK2_CRC16_LOW	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

ADVANCE INFORMATION

5.7.1.201 CRC_12 Register (Offset = 0xFB) [reset = 0x0]

CRC_12 is shown in Figure 5-268 and described in Table 5-240.

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Figure 5-268. CRC_12 Register

7	6	5	4	3	2	1	0
SRAM_BANK2_CRC16_HIGH							
R/W-0b							

Table 5-240. CRC_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SRAM_BANK2_CRC16_HIGH	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

5.7.1.202 CRC_15 Register (Offset = 0xFE) [reset = 0x0]

CRC_15 is shown in Figure 5-269 and described in Table 5-241.

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Figure 5-269. CRC_15 Register

7	6	5	4	3	2	1	0
REGMAP_TRIM_CRC16_LOW							
R/W-0b							

Table 5-241. CRC_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_TRIM_CRC16_LOW	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

5.7.1.203 CRC_16 Register (Offset = 0xFF) [reset = 0x0]

CRC_16 is shown in Figure 5-270 and described in Table 5-242.

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Figure 5-270. CRC_16 Register

7	6	5	4	3	2	1	0
REGMAP_TRIM_CRC16_HIGH							
R/W-0b							

Table 5-242. CRC_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REGMAP_TRIM_CRC16_HIGH	R/W	0b	PFSM program (loaded from EEPROM to SRAM) code CRC16 value.

5.7.1.204 BUCK_CONFIG_ANALOG_0 Register (Offset = 0x100) [reset = 0x0]

BUCK_CONFIG_ANALOG_0 is shown in Figure 5-271 and described in Table 5-243.

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Figure 5-271. BUCK_CONFIG_ANALOG_0 Register

7	6	5	4	3	2	1	0
RESERVED	SEL_TRAD_NON_OVERLAP	SEL_GATE_EARLY_SENSE	RESERVED			SEL_LOOP_NEG_HYST	
R/W-0b	R/W-0b	R/W-0b	R/W-0b			R/W-0b	

Table 5-243. BUCK_CONFIG_ANALOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	SEL_TRAD_NON_OVERLAP	R/W	0b	selects traditional non ovelap --> long dead time 0b = traditional non ovelap not selected 1b = traditional non ovelap selected
5	SEL_GATE_EARLY_SENSE	R/W	0b	early gate sense for traditional non overlap --> shorter dead time if early sense 0b = early gate sense not selected 1b = early gate sense selected
4:2	RESERVED	R/W	0b	
1:0	SEL_LOOP_NEG_HYST	R/W	0b	Selects loop comparator negative hysteresis value. 0b = 800 nA 1b = 1200 nA 10b = 1600 nA 11b = 2000 nA

ADVANCE INFORMATION

5.7.1.205 BUCK_CONFIG_ANALOG_1 Register (Offset = 0x101) [reset = 0x0]

BUCK_CONFIG_ANALOG_1 is shown in Figure 5-272 and described in Table 5-244.

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Figure 5-272. BUCK_CONFIG_ANALOG_1 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK5_SEL_NEG_OCP_HYST	BUCK4_SEL_NEG_OCP_HYST	BUCK3_SEL_NEG_OCP_HYST	BUCK2_SEL_NEG_OCP_HYST	BUCK1_SEL_NEG_OCP_HYST	SEL_FB_FILTER	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-244. BUCK_CONFIG_ANALOG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	BUCK5_SEL_NEG_OCP_HYST	R/W	0b	hysteresis selection for negative current 0b = 1A 1b = 0.5A
5	BUCK4_SEL_NEG_OCP_HYST	R/W	0b	hysteresis selection for negative current 0b = 1A 1b = 0.5A
4	BUCK3_SEL_NEG_OCP_HYST	R/W	0b	hysteresis selection for negative current 0b = 1A 1b = 0.5A
3	BUCK2_SEL_NEG_OCP_HYST	R/W	0b	hysteresis selection for negative current 0b = 1A 1b = 0.5A
2	BUCK1_SEL_NEG_OCP_HYST	R/W	0b	hysteresis selection for negative current 0b = 1A 1b = 0.5A
1:0	SEL_FB_FILTER	R/W	0b	SEL_FB_FILTER 0b = 10MHz 1b = 5MHz 10b = 2.5MHz 11b = 1MHz

ADVANCE INFORMATION

5.7.1.206 BUCK_CONFIG_ANALOG_2 Register (Offset = 0x102) [reset = 0x0]

BUCK_CONFIG_ANALOG_2 is shown in Figure 5-273 and described in Table 5-245.

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Figure 5-273. BUCK_CONFIG_ANALOG_2 Register

7	6	5	4	3	2	1	0
RESERVED						SEL_RAMP_ARTIF	
R/W-0b						R/W-0b	

Table 5-245. BUCK_CONFIG_ANALOG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	SEL_RAMP_ARTIF	R/W	0b	SEL_RAMP_ARTIF 0b = i_slope_int = 3.0/9.0 1b = i_slope_int = 6.0/9.0 10b = i_slope_int = 12.0/9.0 11b = i_slope_int = 24.0/9.0

ADVANCE INFORMATION

5.7.1.207 BUCK_CONFIG_ANALOG_3 Register (Offset = 0x103) [reset = 0x0]

BUCK_CONFIG_ANALOG_3 is shown in Figure 5-274 and described in Table 5-246.

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Figure 5-274. BUCK_CONFIG_ANALOG_3 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK1_SEL_VOUT_ADC_LEVEL		BUCK1_SEL_ISENSE_SLOPE_COMPENSATION	
R/W-0b				R/W-0b		R/W-0b	

Table 5-246. BUCK_CONFIG_ANALOG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	BUCK1_SEL_VOUT_ADC_LEVEL	R/W	0b	Selects p_10m and m_10m comparators reference levels. 0b = 10mV of target vout 1b = 15mV of target vout 10b = 20mV of target vout 11b = 25mV of target vout
1:0	BUCK1_SEL_ISENSE_SLOPE_COMPENSATION	R/W	0b	buckx__isense_slope_compensation 0b = Disabled 1b = Disabled 10b = 220nH inductor 11b = 100nH inductor

ADVANCE INFORMATION

5.7.1.208 BUCK_CONFIG_ANALOG_4 Register (Offset = 0x104) [reset = 0x0]

BUCK_CONFIG_ANALOG_4 is shown in Figure 5-275 and described in Table 5-247.

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Figure 5-275. BUCK_CONFIG_ANALOG_4 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK2_SEL_VOUT_ADC_LEVEL		BUCK2_SEL_ISENSE_SLOPE_COMPENSATION	
R/W-0b				R/W-0b		R/W-0b	

Table 5-247. BUCK_CONFIG_ANALOG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	BUCK2_SEL_VOUT_ADC_LEVEL	R/W	0b	Selects p_10m and m_10m comparators reference levels. 0b = 10mV of target vout 1b = 15mV of target vout 10b = 20mV of target vout 11b = 25mV of target vout
1:0	BUCK2_SEL_ISENSE_SLOPE_COMPENSATION	R/W	0b	buckx__isense_slope_compensation 0b = Disabled 1b = Disabled 10b = 220nH inductor 11b = 100nH inductor

ADVANCE INFORMATION

5.7.1.209 BUCK_CONFIG_ANALOG_5 Register (Offset = 0x105) [reset = 0x0]

BUCK_CONFIG_ANALOG_5 is shown in Figure 5-276 and described in Table 5-248.

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Figure 5-276. BUCK_CONFIG_ANALOG_5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK3_SEL_VOUT_ADC_LEVEL		BUCK3_SEL_ISENSE_SLOPE_COMPENSATION	
R/W-0b				R/W-0b		R/W-0b	

Table 5-248. BUCK_CONFIG_ANALOG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	BUCK3_SEL_VOUT_ADC_LEVEL	R/W	0b	Selects p_10m and m_10m comparators reference levels. 0b = 10mV of target vout 1b = 15mV of target vout 10b = 20mV of target vout 11b = 25mV of target vout
1:0	BUCK3_SEL_ISENSE_SLOPE_COMPENSATION	R/W	0b	buckx__isense_slope_compensation 0b = Disabled 1b = Disabled 10b = 220nH inductor 11b = 100nH inductor

ADVANCE INFORMATION

5.7.1.210 BUCK_CONFIG_ANALOG_6 Register (Offset = 0x106) [reset = 0x0]

BUCK_CONFIG_ANALOG_6 is shown in Figure 5-277 and described in Table 5-249.

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Figure 5-277. BUCK_CONFIG_ANALOG_6 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK4_SEL_VOUT_ADC_LEVEL		BUCK4_SEL_ISENSE_SLOPE_COMPENSATION	
R/W-0b				R/W-0b		R/W-0b	

Table 5-249. BUCK_CONFIG_ANALOG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	BUCK4_SEL_VOUT_ADC_LEVEL	R/W	0b	Selects p_10m and m_10m comparators reference levels. 0b = 10mV of target vout 1b = 15mV of target vout 10b = 20mV of target vout 11b = 25mV of target vout
1:0	BUCK4_SEL_ISENSE_SLOPE_COMPENSATION	R/W	0b	buckx__isense_slope_compensation 0b = Disabled 1b = Disabled 10b = 220nH inductor 11b = 100nH inductor

ADVANCE INFORMATION

5.7.1.211 BUCK_CONFIG_ANALOG_7 Register (Offset = 0x107) [reset = 0x0]

BUCK_CONFIG_ANALOG_7 is shown in Figure 5-278 and described in Table 5-250.

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Figure 5-278. BUCK_CONFIG_ANALOG_7 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_SEL_VOUT_ADC_LEVEL		BUCK5_SEL_ISENSE_SLOPE_COMPENSATION	
R/W-0b				R/W-0b		R/W-0b	

Table 5-250. BUCK_CONFIG_ANALOG_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	BUCK5_SEL_VOUT_ADC_LEVEL	R/W	0b	Selects p_10m and m_10m comparators reference levels. 0b = 10mV of target vout 1b = 15mV of target vout 10b = 20mV of target vout 11b = 25mV of target vout
1:0	BUCK5_SEL_ISENSE_SLOPE_COMPENSATION	R/W	0b	buckx__isense_slope_compensation 0b = Disabled 1b = Disabled 10b = 220nH inductor 11b = 100nH inductor

ADVANCE INFORMATION

5.7.1.212 BUCK_CONFIG_ANALOG_8 Register (Offset = 0x108) [reset = 0x0]

BUCK_CONFIG_ANALOG_8 is shown in Figure 5-279 and described in Table 5-251.

Return to the Summary Table.

Figure 5-279. BUCK_CONFIG_ANALOG_8 Register

7	6	5	4	3	2	1	0
RESERVED						EN_IAVE_LOOP_INJECTOR	EN_SW_RT_SHORT_DETECTORS
R/W-0b						R/W-0b	R/W-0b

Table 5-251. BUCK_CONFIG_ANALOG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	EN_IAVE_LOOP_INJECTOR	R/W	0b	injects actual current information from isense to loop comparator for master buck. Improves the phase margin by decreasing the Q value of LC. 0b = Disabled 1b = Enabled
0	EN_SW_RT_SHORT_DETECTORS	R/W	0b	Enables switch node real time short detection, when en_sw_short_detectors bit is also enabled. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.213 BUCK_CONFIG_RADAR Register (Offset = 0x109) [reset = 0x0]

BUCK_CONFIG_RADAR is shown in Figure 5-280 and described in Table 5-252.

Return to the Summary Table.

Figure 5-280. BUCK_CONFIG_RADAR Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_EN_RADAR_MODE	BUCK4_EN_RADAR_MODE	BUCK3_EN_RADAR_MODE	BUCK2_EN_RADAR_MODE	BUCK1_EN_RADAR_MODE
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-252. BUCK_CONFIG_RADAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_EN_RADAR_MODE	R/W	0b	Radar mode enable for buck. When en_radar_mode is '1': - buck i_coeff[1:0] (buck_config_digi[42:41] is muxed to value 2'd3 - en_dot can be set to '0'. - fast vout integration is not used outside 10mV window - fast vout integration is used after vout ramps When en_radar_mode is '0': - Buck i_coeff[1:0] (buck_config_digi[42:41] is read from the register. - En_dot is muxed to '1'. 0b = Disabled 1b = Enabled
3	BUCK4_EN_RADAR_MODE	R/W	0b	Radar mode enable for buck. When en_radar_mode is '1': - buck i_coeff[1:0] (buck_config_digi[42:41] is muxed to value 2'd3 - en_dot can be set to '0'. - fast vout integration is not used outside 10mV window - fast vout integration is used after vout ramps When en_radar_mode is '0': - Buck i_coeff[1:0] (buck_config_digi[42:41] is read from the register. - En_dot is muxed to '1'. 0b = Disabled 1b = Enabled
2	BUCK3_EN_RADAR_MODE	R/W	0b	Radar mode enable for buck. When en_radar_mode is '1': - buck i_coeff[1:0] (buck_config_digi[42:41] is muxed to value 2'd3 - en_dot can be set to '0'. - fast vout integration is not used outside 10mV window - fast vout integration is used after vout ramps When en_radar_mode is '0': - Buck i_coeff[1:0] (buck_config_digi[42:41] is read from the register. - En_dot is muxed to '1'. 0b = Disabled 1b = Enabled
1	BUCK2_EN_RADAR_MODE	R/W	0b	Radar mode enable for buck. When en_radar_mode is '1': - buck i_coeff[1:0] (buck_config_digi[42:41] is muxed to value 2'd3 - en_dot can be set to '0'. - fast vout integration is not used outside 10mV window - fast vout integration is used after vout ramps When en_radar_mode is '0': - Buck i_coeff[1:0] (buck_config_digi[42:41] is read from the register. - En_dot is muxed to '1'. 0b = Disabled 1b = Enabled

Table 5-252. BUCK_CONFIG_RADAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BUCK1_EN_RADAR_MODE	R/W	0b	Radar mode enable for buck. When en_radar_mode is '1': - buck i_coeff[1:0] (buck_config_digi[42:41] is muxed to value 2'd3 - en_dot can be set to '0'. - fast vout integration is not used outside 10mV window - fast vout integration is used after vout ramps When en_radar_mode is '0': - Buck i_coeff[1:0] (buck_config_digi[42:41] is read from the register. - En_dot is muxed to '1'. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.214 BUCK_CONFIG_DIGITAL_0 Register (Offset = 0x10A) [reset = 0x0]

BUCK_CONFIG_DIGITAL_0 is shown in Figure 5-281 and described in Table 5-253.

Return to the Summary Table.

Figure 5-281. BUCK_CONFIG_DIGITAL_0 Register

7	6	5	4	3	2	1	0
BUCK3_SEL_PHASE_ADD		BUCK1_SEL_PHASE_ADD		BUCK3_SEL_PHASE_SHEDD		BUCK1_SEL_PHASE_SHEDD	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-253. BUCK_CONFIG_DIGITAL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BUCK3_SEL_PHASE_ADD	R/W	0b	Sets the output current level to add more phases. sel_phase_add: 0b = 1.4 A (2MHz & 1000nH) 1b = 2.0 A (4MHz & 470nH) 10b = 2.6 A (4MHz & 330nH) 11b = 3.2 A (8MHz & 100nH)
5:4	BUCK1_SEL_PHASE_ADD	R/W	0b	Sets the output current level to add more phases. sel_phase_add: 0b = 1.4 A (2MHz & 1000nH) 1b = 2.0 A (4MHz & 470nH) 10b = 2.6 A (4MHz & 330nH) 11b = 3.2 A (8MHz & 100nH)
3:2	BUCK3_SEL_PHASE_SHEDD	R/W	0b	Phase shed current levels (A/phase) sel_phase_shed 4_PH / 3_PH / 2_PH: 0b = 0.6 / 0.6 / 0.4 1b = 1.0 / 1.0 / 0.7 10b = 1.3 / 1.3 / 1.0 11b = 1.6 / 1.6 / 1.3
1:0	BUCK1_SEL_PHASE_SHEDD	R/W	0b	Phase shed current levels (A/phase) sel_phase_shed 4_PH / 3_PH / 2_PH: 0b = 0.6 / 0.6 / 0.4 1b = 1.0 / 1.0 / 0.7 10b = 1.3 / 1.3 / 1.0 11b = 1.6 / 1.6 / 1.3

ADVANCE INFORMATION

5.7.1.215 BUCK_CONFIG_DIGITAL_1 Register (Offset = 0x10B) [reset = 0x0]

BUCK_CONFIG_DIGITAL_1 is shown in Figure 5-282 and described in Table 5-254.

Return to the Summary Table.

Figure 5-282. BUCK_CONFIG_DIGITAL_1 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK5_SEL_POS_OCP_HYST	BUCK4_SEL_POS_OCP_HYST	BUCK3_SEL_POS_OCP_HYST	BUCK2_SEL_POS_OCP_HYST	BUCK1_SEL_POS_OCP_HYST	EN_PLL_PROP_EXTEND	EN_SMART_OCP_BLANK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-254. BUCK_CONFIG_DIGITAL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	BUCK5_SEL_POS_OCP_HYST	R/W	0b	hysteresis selection for positive current 0b = 1.5A 1b = 1A
5	BUCK4_SEL_POS_OCP_HYST	R/W	0b	hysteresis selection for positive current 0b = 1.5A 1b = 1A
4	BUCK3_SEL_POS_OCP_HYST	R/W	0b	hysteresis selection for positive current 0b = 1.5A 1b = 1A
3	BUCK2_SEL_POS_OCP_HYST	R/W	0b	hysteresis selection for positive current 0b = 1.5A 1b = 1A
2	BUCK1_SEL_POS_OCP_HYST	R/W	0b	hysteresis selection for positive current 0b = 1.5A 1b = 1A
1	EN_PLL_PROP_EXTEND	R/W	0b	If hs_active signal is shorter than the phase error between reference clk and hs_active, the previous pll prop raw measurement is used to adjust hs_length 0b = Disabled 1b = Enabled
0	EN_SMART_OCP_BLANK	R/W	0b	After detecting the pos ocp in HS, LS is forced until pos_ocp LS is detected. After detecting the neg ocp in LS, HS is forced until neg_ocp HS is detected. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.216 BUCK_CONFIG_DIGITAL_2 Register (Offset = 0x10C) [reset = 0x0]

BUCK_CONFIG_DIGITAL_2 is shown in Figure 5-283 and described in Table 5-255.

Return to the Summary Table.

Figure 5-283. BUCK_CONFIG_DIGITAL_2 Register

7	6	5	4	3	2	1	0
RESERVED				EN_LONG_PFM_EXIT_CNTR	SEL_HS_DETECTOR	RESERVED	
R/W-0b				R/W-0b	R/W-0b	R/W-0b	

Table 5-255. BUCK_CONFIG_DIGITAL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	EN_LONG_PFM_EXIT_CNTR	R/W	0b	Selects consecutive PFM pulse counter target to ECO/PFM exit. 0b = 7 Consecutive PFM pulses 1b = 15 Consecutive PFM pulses
2	SEL_HS_DETECTOR	R/W	0b	Defines how hs_ready is detected. 0b = Digital monitors phase detector error and sets hs_ready when pfd error stays small enough for 8 switching cycles. 1b = Digital monitors the direction of HS lenght filter. If HS length changes direction four times within specified time window, hs ready is detected.
1:0	RESERVED	R/W	0b	

ADVANCE INFORMATION

5.7.1.217 BUCK_CONFIG_DIGITAL_3 Register (Offset = 0x10D) [reset = 0x0]

BUCK_CONFIG_DIGITAL_3 is shown in Figure 5-284 and described in Table 5-256.

Return to the Summary Table.

Figure 5-284. BUCK_CONFIG_DIGITAL_3 Register

7	6	5	4	3	2	1	0
RESERVED		EN_DOT_MODE	EN_PFM_LOAD	RESERVED		EN_POS_OCP	EN_NEG_OCP
R/W-0b		R/W-0b	R/W-0b	R/W-0b		R/W-0b	R/W-0b

Table 5-256. BUCK_CONFIG_DIGITAL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	EN_DOT_MODE	R/W	0b	EN_DOT_MODE 0b = fixed frequency mode 1b = digital pll based on time control activated
4	EN_PFM_LOAD	R/W	0b	Enables pull down resistor in PFM mode when output voltage is higher than 10 mV of target. This is in case power FETs quiescent current pulls vout high when no load. 0b = Disabled 1b = Enabled
3:2	RESERVED	R/W	0b	
1	EN_POS_OCP	R/W	0b	Enables the positive current limit function. 0b = Disabled 1b = Enabled
0	EN_NEG_OCP	R/W	0b	Enables the negative current limit function. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.218 BUCK_CONFIG_DIGITAL_4 Register (Offset = 0x10E) [reset = 0x0]

BUCK_CONFIG_DIGITAL_4 is shown in Figure 5-285 and described in Table 5-257.

Return to the Summary Table.

Figure 5-285. BUCK_CONFIG_DIGITAL_4 Register

7	6	5	4	3	2	1	0
BUCK4_SEL_OUTPUT_CAPS		BUCK3_SEL_OUTPUT_CAPS		BUCK2_SEL_OUTPUT_CAPS		BUCK1_SEL_OUTPUT_CAPS	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 5-257. BUCK_CONFIG_DIGITAL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BUCK4_SEL_OUTPUT_CAPS	R/W	0b	Selection for the loop coefficients when auto_loop_coeffs enabled. See sharepoint
5:4	BUCK3_SEL_OUTPUT_CAPS	R/W	0b	Selection for the loop coefficients when auto_loop_coeffs enabled. See sharepoint
3:2	BUCK2_SEL_OUTPUT_CAPS	R/W	0b	Selection for the loop coefficients when auto_loop_coeffs enabled. See sharepoint
1:0	BUCK1_SEL_OUTPUT_CAPS	R/W	0b	Selection for the loop coefficients when auto_loop_coeffs enabled. See sharepoint

ADVANCE INFORMATION

5.7.1.219 BUCK_CONFIG_DIGITAL_5 Register (Offset = 0x10F) [reset = 0x0]

BUCK_CONFIG_DIGITAL_5 is shown in Figure 5-286 and described in Table 5-258.

Return to the Summary Table.

Figure 5-286. BUCK_CONFIG_DIGITAL_5 Register

7	6	5	4	3	2	1	0
RESERVED	EN_AUTO_LOOP_COEFFS	LOOP_COEFF_FB_MSB	EN_LONG_ZERO_CROSS_FILTER	SEL_ZERO_CROSS_FILTER_AVE	LOOP_COEFF_I_BALANCE	BUCK5_SEL_OUTPUT_CAPS	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-258. BUCK_CONFIG_DIGITAL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	EN_AUTO_LOOP_COEFFS	R/W	0b	EN_AUTO_LOOP_COEFFS 0b = Loop coefficients are defined with loop_coeff_fb and loop_coeff_i_balance registers. 1b = buck logic changes loop coefficients dynamically depending on active phases. The coefficient table can be found from the "buck_coefficients" excel in sharepoint (Design Top Level).
5	LOOP_COEFF_FB_MSB	R/W	0b	
4	EN_LONG_ZERO_CROSS_FILTER	R/W	0b	EN_LONG_ZERO_CROSS_FILTER 0b = Phase adding/PFM entry measurement time modulation waits until ZeroX filter has calculated the PFM entry. 1b = Load monitor time modulation is not waiting ZeroX filter. ZeroX filter is freezed during the phase adding measurement and PFM entry monitorin takes longer time.
3	SEL_ZERO_CROSS_FILTER_AVE	R/W	0b	SEL_ZERO_CROSS_FILTER_AVE 0b = PFM entry requires at least 3 zeroX detection of 8 samples 1b = PFM entry requires at least 5 zeroX detection of 8 samples
2	LOOP_COEFF_I_BALANCE	R/W	0b	Coefficient selection for the loop comparator input pair 2 (Current Balance)
1:0	BUCK5_SEL_OUTPUT_CAPS	R/W	0b	Selection for the loop coefficients when auto_loop_coeffs enabled. See sharepoint

ADVANCE INFORMATION

5.7.1.220 BUCK_CONFIG_DIGITAL_6 Register (Offset = 0x110) [reset = 0x0]

BUCK_CONFIG_DIGITAL_6 is shown in Figure 5-287 and described in Table 5-259.

Return to the Summary Table.

Figure 5-287. BUCK_CONFIG_DIGITAL_6 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK2_SEL_RAMP		BUCK1_SEL_RAMP		EN_SLOW_PLL_COEFFS	EN_PFM_PULSE_WAIT_LS_OCP	BUCK_DIGITAL_SPARE_1
R/W-0b	R/W-0b		R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 5-259. BUCK_CONFIG_DIGITAL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:5	BUCK2_SEL_RAMP	R/W	0b	Select Ramp Generator Slope 0b = 250kV/s 1b = 125kV/s 10b = 62.5kV/s 11b = 31.25kV/s
4:3	BUCK1_SEL_RAMP	R/W	0b	Select Ramp Generator Slope 0b = 250kV/s 1b = 125kV/s 10b = 62.5kV/s 11b = 31.25kV/s
2	EN_SLOW_PLL_COEFFS	R/W	0b	Divides by two the speed of the PLL Digital filter. 0b = Disabled 1b = Enabled
1	EN_PFM_PULSE_WAIT_LS_OCP	R/W	0b	OCP comparator is used during the LS to bring inductor current always below 500mA before allowing new PFM pulse. 0b = Disabled 1b = Enabled
0	BUCK_DIGITAL_SPARE_1	R/W	0b	

ADVANCE INFORMATION

5.7.1.221 BUCK_CONFIG_DIGITAL_7 Register (Offset = 0x111) [reset = 0x0]

BUCK_CONFIG_DIGITAL_7 is shown in Figure 5-288 and described in Table 5-260.

Return to the Summary Table.

Figure 5-288. BUCK_CONFIG_DIGITAL_7 Register

7	6	5	4	3	2	1	0
EN_FAST_PLL_0P7	EN_SW_SHORT_DETECTORS	BUCK5_SEL_RAMP		BUCK4_SEL_RAMP		BUCK3_SEL_RAMP	
R/W-0b	R/W-0b	R/W-0b		R/W-0b		R/W-0b	

Table 5-260. BUCK_CONFIG_DIGITAL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_FAST_PLL_0P7	R/W	0b	Enables fast PLL proportional and integral coefficients for HS length control when duty is above 70% and 2MHz switch frequency is used. 0b = Disabled 1b = Enabled
6	EN_SW_SHORT_DETECTORS	R/W	0b	When this is set and SW pin short is detected, buck swithces are turned to HIZ and main logic generates interrupt and trigger for PFSM. 0b = Disabled 1b = Enabled
5:4	BUCK5_SEL_RAMP	R/W	0b	Select Ramp Generator Slope 0b = 250kV/s 1b = 125kV/s 10b = 62.5kV/s 11b = 31.25kV/s
3:2	BUCK4_SEL_RAMP	R/W	0b	Select Ramp Generator Slope 0b = 250kV/s 1b = 125kV/s 10b = 62.5kV/s 11b = 31.25kV/s
1:0	BUCK3_SEL_RAMP	R/W	0b	Select Ramp Generator Slope 0b = 250kV/s 1b = 125kV/s 10b = 62.5kV/s 11b = 31.25kV/s

ADVANCE INFORMATION

5.7.1.222 BUCK_CONFIG_DIGITAL_8 Register (Offset = 0x112) [reset = 0x0]

BUCK_CONFIG_DIGITAL_8 is shown in Figure 5-289 and described in Table 5-261.

Return to the Summary Table.

Figure 5-289. BUCK_CONFIG_DIGITAL_8 Register

7	6	5	4	3	2	1	0
EN_SLOW_PLL_0P3	EN_CONSTANT_PLL_DVS_COEFF	RESERVED	DIS_DVS_WAIT_COMPARATORS	DIS_PFM_WAITS_HS_DETECTOR	DIS_PFM_WAITS_LS_DETECTOR	EN_I_BALANCE_INTEGRATOR	EN_FAST_VOUT_INTEGRATION
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-261. BUCK_CONFIG_DIGITAL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_SLOW_PLL_0P3	R/W	0b	Enables slow PLL proportional coefficients for HS length control when duty is below 30% 0b = Disabled 1b = Enabled
6	EN_CONSTANT_PLL_DVS_COEFF	R/W	0b	EN_CONSTANT_PLL_DVS_COEFF 0b = HS on-time adaptation speed during the voltage scaling is changed depending on the voltage scaling slew rate. 1b = HS on-time adaptation speed during the voltage scaling is the same value for all slew rates.
5	RESERVED	R/W	0b	
4	DIS_DVS_WAIT_COMPARATORS	R/W	0b	When high vout_ramp_active signal is not waiting output voltage is scaled between 10mV comparator after vout ramps. Vout_ramp_active signal keeps PG low, disables vref filter and gates phase sheding. 0b = Enabled 1b = Disabled
3	DIS_PFM_WAITS_HS_DETECTOR	R/W	0b	When disabled buck does not wait that HS length is detected before entering PFM/ECO mode nor sheding phases. 0b = Enabled 1b = Disabled
2	DIS_PFM_WAITS_LS_DETECTOR	R/W	0b	When disabled buck does not wait that LS length is detected before entering PFM/ECO mode. 0b = Enabled 1b = Disabled
1	EN_I_BALANCE_INTEGRATOR	R/W	0b	Enables current balance integrator 0b = Disabled 1b = Enabled
0	EN_FAST_VOUT_INTEGRATION	R/W	0b	Enables fast vout integrator coefficients when vout is outside +/- 10mV of target 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.223 BUCK_CONFIG_DIGITAL_9 Register (Offset = 0x113) [reset = 0x0]

BUCK_CONFIG_DIGITAL_9 is shown in Figure 5-290 and described in Table 5-262.

Return to the Summary Table.

Figure 5-290. BUCK_CONFIG_DIGITAL_9 Register

7	6	5	4	3	2	1	0
RESERVED	I_COEFF		EN_PWM_LS_DETECTION	RESERVED	EN_LS_AFTER_HIZ	EN_FAST_INTEGRATION_BYPASS_RAMP_RES	EN_M_10M_TRAN_DETECTOR
R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-262. BUCK_CONFIG_DIGITAL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:5	I_COEFF	R/W	0b	Vout integrator is stepped with frequency 825kHz, when vout error is more than 10mV. Vout integrator is stepped with frequency 206kHz/2^{i_coeff}, when vout error is less than 10mV. Current balance integrator is stepped with 51kHz/2^{i_coeff} frequency.
4	EN_PWM_LS_DETECTION	R/W	0b	EN_PWM_LS_DETECTION 0b = PWM LS detection is enabled only when going to PFM and after VOUT ramps to minimize current consumption. 1b = PWM LS detection is enabled always in Master Buck PWM mode.
3	RESERVED	R/W	0b	
2	EN_LS_AFTER_HIZ	R/W	0b	When enabled, Buck goes to LS always after LS Body diode usage to discharge reverse recovery charge. 0b = Disabled 1b = Enabled
1	EN_FAST_INTEGRATION_BYPASS_RAMP_RES	R/W	0b	When fast vout integration is used after vout scaling or when vout is outside 10mV of target value, emulated ramp bias resistor is bypassed.
0	EN_M_10M_TRAN_DETECTOR	R/W	0b	Enables master p_10m comparator usage as a transient detector. All the phases are added immediately ON when transient detected. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.224 BUCK_CONFIG_DIGITAL_10 Register (Offset = 0x114) [reset = 0x0]

BUCK_CONFIG_DIGITAL_10 is shown in Figure 5-291 and described in Table 5-263.

Return to the Summary Table.

Figure 5-291. BUCK_CONFIG_DIGITAL_10 Register

7	6	5	4	3	2	1	0
RESERVED				EN_ADAPTIVE_SINGLE_SHOT	BUCK_NEG_ILIM		
R/W-0b				R/W-0b	R/W-0b		

Table 5-263. BUCK_CONFIG_DIGITAL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	EN_ADAPTIVE_SINGLE_SHOT	R/W	0b	Enables single shot length adaptation 0b = Disabled 1b = Enabled
2:0	BUCK_NEG_ILIM	R/W	0b	Sets the negative current limit for LS switch. 0b = 1A 1b = 2A 10b = 3A 11b = 4A 100b = reserved 101b = reserved 110b = reserved 111b = reserved

ADVANCE INFORMATION

5.7.1.225 BUCK_CONFIG_DIGITAL_11 Register (Offset = 0x115) [reset = 0x0]

BUCK_CONFIG_DIGITAL_11 is shown in Figure 5-292 and described in Table 5-264.

Return to the Summary Table.

Figure 5-292. BUCK_CONFIG_DIGITAL_11 Register

7	6	5	4	3	2	1	0
RESERVED		LONG_SINGLE_SHOT	FIXED_SS_LENGTH				
R/W-0b		R/W-0b	R/W-0b				

Table 5-264. BUCK_CONFIG_DIGITAL_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	LONG_SINGLE_SHOT	R/W	0b	LONG_SINGLE_SHOT 0b = single shot length is adapted ~25ns 1b = single shot length is adapted to ~35ns
4:0	FIXED_SS_LENGTH	R/W	0b	Defines single shot pulse length, when en_adaptive_single_shot is '0'

ADVANCE INFORMATION

5.7.1.226 BUCK_CONFIG_DIGITAL_12 Register (Offset = 0x116) [reset = 0x0]

BUCK_CONFIG_DIGITAL_12 is shown in Figure 5-293 and described in Table 5-265.

Return to the Summary Table.

Figure 5-293. BUCK_CONFIG_DIGITAL_12 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_FREQ_8MHZ	BUCK4_FREQ_8MHZ	BUCK3_FREQ_8MHZ	BUCK2_FREQ_8MHZ	BUCK1_FREQ_8MHZ
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-265. BUCK_CONFIG_DIGITAL_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_FREQ_8MHZ	R/W	0b	8.8MHz frequency select for BUCK 0b = BUCK frequency is 2.2MHz or 4.4MHz according to BUCKx_FREQ_SEL 1b = BUCK frequency is 8.8MHz
3	BUCK4_FREQ_8MHZ	R/W	0b	8.8MHz frequency select for BUCK 0b = BUCK frequency is 2.2MHz or 4.4MHz according to BUCKx_FREQ_SEL 1b = BUCK frequency is 8.8MHz
2	BUCK3_FREQ_8MHZ	R/W	0b	8.8MHz frequency select for BUCK 0b = BUCK frequency is 2.2MHz or 4.4MHz according to BUCKx_FREQ_SEL 1b = BUCK frequency is 8.8MHz
1	BUCK2_FREQ_8MHZ	R/W	0b	8.8MHz frequency select for BUCK 0b = BUCK frequency is 2.2MHz or 4.4MHz according to BUCKx_FREQ_SEL 1b = BUCK frequency is 8.8MHz
0	BUCK1_FREQ_8MHZ	R/W	0b	8.8MHz frequency select for BUCK 0b = BUCK frequency is 2.2MHz or 4.4MHz according to BUCKx_FREQ_SEL 1b = BUCK frequency is 8.8MHz

ADVANCE INFORMATION

5.7.1.227 GENERAL_REG_0 Register (Offset = 0x117) [reset = 0x41]

GENERAL_REG_0 is shown in Figure 5-294 and described in Table 5-266.

Return to the Summary Table.

Figure 5-294. GENERAL_REG_0 Register

7	6	5	4	3	2	1	0
ABIST_ERROR_MASK	VMON_ABIST_EN	FAST_BOOT_BIST	DIS_TSD	DIS_UVLO_OVP_RESET	PFSM_ERR_RESET_DIS	VSYS_DEAD_LOCK_EN	EN_OVP
R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b

Table 5-266. GENERAL_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ABIST_ERROR_MASK	R/W	0b	Mask for ABIST error (SPMI WD, Buck/LDO/VCCA VMON, TSD) 0b = ABIST errors not masked 1b = ABIST errors masked
6	VMON_ABIST_EN	R/W	1b	ABIST enable for Buck/LDO/VCCA OV/UV VMONs. During BOOT_BIST ABIST is done only for VCCA OV/UV VMON if VMON_ABIST_EN=1, since Buck and LDO VMONs are not enabled. During RUNTIME_BIST ABIST is done for all VMONs that are enabled at the moment if VMON_ABIST_EN=1. Buck and LDO VMON ABIST is part of the startup sequence of each VMON. If VMON_ABIST_EN=1 ABIST is run for each buck and LDO VMONs after they are enabled. If VMON_ABIST_EN=0 all OV/UV VMON ABISTs are disabled. 0b = VMON ABIST not enabled 1b = VMON ABIST enabled
5	FAST_BOOT_BIST	R/W	0b	Boot BIST will be faster if LBIST is not run 0b = LBIST is run during boot BIST 1b = LBIST is not run during boot BIST
4	DIS_TSD	R/W	0b	TSD enable/disable 0b = Enabled 1b = Disabled
3	DIS_UVLO_OVP_RESET	R/W	0b	Select if UVLO and OVP cause reset to logic 0b = UVLO/OVP cause reset to logic 1b = UVLO/OVP will not cause reset to logic
2	PFSM_ERR_RESET_DIS	R/W	0b	Select if PFSM_ERR causes reset to logic 0b = PFSM_ERR causes reset to logic 1b = PFSM_ERR will not cause reset to logic
1	VSYS_DEAD_LOCK_EN	R/W	0b	VSYS_DEAD_LOCK_EN 0b = Fault recovery after VCCA OVP is controlled by PFSM 1b = Turn off VCCA with external FET in case of VCCA OVP
0	EN_OVP	R/W	1b	EN_OVP 0b = OVP disabled 1b = OVP enabled

ADVANCE INFORMATION

5.7.1.228 GENERAL_REG_1 Register (Offset = 0x118) [reset = 0x0]

GENERAL_REG_1 is shown in Figure 5-295 and described in Table 5-267.

Return to the Summary Table.

Figure 5-295. GENERAL_REG_1 Register

7	6	5	4	3	2	1	0
EN_INITIALIZE_DPLL_RESTART	REG_CRC_EN	RESERVED	PFSM_ERR_MASK	FREQ_SEL_UNLOCK	MAX_ILIM		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b		

Table 5-267. GENERAL_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_INITIALIZE_DPLL_RESTART	R/W	0b	DPLL restart frequency control 0b = DPLL restarts with same frequency as it was previously disabled 1b = DPLL restarts with same frequency as at first startup (+/-5% of nominal, depending of internal 20MHz oscillator)
6	REG_CRC_EN	R/W	0b	Register CRC enable 0b = Register CRC disabled 1b = Register CRC enabled
5	RESERVED	R/W	0b	
4	PFSM_ERR_MASK	R/W	0b	Masking of PFSM_ERR_INT interrupt: (Default from NVM memory) 0b = Interrupt generated 1b = Interrupt not generated.
3	FREQ_SEL_UNLOCK	R/W	0b	Unlock bit for Buck and Boost frequency selection (BUCKx_FREQ_SEL). (BUCKx_FREQ_SEL can be written if FREQ_SEL_UNLOCK=1 or debug_mode=1) 0b = Locked: user can only read frequency select bits. 1b = Unlocked: user can read and write frequency select bits.
2:0	MAX_ILIM	R/W	0b	Sets the maximum value for BUCKx_ILIM. BUCKx_ILIM values are internally limited to the set maximum and it does not affect the BUCKx_ILIM reg values.

ADVANCE INFORMATION

5.7.1.229 GENERAL_REG_2 Register (Offset = 0x119) [reset = 0x3]

GENERAL_REG_2 is shown in Figure 5-296 and described in Table 5-268.

Return to the Summary Table.

Figure 5-296. GENERAL_REG_2 Register

7	6	5	4	3	2	1	0
WD_EN_EE	DISABLE_USE_TRIMS	DISABLE_CHANGE_BG	DISABLE_VM_NARROW_LIMITS	SEL_RC_OSC	EN_FIXED_DPLL_FREQ	SLOW_AUTOZERO_SEL	DIS_NRSTOUT_MCU_I2C_SPI_RESET
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-1b

Table 5-268. GENERAL_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN_EE	R/W	0b	WD_EN_EE: 0b = Watchdog is disabled and user cannot enable it 1b = Watchdog is enabled if WD_EN=1
6	DISABLE_USE_TRIMS	R/W	0b	Bandgap trim control 0b = All the bandgaps use trims programmed to EEPROM 1b = Forces all the bandgaps to use default trim irrespective of the EEPROM code
5	DISABLE_CHANGE_BG	R/W	0b	DISABLE_CHANGE_BG 0b = Allow regulators to use REFSYS_INT bandgap after initial startup 1b = Forces all the blocks to use safety bandgap at all times
4	DISABLE_VM_NARROW_LIMITS	R/W	0b	DISABLE_VM_NARROW_LIMITS 0b = Use tighter voltage monitor limits after EEPROM load 1b = Use relaxed voltage monitor limits at all times
3	SEL_RC_OSC	R/W	0b	EEPROM register to select RC oscillator instead of DPLL for 52.8MHz clock source. 0b = DPLL 1b = RC oscillator
2	EN_FIXED_DPLL_FREQ	R/W	0b	EEPROM Register bit to select if PLL is disabled and DCO generates fixed frequency based on trim register 0b = PLL is enabled 1b = PLL is disabled and DCO generates fixed frequency based on trim register
1	SLOW_AUTOZERO_SEL	R/W	1b	Voltage monitor comparator autozero period select 0b = 32 kHz 1b = 8 kHz
0	DIS_NRSTOUT_MCU_I2C_SPI_RESET	R/W	1b	Control for reset pulse generated for I2C/SPI slave when NRSTOUT_MCU state changes 0b = Reset I2C/SPI at NRSTOUT_MCU rise/fall 1b = Don't reset I2C/SPI at NRSTOUT_MCU rise/fall

ADVANCE INFORMATION

5.7.1.230 SERIAL_IF_CONFIG Register (Offset = 0x11A) [reset = 0x0]

SERIAL_IF_CONFIG is shown in Figure 5-297 and described in Table 5-269.

Return to the Summary Table.

Figure 5-297. SERIAL_IF_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED					I2C2_CRC_EN	I2C1_SPI_CRC_EN	I2C_SPI_SEL
R/W-0b					R/W-0b	R/W-0b	R/W-0b

Table 5-269. SERIAL_IF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	I2C2_CRC_EN	R/W	0b	CRC enable for I2C2 interface 0b = CRC disabled 1b = CRC enabled
1	I2C1_SPI_CRC_EN	R/W	0b	CRC enable for I2C1 and SPI interfaces 0b = CRC disabled 1b = CRC enabled
0	I2C_SPI_SEL	R/W	0b	Serial data interface select 0b = I2C 1b = SPI

ADVANCE INFORMATION

5.7.1.231 SPMI_CONFIG_1 Register (Offset = 0x11B) [reset = 0x0]

SPMI_CONFIG_1 is shown in Figure 5-298 and described in Table 5-270.

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Figure 5-298. SPMI_CONFIG_1 Register

7	6	5	4	3	2	1	0
RESERVED			SPMI_SLAVE_PASSIVE	SPMI_CLK_SEL		SPMI_MASTER_SEL	SPMI_CRC_EN
R/W-0b			R/W-0b	R/W-0b		R/W-0b	R/W-0b

Table 5-270. SPMI_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	SPMI_SLAVE_PASSIVE	R/W	0b	Instructs the slave of the device to not initiate activity. For the master it means that trigger branches are taken locally. In slave devices no trigger events are injected. 0b = Active slave 1b = Passive slave
3:2	SPMI_CLK_SEL	R/W	0b	Determines the data clock rate of SPMI 0b = 10MHz 1b = 10MHz 10b = 5MHz 11b = 2.5MHz
1	SPMI_MASTER_SEL	R/W	0b	SPMI master/slave selection: 0b = Slave mode 1b = Master mode
0	SPMI_CRC_EN	R/W	0b	SPMI CRC enable 0b = SPMI CRC check disabled 1b = SPMI CRC check enabled

ADVANCE INFORMATION

5.7.1.232 SPMI_CONFIG_2 Register (Offset = 0x11C) [reset = 0x0]

SPMI_CONFIG_2 is shown in Figure 5-299 and described in Table 5-271.

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Figure 5-299. SPMI_CONFIG_2 Register

7	6	5	4	3	2	1	0
SPMI_WAKEUP_EN	SPMI_WD_EN	SPMI_EN	SPMI_WD_AUTO_BOOT	SPMI_SLAVE_ASR_HOLD	SPMI_RETRY_LIMIT		SPMI_IF_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b		R/W-0b

Table 5-271. SPMI_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPMI_WAKEUP_EN	R/W	0b	Enable SPMI wakeup from LP_STANDBY. 0b = Disabled 1b = Enabled
6	SPMI_WD_EN	R/W	0b	Enable the SPMI WD that continuously sends and can confirms response of SPMI slave IDs. 0b = SPMI WD disabled 1b = SPMI WD enabled
5	SPMI_EN	R/W	0b	Enable for SPMI, which is used in multiple TI PMIC solutions. 0b = SPMI disabled 1b = SPMI enabled
4	SPMI_WD_AUTO_BOOT	R/W	0b	SPMI auto boot will gate power-up until all slave devices respond over SPMI 0b = SPMI auto boot disabled 1b = SPMI auto boot enabled
3	SPMI_SLAVE_ASR_HOLD	R/W	0b	SPMI_SLAVE_ASR_HOLD 0b = TBD 1b = Enables SPMI protocol for slave device not requesting A-bit arbitration twice in a row.
2:1	SPMI_RETRY_LIMIT	R/W	0b	SPMI_RETRY_LIMIT 0b = No retry in case of error detected 1b = One retry in case of error detected 10b = Two retries in case of error detected 11b = Three retries in case of error detected
0	SPMI_IF_SEL	R/W	0b	SPMI_IF_SEL 0b = Debug feature and uses master logic to implement logical slave. 1b = TBD

5.7.1.233 SPMI_CONFIG_3 Register (Offset = 0x11D) [reset = 0x0]

SPMI_CONFIG_3 is shown in Figure 5-300 and described in Table 5-272.

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Figure 5-300. SPMI_CONFIG_3 Register

7	6	5	4	3	2	1	0
SPMI_WD_RUNTIME_INTERVAL				SPMI_WD_BOOT_INTERVAL			
R/W-0b				R/W-0b			

Table 5-272. SPMI_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SPMI_WD_RUNTIME_INTERVAL	R/W	0b	Interval time (value*51.2us) to send SPMI SlaveID requests during runtime
3:0	SPMI_WD_BOOT_INTERVAL	R/W	0b	Interval time (value*51.2us) to send SPMI SlaveID requests during boot

ADVANCE INFORMATION

5.7.1.234 SPMI_CONFIG_4 Register (Offset = 0x11E) [reset = 0x0]

SPMI_CONFIG_4 is shown in Figure 5-301 and described in Table 5-273.

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Figure 5-301. SPMI_CONFIG_4 Register

7	6	5	4	3	2	1	0
SPMI_PFSM_RESPONSE_TIMEOUT				SPMI_WD_RESPONSE_TIMEOUT			
R/W-0b				R/W-0b			

Table 5-273. SPMI_CONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SPMI_PFSM_RESPONSE_TIMEOUT	R/W	0b	The timeout threshold (value*12.8us) for a SPMI response to a PFSM trigger notification.
3:0	SPMI_WD_RESPONSE_TIMEOUT	R/W	0b	The timeout threshold (value*25.6us) for a SPMI SlaveID response to a SPMI watchdog request.

5.7.1.235 SPMI_CONFIG_5 Register (Offset = 0x11F) [reset = 0x0]

SPMI_CONFIG_5 is shown in Figure 5-302 and described in Table 5-274.

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Figure 5-302. SPMI_CONFIG_5 Register

7	6	5	4	3	2	1	0
SPMI_WD_RUNTIME_BIST_TIMEOUT				SPMI_WD_BOOT_BIST_TIMEOUT			
R/W-0b				R/W-0b			

Table 5-274. SPMI_CONFIG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SPMI_WD_RUNTIME_BIST_TIMEOUT	R/W	0b	SPMI BIST runtime timeout Equation: $2^{SPMI\_WD\_RUNTIME\_BIST\_TIMEOUT[3:0] + 8}$ Range: 12us <-> 840ms
3:0	SPMI_WD_BOOT_BIST_TIMEOUT	R/W	0b	SPMI BIST boot timeout Equation: $2^{SPMI\_WD\_BOOT\_BIST\_TIMEOUT[3:0] + 16}$ Range: 3.2ms <-> 107s

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5.7.1.236 SPMI_CONFIG_6 Register (Offset = 0x120) [reset = 0x0]

SPMI_CONFIG_6 is shown in Figure 5-303 and described in Table 5-275.

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Figure 5-303. SPMI_CONFIG_6 Register

7	6	5	4	3	2	1	0
BOOT_DELAY							
R/W-0b							

Table 5-275. SPMI_CONFIG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BOOT_DELAY	R/W	0b	System boot delay (value*819.2us) that occurs after boot/runtime BIST.

5.7.1.237 SPMI_ID Register (Offset = 0x121) [reset = 0x0]

SPMI_ID is shown in Figure 5-304 and described in Table 5-276.

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Figure 5-304. SPMI_ID Register

7	6	5	4	3	2	1	0
RESERVED		SPMI_MID		SPMI_SID			
R/W-0b		R/W-0b		R/W-0b			

Table 5-276. SPMI_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:4	SPMI_MID	R/W	0b	The ID of SPMI master. It is pertinent in arbitration of a multiple master setup (Not supported).
3:0	SPMI_SID	R/W	0b	Slave ID for SPMI interface when device is slave.

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5.7.1.238 I2C1_ID_REG Register (Offset = 0x122) [reset = 0x48]

I2C1_ID_REG is shown in Figure 5-305 and described in Table 5-277.

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Figure 5-305. I2C1_ID_REG Register

7	6	5	4	3	2	1	0
RESERVED	I2C1_ID						
R/W-0b	R/W-1001000b						

Table 5-277. I2C1_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	I2C1_ID	R/W	1001000b	I2C ID for I2C1 interface.

5.7.1.239 I2C2_ID_REG Register (Offset = 0x123) [reset = 0x12]

I2C2_ID_REG is shown in Figure 5-306 and described in Table 5-278.

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Figure 5-306. I2C2_ID_REG Register

7	6	5	4	3	2	1	0
RESERVED	I2C2_ID						
R/W-0b	R/W-10010b						

Table 5-278. I2C2_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	I2C2_ID	R/W	10010b	I2C ID for I2C2 interface.

5.7.1.240 CLOCK_REQS Register (Offset = 0x124) [reset = 0x0]

CLOCK_REQS is shown in Figure 5-307 and described in Table 5-279.

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Figure 5-307. CLOCK_REQS Register

7	6	5	4	3	2	1	0
RESERVED	LDO4_PD_FORCE	LDO3_PD_FORCE	LDO2_PD_FORCE	LDO1_PD_FORCE	RESERVED	INT_LDO_PD_FORCE	FORCE_CLK_GATE
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-279. CLOCK_REQS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	LDO4_PD_FORCE	R/W	0b	LDO pulldown control 0b = LDO pulldown not forced 1b = LDO pulldown always enabled
5	LDO3_PD_FORCE	R/W	0b	LDO pulldown control 0b = LDO pulldown not forced 1b = LDO pulldown always enabled
4	LDO2_PD_FORCE	R/W	0b	LDO pulldown control 0b = LDO pulldown not forced 1b = LDO pulldown always enabled
3	LDO1_PD_FORCE	R/W	0b	LDO pulldown control 0b = LDO pulldown not forced 1b = LDO pulldown always enabled
2	RESERVED	R/W	0b	
1	INT_LDO_PD_FORCE	R/W	0b	LDO pulldown control 0b = LDO pulldown not forced 1b = LDO pulldown always enabled
0	FORCE_CLK_GATE	R/W	0b	Force all clocks on. (Bypass manually added clock gates) 0b = Normal clock functionality, clocks on when requested 1b = All clock forced on

5.7.1.241 PHASE_CONFIG Register (Offset = 0x125) [reset = 0x0]

PHASE_CONFIG is shown in Figure 5-308 and described in Table 5-280.

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Figure 5-308. PHASE_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED					MP_CONFIG		
R/W-0b					R/W-0b		

Table 5-280. PHASE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	MP_CONFIG	R/W	0b	Buck multiphase config 0b = 4+1 1b = 1+1+1+1+1 10b = 2+1+1+1 11b = 3+1+1 100b = 2+2+1 101b = 2+2+1 110b = 2+2+1 111b = 2+2+1

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5.7.1.242 SPMI_SLAVE_COUNT Register (Offset = 0x126) [reset = 0x0]

SPMI_SLAVE_COUNT is shown in Figure 5-309 and described in Table 5-281.

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Figure 5-309. SPMI_SLAVE_COUNT Register

7	6	5	4	3	2	1	0
RESERVED					SPMI_SLAVE_CNT		
R/W-0b					R/W-0b		

Table 5-281. SPMI_SLAVE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	SPMI_SLAVE_CNT	R/W	0b	The number of expected Slave SPMI devices in the system. Since the master device contains a slave SPMI it is contained in the count.

5.7.1.243 XCOORD_REG Register (Offset = 0x12C) [reset = 0x0]

XCOORD_REG is shown in Figure 5-310 and described in Table 5-282.

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Figure 5-310. XCOORD_REG Register

7	6	5	4	3	2	1	0
XCOORD							
R/W-0b							

Table 5-282. XCOORD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	XCOORD	R/W	0b	Chip x-coordinate in wafer

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5.7.1.244 YCOORD_REG Register (Offset = 0x12D) [reset = 0x0]

YCOORD_REG is shown in Figure 5-311 and described in Table 5-283.

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Figure 5-311. YCOORD_REG Register

7	6	5	4	3	2	1	0
YCOORD							
R/W-0b							

Table 5-283. YCOORD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	YCOORD	R/W	0b	Chip y-coordinate in wafer

5.7.1.245 WAFERNUM_REG Register (Offset = 0x12E) [reset = 0x0]

WAFERNUM_REG is shown in Figure 5-312 and described in Table 5-284.

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Figure 5-312. WAFERNUM_REG Register

7	6	5	4	3	2	1	0
RESERVED		WAFERNUM					
R/W-0b		R/W-0b					

Table 5-284. WAFERNUM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	WAFERNUM	R/W	0b	Wafer number

5.7.1.246 WAFERLOTNUM_REG_1 Register (Offset = 0x12F) [reset = 0x0]

WAFERLOTNUM_REG_1 is shown in Figure 5-313 and described in Table 5-285.

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Figure 5-313. WAFERLOTNUM_REG_1 Register

7	6	5	4	3	2	1	0
WAFERLOTNUM_23_16							
R/W-0b							

Table 5-285. WAFERLOTNUM_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WAFERLOTNUM_23_16	R/W	0b	24 bit wafer lot number, bits 23:16

5.7.1.247 WAFERLOTNUM_REG_2 Register (Offset = 0x130) [reset = 0x0]

WAFERLOTNUM_REG_2 is shown in Figure 5-314 and described in Table 5-286.

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Figure 5-314. WAFERLOTNUM_REG_2 Register

7	6	5	4	3	2	1	0
WAFERLOTNUM_15_8							
R/W-0b							

Table 5-286. WAFERLOTNUM_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WAFERLOTNUM_15_8	R/W	0b	24 bit wafer lot number, bits 15:8

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5.7.1.248 WAFERLOTNUM_REG_3 Register (Offset = 0x131) [reset = 0x0]

WAFERLOTNUM_REG_3 is shown in Figure 5-315 and described in Table 5-287.

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Figure 5-315. WAFERLOTNUM_REG_3 Register

7	6	5	4	3	2	1	0
WAFERLOTNUM_7_0							
R/W-0b							

Table 5-287. WAFERLOTNUM_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WAFERLOTNUM_7_0	R/W	0b	24 bit wafer lot number, bits 7:0

5.7.1.249 WAFERFAB_REG Register (Offset = 0x132) [reset = 0x0]

WAFERFAB_REG is shown in Figure 5-316 and described in Table 5-288.

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Figure 5-316. WAFERFAB_REG Register

7	6	5	4	3	2	1	0
RESERVED					WAFERFAB		
R/W-0b					R/W-0b		

Table 5-288. WAFERFAB_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	WAFERFAB	R/W	0b	Wafer fab ID

5.7.1.250 BUCK_CONFIG_DIGITAL_13 Register (Offset = 0x133) [reset = 0x0]

BUCK_CONFIG_DIGITAL_13 is shown in Figure 5-317 and described in Table 5-289.

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Figure 5-317. BUCK_CONFIG_DIGITAL_13 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_EN_P_10M_BODY_DIODE	BUCK4_EN_P_10M_BODY_DIODE	BUCK3_EN_P_10M_BODY_DIODE	BUCK2_EN_P_10M_BODY_DIODE	BUCK1_EN_P_10M_BODY_DIODE
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-289. BUCK_CONFIG_DIGITAL_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_EN_P_10M_BODY_DIODE	R/W	0b	Enables LS body diode usage instead of LS FET when output voltage is 10mV higher than the target vout. 0b = Disabled 1b = Enabled
3	BUCK4_EN_P_10M_BODY_DIODE	R/W	0b	Enables LS body diode usage instead of LS FET when output voltage is 10mV higher than the target vout. 0b = Disabled 1b = Enabled
2	BUCK3_EN_P_10M_BODY_DIODE	R/W	0b	Enables LS body diode usage instead of LS FET when output voltage is 10mV higher than the target vout. 0b = Disabled 1b = Enabled
1	BUCK2_EN_P_10M_BODY_DIODE	R/W	0b	Enables LS body diode usage instead of LS FET when output voltage is 10mV higher than the target vout. 0b = Disabled 1b = Enabled
0	BUCK1_EN_P_10M_BODY_DIODE	R/W	0b	Enables LS body diode usage instead of LS FET when output voltage is 10mV higher than the target vout. 0b = Disabled 1b = Enabled

5.7.1.251 BUCK_CONFIG_DIGITAL_14 Register (Offset = 0x134) [reset = 0x0]

BUCK_CONFIG_DIGITAL_14 is shown in Figure 5-318 and described in Table 5-290.

Return to the Summary Table.

Figure 5-318. BUCK_CONFIG_DIGITAL_14 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_DOUBLE_PFM_PULSE	BUCK4_DOUBLE_PFM_PULSE	BUCK3_DOUBLE_PFM_PULSE	BUCK2_DOUBLE_PFM_PULSE	BUCK1_DOUBLE_PFM_PULSE
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-290. BUCK_CONFIG_DIGITAL_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_DOUBLE_PFM_PULSE	R/W	0b	DOUBLE_PFM_PULSE 0b = PFM pulse size is 1.5X compared to pulse size in PWM. 1b = PFM pulse size is double compared to pulse size in PWM.
3	BUCK4_DOUBLE_PFM_PULSE	R/W	0b	DOUBLE_PFM_PULSE 0b = PFM pulse size is 1.5X compared to pulse size in PWM. 1b = PFM pulse size is double compared to pulse size in PWM.
2	BUCK3_DOUBLE_PFM_PULSE	R/W	0b	DOUBLE_PFM_PULSE 0b = PFM pulse size is 1.5X compared to pulse size in PWM. 1b = PFM pulse size is double compared to pulse size in PWM.
1	BUCK2_DOUBLE_PFM_PULSE	R/W	0b	DOUBLE_PFM_PULSE 0b = PFM pulse size is 1.5X compared to pulse size in PWM. 1b = PFM pulse size is double compared to pulse size in PWM.
0	BUCK1_DOUBLE_PFM_PULSE	R/W	0b	DOUBLE_PFM_PULSE 0b = PFM pulse size is 1.5X compared to pulse size in PWM. 1b = PFM pulse size is double compared to pulse size in PWM.

ADVANCE INFORMATION

5.7.1.252 BUCK_CONFIG_DIGITAL_15 Register (Offset = 0x135) [reset = 0x0]

BUCK_CONFIG_DIGITAL_15 is shown in Figure 5-319 and described in Table 5-291.

Return to the Summary Table.

Figure 5-319. BUCK_CONFIG_DIGITAL_15 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_CHANGE_2MHZ_BELOW_0V5	BUCK4_CHANGE_2MHZ_BELOW_0V5	BUCK3_CHANGE_2MHZ_BELOW_0V5	BUCK2_CHANGE_2MHZ_BELOW_0V5	BUCK1_CHANGE_2MHZ_BELOW_0V5
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-291. BUCK_CONFIG_DIGITAL_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	BUCK5_CHANGE_2MHZ_BELOW_0V5	R/W	0b	CHANGE_2MHZ_BELOW_0V5 0b = change below 0.6V 1b = change below 0.5V
3	BUCK4_CHANGE_2MHZ_BELOW_0V5	R/W	0b	CHANGE_2MHZ_BELOW_0V5 0b = change below 0.6V 1b = change below 0.5V
2	BUCK3_CHANGE_2MHZ_BELOW_0V5	R/W	0b	CHANGE_2MHZ_BELOW_0V5 0b = change below 0.6V 1b = change below 0.5V
1	BUCK2_CHANGE_2MHZ_BELOW_0V5	R/W	0b	CHANGE_2MHZ_BELOW_0V5 0b = change below 0.6V 1b = change below 0.5V
0	BUCK1_CHANGE_2MHZ_BELOW_0V5	R/W	0b	CHANGE_2MHZ_BELOW_0V5 0b = change below 0.6V 1b = change below 0.5V

ADVANCE INFORMATION

5.7.1.253 SPREAD_SPECTRUM_CONFIG_1 Register (Offset = 0x13F) [reset = 0x0]

SPREAD_SPECTRUM_CONFIG_1 is shown in Figure 5-320 and described in Table 5-292.

Return to the Summary Table.

Figure 5-320. SPREAD_SPECTRUM_CONFIG_1 Register

7	6	5	4	3	2	1	0
RESERVED						SS_MODE	
R/W-0b						R/W-0b	

Table 5-292. SPREAD_SPECTRUM_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	SS_MODE	R/W	0b	Spread spectrum mode. (Default from NVM memory) 0b = No modulation 1b = Mixed dwell 10b = Blind LFSR 11b = Ramp dwell

ADVANCE INFORMATION

5.7.1.254 SPREAD_SPECTRUM_CONFIG_2 Register (Offset = 0x140) [reset = 0x0]

SPREAD_SPECTRUM_CONFIG_2 is shown in Figure 5-321 and described in Table 5-293.

Return to the Summary Table.

Figure 5-321. SPREAD_SPECTRUM_CONFIG_2 Register

7	6	5	4	3	2	1	0
SS_PARAM2				SS_PARAM1			
R/W-0b				R/W-0b			

Table 5-293. SPREAD_SPECTRUM_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SS_PARAM2	R/W	0b	Spread spectrum parameter 2. SS_MODE=0x0: N/A (No modulation) SS_MODE=0x1: Max dwell SS_MODE=0x2: Fixed dwell SS_MODE=0x3: Max dwell (Default from NVM memory)
3:0	SS_PARAM1	R/W	0b	Spread spectrum parameter 1. SS_MODE=0x0: N/A (No modulation) SS_MODE=0x1: Min dwell SS_MODE=0x2: Max step SS_MODE=0x3: Min dwell (Default from NVM memory)

ADVANCE INFORMATION

5.7.1.255 USER_EE_PROG_UNLOCK Register (Offset = 0x141) [reset = 0x0]

USER_EE_PROG_UNLOCK is shown in Figure 5-322 and described in Table 5-294.

Return to the Summary Table.

Figure 5-322. USER_EE_PROG_UNLOCK Register

7	6	5	4	3	2	1	0
USER_EE_PROG_UNLOCK_CODE							
R/W-0b							

Table 5-294. USER_EE_PROG_UNLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_EE_PROG_UNLOCK_CODE	R/W	0b	User EEPROM programming unlock code. User is allowed to program EEPROM only if value is 0xA5. With any other values the EEPROM programming unlock sequencer (USER_EE_PROG_UNLOCK_SEQ in USER_EE_CTRL_1 register) is disabled and user cannot unlock EEPROM programming.

ADVANCE INFORMATION

5.7.1.256 INT_CONFIG_0 Register (Offset = 0x142) [reset = 0x0]

INT_CONFIG_0 is shown in Figure 5-323 and described in Table 5-295.

Return to the Summary Table.

Figure 5-323. INT_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED					refsys_sel_ibias		refsys_bg_buf_hi_bw
R/W-0b					R/W-0b		R/W-0b

Table 5-295. INT_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:1	refsys_sel_ibias	R/W	0b	Select temperature independent bias current for REFSYS_INT block. 0b = nominal 100nA bias current 1b = 0.6x bias used for emulating temperature effects during debug phase 10b = 5x bias used for emulating temperature effects during debug phase 11b = 10x bias used during WLBI
0	refsys_bg_buf_hi_bw	R/W	0b	refsys_bg_buf_hi_bw 0b = Normal REFSYS_INT bandgap buffer bandwidth 1b = Higher REFSYS_INT bandgap buffer bandwidth

ADVANCE INFORMATION

5.7.1.257 SAFETY_CONFIG_0 Register (Offset = 0x143) [reset = 0x0]

SAFETY_CONFIG_0 is shown in Figure 5-324 and described in Table 5-296.

Return to the Summary Table.

Figure 5-324. SAFETY_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED				safety_sel_ibias		safety_bg_buf_hi_bw	safety_speedup
R/W-0b				R/W-0b		R/W-0b	R/W-0b

Table 5-296. SAFETY_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:2	safety_sel_ibias	R/W	0b	Select temperature independent bias current for SAFETY block. 0b = nominal 100nA bias current 1b = 0.6x bias used for emulating temperature effects during debug phase 10b = 5x bias used for emulating temperature effects during debug phase 11b = 10x bias used during WLBI
1	safety_bg_buf_hi_bw	R/W	0b	SAFETY_INT bandgap buffer bandwidth select 0b = Normal SAFETY_INT bandgap buffer bandwidth 1b = Higher SAFETY_INT bandgap buffer bandwidth
0	safety_speedup	R/W	0b	safety_speedup 0b = slow mode (default): normal bias current level. Comparator Iq ~2.5uA 1b = fast mode: higher bias current level. Comparator Iq ~4.5uA. Fast mode will increase both the speed of comparison and the speed of comparator settling during offset compensation.

ADVANCE INFORMATION

5.7.1.258 VM_VSYS_CONFIG_0 Register (Offset = 0x144) [reset = 0x0]

VM_VSYS_CONFIG_0 is shown in Figure 5-325 and described in Table 5-297.

Return to the Summary Table.

Figure 5-325. VM_VSYS_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED						vm_vsys_dummy_bit	
R/W-0b						R/W-0b	

Table 5-297. VM_VSYS_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	vm_vsys_dummy_bit	R/W	0b	Reserved dummy bits for the VSYS Voltage Monitor block

5.7.1.259 RTC_CONFIG_0 Register (Offset = 0x145) [reset = 0x0]

RTC_CONFIG_0 is shown in Figure 5-326 and described in Table 5-298.

Return to the Summary Table.

Figure 5-326. RTC_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED	xtal_bias_fine				xtal_comp_bias_lvl	xtal_amp_reg_mode	xtal_amp_reg_en
R/W-0b	R/W-0b				R/W-0b	R/W-0b	R/W-0b

Table 5-298. RTC_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:3	xtal_bias_fine	R/W	0b	Crystal oscillator high side transistor bias current control Note! Ibias_xtal depends on XTAL_SEL control 0b = 0.5 x Ibias_xtal 1b = 1.0 x Ibias_xtal 10b = 1.5 x Ibias_xtal 11b = 2.0 x Ibias_xtal 100b = 2.5 x Ibias_xtal 101b = 3.0 x Ibias_xtal 110b = 3.5 x Ibias_xtal 111b = 4.0 x Ibias_xtal 1000b = 4.5 x Ibias_xtal 1001b = 5.0 x Ibias_xtal 1010b = 5.5 x Ibias_xtal 1011b = 6.0 x Ibias_xtal 1100b = 6.5 x Ibias_xtal 1101b = 7.0 x Ibias_xtal 1110b = 7.5 x Ibias_xtal 1111b = 8.0 x Ibias_xtal
2	xtal_comp_bias_lvl	R/W	0b	Crystal comparator bias current select 0b = Nominal crystal comparator bias current 1b = More aggressive
1	xtal_amp_reg_mode	R/W	0b	XTAL amplitude regulation loop Vpp option select 0b = XTAL amplitude regulation loop smaller Vpp option (XTAL_AMP_REG_EN is set to 1) 1b = XTAL amplitude regulation loop higher Vpp option (XTAL_AMP_REG_EN is set to 1)
0	xtal_amp_reg_en	R/W	0b	XTAL amplitude regulation loop enable 0b = XTAL amplitude regulation loop disabled 1b = XTAL ampliture regulation loop enabled

ADVANCE INFORMATION

5.7.1.260 LDO1_3_FILT_CONFIG_0 Register (Offset = 0x146) [reset = 0x0]

LDO1_3_FILT_CONFIG_0 is shown in Figure 5-327 and described in Table 5-299.

Return to the Summary Table.

Figure 5-327. LDO1_3_FILT_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED						vbg_filt_config	
R/W-0b						R/W-0b	

Table 5-299. LDO1_3_FILT_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	vbg_filt_config	R/W	0b	Select reference RC filter value 0b = R = 5MΩ; C = 200pF 1b = R = 100KΩ; C = 200pF 10b = R = 500nA biased PMOS switch; C = 200pF 11b = R = 10nA biased PMOS switch; C = 200pF

5.7.1.261 LDO1_CONFIG_0 Register (Offset = 0x147) [reset = 0x0]

LDO1_CONFIG_0 is shown in Figure 5-328 and described in Table 5-300.

Return to the Summary Table.

Figure 5-328. LDO1_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED		ldo1_dis_ov_pldn	ldo1_en_cp_low_sr	ldo1_dis_cp_leak_comp	ldo1_dis_ilim	ldo1_dis_short_prot	ldo1_en_short_cp
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-300. LDO1_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	ldo1_dis_ov_pldn	R/W	0b	LDO output overvoltage pulldown control 0b = Enable output overvoltage pulldown cicuit 1b = Disable output overvoltage pulldown circuit
4	ldo1_en_cp_low_sr	R/W	0b	LDO charge pump slew rate control 0b = Running charge pump fly cap pull-up in normal slew rate 1b = Running charge pump fly cap pull-up in slow slew rate to reduce output ripple magnitude
3	ldo1_dis_cp_leak_comp	R/W	0b	LDO FET leakage compensation control 0b = Enable power FET leakage compensation in charge pump 1b = Disable power FET leakage compensation in charge pump
2	ldo1_dis_ilim	R/W	0b	LDO current limit control 0b = Enable power FET current limit 1b = Disable power FET currrent limit
1	ldo1_dis_short_prot	R/W	0b	LDO transient short circuit protection control 0b = Enable transient short circuit protection 1b = Disable transient short circuit protection
0	ldo1_en_short_cp	R/W	0b	LDO charge pump output short to ground control 0b = Enable LDO charge pump 1b = Disable LDO charge pump and short out charge pump holding cap (design not verified and will have very high iddq)

ADVANCE INFORMATION

5.7.1.262 LDO2_CONFIG_0 Register (Offset = 0x148) [reset = 0x0]

LDO2_CONFIG_0 is shown in Figure 5-329 and described in Table 5-301.

Return to the Summary Table.

Figure 5-329. LDO2_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED		ldo2_dis_ov_pldn	ldo2_en_cp_low_sr	ldo2_dis_cp_leak_comp	ldo2_dis_ilim	ldo2_dis_short_prot	ldo2_en_short_cp
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-301. LDO2_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	ldo2_dis_ov_pldn	R/W	0b	LDO output overvoltage pulldown control 0b = Enable output overvoltage pulldown cicuit 1b = Disable output overvoltage pulldown circuit
4	ldo2_en_cp_low_sr	R/W	0b	LDO charge pump slew rate control 0b = Running charge pump fly cap pull-up in normal slew rate 1b = Running charge pump fly cap pull-up in slow slew rate to reduce output ripple magnitude
3	ldo2_dis_cp_leak_comp	R/W	0b	LDO FET leakage compensation control 0b = Enable power FET leakage compensation in charge pump 1b = Disable power FET leakage compensation in charge pump
2	ldo2_dis_ilim	R/W	0b	LDO current limit control 0b = Enable power FET current limit 1b = Disable power FET currrent limit
1	ldo2_dis_short_prot	R/W	0b	LDO transient short circuit protection control 0b = Enable transient short circuit protection 1b = Disable transient short circuit protection
0	ldo2_en_short_cp	R/W	0b	LDO charge pump output short to ground control 0b = Enable LDO charge pump 1b = Disable LDO charge pump and short out charge pump holding cap (design not verified and will have very high iddq)

ADVANCE INFORMATION

5.7.1.263 LDO3_CONFIG_0 Register (Offset = 0x149) [reset = 0x0]

LDO3_CONFIG_0 is shown in Figure 5-330 and described in Table 5-302.

Return to the Summary Table.

Figure 5-330. LDO3_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED		ldo3_dis_ov_pldn	ldo3_en_cp_low_sr	ldo3_dis_cp_leak_comp	ldo3_dis_ilim	ldo3_dis_short_prot	ldo3_en_short_cp
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-302. LDO3_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	ldo3_dis_ov_pldn	R/W	0b	LDO output overvoltage pulldown control 0b = Enable output overvoltage pulldown cicuit 1b = Disable output overvoltage pulldown circuit
4	ldo3_en_cp_low_sr	R/W	0b	LDO charge pump slew rate control 0b = Running charge pump fly cap pull-up in normal slew rate 1b = Running charge pump fly cap pull-up in slow slew rate to reduce output ripple magnitude
3	ldo3_dis_cp_leak_comp	R/W	0b	LDO FET leakage compensation control 0b = Enable power FET leakage compensation in charge pump 1b = Disable power FET leakage compensation in charge pump
2	ldo3_dis_ilim	R/W	0b	LDO current limit control 0b = Enable power FET current limit 1b = Disable power FET currrent limit
1	ldo3_dis_short_prot	R/W	0b	LDO transient short circuit protection control 0b = Enable transient short circuit protection 1b = Disable transient short circuit protection
0	ldo3_en_short_cp	R/W	0b	LDO charge pump output short to ground control 0b = Enable LDO charge pump 1b = Disable LDO charge pump and short out charge pump holding cap (design not verified and will have very high iddq)

ADVANCE INFORMATION

5.7.1.264 LDO4_CONFIG_0 Register (Offset = 0x14A) [reset = 0x0]

LDO4_CONFIG_0 is shown in Figure 5-331 and described in Table 5-303.

Return to the Summary Table.

Figure 5-331. LDO4_CONFIG_0 Register

7	6	5	4	3	2	1	0
RESERVED					ldo4_filter_current		ldo4_sel_low_ilim
R/W-0b					R/W-0b		R/W-0b

Table 5-303. LDO4_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:1	ldo4_filter_current	R/W	0b	Selects PMOS LDO noise filter BW 0b = 10nA (default) 1b = 20nA 10b = 50nA 11b = 60nA
0	ldo4_sel_low_ilim	R/W	0b	PMOS LDO current limit level for ATE test 0b = full current 1b = 1/5 of full current < 200mA

ADVANCE INFORMATION

5.7.1.265 TEST_MODE_LOCK Register (Offset = 0x160) [reset = 0x0]

TEST_MODE_LOCK is shown in Figure 5-332 and described in Table 5-304.

Return to the Summary Table.

Figure 5-332. TEST_MODE_LOCK Register

7	6	5	4	3	2	1	0
TM_UNLOCK_CODE							
R-0b							

Table 5-304. TEST_MODE_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_UNLOCK_CODE	R	0b	To enter different test modes set high voltage to AMUX pin and write following code sequences: Debug mode: 0xE6, 0xD3, 0x3B Test mode: 0xE6, 0xD3, 0x3B, 0x5E Scan mode: 0xE6, 0xD3, 0x3B, 0x44 Scan mode+OVST: 0xE6, 0xD3, 0x3B, 0x55

ADVANCE INFORMATION

5.7.1.266 TEST_MODE_STATUS Register (Offset = 0x161) [reset = 0x0]

TEST_MODE_STATUS is shown in Figure 5-333 and described in Table 5-305.

Return to the Summary Table.

Figure 5-333. TEST_MODE_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						test_mode	debug_mode
R-0b						R-0b	R-0b

Table 5-305. TEST_MODE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0b	
1	test_mode	R	0b	1 - Device is in test mode
0	debug_mode	R	0b	1 - Device is in debug mode (This signal is high also in test mode)

5.7.1.267 TEST_SET_SCAN_MODE Register (Offset = 0x162) [reset = 0x0]

TEST_SET_SCAN_MODE is shown in Figure 5-334 and described in Table 5-306.

Return to the Summary Table.

Figure 5-334. TEST_SET_SCAN_MODE Register

7	6	5	4	3	2	1	0
RESERVED						SET_SCAN_OVST_MODE	SET_SCAN_MODE
R/W-0b						R/W-0b	R/W-0b

Table 5-306. TEST_SET_SCAN_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	SET_SCAN_OVST_MODE	R/W	0b	Write 1 to set scan mode with OVST charge pump enabled. Scan mode starts immediately when this bit is set, which means that I2C slave will not give the last ACK after the write sequence.
0	SET_SCAN_MODE	R/W	0b	Write 1 to set scan mode. Scan mode starts immediately when this bit is set, which means that I2C slave will not give the last ACK after the write sequence.

ADVANCE INFORMATION

5.7.1.268 DMUX1_CTRL_1 Register (Offset = 0x163) [reset = 0x0]

DMUX1_CTRL_1 is shown in Figure 5-335 and described in Table 5-307.

Return to the Summary Table.

Figure 5-335. DMUX1_CTRL_1 Register

7	6	5	4	3	2	1	0
TM_DMUX1_MODE		TM_DMUX1_INV	TM_DMUX1_MAIN_SEL				
R/W-0b		R/W-0b	R/W-0b				

Table 5-307. DMUX1_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TM_DMUX1_MODE	R/W	0b	DMUX mode select 0b = Normal 1b = R-mode 10b = CP-mode 11b = Reserved
5	TM_DMUX1_INV	R/W	0b	DMUX inversion select 0b = DMUX not inverted 1b = DMUX inverted
4:0	TM_DMUX1_MAIN_SEL	R/W	0b	

5.7.1.269 DMUX1_CTRL_2 Register (Offset = 0x164) [reset = 0x0]

DMUX1_CTRL_2 is shown in Figure 5-336 and described in Table 5-308.

Return to the Summary Table.

Figure 5-336. DMUX1_CTRL_2 Register

7	6	5	4	3	2	1	0
TM_DMUX1_DIV			TM_DMUX1_SUB_SEL				
R/W-0b			R/W-0b				

Table 5-308. DMUX1_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TM_DMUX1_DIV	R/W	0b	Testmux divider 0b = Divider disabled 1b = Divide by 2 10b = Divide by 4 11b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Divide by 64 111b = Divide by 128
4:0	TM_DMUX1_SUB_SEL	R/W	0b	

ADVANCE INFORMATION

5.7.1.270 DMUX2_CTRL_1 Register (Offset = 0x165) [reset = 0x0]

DMUX2_CTRL_1 is shown in Figure 5-337 and described in Table 5-309.

Return to the Summary Table.

Figure 5-337. DMUX2_CTRL_1 Register

7	6	5	4	3	2	1	0
TM_DMUX2_MODE		TM_DMUX2_INV	TM_DMUX2_MAIN_SEL				
R/W-0b		R/W-0b	R/W-0b				

Table 5-309. DMUX2_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TM_DMUX2_MODE	R/W	0b	DMUX mode select 0b = Normal 1b = R-mode 10b = CP-mode 11b = Reserved
5	TM_DMUX2_INV	R/W	0b	DMUX inversion select 0b = DMUX not inverted 1b = DMUX inverted
4:0	TM_DMUX2_MAIN_SEL	R/W	0b	

5.7.1.271 DMUX2_CTRL_2 Register (Offset = 0x166) [reset = 0x0]

DMUX2_CTRL_2 is shown in Figure 5-338 and described in Table 5-310.

Return to the Summary Table.

Figure 5-338. DMUX2_CTRL_2 Register

7	6	5	4	3	2	1	0
TM_DMUX2_DIV			TM_DMUX2_SUB_SEL				
R/W-0b			R/W-0b				

Table 5-310. DMUX2_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TM_DMUX2_DIV	R/W	0b	Testmux divider 0b = Divider disabled 1b = Divide by 2 10b = Divide by 4 11b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Divide by 64 111b = Divide by 128
4:0	TM_DMUX2_SUB_SEL	R/W	0b	

ADVANCE INFORMATION

5.7.1.272 DMUX3_CTRL_1 Register (Offset = 0x167) [reset = 0x0]

DMUX3_CTRL_1 is shown in Figure 5-339 and described in Table 5-311.

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Figure 5-339. DMUX3_CTRL_1 Register

7	6	5	4	3	2	1	0
TM_DMUX3_MODE		TM_DMUX3_INV	TM_DMUX3_MAIN_SEL				
R/W-0b		R/W-0b	R/W-0b				

Table 5-311. DMUX3_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TM_DMUX3_MODE	R/W	0b	DMUX mode select 0b = Normal 1b = R-mode 10b = CP-mode 11b = Reserved
5	TM_DMUX3_INV	R/W	0b	DMUX inversion select 0b = DMUX not inverted 1b = DMUX inverted
4:0	TM_DMUX3_MAIN_SEL	R/W	0b	

5.7.1.273 DMUX3_CTRL_2 Register (Offset = 0x168) [reset = 0x0]

DMUX3_CTRL_2 is shown in Figure 5-340 and described in Table 5-312.

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Figure 5-340. DMUX3_CTRL_2 Register

7	6	5	4	3	2	1	0
TM_DMUX3_DIV			TM_DMUX3_SUB_SEL				
R/W-0b			R/W-0b				

Table 5-312. DMUX3_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TM_DMUX3_DIV	R/W	0b	Testmux divider 0b = Divider disabled 1b = Divide by 2 10b = Divide by 4 11b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Divide by 64 111b = Divide by 128
4:0	TM_DMUX3_SUB_SEL	R/W	0b	

ADVANCE INFORMATION

5.7.1.274 DMUX4_CTRL_1 Register (Offset = 0x169) [reset = 0x0]

DMUX4_CTRL_1 is shown in Figure 5-341 and described in Table 5-313.

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Figure 5-341. DMUX4_CTRL_1 Register

7	6	5	4	3	2	1	0
TM_DMUX4_MODE		TM_DMUX4_INV	TM_DMUX4_MAIN_SEL				
R/W-0b		R/W-0b	R/W-0b				

Table 5-313. DMUX4_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TM_DMUX4_MODE	R/W	0b	DMUX mode select 0b = Normal 1b = R-mode 10b = CP-mode 11b = Reserved
5	TM_DMUX4_INV	R/W	0b	DMUX inversion select 0b = DMUX not inverted 1b = DMUX inverted
4:0	TM_DMUX4_MAIN_SEL	R/W	0b	

5.7.1.275 DMUX4_CTRL_2 Register (Offset = 0x16A) [reset = 0x0]

DMUX4_CTRL_2 is shown in Figure 5-342 and described in Table 5-314.

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Figure 5-342. DMUX4_CTRL_2 Register

7	6	5	4	3	2	1	0
TM_DMUX4_DIV			TM_DMUX4_SUB_SEL				
R/W-0b			R/W-0b				

Table 5-314. DMUX4_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TM_DMUX4_DIV	R/W	0b	Testmux divider 0b = Divider disabled 1b = Divide by 2 10b = Divide by 4 11b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Divide by 64 111b = Divide by 128
4:0	TM_DMUX4_SUB_SEL	R/W	0b	

ADVANCE INFORMATION

5.7.1.276 DMUX5_CTRL_1 Register (Offset = 0x16B) [reset = 0x0]

DMUX5_CTRL_1 is shown in Figure 5-343 and described in Table 5-315.

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Figure 5-343. DMUX5_CTRL_1 Register

7	6	5	4	3	2	1	0
TM_DMUX5_MODE		TM_DMUX5_INV	TM_DMUX5_MAIN_SEL				
R/W-0b		R/W-0b	R/W-0b				

Table 5-315. DMUX5_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TM_DMUX5_MODE	R/W	0b	DMUX mode select 0b = Normal 1b = R-mode 10b = CP-mode 11b = Reserved
5	TM_DMUX5_INV	R/W	0b	DMUX inversion select 0b = DMUX not inverted 1b = DMUX inverted
4:0	TM_DMUX5_MAIN_SEL	R/W	0b	

5.7.1.277 DMUX5_CTRL_2 Register (Offset = 0x16C) [reset = 0x0]

DMUX5_CTRL_2 is shown in Figure 5-344 and described in Table 5-316.

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Figure 5-344. DMUX5_CTRL_2 Register

7	6	5	4	3	2	1	0
TM_DMUX5_DIV			TM_DMUX5_SUB_SEL				
R/W-0b			R/W-0b				

Table 5-316. DMUX5_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TM_DMUX5_DIV	R/W	0b	Testmux divider 0b = Divider disabled 1b = Divide by 2 10b = Divide by 4 11b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Divide by 64 111b = Divide by 128
4:0	TM_DMUX5_SUB_SEL	R/W	0b	

ADVANCE INFORMATION

5.7.1.278 TEST_REG_8 Register (Offset = 0x16D) [reset = 0x0]

TEST_REG_8 is shown in Figure 5-345 and described in Table 5-317.

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Figure 5-345. TEST_REG_8 Register

7	6	5	4	3	2	1	0
RESERVED		START_ABIST	CHANGE_BG	VM_NARROW_LIMITS	USE_TRIMS	NINT_TX_DIS	NINT_TX
R/W-0b		R/WSelfClrF-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-317. TEST_REG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	START_ABIST	R/WSelfClrF	0b	When written high starts ABIST. Bit is automatically cleared.
4	CHANGE_BG	R/W	0b	Direct control of which bandgap is used for regulators 0b = Use SAFETY bandgap for all blocks 1b = Use REFSYS_INT bandfap for regulators
3	VM_NARROW_LIMITS	R/W	0b	Voltage monitor accuracy control. 0b = Use more relaxed voltage monitor limits 1b = Use more tight voltage monitor limits (normally used after EEPROM is loaded)
2	USE_TRIMS	R/W	0b	Bandgap trim override. 0b = Use default trim code for all bandgaps 1b = Use EEPROM trim codes for all bandgaps
1	NINT_TX_DIS	R/W	0b	NINT IO OUTPUT BUFFER DISABLE CONTROL 0b = Output buffer enabled 1b = Output buffer disabled
0	NINT_TX	R/W	0b	Direct NINT pin control, when NINT_TX_DIS bit is not set 0b = NINT_TX=0 1b = NINT_TX=1

ADVANCE INFORMATION

5.7.1.279 TEST_REG_9 Register (Offset = 0x16E) [reset = 0x0]

TEST_REG_9 is shown in Figure 5-346 and described in Table 5-318.

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Figure 5-346. TEST_REG_9 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_MODE						
R/W-0b	R/W-0b						

Table 5-318. TEST_REG_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	BUCK1_MODE	R/W	0b	Controls BUCK operation mode 0b = disabled 1b = auto/normal mode (pfm allowed) 10b = auto/normal mode (eco allowed) 11b = force pwm autophases 100b = force pwm max phases 101b = master warm start standby mode 110b = slave 111b = slave warm start standby mode

ADVANCE INFORMATION

5.7.1.280 TEST_REG_10 Register (Offset = 0x16F) [reset = 0x0]

TEST_REG_10 is shown in Figure 5-347 and described in Table 5-319.

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Figure 5-347. TEST_REG_10 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK2_MODE						
R/W-0b	R/W-0b						

Table 5-319. TEST_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	BUCK2_MODE	R/W	0b	Controls BUCK operation mode 0b = disabled 1b = auto/normal mode (pfm allowed) 10b = auto/normal mode (eco allowed) 11b = force pwm autophases 100b = force pwm max phases 101b = master warm start standby mode 110b = slave 111b = slave warm start standby mode

5.7.1.281 TEST_REG_11 Register (Offset = 0x170) [reset = 0x0]

TEST_REG_11 is shown in Figure 5-348 and described in Table 5-320.

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Figure 5-348. TEST_REG_11 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK3_MODE						
R/W-0b	R/W-0b						

Table 5-320. TEST_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	BUCK3_MODE	R/W	0b	Controls BUCK operation mode 0b = disabled 1b = auto/normal mode (pfm allowed) 10b = auto/normal mode (eco allowed) 11b = force pwm autophases 100b = force pwm max phases 101b = master warm start standby mode 110b = slave 111b = slave warm start standby mode

ADVANCE INFORMATION

5.7.1.282 TEST_REG_12 Register (Offset = 0x171) [reset = 0x0]

TEST_REG_12 is shown in Figure 5-349 and described in Table 5-321.

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Figure 5-349. TEST_REG_12 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK4_MODE						
R/W-0b	R/W-0b						

Table 5-321. TEST_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	BUCK4_MODE	R/W	0b	Controls BUCK operation mode 0b = disabled 1b = auto/normal mode (pfm allowed) 10b = auto/normal mode (eco allowed) 11b = force pwm autophases 100b = force pwm max phases 101b = master warm start standby mode 110b = slave 111b = slave warm start standby mode

5.7.1.283 TEST_REG_13 Register (Offset = 0x172) [reset = 0x0]

TEST_REG_13 is shown in Figure 5-350 and described in Table 5-322.

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Figure 5-350. TEST_REG_13 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK5_MODE						
R/W-0b	R/W-0b						

Table 5-322. TEST_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	BUCK5_MODE	R/W	0b	Controls BUCK operation mode 0b = disabled 1b = auto/normal mode (pfm allowed) 10b = auto/normal mode (eco allowed) 11b = force pwm autophases 100b = force pwm max phases 101b = master warm start standby mode 110b = slave 111b = slave warm start standby mode

ADVANCE INFORMATION

5.7.1.284 TEST_REG_14 Register (Offset = 0x173) [reset = 0x0]

TEST_REG_14 is shown in Figure 5-351 and described in Table 5-323.

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Figure 5-351. TEST_REG_14 Register

7	6	5	4	3	2	1	0
RESERVED		TEST_SINGLE_SHOT	BUCK5_VSET_MSB	BUCK4_VSET_MSB	BUCK3_VSET_MSB	BUCK2_VSET_MSB	BUCK1_VSET_MSB
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-323. TEST_REG_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	TEST_SINGLE_SHOT	R/W	0b	Sets all single shots to oscillator mode.
4	BUCK5_VSET_MSB	R/W	0b	Controls Buck5 voltage MSB bit. BUCK5_VSEL_BITS = 0. Buck5 voltage control word = {BUCK5_VSET_MSB, BUCK5_VSET1} BUCK5_VSEL_BITS = 1. Buck5 voltage control word = {BUCK5_VSET_MSB, BUCK5_VSET2} 0b = MSB=0 1b = MSB=1
3	BUCK4_VSET_MSB	R/W	0b	Controls Buck4 voltage MSB bit. BUCK4_VSEL_BITS = 0. Buck4 voltage control word = {BUCK4_VSET_MSB, BUCK4_VSET1} BUCK4_VSEL_BITS = 1. Buck4 voltage control word = {BUCK4_VSET_MSB, BUCK4_VSET2} 0b = MSB=0 1b = MSB=1
2	BUCK3_VSET_MSB	R/W	0b	Controls Buck3 voltage MSB bit. BUCK3_VSEL_BITS = 0. Buck3 voltage control word = {BUCK3_VSET_MSB, BUCK3_VSET1} BUCK3_VSEL_BITS = 1. Buck3 voltage control word = {BUCK3_VSET_MSB, BUCK3_VSET2} 0b = MSB=0 1b = MSB=1
1	BUCK2_VSET_MSB	R/W	0b	Controls Buck2 voltage MSB bit. BUCK2_VSEL_BITS = 0. Buck2 voltage control word = {BUCK2_VSET_MSB, BUCK2_VSET1} BUCK2_VSEL_BITS = 1. Buck2 voltage control word = {BUCK2_VSET_MSB, BUCK2_VSET2} 0b = MSB=0 1b = MSB=1
0	BUCK1_VSET_MSB	R/W	0b	Controls Buck1 voltage MSB bit. BUCK1_VSEL_BITS = 0. Buck1 voltage control word = {BUCK1_VSET_MSB, BUCK1_VSET1} BUCK1_VSEL_BITS = 1. Buck1 voltage control word = {BUCK1_VSET_MSB, BUCK1_VSET2} 0b = MSB=0 1b = MSB=1

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5.7.1.285 TEST_REG_15 Register (Offset = 0x174) [reset = 0x0]

TEST_REG_15 is shown in Figure 5-352 and described in Table 5-324.

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Figure 5-352. TEST_REG_15 Register

7	6	5	4	3	2	1	0
TEST_RTC_LDO_UVLO_DIS	RESERVED	TEST_WLBI_MODE	BG_XMON_EN	RESERVED	SAFETY_EN_REFS	LDO_EE_PLDN	LDO_EE_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-324. TEST_REG_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TEST_RTC_LDO_UVLO_DIS	R/W	0b	RTC_LDO UVLO disable control 0b = RTC_LDO uvlo enabled 1b = RTC_LDO uvlo disabled
6	RESERVED	R/W	0b	
5	TEST_WLBI_MODE	R/W	0b	WLBI enable for analog blocks that configures those blocks correctly for WLBI that don't get 10x bias current. 0b = WLBI mode disabled 1b = WLBI mode enabled
4	BG_XMON_EN	R/W	0b	Not used
3	RESERVED	R/W	0b	
2	SAFETY_EN_REFS	R/W	0b	Enables current distribution and 1.20V reference buffer inside the SAFETY block. 0b = Disabled 1b = Enabled
1	LDO_EE_PLDN	R/W	0b	EEPROM 1.5V LDO pull down enable in test mode 0b = Disabled 1b = Enabled
0	LDO_EE_EN	R/W	0b	EEPROM 1.5V LDO enable in test mode 0b = Disabled 1b = Enabled

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5.7.1.286 TEST_REG_16 Register (Offset = 0x175) [reset = 0x0]

TEST_REG_16 is shown in Figure 5-353 and described in Table 5-325.

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Figure 5-353. TEST_REG_16 Register

7	6	5	4	3	2	1	0
RESERVED		TSD_SEL_SENSOR		TSD_SEL_THRESHOLD			TSD_FORCE
R/W-0b		R/W-0b		R/W-0b			R/W-0b

Table 5-325. TEST_REG_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:4	TSD_SEL_SENSOR	R/W	0b	Select 1 of 4 TSD sense diodes 0b = Diode 1 1b = Diode 2 10b = Diode 3 11b = Diode 4
3:1	TSD_SEL_THRESHOLD	R/W	0b	Direct selection of TSD threshold in test mode. 0b = 110C 1b = 120C 10b = 130C 11b = 140C 100b = 150C 101b = Reserved 110b = Reserved 111b = Reserved
0	TSD_FORCE	R/W	0b	Prevents sensor diode rotation 0b = Rotation enabled 1b = Rotation disabled

ADVANCE INFORMATION

5.7.1.287 TEST_SPMI_1 Register (Offset = 0x176) [reset = 0x0]

TEST_SPMI_1 is shown in Figure 5-354 and described in Table 5-326.

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Figure 5-354. TEST_SPMI_1 Register

7	6	5	4	3	2	1	0
TM_SPMI_TX_PAYLOAD							
R/W-0b							

Table 5-326. TEST_SPMI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_SPMI_TX_PAYLOAD	R/W	0b	SPMI TX payload of manually generated SPMI transaction.

5.7.1.288 TEST_SPMI_2 Register (Offset = 0x177) [reset = 0x0]

TEST_SPMI_2 is shown in Figure 5-355 and described in Table 5-327.

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Figure 5-355. TEST_SPMI_2 Register

7	6	5	4	3	2	1	0
TM_SPMI_TX_ADDRESS							
R/W-0b							

Table 5-327. TEST_SPMI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_SPMI_TX_ADDRESS	R/W	0b	SPMI TX address of manually generated SPMI transaction.

5.7.1.289 TEST_SPMI_5 Register (Offset = 0x179) [reset = 0x0]

TEST_SPMI_5 is shown in Figure 5-356 and described in Table 5-328.

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Figure 5-356. TEST_SPMI_5 Register

7	6	5	4	3	2	1	0
SPMI_TX_DONE	SPMI_RX_DONE	RESERVED		TM_SPMI_TX_SLAVE_SEL	TM_SPMI_TX_REQ_HIGH	TM_SPMI_TX_REQ	TM_SPMI_TEST_MODE
R-0b	R-0b	R/W-0b		R/W-0b	R/W-0b	R/WSelfClrF-0b	R/W-0b

Table 5-328. TEST_SPMI_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPMI_TX_DONE	R	0b	Initiates the transmission of a manually generated SPMI command. Also clears SPMI_RX_DONE.
6	SPMI_RX_DONE	R	0b	Indicates an SPMI command has been received and placed in SPMI_RX_CMD/SPMI_RX_PAYLOAD.
5:4	RESERVED	R/W	0b	
3	TM_SPMI_TX_SLAVE_SEL	R/W	0b	Specifies the packet source (Master(0) or Slave(1)) of a manually generated SPMI packet. 0b = Master 1b = Slave
2	TM_SPMI_TX_REQ_HIGH	R/W	0b	Specifies the Priority level (High(1)/Low(0)) of a manually generated SPMI packet. 0b = Low priority level 1b = High priority level
1	TM_SPMI_TX_REQ	R/WSelfClrF	0b	Request transmission of an SPMI command with contents dictated by SPMI testmode registers.
0	TM_SPMI_TEST_MODE	R/W	0b	Permits the transmission of manually generated SPMI packets. 0b = Test mode disabled 1b = Test mode enabled

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5.7.1.290 TEST_SPMI_6 Register (Offset = 0x17A) [reset = 0x0]

TEST_SPMI_6 is shown in Figure 5-357 and described in Table 5-329.

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Figure 5-357. TEST_SPMI_6 Register

7	6	5	4	3	2	1	0
SPMI_RX_CMD							
R-0b							

Table 5-329. TEST_SPMI_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPMI_RX_CMD	R	0b	Indicates SPMI packet received (Normal or test modes). Reset by TM_SPMI_TX_REQ

5.7.1.291 TEST_SPMI_7 Register (Offset = 0x17B) [reset = 0x0]

TEST_SPMI_7 is shown in Figure 5-358 and described in Table 5-330.

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Figure 5-358. TEST_SPMI_7 Register

7	6	5	4	3	2	1	0
SPMI_RX_PAYLOAD							
R-0b							

Table 5-330. TEST_SPMI_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPMI_RX_PAYLOAD	R	0b	Payload of last received SPMI command.

5.7.1.292 TEST_PFSM_0 Register (Offset = 0x17C) [reset = 0x0]

TEST_PFSM_0 is shown in Figure 5-359 and described in Table 5-331.

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Figure 5-359. TEST_PFSM_0 Register

7	6	5	4	3	2	1	0
op_end	op_ready	pfsm_branch_self	pfsm_trigger_id				
R-0b	R-0b	R-0b	R-0b				

Table 5-331. TEST_PFSM_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	op_end	R	0b	
6	op_ready	R	0b	
5	pfsm_branch_self	R	0b	
4:0	pfsm_trigger_id	R	0b	

5.7.1.293 TEST_PFSM_1 Register (Offset = 0x17D) [reset = 0x0]

TEST_PFSM_1 is shown in Figure 5-360 and described in Table 5-332.

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Figure 5-360. TEST_PFSM_1 Register

7	6	5	4	3	2	1	0
op_breakpoint_match	op_debug_halt	RESERVED		TM_PFSM_BREAKPOINT_EN	TM_PFSM_SINGLE_STEP_PULSE	TM_PFSM_SINGLE_STEP_EN	FREEZE_PFSM
R-0b	R-0b	R/W-0b		R/W-0b	R/WSelfClrF-0b	R/W-0b	R/W-0b

Table 5-332. TEST_PFSM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	op_breakpoint_match	R	0b	
6	op_debug_halt	R	0b	
5:4	RESERVED	R/W	0b	
3	TM_PFSM_BREAKPOINT_EN	R/W	0b	If TM_PFSM_BREAKPOINT_EN_BITS=1 then TM_PFSM_BREAKPOINT_ADDRESS_BITS becomes a PFSM engine software breakpoint. 0b = Disabled 1b = Enabled
2	TM_PFSM_SINGLE_STEP_PULSE	R/WSelfClrF	0b	If TM_PFSM_SINGLE_STEP_EN_BITS=1 then TM_PFSM_SINGLE_STEP_PULSE_BITS causes the PFSM engine to execute the current instruction.
1	TM_PFSM_SINGLE_STEP_EN	R/W	0b	If TM_PFSM_SINGLE_STEP_EN_BITS=1 then TM_PFSM_SINGLE_STEP_PULSE_BITS causes the PFSM engine to execute the current instruction. 0b = Disabled 1b = Enabled
0	FREEZE_PFSM	R/W	0b	FREEZE_PFSM 0b = PFSM is running, SRAM cannot be read by I2C/SPI 1b = PFSM is frozen, SRAM can be read by I2C/SPI

ADVANCE INFORMATION

5.7.1.294 TEST_PFSM_2 Register (Offset = 0x17E) [reset = 0x0]

TEST_PFSM_2 is shown in Figure 5-361 and described in Table 5-333.

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Figure 5-361. TEST_PFSM_2 Register

7	6	5	4	3	2	1	0
RESERVED			TM_PFSM_BREAKPOINT_ADDRESS_12_8				
R/W-0b			R/W-0b				

Table 5-333. TEST_PFSM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	TM_PFSM_BREAKPOINT_ADDRESS_12_8	R/W	0b	If TM_PFSM_BREAKPOINT_EN_BITS=1 then TM_PFSM_BREAKPOINT_ADDRESS_12_8_BITS becomes a PFSM engine software breakpoint.

5.7.1.295 TEST_PFSM_3 Register (Offset = 0x17F) [reset = 0x0]

TEST_PFSM_3 is shown in Figure 5-362 and described in Table 5-334.

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Figure 5-362. TEST_PFSM_3 Register

7	6	5	4	3	2	1	0
TM_PFSM_BREAKPOINT_ADDRESS_7_0							
R/W-0b							

Table 5-334. TEST_PFSM_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_PFSM_BREAKPOINT_ADDRESS_7_0	R/W	0b	If TM_PFSM_BREAKPOINT_EN_BITS=1 then TM_PFSM_BREAKPOINT_ADDRESS_7_0_BITS becomes a PFSM engine software breakpoint.

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5.7.1.296 TEST_FFSM_1 Register (Offset = 0x180) [reset = 0x0]

TEST_FFSM_1 is shown in Figure 5-363 and described in Table 5-335.

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Figure 5-363. TEST_FFSM_1 Register

7	6	5	4	3	2	1	0
RESERVED				fixed_fsm_state			
R-0b				R-0b			

Table 5-335. TEST_FFSM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	fixed_fsm_state	R	0b	Current FSM state. 0b = FSM_RESET 1b = FSM_NVM_LDO_SU 10b = FSM_NVM_READ 11b = FSM_CHANGE_BG_DELAY 100b = FSM_NARROW_LIMITS_DELAY 101b = FSM_BOOT_BIST 110b = FSM_MISSION_STATES 111b = FSM_SHUTDOWN 1000b = FSM_RUNTIME_BIST 1001b = FSM_USER_EE_PROG_SU 1010b = FSM_USER_EE_PROG 1011b = Reserved 1100b = Reserved 1101b = Reserved 1110b = Reserved 1111b = FSM_OFF (Test mode)

ADVANCE INFORMATION

5.7.1.297 TEST_FFSM_2 Register (Offset = 0x181) [reset = 0x0]

TEST_FFSM_2 is shown in Figure 5-364 and described in Table 5-336.

Return to the Summary Table.

Figure 5-364. TEST_FFSM_2 Register

7	6	5	4	3	2	1	0
RESERVED			force_fixed_fsm_state	next_fixed_fsm_state			
R/W-0b			R/W-0b	R/W-0b			

Table 5-336. TEST_FFSM_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	force_fixed_fsm_state	R/W	0b	Force fixed FSM state 0b = Fixed FSM works normally. 1b = Fixed FSM is forced to state defined by next_fixed_fsm_state.
3:0	next_fixed_fsm_state	R/W	0b	State where fixed FSM will be forced if force_fixed_fsm_state=1 0b = FSM_RESET 1b = FSM_NVM_LDO_SU 10b = FSM_NVM_READ 11b = FSM_CHANGE_BG_DELAY 100b = FSM_NARROW_LIMITS_DELAY 101b = FSM_BOOT_BIST 110b = FSM_MISSION_STATES 111b = FSM_SHUTDOWN 1000b = FSM_RUNTIME_BIST 1001b = FSM_USER_EE_PROG_SU 1010b = FSM_USER_EE_PROG 1011b = Reserved 1100b = Reserved 1101b = Reserved 1110b = Reserved 1111b = FSM_OFF (Test mode)

ADVANCE INFORMATION

5.7.1.298 TEST_REG_29 Register (Offset = 0x182) [reset = 0x0]

TEST_REG_29 is shown in Figure 5-365 and described in Table 5-337.

Return to the Summary Table.

Figure 5-365. TEST_REG_29 Register

7	6	5	4	3	2	1	0
FORCE_AUTOZERO_HIGH	FORCE_AUTOZERO_LOW	TM_LDOINT_DIS	LDO_INT_PLDN	LDO4_PD_DISABLE	LDO3_PD_DISABLE	LDO2_PD_DISABLE	LDO1_PD_DISABLE
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-337. TEST_REG_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE_AUTOZERO_HIGH	R/W	0b	Forces LDO/BUCK/VCCA VMON autozero signals high. If set high need to mask comparator interrupts in order to avoid PFSM shutdown. 0b = Autozero signals not forced 1b = Autozero signals forced high
6	FORCE_AUTOZERO_LOW	R/W	0b	Forces LDO/BUCK/VCCA VMON autozero signals low if not forced high. 0b = Autozero signals not forced 1b = Autozero signals forced low
5	TM_LDOINT_DIS	R/W	0b	LDOINT control in test mode. If not in test mode this bit has no effect. 0b = LDOINT enabled 1b = LDOINT disabled
4	LDO_INT_PLDN	R/W	0b	LDO_INT PULLDOWN CONTROL 0b = Pulldown disabled 1b = Pulldown enabled if not overriden by en_ovst or en_hiz bits
3	LDO4_PD_DISABLE	R/W	0b	LDO4 PULLDOWN CONTROL 0b = Pulldown disabled 1b = Pulldown enabled if not overriden by en_ovst or en_hiz bits
2	LDO3_PD_DISABLE	R/W	0b	LDO3 PULLDOWN CONTROL 0b = Pulldown disabled 1b = Pulldown enabled if not overriden by en_ovst or en_hiz bits
1	LDO2_PD_DISABLE	R/W	0b	LDO2 PULLDOWN CONTROL 0b = Pulldown disabled 1b = Pulldown enabled if not overriden by en_ovst or en_hiz bits
0	LDO1_PD_DISABLE	R/W	0b	LDO1 PULLDOWN CONTROL 0b = Pulldown disabled 1b = Pulldown enabled if not overriden by en_ovst or en_hiz bits

ADVANCE INFORMATION

5.7.1.299 TEST_REG_30 Register (Offset = 0x183) [reset = 0x0]

TEST_REG_30 is shown in Figure 5-366 and described in Table 5-338.

Return to the Summary Table.

Figure 5-366. TEST_REG_30 Register

7	6	5	4	3	2	1	0
RESERVED			OSC_128KHZ_EN	OSC_MONITOR_20MHZ_EN	OSC_20MHZ_EN	OSC_52M8HZ_EN	DPLL_EN
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-338. TEST_REG_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	OSC_128KHZ_EN	R/W	0b	128kHz Oscillator enable 0b = Disabled 1b = Enabled
3	OSC_MONITOR_20MHZ_EN	R/W	0b	20MHz monitoring oscillator enable 0b = Disabled 1b = Enabled
2	OSC_20MHZ_EN	R/W	0b	20MHz main oscillator enable 0b = Disabled 1b = Enabled
1	OSC_52M8HZ_EN	R/W	0b	52.8MHz oscillator enable. This oscillator is used to replace DPLL with a fixed clock if that function is not working properly. 0b = Disabled 1b = Enabled
0	DPLL_EN	R/W	0b	Buck digital PLL enable. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.300 TEST_SRAM_1 Register (Offset = 0x184) [reset = 0x0]

TEST_SRAM_1 is shown in Figure 5-367 and described in Table 5-339.

Return to the Summary Table.

Figure 5-367. TEST_SRAM_1 Register

7	6	5	4	3	2	1	0
RESERVED						TM_SRAM_MARGIN1	TM_SRAM_MARGIN0
R/W-0b						R/W-0b	R/W-0b

Table 5-339. TEST_SRAM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	TM_SRAM_MARGIN1	R/W	0b	SRAM test mode select. MARGIN1 = 0 and MARGIN0 = 0 - Normal mode MARGIN1 = 0 and MARGIN0 = 1 - Pre-charge test MARGIN1 = 1 and MARGIN0 = 0 - Bit-line/Word-line stress MARGIN1 = 1 and MARGIN0 = 1 - DFT Active Normal mode : Mode used in normal functional mode. Pre-charge test : The Pre-charge mode shortens the internally timed bit-line precharge window. The pre-charge test pattern algorithm should be read after write down the column with the read pattern being the inverse of the write pattern. The worst case for pre-charge is not having enough time to charge the bitlines to VDD after a write before a read on the next cycle. To margin this operation we shorten the pre-charge time on the write by using a slower time, then read aggressively with a shorter sense time. Bit-line/Word-line stress : The Bit-line/Word-line test replaces the self timing operation with the input clock. The tester can then stretch the input clock to provide the stress conditions. Normal word-line access and sense-amp turn on is initiated on the rising edge of CLK as usual. The internal timing circuits which would normally truncate these actions is disabled in this mode, and the actions are not ended until the falling edge of CLK. This causes certain critical transistors to remain on for longer than normal periods of time enhancing effects such as NBTI. DFT Active : The DFT Active test shortens the RAM's internal self timing duration for both read and write operation. This is an effective screen for weak bits at probe. The DFT modes are controlled directly from the test chip inputs. MBIST does not select a DFT mode.

Table 5-339. TEST_SRAM_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TM_SRAM_MARGIN0	R/W	0b	SRAM test mode select. MARGIN1 = 0 and MARGIN0 = 0 - Normal mode MARGIN1 = 0 and MARGIN0 = 1 - Pre-charge test MARGIN1 = 1 and MARGIN0 = 0 - Bit-line/Word-line stress MARGIN1 = 1 and MARGIN0 = 1 - DFT Active Normal mode : Mode used in normal functional mode. Pre-charge test : The Pre-charge mode shortens the internally timed bit-line precharge window. The pre-charge test pattern algorithm should be read after write down the column with the read pattern being the inverse of the write pattern. The worst case for pre-charge is not having enough time to charge the bitlines to VDD after a write before a read on the next cycle. To margin this operation we shorten the pre-charge time on the write by using a slower time, then read aggressively with a shorter sense time. Bit-line/Word-line stress : The Bit-line/Word-line test replaces the self timing operation with the input clock. The tester can then stretch the input clock to provide the stress conditions. Normal word-line access and sense-amp turn on is initiated on the rising edge of CLK as usual. The internal timing circuits which would normally truncate these actions is disabled in this mode, and the actions are not ended until the falling edge of CLK. This causes certain critical transistors to remain on for longer than normal periods of time enhancing effects such as NBTI. DFT Active : The DFT Active test shortens the RAM's internal self timing duration for both read and write operation. This is an effective screen for weak bits at probe. The DFT modes are controlled directly from the test chip inputs. MBIST does not select a DFT mode.

ADVANCE INFORMATION

5.7.1.301 TEST_RTC_CAL_0 Register (Offset = 0x188) [reset = 0x0]

TEST_RTC_CAL_0 is shown in Figure 5-368 and described in Table 5-340.

Return to the Summary Table.

Figure 5-368. TEST_RTC_CAL_0 Register

7	6	5	4	3	2	1	0
RESERVED						RTC_TEST_MODE2	RTC_TEST_MODE1
R/W-0b						R/W-0b	R/W-0b

Table 5-340. TEST_RTC_CAL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	RTC_TEST_MODE2	R/W	0b	Causes the prescaler to increment on every clock, independent of whether the 20MHz or the 32KHz is the active clock. 0b = RTC test mode 2 disabled 1b = RTC test mode 2 enabled
0	RTC_TEST_MODE1	R/W	0b	Causes the prescaler to divide by 3 instead of its usual 32768; Thereby speeding up the RTC by a factor of nearly 10000. 0b = RTC test mode 1 disabled 1b = RTC test mode 1 enabled

ADVANCE INFORMATION

5.7.1.302 TEST_PADRING_0 Register (Offset = 0x18A) [reset = 0x0]

TEST_PADRING_0 is shown in Figure 5-369 and described in Table 5-341.

Return to the Summary Table.

Figure 5-369. TEST_PADRING_0 Register

7	6	5	4	3	2	1	0
test_en_drv_tx_dis	test_en_atab_loop_cp_current	test_en_atab_loop_cp					test_en_nint_cp_osc
R/W-0b	R/W-0b	R/W-0b					R/W-0b

Table 5-341. TEST_PADRING_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_en_drv_tx_dis	R/W	0b	EN_DRV output buffer disable. Will be used in input buffer VIL/VIH testing. 0b = Output buffer enabled 1b = Output buffer disabled
6	test_en_atab_loop_cp_current	R/W	0b	enable for current mode output cell used in VMON closed-loop tests. 0b = Disabled 1b = Enabled
5:1	test_en_atab_loop_cp	R/W	0b	enable for current bias distribution in padring. Needed for VMON closed loop tests! 0b = Disabled 1b = Enabled
0	test_en_nint_cp_osc	R/W	0b	OVST charge pump oscillator enable. In addition to this bit, test_en_nint_cp_pd must be set to 0 before CP is fully functional. 0b = Disabled 1b = Enabled

ADVANCE INFORMATION

5.7.1.303 TEST_PADRING_1 Register (Offset = 0x18B) [reset = 0x0]

TEST_PADRING_1 is shown in Figure 5-370 and described in Table 5-342.

Return to the Summary Table.

Figure 5-370. TEST_PADRING_1 Register

7	6	5	4	3	2	1	0
RESERVED			test_en_atab_1v8				
R/W-0b			R/W-0b				

Table 5-342. TEST_PADRING_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	test_en_atab_1v8	R/W	0b	Analog 1.8V main test bus switch. Block mapping is described in LEO testpin definition excel. b00000 - Off b00001 - ATAB1 b00010 - ATAB2 b00100 - ATAB3 b01000 - ATAB4 b10000 - ATAB5

ADVANCE INFORMATION

5.7.1.304 TEST_PADRING_3 Register (Offset = 0x18C) [reset = 0x0]

TEST_PADRING_3 is shown in Figure 5-371 and described in Table 5-343.

Return to the Summary Table.

Figure 5-371. TEST_PADRING_3 Register

7	6	5	4	3	2	1	0
RESERVED			test_en_atab_5v				
R/W-0b			R/W-0b				

Table 5-343. TEST_PADRING_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	test_en_atab_5v	R/W	0b	Analog 5V main test bus switch. Block mapping is described in LEO testpin definition excel. b00000 - Off b00001 - ATAB1 b00010 - ATAB2 b00100 - ATAB3 b01000 - ATAB4 b10000 - ATAB5

ADVANCE INFORMATION

5.7.1.305 TEST_PADRING_4 Register (Offset = 0x18D) [reset = 0x0]

TEST_PADRING_4 is shown in Figure 5-372 and described in Table 5-344.

Return to the Summary Table.

Figure 5-372. TEST_PADRING_4 Register

7	6	5	4	3	2	1	0
RESERVED			test_en_kelvin_12_8				
R/W-0b			R/W-0b				

Table 5-344. TEST_PADRING_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	test_en_kelvin_12_8	R/W	0b	MSB(12_8) LSB(7_0) Bit<13> 0x10 0x00 – LDO1 output kelvin Bit<12> 0x08 0x00 – LDO4 input kelvin Bit<11> 0x04 0x00 – VCCA kelvin Bit<10> 0x02 0x00 – LDO2 output kelvin Bit<9> 0x01 0x00 – LDO3 input kelvin Bit>8> 0x00 0x80 – LDO3 output kelvin Bit<7> 0x00 0x40 – LDO1_2 input kelvin Bit<6> 0x00 0x20 – INT LDO output = VDDA kelvin Bit<5> 0x00 0x10 – LDO4 output kelvin Bit<4> 0x00 0x08 – RTC LDO output kelvin Bit<3> 0x00 0x04 – PBKG kelvin Bit<2> 0x00 0x02 – REF_GND kelvin Bit<1> 0x00 0x01 - Reserved

5.7.1.306 TEST_PADRING_5 Register (Offset = 0x18E) [reset = 0x0]

TEST_PADRING_5 is shown in Figure 5-373 and described in Table 5-345.

Return to the Summary Table.

Figure 5-373. TEST_PADRING_5 Register

7	6	5	4	3	2	1	0
test_en_kelvin_7_0							
R/W-0b							

Table 5-345. TEST_PADRING_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	test_en_kelvin_7_0	R/W	0b	MSB(12_8) LSB(7_0) Bit<13> 0x10 0x00 – LDO1 output kelvin Bit<12> 0x08 0x00 – LDO4 input kelvin Bit<11> 0x04 0x00 – VCCA kelvin Bit<10> 0x02 0x00 – LDO2 output kelvin Bit<9> 0x01 0x00 – LDO3 input kelvin Bit>8> 0x00 0x80 – LDO3 output kelvin Bit<7> 0x00 0x40 – LDO1_2 input kelvin Bit<6> 0x00 0x20 – INT LDO output = VDDA kelvin Bit<5> 0x00 0x10 – LDO4 output kelvin Bit<4> 0x00 0x08 – RTC LDO output kelvin Bit<3> 0x00 0x04 – PBKG kelvin Bit<2> 0x00 0x02 – REF_GND kelvin Bit<1> 0x00 0x01 - Reserved

ADVANCE INFORMATION

5.7.1.307 TEST_PADRING_6 Register (Offset = 0x18F) [reset = 0x0]

TEST_PADRING_6 is shown in Figure 5-374 and described in Table 5-346.

Return to the Summary Table.

Figure 5-374. TEST_PADRING_6 Register

7	6	5	4	3	2	1	0
RESERVED			test_en_atab_loop_rc				
R/W-0b			R/W-0b				

Table 5-346. TEST_PADRING_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	test_en_atab_loop_rc	R/W	0b	Comparator closed loop trim RC mode as depicted in LEO testpin definition b00000 - Off b00001 - RC1 (GPIO1) b00010 - RC2 (GPIO2) b00100 - RC3 (nRSTOUT) b01000 - RC4 (GPIO7) b10000 - RC5 (GPIO8)

5.7.1.308 TEST_PADRING_7 Register (Offset = 0x190) [reset = 0x0]

TEST_PADRING_7 is shown in Figure 5-375 and described in Table 5-347.

Return to the Summary Table.

Figure 5-375. TEST_PADRING_7 Register

7	6	5	4	3	2	1	0
RESERVED		test_dis_nint_cp_pd	TEST_PADRING_SPARE				
R/W-0b		R/W-0b	R/W-0b				

Table 5-347. TEST_PADRING_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_dis_nint_cp_pd	R/W	0b	HV TESTBUS PULLDOWN CONTROL (HV testbus connected to NINT pin) 0b = HV testbus pulldown enabled 1b = HV testbus pulldown disabled
4:0	TEST_PADRING_SPARE	R/W	0b	

ADVANCE INFORMATION

5.7.1.309 TEST_VMVCCA_0 Register (Offset = 0x191) [reset = 0x0]

TEST_VMVCCA_0 is shown in Figure 5-376 and described in Table 5-348.

Return to the Summary Table.

Figure 5-376. TEST_VMVCCA_0 Register

7	6	5	4	3	2	1	0
RESERVED					test_vmvcca_iptat	test_vmvcca_vref_1v2	test_vmvcca_bg
R/W-0b					R/W-0b	R/W-0b	R/W-0b

Table 5-348. TEST_VMVCCA_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	test_vmvcca_iptat	R/W	0b	Test switch to connect 500nA PTAT PMOS type bias current in VMVCCA to ATAB_5V_1
1	test_vmvcca_vref_1v2	R/W	0b	Test switch to connect output of the vref resistor divider in VMVCCA to ATAB_5V_1
0	test_vmvcca_bg	R/W	0b	Test switch to connect output of the bandgap in VMVCCA to ATAB_5V_1

ADVANCE INFORMATION

5.7.1.310 TEST_VMPVIN_0 Register (Offset = 0x192) [reset = 0x0]

TEST_VMPVIN_0 is shown in Figure 5-377 and described in Table 5-349.

Return to the Summary Table.

Figure 5-377. TEST_VMPVIN_0 Register

7	6	5	4	3	2	1	0
RESERVED					test_vmpvin_iptat	test_vmpvin_vref_1v2	test_vmpvin_bg
R/W-0b					R/W-0b	R/W-0b	R/W-0b

Table 5-349. TEST_VMPVIN_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	test_vmpvin_iptat	R/W	0b	Test switch to connect 500nA PTAT PMOS type bias current in VMVCCA to ATAB_5V_1
1	test_vmpvin_vref_1v2	R/W	0b	Test switch to connect output of the vref resistor divider in VMVCCA to ATAB_5V_1
0	test_vmpvin_bg	R/W	0b	Test switch to connect output of the bandgap in VMVCCA to ATAB_5V_1

ADVANCE INFORMATION

5.7.1.311 TEST_INT_0 Register (Offset = 0x193) [reset = 0x0]

TEST_INT_0 is shown in Figure 5-378 and described in Table 5-350.

Return to the Summary Table.

Figure 5-378. TEST_INT_0 Register

7	6	5	4	3	2	1	0
test_refsys_iptat	test_refsys_ldo_int_en_ilim2	test_refsys_ldo_int_en_ilim	test_refsys_ldo_int_pupd_hiz	test_refsys_ldo_int_en_ovst	test_refsys_ldo_int_en_vout_kelvin	test_refsys_bg	test_refsys_ibias
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-350. TEST_INT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_refsys_iptat	R/W	0b	Test switch to connect 500nA IPTAT current from PMOS current source to ATAB_5V0_3
6	test_refsys_ldo_int_en_ilim2	R/W	0b	Scale INT LDO current limit branch 2 down so that ILIM<200mA.
5	test_refsys_ldo_int_en_ilim	R/W	0b	Scale INT LDO current limit branch 1 down so that ILIM<200mA.
4	test_refsys_ldo_int_pupd_hiz	R/W	0b	Force REFSYS INT LDO output to HiZ
3	test_refsys_ldo_int_en_ovst	R/W	0b	REFSYS_INT LDO OVST enable. Refer to OVST document for details.
2	test_refsys_ldo_int_en_vout_kelvin	R/W	0b	Not used.
1	test_refsys_bg	R/W	0b	Test switch to connect REFSYS_INT bandgap output to ATAB_5V_3
0	test_refsys_ibias	R/W	0b	Test switch to connect REFSYS_INT 0TC 500nA PMOS type current to ATAB_1V8_3

5.7.1.312 TEST_INT_1 Register (Offset = 0x194) [reset = 0x0]

TEST_INT_1 is shown in Figure 5-379 and described in Table 5-351.

Return to the Summary Table.

Figure 5-379. TEST_INT_1 Register

7	6	5	4	3	2	1	0
RESERVED				test_refsys_ldo_int_out_stage_dis	test_refsys_amux_buffer_en_hiz	test_refsys_bg_buffer_en_hiz	test_refsys_bg_buffer
R/W-0b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-351. TEST_INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	test_refsys_ldo_int_out_stage_dis	R/W	0b	Disable REFSYS_INT LDO output stage so that output can be forced higher/lower than target voltage.
2	test_refsys_amux_buffer_en_hiz	R/W	0b	Disable REFSYS_INT AMUXOUT pin buffer pull-down so that AMUX pin can be freely forced high/low
1	test_refsys_bg_buffer_en_hiz	R/W	0b	Force bandgap reference buffer output to be high impedance
0	test_refsys_bg_buffer	R/W	0b	Connect bandgap buffer output to ATAB_5V_3

ADVANCE INFORMATION

5.7.1.313 TEST_SAFETY_0 Register (Offset = 0x195) [reset = 0x0]

TEST_SAFETY_0 is shown in Figure 5-380 and described in Table 5-352.

Return to the Summary Table.

Figure 5-380. TEST_SAFETY_0 Register

7	6	5	4	3	2	1	0
test_vmon_buck					test_tsd		
R/W-0b					R/W-0b		

Table 5-352. TEST_SAFETY_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	test_vmon_buck	R/W	0b	Test switch to connect VMON Buck OV and UV comparator inputs to ATAB_1V8_1-4
2:0	test_tsd	R/W	0b	Test_tsd<2:0> <2> Test control for tsd comparator sensor input mux <1> Test control for tsd atab mux <0> Test control for tsd atab mux

ADVANCE INFORMATION

5.7.1.314 TEST_SAFETY_1 Register (Offset = 0x196) [reset = 0x0]

TEST_SAFETY_1 is shown in Figure 5-381 and described in Table 5-353.

Return to the Summary Table.

Figure 5-381. TEST_SAFETY_1 Register

7	6	5	4	3	2	1	0
test_safety_bg_buffer_en_hiz	test_vmon_vcca		test_safety_ibias	test_vmon_ldo			
R/W-0b	R/W-0b		R/W-0b	R/W-0b			

Table 5-353. TEST_SAFETY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_safety_bg_buffer_en_hiz	R/W	0b	Force SAFETY bandgap buffer output to HiZ
6:5	test_vmon_vcca	R/W	0b	01 - Will connect VCCA VMON OV and UV comparator inputs to ATAB_1V8_1-4 10 - Will connect 0.600V reference to ATAB_1V8_4
4	test_safety_ibias	R/W	0b	Test switch to connect SAFETY temperature independent 100nA PMOS type bias current to ATAB1
3:0	test_vmon_ldo	R/W	0b	Test switch to connect VMON LDO OV and UV comparator inputs to ATAB_1V8_1-4

ADVANCE INFORMATION

5.7.1.315 TEST_SAFETY_2 Register (Offset = 0x197) [reset = 0x0]

TEST_SAFETY_2 is shown in Figure 5-382 and described in Table 5-354.

Return to the Summary Table.

Figure 5-382. TEST_SAFETY_2 Register

7	6	5	4	3	2	1	0
RESERVED						test_safety_vref_1v2	test_safety_bias_dist
R/W-0b						R/W-0b	R/W-0b

Table 5-354. TEST_SAFETY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	test_safety_vref_1v2	R/W	0b	Test switch to connect buffered 1.2V SAFETY bandgap voltage to ATAB_1V8_1
0	test_safety_bias_dist	R/W	0b	Test switch to connect SAFETY 0TC 100nA PMOS type current to ATAB_1V8_1

5.7.1.316 TEST_VM_VSYS_0 Register (Offset = 0x198) [reset = 0x0]

TEST_VM_VSYS_0 is shown in Figure 5-383 and described in Table 5-355.

Return to the Summary Table.

Figure 5-383. TEST_VM_VSYS_0 Register

7	6	5	4	3	2	1	0
RESERVED	test_vsys_vref_ramp	test_vsys_en_cp_osc	test_vsys_cp_voltage	test_vsys_ibias	test_vsys_bg	test_vsys_vdda_voltage	test_vsys_en_ovst
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-355. TEST_VM_VSYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	test_vsys_vref_ramp	R/W	0b	Test switch to connect startup bandgap ramp to ATAB_1V8_1
5	test_vsys_en_cp_osc	R/W	0b	Enable for the VSYS charge pump oscillator
4	test_vsys_cp_voltage	R/W	0b	Test switch to connect charge pump internal max. 5V power supply to ATAB_1V8_1V_1
3	test_vsys_ibias	R/W	0b	Test switch to connect 100nA PMOS type bias current to ATAB_5V_1
2	test_vsys_bg	R/W	0b	Test switch to connect bandgap resistor divider to ATAB_1V8_1
1	test_vsys_vdda_voltage	R/W	0b	Test switch to connect analog internal max. 5V power supply to ATAB_5V_1
0	test_vsys_en_ovst	R/W	0b	OVST test switch enable so that VSYS_SENSE voltage connects to internal VDDA and CP_VOLTAGE power rails and their filters.

5.7.1.317 TEST_RTC_0 Register (Offset = 0x199) [reset = 0x0]

TEST_RTC_0 is shown in Figure 5-384 and described in Table 5-356.

Return to the Summary Table.

Figure 5-384. TEST_RTC_0 Register

7	6	5	4	3	2	1	0
test_rtc_ldo_pldn	test_rtc_iptat	test_rtc_ldo_en_ilim2	test_rtc_ldo_en_ilim	test_rtc_ldo_pupd_hiz	test_rtc_ldo_en_ovst	test_rtc_ldo_en_vout_kelvin	test_rtc_bg
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-356. TEST_RTC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_rtc_ldo_pldn	R/W	0b	LDO_RTC PULLDOWN CONTROL 0b = Pulldown disabled 1b = Pulldown enabled, if not prevented by en_hiz or ovst control bits
6	test_rtc_iptat	R/W	0b	Test switch to connect 500nA IPTAT current from PMOS current source to ATAB_5V0_4
5	test_rtc_ldo_en_ilim2	R/W	0b	LDO_RTC secondary current limit level selection 0b = Current limit level is 350mA, if test_rtc_ldo_en_ilim is also 0 1b = Current limit level is 50mA
4	test_rtc_ldo_en_ilim	R/W	0b	LDO_RTC primary current limit level selection 0b = Current limit level is 180mA, , if test_rtc_ldo_en_ilim2 is also 0 1b = Current limit level is 45mA
3	test_rtc_ldo_pupd_hiz	R/W	0b	LDO_RTC pull down disable control 0b = Pulldown is active when LDO is disabled 1b = Pulldown is disabled and LDO pull down resistor is in HiZ
2	test_rtc_ldo_en_ovst	R/W	0b	LDO_RTC OVST enable, which disabled pull down and reconfigures compensation capacitor for OVST
1	test_rtc_ldo_en_vout_kelvin	R/W	0b	Not used.
0	test_rtc_bg	R/W	0b	Test switch to connect bandgap resistor divider to ATAB_5V0_4

ADVANCE INFORMATION

5.7.1.318 TEST_RTC_1 Register (Offset = 0x19A) [reset = 0x0]

TEST_RTC_1 is shown in Figure 5-385 and described in Table 5-357.

Return to the Summary Table.

Figure 5-385. TEST_RTC_1 Register

7	6	5	4	3	2	1	0
RESERVED						test_rtc_ldo_out_stage_dis	test_rtc_xtal
R/W-0b						R/W-0b	R/W-0b

Table 5-357. TEST_RTC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	test_rtc_ldo_out_stage_dis	R/W	0b	LDO_RTC output stage control 0b = Output stage can operate normally 1b = Ouput stage is forced to HiZ
0	test_rtc_xtal	R/W	0b	CRYSTAL OSCILLATOR TEST CONTROL 0b = Crystal osc bias current testmode not active 1b = Crystal osc bias current connected to analog testbus

ADVANCE INFORMATION

5.7.1.319 TEST_LDO1_3_FILT_0 Register (Offset = 0x19B) [reset = 0x0]

TEST_LDO1_3_FILT_0 is shown in Figure 5-386 and described in Table 5-358.

Return to the Summary Table.

Figure 5-386. TEST_LDO1_3_FILT_0 Register

7	6	5	4	3	2	1	0
RESERVED						vbg_filt_test	
R/W-0b						R/W-0b	

Table 5-358. TEST_LDO1_3_FILT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1:0	vbg_filt_test	R/W	0b	Test mode for RC filter 0b = Normal mode 1b = Forced filter mode independent of ldo internal sequencing during startup 10b = Bypass filter resistor 11b = Bypass filter resistor and forced filter mode independent of ldo internal sequencing during startup

ADVANCE INFORMATION

5.7.1.320 TEST_LDO1_0 Register (Offset = 0x19C) [reset = 0x0]

TEST_LDO1_0 is shown in Figure 5-387 and described in Table 5-359.

Return to the Summary Table.

Figure 5-387. TEST_LDO1_0 Register

7	6	5	4	3	2	1	0
ldo1_dis_ilim2	ldo1_dis_ilim1	ldo1_en_ilim_trim	ldo1_en_ldo_vref_hiz	ldo1_en_ldo_vref	ldo1_en_unity_gain	ldo1_en_hiz	ldo1_en_ovst
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-359. TEST_LDO1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ldo1_dis_ilim2	R/W	0b	Disable current limit protection comparator 2 0b = Normal mode 1b = Disable current limit comparator 2
6	ldo1_dis_ilim1	R/W	0b	Disable current limit protection comparator 1 0b = Normal mode 1b = Disable current limit comparator 1
5	ldo1_en_ilim_trim	R/W	0b	Reduce current limit threshold to 1/7 for trimming 0b = Normal mode 1b = Reduce current limit threshold to 1/7
4	ldo1_en_ldo_vref_hiz	R/W	0b	HiZ LDO reference buffer output and force it with AMUX 0b = Normal mode 1b = HiZ LDO reference buffer output
3	ldo1_en_ldo_vref	R/W	0b	Send LDO reference buffer output to AMUX 0b = Normal mode 1b = Send LDO reference buffer output to AMUX for trimming
2	ldo1_en_unity_gain	R/W	0b	Bypass divided-by-2 feedback resistor divider to config LDO to unity gain 0b = Normal mode 1b = Force LDO in unity gain config for trimming
1	ldo1_en_hiz	R/W	0b	Disable output pull down 0b = Normal mode 1b = Disable output pulldown
0	ldo1_en_ovst	R/W	0b	Enable OVST mode 0b = 0 - Normal mode 1 - OVST mode 1b = 0 - Normal mode 1 - OVST mode

ADVANCE INFORMATION

5.7.1.321 TEST_LDO1_1 Register (Offset = 0x19D) [reset = 0x0]

TEST_LDO1_1 is shown in Figure 5-388 and described in Table 5-360.

Return to the Summary Table.

Figure 5-388. TEST_LDO1_1 Register

7	6	5	4	3	2	1	0
RESERVED						ldo1_cp_test_sel	ldo1_en_cp_test_mode
R/W-0b						R/W-0b	R/W-0b

Table 5-360. TEST_LDO1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	ldo1_cp_test_sel	R/W	0b	LDO internal charge pump test mux channel select, only active when ldo_en_cp_test_mode = 1 0b = Select Holding capacitor top plate (Power FET gate) 1b = Select Holding capacitor bottom plate (Error amp output)
0	ldo1_en_cp_test_mode	R/W	0b	Enable LDO internal charge pump test mux 0b = Disable test muxes 1b = Enable test muxes

ADVANCE INFORMATION

5.7.1.322 TEST_LDO2_0 Register (Offset = 0x19E) [reset = 0x0]

TEST_LDO2_0 is shown in Figure 5-389 and described in Table 5-361.

Return to the Summary Table.

Figure 5-389. TEST_LDO2_0 Register

7	6	5	4	3	2	1	0
ldo2_dis_ilim2	ldo2_dis_ilim1	ldo2_en_ilim_trim	ldo2_en_ldo_vref_hiz	ldo2_en_ldo_vref	ldo2_en_unity_gain	ldo2_en_hiz	ldo2_en_ovst
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-361. TEST_LDO2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ldo2_dis_ilim2	R/W	0b	Disable current limit protection comparator 2 0b = Normal mode 1b = Disable current limit comparator 2
6	ldo2_dis_ilim1	R/W	0b	Disable current limit protection comparator 1 0b = Normal mode 1b = Disable current limit comparator 1
5	ldo2_en_ilim_trim	R/W	0b	Reduce current limit threshold to 1/7 for trimming 0b = Normal mode 1b = Reduce current limit threshold to 1/7
4	ldo2_en_ldo_vref_hiz	R/W	0b	HiZ LDO reference buffer output and force it with AMUX 0b = Normal mode 1b = HiZ LDO reference buffer output
3	ldo2_en_ldo_vref	R/W	0b	Send LDO reference buffer output to AMUX 0b = Normal mode 1b = Send LDO reference buffer output to AMUX for trimming
2	ldo2_en_unity_gain	R/W	0b	Bypass divided-by-2 feedback resistor divider to config LDO to unity gain 0b = Normal mode 1b = Force LDO in unity gain config for trimming
1	ldo2_en_hiz	R/W	0b	Disable output pull down 0b = Normal mode 1b = Disable output pulldown
0	ldo2_en_ovst	R/W	0b	Enable OVST mode 0b = 0 - Normal mode 1 - OVST mode 1b = 0 - Normal mode 1 - OVST mode

ADVANCE INFORMATION

5.7.1.323 TEST_LDO2_1 Register (Offset = 0x19F) [reset = 0x0]

TEST_LDO2_1 is shown in Figure 5-390 and described in Table 5-362.

Return to the Summary Table.

Figure 5-390. TEST_LDO2_1 Register

7	6	5	4	3	2	1	0
RESERVED						ldo2_cp_test_sel	ldo2_en_cp_test_mode
R/W-0b						R/W-0b	R/W-0b

Table 5-362. TEST_LDO2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	ldo2_cp_test_sel	R/W	0b	LDO internal charge pump test mux channel select, only active when ldo_en_cp_test_mode = 1 0b = Select Holding capacitor top plate (Power FET gate) 1b = Select Holding capacitor bottom plate (Error amp output)
0	ldo2_en_cp_test_mode	R/W	0b	Enable LDO internal charge pump test mux 0b = Disable test muxes 1b = Enable test muxes

ADVANCE INFORMATION

5.7.1.324 TEST_LDO3_0 Register (Offset = 0x1A0) [reset = 0x0]

TEST_LDO3_0 is shown in Figure 5-391 and described in Table 5-363.

Return to the Summary Table.

Figure 5-391. TEST_LDO3_0 Register

7	6	5	4	3	2	1	0
ldo3_dis_ilim2	ldo3_dis_ilim1	ldo3_en_ilim_trim	ldo3_en_ldo_vref_hiz	ldo3_en_ldo_vref	ldo3_en_unity_gain	ldo3_en_hiz	ldo3_en_ovst
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-363. TEST_LDO3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ldo3_dis_ilim2	R/W	0b	Disable current limit protection comparator 2 0b = Normal mode 1b = Disable current limit comparator 2
6	ldo3_dis_ilim1	R/W	0b	Disable current limit protection comparator 1 0b = Normal mode 1b = Disable current limit comparator 1
5	ldo3_en_ilim_trim	R/W	0b	Reduce current limit threshold to 1/7 for trimming 0b = Normal mode 1b = Reduce current limit threshold to 1/7
4	ldo3_en_ldo_vref_hiz	R/W	0b	HiZ LDO reference buffer output and force it with AMUX 0b = Normal mode 1b = HiZ LDO reference buffer output
3	ldo3_en_ldo_vref	R/W	0b	Send LDO reference buffer output to AMUX 0b = Normal mode 1b = Send LDO reference buffer output to AMUX for trimming
2	ldo3_en_unity_gain	R/W	0b	Bypass divided-by-2 feedback resistor divider to config LDO to unity gain 0b = Normal mode 1b = Force LDO in unity gain config for trimming
1	ldo3_en_hiz	R/W	0b	Disable output pull down 0b = Normal mode 1b = Disable output pulldown
0	ldo3_en_ovst	R/W	0b	Enable OVST mode 0b = 0 - Normal mode 1 - OVST mode 1b = 0 - Normal mode 1 - OVST mode

ADVANCE INFORMATION

5.7.1.325 TEST_LDO3_1 Register (Offset = 0x1A1) [reset = 0x0]

TEST_LDO3_1 is shown in Figure 5-392 and described in Table 5-364.

Return to the Summary Table.

Figure 5-392. TEST_LDO3_1 Register

7	6	5	4	3	2	1	0
RESERVED						ldo3_cp_test_sel	ldo3_en_cp_test_mode
R/W-0b						R/W-0b	R/W-0b

Table 5-364. TEST_LDO3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	ldo3_cp_test_sel	R/W	0b	LDO internal charge pump test mux channel select, only active when ldo_en_cp_test_mode = 1 0b = Select Holding capacitor top plate (Power FET gate) 1b = Select Holding capacitor bottom plate (Error amp output)
0	ldo3_en_cp_test_mode	R/W	0b	Enable LDO internal charge pump test mux 0b = Disable test muxes 1b = Enable test muxes

ADVANCE INFORMATION

5.7.1.326 TEST_LDO4_0 Register (Offset = 0x1A2) [reset = 0x0]

TEST_LDO4_0 is shown in Figure 5-393 and described in Table 5-365.

Return to the Summary Table.

Figure 5-393. TEST_LDO4_0 Register

7	6	5	4	3	2	1	0
RESERVED	ldo4_test_en_faster_trim	ldo4_en_ovst2	ldo4_en_hiz	ldo4_en_kelvin	ldo4_en_ovst	ldo4_test_en_ilim2	ldo4_test_en_ilim
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-365. TEST_LDO4_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	ldo4_test_en_faster_trim	R/W	0b	LDO4 noise filter bypass enable that speeds up LDO4 VREF settling 0b = Disabled 1b = Enabled
5	ldo4_en_ovst2	R/W	0b	LDO4 OVST enable, which disables pull down and enables error amplifier compensation capacitor for OVST 0b = OVST disabled 1b = OVST enabled
4	ldo4_en_hiz	R/W	0b	LDO4 pull down disable control 0b = Pulldown is active when LDO is disabled 1b = Pulldown is disabled and LDO pull down resistor is in HiZ
3	ldo4_en_kelvin	R/W	0b	Not used.
2	ldo4_en_ovst	R/W	0b	LDO4 OVST enable, which disabled pull down and enables noise filter and pass fet for OVST 0b = Disabled 1b = Enabled
1	ldo4_test_en_ilim2	R/W	0b	LDO4 current limit test mode control 0b = Current limit level is 600mA, if ldo4_test_en_ilim is also 0 1b = Current limit level is 125mA
0	ldo4_test_en_ilim	R/W	0b	LDO4 current limit test mode control 0b = Current limit level is 600mA, if ldo4_test_en_ilim2 is also 0 1b = Current limit level is 125mA

ADVANCE INFORMATION

5.7.1.327 TEST_EE_LDO_0 Register (Offset = 0x1A3) [reset = 0x0]

TEST_EE_LDO_0 is shown in Figure 5-394 and described in Table 5-366.

Return to the Summary Table.

Figure 5-394. TEST_EE_LDO_0 Register

7	6	5	4	3	2	1	0
RESERVED				test_en_tmux2_in	test_en_tmux1_in	test_dft_iddq_scale	
R/W-0b				R/W-0b	R/W-0b	R/W-0b	

Table 5-366. TEST_EE_LDO_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3	test_en_tmux2_in	R/W	0b	EEPROM LDO low current vout test switch 0b = Disabled 1b = Enabled
2	test_en_tmux1_in	R/W	0b	EEPROM LDO high current vout test switch 0b = Disabled 1b = Enabled
1:0	test_dft_iddq_scale	R/W	0b	Test bit to scale down EEPROM LDO bias current. 0b = 100% bias current 1b = 75% bias current 10b = 50% bias current 11b = 25% bias current

ADVANCE INFORMATION

5.7.1.328 TEST_BB_0 Register (Offset = 0x1A4) [reset = 0x0]

TEST_BB_0 is shown in Figure 5-395 and described in Table 5-367.

Return to the Summary Table.

Figure 5-395. TEST_BB_0 Register

7	6	5	4	3	2	1	0
RESERVED				TEST_BB_SPARE			
R/W-0b				R/W-0b			

Table 5-367. TEST_BB_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	TEST_BB_SPARE	R/W	0b	

5.7.1.329 BUCK1_ATEST_REG_0 Register (Offset = 0x1A5) [reset = 0x0]

BUCK1_ATEST_REG_0 is shown in Figure 5-396 and described in Table 5-368.

Return to the Summary Table.

Figure 5-396. BUCK1_ATEST_REG_0 Register

7	6	5	4	3	2	1	0
test_ramp_emu_1	test_ramp_artif_pd_1	test_ramp_artif_1	test_integ_dac_short_output_1	buck_atab_sel_1			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-368. BUCK1_ATEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_ramp_emu_1	R/W	0b	activates ramp_emu oscillator test mode
6	test_ramp_artif_pd_1	R/W	0b	pull down artif ramp outputs
5	test_ramp_artif_1	R/W	0b	activates ramp_artif oscillator test mode
4	test_integ_dac_short_output_1	R/W	0b	short integrator dac outputs
3:0	buck_atab_sel_1	R/W	0b	connects internal nets to atab.

ADVANCE INFORMATION

5.7.1.330 BUCK1_ATEST_REG_1 Register (Offset = 0x1A6) [reset = 0x0]

BUCK1_ATEST_REG_1 is shown in Figure 5-397 and described in Table 5-369.

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Figure 5-397. BUCK1_ATEST_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED		test_sw_short_detector_1	test_ovst_1		test_hs_gate_1	test_iave_1	test_ramp_emu_pd_1
R/W-0b		R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 5-369. BUCK1_ATEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_sw_short_detector_1	R/W	0b	Muxes short detector latches set signals instead of latches outputs.
4:3	test_ovst_1	R/W	0b	Not used
2	test_hs_gate_1	R/W	0b	connect hs gate to atab_hv test bus
1	test_iave_1	R/W	0b	bypass for average current level shifting function
0	test_ramp_emu_pd_1	R/W	0b	shorts ramp generating capacitors to ground, output is still ac coupled

ADVANCE INFORMATION

5.7.1.331 BUCK1_ATEST_REG_2 Register (Offset = 0x1A7) [reset = 0x0]

BUCK1_ATEST_REG_2 is shown in Figure 5-398 and described in Table 5-370.

Return to the Summary Table.

Figure 5-398. BUCK1_ATEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED					test_spare_1		
R/W-0b					R/W-0b		

Table 5-370. BUCK1_ATEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	test_spare_1	R/W	0b	

5.7.1.332 BUCK1_DTEST_REG_0 Register (Offset = 0x1A8) [reset = 0x0]

BUCK1_DTEST_REG_0 is shown in Figure 5-399 and described in Table 5-371.

Return to the Summary Table.

Figure 5-399. BUCK1_DTEST_REG_0 Register

7	6	5	4	3	2	1	0
force_pfm_1	swc_buck_hiz_1	swc_buck_hs_1	buck_dtab0_sel_1				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-371. BUCK1_DTEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	force_pfm_1	R/W	0b	Forces buck to PFM when buck_mode is enabled for auto mode (not buck testmode)
6	swc_buck_hiz_1	R/W	0b	Sets switches to HIZ.
5	swc_buck_hs_1	R/W	0b	(1=hs on & ls off, 0=ls on & hs off) --hs needs also gate voltage force and swc_buck_hiz must be 0.
4:0	buck_dtab0_sel_1	R/W	0b	Selection for buck digital test bus0.

ADVANCE INFORMATION

5.7.1.333 BUCK1_DTEST_REG_1 Register (Offset = 0x1A9) [reset = 0x0]

BUCK1_DTEST_REG_1 is shown in Figure 5-400 and described in Table 5-372.

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Figure 5-400. BUCK1_DTEST_REG_1 Register

7	6	5	4	3	2	1	0
test_pulse_generator_1	test_sample_izero_1	test_iave_pd_1	buck_dtab1_sel_1				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-372. BUCK1_DTEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_pulse_generator_1	R/W	0b	Sets HS and LS pulse generators to oscillator mode. Pulse generator length can be controlled with test_integrator_word. When test_pulse_gen_fixed is set, this defines which of the HS or LS pulse generator has fixed length
6	test_sample_izero_1	R/W	0b	izero comparator latches sw pin voltage at negedge of this signal
5	test_iave_pd_1	R/W	0b	Enables pull down for the i_ave signals (loop_comp input pair 2)
4:0	buck_dtab1_sel_1	R/W	0b	Selection for buck digital test bus1.

5.7.1.334 BUCK1_DTEST_REG_2 Register (Offset = 0x1AA) [reset = 0x0]

BUCK1_DTEST_REG_2 is shown in Figure 5-401 and described in Table 5-373.

Return to the Summary Table.

Figure 5-401. BUCK1_DTEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED		test_bypass_ramp_bias_res_1	test_buck_weak_driver_1	dis_vref_filter_1	dis_loop_comp_hyst_1	test_blank_1	test_single_shot_1
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-373. BUCK1_DTEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_bypass_ramp_bias_res_1	R/W	0b	When high, emulated ramp DC bias resistor is bypassed
4	test_buck_weak_driver_1	R/W	0b	0 - weak driver hiz 1 - weak driver high
3	dis_vref_filter_1	R/W	0b	This register has two functions in testmode: 1. Bypass vref filter 2. Bypass load monitor filter
2	dis_loop_comp_hyst_1	R/W	0b	Disables loop comparator negative hysteresis
1	test_blank_1	R/W	0b	Sets all single shots to oscillator mode with blank feedback
0	test_single_shot_1	R/W	0b	Sets all single shots to oscillator mode.

ADVANCE INFORMATION

5.7.1.335 BUCK1_DTEST_REG_3 Register (Offset = 0x1AB) [reset = 0x0]

BUCK1_DTEST_REG_3 is shown in Figure 5-402 and described in Table 5-374.

Return to the Summary Table.

Figure 5-402. BUCK1_DTEST_REG_3 Register

7	6	5	4	3	2	1	0
test_integrator_word_1							
R/W-0b							

Table 5-374. BUCK1_DTEST_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	test_integrator_word_1	R/W	0b	These bits controls in testmode: 1. Integrator digital word 2. pulse generator delay selection 3. sel_load_ref[4:0] (Load monitor reference level)

5.7.1.336 BUCK1_DTEST_REG_4 Register (Offset = 0x1AC) [reset = 0x0]

BUCK1_DTEST_REG_4 is shown in Figure 5-403 and described in Table 5-375.

Return to the Summary Table.

Figure 5-403. BUCK1_DTEST_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED			test_bypass_sw_latches_1	test_pulse_gen_fixed_1	test_dis_autozero_1	test_carousel_ctrl_1	
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-375. BUCK1_DTEST_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	test_bypass_sw_latches_1	R/W	0b	When enabled buck_hiz and buck_hs can be controlled by test_buck_hiz and test_buck_hs bits
3	test_pulse_gen_fixed_1	R/W	0b	When test_pulse_gen_fixed is set, test_pulse_generator defines which one of LS or HS pulse generator is set to fixed value: 0:Pulse generator LS length is fixed and HS is controlled with test_integrator_word 1:Pulse generator HS length is fixed and LS is controlled with test_integrator_word
2	test_dis_autozero_1	R/W	0b	Disables isense and ibal autozero
1:0	test_carousel_ctrl_1	R/W	0b	Test control for isense LS and HS comparators 0:Carousel normal operation 1:sel_comp = 0 2:sel_comp = 1 3:sel_comp = 2

ADVANCE INFORMATION

5.7.1.337 BUCK2_ATEST_REG_0 Register (Offset = 0x1AE) [reset = 0x0]

BUCK2_ATEST_REG_0 is shown in Figure 5-404 and described in Table 5-376.

Return to the Summary Table.

Figure 5-404. BUCK2_ATEST_REG_0 Register

7	6	5	4	3	2	1	0
test_ramp_emu_2	test_ramp_artif_pd_2	test_ramp_artif_2	test_integ_dac_short_output_2	buck_atab_sel_2			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-376. BUCK2_ATEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_ramp_emu_2	R/W	0b	activates ramp_emu oscillator test mode
6	test_ramp_artif_pd_2	R/W	0b	pull down artif ramp outputs
5	test_ramp_artif_2	R/W	0b	activates ramp_artif oscillator test mode
4	test_integ_dac_short_output_2	R/W	0b	short integrator dac outputs
3:0	buck_atab_sel_2	R/W	0b	connects internal nets to atab.

ADVANCE INFORMATION

5.7.1.338 BUCK2_ATEST_REG_1 Register (Offset = 0x1AF) [reset = 0x0]

BUCK2_ATEST_REG_1 is shown in Figure 5-405 and described in Table 5-377.

Return to the Summary Table.

Figure 5-405. BUCK2_ATEST_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED		test_sw_short_detector_2	test_ovst_2		test_hs_gate_2	test_iave_2	test_ramp_emu_pd_2
R/W-0b		R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 5-377. BUCK2_ATEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_sw_short_detector_2	R/W	0b	Muxes short detector latches set signals instead of latches outputs.
4:3	test_ovst_2	R/W	0b	Not used
2	test_hs_gate_2	R/W	0b	connect hs gate to atab_hv test bus
1	test_iave_2	R/W	0b	bypass for average current level shifting function
0	test_ramp_emu_pd_2	R/W	0b	shorts ramp generating capacitors to ground, output is still ac coupled

ADVANCE INFORMATION

5.7.1.339 BUCK2_ATEST_REG_2 Register (Offset = 0x1B0) [reset = 0x0]

BUCK2_ATEST_REG_2 is shown in Figure 5-406 and described in Table 5-378.

Return to the Summary Table.

Figure 5-406. BUCK2_ATEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED					test_spare_2		
R/W-0b					R/W-0b		

Table 5-378. BUCK2_ATEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	test_spare_2	R/W	0b	

5.7.1.340 BUCK2_DTEST_REG_0 Register (Offset = 0x1B1) [reset = 0x0]

BUCK2_DTEST_REG_0 is shown in Figure 5-407 and described in Table 5-379.

Return to the Summary Table.

Figure 5-407. BUCK2_DTEST_REG_0 Register

7	6	5	4	3	2	1	0
force_pfm_2	swc_buck_hiz_2	swc_buck_hs_2	buck_dtab0_sel_2				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-379. BUCK2_DTEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	force_pfm_2	R/W	0b	Forces buck to PFM when buck_mode is enabled for auto mode (not buck testmode)
6	swc_buck_hiz_2	R/W	0b	Sets switches to HIZ.
5	swc_buck_hs_2	R/W	0b	(1=hs on & ls off, 0=ls on & hs off) --hs needs also gate voltage force and swc_buck_hiz must be 0.
4:0	buck_dtab0_sel_2	R/W	0b	Selection for buck digital test bus0.

ADVANCE INFORMATION

5.7.1.341 BUCK2_DTEST_REG_1 Register (Offset = 0x1B2) [reset = 0x0]

BUCK2_DTEST_REG_1 is shown in Figure 5-408 and described in Table 5-380.

Return to the Summary Table.

Figure 5-408. BUCK2_DTEST_REG_1 Register

7	6	5	4	3	2	1	0
test_pulse_generator_2	test_sample_izero_2	test_iave_pd_2	buck_dtab1_sel_2				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-380. BUCK2_DTEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_pulse_generator_2	R/W	0b	Sets HS and LS pulse generators to oscillator mode. Pulse generator length can be controlled with test_integrator_word. When test_pulse_gen_fixed is set, this defines which of the HS or LS pulse generator has fixed length
6	test_sample_izero_2	R/W	0b	izero comparator latches sw pin voltage at negedge of this signal
5	test_iave_pd_2	R/W	0b	Enables pull down for the i_ave signals (loop_comp input pair 2)
4:0	buck_dtab1_sel_2	R/W	0b	Selection for buck digital test bus1.

ADVANCE INFORMATION

5.7.1.342 BUCK2_DTEST_REG_2 Register (Offset = 0x1B3) [reset = 0x0]

BUCK2_DTEST_REG_2 is shown in Figure 5-409 and described in Table 5-381.

Return to the Summary Table.

Figure 5-409. BUCK2_DTEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED		test_bypass_ramp_bias_res_2	test_buck_weak_driver_2	dis_vref_filter_2	dis_loop_comp_hyst_2	test_blank_2	test_single_shot_2
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-381. BUCK2_DTEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_bypass_ramp_bias_res_2	R/W	0b	When high, emulated ramp DC bias resistor is bypassed
4	test_buck_weak_driver_2	R/W	0b	0 - weak driver hiz 1 - weak driver high
3	dis_vref_filter_2	R/W	0b	This register has two functions in testmode: 1. Bypass vref filter 2. Bypass load monitor filter
2	dis_loop_comp_hyst_2	R/W	0b	Disables loop comparator negative hysteresis
1	test_blank_2	R/W	0b	Sets all single shots to oscillator mode with blank feedback
0	test_single_shot_2	R/W	0b	Sets all single shots to oscillator mode.

ADVANCE INFORMATION

5.7.1.343 BUCK2_DTEST_REG_3 Register (Offset = 0x1B4) [reset = 0x0]

BUCK2_DTEST_REG_3 is shown in Figure 5-410 and described in Table 5-382.

Return to the Summary Table.

Figure 5-410. BUCK2_DTEST_REG_3 Register

7	6	5	4	3	2	1	0
test_integrator_word_2							
R/W-0b							

Table 5-382. BUCK2_DTEST_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	test_integrator_word_2	R/W	0b	These bits controls in testmode: 1. Integrator digital word 2. pulse generator delay selection 3. sel_load_ref[4:0] (Load monitor reference level)

5.7.1.344 BUCK2_DTEST_REG_4 Register (Offset = 0x1B5) [reset = 0x0]

BUCK2_DTEST_REG_4 is shown in Figure 5-411 and described in Table 5-383.

Return to the Summary Table.

Figure 5-411. BUCK2_DTEST_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED			test_bypass_sw_latches_2	test_pulse_gen_fixed_2	test_dis_autozero_2	test_carousel_ctrl_2	
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-383. BUCK2_DTEST_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	test_bypass_sw_latches_2	R/W	0b	When enabled buck_hiz and buck_hs can be controlled by test_buck_hiz and test_buck_hs bits
3	test_pulse_gen_fixed_2	R/W	0b	When test_pulse_gen_fixed is set, test_pulse_generator defines which one of LS or HS pulse generator is set to fixed value: 0:Pulse generator LS length is fixed and HS is controlled with test_integrator_word 1:Pulse generator HS length is fixed and LS is controlled with test_integrator_word
2	test_dis_autozero_2	R/W	0b	Disables isense and ibal autozero
1:0	test_carousel_ctrl_2	R/W	0b	Test control for isense LS and HS comparators 0:Carousel normal operation 1:sel_comp = 0 2:sel_comp = 1 3:sel_comp = 2

ADVANCE INFORMATION

5.7.1.345 BUCK3_ATEST_REG_0 Register (Offset = 0x1B7) [reset = 0x0]

BUCK3_ATEST_REG_0 is shown in Figure 5-412 and described in Table 5-384.

Return to the Summary Table.

Figure 5-412. BUCK3_ATEST_REG_0 Register

7	6	5	4	3	2	1	0
test_ramp_emu_3	test_ramp_artif_pd_3	test_ramp_artif_3	test_integ_dac_short_output_3	buck_atab_sel_3			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-384. BUCK3_ATEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_ramp_emu_3	R/W	0b	activates ramp_emu oscillator test mode
6	test_ramp_artif_pd_3	R/W	0b	pull down artif ramp outputs
5	test_ramp_artif_3	R/W	0b	activates ramp_artif oscillator test mode
4	test_integ_dac_short_output_3	R/W	0b	short integrator dac outputs
3:0	buck_atab_sel_3	R/W	0b	connects internal nets to atab.

ADVANCE INFORMATION

5.7.1.346 BUCK3_ATEST_REG_1 Register (Offset = 0x1B8) [reset = 0x0]

BUCK3_ATEST_REG_1 is shown in Figure 5-413 and described in Table 5-385.

Return to the Summary Table.

Figure 5-413. BUCK3_ATEST_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED		test_sw_short_detector_3	test_ovst_3		test_hs_gate_3	test_iave_3	test_ramp_emu_pd_3
R/W-0b		R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 5-385. BUCK3_ATEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_sw_short_detector_3	R/W	0b	Muxes short detector latches set signals instead of latches outputs.
4:3	test_ovst_3	R/W	0b	Not used
2	test_hs_gate_3	R/W	0b	connect hs gate to atab_hv test bus
1	test_iave_3	R/W	0b	bypass for average current level shifting function
0	test_ramp_emu_pd_3	R/W	0b	shorts ramp generating capacitors to ground, output is still ac coupled

ADVANCE INFORMATION

5.7.1.347 BUCK3_ATEST_REG_2 Register (Offset = 0x1B9) [reset = 0x0]

BUCK3_ATEST_REG_2 is shown in Figure 5-414 and described in Table 5-386.

Return to the Summary Table.

Figure 5-414. BUCK3_ATEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED					test_spare_3		
R/W-0b					R/W-0b		

Table 5-386. BUCK3_ATEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	test_spare_3	R/W	0b	

5.7.1.348 BUCK3_DTEST_REG_0 Register (Offset = 0x1BA) [reset = 0x0]

BUCK3_DTEST_REG_0 is shown in Figure 5-415 and described in Table 5-387.

Return to the Summary Table.

Figure 5-415. BUCK3_DTEST_REG_0 Register

7	6	5	4	3	2	1	0
force_pfm_3	swc_buck_hiz_3	swc_buck_hs_3	buck_dtab0_sel_3				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-387. BUCK3_DTEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	force_pfm_3	R/W	0b	Forces buck to PFM when buck_mode is enabled for auto mode (not buck testmode)
6	swc_buck_hiz_3	R/W	0b	Sets switches to HIZ.
5	swc_buck_hs_3	R/W	0b	(1=hs on & ls off, 0=ls on & hs off) --hs needs also gate voltage force and swc_buck_hiz must be 0.
4:0	buck_dtab0_sel_3	R/W	0b	Selection for buck digital test bus0.

ADVANCE INFORMATION

5.7.1.349 BUCK3_DTEST_REG_1 Register (Offset = 0x1BB) [reset = 0x0]

BUCK3_DTEST_REG_1 is shown in Figure 5-416 and described in Table 5-388.

Return to the Summary Table.

Figure 5-416. BUCK3_DTEST_REG_1 Register

7	6	5	4	3	2	1	0
test_pulse_generator_3	test_sample_izero_3	test_iave_pd_3	buck_dtab1_sel_3				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-388. BUCK3_DTEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_pulse_generator_3	R/W	0b	Sets HS and LS pulse generators to oscillator mode. Pulse generator length can be controlled with test_integrator_word. When test_pulse_gen_fixed is set, this defines which of the HS or LS pulse generator has fixed length
6	test_sample_izero_3	R/W	0b	izero comparator latches sw pin voltage at negedge of this signal
5	test_iave_pd_3	R/W	0b	Enables pull down for the i_ave signals (loop_comp input pair 2)
4:0	buck_dtab1_sel_3	R/W	0b	Selection for buck digital test bus1.

5.7.1.350 BUCK3_DTEST_REG_2 Register (Offset = 0x1BC) [reset = 0x0]

BUCK3_DTEST_REG_2 is shown in Figure 5-417 and described in Table 5-389.

Return to the Summary Table.

Figure 5-417. BUCK3_DTEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED		test_bypass_ramp_bias_res_3	test_buck_weak_driver_3	dis_vref_filter_3	dis_loop_comp_hyst_3	test_blank_3	test_single_shot_3
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-389. BUCK3_DTEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_bypass_ramp_bias_res_3	R/W	0b	When high, emulated ramp DC bias resistor is bypassed
4	test_buck_weak_driver_3	R/W	0b	0 - weak driver hiz 1 - weak driver high
3	dis_vref_filter_3	R/W	0b	This register has two functions in testmode: 1. Bypass vref filter 2. Bypass load monitor filter
2	dis_loop_comp_hyst_3	R/W	0b	Disables loop comparator negative hysteresis
1	test_blank_3	R/W	0b	Sets all single shots to oscillator mode with blank feedback
0	test_single_shot_3	R/W	0b	Sets all single shots to oscillator mode.

ADVANCE INFORMATION

5.7.1.351 BUCK3_DTEST_REG_3 Register (Offset = 0x1BD) [reset = 0x0]

BUCK3_DTEST_REG_3 is shown in Figure 5-418 and described in Table 5-390.

Return to the Summary Table.

Figure 5-418. BUCK3_DTEST_REG_3 Register

7	6	5	4	3	2	1	0
test_integrator_word_3							
R/W-0b							

Table 5-390. BUCK3_DTEST_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	test_integrator_word_3	R/W	0b	These bits controls in testmode: 1. Integrator digital word 2. pulse generator delay selection 3. sel_load_ref[4:0] (Load monitor reference level)

5.7.1.352 BUCK3_DTEST_REG_4 Register (Offset = 0x1BE) [reset = 0x0]

BUCK3_DTEST_REG_4 is shown in Figure 5-419 and described in Table 5-391.

Return to the Summary Table.

Figure 5-419. BUCK3_DTEST_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED			test_bypass_sw_latches_3	test_pulse_gen_fixed_3	test_dis_autozero_3	test_carousel_ctrl_3	
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-391. BUCK3_DTEST_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	test_bypass_sw_latches_3	R/W	0b	When enabled buck_hiz and buck_hs can be controlled by test_buck_hiz and test_buck_hs bits
3	test_pulse_gen_fixed_3	R/W	0b	When test_pulse_gen_fixed is set, test_pulse_generator defines which one of LS or HS pulse generator is set to fixed value: 0:Pulse generator LS length is fixed and HS is controlled with test_integrator_word 1:Pulse generator HS length is fixed and LS is controlled with test_integrator_word
2	test_dis_autozero_3	R/W	0b	Disables isense and ibal autozero
1:0	test_carousel_ctrl_3	R/W	0b	Test control for isense LS and HS comparators 0:Carousel normal operation 1:sel_comp = 0 2:sel_comp = 1 3:sel_comp = 2

ADVANCE INFORMATION

5.7.1.353 BUCK4_ATEST_REG_0 Register (Offset = 0x1C0) [reset = 0x0]

BUCK4_ATEST_REG_0 is shown in Figure 5-420 and described in Table 5-392.

Return to the Summary Table.

Figure 5-420. BUCK4_ATEST_REG_0 Register

7	6	5	4	3	2	1	0
test_ramp_emu_4	test_ramp_artif_pd_4	test_ramp_artif_4	test_integ_dac_short_output_4	buck_atab_sel_4			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-392. BUCK4_ATEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_ramp_emu_4	R/W	0b	activates ramp_emu oscillator test mode
6	test_ramp_artif_pd_4	R/W	0b	pull down artif ramp outputs
5	test_ramp_artif_4	R/W	0b	activates ramp_artif oscillator test mode
4	test_integ_dac_short_output_4	R/W	0b	short integrator dac outputs
3:0	buck_atab_sel_4	R/W	0b	connects internal nets to atab.

ADVANCE INFORMATION

5.7.1.354 BUCK4_ATEST_REG_1 Register (Offset = 0x1C1) [reset = 0x0]

BUCK4_ATEST_REG_1 is shown in Figure 5-421 and described in Table 5-393.

Return to the Summary Table.

Figure 5-421. BUCK4_ATEST_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED		test_sw_short_detector_4	test_ovst_4		test_hs_gate_4	test_iave_4	test_ramp_emu_pd_4
R/W-0b		R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 5-393. BUCK4_ATEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_sw_short_detector_4	R/W	0b	Muxes short detector latches set signals instead of latches outputs.
4:3	test_ovst_4	R/W	0b	Not used
2	test_hs_gate_4	R/W	0b	connect hs gate to atab_hv test bus
1	test_iave_4	R/W	0b	bypass for average current level shifting function
0	test_ramp_emu_pd_4	R/W	0b	shorts ramp generating capacitors to ground, output is still ac coupled

ADVANCE INFORMATION

5.7.1.355 BUCK4_ATEST_REG_2 Register (Offset = 0x1C2) [reset = 0x0]

BUCK4_ATEST_REG_2 is shown in Figure 5-422 and described in Table 5-394.

Return to the Summary Table.

Figure 5-422. BUCK4_ATEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED					test_spare_4		
R/W-0b					R/W-0b		

Table 5-394. BUCK4_ATEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	test_spare_4	R/W	0b	

5.7.1.356 BUCK4_DTEST_REG_0 Register (Offset = 0x1C3) [reset = 0x0]

BUCK4_DTEST_REG_0 is shown in Figure 5-423 and described in Table 5-395.

Return to the Summary Table.

Figure 5-423. BUCK4_DTEST_REG_0 Register

7	6	5	4	3	2	1	0
force_pfm_4	swc_buck_hiz_4	swc_buck_hs_4	buck_dtab0_sel_4				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-395. BUCK4_DTEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	force_pfm_4	R/W	0b	Forces buck to PFM when buck_mode is enabled for auto mode (not buck testmode)
6	swc_buck_hiz_4	R/W	0b	Sets switches to HIZ.
5	swc_buck_hs_4	R/W	0b	(1=hs on & ls off, 0=ls on & hs off) --hs needs also gate voltage force and swc_buck_hiz must be 0.
4:0	buck_dtab0_sel_4	R/W	0b	Selection for buck digital test bus0.

ADVANCE INFORMATION

5.7.1.357 BUCK4_DTEST_REG_1 Register (Offset = 0x1C4) [reset = 0x0]

BUCK4_DTEST_REG_1 is shown in Figure 5-424 and described in Table 5-396.

Return to the Summary Table.

Figure 5-424. BUCK4_DTEST_REG_1 Register

7	6	5	4	3	2	1	0
test_pulse_generator_4	test_sample_izero_4	test_iave_pd_4	buck_dtab1_sel_4				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-396. BUCK4_DTEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_pulse_generator_4	R/W	0b	Sets HS and LS pulse generators to oscillator mode. Pulse generator length can be controlled with test_integrator_word. When test_pulse_gen_fixed is set, this defines which of the HS or LS pulse generator has fixed length
6	test_sample_izero_4	R/W	0b	izero comparator latches sw pin voltage at negedge of this signal
5	test_iave_pd_4	R/W	0b	Enables pull down for the i_ave signals (loop_comp input pair 2)
4:0	buck_dtab1_sel_4	R/W	0b	Selection for buck digital test bus1.

5.7.1.358 BUCK4_DTEST_REG_2 Register (Offset = 0x1C5) [reset = 0x0]

BUCK4_DTEST_REG_2 is shown in Figure 5-425 and described in Table 5-397.

Return to the Summary Table.

Figure 5-425. BUCK4_DTEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED		test_bypass_ramp_bias_res_4	test_buck_weak_driver_4	dis_vref_filter_4	dis_loop_comp_hyst_4	test_blank_4	test_single_shot_4
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-397. BUCK4_DTEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_bypass_ramp_bias_res_4	R/W	0b	When high, emulated ramp DC bias resistor is bypassed
4	test_buck_weak_driver_4	R/W	0b	0 - weak driver hiz 1 - weak driver high
3	dis_vref_filter_4	R/W	0b	This register has two functions in testmode: 1. Bypass vref filter 2. Bypass load monitor filter
2	dis_loop_comp_hyst_4	R/W	0b	Disables loop comparator negative hysteresis
1	test_blank_4	R/W	0b	Sets all single shots to oscillator mode with blank feedback
0	test_single_shot_4	R/W	0b	Sets all single shots to oscillator mode.

ADVANCE INFORMATION

5.7.1.359 BUCK4_DTEST_REG_3 Register (Offset = 0x1C6) [reset = 0x0]

BUCK4_DTEST_REG_3 is shown in Figure 5-426 and described in Table 5-398.

Return to the Summary Table.

Figure 5-426. BUCK4_DTEST_REG_3 Register

7	6	5	4	3	2	1	0
test_integrator_word_4							
R/W-0b							

Table 5-398. BUCK4_DTEST_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	test_integrator_word_4	R/W	0b	These bits controls in testmode: 1. Integrator digital word 2. pulse generator delay selection 3. sel_load_ref[4:0] (Load monitor reference level)

ADVANCE INFORMATION

5.7.1.360 BUCK4_DTEST_REG_4 Register (Offset = 0x1C7) [reset = 0x0]

BUCK4_DTEST_REG_4 is shown in Figure 5-427 and described in Table 5-399.

Return to the Summary Table.

Figure 5-427. BUCK4_DTEST_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED			test_bypass_sw_latches_4	test_pulse_gen_fixed_4	test_dis_autozero_4	test_carousel_ctrl_4	
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-399. BUCK4_DTEST_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	test_bypass_sw_latches_4	R/W	0b	When enabled buck_hiz and buck_hs can be controlled by test_buck_hiz and test_buck_hs bits
3	test_pulse_gen_fixed_4	R/W	0b	When test_pulse_gen_fixed is set, test_pulse_generator defines which one of LS or HS pulse generator is set to fixed value: 0:Pulse generator LS length is fixed and HS is controlled with test_integrator_word 1:Pulse generator HS length is fixed and LS is controlled with test_integrator_word
2	test_dis_autozero_4	R/W	0b	Disables isense and ibal autozero
1:0	test_carousel_ctrl_4	R/W	0b	Test control for isense LS and HS comparators 0:Carousel normal operation 1:sel_comp = 0 2:sel_comp = 1 3:sel_comp = 2

ADVANCE INFORMATION

5.7.1.361 BUCK5_ATEST_REG_0 Register (Offset = 0x1C9) [reset = 0x0]

BUCK5_ATEST_REG_0 is shown in Figure 5-428 and described in Table 5-400.

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Figure 5-428. BUCK5_ATEST_REG_0 Register

7	6	5	4	3	2	1	0
test_ramp_emu_5	test_ramp_artif_pd_5	test_ramp_artif_5	test_integ_dac_short_output_5	buck_atab_sel_5			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b			

Table 5-400. BUCK5_ATEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_ramp_emu_5	R/W	0b	activates ramp_emu oscillator test mode
6	test_ramp_artif_pd_5	R/W	0b	pull down artif ramp outputs
5	test_ramp_artif_5	R/W	0b	activates ramp_artif oscillator test mode
4	test_integ_dac_short_output_5	R/W	0b	short integrator dac outputs
3:0	buck_atab_sel_5	R/W	0b	connects internal nets to atab.

ADVANCE INFORMATION

5.7.1.362 BUCK5_ATEST_REG_1 Register (Offset = 0x1CA) [reset = 0x0]

BUCK5_ATEST_REG_1 is shown in Figure 5-429 and described in Table 5-401.

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Figure 5-429. BUCK5_ATEST_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED		test_sw_short_detector_5	test_ovst_5		test_hs_gate_5	test_iave_5	test_ramp_emu_pd_5
R/W-0b		R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 5-401. BUCK5_ATEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_sw_short_detector_5	R/W	0b	Muxes short detector latches set signals instead of latches outputs.
4:3	test_ovst_5	R/W	0b	Not used
2	test_hs_gate_5	R/W	0b	connect hs gate to atab_hv test bus
1	test_iave_5	R/W	0b	bypass for average current level shifting function
0	test_ramp_emu_pd_5	R/W	0b	shorts ramp generating capacitors to ground, output is still ac coupled

ADVANCE INFORMATION

5.7.1.363 BUCK5_ATEST_REG_2 Register (Offset = 0x1CB) [reset = 0x0]

BUCK5_ATEST_REG_2 is shown in Figure 5-430 and described in Table 5-402.

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Figure 5-430. BUCK5_ATEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED					test_spare_5		
R/W-0b					R/W-0b		

Table 5-402. BUCK5_ATEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	test_spare_5	R/W	0b	

5.7.1.364 BUCK5_DTEST_REG_0 Register (Offset = 0x1CC) [reset = 0x0]

BUCK5_DTEST_REG_0 is shown in Figure 5-431 and described in Table 5-403.

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Figure 5-431. BUCK5_DTEST_REG_0 Register

7	6	5	4	3	2	1	0
force_pfm_5	swc_buck_hiz_5	swc_buck_hs_5	buck_dtab0_sel_5				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-403. BUCK5_DTEST_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	force_pfm_5	R/W	0b	Forces buck to PFM when buck_mode is enabled for auto mode (not buck testmode)
6	swc_buck_hiz_5	R/W	0b	Sets switches to HIZ.
5	swc_buck_hs_5	R/W	0b	(1=hs on & ls off, 0=ls on & hs off) --hs needs also gate voltage force and swc_buck_hiz must be 0.
4:0	buck_dtab0_sel_5	R/W	0b	Selection for buck digital test bus0.

ADVANCE INFORMATION

5.7.1.365 BUCK5_DTEST_REG_1 Register (Offset = 0x1CD) [reset = 0x0]

BUCK5_DTEST_REG_1 is shown in Figure 5-432 and described in Table 5-404.

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Figure 5-432. BUCK5_DTEST_REG_1 Register

7	6	5	4	3	2	1	0
test_pulse_generator_5	test_sample_izero_5	test_iave_pd_5	buck_dtab1_sel_5				
R/W-0b	R/W-0b	R/W-0b	R/W-0b				

Table 5-404. BUCK5_DTEST_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	test_pulse_generator_5	R/W	0b	Sets HS and LS pulse generators to oscillator mode. Pulse generator length can be controlled with test_integrator_word. When test_pulse_gen_fixed is set, this defines which of the HS or LS pulse generator has fixed length
6	test_sample_izero_5	R/W	0b	izero comparator latches sw pin voltage at negedge of this signal
5	test_iave_pd_5	R/W	0b	Enables pull down for the i_ave signals (loop_comp input pair 2)
4:0	buck_dtab1_sel_5	R/W	0b	Selection for buck digital test bus1.

5.7.1.366 BUCK5_DTEST_REG_2 Register (Offset = 0x1CE) [reset = 0x0]

BUCK5_DTEST_REG_2 is shown in Figure 5-433 and described in Table 5-405.

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Figure 5-433. BUCK5_DTEST_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED		test_bypass_ramp_bias_res_5	test_buck_weak_driver_5	dis_vref_filter_5	dis_loop_comp_hyst_5	test_blank_5	test_single_shot_5
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-405. BUCK5_DTEST_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	test_bypass_ramp_bias_res_5	R/W	0b	When high, emulated ramp DC bias resistor is bypassed
4	test_buck_weak_driver_5	R/W	0b	0 - weak driver hiz 1 - weak driver high
3	dis_vref_filter_5	R/W	0b	This register has two functions in testmode: 1. Bypass vref filter 2. Bypass load monitor filter
2	dis_loop_comp_hyst_5	R/W	0b	Disables loop comparator negative hysteresis
1	test_blank_5	R/W	0b	Sets all single shots to oscillator mode with blank feedback
0	test_single_shot_5	R/W	0b	Sets all single shots to oscillator mode.

ADVANCE INFORMATION

5.7.1.367 BUCK5_DTEST_REG_3 Register (Offset = 0x1CF) [reset = 0x0]

BUCK5_DTEST_REG_3 is shown in Figure 5-434 and described in Table 5-406.

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Figure 5-434. BUCK5_DTEST_REG_3 Register

7	6	5	4	3	2	1	0
test_integrator_word_5							
R/W-0b							

Table 5-406. BUCK5_DTEST_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	test_integrator_word_5	R/W	0b	These bits controls in testmode: 1. Integrator digital word 2. pulse generator delay selection 3. sel_load_ref[4:0] (Load monitor reference level)

5.7.1.368 BUCK5_DTEST_REG_4 Register (Offset = 0x1D0) [reset = 0x0]

BUCK5_DTEST_REG_4 is shown in Figure 5-435 and described in Table 5-407.

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Figure 5-435. BUCK5_DTEST_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED			test_bypass_sw_latches_5	test_pulse_gen_fixed_5	test_dis_autozero_5	test_carousel_ctrl_5	
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	

Table 5-407. BUCK5_DTEST_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	test_bypass_sw_latches_5	R/W	0b	When enabled buck_hiz and buck_hs can be controlled by test_buck_hiz and test_buck_hs bits
3	test_pulse_gen_fixed_5	R/W	0b	When test_pulse_gen_fixed is set, test_pulse_generator defines which one of LS or HS pulse generator is set to fixed value: 0:Pulse generator LS length is fixed and HS is controlled with test_integrator_word 1:Pulse generator HS length is fixed and LS is controlled with test_integrator_word
2	test_dis_autozero_5	R/W	0b	Disables isense and ibal autozero
1:0	test_carousel_ctrl_5	R/W	0b	Test control for isense LS and HS comparators 0:Carousel normal operation 1:sel_comp = 0 2:sel_comp = 1 3:sel_comp = 2

ADVANCE INFORMATION

5.7.1.369 BUCK1_STATE Register (Offset = 0x1D2) [reset = 0x0]

BUCK1_STATE is shown in Figure 5-436 and described in Table 5-408.

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Figure 5-436. BUCK1_STATE Register

7	6	5	4	3	2	1	0
RESERVED				buck_state_1			
R-0b				R-0b			

Table 5-408. BUCK1_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	buck_state_1	R	0b	0000 - DISABLED 0001 - BIAS_DELAY 0011 - CHECK_VOUT 0010 - PWM_1PH 0110 - PWM_2PH 0111 - PWM_3PH 0101 - PWM_4PH 0100 - PFM_MODE 1100 - SOFT_SHUT_DOWN 1101 - SLAVE_STAND_BY 1111 - SLAVE_SLEEPING 1110 - SLAVE_PWM 1010 - SLAVE_SHEDING 1000 - TEST_MODE

5.7.1.370 BUCK2_STATE Register (Offset = 0x1D3) [reset = 0x0]

BUCK2_STATE is shown in Figure 5-437 and described in Table 5-409.

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Figure 5-437. BUCK2_STATE Register

7	6	5	4	3	2	1	0
RESERVED				buck_state_2			
R-0b				R-0b			

Table 5-409. BUCK2_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	buck_state_2	R	0b	0000 - DISABLED 0001 - BIAS_DELAY 0011 - CHECK_VOUT 0010 - PWM_1PH 0110 - PWM_2PH 0111 - PWM_3PH 0101 - PWM_4PH 0100 - PFM_MODE 1100 - SOFT_SHUT_DOWN 1101 - SLAVE_STAND_BY 1111 - SLAVE_SLEEPING 1110 - SLAVE_PWM 1010 - SLAVE_SHEDING 1000 - TEST_MODE

ADVANCE INFORMATION

5.7.1.371 BUCK3_STATE Register (Offset = 0x1D4) [reset = 0x0]

BUCK3_STATE is shown in Figure 5-438 and described in Table 5-410.

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Figure 5-438. BUCK3_STATE Register

7	6	5	4	3	2	1	0
RESERVED				buck_state_3			
R-0b				R-0b			

Table 5-410. BUCK3_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	buck_state_3	R	0b	0000 - DISABLED 0001 - BIAS_DELAY 0011 - CHECK_VOUT 0010 - PWM_1PH 0110 - PWM_2PH 0111 - PWM_3PH 0101 - PWM_4PH 0100 - PFM_MODE 1100 - SOFT_SHUT_DOWN 1101 - SLAVE_STAND_BY 1111 - SLAVE_SLEEPING 1110 - SLAVE_PWM 1010 - SLAVE_SHEDING 1000 - TEST_MODE

5.7.1.372 BUCK4_STATE Register (Offset = 0x1D5) [reset = 0x0]

BUCK4_STATE is shown in Figure 5-439 and described in Table 5-411.

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Figure 5-439. BUCK4_STATE Register

7	6	5	4	3	2	1	0
RESERVED				buck_state_4			
R-0b				R-0b			

Table 5-411. BUCK4_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	buck_state_4	R	0b	0000 - DISABLED 0001 - BIAS_DELAY 0011 - CHECK_VOUT 0010 - PWM_1PH 0110 - PWM_2PH 0111 - PWM_3PH 0101 - PWM_4PH 0100 - PFM_MODE 1100 - SOFT_SHUT_DOWN 1101 - SLAVE_STAND_BY 1111 - SLAVE_SLEEPING 1110 - SLAVE_PWM 1010 - SLAVE_SHEDING 1000 - TEST_MODE

5.7.1.373 BUCK5_STATE Register (Offset = 0x1D6) [reset = 0x0]

BUCK5_STATE is shown in Figure 5-440 and described in Table 5-412.

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Figure 5-440. BUCK5_STATE Register

7	6	5	4	3	2	1	0
RESERVED				buck_state_5			
R-0b				R-0b			

Table 5-412. BUCK5_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	
3:0	buck_state_5	R	0b	0000 - DISABLED 0001 - BIAS_DELAY 0011 - CHECK_VOUT 0010 - PWM_1PH 0110 - PWM_2PH 0111 - PWM_3PH 0101 - PWM_4PH 0100 - PFM_MODE 1100 - SOFT_SHUT_DOWN 1101 - SLAVE_STAND_BY 1111 - SLAVE_SLEEPING 1110 - SLAVE_PWM 1010 - SLAVE_SHEDING 1000 - TEST_MODE

5.7.1.374 BUCK1_INTEGRATOR Register (Offset = 0x1D7) [reset = 0x0]

BUCK1_INTEGRATOR is shown in Figure 5-441 and described in Table 5-413.

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Figure 5-441. BUCK1_INTEGRATOR Register

7	6	5	4	3	2	1	0
buck_integrator_word_1							
R-0b							

Table 5-413. BUCK1_INTEGRATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	buck_integrator_word_1	R	0b	

ADVANCE INFORMATION

5.7.1.375 BUCK2_INTEGRATOR Register (Offset = 0x1D8) [reset = 0x0]

BUCK2_INTEGRATOR is shown in Figure 5-442 and described in Table 5-414.

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Figure 5-442. BUCK2_INTEGRATOR Register

7	6	5	4	3	2	1	0
buck_integrator_word_2							
R-0b							

Table 5-414. BUCK2_INTEGRATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	buck_integrator_word_2	R	0b	

5.7.1.376 BUCK3_INTEGRATOR Register (Offset = 0x1D9) [reset = 0x0]

BUCK3_INTEGRATOR is shown in Figure 5-443 and described in Table 5-415.

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Figure 5-443. BUCK3_INTEGRATOR Register

7	6	5	4	3	2	1	0
buck_integrator_word_3							
R-0b							

Table 5-415. BUCK3_INTEGRATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	buck_integrator_word_3	R	0b	

5.7.1.377 BUCK4_INTEGRATOR Register (Offset = 0x1DA) [reset = 0x0]

BUCK4_INTEGRATOR is shown in Figure 5-444 and described in Table 5-416.

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Figure 5-444. BUCK4_INTEGRATOR Register

7	6	5	4	3	2	1	0
buck_integrator_word_4							
R-0b							

Table 5-416. BUCK4_INTEGRATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	buck_integrator_word_4	R	0b	

5.7.1.378 BUCK5_INTEGRATOR Register (Offset = 0x1DB) [reset = 0x0]

BUCK5_INTEGRATOR is shown in Figure 5-445 and described in Table 5-417.

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Figure 5-445. BUCK5_INTEGRATOR Register

7	6	5	4	3	2	1	0
buck_integrator_word_5							
R-0b							

Table 5-417. BUCK5_INTEGRATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	buck_integrator_word_5	R	0b	

ADVANCE INFORMATION

5.7.1.379 BUCK_STATUS Register (Offset = 0x1DC) [reset = 0x0]

BUCK_STATUS is shown in Figure 5-446 and described in Table 5-418.

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Figure 5-446. BUCK_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			buck5_active	buck4_active	buck3_active	buck2_active	buck1_active
R-0b			R-0b	R-0b	R-0b	R-0b	R-0b

Table 5-418. BUCK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0b	
4	buck5_active	R	0b	Buck is enabled OR buck FSM is active (state != DISABLED)
3	buck4_active	R	0b	Buck is enabled OR buck FSM is active (state != DISABLED)
2	buck3_active	R	0b	Buck is enabled OR buck FSM is active (state != DISABLED)
1	buck2_active	R	0b	Buck is enabled OR buck FSM is active (state != DISABLED)
0	buck1_active	R	0b	Buck is enabled OR buck FSM is active (state != DISABLED)

5.7.1.380 EEPROM_CONTROL_1 Register (Offset = 0x1E0) [reset = 0x0]

EEPROM_CONTROL_1 is shown in Figure 5-447 and described in Table 5-419.

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The TM_EE_CFG_* bits provide configuration information that will effect TM_EE_CMD_* operation.

Figure 5-447. EEPROM_CONTROL_1 Register

7	6	5	4	3	2	1	0
RESERVED			TM_EE_CFG_SHADOW_WRITE_DIS	TM_EE_CFG_MARGIN_READ	TM_EE_CFG_CKB_PROG	TM_EE_CFG_BULK_ERASE	TM_EE_CFG_BULK_PROG
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-419. EEPROM_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4	TM_EE_CFG_SHADOW_WRITE_DIS	R/W	0b	For a EE_CMD_READ will drive Eeprom testmode signals for a Margin Read.
3	TM_EE_CFG_MARGIN_READ	R/W	0b	For a EE_CMD_READ will drive Eeprom testmode signals for a Margin Read.
2	TM_EE_CFG_CKB_PROG	R/W	0b	For a EE_CMD_PROG will program even Eeprom to TM_EE_WRITE_DATA<3-0> and odd Eeprom to ~TM_EE_WRITE_DATA<3-0>.
1	TM_EE_CFG_BULK_ERASE	R/W	0b	For a EE_CMD_ERASE will erase entire Eeprom in a single erase cycle.
0	TM_EE_CFG_BULK_PROG	R/W	0b	For a EE_CMD_PROG will program the entire Eeprom (Value = TM_EE_WRITE_DATA<3-0>) in a single program cycle.

ADVANCE INFORMATION

5.7.1.381 EEPROM_CONTROL_2 Register (Offset = 0x1E1) [reset = 0x0]

EEPROM_CONTROL_2 is shown in Figure 5-448 and described in Table 5-420.

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Any disabled banks will be skipped during automated command load and program operations
Note this bit has no value for a single bank and the corresponding bit can be safely tied low.

Figure 5-448. EEPROM_CONTROL_2 Register

7	6	5	4	3	2	1	0
RESERVED		TM_EE_CFG_SINGLE	RESERVED	TM_EE_CFG_BANK_DIS			
R/W-0b		R/W-0b	R/W-0b	R/W-0b			

Table 5-420. EEPROM_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	TM_EE_CFG_SINGLE	R/W	0b	Configure Eeprom program/read commands to operate on a single address specified by TM_EE_ADDR
4	RESERVED	R/W	0b	
3:0	TM_EE_CFG_BANK_DIS	R/W	0b	One-hot disable for the 5 Eeprom banks in the Leo project.

ADVANCE INFORMATION

5.7.1.382 EEPROM_CONTROL_3 Register (Offset = 0x1E2) [reset = 0x0]

EEPROM_CONTROL_3 is shown in Figure 5-449 and described in Table 5-421.

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Figure 5-449. EEPROM_CONTROL_3 Register

7	6	5	4	3	2	1	0
RESERVED		TM_EE_ADDR					
R/W-0b		R/W-0b					

Table 5-421. EEPROM_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	TM_EE_ADDR	R/W	0b	EEPROM address for prog and read

5.7.1.383 EEPROM_CONTROL_8 Register (Offset = 0x1E7) [reset = 0x0]

EEPROM_CONTROL_8 is shown in Figure 5-450 and described in Table 5-422.

Return to the Summary Table.

EEPROM data for prog and read

Figure 5-450. EEPROM_CONTROL_8 Register

7	6	5	4	3	2	1	0
TM_EE_WRITE_DATA3							
R/W-0b							

Table 5-422. EEPROM_CONTROL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_WRITE_DATA3	R/W	0b	Data byte 3 used by bulk/checkboard programming

ADVANCE INFORMATION

5.7.1.384 EEPROM_CONTROL_9 Register (Offset = 0x1E8) [reset = 0x0]

EEPROM_CONTROL_9 is shown in Figure 5-451 and described in Table 5-423.

Return to the Summary Table.

EEPROM data for prog and read

Figure 5-451. EEPROM_CONTROL_9 Register

7	6	5	4	3	2	1	0
TM_EE_WRITE_DATA2							
R/W-0b							

Table 5-423. EEPROM_CONTROL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_WRITE_DATA2	R/W	0b	Data byte 2 used by bulk/checkboard programming

ADVANCE INFORMATION

5.7.1.385 EEPROM_CONTROL_10 Register (Offset = 0x1E9) [reset = 0x0]

EEPROM_CONTROL_10 is shown in Figure 5-452 and described in Table 5-424.

Return to the Summary Table.

EEPROM data for prog and read

Figure 5-452. EEPROM_CONTROL_10 Register

7	6	5	4	3	2	1	0
TM_EE_WRITE_DATA1							
R/W-0b							

Table 5-424. EEPROM_CONTROL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_WRITE_DATA1	R/W	0b	Data byte 1 used by bulk/checkboard programming

5.7.1.386 EEPROM_CONTROL_11 Register (Offset = 0x1EA) [reset = 0x0]

EEPROM_CONTROL_11 is shown in Figure 5-453 and described in Table 5-425.

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EEPROM data for prog and read

Figure 5-453. EEPROM_CONTROL_11 Register

7	6	5	4	3	2	1	0
TM_EE_WRITE_DATA0							
R/W-0b							

Table 5-425. EEPROM_CONTROL_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_WRITE_DATA0	R/W	0b	Data byte 0 used by bulk/checkboard programming

ADVANCE INFORMATION

5.7.1.387 EEPROM_CONTROL_12 Register (Offset = 0x1EB) [reset = 0x0]

EEPROM_CONTROL_12 is shown in Figure 5-454 and described in Table 5-426.

Return to the Summary Table.

Figure 5-454. EEPROM_CONTROL_12 Register

7	6	5	4	3	2	1	0
TM_EE_READ_DATA3							
R-0b							

Table 5-426. EEPROM_CONTROL_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_READ_DATA3	R	0b	

5.7.1.388 EEPROM_CONTROL_13 Register (Offset = 0x1EC) [reset = 0x0]

EEPROM_CONTROL_13 is shown in Figure 5-455 and described in Table 5-427.

Return to the Summary Table.

Figure 5-455. EEPROM_CONTROL_13 Register

7	6	5	4	3	2	1	0
TM_EE_READ_DATA2							
R-0b							

Table 5-427. EEPROM_CONTROL_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_READ_DATA2	R	0b	

ADVANCE INFORMATION

5.7.1.389 EEPROM_CONTROL_14 Register (Offset = 0x1ED) [reset = 0x0]

EEPROM_CONTROL_14 is shown in Figure 5-456 and described in Table 5-428.

Return to the Summary Table.

Figure 5-456. EEPROM_CONTROL_14 Register

7	6	5	4	3	2	1	0
TM_EE_READ_DATA1							
R-0b							

Table 5-428. EEPROM_CONTROL_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_READ_DATA1	R	0b	

5.7.1.390 EEPROM_CONTROL_15 Register (Offset = 0x1EE) [reset = 0x0]

EEPROM_CONTROL_15 is shown in Figure 5-457 and described in Table 5-429.

Return to the Summary Table.

Figure 5-457. EEPROM_CONTROL_15 Register

7	6	5	4	3	2	1	0
TM_EE_READ_DATA0							
R-0b							

Table 5-429. EEPROM_CONTROL_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TM_EE_READ_DATA0	R	0b	

5.7.1.391 EEPROM_CONTROL_16 Register (Offset = 0x1EF) [reset = 0x0]

EEPROM_CONTROL_16 is shown in Figure 5-458 and described in Table 5-430.

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The TM_EE_CMD_* bits execute commands that are carried out by the digital Eeprom controller. These bits are all WriteSelfClear, such that they are only high for 1 cycle to initiate the operation.
If multiple commands are set together they will execute in the order 1)TM_EE_CMD_READ 2)TM_EE_CMD_ERASE 3)TM_EE_CMD_PROG.

Figure 5-458. EEPROM_CONTROL_16 Register

7	6	5	4	3	2	1	0
RESERVED						TM_EE_CMD_PROG	TM_EE_CMD_READ
R/W-0b						R/WSelfClrF-0b	R/WSelfClrF-0b

Table 5-430. EEPROM_CONTROL_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b	
1	TM_EE_CMD_PROG	R/WSelfClrF	0b	By default it will program the entire Eeprom using the contents of the shadow registers. This requires 1 Eeprom program cycle for each register address. See TM_EE_CFG_*_PROG for alternate behavior. When accessing individual EEPROM addresses (TM_EE_CFG_SINGLE=1), this bit is write protected if access points to trim values according to TM_EE_ADDR and TM_EE_CFG_BANK_DIS.
0	TM_EE_CMD_READ	R/WSelfClrF	0b	By default it will read the entire Eeprom into the shadow registesrs. This requires 1 Eeprom read cycle for each register address. See TM_EE_CFG_*_READ for alternate behavior. When accessing individual EEPROM addresses (TM_EE_CFG_SINGLE=1), this bit is write protected if access points to trim values according to TM_EE_ADDR and TM_EE_CFG_BANK_DIS.

5.7.1.392 EEPROM_CONTROL_17 Register (Offset = 0x1F0) [reset = 0x0]

EEPROM_CONTROL_17 is shown in Figure 5-459 and described in Table 5-431.

Return to the Summary Table.

Directly force Eeprom control signals (Corresponding name) and thereby bypassing the use of the Eeprom controller.
Note these register bits are ORed with Eeprom controller driver, so it is imperative that they are used separately.
For detailed description of Eeprom control signals see Synopsys Design Ware NVM Databook (https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.33756.60785).

Figure 5-459. EEPROM_CONTROL_17 Register

7	6	5	4	3	2	1	0
RESERVED		TM_EE_FORCE_EN	TM_EE_FORCE_READ	TM_EE_FORCE_PROG	TM_EE_FORCE_ERASE	TM_EE_FORCE_IP_EN	TM_EE_FORCE_CP_EN
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-431. EEPROM_CONTROL_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	TM_EE_FORCE_EN	R/W	0b	Force direct control of Eeprom via TM bits
4	TM_EE_FORCE_READ	R/W	0b	When high forces eeprom read input high
3	TM_EE_FORCE_PROG	R/W	0b	When high forces eeprom prog input high
2	TM_EE_FORCE_ERASE	R/W	0b	When high forces eeprom erase input high
1	TM_EE_FORCE_IP_EN	R/W	0b	When high forces eeprom ip_en input high
0	TM_EE_FORCE_CP_EN	R/W	0b	When high forces eeprom cp_enable input high

ADVANCE INFORMATION

5.7.1.393 EEPROM_CONTROL_18 Register (Offset = 0x1F1) [reset = 0x0]

EEPROM_CONTROL_18 is shown in Figure 5-460 and described in Table 5-432.

Return to the Summary Table.

Directly drive Eeprom test signals (Corresponding name) and thereby bypassing the use of the Eeprom controller.
Be aware that some of these signals are also utilized by Eeprom controller to achieve higher level functionality (See TM_EE_CFG_*).
For detailed description of Eeprom control signals see Synopsys Design Ware NVM Databook (https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.33756.60785).

Figure 5-460. EEPROM_CONTROL_18 Register

7	6	5	4	3	2	1	0
TM_EE_TEST_CELL_CURRENT_MON_EN	TM_EE_TEST_OSC_MON_EN	TM_EE_TEST_HV_BIAS_WEAK_RATIO_EN	TM_EE_TEST_MARGIN_OVR_EN	TM_EE_TEST_MARGIN_READ_EN	TM_EE_TEST_BULK_EVEN_EN	TM_EE_TEST_BULK_ODD_EN	TM_EE_FAST_ERASE_PROG_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 5-432. EEPROM_CONTROL_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TM_EE_TEST_CELL_CURRENT_MON_EN	R/W	0b	Cell current monitor test mode enable.
6	TM_EE_TEST_OSC_MON_EN	R/W	0b	Oscillator monitor test mode enable.
5	TM_EE_TEST_HV_BIAS_WEAK_RATIO_EN	R/W	0b	HV Bias weak ratio test mode enable.
4	TM_EE_TEST_MARGIN_OVR_EN	R/W	0b	Margin read override test mode enable.
3	TM_EE_TEST_MARGIN_READ_EN	R/W	0b	Margin read test mode enable.
2	TM_EE_TEST_BULK_EVEN_EN	R/W	0b	Bulk program/erase on even rows test mode enable.
1	TM_EE_TEST_BULK_ODD_EN	R/W	0b	Bulk program/erase on odd rows test mode enable.
0	TM_EE_FAST_ERASE_PROG_EN	R/W	0b	Fast erase/program enable - Intended to reduce production test time.

ADVANCE INFORMATION

5.7.1.394 EEPROM_CONTROL_19 Register (Offset = 0x1F2) [reset = 0x0]

EEPROM_CONTROL_19 is shown in Figure 5-461 and described in Table 5-433.

Return to the Summary Table.

Figure 5-461. EEPROM_CONTROL_19 Register

7	6	5	4	3	2	1	0
RESERVED		TM_EE_PROG_SERIAL	TM_EE_TEST_V1V_MON_OVR_EN	TM_EE_TEST_VTUN_MON_EN	TM_EE_MARGIN_TRIM		
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b		

Table 5-433. EEPROM_CONTROL_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5	TM_EE_PROG_SERIAL	R/W	0b	Program eeprom banks in a serial fashion.
4	TM_EE_TEST_V1V_MON_OVR_EN	R/W	0b	V1V monitor/override enable - Used to enable the test mode to monitor internal V1V reference voltage on TEST_V1V_MON_OVR.
3	TM_EE_TEST_VTUN_MON_EN	R/W	0b	VTUN monitor enable - Used to enable the test mode to monitor internal tunneling voltage on TEST_VTUN_MON.
2:0	TM_EE_MARGIN_TRIM	R/W	0b	Margin read setting - Swts margin level only during margin read test mode. In user mode these pins are ignored.

ADVANCE INFORMATION

5.7.1.395 EEPROM_CONTROL_20 Register (Offset = 0x1F3) [reset = 0x0]

EEPROM_CONTROL_20 is shown in Figure 5-462 and described in Table 5-434.

Return to the Summary Table.

Figure 5-462. EEPROM_CONTROL_20 Register

7	6	5	4	3	2	1	0
RESERVED					tm_ee_read_fail	ee_active	tm_ee_ready
R-0b					R-0b	R-0b	R-0b

Table 5-434. EEPROM_CONTROL_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0b	
2	tm_ee_read_fail	R	0b	Indicates a mismatch occurred during an Eeprom Read. This is only meaningful under specific testmode conditions.
1	ee_active	R	0b	High if any of the eeprom controllers are active (Reading, Erasing, or Programming)
0	tm_ee_ready	R	0b	Indication that all eeprom banks are ready, which is useful for manual eeprom operations.

5.7.1.396 TRIM_VMVCCA_0 Register (Offset = 0x200) [reset = 0x0]

TRIM_VMVCCA_0 is shown in Figure 5-463 and described in Table 5-435.

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Figure 5-463. TRIM_VMVCCA_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmvcca_bg				
R/W-0b			R/W-0b				

Table 5-435. TRIM_VMVCCA_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmvcca_bg	R/W	0b	

ADVANCE INFORMATION

5.7.1.397 TRIM_VMVCCA_1 Register (Offset = 0x201) [reset = 0x0]

TRIM_VMVCCA_1 is shown in Figure 5-464 and described in Table 5-436.

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Figure 5-464. TRIM_VMVCCA_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmvcca_rdiv_1v2				
R/W-0b			R/W-0b				

Table 5-436. TRIM_VMVCCA_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmvcca_rdiv_1v2	R/W	0b	

5.7.1.398 TRIM_VMVCCA_2 Register (Offset = 0x202) [reset = 0x0]

TRIM_VMVCCA_2 is shown in Figure 5-465 and described in Table 5-437.

Return to the Summary Table.

Figure 5-465. TRIM_VMVCCA_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmvcca_rdiv_0v6				
R/W-0b			R/W-0b				

Table 5-437. TRIM_VMVCCA_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmvcca_rdiv_0v6	R/W	0b	

ADVANCE INFORMATION

5.7.1.399 TRIM_VMPVIN_0 Register (Offset = 0x204) [reset = 0x0]

TRIM_VMPVIN_0 is shown in Figure 5-466 and described in Table 5-438.

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Figure 5-466. TRIM_VMPVIN_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmpvin_bg				
R/W-0b			R/W-0b				

Table 5-438. TRIM_VMPVIN_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmpvin_bg	R/W	0b	

5.7.1.400 TRIM_VMPVIN_1 Register (Offset = 0x205) [reset = 0x0]

TRIM_VMPVIN_1 is shown in Figure 5-467 and described in Table 5-439.

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Figure 5-467. TRIM_VMPVIN_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmpvin_rdiv_1v2				
R/W-0b			R/W-0b				

Table 5-439. TRIM_VMPVIN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmpvin_rdiv_1v2	R/W	0b	

ADVANCE INFORMATION

5.7.1.401 TRIM_INT_0 Register (Offset = 0x207) [reset = 0x0]

TRIM_INT_0 is shown in Figure 5-468 and described in Table 5-440.

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Figure 5-468. TRIM_INT_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_refsys_bg				
R/W-0b			R/W-0b				

Table 5-440. TRIM_INT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_refsys_bg	R/W	0b	

5.7.1.402 TRIM_INT_1 Register (Offset = 0x208) [reset = 0x0]

TRIM_INT_1 is shown in Figure 5-469 and described in Table 5-441.

Return to the Summary Table.

Figure 5-469. TRIM_INT_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_refsys_rdiv_1v2				
R/W-0b			R/W-0b				

Table 5-441. TRIM_INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_refsys_rdiv_1v2	R/W	0b	

ADVANCE INFORMATION

5.7.1.403 TRIM_INT_2 Register (Offset = 0x209) [reset = 0x0]

TRIM_INT_2 is shown in Figure 5-470 and described in Table 5-442.

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Figure 5-470. TRIM_INT_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_refsys_ibias				
R/W-0b			R/W-0b				

Table 5-442. TRIM_INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_refsys_ibias	R/W	0b	

5.7.1.404 TRIM_INT_3 Register (Offset = 0x20A) [reset = 0x10]

TRIM_INT_3 is shown in Figure 5-471 and described in Table 5-443.

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Figure 5-471. TRIM_INT_3 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ldo_int				
R/W-0b			R/W-10000b				

Table 5-443. TRIM_INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ldo_int	R/W	10000b	

ADVANCE INFORMATION

5.7.1.405 TRIM_INT_4 Register (Offset = 0x20B) [reset = 0xF]

TRIM_INT_4 is shown in Figure 5-472 and described in Table 5-444.

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trim_osc_20mhz is separated from int_trim_ocore bus, so that it can be located to RTC domain.
The reason for moving it to RTC domain is to speed up startup from LP_STANDBY.
RTC domain stays powered up in LP_STANDBY so counting the 100us NVM_LDO startup delay is done with correct trim value.
trim_osc_20mhz is routed through INT domain to LEO_FS_DIGITAL output, so the output will be INT domain signal (since it goes throug level shifters).

Figure 5-472. TRIM_INT_4 Register

7	6	5	4	3	2	1	0
RESERVED	trim_osc_20mhz						
R/W-0b	R/W-1111b						

Table 5-444. TRIM_INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	trim_osc_20mhz	R/W	1111b	

ADVANCE INFORMATION

5.7.1.406 TRIM_INT_5 Register (Offset = 0x20C) [reset = 0x0]

TRIM_INT_5 is shown in Figure 5-473 and described in Table 5-445.

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Figure 5-473. TRIM_INT_5 Register

7	6	5	4	3	2	1	0
RESERVED		trim_osc_128khz					
R/W-0b		R/W-0b					

Table 5-445. TRIM_INT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_osc_128khz	R/W	0b	

ADVANCE INFORMATION

5.7.1.407 TRIM_INT_6 Register (Offset = 0x20D) [reset = 0x0]

TRIM_INT_6 is shown in Figure 5-474 and described in Table 5-446.

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Figure 5-474. TRIM_INT_6 Register

7	6	5	4	3	2	1	0
RESERVED	trim_osc_52mhz						
R/W-0b	R/W-0b						

Table 5-446. TRIM_INT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	trim_osc_52mhz	R/W	0b	

5.7.1.408 TRIM_INT_7 Register (Offset = 0x20E) [reset = 0x0]

TRIM_INT_7 is shown in Figure 5-475 and described in Table 5-447.

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Figure 5-475. TRIM_INT_7 Register

7	6	5	4	3	2	1	0
RESERVED				trim_amux_buffer			
R/W-0b				R/W-0b			

Table 5-447. TRIM_INT_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_amux_buffer	R/W	0b	

ADVANCE INFORMATION

5.7.1.409 TRIM_INT_8 Register (Offset = 0x20F) [reset = 0x0]

TRIM_INT_8 is shown in Figure 5-476 and described in Table 5-448.

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Figure 5-476. TRIM_INT_8 Register

7	6	5	4	3	2	1	0
RESERVED	trim_monitor_osc_20mhz						
R/W-0b	R/W-0b						

Table 5-448. TRIM_INT_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	trim_monitor_osc_20mhz	R/W	0b	

5.7.1.410 TRIM_SAFETY_0 Register (Offset = 0x212) [reset = 0x0]

TRIM_SAFETY_0 is shown in Figure 5-477 and described in Table 5-449.

Return to the Summary Table.

Figure 5-477. TRIM_SAFETY_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_safety_ibias				
R/W-0b			R/W-0b				

Table 5-449. TRIM_SAFETY_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_safety_ibias	R/W	0b	

5.7.1.411 TRIM_SAFETY_1 Register (Offset = 0x213) [reset = 0x0]

TRIM_SAFETY_1 is shown in Figure 5-478 and described in Table 5-450.

Return to the Summary Table.

Figure 5-478. TRIM_SAFETY_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck1_lshift_ov				
R/W-0b			R/W-0b				

Table 5-450. TRIM_SAFETY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck1_lshift_ov	R/W	0b	

5.7.1.412 TRIM_SAFETY_2 Register (Offset = 0x214) [reset = 0x0]

TRIM_SAFETY_2 is shown in Figure 5-479 and described in Table 5-451.

Return to the Summary Table.

Figure 5-479. TRIM_SAFETY_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck1_lshift_uv				
R/W-0b			R/W-0b				

Table 5-451. TRIM_SAFETY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck1_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.413 TRIM_SAFETY_3 Register (Offset = 0x215) [reset = 0x0]

TRIM_SAFETY_3 is shown in Figure 5-480 and described in Table 5-452.

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Figure 5-480. TRIM_SAFETY_3 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck1_vref_dac				
R/W-0b			R/W-0b				

Table 5-452. TRIM_SAFETY_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck1_vref_dac	R/W	0b	

5.7.1.414 TRIM_SAFETY_4 Register (Offset = 0x216) [reset = 0x0]

TRIM_SAFETY_4 is shown in Figure 5-481 and described in Table 5-453.

Return to the Summary Table.

Figure 5-481. TRIM_SAFETY_4 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck1_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-453. TRIM_SAFETY_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck1_rdiv_uv	R/W	0b	

5.7.1.415 TRIM_SAFETY_5 Register (Offset = 0x217) [reset = 0x0]

TRIM_SAFETY_5 is shown in Figure 5-482 and described in Table 5-454.

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Figure 5-482. TRIM_SAFETY_5 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck2_lshift_ov				
R/W-0b			R/W-0b				

Table 5-454. TRIM_SAFETY_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck2_lshift_ov	R/W	0b	

5.7.1.416 TRIM_SAFETY_6 Register (Offset = 0x218) [reset = 0x0]

TRIM_SAFETY_6 is shown in Figure 5-483 and described in Table 5-455.

Return to the Summary Table.

Figure 5-483. TRIM_SAFETY_6 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck2_lshift_uv				
R/W-0b			R/W-0b				

Table 5-455. TRIM_SAFETY_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck2_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.417 TRIM_SAFETY_7 Register (Offset = 0x219) [reset = 0x0]

TRIM_SAFETY_7 is shown in Figure 5-484 and described in Table 5-456.

Return to the Summary Table.

Figure 5-484. TRIM_SAFETY_7 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck2_vref_dac				
R/W-0b			R/W-0b				

Table 5-456. TRIM_SAFETY_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck2_vref_dac	R/W	0b	

5.7.1.418 TRIM_SAFETY_8 Register (Offset = 0x21A) [reset = 0x0]

TRIM_SAFETY_8 is shown in Figure 5-485 and described in Table 5-457.

Return to the Summary Table.

Figure 5-485. TRIM_SAFETY_8 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck2_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-457. TRIM_SAFETY_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck2_rdiv_uv	R/W	0b	

5.7.1.419 TRIM_SAFETY_9 Register (Offset = 0x21B) [reset = 0x0]

TRIM_SAFETY_9 is shown in Figure 5-486 and described in Table 5-458.

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Figure 5-486. TRIM_SAFETY_9 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck3_lshift_ov				
R/W-0b			R/W-0b				

Table 5-458. TRIM_SAFETY_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck3_lshift_ov	R/W	0b	

5.7.1.420 TRIM_SAFETY_10 Register (Offset = 0x21C) [reset = 0x0]

TRIM_SAFETY_10 is shown in Figure 5-487 and described in Table 5-459.

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Figure 5-487. TRIM_SAFETY_10 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck3_lshift_uv				
R/W-0b			R/W-0b				

Table 5-459. TRIM_SAFETY_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck3_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.421 TRIM_SAFETY_11 Register (Offset = 0x21D) [reset = 0x0]

TRIM_SAFETY_11 is shown in Figure 5-488 and described in Table 5-460.

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Figure 5-488. TRIM_SAFETY_11 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck3_vref_dac				
R/W-0b			R/W-0b				

Table 5-460. TRIM_SAFETY_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck3_vref_dac	R/W	0b	

ADVANCE INFORMATION

5.7.1.422 TRIM_SAFETY_12 Register (Offset = 0x21E) [reset = 0x0]

TRIM_SAFETY_12 is shown in Figure 5-489 and described in Table 5-461.

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Figure 5-489. TRIM_SAFETY_12 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck3_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-461. TRIM_SAFETY_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck3_rdiv_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.423 TRIM_SAFETY_13 Register (Offset = 0x21F) [reset = 0x0]

TRIM_SAFETY_13 is shown in Figure 5-490 and described in Table 5-462.

Return to the Summary Table.

Figure 5-490. TRIM_SAFETY_13 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck4_lshift_ov				
R/W-0b			R/W-0b				

Table 5-462. TRIM_SAFETY_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck4_lshift_ov	R/W	0b	

5.7.1.424 TRIM_SAFETY_14 Register (Offset = 0x220) [reset = 0x0]

TRIM_SAFETY_14 is shown in Figure 5-491 and described in Table 5-463.

Return to the Summary Table.

Figure 5-491. TRIM_SAFETY_14 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck4_lshift_uv				
R/W-0b			R/W-0b				

Table 5-463. TRIM_SAFETY_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck4_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.425 TRIM_SAFETY_15 Register (Offset = 0x221) [reset = 0x0]

TRIM_SAFETY_15 is shown in Figure 5-492 and described in Table 5-464.

Return to the Summary Table.

Figure 5-492. TRIM_SAFETY_15 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck4_vref_dac				
R/W-0b			R/W-0b				

Table 5-464. TRIM_SAFETY_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck4_vref_dac	R/W	0b	

ADVANCE INFORMATION

5.7.1.426 TRIM_SAFETY_16 Register (Offset = 0x222) [reset = 0x0]

TRIM_SAFETY_16 is shown in Figure 5-493 and described in Table 5-465.

Return to the Summary Table.

Figure 5-493. TRIM_SAFETY_16 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck4_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-465. TRIM_SAFETY_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck4_rdiv_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.427 TRIM_SAFETY_17 Register (Offset = 0x223) [reset = 0x0]

TRIM_SAFETY_17 is shown in Figure 5-494 and described in Table 5-466.

Return to the Summary Table.

Figure 5-494. TRIM_SAFETY_17 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck5_lshift_ov				
R/W-0b			R/W-0b				

Table 5-466. TRIM_SAFETY_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck5_lshift_ov	R/W	0b	

5.7.1.428 TRIM_SAFETY_18 Register (Offset = 0x224) [reset = 0x0]

TRIM_SAFETY_18 is shown in Figure 5-495 and described in Table 5-467.

Return to the Summary Table.

Figure 5-495. TRIM_SAFETY_18 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck5_lshift_uv				
R/W-0b			R/W-0b				

Table 5-467. TRIM_SAFETY_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck5_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.429 TRIM_SAFETY_19 Register (Offset = 0x225) [reset = 0x0]

TRIM_SAFETY_19 is shown in Figure 5-496 and described in Table 5-468.

Return to the Summary Table.

Figure 5-496. TRIM_SAFETY_19 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck5_vref_dac				
R/W-0b			R/W-0b				

Table 5-468. TRIM_SAFETY_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck5_vref_dac	R/W	0b	

5.7.1.430 TRIM_SAFETY_20 Register (Offset = 0x226) [reset = 0x0]

TRIM_SAFETY_20 is shown in Figure 5-497 and described in Table 5-469.

Return to the Summary Table.

Figure 5-497. TRIM_SAFETY_20 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_buck5_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-469. TRIM_SAFETY_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_buck5_rdiv_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.431 TRIM_SAFETY_21 Register (Offset = 0x227) [reset = 0x0]

TRIM_SAFETY_21 is shown in Figure 5-498 and described in Table 5-470.

Return to the Summary Table.

Figure 5-498. TRIM_SAFETY_21 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo1_lshift_ov				
R/W-0b			R/W-0b				

Table 5-470. TRIM_SAFETY_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo1_lshift_ov	R/W	0b	

5.7.1.432 TRIM_SAFETY_22 Register (Offset = 0x228) [reset = 0x0]

TRIM_SAFETY_22 is shown in Figure 5-499 and described in Table 5-471.

Return to the Summary Table.

Figure 5-499. TRIM_SAFETY_22 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo1_lshift_uv				
R/W-0b			R/W-0b				

Table 5-471. TRIM_SAFETY_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo1_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.433 TRIM_SAFETY_23 Register (Offset = 0x229) [reset = 0x0]

TRIM_SAFETY_23 is shown in Figure 5-500 and described in Table 5-472.

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Figure 5-500. TRIM_SAFETY_23 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo1_vref_dac				
R/W-0b			R/W-0b				

Table 5-472. TRIM_SAFETY_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo1_vref_dac	R/W	0b	

5.7.1.434 TRIM_SAFETY_24 Register (Offset = 0x22A) [reset = 0x0]

TRIM_SAFETY_24 is shown in Figure 5-501 and described in Table 5-473.

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Figure 5-501. TRIM_SAFETY_24 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo1_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-473. TRIM_SAFETY_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo1_rdiv_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.435 TRIM_SAFETY_25 Register (Offset = 0x22B) [reset = 0x0]

TRIM_SAFETY_25 is shown in Figure 5-502 and described in Table 5-474.

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Figure 5-502. TRIM_SAFETY_25 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo2_lshift_ov				
R/W-0b			R/W-0b				

Table 5-474. TRIM_SAFETY_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo2_lshift_ov	R/W	0b	

5.7.1.436 TRIM_SAFETY_26 Register (Offset = 0x22C) [reset = 0x0]

TRIM_SAFETY_26 is shown in Figure 5-503 and described in Table 5-475.

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Figure 5-503. TRIM_SAFETY_26 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo2_lshift_uv				
R/W-0b			R/W-0b				

Table 5-475. TRIM_SAFETY_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo2_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.437 TRIM_SAFETY_27 Register (Offset = 0x22D) [reset = 0x0]

TRIM_SAFETY_27 is shown in Figure 5-504 and described in Table 5-476.

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Figure 5-504. TRIM_SAFETY_27 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo2_vref_dac				
R/W-0b			R/W-0b				

Table 5-476. TRIM_SAFETY_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo2_vref_dac	R/W	0b	

5.7.1.438 TRIM_SAFETY_28 Register (Offset = 0x22E) [reset = 0x0]

TRIM_SAFETY_28 is shown in Figure 5-505 and described in Table 5-477.

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Figure 5-505. TRIM_SAFETY_28 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo2_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-477. TRIM_SAFETY_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo2_rdiv_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.439 TRIM_SAFETY_29 Register (Offset = 0x22F) [reset = 0x0]

TRIM_SAFETY_29 is shown in Figure 5-506 and described in Table 5-478.

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Figure 5-506. TRIM_SAFETY_29 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo3_lshift_ov				
R/W-0b			R/W-0b				

Table 5-478. TRIM_SAFETY_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo3_lshift_ov	R/W	0b	

5.7.1.440 TRIM_SAFETY_30 Register (Offset = 0x230) [reset = 0x0]

TRIM_SAFETY_30 is shown in Figure 5-507 and described in Table 5-479.

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Figure 5-507. TRIM_SAFETY_30 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo3_lshift_uv				
R/W-0b			R/W-0b				

Table 5-479. TRIM_SAFETY_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo3_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.441 TRIM_SAFETY_31 Register (Offset = 0x231) [reset = 0x0]

TRIM_SAFETY_31 is shown in Figure 5-508 and described in Table 5-480.

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Figure 5-508. TRIM_SAFETY_31 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo3_vref_dac				
R/W-0b			R/W-0b				

Table 5-480. TRIM_SAFETY_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo3_vref_dac	R/W	0b	

5.7.1.442 TRIM_SAFETY_32 Register (Offset = 0x232) [reset = 0x0]

TRIM_SAFETY_32 is shown in Figure 5-509 and described in Table 5-481.

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Figure 5-509. TRIM_SAFETY_32 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo3_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-481. TRIM_SAFETY_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo3_rdiv_uv	R/W	0b	

5.7.1.443 TRIM_SAFETY_33 Register (Offset = 0x233) [reset = 0x0]

TRIM_SAFETY_33 is shown in Figure 5-510 and described in Table 5-482.

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Figure 5-510. TRIM_SAFETY_33 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo4_lshift_ov				
R/W-0b			R/W-0b				

Table 5-482. TRIM_SAFETY_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo4_lshift_ov	R/W	0b	

5.7.1.444 TRIM_SAFETY_34 Register (Offset = 0x234) [reset = 0x0]

TRIM_SAFETY_34 is shown in Figure 5-511 and described in Table 5-483.

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Figure 5-511. TRIM_SAFETY_34 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo4_lshift_uv				
R/W-0b			R/W-0b				

Table 5-483. TRIM_SAFETY_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo4_lshift_uv	R/W	0b	

ADVANCE INFORMATION

5.7.1.445 TRIM_SAFETY_35 Register (Offset = 0x235) [reset = 0x0]

TRIM_SAFETY_35 is shown in Figure 5-512 and described in Table 5-484.

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Figure 5-512. TRIM_SAFETY_35 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo4_vref_dac				
R/W-0b			R/W-0b				

Table 5-484. TRIM_SAFETY_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo4_vref_dac	R/W	0b	

5.7.1.446 TRIM_SAFETY_36 Register (Offset = 0x236) [reset = 0x0]

TRIM_SAFETY_36 is shown in Figure 5-513 and described in Table 5-485.

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Figure 5-513. TRIM_SAFETY_36 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vmon_ldo4_rdiv_uv				
R/W-0b			R/W-0b				

Table 5-485. TRIM_SAFETY_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vmon_ldo4_rdiv_uv	R/W	0b	

5.7.1.447 TRIM_SAFETY_37 Register (Offset = 0x237) [reset = 0x0]

TRIM_SAFETY_37 is shown in Figure 5-514 and described in Table 5-486.

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Figure 5-514. TRIM_SAFETY_37 Register

7	6	5	4	3	2	1	0
RESERVED			trim_tsd_offset				
R/W-0b			R/W-0b				

Table 5-486. TRIM_SAFETY_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_tsd_offset	R/W	0b	

5.7.1.448 TRIM_SAFETY_38 Register (Offset = 0x238) [reset = 0x0]

TRIM_SAFETY_38 is shown in Figure 5-515 and described in Table 5-487.

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Figure 5-515. TRIM_SAFETY_38 Register

7	6	5	4	3	2	1	0
RESERVED			trim_tsd_gain				
R/W-0b			R/W-0b				

Table 5-487. TRIM_SAFETY_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_tsd_gain	R/W	0b	

ADVANCE INFORMATION

5.7.1.449 TRIM_VM_VSYS_0 Register (Offset = 0x23A) [reset = 0x0]

TRIM_VM_VSYS_0 is shown in Figure 5-516 and described in Table 5-488.

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Figure 5-516. TRIM_VM_VSYS_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vsys_mon_bg				
R/W-0b			R/W-0b				

Table 5-488. TRIM_VM_VSYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vsys_mon_bg	R/W	0b	

5.7.1.450 TRIM_VM_VSYS_1 Register (Offset = 0x23B) [reset = 0x0]

TRIM_VM_VSYS_1 is shown in Figure 5-517 and described in Table 5-489.

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Figure 5-517. TRIM_VM_VSYS_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vsys_mon_rdiv_1v2				
R/W-0b			R/W-0b				

Table 5-489. TRIM_VM_VSYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vsys_mon_rdiv_1v2	R/W	0b	

ADVANCE INFORMATION

5.7.1.451 TRIM_RTC_0 Register (Offset = 0x23D) [reset = 0x0]

TRIM_RTC_0 is shown in Figure 5-518 and described in Table 5-490.

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Figure 5-518. TRIM_RTC_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_rtc_bg				
R/W-0b			R/W-0b				

Table 5-490. TRIM_RTC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_rtc_bg	R/W	0b	

5.7.1.452 TRIM_RTC_1 Register (Offset = 0x23E) [reset = 0x0]

TRIM_RTC_1 is shown in Figure 5-519 and described in Table 5-491.

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Figure 5-519. TRIM_RTC_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_rtc_rdiv_1v2				
R/W-0b			R/W-0b				

Table 5-491. TRIM_RTC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_rtc_rdiv_1v2	R/W	0b	

ADVANCE INFORMATION

5.7.1.453 TRIM_RTC_2 Register (Offset = 0x23F) [reset = 0x10]

TRIM_RTC_2 is shown in Figure 5-520 and described in Table 5-492.

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Figure 5-520. TRIM_RTC_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_rtc_ldo				
R/W-0b			R/W-10000b				

Table 5-492. TRIM_RTC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_rtc_ldo	R/W	10000b	

5.7.1.454 TRIM_DPLL_0 Register (Offset = 0x245) [reset = 0x0]

TRIM_DPLL_0 is shown in Figure 5-521 and described in Table 5-493.

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Figure 5-521. TRIM_DPLL_0 Register

7	6	5	4	3	2	1	0
RESERVED	trim_dco						
R/W-0b	R/W-0b						

Table 5-493. TRIM_DPLL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	trim_dco	R/W	0b	

5.7.1.455 TRIM_LDO1_0 Register (Offset = 0x247) [reset = 0x0]

TRIM_LDO1_0 is shown in Figure 5-522 and described in Table 5-494.

Return to the Summary Table.

Figure 5-522. TRIM_LDO1_0 Register

7	6	5	4	3	2	1	0
RESERVED		trim_ldo1_ref					
R/W-0b		R/W-0b					

Table 5-494. TRIM_LDO1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_ldo1_ref	R/W	0b	

5.7.1.456 TRIM_LDO1_1 Register (Offset = 0x248) [reset = 0x0]

TRIM_LDO1_1 is shown in Figure 5-523 and described in Table 5-495.

Return to the Summary Table.

Figure 5-523. TRIM_LDO1_1 Register

7	6	5	4	3	2	1	0
RESERVED		trim_ldo1					
R/W-0b		R/W-0b					

Table 5-495. TRIM_LDO1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_ldo1	R/W	0b	

ADVANCE INFORMATION

5.7.1.457 TRIM_LDO1_2 Register (Offset = 0x249) [reset = 0x0]

TRIM_LDO1_2 is shown in Figure 5-524 and described in Table 5-496.

Return to the Summary Table.

Figure 5-524. TRIM_LDO1_2 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo1_ilim1			
R/W-0b				R/W-0b			

Table 5-496. TRIM_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo1_ilim1	R/W	0b	

5.7.1.458 TRIM_LDO1_3 Register (Offset = 0x24A) [reset = 0x0]

TRIM_LDO1_3 is shown in Figure 5-525 and described in Table 5-497.

Return to the Summary Table.

Figure 5-525. TRIM_LDO1_3 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo1_ilim2			
R/W-0b				R/W-0b			

Table 5-497. TRIM_LDO1_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo1_ilim2	R/W	0b	

ADVANCE INFORMATION

5.7.1.459 TRIM_LDO2_0 Register (Offset = 0x24C) [reset = 0x0]

TRIM_LDO2_0 is shown in Figure 5-526 and described in Table 5-498.

Return to the Summary Table.

Figure 5-526. TRIM_LDO2_0 Register

7	6	5	4	3	2	1	0
RESERVED		trim_ldo2_ref					
R/W-0b		R/W-0b					

Table 5-498. TRIM_LDO2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_ldo2_ref	R/W	0b	

5.7.1.460 TRIM_LDO2_1 Register (Offset = 0x24D) [reset = 0x0]

TRIM_LDO2_1 is shown in Figure 5-527 and described in Table 5-499.

Return to the Summary Table.

Figure 5-527. TRIM_LDO2_1 Register

7	6	5	4	3	2	1	0
RESERVED		trim_ldo2					
R/W-0b		R/W-0b					

Table 5-499. TRIM_LDO2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_ldo2	R/W	0b	

ADVANCE INFORMATION

5.7.1.461 TRIM_LDO2_2 Register (Offset = 0x24E) [reset = 0x0]

TRIM_LDO2_2 is shown in Figure 5-528 and described in Table 5-500.

Return to the Summary Table.

Figure 5-528. TRIM_LDO2_2 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo2_ilim1			
R/W-0b				R/W-0b			

Table 5-500. TRIM_LDO2_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo2_ilim1	R/W	0b	

5.7.1.462 TRIM_LDO2_3 Register (Offset = 0x24F) [reset = 0x0]

TRIM_LDO2_3 is shown in Figure 5-529 and described in Table 5-501.

Return to the Summary Table.

Figure 5-529. TRIM_LDO2_3 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo2_ilim2			
R/W-0b				R/W-0b			

Table 5-501. TRIM_LDO2_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo2_ilim2	R/W	0b	

ADVANCE INFORMATION

5.7.1.463 TRIM_LDO3_0 Register (Offset = 0x251) [reset = 0x0]

TRIM_LDO3_0 is shown in Figure 5-530 and described in Table 5-502.

Return to the Summary Table.

Figure 5-530. TRIM_LDO3_0 Register

7	6	5	4	3	2	1	0
RESERVED		trim_ldo3_ref					
R/W-0b		R/W-0b					

Table 5-502. TRIM_LDO3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_ldo3_ref	R/W	0b	

5.7.1.464 TRIM_LDO3_1 Register (Offset = 0x252) [reset = 0x0]

TRIM_LDO3_1 is shown in Figure 5-531 and described in Table 5-503.

Return to the Summary Table.

Figure 5-531. TRIM_LDO3_1 Register

7	6	5	4	3	2	1	0
RESERVED		trim_ldo3					
R/W-0b		R/W-0b					

Table 5-503. TRIM_LDO3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0b	
5:0	trim_ldo3	R/W	0b	

ADVANCE INFORMATION

5.7.1.465 TRIM_LDO3_2 Register (Offset = 0x253) [reset = 0x0]

TRIM_LDO3_2 is shown in Figure 5-532 and described in Table 5-504.

Return to the Summary Table.

Figure 5-532. TRIM_LDO3_2 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo3_ilim1			
R/W-0b				R/W-0b			

Table 5-504. TRIM_LDO3_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo3_ilim1	R/W	0b	

5.7.1.466 TRIM_LDO3_3 Register (Offset = 0x254) [reset = 0x0]

TRIM_LDO3_3 is shown in Figure 5-533 and described in Table 5-505.

Return to the Summary Table.

Figure 5-533. TRIM_LDO3_3 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo3_ilim2			
R/W-0b				R/W-0b			

Table 5-505. TRIM_LDO3_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo3_ilim2	R/W	0b	

ADVANCE INFORMATION

5.7.1.467 TRIM_LDO4_0 Register (Offset = 0x256) [reset = 0x0]

TRIM_LDO4_0 is shown in Figure 5-534 and described in Table 5-506.

Return to the Summary Table.

Figure 5-534. TRIM_LDO4_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ldo4_low				
R/W-0b			R/W-0b				

Table 5-506. TRIM_LDO4_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ldo4_low	R/W	0b	

5.7.1.468 TRIM_LDO4_1 Register (Offset = 0x257) [reset = 0x0]

TRIM_LDO4_1 is shown in Figure 5-535 and described in Table 5-507.

Return to the Summary Table.

Figure 5-535. TRIM_LDO4_1 Register

7	6	5	4	3	2	1	0
RESERVED	trim_ldo4_high						
R/W-0b	R/W-0b						

Table 5-507. TRIM_LDO4_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	trim_ldo4_high	R/W	0b	

5.7.1.469 TRIM_LDO4_2 Register (Offset = 0x258) [reset = 0x0]

TRIM_LDO4_2 is shown in Figure 5-536 and described in Table 5-508.

Return to the Summary Table.

Figure 5-536. TRIM_LDO4_2 Register

7	6	5	4	3	2	1	0
RESERVED				trim_ldo4_ilim			
R/W-0b				R/W-0b			

Table 5-508. TRIM_LDO4_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_ldo4_ilim	R/W	0b	

5.7.1.470 BUCK1_TRIM_REG_0 Register (Offset = 0x260) [reset = 0x0]

BUCK1_TRIM_REG_0 is shown in Figure 5-537 and described in Table 5-509.

Return to the Summary Table.

Figure 5-537. BUCK1_TRIM_REG_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vref_dac_1				
R/W-0b			R/W-0b				

Table 5-509. BUCK1_TRIM_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vref_dac_1	R/W	0b	Trim reference DAC gain

ADVANCE INFORMATION

5.7.1.471 BUCK1_TRIM_REG_1 Register (Offset = 0x261) [reset = 0x0]

BUCK1_TRIM_REG_1 is shown in Figure 5-538 and described in Table 5-510.

Return to the Summary Table.

Figure 5-538. BUCK1_TRIM_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_level_shift_gain_1				
R/W-0b			R/W-0b				

Table 5-510. BUCK1_TRIM_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_level_shift_gain_1	R/W	0b	Trim level shifter gain (part of output voltage programming)

5.7.1.472 BUCK1_TRIM_REG_2 Register (Offset = 0x262) [reset = 0x0]

BUCK1_TRIM_REG_2 is shown in Figure 5-539 and described in Table 5-511.

Return to the Summary Table.

Figure 5-539. BUCK1_TRIM_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_loop_comp_1				
R/W-0b			R/W-0b				

Table 5-511. BUCK1_TRIM_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_loop_comp_1	R/W	0b	Trim loop comparator offset

ADVANCE INFORMATION

5.7.1.473 BUCK1_TRIM_REG_3 Register (Offset = 0x263) [reset = 0x0]

BUCK1_TRIM_REG_3 is shown in Figure 5-540 and described in Table 5-512.

Return to the Summary Table.

Figure 5-540. BUCK1_TRIM_REG_3 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_gain_1		
R/W-0b					R/W-0b		

Table 5-512. BUCK1_TRIM_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_gain_1	R/W	0b	Trim VOUT_ADC gain

5.7.1.474 BUCK1_TRIM_REG_4 Register (Offset = 0x264) [reset = 0x0]

BUCK1_TRIM_REG_4 is shown in Figure 5-541 and described in Table 5-513.

Return to the Summary Table.

Figure 5-541. BUCK1_TRIM_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED				trim_vout_adc_offset_1			
R/W-0b				R/W-0b			

Table 5-513. BUCK1_TRIM_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_vout_adc_offset_1	R/W	0b	Trim VOUT_ADC offset

ADVANCE INFORMATION

5.7.1.475 BUCK1_TRIM_REG_5 Register (Offset = 0x265) [reset = 0x0]

BUCK1_TRIM_REG_5 is shown in Figure 5-542 and described in Table 5-514.

Return to the Summary Table.

Figure 5-542. BUCK1_TRIM_REG_5 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_ptat_1		
R/W-0b					R/W-0b		

Table 5-514. BUCK1_TRIM_REG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_ptat_1	R/W	0b	Trim VOUT_ADC bias current

5.7.1.476 BUCK1_TRIM_REG_6 Register (Offset = 0x266) [reset = 0x0]

BUCK1_TRIM_REG_6 is shown in Figure 5-543 and described in Table 5-515.

Return to the Summary Table.

Figure 5-543. BUCK1_TRIM_REG_6 Register

7	6	5	4	3	2	1	0
RESERVED				trim_emu_ramp_1			
R/W-0b				R/W-0b			

Table 5-515. BUCK1_TRIM_REG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_emu_ramp_1	R/W	0b	Trim emulated ramp amplitude

ADVANCE INFORMATION

5.7.1.477 BUCK1_TRIM_REG_7 Register (Offset = 0x267) [reset = 0x0]

BUCK1_TRIM_REG_7 is shown in Figure 5-544 and described in Table 5-516.

Return to the Summary Table.

Figure 5-544. BUCK1_TRIM_REG_7 Register

7	6	5	4	3	2	1	0
RESERVED				trim_artif_ramp_1			
R/W-0b				R/W-0b			

Table 5-516. BUCK1_TRIM_REG_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_artif_ramp_1	R/W	0b	Trim artificial ramp amplitude

5.7.1.478 BUCK1_TRIM_REG_8 Register (Offset = 0x268) [reset = 0x0]

BUCK1_TRIM_REG_8 is shown in Figure 5-545 and described in Table 5-517.

Return to the Summary Table.

Figure 5-545. BUCK1_TRIM_REG_8 Register

7	6	5	4	3	2	1	0
RESERVED			trim_hs_replica_1				
R/W-0b			R/W-0b				

Table 5-517. BUCK1_TRIM_REG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_hs_replica_1	R/W	0b	Trim HS OCP reference level

ADVANCE INFORMATION

5.7.1.479 BUCK1_TRIM_REG_9 Register (Offset = 0x269) [reset = 0x0]

BUCK1_TRIM_REG_9 is shown in Figure 5-546 and described in Table 5-518.

Return to the Summary Table.

Figure 5-546. BUCK1_TRIM_REG_9 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ls_replica_1				
R/W-0b			R/W-0b				

Table 5-518. BUCK1_TRIM_REG_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ls_replica_1	R/W	0b	Trim LS OCP reference level

5.7.1.480 BUCK1_TRIM_REG_10 Register (Offset = 0x26A) [reset = 0x0]

BUCK1_TRIM_REG_10 is shown in Figure 5-547 and described in Table 5-519.

Return to the Summary Table.

Figure 5-547. BUCK1_TRIM_REG_10 Register

7	6	5	4	3	2	1	0
RESERVED				trim_fb_gain_stage_offset_1			
R/W-0b				R/W-0b			

Table 5-519. BUCK1_TRIM_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_fb_gain_stage_offset_1	R/W	0b	Offset trim for feedback amplifier

ADVANCE INFORMATION

5.7.1.481 BUCK1_TRIM_REG_11 Register (Offset = 0x26B) [reset = 0x0]

BUCK1_TRIM_REG_11 is shown in Figure 5-548 and described in Table 5-520.

Return to the Summary Table.

Figure 5-548. BUCK1_TRIM_REG_11 Register

7	6	5	4	3	2	1	0
RESERVED				trim_integ_dac_gain_1			
R/W-0b				R/W-0b			

Table 5-520. BUCK1_TRIM_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_integ_dac_gain_1	R/W	0b	Trim gain for integrator

ADVANCE INFORMATION

5.7.1.482 BUCK1_TRIM_REG_12 Register (Offset = 0x26C) [reset = 0x0]

BUCK1_TRIM_REG_12 is shown in Figure 5-549 and described in Table 5-521.

Return to the Summary Table.

Figure 5-549. BUCK1_TRIM_REG_12 Register

7	6	5	4	3	2	1	0
RESERVED				trim_slope_1			
R/W-0b				R/W-0b			

Table 5-521. BUCK1_TRIM_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_slope_1	R/W	0b	Trims Inductor dI/dt compensation. Improves current limit accuracy.

ADVANCE INFORMATION

5.7.1.483 BUCK1_TRIM_REG_13 Register (Offset = 0x26D) [reset = 0x0]

BUCK1_TRIM_REG_13 is shown in Figure 5-550 and described in Table 5-522.

Return to the Summary Table.

Figure 5-550. BUCK1_TRIM_REG_13 Register

7	6	5	4	3	2	1	0
RESERVED				trim_spare_1			
R/W-0b				R/W-0b			

Table 5-522. BUCK1_TRIM_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_spare_1	R/W	0b	

ADVANCE INFORMATION

5.7.1.484 BUCK2_TRIM_REG_0 Register (Offset = 0x280) [reset = 0x0]

BUCK2_TRIM_REG_0 is shown in Figure 5-551 and described in Table 5-523.

Return to the Summary Table.

Figure 5-551. BUCK2_TRIM_REG_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vref_dac_2				
R/W-0b			R/W-0b				

Table 5-523. BUCK2_TRIM_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vref_dac_2	R/W	0b	Trim reference DAC gain

ADVANCE INFORMATION

5.7.1.485 BUCK2_TRIM_REG_1 Register (Offset = 0x281) [reset = 0x0]

BUCK2_TRIM_REG_1 is shown in Figure 5-552 and described in Table 5-524.

Return to the Summary Table.

Figure 5-552. BUCK2_TRIM_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_level_shift_gain_2				
R/W-0b			R/W-0b				

Table 5-524. BUCK2_TRIM_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_level_shift_gain_2	R/W	0b	Trim level shifter gain (part of output voltage programming)

5.7.1.486 BUCK2_TRIM_REG_2 Register (Offset = 0x282) [reset = 0x0]

BUCK2_TRIM_REG_2 is shown in Figure 5-553 and described in Table 5-525.

Return to the Summary Table.

Figure 5-553. BUCK2_TRIM_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_loop_comp_2				
R/W-0b			R/W-0b				

Table 5-525. BUCK2_TRIM_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_loop_comp_2	R/W	0b	Trim loop comparator offset

ADVANCE INFORMATION

5.7.1.487 BUCK2_TRIM_REG_3 Register (Offset = 0x283) [reset = 0x0]

BUCK2_TRIM_REG_3 is shown in Figure 5-554 and described in Table 5-526.

Return to the Summary Table.

Figure 5-554. BUCK2_TRIM_REG_3 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_gain_2		
R/W-0b					R/W-0b		

Table 5-526. BUCK2_TRIM_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_gain_2	R/W	0b	Trim VOUT_ADC gain

5.7.1.488 BUCK2_TRIM_REG_4 Register (Offset = 0x284) [reset = 0x0]

BUCK2_TRIM_REG_4 is shown in Figure 5-555 and described in Table 5-527.

Return to the Summary Table.

Figure 5-555. BUCK2_TRIM_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED				trim_vout_adc_offset_2			
R/W-0b				R/W-0b			

Table 5-527. BUCK2_TRIM_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_vout_adc_offset_2	R/W	0b	Trim VOUT_ADC offset

ADVANCE INFORMATION

5.7.1.489 BUCK2_TRIM_REG_5 Register (Offset = 0x285) [reset = 0x0]

BUCK2_TRIM_REG_5 is shown in Figure 5-556 and described in Table 5-528.

Return to the Summary Table.

Figure 5-556. BUCK2_TRIM_REG_5 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_ptat_2		
R/W-0b					R/W-0b		

Table 5-528. BUCK2_TRIM_REG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_ptat_2	R/W	0b	Trim VOUT_ADC bias current

5.7.1.490 BUCK2_TRIM_REG_6 Register (Offset = 0x286) [reset = 0x0]

BUCK2_TRIM_REG_6 is shown in Figure 5-557 and described in Table 5-529.

Return to the Summary Table.

Figure 5-557. BUCK2_TRIM_REG_6 Register

7	6	5	4	3	2	1	0
RESERVED				trim_emu_ramp_2			
R/W-0b				R/W-0b			

Table 5-529. BUCK2_TRIM_REG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_emu_ramp_2	R/W	0b	Trim emulated ramp amplitude

ADVANCE INFORMATION

5.7.1.491 BUCK2_TRIM_REG_7 Register (Offset = 0x287) [reset = 0x0]

BUCK2_TRIM_REG_7 is shown in Figure 5-558 and described in Table 5-530.

Return to the Summary Table.

Figure 5-558. BUCK2_TRIM_REG_7 Register

7	6	5	4	3	2	1	0
RESERVED				trim_artif_ramp_2			
R/W-0b				R/W-0b			

Table 5-530. BUCK2_TRIM_REG_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_artif_ramp_2	R/W	0b	Trim artificial ramp amplitude

5.7.1.492 BUCK2_TRIM_REG_8 Register (Offset = 0x288) [reset = 0x0]

BUCK2_TRIM_REG_8 is shown in Figure 5-559 and described in Table 5-531.

Return to the Summary Table.

Figure 5-559. BUCK2_TRIM_REG_8 Register

7	6	5	4	3	2	1	0
RESERVED			trim_hs_replica_2				
R/W-0b			R/W-0b				

Table 5-531. BUCK2_TRIM_REG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_hs_replica_2	R/W	0b	Trim HS OCP reference level

ADVANCE INFORMATION

5.7.1.493 BUCK2_TRIM_REG_9 Register (Offset = 0x289) [reset = 0x0]

BUCK2_TRIM_REG_9 is shown in Figure 5-560 and described in Table 5-532.

Return to the Summary Table.

Figure 5-560. BUCK2_TRIM_REG_9 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ls_replica_2				
R/W-0b			R/W-0b				

Table 5-532. BUCK2_TRIM_REG_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ls_replica_2	R/W	0b	Trim LS OCP reference level

5.7.1.494 BUCK2_TRIM_REG_10 Register (Offset = 0x28A) [reset = 0x0]

BUCK2_TRIM_REG_10 is shown in Figure 5-561 and described in Table 5-533.

Return to the Summary Table.

Figure 5-561. BUCK2_TRIM_REG_10 Register

7	6	5	4	3	2	1	0
RESERVED				trim_fb_gain_stage_offset_2			
R/W-0b				R/W-0b			

Table 5-533. BUCK2_TRIM_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_fb_gain_stage_offset_2	R/W	0b	Offset trim for feedback amplifier

ADVANCE INFORMATION

5.7.1.495 BUCK2_TRIM_REG_11 Register (Offset = 0x28B) [reset = 0x0]

BUCK2_TRIM_REG_11 is shown in Figure 5-562 and described in Table 5-534.

Return to the Summary Table.

Figure 5-562. BUCK2_TRIM_REG_11 Register

7	6	5	4	3	2	1	0
RESERVED				trim_integ_dac_gain_2			
R/W-0b				R/W-0b			

Table 5-534. BUCK2_TRIM_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_integ_dac_gain_2	R/W	0b	Trim gain for integrator

5.7.1.496 BUCK2_TRIM_REG_12 Register (Offset = 0x28C) [reset = 0x0]

BUCK2_TRIM_REG_12 is shown in Figure 5-563 and described in Table 5-535.

Return to the Summary Table.

Figure 5-563. BUCK2_TRIM_REG_12 Register

7	6	5	4	3	2	1	0
RESERVED				trim_slope_2			
R/W-0b				R/W-0b			

Table 5-535. BUCK2_TRIM_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_slope_2	R/W	0b	Trims Inductor dI/dt compensation. Improves current limit accuracy.

ADVANCE INFORMATION

5.7.1.497 BUCK2_TRIM_REG_13 Register (Offset = 0x28D) [reset = 0x0]

BUCK2_TRIM_REG_13 is shown in Figure 5-564 and described in Table 5-536.

Return to the Summary Table.

Figure 5-564. BUCK2_TRIM_REG_13 Register

7	6	5	4	3	2	1	0
RESERVED				trim_spare_2			
R/W-0b				R/W-0b			

Table 5-536. BUCK2_TRIM_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_spare_2	R/W	0b	

ADVANCE INFORMATION

5.7.1.498 BUCK3_TRIM_REG_0 Register (Offset = 0x2A0) [reset = 0x0]

BUCK3_TRIM_REG_0 is shown in Figure 5-565 and described in Table 5-537.

Return to the Summary Table.

Figure 5-565. BUCK3_TRIM_REG_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vref_dac_3				
R/W-0b			R/W-0b				

Table 5-537. BUCK3_TRIM_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vref_dac_3	R/W	0b	Trim reference DAC gain

ADVANCE INFORMATION

5.7.1.499 BUCK3_TRIM_REG_1 Register (Offset = 0x2A1) [reset = 0x0]

BUCK3_TRIM_REG_1 is shown in Figure 5-566 and described in Table 5-538.

Return to the Summary Table.

Figure 5-566. BUCK3_TRIM_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_level_shift_gain_3				
R/W-0b			R/W-0b				

Table 5-538. BUCK3_TRIM_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_level_shift_gain_3	R/W	0b	Trim level shifter gain (part of output voltage programming)

5.7.1.500 BUCK3_TRIM_REG_2 Register (Offset = 0x2A2) [reset = 0x0]

BUCK3_TRIM_REG_2 is shown in Figure 5-567 and described in Table 5-539.

Return to the Summary Table.

Figure 5-567. BUCK3_TRIM_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_loop_comp_3				
R/W-0b			R/W-0b				

Table 5-539. BUCK3_TRIM_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_loop_comp_3	R/W	0b	Trim loop comparator offset

ADVANCE INFORMATION

5.7.1.501 BUCK3_TRIM_REG_3 Register (Offset = 0x2A3) [reset = 0x0]

BUCK3_TRIM_REG_3 is shown in Figure 5-568 and described in Table 5-540.

Return to the Summary Table.

Figure 5-568. BUCK3_TRIM_REG_3 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_gain_3		
R/W-0b					R/W-0b		

Table 5-540. BUCK3_TRIM_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_gain_3	R/W	0b	Trim VOUT_ADC gain

5.7.1.502 BUCK3_TRIM_REG_4 Register (Offset = 0x2A4) [reset = 0x0]

BUCK3_TRIM_REG_4 is shown in Figure 5-569 and described in Table 5-541.

Return to the Summary Table.

Figure 5-569. BUCK3_TRIM_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED				trim_vout_adc_offset_3			
R/W-0b				R/W-0b			

Table 5-541. BUCK3_TRIM_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_vout_adc_offset_3	R/W	0b	Trim VOUT_ADC offset

ADVANCE INFORMATION

5.7.1.503 BUCK3_TRIM_REG_5 Register (Offset = 0x2A5) [reset = 0x0]

BUCK3_TRIM_REG_5 is shown in Figure 5-570 and described in Table 5-542.

Return to the Summary Table.

Figure 5-570. BUCK3_TRIM_REG_5 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_ptat_3		
R/W-0b					R/W-0b		

Table 5-542. BUCK3_TRIM_REG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_ptat_3	R/W	0b	Trim VOUT_ADC bias current

ADVANCE INFORMATION

5.7.1.504 BUCK3_TRIM_REG_6 Register (Offset = 0x2A6) [reset = 0x0]

BUCK3_TRIM_REG_6 is shown in Figure 5-571 and described in Table 5-543.

Return to the Summary Table.

Figure 5-571. BUCK3_TRIM_REG_6 Register

7	6	5	4	3	2	1	0
RESERVED				trim_emu_ramp_3			
R/W-0b				R/W-0b			

Table 5-543. BUCK3_TRIM_REG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_emu_ramp_3	R/W	0b	Trim emulated ramp amplitude

ADVANCE INFORMATION

5.7.1.505 BUCK3_TRIM_REG_7 Register (Offset = 0x2A7) [reset = 0x0]

BUCK3_TRIM_REG_7 is shown in Figure 5-572 and described in Table 5-544.

Return to the Summary Table.

Figure 5-572. BUCK3_TRIM_REG_7 Register

7	6	5	4	3	2	1	0
RESERVED				trim_artif_ramp_3			
R/W-0b				R/W-0b			

Table 5-544. BUCK3_TRIM_REG_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_artif_ramp_3	R/W	0b	Trim artificial ramp amplitude

ADVANCE INFORMATION

5.7.1.506 BUCK3_TRIM_REG_8 Register (Offset = 0x2A8) [reset = 0x0]

BUCK3_TRIM_REG_8 is shown in Figure 5-573 and described in Table 5-545.

Return to the Summary Table.

Figure 5-573. BUCK3_TRIM_REG_8 Register

7	6	5	4	3	2	1	0
RESERVED			trim_hs_replica_3				
R/W-0b			R/W-0b				

Table 5-545. BUCK3_TRIM_REG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_hs_replica_3	R/W	0b	Trim HS OCP reference level

ADVANCE INFORMATION

5.7.1.507 BUCK3_TRIM_REG_9 Register (Offset = 0x2A9) [reset = 0x0]

BUCK3_TRIM_REG_9 is shown in Figure 5-574 and described in Table 5-546.

Return to the Summary Table.

Figure 5-574. BUCK3_TRIM_REG_9 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ls_replica_3				
R/W-0b			R/W-0b				

Table 5-546. BUCK3_TRIM_REG_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ls_replica_3	R/W	0b	Trim LS OCP reference level

5.7.1.508 BUCK3_TRIM_REG_10 Register (Offset = 0x2AA) [reset = 0x0]

BUCK3_TRIM_REG_10 is shown in Figure 5-575 and described in Table 5-547.

Return to the Summary Table.

Figure 5-575. BUCK3_TRIM_REG_10 Register

7	6	5	4	3	2	1	0
RESERVED				trim_fb_gain_stage_offset_3			
R/W-0b				R/W-0b			

Table 5-547. BUCK3_TRIM_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_fb_gain_stage_offset_3	R/W	0b	Offset trim for feedback amplifier

ADVANCE INFORMATION

5.7.1.509 BUCK3_TRIM_REG_11 Register (Offset = 0x2AB) [reset = 0x0]

BUCK3_TRIM_REG_11 is shown in Figure 5-576 and described in Table 5-548.

Return to the Summary Table.

Figure 5-576. BUCK3_TRIM_REG_11 Register

7	6	5	4	3	2	1	0
RESERVED				trim_integ_dac_gain_3			
R/W-0b				R/W-0b			

Table 5-548. BUCK3_TRIM_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_integ_dac_gain_3	R/W	0b	Trim gain for integrator

5.7.1.510 BUCK3_TRIM_REG_12 Register (Offset = 0x2AC) [reset = 0x0]

BUCK3_TRIM_REG_12 is shown in Figure 5-577 and described in Table 5-549.

Return to the Summary Table.

Figure 5-577. BUCK3_TRIM_REG_12 Register

7	6	5	4	3	2	1	0
RESERVED				trim_slope_3			
R/W-0b				R/W-0b			

Table 5-549. BUCK3_TRIM_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_slope_3	R/W	0b	Trims Inductor dI/dt compensation. Improves current limit accuracy.

ADVANCE INFORMATION

5.7.1.511 BUCK3_TRIM_REG_13 Register (Offset = 0x2AD) [reset = 0x0]

BUCK3_TRIM_REG_13 is shown in Figure 5-578 and described in Table 5-550.

Return to the Summary Table.

Figure 5-578. BUCK3_TRIM_REG_13 Register

7	6	5	4	3	2	1	0
RESERVED				trim_spare_3			
R/W-0b				R/W-0b			

Table 5-550. BUCK3_TRIM_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_spare_3	R/W	0b	

5.7.1.512 BUCK4_TRIM_REG_0 Register (Offset = 0x2C0) [reset = 0x0]

BUCK4_TRIM_REG_0 is shown in Figure 5-579 and described in Table 5-551.

Return to the Summary Table.

Figure 5-579. BUCK4_TRIM_REG_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vref_dac_4				
R/W-0b			R/W-0b				

Table 5-551. BUCK4_TRIM_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vref_dac_4	R/W	0b	Trim reference DAC gain

5.7.1.513 BUCK4_TRIM_REG_1 Register (Offset = 0x2C1) [reset = 0x0]

BUCK4_TRIM_REG_1 is shown in Figure 5-580 and described in Table 5-552.

Return to the Summary Table.

Figure 5-580. BUCK4_TRIM_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_level_shift_gain_4				
R/W-0b			R/W-0b				

Table 5-552. BUCK4_TRIM_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_level_shift_gain_4	R/W	0b	Trim level shifter gain (part of output voltage programming)

5.7.1.514 BUCK4_TRIM_REG_2 Register (Offset = 0x2C2) [reset = 0x0]

BUCK4_TRIM_REG_2 is shown in Figure 5-581 and described in Table 5-553.

Return to the Summary Table.

Figure 5-581. BUCK4_TRIM_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_loop_comp_4				
R/W-0b			R/W-0b				

Table 5-553. BUCK4_TRIM_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_loop_comp_4	R/W	0b	Trim loop comparator offset

ADVANCE INFORMATION

5.7.1.515 BUCK4_TRIM_REG_3 Register (Offset = 0x2C3) [reset = 0x0]

BUCK4_TRIM_REG_3 is shown in Figure 5-582 and described in Table 5-554.

Return to the Summary Table.

Figure 5-582. BUCK4_TRIM_REG_3 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_gain_4		
R/W-0b					R/W-0b		

Table 5-554. BUCK4_TRIM_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_gain_4	R/W	0b	Trim VOUT_ADC gain

ADVANCE INFORMATION

5.7.1.516 BUCK4_TRIM_REG_4 Register (Offset = 0x2C4) [reset = 0x0]

BUCK4_TRIM_REG_4 is shown in Figure 5-583 and described in Table 5-555.

Return to the Summary Table.

Figure 5-583. BUCK4_TRIM_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED				trim_vout_adc_offset_4			
R/W-0b				R/W-0b			

Table 5-555. BUCK4_TRIM_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_vout_adc_offset_4	R/W	0b	Trim VOUT_ADC offset

ADVANCE INFORMATION

5.7.1.517 BUCK4_TRIM_REG_5 Register (Offset = 0x2C5) [reset = 0x0]

BUCK4_TRIM_REG_5 is shown in Figure 5-584 and described in Table 5-556.

Return to the Summary Table.

Figure 5-584. BUCK4_TRIM_REG_5 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_ptat_4		
R/W-0b					R/W-0b		

Table 5-556. BUCK4_TRIM_REG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_ptat_4	R/W	0b	Trim VOUT_ADC bias current

ADVANCE INFORMATION

5.7.1.518 BUCK4_TRIM_REG_6 Register (Offset = 0x2C6) [reset = 0x0]

BUCK4_TRIM_REG_6 is shown in Figure 5-585 and described in Table 5-557.

Return to the Summary Table.

Figure 5-585. BUCK4_TRIM_REG_6 Register

7	6	5	4	3	2	1	0
RESERVED				trim_emu_ramp_4			
R/W-0b				R/W-0b			

Table 5-557. BUCK4_TRIM_REG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_emu_ramp_4	R/W	0b	Trim emulated ramp amplitude

ADVANCE INFORMATION

5.7.1.519 BUCK4_TRIM_REG_7 Register (Offset = 0x2C7) [reset = 0x0]

BUCK4_TRIM_REG_7 is shown in Figure 5-586 and described in Table 5-558.

Return to the Summary Table.

Figure 5-586. BUCK4_TRIM_REG_7 Register

7	6	5	4	3	2	1	0
RESERVED				trim_artif_ramp_4			
R/W-0b				R/W-0b			

Table 5-558. BUCK4_TRIM_REG_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_artif_ramp_4	R/W	0b	Trim artificial ramp amplitude

ADVANCE INFORMATION

5.7.1.520 BUCK4_TRIM_REG_8 Register (Offset = 0x2C8) [reset = 0x0]

BUCK4_TRIM_REG_8 is shown in Figure 5-587 and described in Table 5-559.

Return to the Summary Table.

Figure 5-587. BUCK4_TRIM_REG_8 Register

7	6	5	4	3	2	1	0
RESERVED			trim_hs_replica_4				
R/W-0b			R/W-0b				

Table 5-559. BUCK4_TRIM_REG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_hs_replica_4	R/W	0b	Trim HS OCP reference level

ADVANCE INFORMATION

5.7.1.521 BUCK4_TRIM_REG_9 Register (Offset = 0x2C9) [reset = 0x0]

BUCK4_TRIM_REG_9 is shown in Figure 5-588 and described in Table 5-560.

Return to the Summary Table.

Figure 5-588. BUCK4_TRIM_REG_9 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ls_replica_4				
R/W-0b			R/W-0b				

Table 5-560. BUCK4_TRIM_REG_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ls_replica_4	R/W	0b	Trim LS OCP reference level

5.7.1.522 BUCK4_TRIM_REG_10 Register (Offset = 0x2CA) [reset = 0x0]

BUCK4_TRIM_REG_10 is shown in Figure 5-589 and described in Table 5-561.

Return to the Summary Table.

Figure 5-589. BUCK4_TRIM_REG_10 Register

7	6	5	4	3	2	1	0
RESERVED				trim_fb_gain_stage_offset_4			
R/W-0b				R/W-0b			

Table 5-561. BUCK4_TRIM_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_fb_gain_stage_offset_4	R/W	0b	Offset trim for feedback amplifier

ADVANCE INFORMATION

5.7.1.523 BUCK4_TRIM_REG_11 Register (Offset = 0x2CB) [reset = 0x0]

BUCK4_TRIM_REG_11 is shown in Figure 5-590 and described in Table 5-562.

Return to the Summary Table.

Figure 5-590. BUCK4_TRIM_REG_11 Register

7	6	5	4	3	2	1	0
RESERVED				trim_integ_dac_gain_4			
R/W-0b				R/W-0b			

Table 5-562. BUCK4_TRIM_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_integ_dac_gain_4	R/W	0b	Trim gain for integrator

5.7.1.524 BUCK4_TRIM_REG_12 Register (Offset = 0x2CC) [reset = 0x0]

BUCK4_TRIM_REG_12 is shown in Figure 5-591 and described in Table 5-563.

Return to the Summary Table.

Figure 5-591. BUCK4_TRIM_REG_12 Register

7	6	5	4	3	2	1	0
RESERVED				trim_slope_4			
R/W-0b				R/W-0b			

Table 5-563. BUCK4_TRIM_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_slope_4	R/W	0b	Trims Inductor dI/dt compensation. Improves current limit accuracy.

ADVANCE INFORMATION

5.7.1.525 BUCK4_TRIM_REG_13 Register (Offset = 0x2CD) [reset = 0x0]

BUCK4_TRIM_REG_13 is shown in Figure 5-592 and described in Table 5-564.

Return to the Summary Table.

Figure 5-592. BUCK4_TRIM_REG_13 Register

7	6	5	4	3	2	1	0
RESERVED				trim_spare_4			
R/W-0b				R/W-0b			

Table 5-564. BUCK4_TRIM_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_spare_4	R/W	0b	

5.7.1.526 BUCK5_TRIM_REG_0 Register (Offset = 0x2E0) [reset = 0x0]

BUCK5_TRIM_REG_0 is shown in Figure 5-593 and described in Table 5-565.

Return to the Summary Table.

Figure 5-593. BUCK5_TRIM_REG_0 Register

7	6	5	4	3	2	1	0
RESERVED			trim_vref_dac_5				
R/W-0b			R/W-0b				

Table 5-565. BUCK5_TRIM_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_vref_dac_5	R/W	0b	Trim reference DAC gain

ADVANCE INFORMATION

5.7.1.527 BUCK5_TRIM_REG_1 Register (Offset = 0x2E1) [reset = 0x0]

BUCK5_TRIM_REG_1 is shown in Figure 5-594 and described in Table 5-566.

Return to the Summary Table.

Figure 5-594. BUCK5_TRIM_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED			trim_level_shift_gain_5				
R/W-0b			R/W-0b				

Table 5-566. BUCK5_TRIM_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_level_shift_gain_5	R/W	0b	Trim level shifter gain (part of output voltage programming)

5.7.1.528 BUCK5_TRIM_REG_2 Register (Offset = 0x2E2) [reset = 0x0]

BUCK5_TRIM_REG_2 is shown in Figure 5-595 and described in Table 5-567.

Return to the Summary Table.

Figure 5-595. BUCK5_TRIM_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			trim_loop_comp_5				
R/W-0b			R/W-0b				

Table 5-567. BUCK5_TRIM_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_loop_comp_5	R/W	0b	Trim loop comparator offset

ADVANCE INFORMATION

5.7.1.529 BUCK5_TRIM_REG_3 Register (Offset = 0x2E3) [reset = 0x0]

BUCK5_TRIM_REG_3 is shown in Figure 5-596 and described in Table 5-568.

Return to the Summary Table.

Figure 5-596. BUCK5_TRIM_REG_3 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_gain_5		
R/W-0b					R/W-0b		

Table 5-568. BUCK5_TRIM_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_gain_5	R/W	0b	Trim VOUT_ADC gain

5.7.1.530 BUCK5_TRIM_REG_4 Register (Offset = 0x2E4) [reset = 0x0]

BUCK5_TRIM_REG_4 is shown in Figure 5-597 and described in Table 5-569.

Return to the Summary Table.

Figure 5-597. BUCK5_TRIM_REG_4 Register

7	6	5	4	3	2	1	0
RESERVED				trim_vout_adc_offset_5			
R/W-0b				R/W-0b			

Table 5-569. BUCK5_TRIM_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_vout_adc_offset_5	R/W	0b	Trim VOUT_ADC offset

ADVANCE INFORMATION

5.7.1.531 BUCK5_TRIM_REG_5 Register (Offset = 0x2E5) [reset = 0x0]

BUCK5_TRIM_REG_5 is shown in Figure 5-598 and described in Table 5-570.

Return to the Summary Table.

Figure 5-598. BUCK5_TRIM_REG_5 Register

7	6	5	4	3	2	1	0
RESERVED					trim_vout_adc_ptat_5		
R/W-0b					R/W-0b		

Table 5-570. BUCK5_TRIM_REG_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2:0	trim_vout_adc_ptat_5	R/W	0b	Trim VOUT_ADC bias current

5.7.1.532 BUCK5_TRIM_REG_6 Register (Offset = 0x2E6) [reset = 0x0]

BUCK5_TRIM_REG_6 is shown in Figure 5-599 and described in Table 5-571.

Return to the Summary Table.

Figure 5-599. BUCK5_TRIM_REG_6 Register

7	6	5	4	3	2	1	0
RESERVED				trim_emu_ramp_5			
R/W-0b				R/W-0b			

Table 5-571. BUCK5_TRIM_REG_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_emu_ramp_5	R/W	0b	Trim emulated ramp amplitude

ADVANCE INFORMATION

5.7.1.533 BUCK5_TRIM_REG_7 Register (Offset = 0x2E7) [reset = 0x0]

BUCK5_TRIM_REG_7 is shown in Figure 5-600 and described in Table 5-572.

Return to the Summary Table.

Figure 5-600. BUCK5_TRIM_REG_7 Register

7	6	5	4	3	2	1	0
RESERVED				trim_artif_ramp_5			
R/W-0b				R/W-0b			

Table 5-572. BUCK5_TRIM_REG_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_artif_ramp_5	R/W	0b	Trim artificial ramp amplitude

5.7.1.534 BUCK5_TRIM_REG_8 Register (Offset = 0x2E8) [reset = 0x0]

BUCK5_TRIM_REG_8 is shown in Figure 5-601 and described in Table 5-573.

Return to the Summary Table.

Figure 5-601. BUCK5_TRIM_REG_8 Register

7	6	5	4	3	2	1	0
RESERVED			trim_hs_replica_5				
R/W-0b			R/W-0b				

Table 5-573. BUCK5_TRIM_REG_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_hs_replica_5	R/W	0b	Trim HS OCP reference level

ADVANCE INFORMATION

5.7.1.535 BUCK5_TRIM_REG_9 Register (Offset = 0x2E9) [reset = 0x0]

BUCK5_TRIM_REG_9 is shown in Figure 5-602 and described in Table 5-574.

Return to the Summary Table.

Figure 5-602. BUCK5_TRIM_REG_9 Register

7	6	5	4	3	2	1	0
RESERVED			trim_ls_replica_5				
R/W-0b			R/W-0b				

Table 5-574. BUCK5_TRIM_REG_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b	
4:0	trim_ls_replica_5	R/W	0b	Trim LS OCP reference level

5.7.1.536 BUCK5_TRIM_REG_10 Register (Offset = 0x2EA) [reset = 0x0]

BUCK5_TRIM_REG_10 is shown in Figure 5-603 and described in Table 5-575.

Return to the Summary Table.

Figure 5-603. BUCK5_TRIM_REG_10 Register

7	6	5	4	3	2	1	0
RESERVED				trim_fb_gain_stage_offset_5			
R/W-0b				R/W-0b			

Table 5-575. BUCK5_TRIM_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_fb_gain_stage_offset_5	R/W	0b	Offset trim for feedback amplifier

ADVANCE INFORMATION

5.7.1.537 BUCK5_TRIM_REG_11 Register (Offset = 0x2EB) [reset = 0x0]

BUCK5_TRIM_REG_11 is shown in Figure 5-604 and described in Table 5-576.

Return to the Summary Table.

Figure 5-604. BUCK5_TRIM_REG_11 Register

7	6	5	4	3	2	1	0
RESERVED				trim_integ_dac_gain_5			
R/W-0b				R/W-0b			

Table 5-576. BUCK5_TRIM_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_integ_dac_gain_5	R/W	0b	Trim gain for integrator

5.7.1.538 BUCK5_TRIM_REG_12 Register (Offset = 0x2EC) [reset = 0x0]

BUCK5_TRIM_REG_12 is shown in Figure 5-605 and described in Table 5-577.

Return to the Summary Table.

Figure 5-605. BUCK5_TRIM_REG_12 Register

7	6	5	4	3	2	1	0
RESERVED				trim_slope_5			
R/W-0b				R/W-0b			

Table 5-577. BUCK5_TRIM_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_slope_5	R/W	0b	Trims Inductor dI/dt compensation. Improves current limit accuracy.

ADVANCE INFORMATION

5.7.1.539 BUCK5_TRIM_REG_13 Register (Offset = 0x2ED) [reset = 0x0]

BUCK5_TRIM_REG_13 is shown in Figure 5-606 and described in Table 5-578.

Return to the Summary Table.

Figure 5-606. BUCK5_TRIM_REG_13 Register

7	6	5	4	3	2	1	0
RESERVED				trim_spare_5			
R/W-0b				R/W-0b			

Table 5-578. BUCK5_TRIM_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b	
3:0	trim_spare_5	R/W	0b	

5.7.1.540 WD_ANSWER_REG Register (Offset = 0x401) [reset = 0x0]

WD_ANSWER_REG is shown in Figure 5-607 and described in Table 5-579.

Return to the Summary Table.

Figure 5-607. WD_ANSWER_REG Register

7	6	5	4	3	2	1	0
WD_ANSWER							
R/W-0b							

Table 5-579. WD_ANSWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WD_ANSWER	R/W	0b	MCU answer byte. The MCU must write the expected reference Answer-x into this register. Each watchdog question requires four answer bytes: - Three answer bytes (Answer-3, Answer-2, Answer-1) must be written in Window-1. - The fourth (final) answer-byte (Answer-0) must be written in Window-2. The number of written answer bytes is tracked with the WD_ANSW_CNT counter in the WD_QUESTION_ANSW_CNT register. These bits only apply for Watchdog in Q&A mode.

5.7.1.541 WD_QUESTION_ANSW_CNT Register (Offset = 0x402) [reset = 0x30]

WD_QUESTION_ANSW_CNT is shown in Figure 5-608 and described in Table 5-580.

Return to the Summary Table.

Figure 5-608. WD_QUESTION_ANSW_CNT Register

7	6	5	4	3	2	1	0
RESERVED		WD_ANSW_CNT		WD_QUESTION			
R-0b		R-11b		R-0b			

Table 5-580. WD_QUESTION_ANSW_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0b	
5:4	WD_ANSW_CNT	R	11b	Current, received watchdog-answer count state. These bits only apply for Watchdog in Q&A mode.
3:0	WD_QUESTION	R	0b	Watchdog question. The MCU must read (or calculate) the current watchdog question value to generate correct answers. These bits only apply for Watchdog in Q&A mode.

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5.7.1.542 WD_WIN1_CFG Register (Offset = 0x403) [reset = 0x7F]

WD_WIN1_CFG is shown in Figure 5-609 and described in Table 5-581.

Return to the Summary Table.

Figure 5-609. WD_WIN1_CFG Register

7	6	5	4	3	2	1	0
RESERVED	WD_WIN1						
R/W-0b	R/W-1111111b						

Table 5-581. WD_WIN1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	WD_WIN1	R/W	1111111b	These bits are for programming the duration of Watchdog Window-1 (see Watchdoc chapter). These bits can be only be written when the watchdog is in the Long Window.

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5.7.1.543 WD_WIN2_CFG Register (Offset = 0x404) [reset = 0x7F]

WD_WIN2_CFG is shown in Figure 5-610 and described in Table 5-582.

Return to the Summary Table.

Figure 5-610. WD_WIN2_CFG Register

7	6	5	4	3	2	1	0
RESERVED	WD_WIN2						
R/W-0b	R/W-1111111b						

Table 5-582. WD_WIN2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6:0	WD_WIN2	R/W	1111111b	These bits are for programming the duration of Watchdog Window-2 (see Watchdog chapter). These bits can be only be written when the watchdog is in the Long Window.

5.7.1.544 WD_LONGWIN_CFG Register (Offset = 0x405) [reset = 0xFF]

WD_LONGWIN_CFG is shown in Figure 5-611 and described in Table 5-583.

Return to the Summary Table.

Figure 5-611. WD_LONGWIN_CFG Register

7	6	5	4	3	2	1	0
WD_LONGWIN							
R/W-11111111b							

Table 5-583. WD_LONGWIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WD_LONGWIN	R/W	11111111b	These bits are for programming the duration of Watchdog Long Window (see Watchdog chapter). These bits can be only be written when the watchdog is in the Long Window.

5.7.1.545 WD_MODE_REG Register (Offset = 0x406) [reset = 0x2]

WD_MODE_REG is shown in Figure 5-612 and described in Table 5-584.

Return to the Summary Table.

Figure 5-612. WD_MODE_REG Register

7	6	5	4	3	2	1	0
RESERVED					WD_PWRHOLD	WD_MODE_SELECT	WD_RETURN_LONGWIN
R/W-0b					R/W-0b	R/W-1b	R/W-0b

Table 5-584. WD_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b	
2	WD_PWRHOLD	R/W	0b	Device sets WD_PWRHOLD if hardware condition on pin DISABLE_WDOG (mapped to GPIO8 pin) is applied at startup (see Watchdog chapter). MCU can write this bit to 1. MCU needs to clear this bit to get out of the Long Window: 0b = watchdog goes out of the Long Window and starts the first watchdog-sequence when the configured Long Window time-interval elapses 1b = watchdog stays in Long Window
1	WD_MODE_SELECT	R/W	1b	Watchdog mode-select: MCU can set this to required value only when watchdog is in the Long Window. 0b = Trigger Mode 1b = Q&A mode.
0	WD_RETURN_LONGWIN	R/W	0b	MCU can set this bit to put the watchdog from operating back to the Long Window (see Watchdog chapter): 0b = Watchdog continues operating 1b = Watchdog returns to Long-Window after completion of the current watchdog-sequence.

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5.7.1.546 WD_QA_CFG Register (Offset = 0x407) [reset = 0xA]

WD_QA_CFG is shown in Figure 5-613 and described in Table 5-585.

Return to the Summary Table.

Figure 5-613. WD_QA_CFG Register

7	6	5	4	3	2	1	0
WD_QA_FDBK		WD_QA_LFSR		WD_QUESTION_SEED			
R/W-0b		R/W-0b		R/W-1010b			

Table 5-585. WD_QA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	WD_QA_FDBK	R/W	0b	Feedback configuration bits for the watchdog question. These bits control the sequence of the generated questions and respective reference answers (see Watchdog chapter). These bits are only used for the watchdog in Q&A mode. These bits can be only be written when the watchdog is in the Long Window.
5:4	WD_QA_LFSR	R/W	0b	LFSR-equation configuration bits for the watchdog question (see Watchdog chapter). These bits are only used for the watchdog in Q&A mode. These bits can be only be written when the watchdog is in the Long Window.
3:0	WD_QUESTION_SEED	R/W	1010b	The watchdog question-seed value (see Watchdog chapter). The MCU updates the question-seed value to generate a set of new questions. These bits can be only be written when the watchdog is in the Long Window.

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5.7.1.547 WD_ERR_STATUS Register (Offset = 0x408) [reset = 0x0]

WD_ERR_STATUS is shown in Figure 5-614 and described in Table 5-586.

Return to the Summary Table.

Figure 5-614. WD_ERR_STATUS Register

7	6	5	4	3	2	1	0
WD_RST_INT	WD_FAIL_INT	WD_ANSW_ERR	WD_SEQ_ERR	WD_ANSW_EARLY	WD_TRIG_EARLY	WD_TIMEOUT	WD_LONGWIN_TIMEOUT_INT
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 5-586. WD_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_RST_INT	R/W1C	0b	Latched status bit to indicate that the device went through warm reset due to WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]). Write 1 to clear.
6	WD_FAIL_INT	R/W1C	0b	Latched status bit to indicate that the watchdog has cleared the ENABLE_DRV bit due to WD_FAIL_CNT[3:0] > WD_FAIL_TH[2:0]. Write 1 to clear.
5	WD_ANSW_ERR	R/W1C	0b	Latched status bit to indicate that the watchdog has detected an incorrect answer-byte. Write 1 to clear. This bit only applies for Watchdog in Q&A mode.
4	WD_SEQ_ERR	R/W1C	0b	Latched status bit to indicate that the watchdog has detected an incorrect sequence of the answer-bytes. Write 1 to clear. This bit only applies for Watchdog in Q&A mode.
3	WD_ANSW_EARLY	R/W1C	0b	Latched status bit to indicate that the watchdog has received the final answer-byte in Window-1. Write 1 to clear. This bit only applies for Watchdog in Q&A mode.
2	WD_TRIG_EARLY	R/W1C	0b	Latched status bit to indicate that the watchdog has received the watchdog-trigger in Window-1. Write 1 to clear. This bit only applies for Watchdog in Trigger mode.
1	WD_TIMEOUT	R/W1C	0b	Latched status bit to indicate that the watchdog has detected a time-out event in the started watchdog sequence. Write 1 to clear.
0	WD_LONGWIN_TIMEOUT_INT	R/W1C	0b	Latched status bit to indicate that device went through warm reset due to elapse of Long Window time-interval. Write 1 to clear interrupt.

5.7.1.548 WD_THR_CFG Register (Offset = 0x409) [reset = 0xFF]

WD_THR_CFG is shown in Figure 5-615 and described in Table 5-587.

Return to the Summary Table.

Figure 5-615. WD_THR_CFG Register

7	6	5	4	3	2	1	0
WD_RST_EN	WD_EN	WD_FAIL_TH			WD_RST_TH		
R/W-1b	R/W-1b	R/W-111b			R/W-111b		

Table 5-587. WD_THR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_RST_EN	R/W	1b	Watchdog reset configuration bit: This bit can be only be written when the watchdog is in the Long Window. 0b = No warm reset when WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]) 1b = Warm reset when WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]).
6	WD_EN	R/W	1b	Watchdog enable configuration bit: This bit can be only be written when the watchdog is in the Long Window. 0b = watchdog disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt status bits are cleared 1b = watchdog enabled. MCU can set ENABLE_DRV bit to 1 if: - watchdog is out of the Long Window - WD_FAIL_CNT[3:0] =< WD_FAIL_TH[2:0] - WD_FIRST_OK=1 - all other interrupt status bits are cleared.
5:3	WD_FAIL_TH	R/W	111b	Configuration bits for the 1st threshold of the watchdog fail counter: Device clears ENABLE_DRV bit when WD_FAIL_CNT[3:0] > WD_FAIL_TH[2:0]. These bits can be only be written when the watchdog is in the Long Window.
2:0	WD_RST_TH	R/W	111b	Configuration bits for the 2nd threshold of the watchdog fail counter: Device goes through warm reset when WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]). These bits can be only be written when the watchdog is in the Long Window.

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5.7.1.549 WD_FAIL_CNT_REG Register (Offset = 0x40A) [reset = 0x20]

WD_FAIL_CNT_REG is shown in Figure 5-616 and described in Table 5-588.

Return to the Summary Table.

Figure 5-616. WD_FAIL_CNT_REG Register

7	6	5	4	3	2	1	0
RESERVED	WD_BAD_EVENT	WD_FIRST_OK	RESERVED	WD_FAIL_CNT			
R-0b	R-0b	R-1b	R-0b	R-0b			

Table 5-588. WD_FAIL_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	
6	WD_BAD_EVENT	R	0b	Status bit to indicate that the watchdog has detected a bad event in the current watchdog sequence. The device clears this bit at the end of the watchdog sequence.
5	WD_FIRST_OK	R	1b	Status bit to indicate that the watchdog has detected a good event. The device clears this bit when the watchdog goes to the Long Window.
4	RESERVED	R	0b	
3:0	WD_FAIL_CNT	R	0b	Status bits to indicate the value of the Watchdog Fail Counter. The device clears these bits when the watchdog goes to the Long Window.

6 Applications, Implementation, and Layout Sections

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The following sections will provide more detail on the proper utilization of the PMIC. Each orderable part number has unique default non-volatile memory settings and the relevant User's Guide for that orderable are available in the product folder. Reference these User's Guides for specific application information. More generic topics and some examples are outlined here.

To help with new designs, a variety of tools and documents are available in the product folder. Some examples are:

- Evaluation module and User Guide which allow testing of various orderable part numbers, including multi-PMIC operation
- GUI to communicate with the PMIC
- Schematic and layout checklist

Periodically, new tools and documents will be added to aid in new designs.

6.2 Typical Application

The PMIC is generally used to power a processor. The number of regulators needed, the required sequencing, the load current requirements, and the voltage characteristics are all critical in determining the number of PMICs used in the system as well as the external components used with it. The following section provides a generic case. For specific cases, refer to the relevant User's Guide based on the orderable part number.

6.2.1 Powering a Processor

In this example, a single PMIC is used to power a generic processor. For this case, the PMIC is used in 2+1+1+1 buck phase configuration where BUCK1 and BUCK2 are used in parallel to supply higher currents.

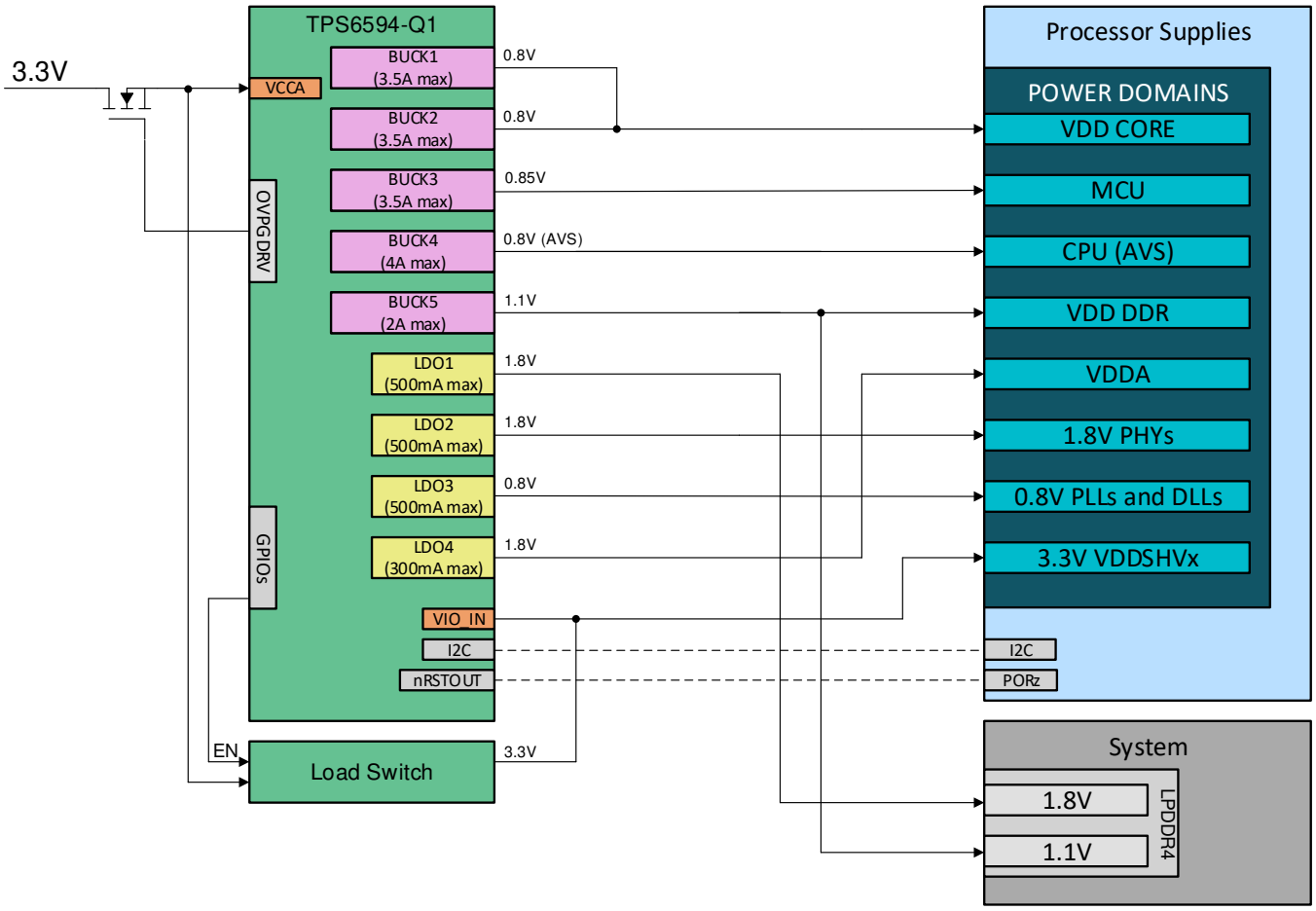

Figure 6-1. Example Power Map

6.2.1.1 Design Requirements

The design requirements for the sample processor in Figure 6-1 are outlined below:

- VDD CORE rail requires 0.8 V, 5 A
- MCU rail requires 0.85 V, 2 A
- CPU (AVS) rail requires 0.8 V, 3 A and the ability to support Adaptive Voltage Scaling
- LPDDR4 is used, which requires 1.1 V, 1 A and 1.8 V, 200 mA
- 1.8V PHYs and 0.8V PLLs and DLLs which are noise sensitive
- VDDA supplies the processor's most noise sensitive components, requires 100 mA, and requires extra low noise
- Protection from 3.3 V overvoltage (functional safety variant only)

6.2.1.2 Detailed Design Procedure

Based on the above requirements, the PMIC was configured with the connections outlined in Figure 6-1. BUCK1 and BUCK2 are used in multiphase operation to support the 5 A current. LDO2 and LDO3 are used to power 1.8 V PHYs and 0.8 V PLLs and DLLs because they are lower noise than a buck regulator and it isolates them from the noise of VDD CORE and the LPDDR4 1.8 V supply. LDO4 was used to power VDDA because it is has even better noise performance.

Using this configuration information, components can be chosen to use with the PMIC.

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6.2.1.2.1 VCCA, VSYS_SENSE, and OVPGDRV

The VCCA pin provides power to LDOVINT and other internal functions. It is always connected in parallel with the buck input pins (PVIN_Bx pins). The VSYS_SENSE pin and OVPGDRV pin protect the device from being damaged by an overvoltage event from the pre-regulator by disconnecting the low voltage VCCA-powered pins from VSYS. The VCCA pin can be connected to an optional 0.47-µF bypass capacitor close to the pin. For cases where the pre-regulator is not located near the device, place some additional bulk capacitance before the protection FET to stabilize the VSYS supply near the device.

For the input protection, total capacitance on the VSYS node must guarantee that VCCA does not rise above 8 V before the PMIC disables the protection FET in case of pre-regulator high side FET short failure. The maximum time specification is 15 µs, which leads to a maximum average slew rate of 133 mV / µs in the 6 V to 8 V range. The capacitance varies based on the pre-regulator inductor and the pre-regulator input filter and it is recommended to simulate this circuit to get an initial estimate on the required capacitance.

Choose a Zener diode with a breakdown voltage less than the recommended max of the VSYS_SENSE pin (12 V max) and greater than the overvoltage detection voltage (VSYS_OVP_Rising of 6.2 V) at all times for proper protection. Choose the protection resistors values to guarantee that the voltage across the Zener diode remains within those two boundaries and that the current is not greater than the Zener diode max current for the full desired input voltage protection range. For increased reliability, two resistors with 90° physical orientation offset are recommended to reduce risk of a single point short resulting in IC damage.

Finally, choose the protection NMOS FET with sufficient current and voltage ratings for the application with minimal gate charge values. The turn-on and turn-off time of the protection FET is generally very fast relative to the detection time, so gate charge is not as critical as R_{DSON} in general. The components chosen for the evaluation module to cover a broad set of applications are shown in Table 6-1. To determine the required minimum FET $R_{DS(ON)}$, the maximum input current is first measured or calculated based on output current requirements multiplied by the duty cycle (V_{OUT} / V_{IN}) and then divided by the buck efficiency. Next, determine the $VCCA_{UV\_TH}$ from the VCCA_PG_WINDOW.VCCA_UV_THR register setting. The $R_{DS(ON)}$ maximum must be less than the $VCCA_{UV\_TH}$ minimum divided by the input current maximum to ensure that VCCA does not drop below $VCCA_{UV\_TH}$ at maximum loading. From there, the second factor to consider is to minimize the Q_{GS} for faster FET turn off time.

For cases where input voltage protection is not required, float VSYS_SENSE and OVPGDRV and the protection diode and FET are not needed.

Table 6-1. Recommended VCCA, VSYS_SENSE, and OVPGDRV Components

Component	MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
Capacitor	Murata	GCM155C71A474KE36	0.47 µF, 10 V, X7R	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B3X7S1A474K050BB	0.47 µF, 10 V, X7R	0402	1.0 x 0.5	-
Zener Diode	ON Semiconductor	MM3Z10VST1G	10 V, 300 mW	SOD-323	2.5 x 1.25 x 0.9	Yes
Zener Diode	Vishay-Dale	BZX84B10-G3-08	10 V, 300 mW	SOT-23-3	3.1 x 2.6 x 1.15	-
Resistor(1)	Vishay-Dale	CRCW0402240RJNED	240 Ω	0402	1.0 x 0.5	Yes
NMOS FET	On Semiconductor	NVMFS4C05N	30 V, 4.0 mΩ, 127 A	-	5.15 x 6.15 x 1.0	Yes
NMOS FET	Diodes Incorporated	DMNH3010LK3	30 V, 11.5 mΩ, 50 A	-	6.70 x 10.41 x 2.39	-

(1) Two resistors are used in series to create an effective 480 Ω total resistance

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6.2.1.2.2 Internal LDOs

The internal LDOs, VOUT_LDOVINT and VOUT_LDOVRTC, require external 2.2 µF capacitors for stabilization. The recommended components are shown below.

Table 6-2. Recommended Internal LDO Components

Component	MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
Capacitor	Murata	GCM188R70J225KE22	2.2 µF, 6.3V, X7R	0603	1.6 x 0.8	-
Capacitor	TDK	CGA3E1X7S1C225M080AC	2.2 µF, 6.3 V, X7R	0603	1.6 x 0.8	-

6.2.1.2.3 Crystal Oscillator

A crystal oscillator can be used for application requiring a high accuracy real-time clock module. The OSC32KCAP pin is bypassed with a 100-nF bypass capacitor for noise rejection. For the OSC32KIN and OSC32KOUT pins, a simplified oscillator schematic is shown in Figure 6-2 to determine what external load capacitors are needed for the crystal.

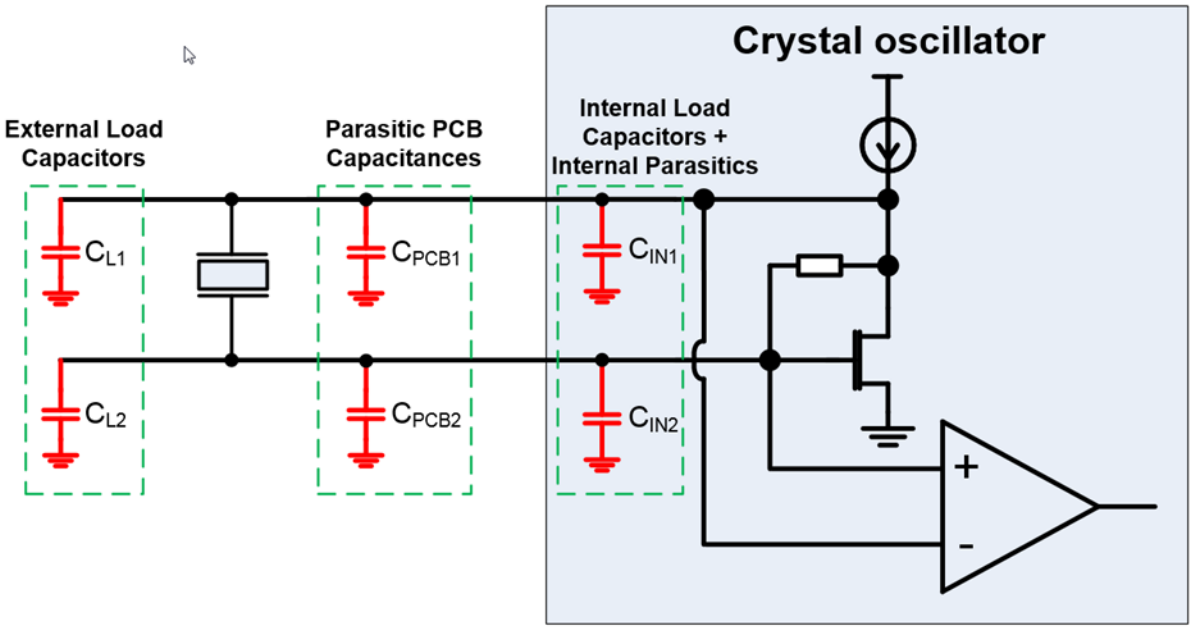

Figure 6-2. Crystal Oscillator Component Selection

C_{IN1} and C_{IN2} are both 12 pF for this device. C_{PCB1} and C_{PCB2} will depend on the board but is generally around 1 pF. The crystal oscillator chosen should have a required load capacitance of either 6 pF, 9 pF, or 12.5 pF and the value of the XTAL_SEL bit in the RTC_CTRL_2 register should be updated based on the oscillator chosen. To achieve the required load capacitance (C_L) for the oscillator, Equation 26 is used. It assumes that the crystal series capacitance is negligible.

$$C_L = (C_{L1} + C_{PCB1} + C_{IN1}) \times (C_{L2} + C_{PCB2} + C_{IN2}) / ((C_{L1} + C_{PCB1} + C_{IN1}) + (C_{L2} + C_{PCB2} + C_{IN2})) \quad (26)$$

Assuming $C_{L1} = C_{L2}$, this simplifies to $C_{L1} = 2 \times C_L - C_{PCB} - C_{IN}$. Simplifying this into the standard capacitor values typically available results in the following general capacitor recommendations. If more precise matching is desired, complete the exercise without series capacitance neglected and with exact PCB parasitic capacitance. Too much capacitance will result in the oscillator frequency being lower than expected, while not enough capacitance has the opposite impact.

ADVANCE INFORMATION

Table 6-3. Approximate Crystal Oscillator Load Capacitors

Crystal C_L (pF)	Component $C_{L1} = C_{L2}$ (pF)
6	0
9	6
12.5	12.5

The recommended components using a 9 pF oscillator as an example are in Table 6-4. If an alternate load capacitance crystal is used, the values of the load capacitors should be adjusted to match based on the above.

Table 6-4. Recommended Crystal Oscillator Components for 9 pF Crystal

Component	MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
Capacitor	Murata	GCM155R71C104JA55D	100 nF, 16 V, X7R	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B1X7R1C104K050BC	100 nF, 16 V, X7R	0402	1.0 x 0.5	-
Crystal	NDK	NX3215SD-32.768K-STD-MUS-6	32.768 kHz, ±20 ppm, 9 pF		3.2 x 1.5 x 0.9	Yes
Crystal	Abracon	ABS07AIG-32.768kHz-9-T	32.768 kHz, ±20 ppm, 9 pF		3.2 x 1.5 x 0.9	-
Capacitor	Murata	GCM1555C1H6R0CA16	6 pF, 50 V, C0G/NP0	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B2C0G1H060D050BA	6 pF, 50 V, C0G/NP0	0402	1.0 x 0.5	-

ADVANCE INFORMATION

6.2.1.2.4 Buck Input Capacitors

For optimal performance, every buck needs an input capacitor, and the capacitor should be at least 10 µF, 10 V and shall be placed as close to the buck input pins as possible. If the board size allows a larger foot print, a 22 µF, 10 V capacitor is recommended. See Table 6-5 for the recommended input capacitors, and the Section 6.2.1.4 for more information about component placement.

Table 6-5. Recommended Buck Input Capacitors(1)

MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
TDK	CGA4J1X7S1C106K125AC	10 µF, 16 V, X7R	0805	2.0 × 1.25 × 1.25	Yes
Murata	GCM21BR71A106KE22	10 µF, 10 V, X7R	0805	2.0 × 1.25 × 1.25	-

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.

6.2.1.2.5 Buck Output Capacitors

The buck converters have seven potential NVM configurations which can impact the output capacitor selection. Refer the part number specific User's Guide to identify which configuration applies to each buck regulator. The actual minimal capacitance requirements to achieve a specific accuracy or ripple target will vary depending on the input voltage, output voltage, and load transient characteristics, however some guidance is provided below. The local output capacitors shall be placed as close to the inductor as possible to minimize electromagnetic emissions. Every buck output requires a local output capacitor to form the capacitive part of the LC output filter. It is recommended to place all large capacitors near the inductor. See Section 6.2.1.4 for more information about component placement.

To achieve better ripple and transient performance, additional high pass filter caps are recommended to compensate for the parasitic impedances due to board routing and provide faster transient response to a load step. These caps are placed close to the point of load and are also the input capacitors of the load. These capacitors are referred to as POL caps later in this document. POL capacitor usage will vary based on the application and generally follows the SoC or FPGA input capacitor requirements. Low ESL 3-terminal caps are recommended, as their high performance can help reduce the total number of capacitors required which simplifies board layout design and saves board area. They also help to reduce the total cost of the solution.

Figure 6-3 is an example power distribution network (PDN) of local and POL caps at the output of a buck for optimal ripple and transient performance. Table 6-6 lists the local and POL capacitors used to validate the buck transient and ripple performance specified in the parametric table for each of the seven configurations. Table 6-7 lists the actual capacitor part numbers used for the different use case tests, neglecting capacitors below 10 µF. It is recommended to simulate and validate that the capacitor network chosen for a particular design meets the desired requirements as these are provided as guidelines.

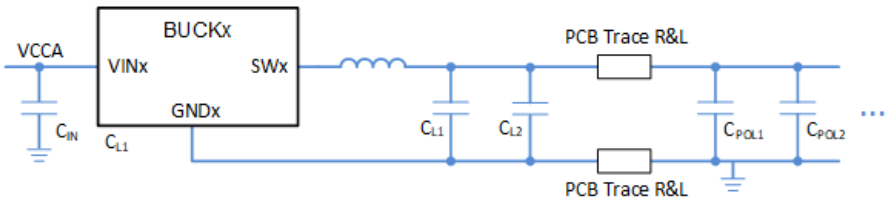

Figure 6-3. Example Power Distribution Network (PDN) of Local and POL Capacitors

Table 6-6. Local and POL Capacitors used for Buck Use Case Validation

Configuration	C_{OUT}	L	C_{L1} / phase	C_{L2} (total)	C_{POL1} (total)
4.4 MHz V_{OUT} Less than 1.9 V, Multiphase or High C_{OUT} Single Phase	Low	220 nH	47 µF × 1		10 µF × 4
	High	220 nH	47 µF × 4		10 µF × 2
DDR VTT Termination, 4.4 MHz Single Phase Only	-	470 nH	22 µF × 1		10 µF × 2

ADVANCE INFORMATION

Table 6-6. Local and POL Capacitors used for Buck Use Case Validation (continued)

Configuration	C_{OUT}	L	C_{L1} / phase	C_{L2} (total)	C_{POL1} (total)
4.4 MHz V_{OUT} Less than 1.9 V, Low C_{OUT}, Single Phase Only	Low	220 nH	22 µF × 1		10 µF × 2
	High	220 nH	47 µF × 1		10 µF × 4
4.4 MHz V_{OUT} Greater than 1.7 V, Single Phase Only	Low	470 nH	47 µF × 1		10 µF × 4
	High	470 nH	47 µF × 2		10 µF × 2
2.2 MHz Full V_{OUT} Range and V_{IN} Greater than 4.5 V, Single Phase Only	Low	1000 nH	47 µF × 3		10 µF × 4
	High	1000 nH	47 µF × 3	680 µF × 1	10 µF × 4
2.2 MHz V_{OUT} Less than 1.9 V Multiphase or Single Phase	Low	470 nH	47 µF × 3		10 µF × 4
	High	470 nH	47 µF × 3	680 µF × 1	10 µF × 4
2.2 MHz Full V_{OUT} and Full V_{IN} Range, Single Phase Only	Low	1000 nH	47 µF × 3		10 µF × 2
	High	1000 nH	100 µF × 4		10 µF × 2

Table 6-7. Recommended Buck Converter Output Capacitor Components(1)

MANUFACTURER	PART NUMBER	VALUE	EIA Size Code	SIZE (mm)	Used for Validation
Murata	NFM15HC105D0G(2)	1 µF, 4 V, X7S	0402	1.0 × 0.5	Yes
TDK	YFF18AC0J105M(2)	1 µF, 6.3 V	0603	1.6 × 0.8	-
Murata	NFM18HC106D0G(2)	10 µF, 4 V, X7S	0603	1.6 × 0.8	Yes
TDK	YFF18AC0G475M(2)	4.7 µF, 6.3 V	0603	1.6 × 0.8	-
Murata	GCM31CR71A226KE02	22 µF, 10 V, X7R	1206	3.2 × 1.6	Yes
Murata	GCM21BD7CGA5L1X7R0J226M T0J226M	22 µF, 6.3 V, X7T	0805	2.0 × 1.25 × 1.25	-
TDK	CGA5L1X7R0J226MT	22 µF, 6.3 V, X7R	1206	3.2 × 1.6	-
TDK	CGA4J1X7T0J226MT	22 µF, 6.3 V, X7T	0805	2.0 × 1.25 × 1.25	-
Murata	GCM32ER70J476ME19	47 µF, 6.3 V, X7R	1210	3.2 × 2.5	Yes
Murata	GCM31CD70G476M	47 µF, 4 V, X7T	1206	3.2 × 1.6	-
TDK	CGA6P1X7S1A476MT	47 µF, 10 V, X7S	1210	3.2 × 2.5	-
TDK	CGA5L1X7T0G476MT	47 µF, 4 V, X7T	1206	3.2 × 1.6	-
Murata	GCM32ED70G107MEC4	100 µF, 4 V, X7S	1210	3.2 × 2.5	Yes
TDK	CGA6P1X7T0G107MT	100 µF, 4 V, X7T	1210	3.2 × 2.5	-
Kemet	T510X687K006ATA023(3)	680 µF, 6.3 V	2917	7.4 × 5.0	Yes

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.
(2) Low ESL 3-terminal cap
(3) Dependent on availability; may switch to 470 µF

ADVANCE INFORMATION

6.2.1.2.6 Buck Inductors

Inductor should be chosen based on the buck configuration. See Table 6-6 for the appropriate nominal inductance.

Recommended inductors based on these requirements are shown below.

Table 6-8. Recommended Buck Converter Inductors(1)

MANUFACTURER	PART NUMBER	VALUE	SIZE (mm)	Used for Validation
TDK	TFM322512ALMA1R0MTAA	1000 nH, 4 A Max, 150 °C	3.2 × 2.5 × 1.2	Yes
Murata	DFE322520FD-1R0M=P2	1000 nH, 4.1 A Max, 125 °C	3.2 x 2.5 x 2.0	-
TDK	TFM322512ALMAR47MTAA	470 nH, 5.3 A Max, 150 °C	3.2 × 2.5 × 1.2	Yes
TDK	TFM252012ALMAR47MTAA	470 nH, 4.9 A Max, 150 °C	2.5 x 2.0 x 1.2	-
Murata	DFE2HCAHR47MJ0	470 nH, 4.5 A Max, 150 °C	2.5 × 2.0 × 1.2	-
TDK	TFM322512ALMAR22MTAA	220 nH, 7.6 A Max, 150 °C	3.2 x 2.5 x 1.2	Yes

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.

Table 6-8. Recommended Buck Converter Inductors(1) (continued)

MANUFACTURER	PART NUMBER	VALUE	SIZE (mm)	Used for Validation
TDK	TFM201610ALMAR24MTAA	220 nH, 5 A Max, 150 °C	2.0 x 1.6 x 1.2	-
Murata	DFE2MCAHR24MJ0	240 nH, 4.2 A Max, 150 °C	2.0 x 1.6 x 1.2	-

6.2.1.2.7 LDO Input Capacitors

All LDO inputs require an input decoupling capacitor to minimize input ripple voltage. Using a 2.2-µF capacitor for each LDO is recommended. Depending on the input voltage of the LDO, a 6.3-V, 10-V, or 16-V capacitor can be used. For optimal performance, the input capacitors should be placed as close to the LDO input pins as possible. See the Section 6.2.1.4 for more information about component placement. See Table 6-9 for the recommended input capacitors.

Table 6-9. Recommended LDO Input Capacitors(1)

MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
TDK	CGA3E1X7S1C225M080AC	2.2 µF, 16 V, X7S	0603	1.6 x 0.8	Yes
Murata	GCM188R70J225KE22	2.2 µF, 16 V, X7R	0603	1.6 x 0.8	-

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.

6.2.1.2.8 LDO Output Capacitors

All LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2-µF capacitor for each LDO output is recommended. Note, this requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application or system should be evaluated for stability. See Table 6-10 for the specific part number of the recommended output capacitors. For BOM optimization purposes, the same capacitor part number was used for both LDO input and LDO output.

Table 6-10. Recommended LDO Output Capacitors(1)

MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
TDK	CGA3E1X7S1C225M080AC	2.2 µF, 16V, X7S	0603	1.6 x 0.8	Yes
Murata	GCM188R70J225KE22	2.2 µF, 16V, X7R	0603	1.6 x 0.8	-

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.

6.2.1.2.9 Digital Signal Connections

A detailed description of the application of each pin will go here. The VIO_IN pin may be optionally bypassed with a 0.47 µF bypass capacitor close to the pin.

Table 6-11. Recommended VIO_IN Capacitor

Component	MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
Capacitor	Murata	GCM155C71A474KE36	0.47 µF, 10 V, X7S	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B3X7S1A474K050BB	0.47 µF, 10 V, X7S	0402	1.0 x 0.5	-

I^2C pull-up resistor values for example.

ADVANCE INFORMATION

6.2.1.3 Application Curves

This section will contain some of the following types of graphs:

- Efficiency
- Load Reg
- Line Reg
- Temp Reg
- Phase adding / shedding (phases vs load)
- Startup (loaded and unloaded)
- Shutdown (loaded and unloaded)
- Ripple
- PFM to PWM to PFM
- 1 phase to n-phase transition
- Transients
- Slew rate options
- Examples of failures (i.e. start-up with short)

6.2.1.4 Layout

6.2.1.4.1 Layout Guidelines

This section will contain information regarding the recommended layout of the device.

For LDOs, the feedback is internal so keep PCB resistance between LDO output and target load in the range of the acceptable voltage drop.

6.2.1.4.2 Layout Example

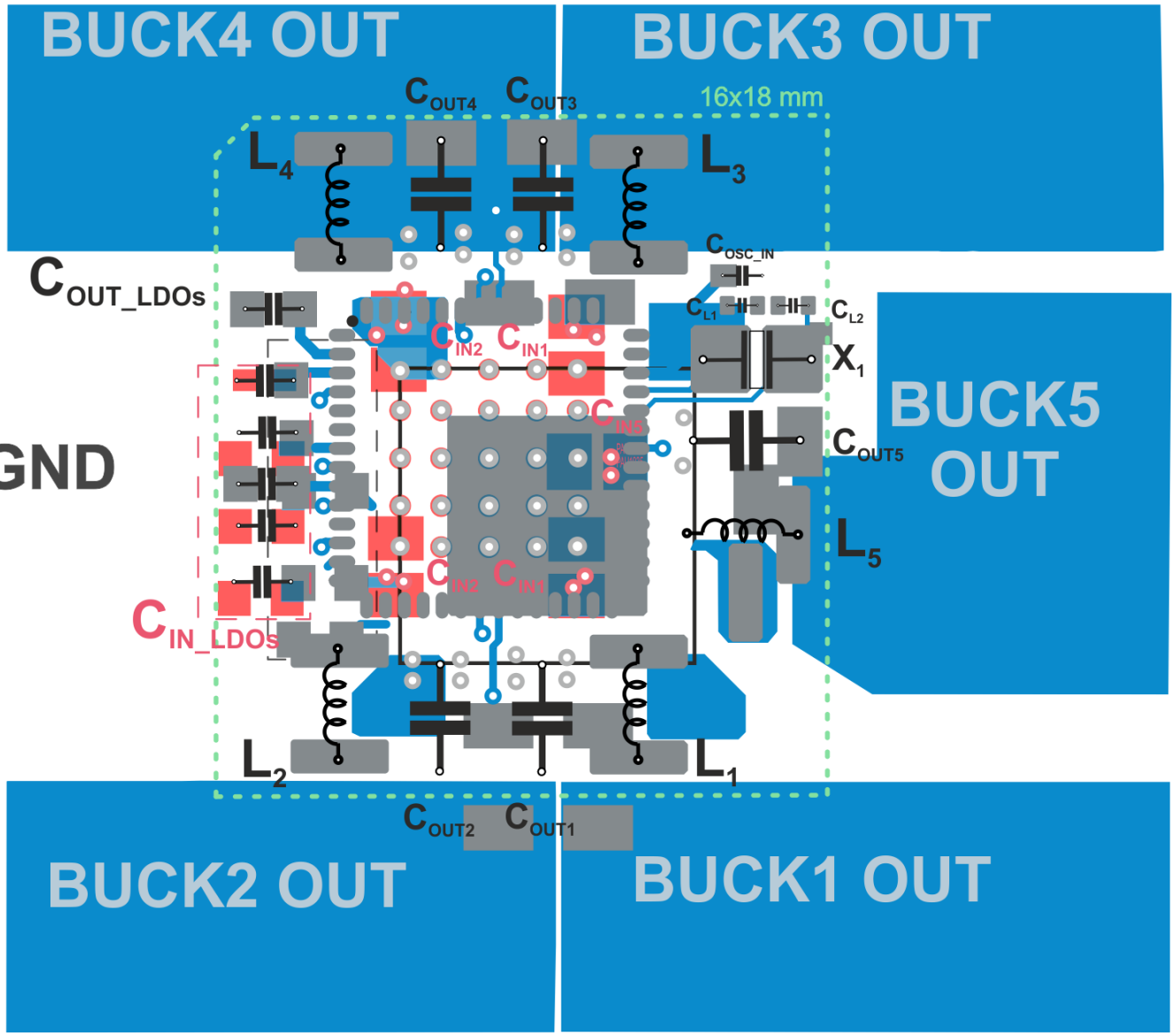

Figure 6-4. Example PMIC Layout

This example shows a top and bottom layout of the key power components and the crystal oscillator based on the EVM.

6.2.1.5 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.8 V and 5.5 V. This input supply must be well regulated and can withstand maximum input current and keep a stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high drop in the device supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

6.2.2 System Examples

This section will contain information on using this device with another companion PMIC, MCU, and processor.

6.2.3 Dos and Don’ts

This section will contain some graphical representations of common circuit design mistakes related to the device.

6.2.4 Initialization Setup

This is an optional section. It may be used to cover what items to review regarding GPIO or I2C communication required to power up the device or it may be omitted if previous sections cover these topics sufficiently.

7 器件和文档支持

7.1 器件支持

7.1.1 第三方产品免责声明

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7.1.2 器件命名规则

本数据表使用下列缩略词和术语。有关术语、缩写和定义的详细列表，请参阅《TI 术语表》。

ADC	模数转换器
APE	应用处理器引擎
AVS	自适应电压调节
DVS	动态电压调节
GPIO	通用输入/输出
LDO	低压降线性稳压器
PM	电源管理
PMIC	电源管理集成电路
PSRR	电源抑制比
RTC	实时时钟
NA	不适用
NVM	非易失性存储器
ESR	等效串联电阻
PMU	电源管理单元
PFM	脉频调制
PWM	脉宽调制
SPI	串行外设接口
EPC	嵌入式电源控制器
FSD	首次电源检测

7.2 文档支持

7.2.1 相关文档

请参阅如下相关文档：：

7.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.5 商标

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7.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

表 8-1. TPS6594-Q1封装特性

封装	说明
类型	VQFN
尺寸 (mm)	8mm × 8mm
间距 (mm)	0.5
ViP（过孔位于焊盘中）	否
引脚数	56
厚度 (mm)（包括引脚的最大高度）	1
湿敏等级目标	JEDEC MSL3 (260°C)
其它	绿色环保，符合 RoHS 标准

ADVANCE INFORMATION

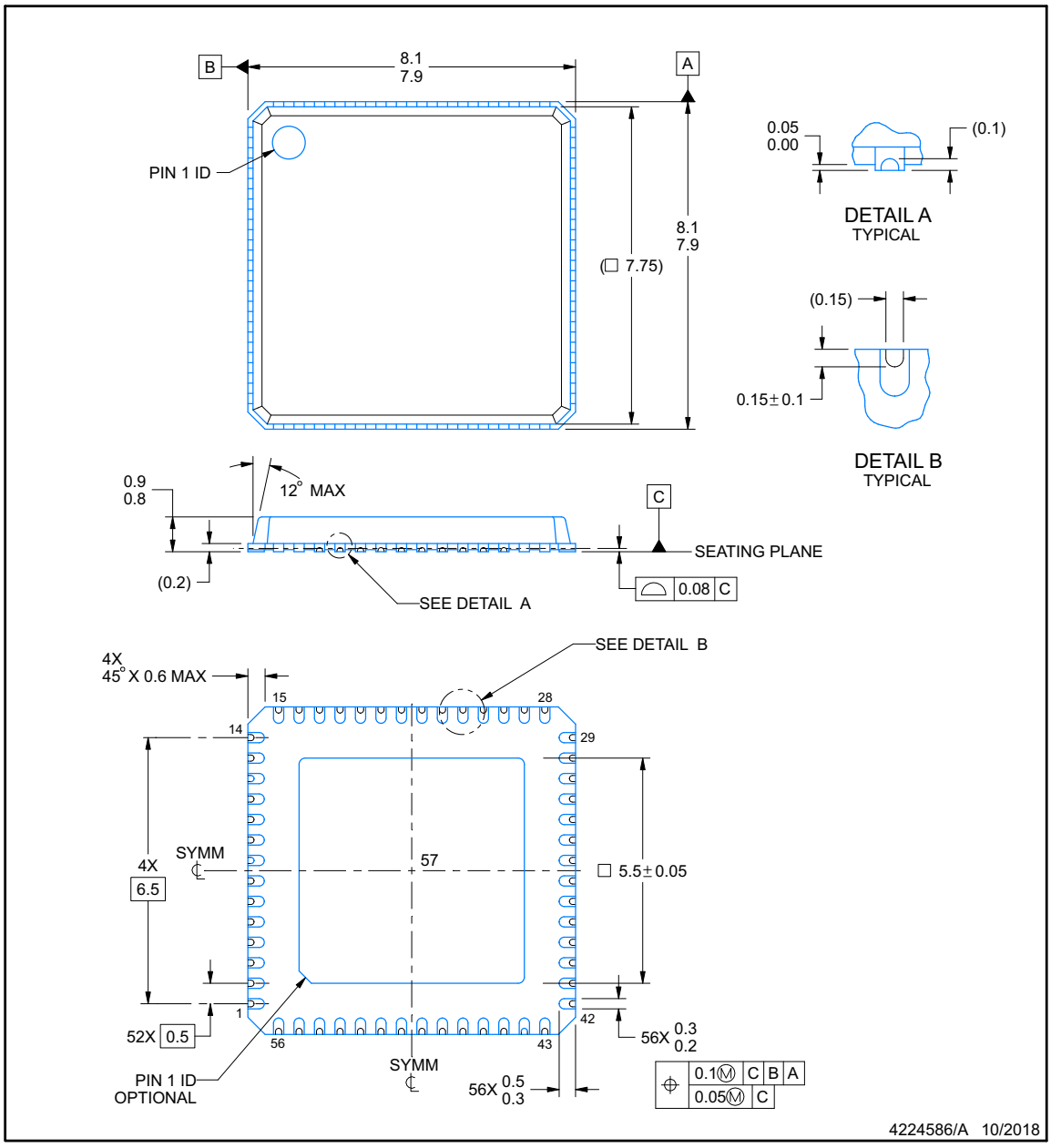
8.1 封装机械数据

RWE0056C

PACKAGE OUTLINE

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

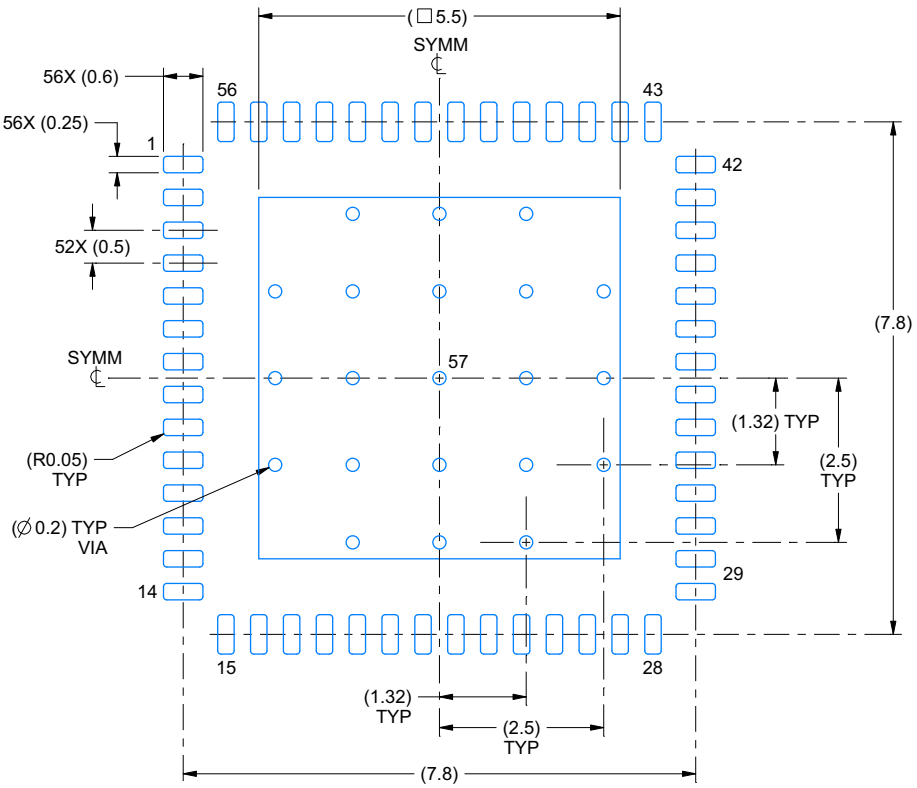
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

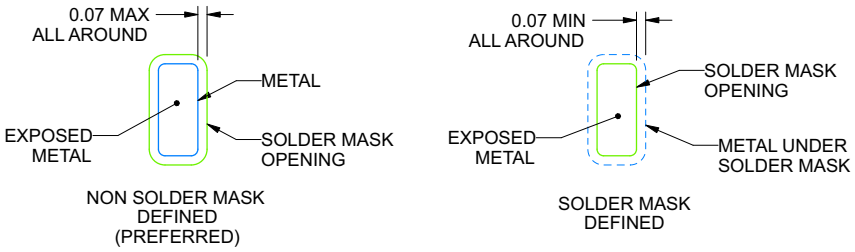
RWE0056C

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

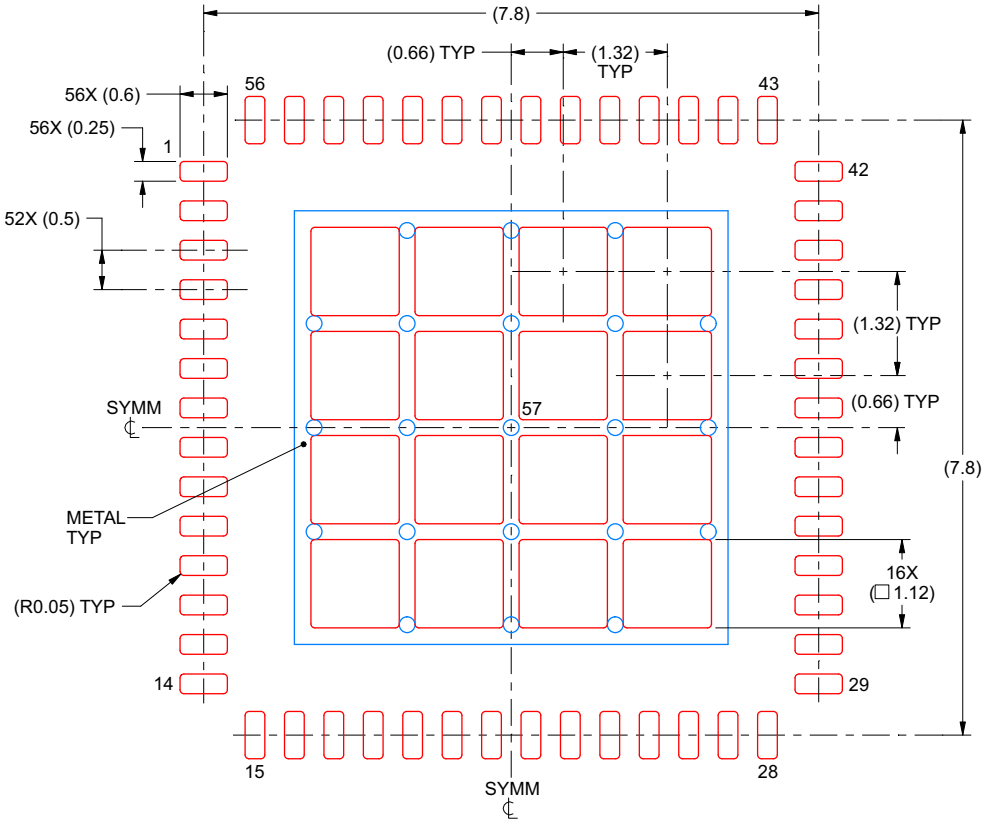
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RWE0056C — **VQFNP - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 57:
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4224586/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS659411F0RWERQ1	ACTIVE	VQFNP	RWE	56	2000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS659413F0RWERQ1	ACTIVE	VQFNP	RWE	56	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

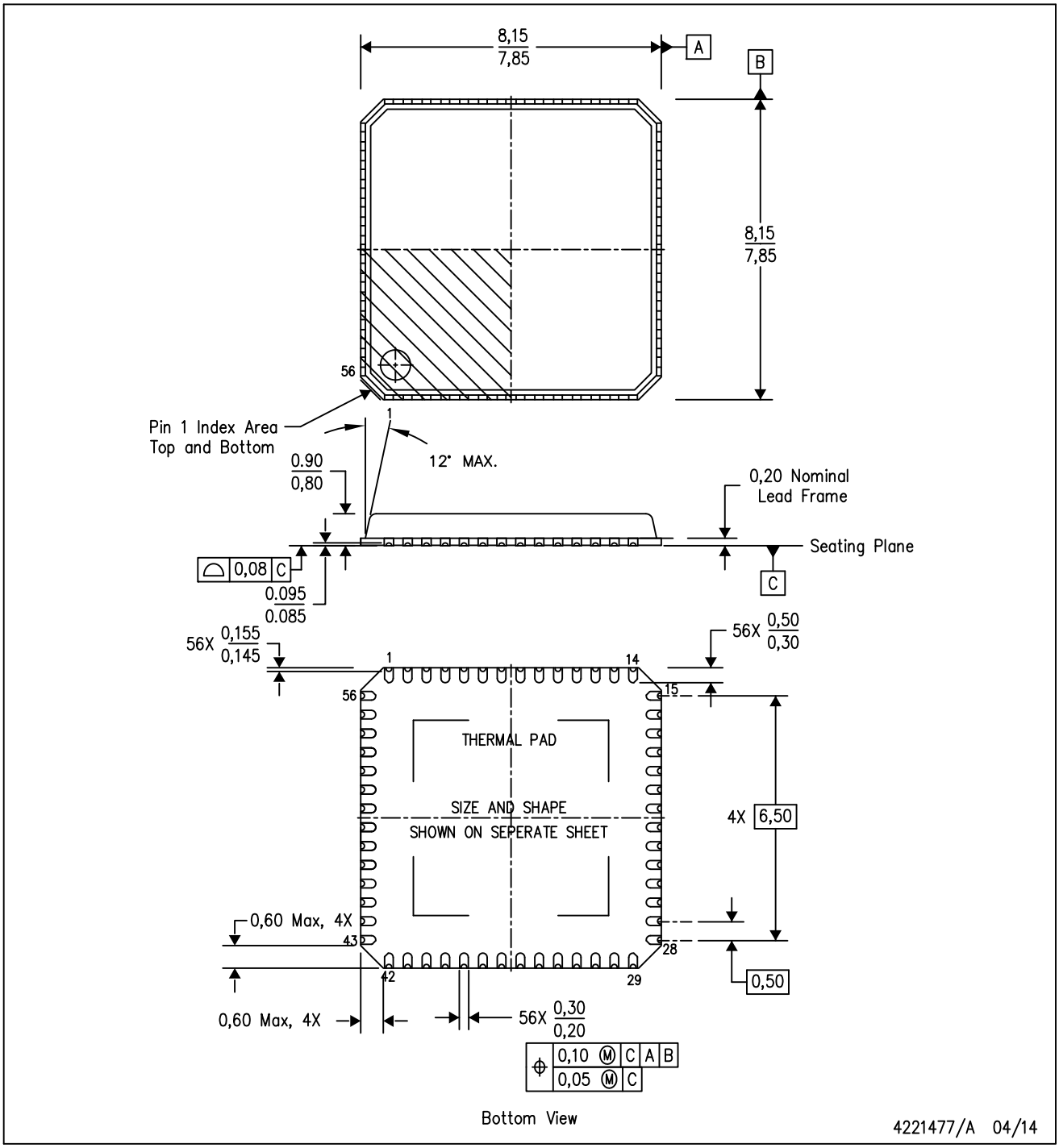
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RWE (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.
G. Slot/Dimple added to external leads.

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>>TI(德州仪器)