TEXAS INSTRUMENTS

SN54HC165, SN74HC165

SCLS116H – DECEMBER 1982 – REVISED DECEMBER 2015

SNx4HC165 8-Bit Parallel-Load Shift Registers

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption, 80-µA Maximum I_{CC}
- Typical t_{pd} = 13 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA Maximum
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Programable Logic Controllers
- Appliances
- Video Display Systems
- Output Expander
- Keyboards

3 Description

The SNx4HC165 devices are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A−H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The SNx4HC165 devices also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

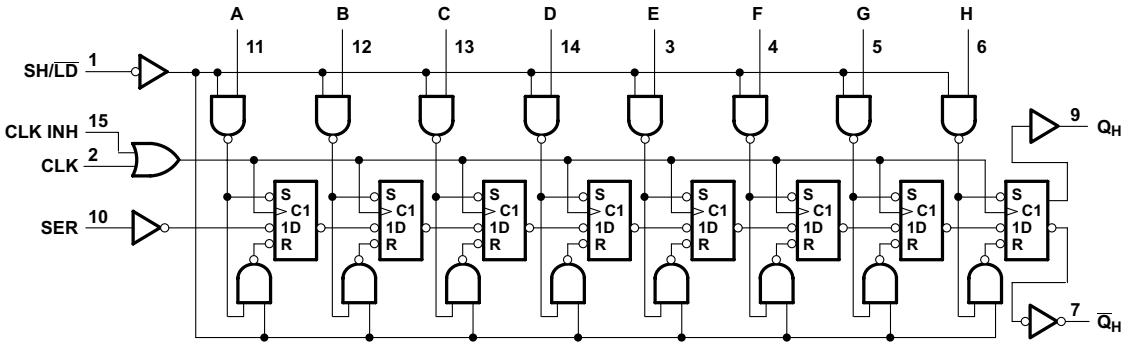
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Because a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC165D	SOIC (16)	10.00 mm × 6.20 mm
SN74HC165DB	SSOP (16)	8.20 mm × 6.50 mm
SN74HC165N	PDIP (16)	6.60 mm × 18.92 mm
SN74HC165NS	SO (16)	8.20 mm × 9.90 mm
SN74HC165PW	TSSOP (16)	6.60 mm × 5.10 mm
SN54HC165FK	LCCC (20)	9.09 mm × 9.09 mm
SN54HC165J	CDIP (16)	21.34 mm × 7.52 mm
SN54HC165W	CFP (16)	9.40 mm × 7.75 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram Positive Logic



Pin numbers shown are for the D, DB, J, N, NS, PW and W packages.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2013) to Revision H — **Page**

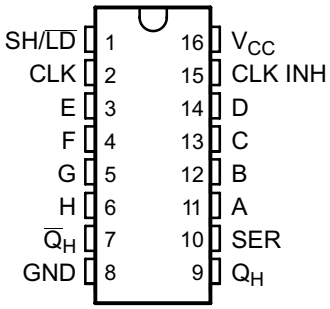
- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added Military Disclaimer to *Features* list. ... 1
- Added ESD warning. ... 16

Changes from Revision F (December 2010) to Revision G — **Page**

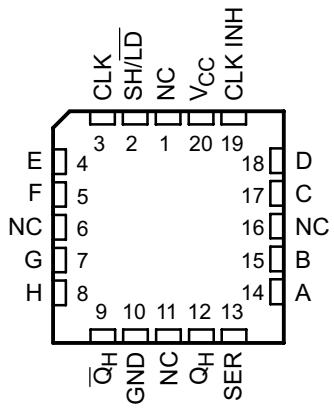
- Updated document to new TI data sheet format - no specification changes. ... 1
- Removed *Ordering Information* table. ... 1
- Added Handling Ratings table. ... 4
- Extended maximum temperature operating range from 85°C to 125°C. ... 4

5 Pin Configuration and Functions

D, DB, N, NS, J, W, or PW Package
16-Pin SOIC, SSOP, PDIP, SO, CDIP, CFP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions(1)

PIN			I/O	DESCRIPTION
NAME	D, DB, N, NS, PW, J or W	FK		
A	11	14	I	Parallel Input
B	12	15	I	Parallel Input
C	13	17	I	Parallel Input
CLK	2	3	I	Clock input
CLK INH	15	19	I	Clock Inhibit, when High No change in output
D	14	18	I	Parallel Input
E	3	4	I	Parallel Input
F	4	5	I	Parallel Input
G	5	7	I	Parallel Input
GND	8	10	—	Ground Pin
H	6	8	I	Parallel Input
NC	—	1	—	Not Connected
		6		
		11		
		16		
Q_H	9	12	O	Serial Output
$\overline{Q}_H$	7	9	O	Complementary Serial Output
SER	10	13	I	Serial Input
SH/$\overline{LD}$	1	2	I	Shift or Load input, When High Data, shifted. When Low data is loaded from parallel inputs
V_{CC}	16	20	—	Power Pin

(1) NC – No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$(2)	Input transition rise and fall time	V_{CC} = 2 V			1000	ns/V
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC165	–55		125	°C
		SN74HC165	–40		125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

6.4 Thermal Information

THERMAL METRIC(1)		SN74HC165					UNIT
		D (SOIC)	DB (SSOP)	N (DIP)	NS (SO)	PW (TSSOP)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, T_A = 25°C

over recommended operating free-air temperature range for both the SN74HC165 and SN54HC165 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		V
			4.5 V	4.4	4.499		
			6 V	5.9	5.999		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1	V
			4.5 V		0.001	0.1	
			6 V		0.001	0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26	
		I_{OL} = 5.2 mA	6 V		0.15	0.26	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8	µA
C_i			2 V to 6 V		3	10	pF

6.6 Electrical Characteristics, SN54HC165

over recommended operating free-air temperature range, T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9			V
			4.5 V	4.4			
			6 V	5.9			
		I_{OH} = –4 mA	4.5 V	3.7			
		I_{OH} = –5.2 mA	6 V	5.2			
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V			0.1	V
			4.5 V			0.1	
			6 V			0.1	
		I_{OL} = 4 mA	4.5 V			0.4	
		I_{OL} = 5.2 mA	6 V			0.4	
I_I	V_I = V_{CC} or 0		6 V			±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			160	µA
C_i			2 V to 6 V			10	pF

6.7 Electrical Characteristics, SN74HC165

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	T_A = –40°C to 125°C	2 V	1.9			V
				4.5 V	4.4			
				6 V	5.9			
		I_{OH} = –4 mA	T_A = –40°C to 85°C	4.5 V	3.84			
			T_A = –40°C to 125°C		3.7			
		I_{OH} = –5.2 mA	T_A = –40°C to 85°C	6 V	5.34			
			T_A = –40°C to 125°C		5.2			
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	T_A = –40°C to 125°C	2 V			0.1	V
				4.5 V			0.1	
				6 V			0.1	
		I_{OL} = 4 mA	T_A = –40°C to 125°C	4.5 V			0.33	
		I_{OL} = 5.2 mA	T_A = –40°C to 125°C	6 V			0.33	

Electrical Characteristics, SN74HC165 (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
I_I	$V_I = V_{CC}$ or 0	T_A = –40°C to 125°C	6 V			±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	T_A = –40°C to 85°C	6 V			80	µA
		T_A = –40°C to 125°C				160	
C_i	Recommended T_A = –40°C to 125°C		2 V to 6 V			10	pF

6.8 Switching Characteristics, T_A = 25°C

over recommended operating free-air temperature range for both the SN74HC165 and SN54HC165, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}			2 V	6	13		MHz
			4.5 V	31	50		
			6 V	36	62		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		80	150	ns
			4.5 V		20	30	
			6 V		16	26	
	CLK	Q_H or $\overline{Q}_H$	2 V		75	150	
			4.5 V		15	30	
			6 V		13	26	
	H	Q_H or $\overline{Q}_H$	2 V		75	150	
			4.5 V		15	30	
			6 V		13	26	
t_t		Any	2 V		38	75	ns
			4.5 V		8	15	
			6 V		6	13	

6.9 Switching Characteristics, SN54HC165

over recommended operating free-air temperature range, T_A = –55°C to 125°C, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			2 V	4.2		MHz
			4.5 V	21		
			6 V	25		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		225	ns
			4.5 V		45	
			6 V		38	
	CLK	Q_H or $\overline{Q}_H$	2 V		225	
			4.5 V		45	
			6 V		38	
	H	Q_H or $\overline{Q}_H$	2 V		225	
			4.5 V		45	
			6 V		38	
t_t		Any	2 V		110	ns
			4.5 V		22	
			6 V		19	

6.10 Switching Characteristics, SN74HC165

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	TEMPERATURE	MIN	MAX	UNIT
f_{max}			2 V	T_A = –40°C to 85°C	5		MHz
				T_A = –40°C to 125°C	4.2		
			4.5 V	T_A = –40°C to 85°C	25		
				T_A = –40°C to 125°C	21		
			6 V	T_A = –40°C to 85°C	29		
				T_A = –40°C to 125°C	25		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V	T_A = –40°C to 85°C		190	ns
				T_A = –40°C to 125°C		225	
			4.5 V	T_A = –40°C to 85°C		38	
				T_A = –40°C to 125°C		45	
			6 V	T_A = –40°C to 85°C		32	
				T_A = –40°C to 125°C		38	
	CLK	Q_H or $\overline{Q}_H$	2 V	T_A = –40°C to 85°C		190	
				T_A = –40°C to 125°C		225	
			4.5 V	T_A = –40°C to 85°C		38	
				T_A = –40°C to 125°C		45	
			6 V	T_A = –40°C to 85°C		32	
				T_A = –40°C to 125°C		38	
	H	Q_H or $\overline{Q}_H$	2 V	T_A = –40°C to 85°C		190	
				T_A = –40°C to 125°C		225	
			4.5 V	T_A = –40°C to 85°C		38	
				T_A = –40°C to 125°C		45	
			6 V	T_A = –40°C to 85°C		32	
				T_A = –40°C to 125°C		38	
t_t		Any	2 V	T_A = –40°C to 85°C		95	ns
				T_A = –40°C to 125°C		110	
			4.5 V	T_A = –40°C to 85°C		19	
				T_A = –40°C to 125°C		22	
			6 V	T_A = –40°C to 85°C		16	
				T_A = –40°C to 125°C		19	

6.11 Timing Requirements, T_A = 25°C

over recommended operating free-air temperature range for both the SN74HC165 and SN54HC165 (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		2 V		6	MHz
			4.5 V		31	
			6 V		36	
t_w	Pulse duration	SH/$\overline{LD}$ low	2 V	80		ns
			4.5 V	16		
			6 V	14		
		CLK high or low	2 V	80		
			4.5 V	16		
			6 V	14		

Timing Requirements, T_A = 25°C (continued)

over recommended operating free-air temperature range for both the SN74HC165 and SN54HC165 (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
t_{su}	Set-up time	SH/$\overline{LD}$ high before CLK↑	2 V	80		ns
			4.5 V	16		
			6 V	14		
		SER before CLK↑	2 V	40		
			4.5 V	8		
			6 V	7		
		CLK INH low before CLK↑	2 V	100		
			4.5 V	20		
			6 V	17		
		CLK INH high before CLK↑	2 V	40		
			4.5 V	8		
			6 V	7		
		Data before SH/$\overline{LD}$↓	2 V	100		
			4.5 V	20		
			6 V	17		
t_h	Hold time	SER data after CLK↑	2 V	5		ns
			4.5 V	5		
			6 V	5		
		PAR data after SH/$\overline{LD}$↓	2 V	5		
			4.5 V	5		
			6 V	5		

6.12 Timing Requirements, SN54HC165

over recommended operating free-air temperature range, T_A = –55°C to 125°C (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		2 V		4.2	MHz
			4.5 V		21	
			6 V		25	
t_w	Pulse duration	SH/$\overline{LD}$ low	2 V	120		ns
			4.5 V	24		
			6 V	20		
		CLK high or low	2 V	120		
			4.5 V	24		
			6 V	20		

Timing Requirements, SN54HC165 (continued)

over recommended operating free-air temperature range, T_A = –55°C to 125°C (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
t_{su}	Set-up time	SH/$\overline{LD}$ high before CLK↑	2 V	120		ns
			4.5 V	24		
			6 V	20		
		SER before CLK↑	2 V	60		
			4.5 V	12		
			6 V	10		
		CLK INH low before CLK↑	2 V	150		
			4.5 V	30		
			6 V	25		
		CLK INH high before CLK↑	2 V	60		
			4.5 V	12		
			6 V	10		
		Data before SH/$\overline{LD}$↓	2 V	150		
			4.5 V	30		
			6 V	26		
t_h	Hold time	SER data after CLK↑	2 V	5		ns
			4.5 V	5		
			6 V	5		
		PAR data after SH/$\overline{LD}$↓	2 V	5		
			4.5 V	5		
			6 V	5		

6.13 Timing Requirements, SN74HC165

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	TEMPERATURE	MIN	MAX	UNIT
f_{clock}	Clock frequency		2 V	T_A = –40°C to 85°C		5	MHz
				T_A = –40°C to 125°C		4.2	
			4.5 V	T_A = –40°C to 85°C		25	
				T_A = –40°C to 125°C		21	
			6 V	T_A = –40°C to 85°C		29	
				T_A = –40°C to 125°C		25	
t_w	Pulse duration	SH/$\overline{LD}$ low	2 V	T_A = –40°C to 85°C	100		ns
				T_A = –40°C to 125°C	120		
			4.5 V	T_A = –40°C to 85°C	20		
				T_A = –40°C to 125°C	24		
			6 V	T_A = –40°C to 85°C	17		
				T_A = –40°C to 125°C	20		
		CLK high or low	2 V	T_A = –40°C to 85°C	100		
				T_A = –40°C to 125°C	120		
			4.5 V	T_A = –40°C to 85°C	20		
				T_A = –40°C to 125°C	24		
			6 V	T_A = –40°C to 85°C	17		
				T_A = –40°C to 125°C	20		

Timing Requirements, SN74HC165 (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	TEMPERATURE	MIN	MAX	UNIT
t_{su}	Set-up time	SH/$\overline{LD}$ high before CLK↑	2 V	T_A = –40°C to 85°C	100		ns
				T_A = –40°C to 125°C	120		
			4.5 V	T_A = –40°C to 85°C	20		
				T_A = –40°C to 125°C	24		
			6 V	T_A = –40°C to 85°C	17		
				T_A = –40°C to 125°C	20		
		SER before CLK↑	2 V	T_A = –40°C to 85°C	50		
				T_A = –40°C to 125°C	60		
			4.5 V	T_A = –40°C to 85°C	10		
				T_A = –40°C to 125°C	12		
			6 V	T_A = –40°C to 85°C	9		
				T_A = –40°C to 125°C	10		
		CLK INH low before CLK↑	2 V	T_A = –40°C to 85°C	125		
				T_A = –40°C to 125°C	150		
			4.5 V	T_A = –40°C to 85°C	25		
				T_A = –40°C to 125°C	30		
			6 V	T_A = –40°C to 85°C	21		
				T_A = –40°C to 125°C	25		
		CLK INH high before CLK↑	2 V	T_A = –40°C to 85°C	50		
				T_A = –40°C to 125°C	60		
			4.5 V	T_A = –40°C to 85°C	10		
				T_A = –40°C to 125°C	12		
			6 V	T_A = –40°C to 85°C	9		
				T_A = –40°C to 125°C	10		
		Data before SH/$\overline{LD}$↓	2 V	T_A = –40°C to 85°C	125		
				T_A = –40°C to 125°C	150		
			4.5 V	T_A = –40°C to 85°C	25		
				T_A = –40°C to 125°C	30		
			6 V	T_A = –40°C to 85°C	21		
				T_A = –40°C to 125°C	26		
t_h	Hold time	SER data after CLK↑	2 V	T_A = –40°C to 125°C	5		ns
			4.5 V	T_A = –40°C to 125°C	5		
			6 V	T_A = –40°C to 125°C	5		
		PAR data after SH/$\overline{LD}$↓	2 V	T_A = –40°C to 125°C	5		
			4.5 V	T_A = –40°C to 125°C	5		
			6 V	T_A = –40°C to 125°C	5		

6.14 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	75	pF

6.15 Typical Characteristics

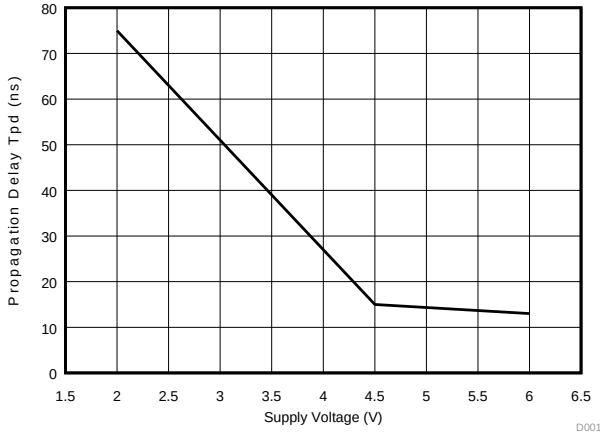
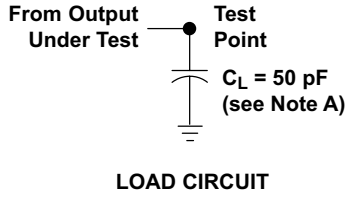
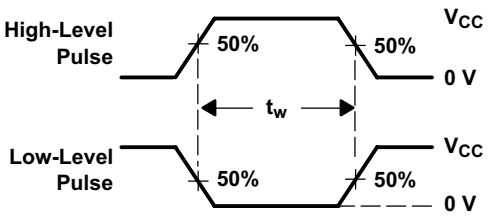


Figure 1. Propagation Delay vs Supply Voltage at T_A = 25°C

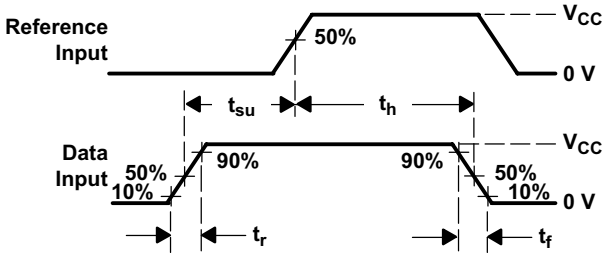
7 Parameter Measurement Information



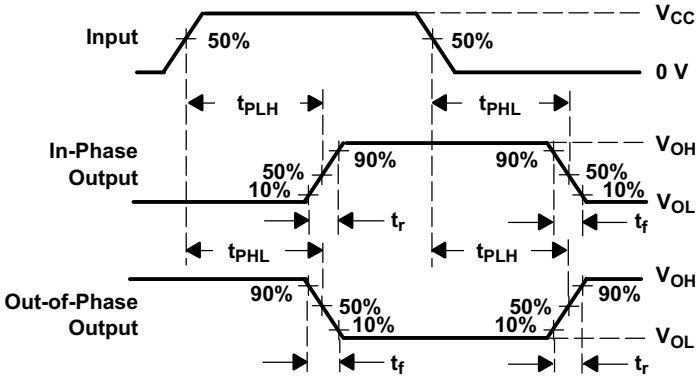
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

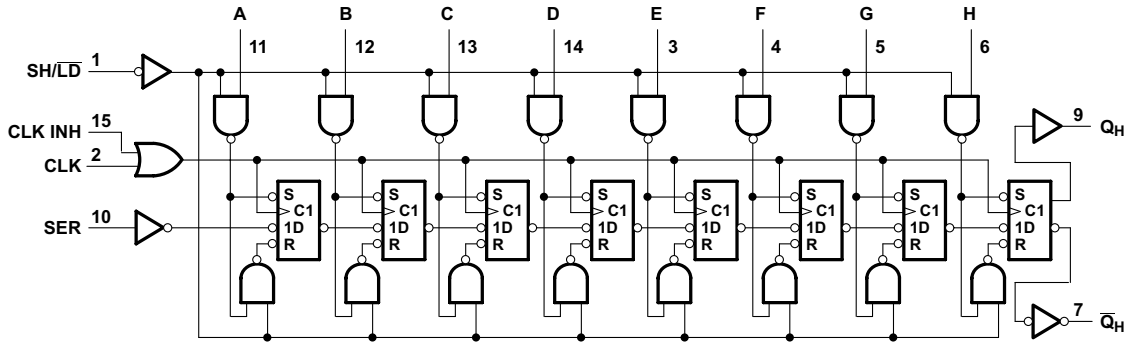
8.1 Overview

The SNx4HC165 is an 8-bit Parallel load shift register with 1 serial input and 8 parallel load input. The device loads all the 8 bits simultaneously through parallel load input when SH/$\overline{LD}$ is low. This will also ignore any input at CLK or CLK INH.

The device shifts the data when CLK toggles. The data is shifted on rising edge of the clock. Clock Inhibit (CLK INH) inhibits the clock function resulting in no change of the output. If SH/$\overline{LD}$ is low clock inputs are ignored. To realize the shift function, SH/$\overline{LD}$ should be high.

CLK and CLK INH functions are interchangeable. If CLK is low then change a clock signal at CLK INH pin causes a shift of data to Q_H. If CLK INH is Low clock signal on CLK pin shifts the data out to Q_H.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Figure 3. Logic Diagram Positive Logic

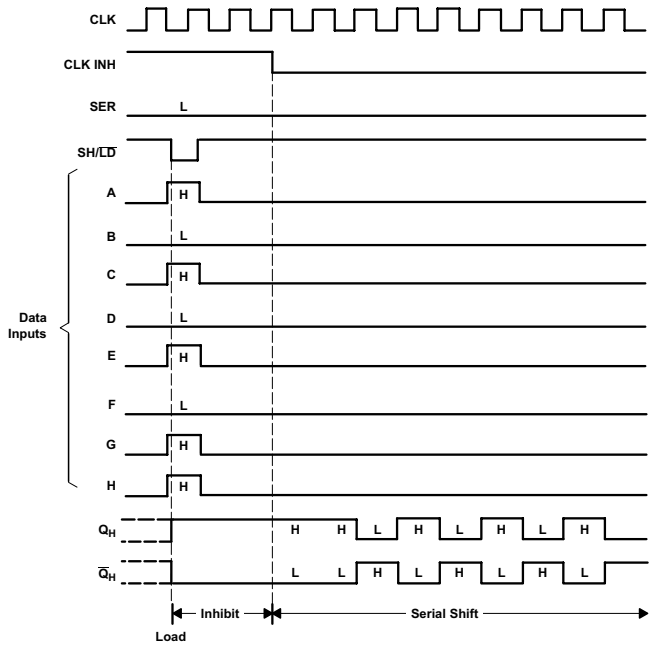


Figure 4. Typical Shift, Load, and Inhibit Sequence

8.3 Feature Description

The SNx4HC165 has a wide operating voltage range of 2 V to 6 V, outputs that can drive up to 10 LSTTL loads and Low Power Consumption, 80-μA maximum I. It is typically t_{pd} = 13 ns and has ±4-mA output drive at 5 V with low input current of 1-μA maximum. The device features the direct overloading load of data input, meaning parallel data is loaded irrespective of clock signals.

8.4 Device Functional Table

Table 1 lists the functional modes of the SNx4HC165.

Table 1. Function Table

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift(1)
H	↑	L	Shift(1)

(1) Shift : Content of each internal register shifts towards serial output Q_H. Data at SER is shifted into the first register

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC165 is an 8-bit shift register that can be used as a serializer in order to reduce the number of connection needed when transmitting signals between boards or to the device. SNx4HC165 can be used to expand inputs for processors with limited GPIOs for examples basic keyboard interface to the controller. SNx4HC165 allows inputs to be load into the shift registers and clock is used to shift data to the processor. Multiple SNx4HC165 can be cascaded together to allow more digital inputs to be interfaced with single processor by connecting output of the cascaded shift register Q_H to serial input SER of the SNx4HC165 and so on. Note this application does not allow the communication to be bi-direction in nature as data can only be read by the processor not written back.

9.2 Typical Application

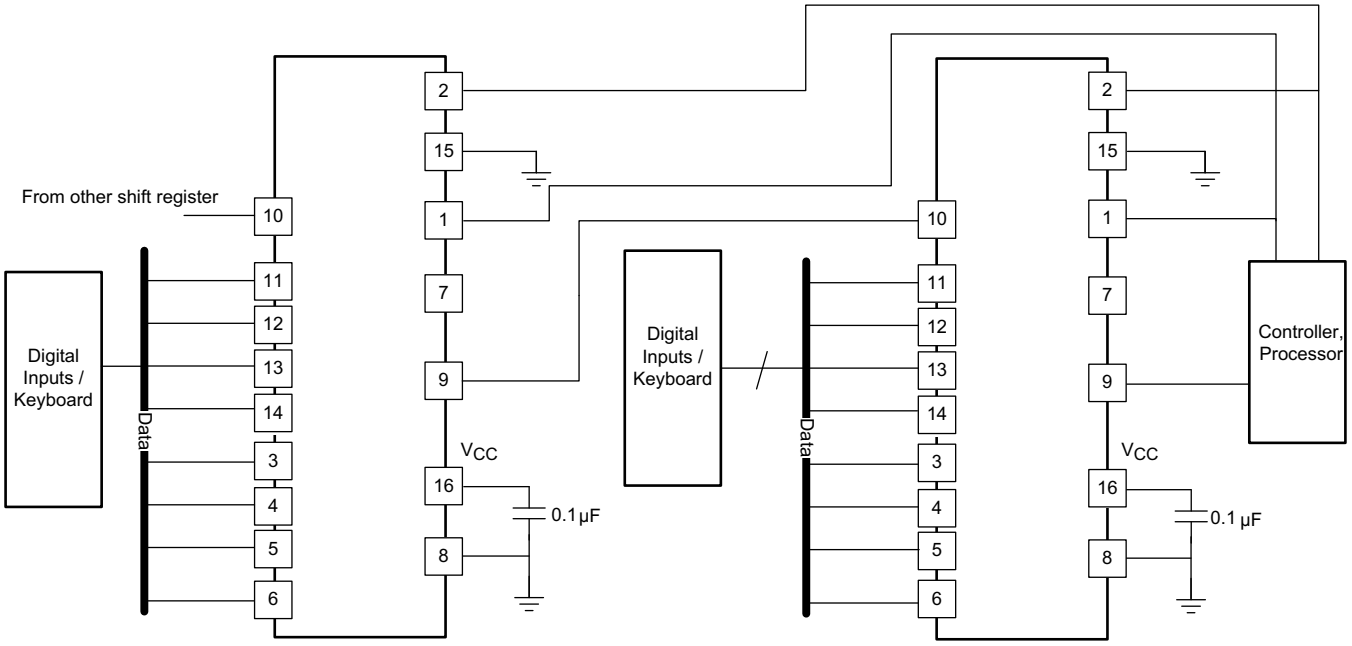


Figure 5. Typical Application Diagram for SN74HC165

9.2.1 Design Requirements

Ensure that the incoming clock rising edge meets the criteria in *Recommended Operating Conditions*.

9.2.2 Detailed Design Procedure

Ensure that input and output voltages do not exceed ratings in *Absolute Maximum Ratings*.

Input voltage threshold information for each device can be found in the Electrical Characteristics tables in the *Specifications* section.

Detailed timing requirements for each device can be found in Timing Requirements tables in the *Specifications section*.

Typical Application (continued)

9.2.3 Application Curve

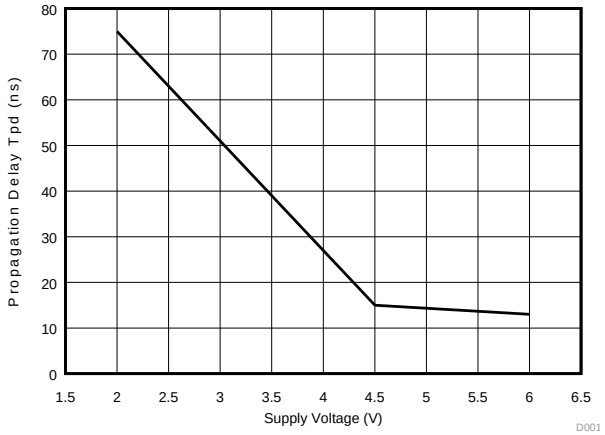


Figure 6. Propagation Delay vs Supply Voltage at T_A = 25°C

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin must have a good bypass capacitor in order to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 7 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

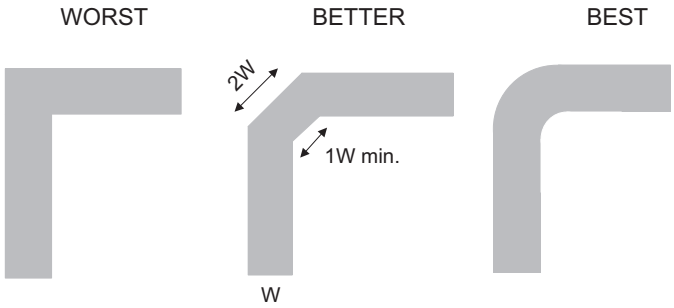


Figure 7. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Implications of Slow or Floating CMOS Inputs, SCBA004.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC165	Click here	Click here	Click here	Click here	Click here
SN74HC165	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84095012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84095012A SNJ54HC 165FK	Samples
8409501EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409501EA SNJ54HC165J	Samples
8409501FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409501FA SNJ54HC165W	Samples
SN54HC165J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC165J	Samples
SN74HC165DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165DRG3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC165N	Samples
SN74HC165NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC165N	Samples
SN74HC165NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165PWRG3	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SN74HC165PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC165	Samples
SNJ54HC165FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84095012A SNJ54HC 165FK	Samples
SNJ54HC165J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409501EA SNJ54HC165J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC165W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409501FA SNJ54HC165W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC165, SN74HC165 :

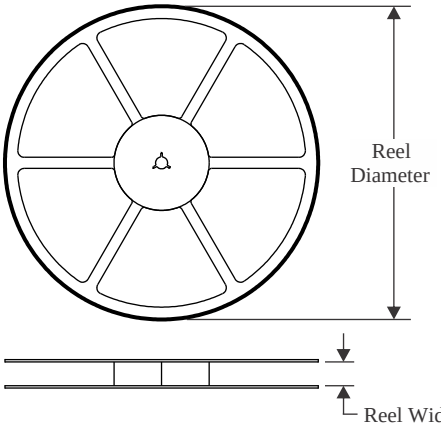
- Catalog : SN74HC165
- Automotive : SN74HC165-Q1, SN74HC165-Q1
- Enhanced Product : SN74HC165-EP, SN74HC165-EP
- Military : SN54HC165

NOTE: Qualified Version Definitions:

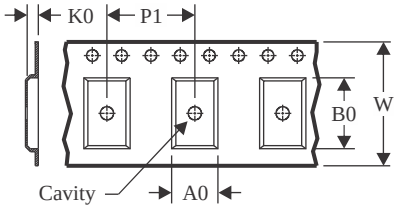
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

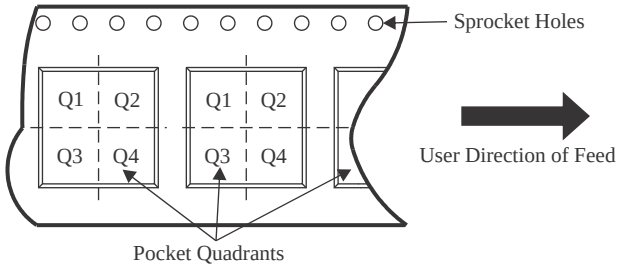


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

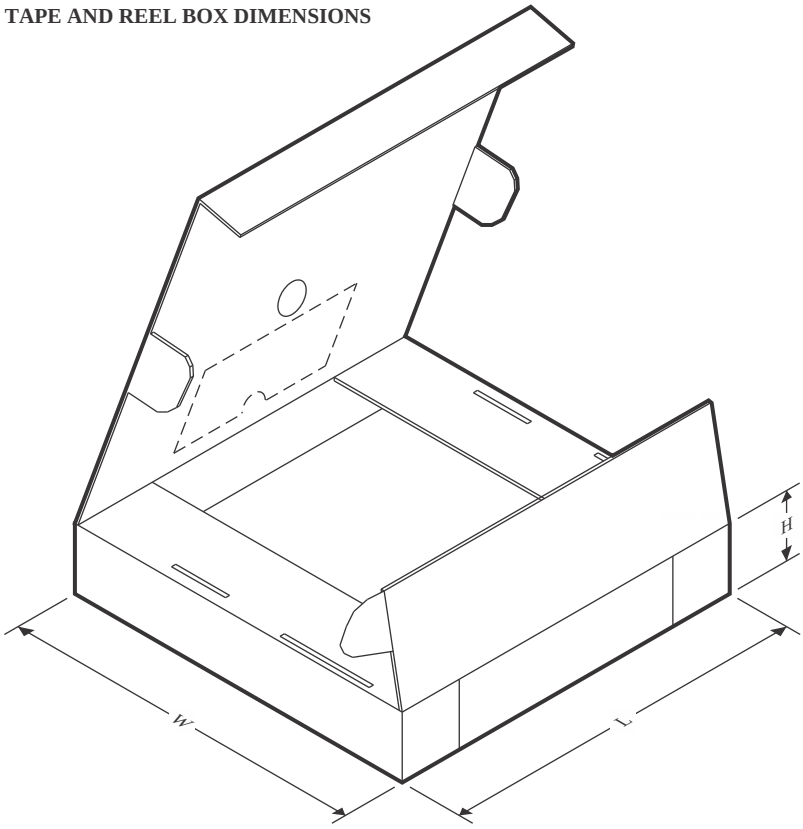
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC165DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC165DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC165DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC165DRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC165DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC165DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC165NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC165NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC165PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC165PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC165PWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC165PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC165PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

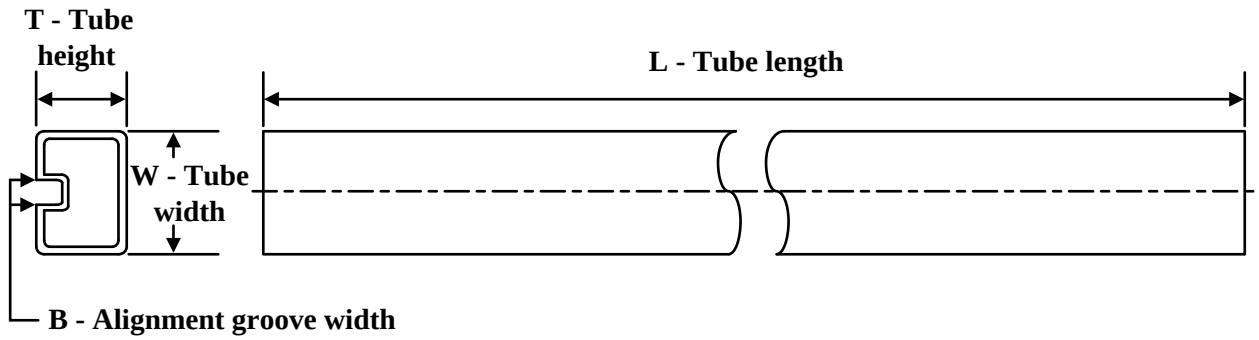
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC165DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC165DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC165DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC165DRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74HC165DRG4	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC165DRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC165NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC165NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC165PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC165PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC165PWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74HC165PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC165PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

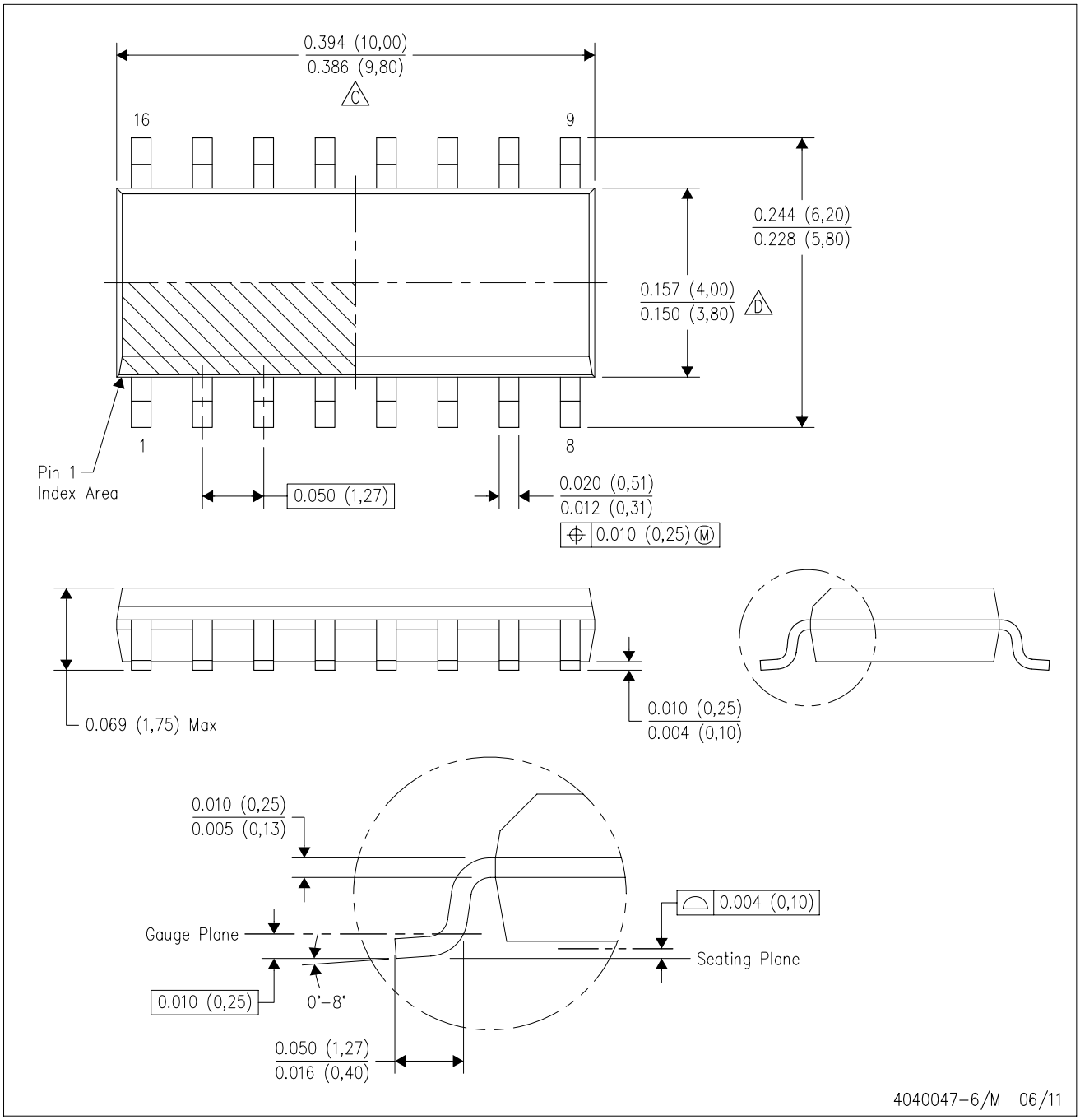
TUBE



*All dimensions are nominal

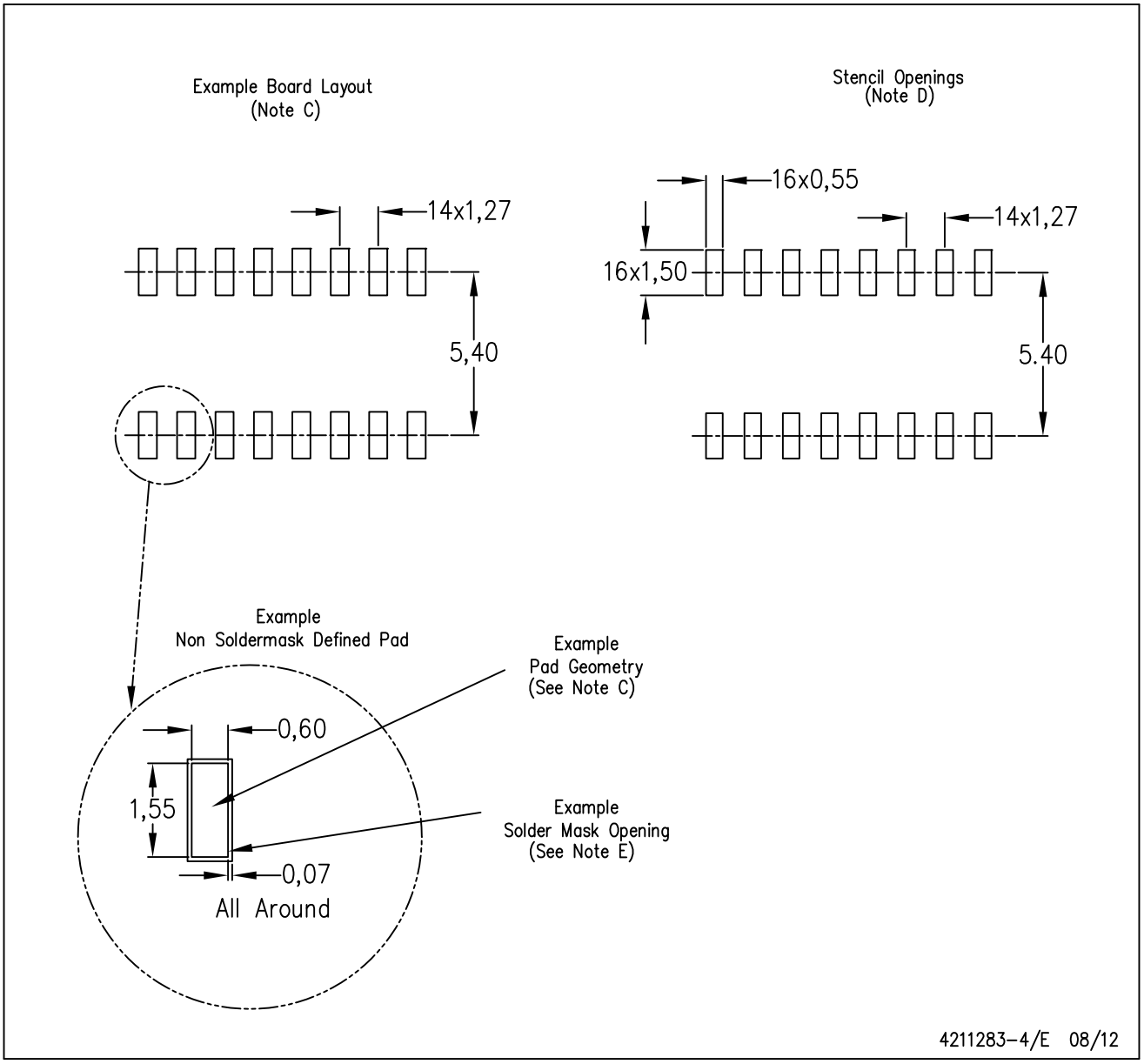
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
84095012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8409501FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC165N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC165N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC165NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC165NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC165FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC165W	W	CFP	16	25	506.98	26.16	6220	NA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



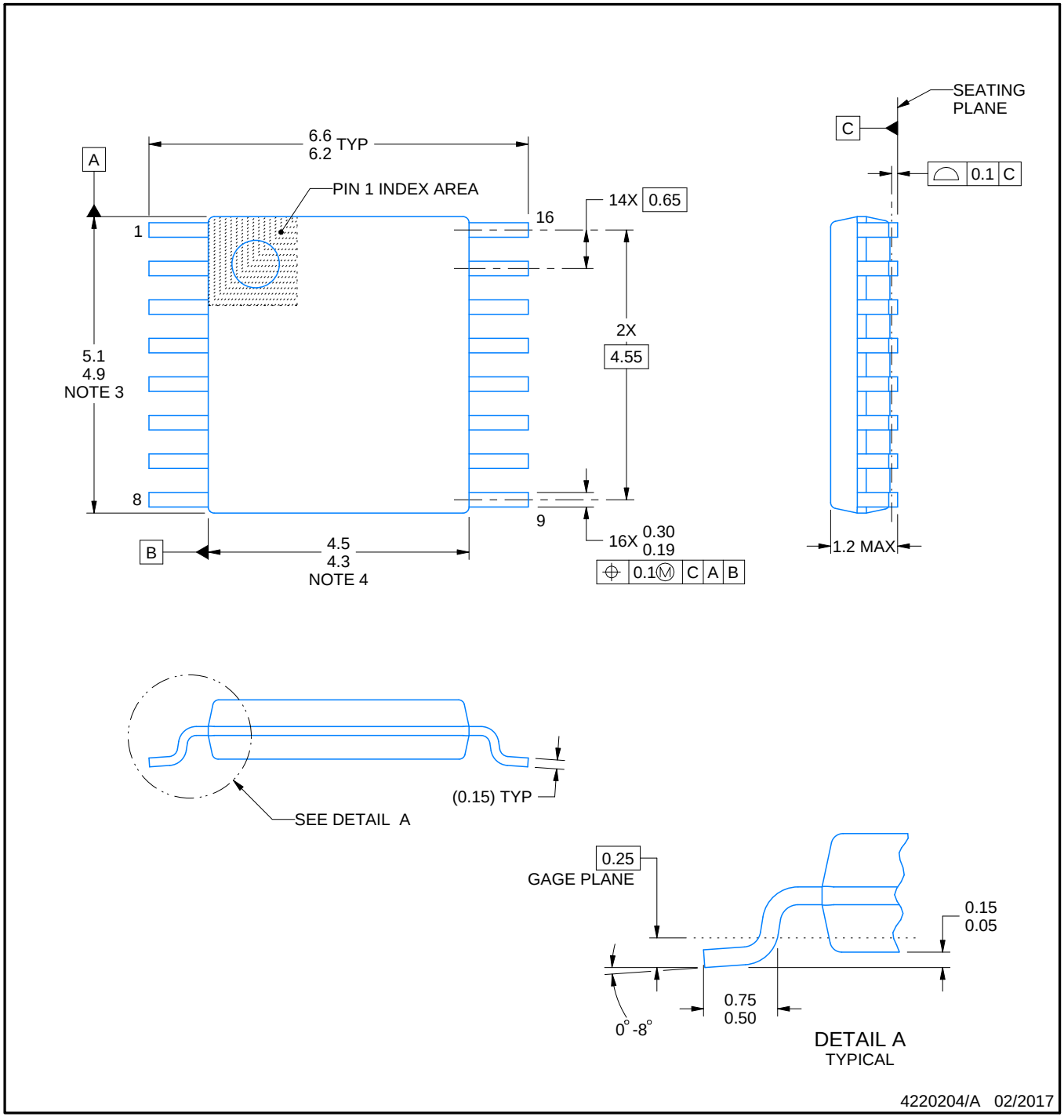
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

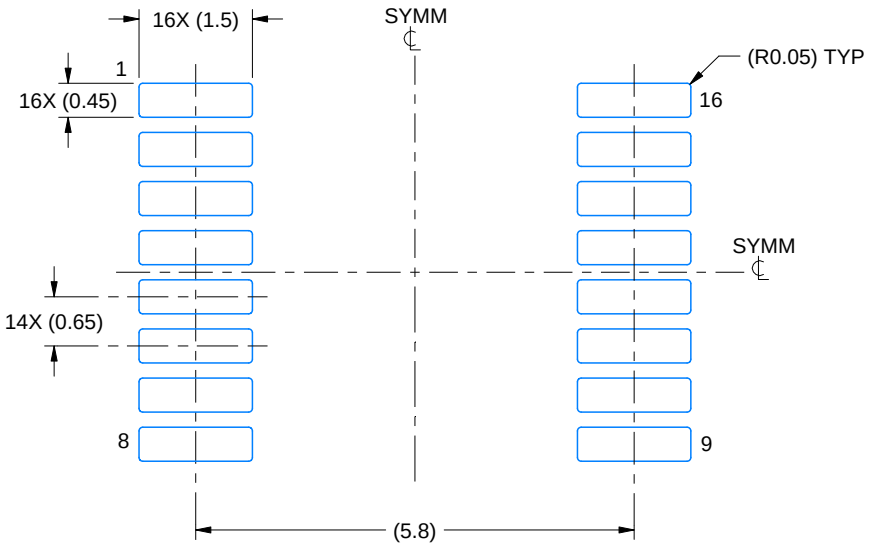
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

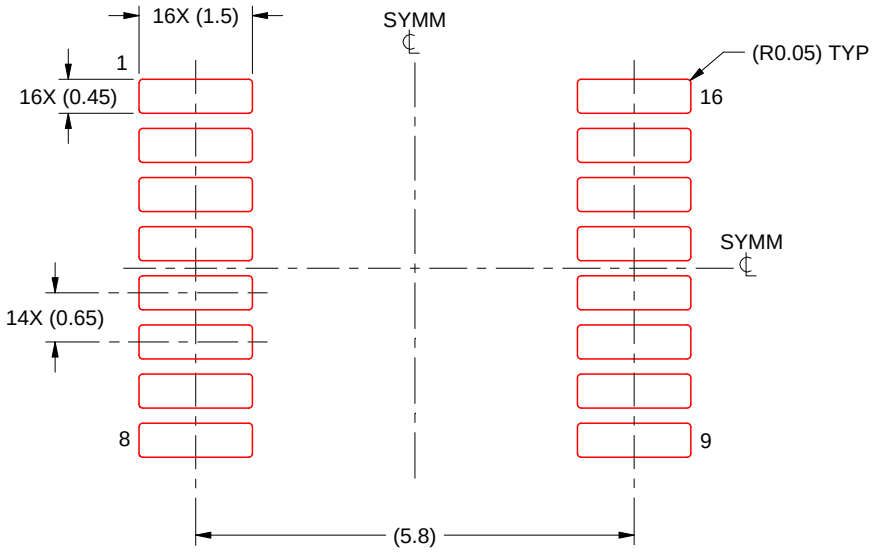
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

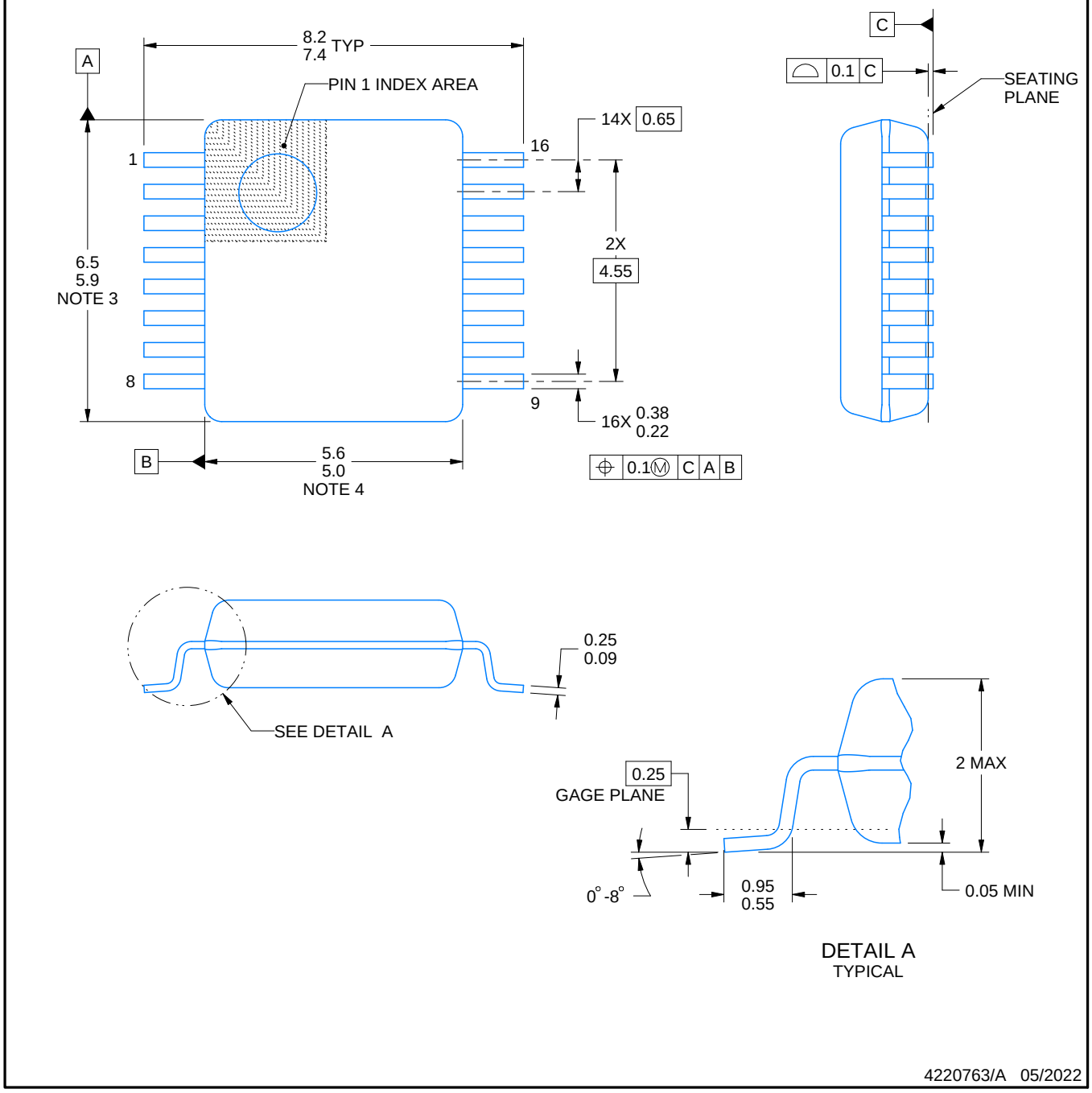
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

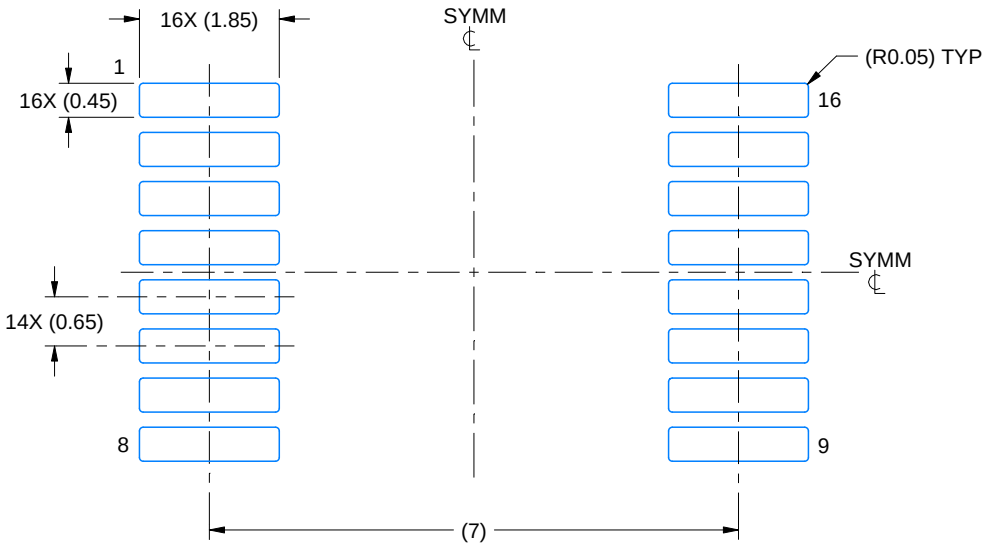
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

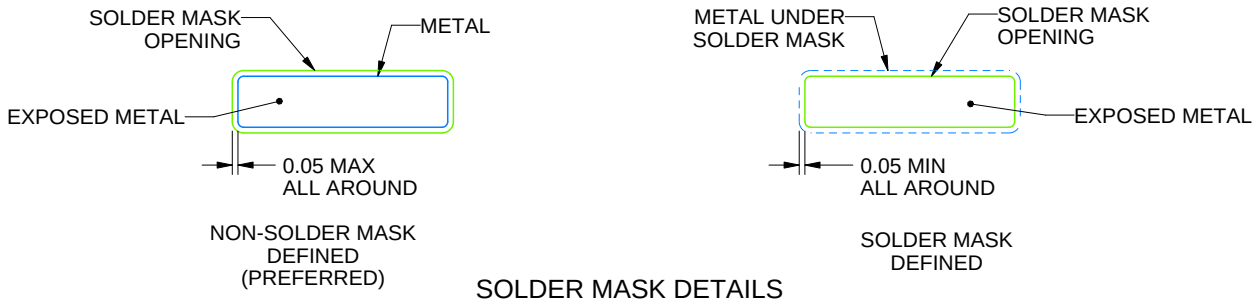


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

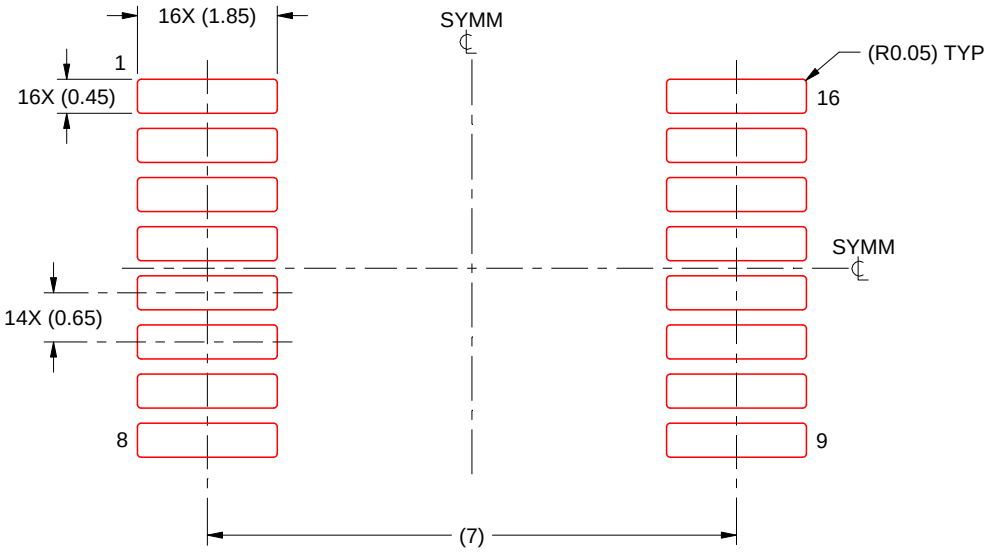
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

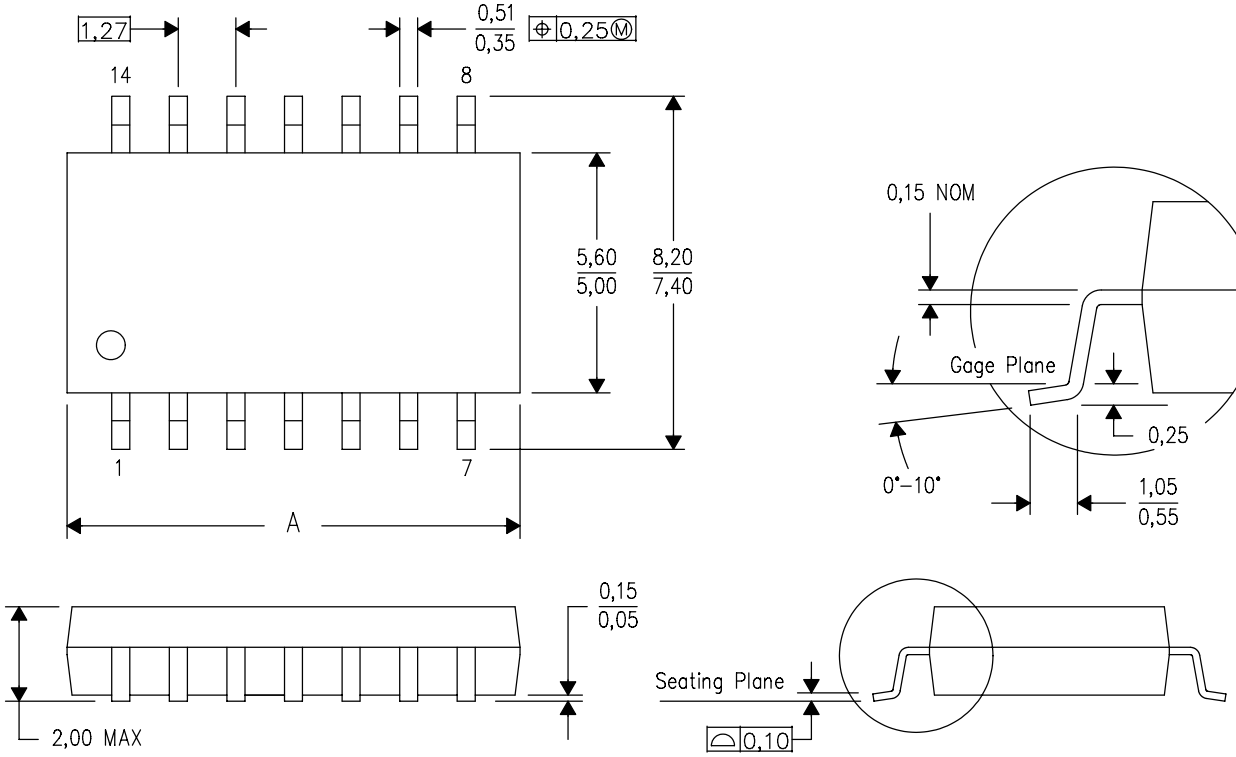
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

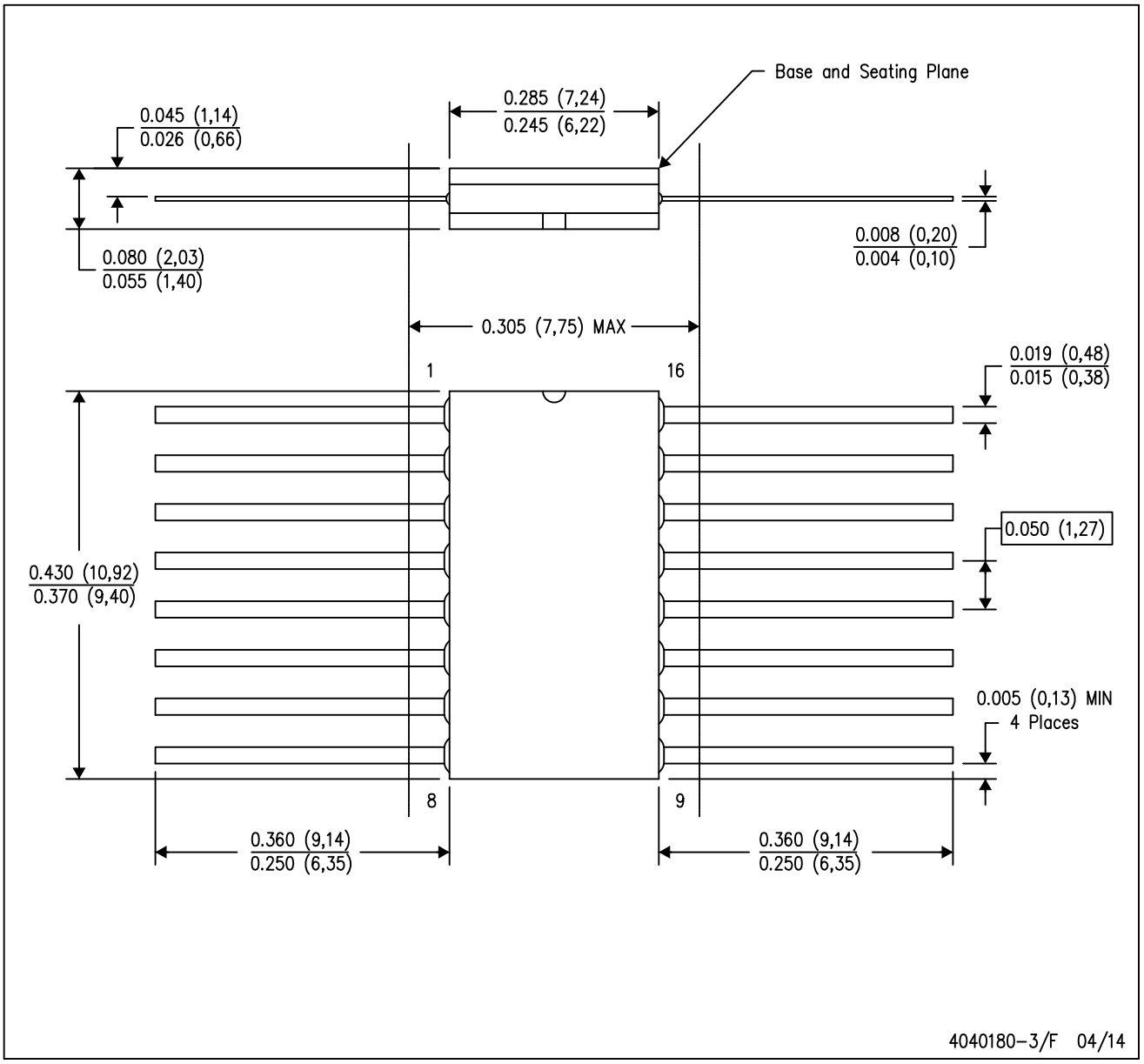


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

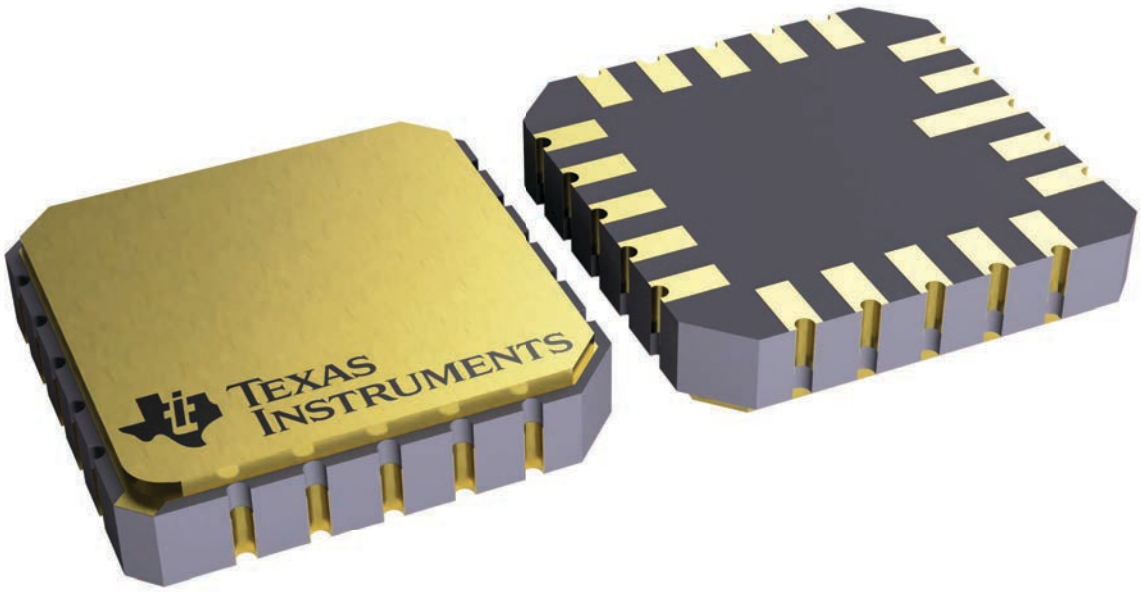
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

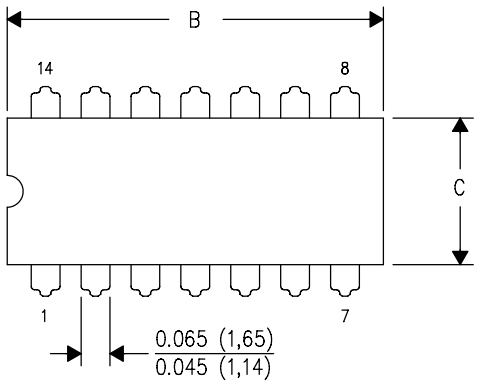


4229370VA\

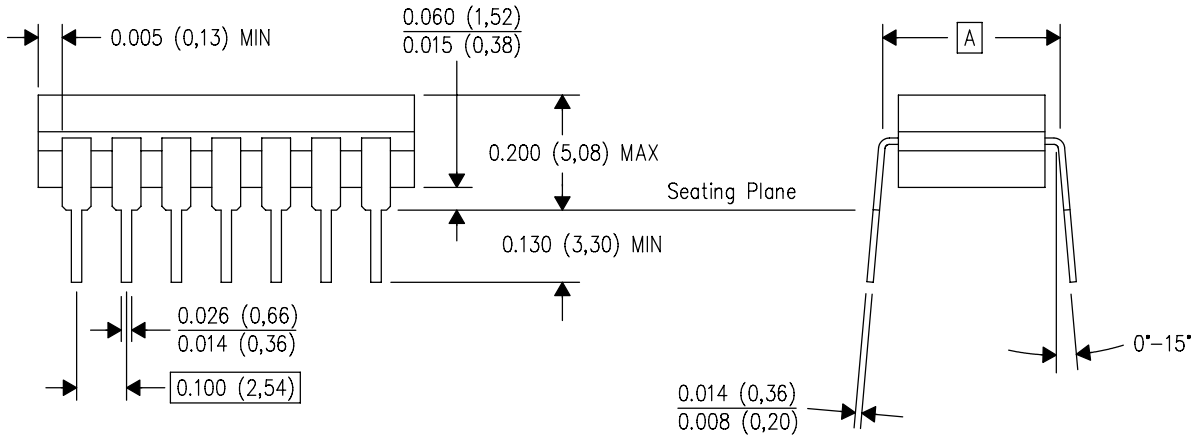
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



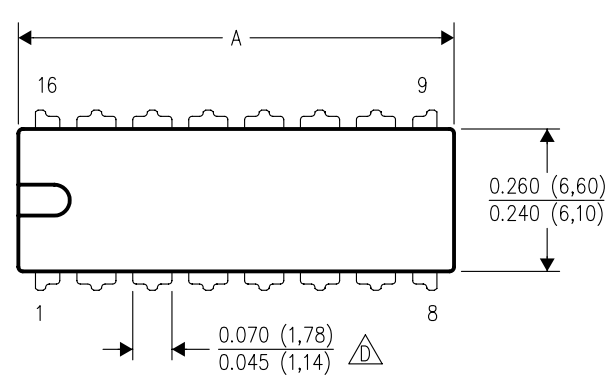
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

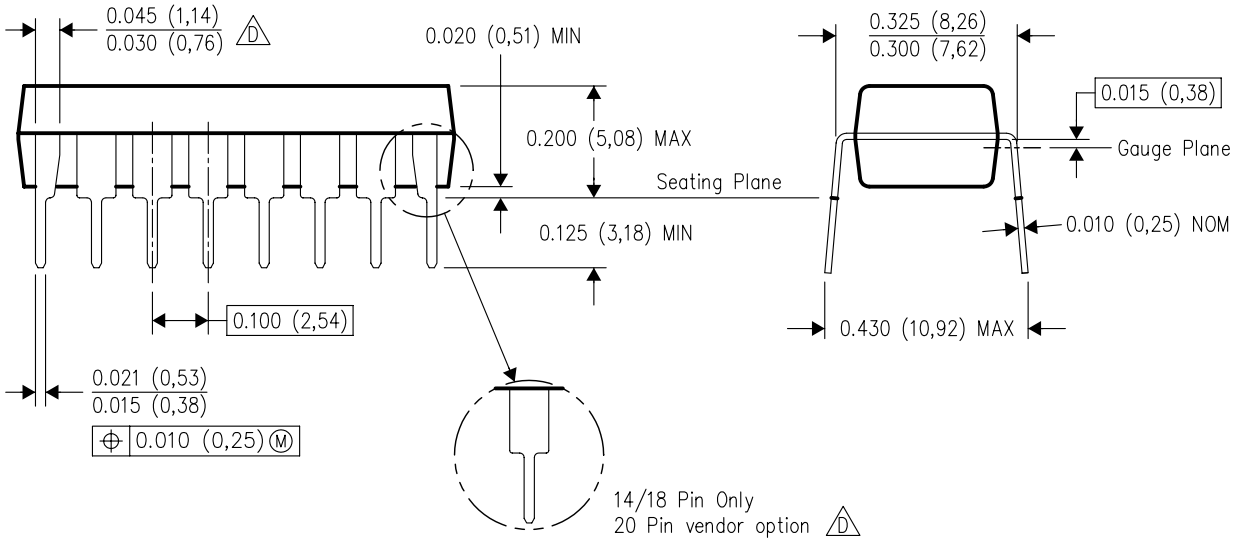
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

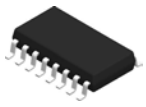


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

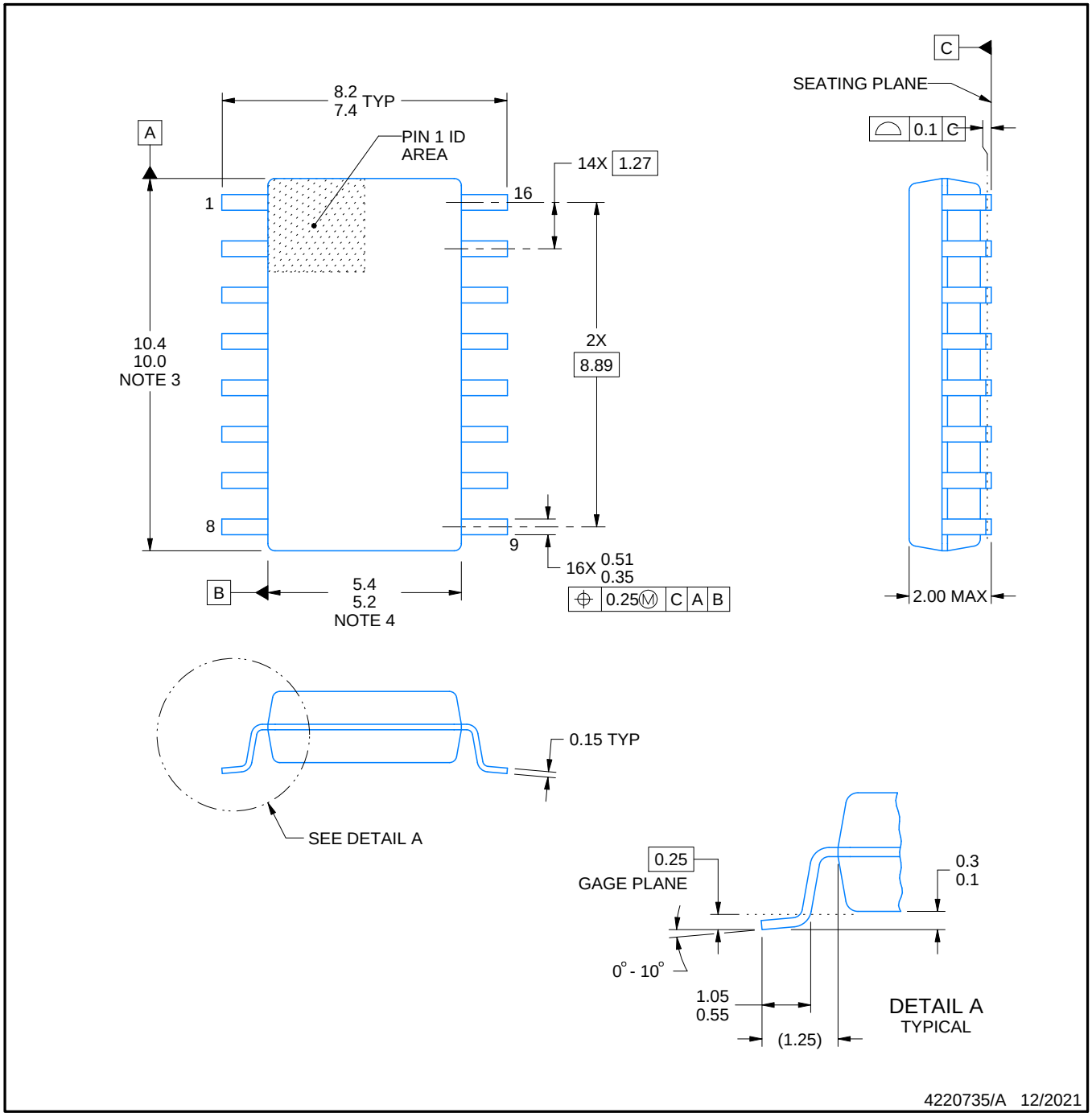


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

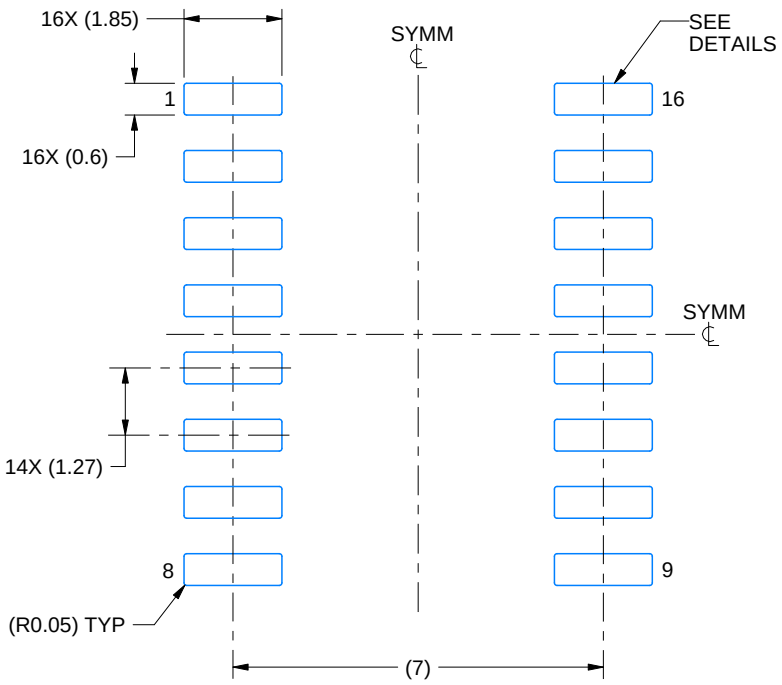
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

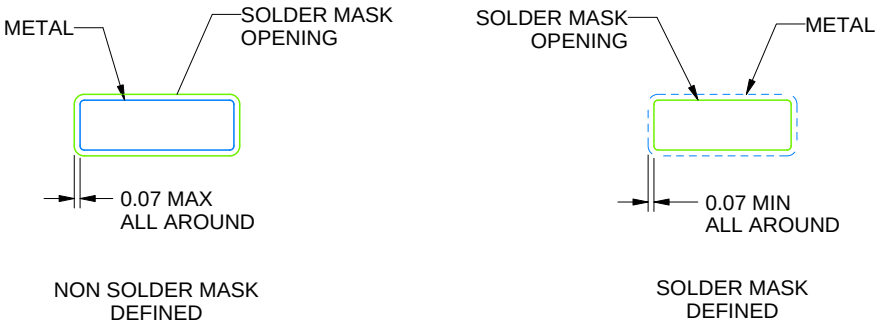
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

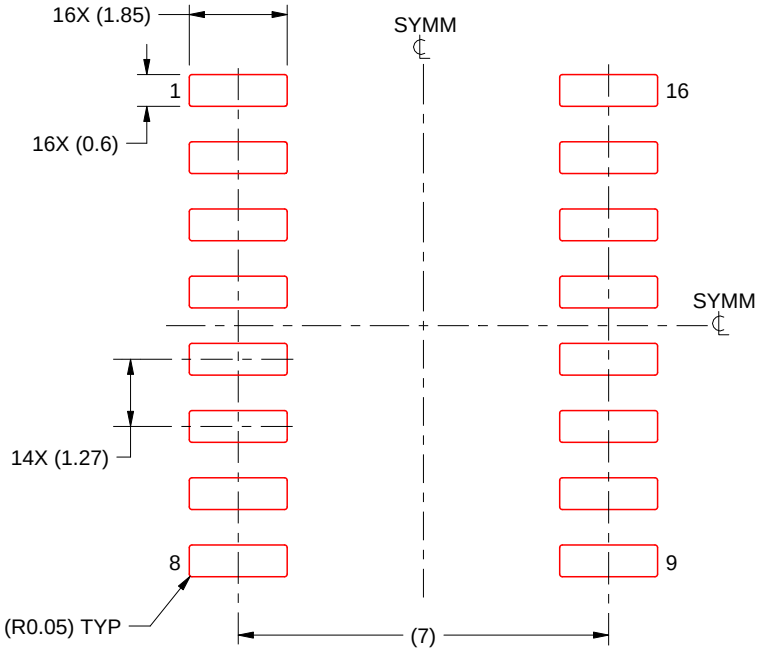
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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