Dual, Wideband, High Output Current Operational Amplifier with Active Off-Line Control

Check for Samples: OPA2673

FEATURES

- **WIDEBAND +12V OPERATION: 340MHz (G = +4V/V)**
- **UNITY-GAIN STABLE: 600MHz (G = +1)**
- **HIGH OUTPUT CURRENT: 700mA**
- **OUTPUT VOLTAGE SWING: 9.8V_{PP}**
- **HIGH SLEW RATE: 3000V/μs**
- **LOW SUPPLY CURRENT: 16mA/ch**
- **OVERTEMPERATURE PROTECTION CIRCUIT**
- **FLEXIBLE POWER CONTROL**
- **OUTPUT CURRENT LIMIT (±800mA)**
- **ACTIVE OFF-LINE FOR TDMA**

APPLICATIONS

- **POWER LINE MODEMS**
- **MATCHED I/Q CHANNEL AMPLIFIERS**
- **BROADBAND VIDEO LINE DRIVERS**
- **ARB LINE DRIVERS**
- **HIGH CAP LOAD DRIVERS**

RELATED PRODUCTS

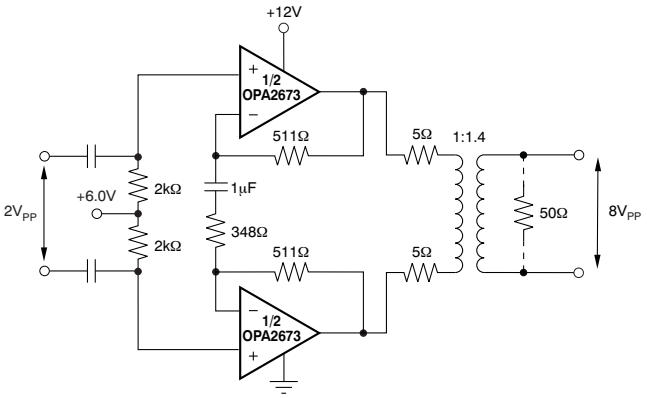
SINGLES	DUALS	TRIPLES	NOTES
OPA691	OPA2691	OPA3691	Single +12V Capable
—	THS6042	—	±15V Capable
—	OPA2677	—	Single +12V Capable
—	OPA2674	—	Single +12V Capable, Output Current Limit

DESCRIPTION

The OPA2673 provides the high output current and low distortion required in emerging Power Line Modem driver applications. Operating on a single +12V supply, the OPA2673 consumes a low 16mA/ch quiescent current to deliver a very high 700mA output current. This output current supports even the most demanding Power Line Modem requirements with greater than 460mA minimum output current (+25°C minimum value) with low harmonic distortion.

Power control features are included to allow system power consumption to be minimized. Two logic control lines allow four quiescent power settings: full power, 75% bias power in applications that are less demanding, 50% bias power cutback for short loops, and offline with active offline control to present a high impedance even with large signals present at the output pin.

Specified on ±6V supplies (to support +12V operation), the OPA2673 also supports up to +13V single or ±6.5V dual supplies. Video applications benefit from a very high output current to drive up to 10 parallel video loads (15Ω) with < 0.1%/0.1° dG/dΦ nonlinearity.



Single-Supply Line Driver

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2673	QFN-16	RGV	–40°C to +85°C	OPA2673	OPA2673IRGVT	Tape and Reel, 250
					OPA2673IRGVR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

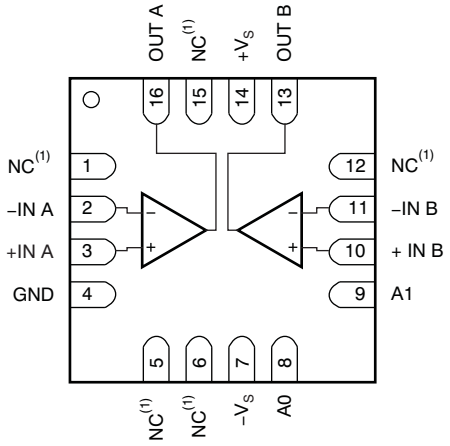
Over operating free-air temperature range (unless otherwise noted).

PARAMETER		OPA2673	UNIT
Power supply		±6.5	V_{DC}
Internal power dissipation		See Thermal Characteristics	
Differential input voltage		±2	V
Input common-mode voltage range		$\pm V_S$	V
Storage temperature range: RGV package		–65 to +125	°C
Junction temperature, T_J		+150	°C
Continuous operating junction temperature		+139	°C
ESD rating:	Human body model (HBM)	2000	V
	Charge device model (CDM)	1500	V
	Machine model (MM)	200	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PIN CONFIGURATION

RGV PACKAGE
QFN-16
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±6V

At T_A = +25°C, A0 = A1 = 0 (full power), G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 76 for ac performance only. Single channel specifications, except where noted.

		OPA2673IRGV						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNIT	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE								
Small-signal bandwidth	G = +1V/V, R_F = 511Ω, V_O = 500mV_{PP}	600				MHz	typ	C
	G = +2V/V, R_F = 475Ω, V_O = 500mV_{PP}	450				MHz	typ	C
	G = +4V/V, R_F = 402Ω, V_O = 500mV_{PP}	340	270	265	260	MHz	min	B
	G = +8V/V, R_F = 250Ω, V_O = 500mV_{PP}	360	270	265	260	MHz	min	B
Peaking at a gain of +1V/V	G = +1V/V, R_F = 511Ω	2				dB	typ	C
Bandwidth for 0.1dB flatness	G = +4V/V, V_O = 500mV_{PP}	50				MHz	typ	C
Large-signal bandwidth	G = +4V/V, V_O = 5V_{PP}	300				MHz	typ	C
Slew rate	G = +4V/V, 5V step	3000	2600	2400	2300	V/µs	min	B
Rise-and-fall time	G = +4V/V, 2V step	1.2				ns	typ	C
Harmonic distortion	G = +4V/V, V_O = 2V_{PP}, 10MHz, R_L = 50Ω							
2nd harmonic	A1 = 0, A0 = 0, full bias	–67	–61	–60	–59	dBc	max	B
	A1 = 0, A0 = 1, 75% bias	–70	–60	–59	–58	dBc	max	B
	A1 = 1, A0 = 0, 50% bias	–69				dBc	typ	C
3rd harmonic	A1 = 0, A0 = 0, full bias	–80	–73	–72	–70	dBc	max	B
	A1 = 0, A0 = 1, 75% bias	–75	–68	–67	–66	dBc	max	B
	A1 = 1, A0 = 0, 50% bias	–68				dBc	typ	C
	G = +4V/V, V_O = 2V_{PP}, 20MHz, R_L = 50Ω							
2nd harmonic	A1 = 0, A0 = 0, full bias	-68	–62	–61	–60	dBc	max	B
	A1 = 0, A0 = 1, 75% bias	-67	–60	–59	–58	dBc	max	B
	A1 = 1, A0 = 0, 50% bias	-65				dBc	typ	C
3rd harmonic	A1 = 0, A0 = 0, full bias	-72	–63	–62	–61	dBc	max	B
	A1 = 0, A0 = 1, 75% bias	-66	–60	–53	–58	dBc	max	B
	A1 = 1, A0 = 0, 50% bias	-60				dBc	typ	C
Input voltage noise	f > 1MHz	2.4	2.8	3.2	3.6	nV/√Hz	max	B
Noninverting input current noise	f > 1MHz	5.2	5.8	5.3	6.0	pA/√Hz	max	B
Inverting input current noise	f > 1MHz	35	40	42	43	pA/√Hz	max	B
Differential gain error	NTSC, R_L = 150Ω	0.03				%	typ	C
	NTSC, R_L = 37.5Ω	0.05				%	typ	C
Differential phase error	NTSC, R_L = 150Ω	0.01				degrees	typ	C
	NTSC, R_L = 37.5Ω	0.04				degrees	typ	C
Channel-to-channel crosstalk (QFN-16)	f = 5MHz, Input-referred	–92				dBc	typ	C
DC PERFORMANCE[4]								
Open-loop transimpedance gain (Z_{OL})	Differential, V_O = 0V, R_L = 100Ω	90	**60**	56	55	kΩ	min	A
Input offset voltage, full bias	V_{CM} = 0V	±2	**±7**	±8	±9	mV	max	A
Average offset drift, full bias	V_{CM} = 0V			±25	±30	µV/°C	max	B
Input offset voltage matching, full bias	V_{CM} = 0V	±0.5	**±2**	±2.5	±2.5	mV	max	A
Input offset voltage, 75% bias	V_{CM} = 0V	±2	±7	±8	±9	mV	max	B
Input offset voltage, 50% bias	V_{CM} = 0V	±2	±7	±8	±9	mV	max	B

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +18°C at high temperature limit for over temperature specifications.
(4) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, A0 = A1 = 0 (full power), G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 76 for ac performance only. Single channel specifications, except where noted.

		OPA2673IRGV						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNIT	MIN/ MAX	TEST LEVEL[1]
DC PERFORMANCE (continued)								
Noninverting input bias current	V_{CM} = 0V	±5	**±25**	±27	±28	µA	max	A
Noninverting input bias current drift	V_{CM} = 0V			±45	±47	µA/°C	max	B
Noninverting input bias current matching	V_{CM} = 0V	±0.5	**±5**	±6	±7	µA	max	A
Inverting input bias current	V_{CM} = 0V	±6	**±48**	±52	±55	µA	max	A
Inverting input bias current drift	V_{CM} = 0V			±90	±110	µA/°C	max	B
Inverting input bias current matching	V_{CM} = 0V	±6	**±25**	±30	±30	µA	max	A
INPUT[5]								
Common-mode input range[6]		±3.6	**±3.5**	±3.3	±3.2	V	min	A
Common-mode rejection ratio	V_{CM} = 0V, Input-referred	56	**50**	48	47	dB	min	A
Noninverting input impedance		1.5 || 1.5				MΩ || pF	typ	C
Inverting input resistance	Open-loop	32	16			Ω	min	B
Inverting input resistance	Open-loop	32	40			Ω	max	B
Shutdown isolation	G = +4V/V, f = 1MHz, $A_1 = A_0$ = 1	85				dB	typ	C
OUTPUT								
Voltage output swing	No load	±4.9	**±4.8**	±4.75	±4.7	V	min	A
	100Ω load	±4.8	±4.75	±4.7	±4.65	V	min	B
	25Ω load	±4.7	**±4.5**	±4.45	±4.4	V	min	A
Output current at full power (peak)	R_L = 4Ω, A1 = 0, A0 = 0	±700	**±460**	±440	±425	mA	min	A
Output current at 75% bias (peak)	R_L = 4Ω, A1 = 0, A0 = 1	±500	**±350**	±325	±300	mA	min	A
Output current at 50% bias (peak)	R_L = 4Ω, A1 = 1, A0 = 0	±180	**±120**	±115	±110	mA	min	A
Short-cIrcuit current	V_O = 0V	±800				mA	typ	C
Closed-loop output impedance at full power	G = +4V/V, f ≤ 100kHz, A1 = 0, A0 = 0	0.01				Ω	typ	C
Closed-loop output impedance at 75% bias	G = +4V/V, f ≤ 100kHz, A1 = 0, A0 = 1	0.01				Ω	typ	C
Closed-loop output impedance at 50% bias	G = +4V/V, f ≤ 100kHz, A1 = 1, A0 = 0	0.01				Ω	typ	C
Output impedance at shutdown		25 || 4				kΩ || pF	typ	C
Output switching glitch	Inputs at GND	±20				mV	typ	C
POWER CONTROL								
Maximum logic 0	A1, A0, V_S = ±6V		**0.8**	0.8	0.8	V	max	A
Minimum logic 1	A1, A0, V_S = ±6V		**2**	2	2	V	min	A
Logic input current	A0, A1 = 0, each line	6	**8**	9	10	µA	max	A
	A0, A1 = 1, each line	–50	**–110**	–125	–150	µA	min	A

(5) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.
(6) Tested < 3dB below minimum CMRR specifications at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, A0 = A1 = 0 (full power), G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 76 for ac performance only. Single channel specifications, except where noted.

PARAMETER	CONDITIONS	OPA2673IRGV				UNIT	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
POWER SUPPLY								
Specified operating voltage		±6				V	typ	C
Maximum operating voltage			**±6.5**	±6.5	±6.5	V	max	A
Minimum operating voltage (dual supply)		±3.5				V	typ	C
Minimum operating voltage (single supply)		+5.75				V	typ	C
Maximum quiescent current at full power	V_S = ±6V, Total both channels, A1 = 0, A0 = 0	32	**38**	40	42	mA	max	A
Minimum quiescent current at full power	V_S = ±6V, Total both channels, A1 = 0, A0 = 0	32	**26**	25	24	mA	min	A
Supply current at 75% bias	V_S = ±6V, Total both channels, A1 = 0, A0 = 1	24	**29**	31	33	mA	max	A
Supply current at 50% bias	V_S = ±6V, Total both channels, A1 = 1, A0 = 0	16	**19**	20	21	mA	max	A
Supply current (off-line)	V_S = ±6V, Total both channels, A1 = 1, A0 = 1	5.5	**7**	7.5	8	mA	max	A
Supply current step time								
Power-supply rejection ratio (–PSRR)	Input-referred	54	**49**	48	47	dB	min	A
THERMAL CHARACTERISTICS								
Specified operating temperature range	IRGV package	–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
RGV QFN-16	PowerPAD soldered to PCB	45				°C/W	typ	C
	PowerPAD floating(7)	75						

(7) PowerPad is physically connected to the negative ($-V_S$) supply for dual-supply configuration or ground (GND) for single-supply configuration.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

SMALL-SIGNAL FREQUENCY RESPONSE

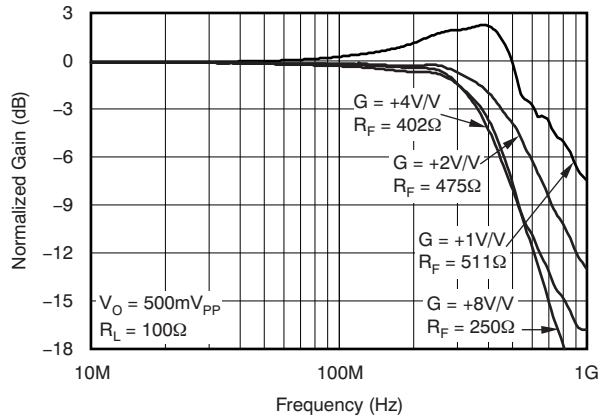


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE OVER POWER SETTINGS

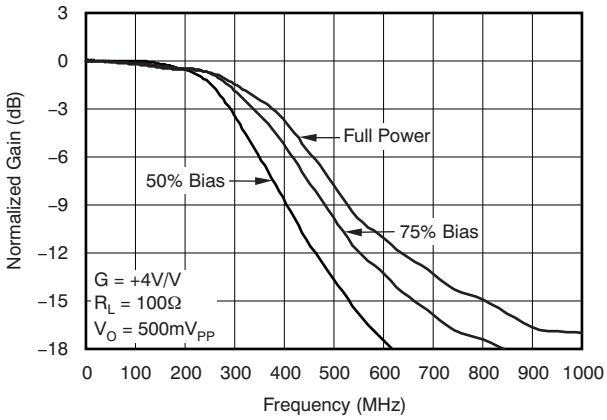


Figure 2.

LARGE-SIGNAL FREQUENCY RESPONSE

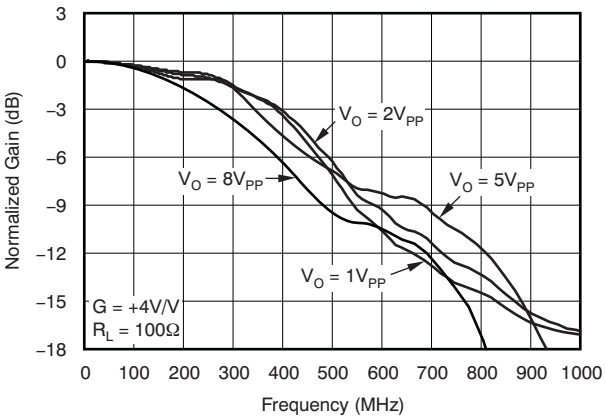


Figure 3.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSES

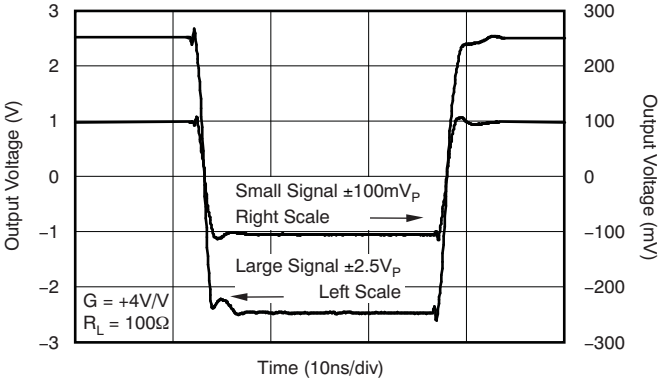


Figure 4.

CHANNEL-TO-CHANNEL CROSSTALK

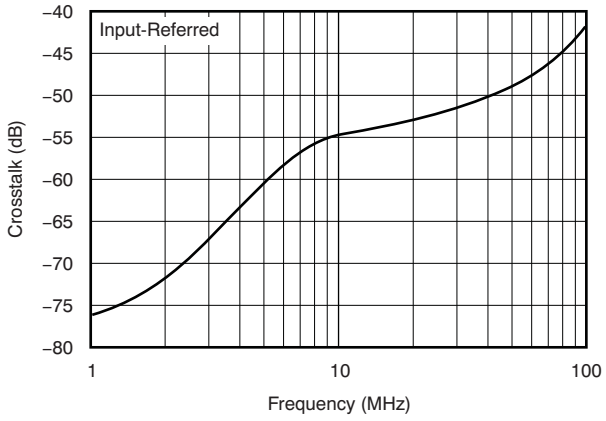


Figure 5.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

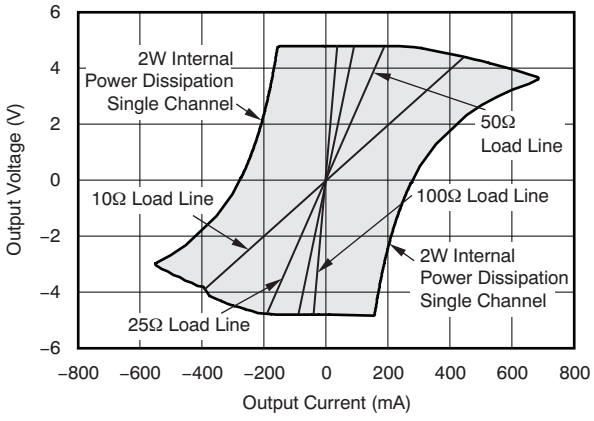


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

HARMONIC DISTORTION vs FREQUENCY

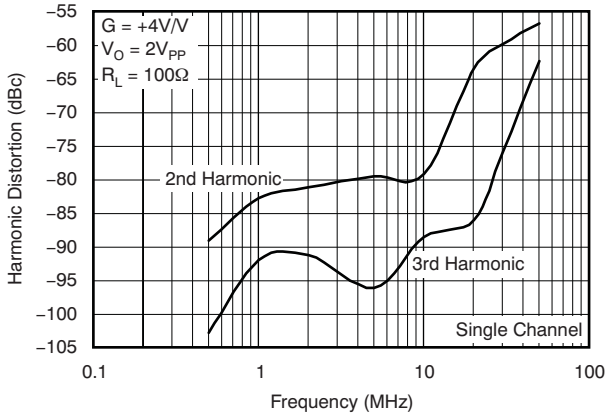


Figure 7.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

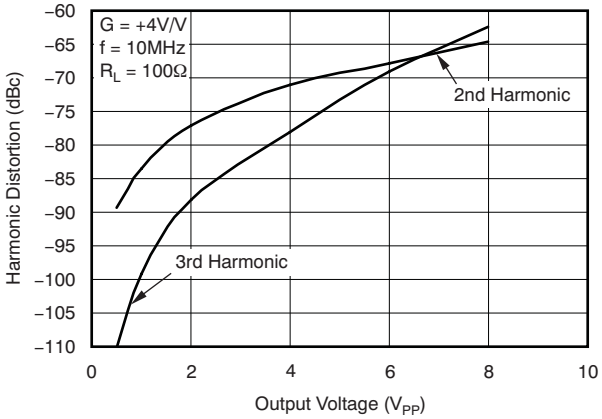


Figure 8.

HARMONIC DISTORTION vs LOAD RESISTANCE

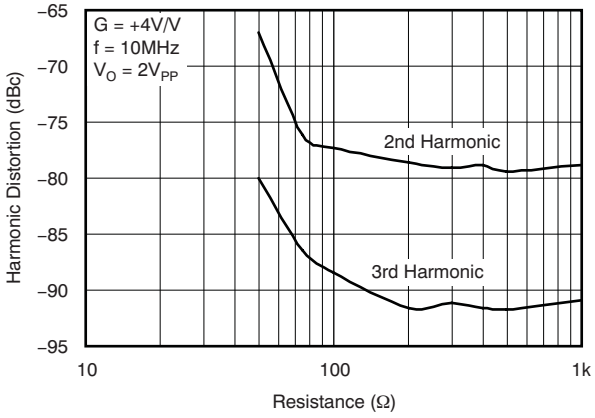


Figure 9.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

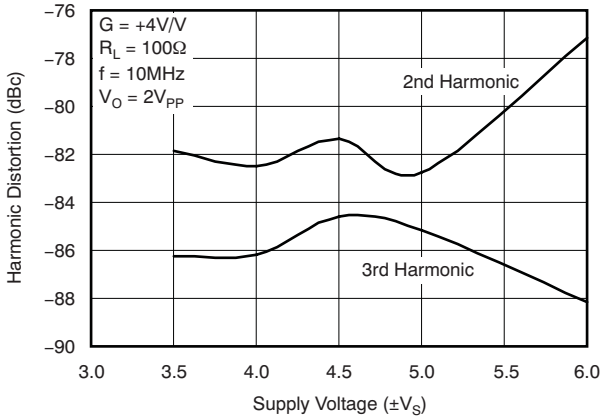


Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

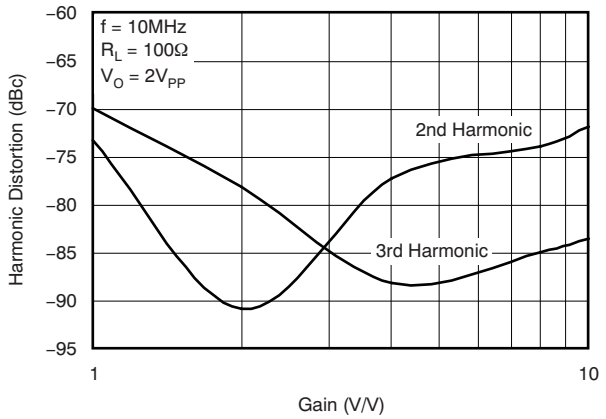


Figure 11.

TWO-TONE, THIRD-ORDER INTERMODULATION INTERCEPT

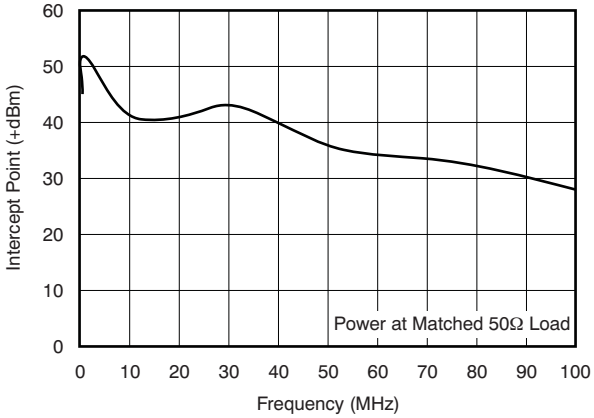


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

OVERDRIVE RECOVERY

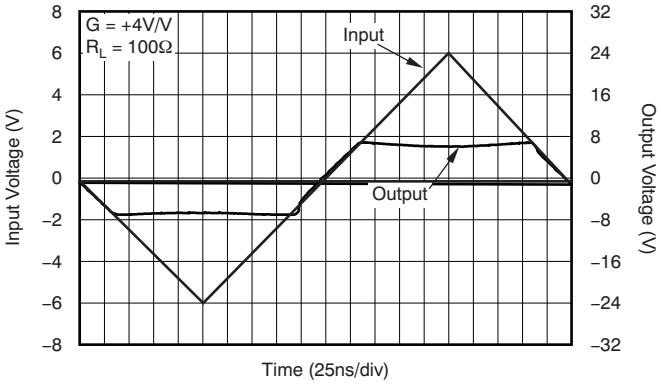


Figure 13.

CMRR AND PSRR vs FREQUENCY

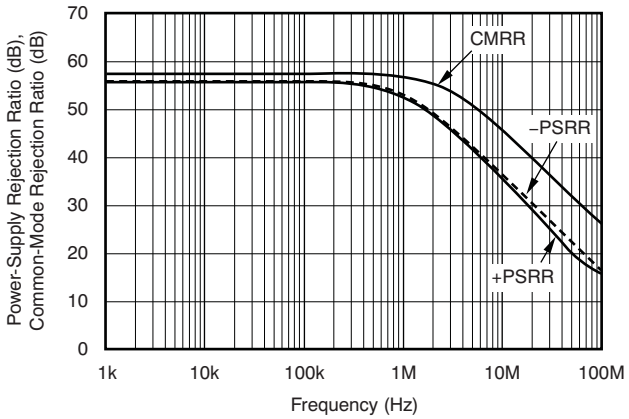


Figure 14.

OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE

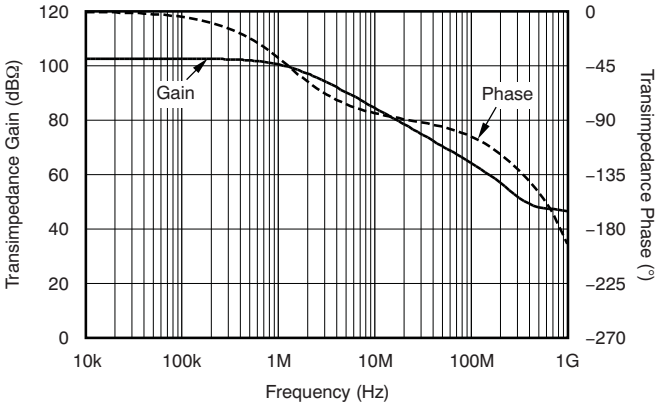


Figure 15.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

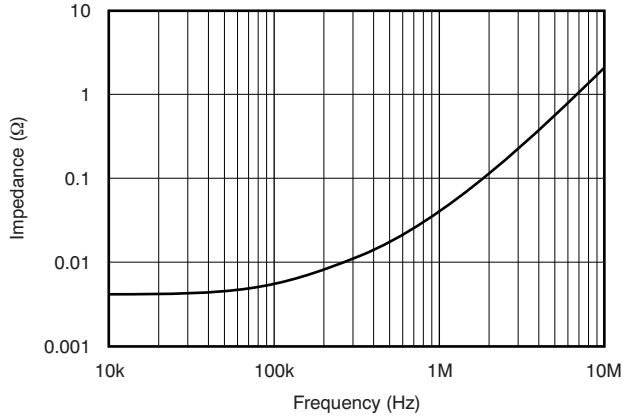


Figure 16.

ACTIVE OFF-LINE IMPEDANCE vs FREQUENCY

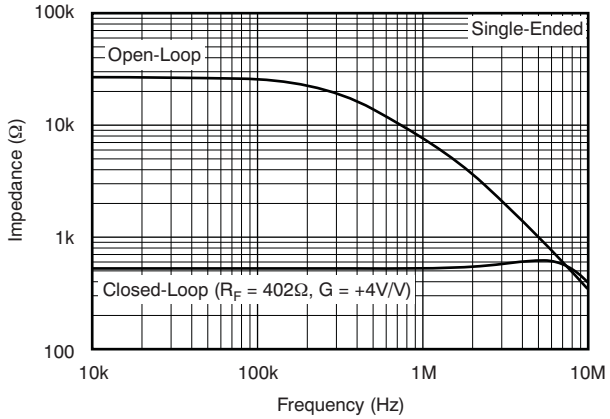


Figure 17.

COMMON-MODE INPUT VOLTAGE RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE

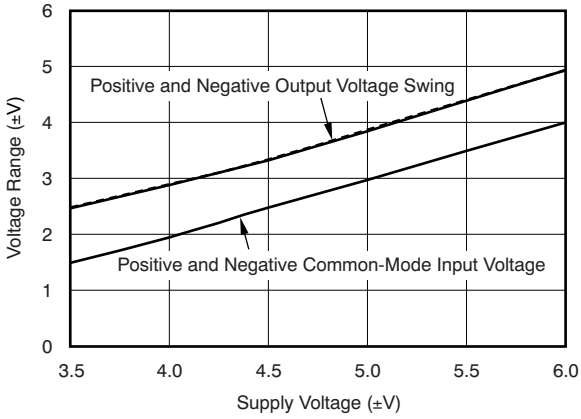


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

COMPOSITE VIDEO (dG/dϕ)

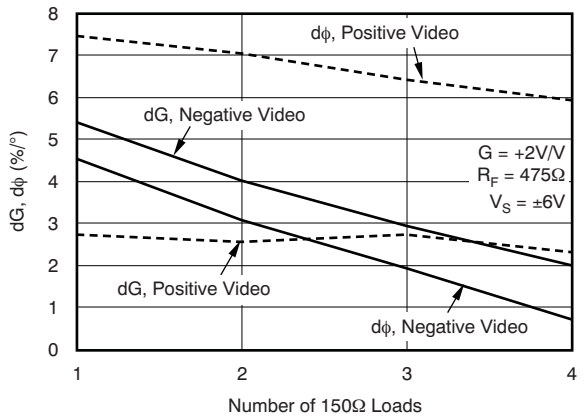


Figure 19.

TYPICAL DC DRIFT OVER TEMPERATURE

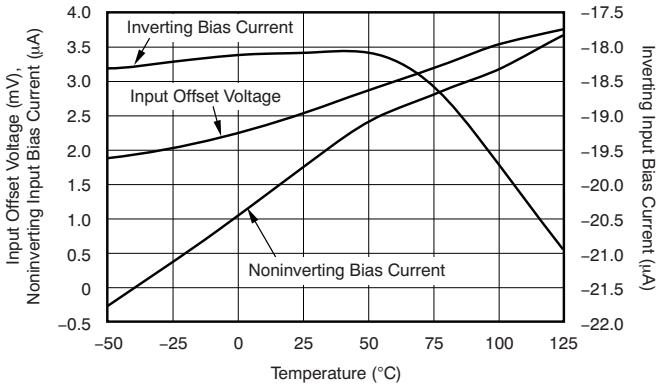


Figure 20.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

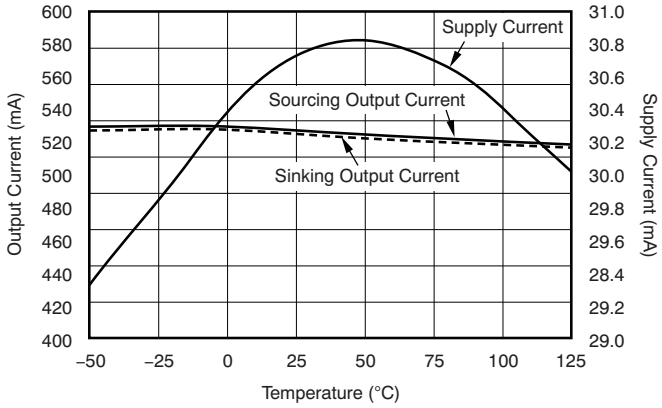


Figure 21.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

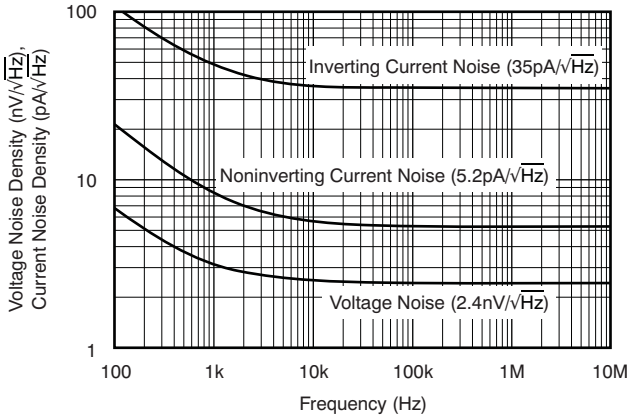


Figure 22.

TYPICAL CHARACTERISTICS: V_S = ±6V Differential, Full Bias

At T_A = +25°C, R_F = 511Ω, R_L = 100Ω Differential, G_{DIFF} = +4V/V, and G_{CM} = +1V/V, unless otherwise specified.

SMALL-SIGNAL FREQUENCY RESPONSE

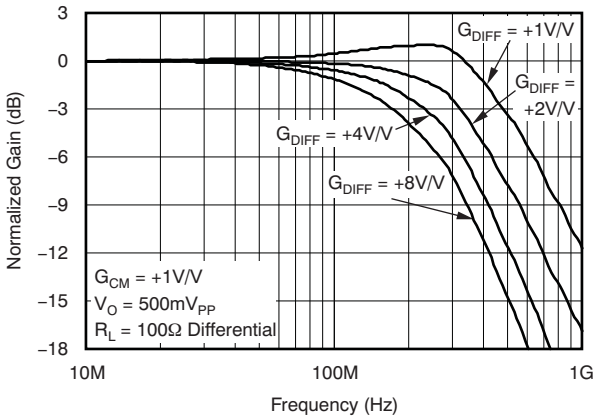


Figure 23.

SMALL-SIGNAL FREQUENCY RESPONSE OVER POWER SETTING

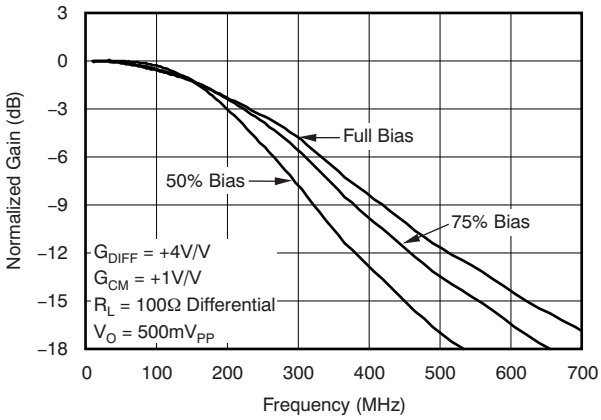


Figure 24.

LARGE-SIGNAL FREQUENCY RESPONSE

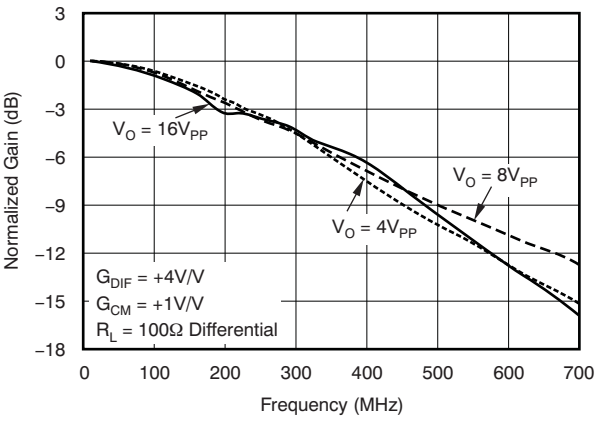


Figure 25.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSES

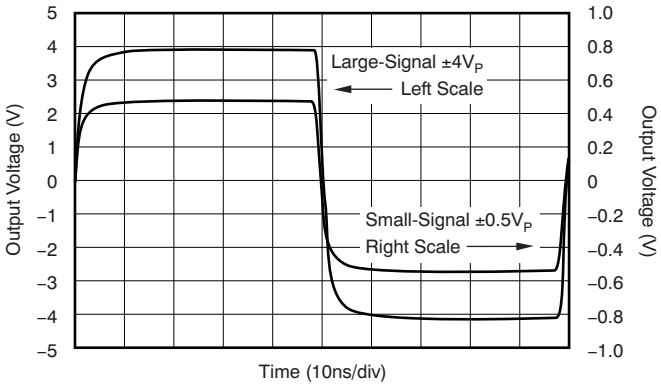


Figure 26.

DIFFERENTIAL R_S vs CAPACITIVE LOAD

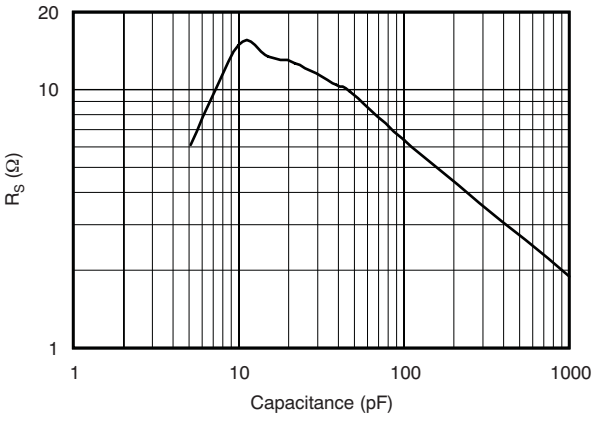


Figure 27.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

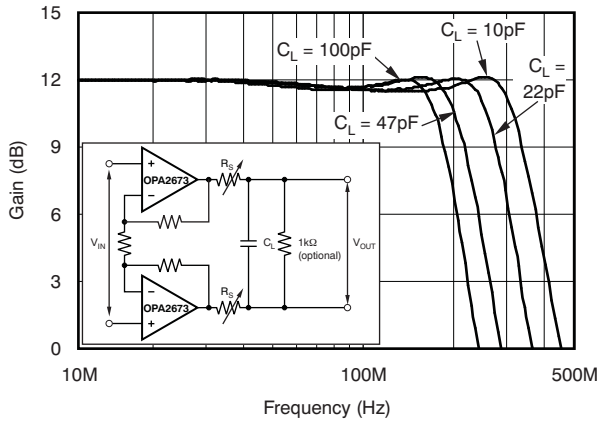


Figure 28.

TYPICAL CHARACTERISTICS: V_S = ±6V Differential, Full Bias (continued)

At T_A = +25°C, R_F = 511Ω, R_L = 100Ω Differential, G_{DIFF} = +4V/V, and G_{CM} = +1V/V, unless otherwise specified.

HARMONIC DISTORTION vs FREQUENCY

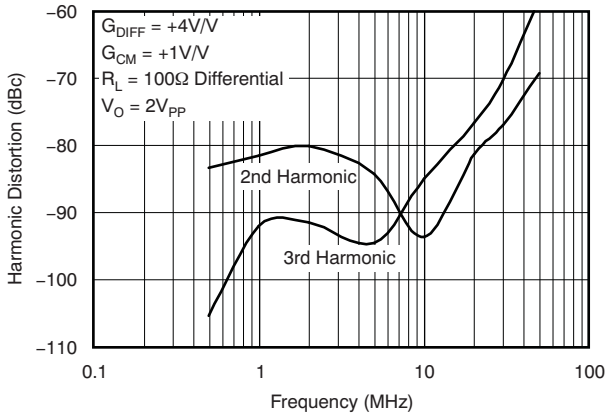


Figure 29.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

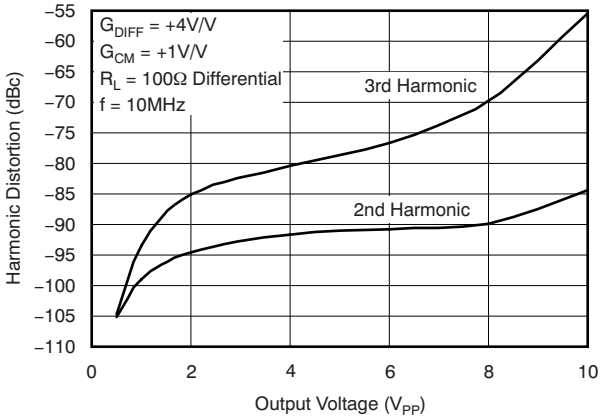


Figure 30.

HARMONIC DISTORTION vs LOAD RESISTANCE

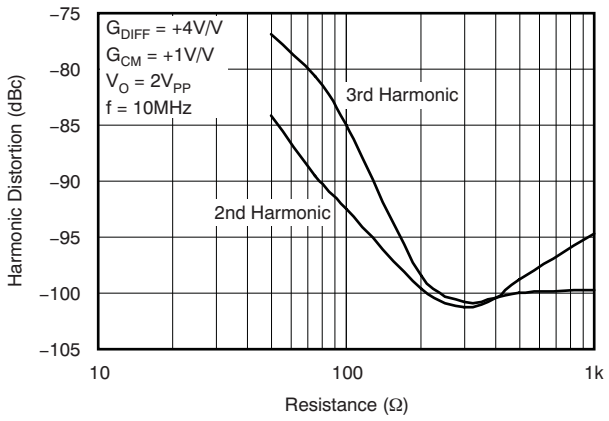


Figure 31.

HARMONIC DISTORTION vs NONINVERTING GAIN

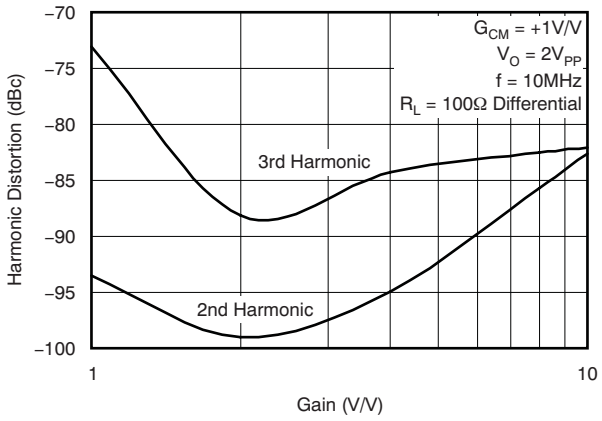


Figure 32.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

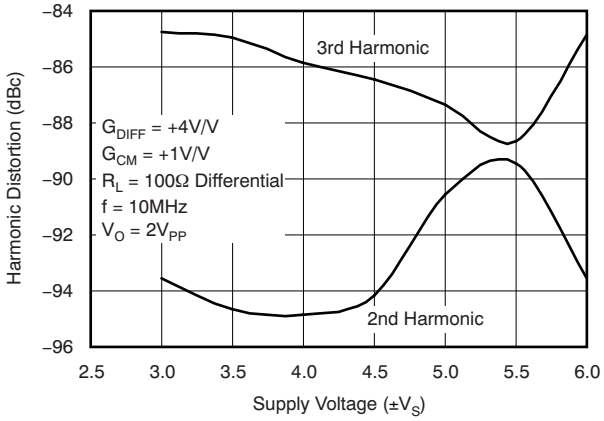


Figure 33.

TYPICAL CHARACTERISTICS: V_S = ±6V, 75% Bias

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

SMALL-SIGNAL FREQUENCY RESPONSE

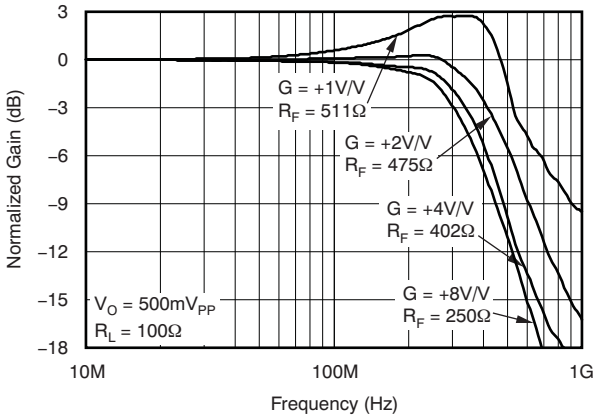


Figure 34.

LARGE-SIGNAL FREQUENCY RESPONSE

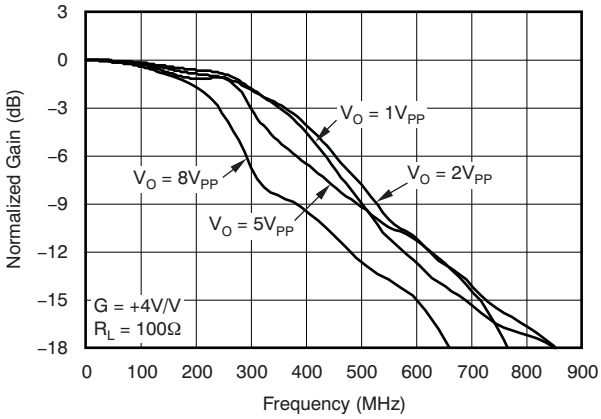


Figure 35.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSES

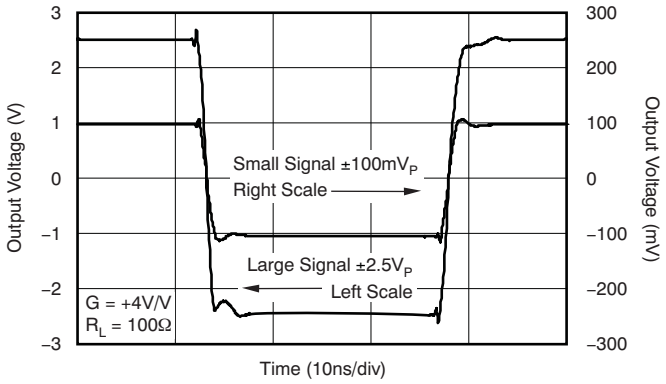


Figure 36.

OVERDRIVE RECOVERY

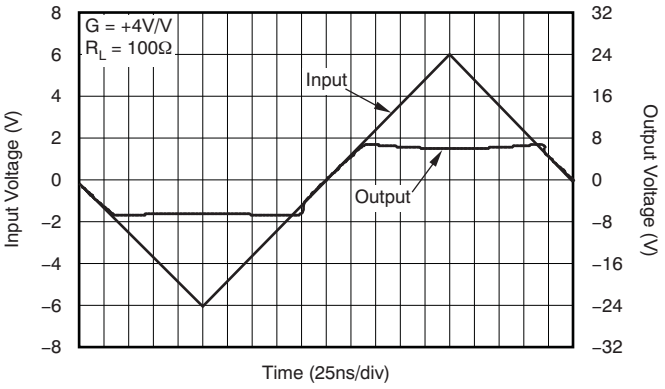


Figure 37.

COMPOSITE VIDEO (dG/dϕ)

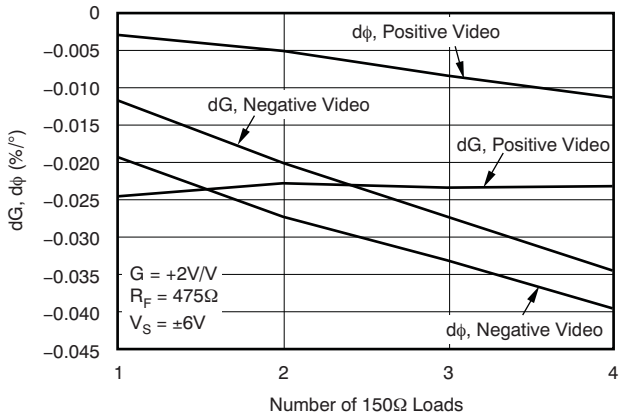


Figure 38.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

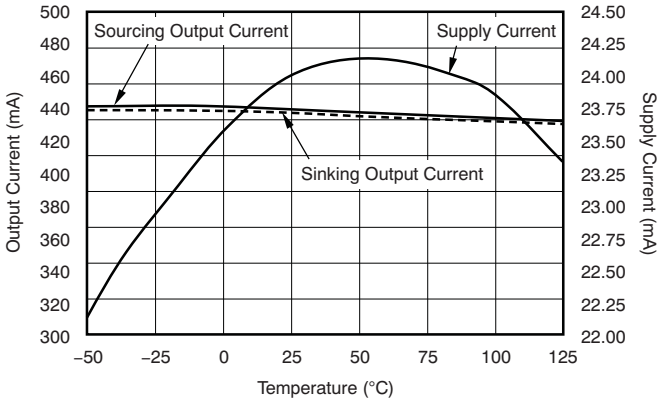


Figure 39.

TYPICAL CHARACTERISTICS: V_S = ±6V, 75% Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

HARMONIC DISTORTION vs FREQUENCY

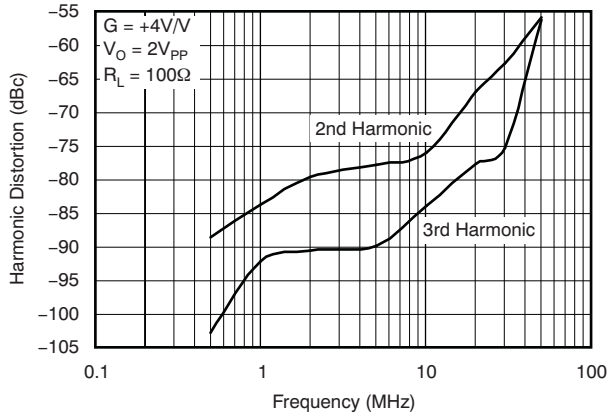


Figure 40.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

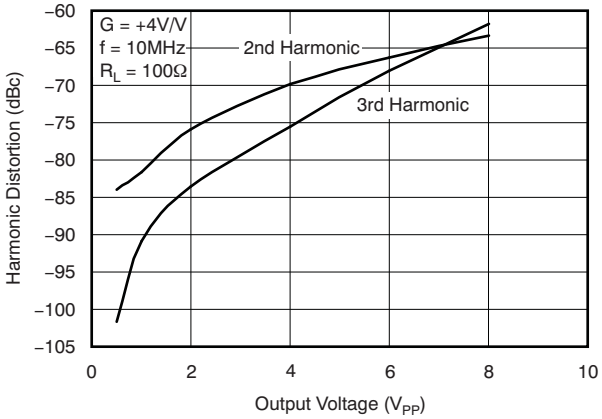


Figure 41.

HARMONIC DISTORTION vs LOAD RESISTANCE

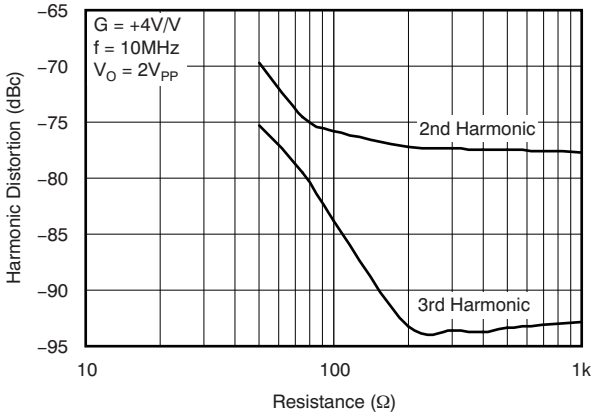


Figure 42.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

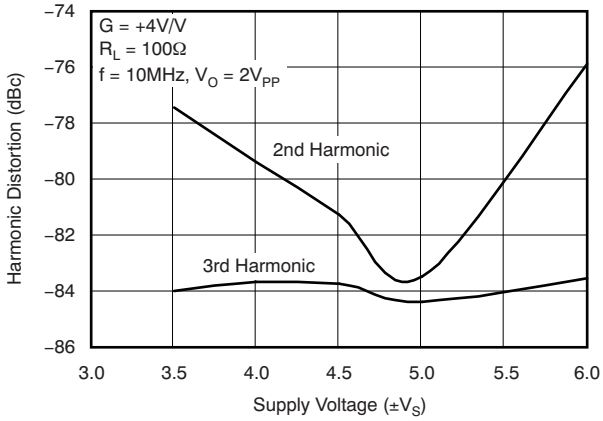


Figure 43.

HARMONIC DISTORTION vs NONINVERTING GAIN

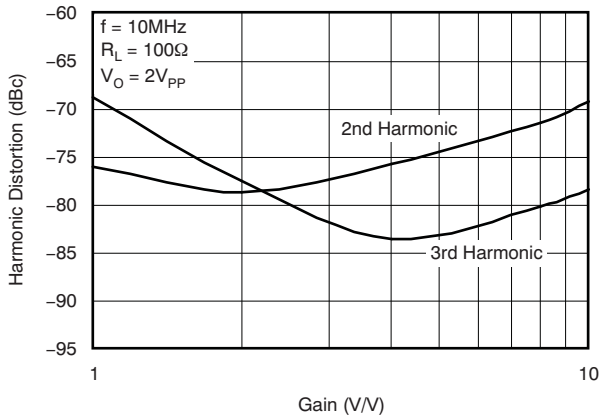


Figure 44.

TWO-TONE, THIRD-ORDER INTERMODULATION INTERCEPT

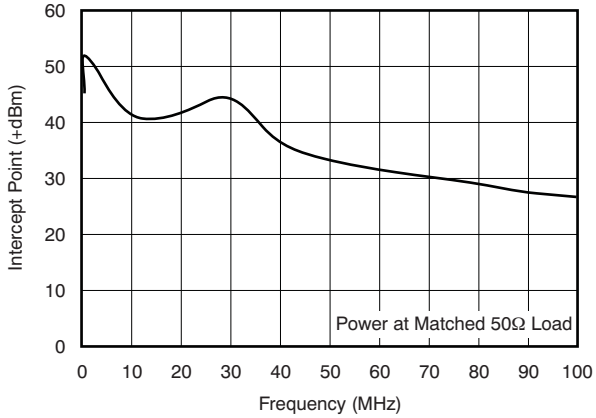


Figure 45.

TYPICAL CHARACTERISTICS: V_S = ±6V, 75% Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

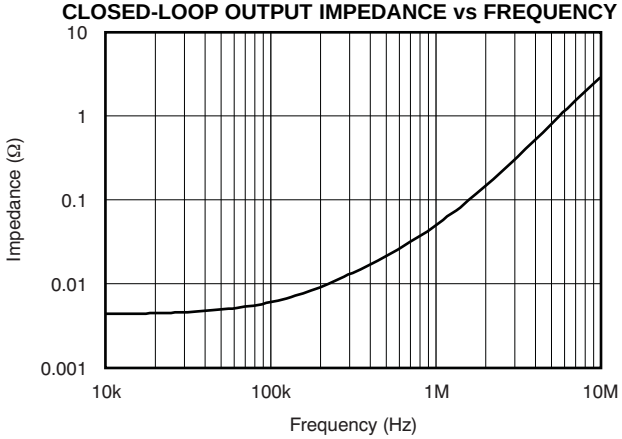


Figure 46.

TYPICAL CHARACTERISTICS: V_S = ±6V Differential, 75% Bias

At T_A = +25°C, R_F = 511Ω, R_L = 100Ω Differential, G_{DIFF} = +4V/V, and G_{CM} = +1V/V, unless otherwise specified.

SMALL-SIGNAL FREQUENCY RESPONSE

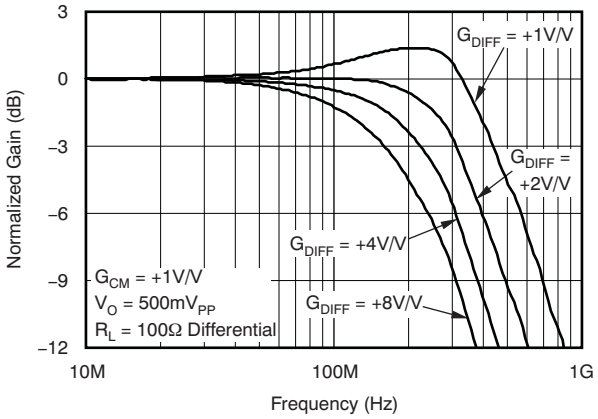


Figure 47.

LARGE-SIGNAL FREQUENCY RESPONSE

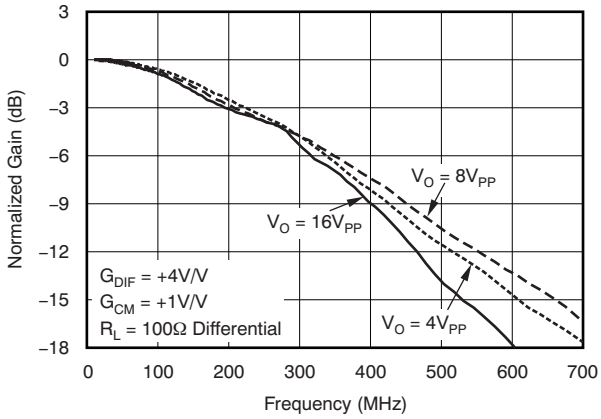


Figure 48.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSES

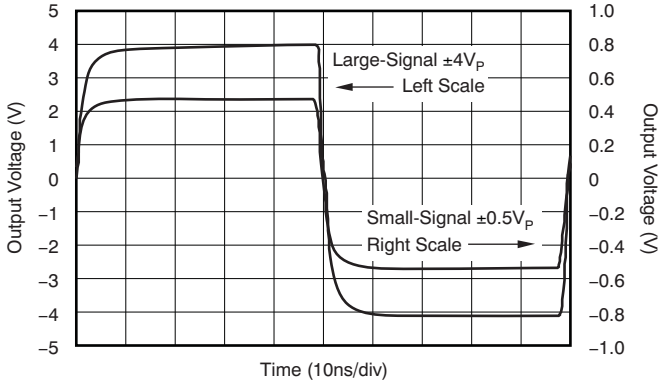


Figure 49.

HARMONIC DISTORTION vs FREQUENCY

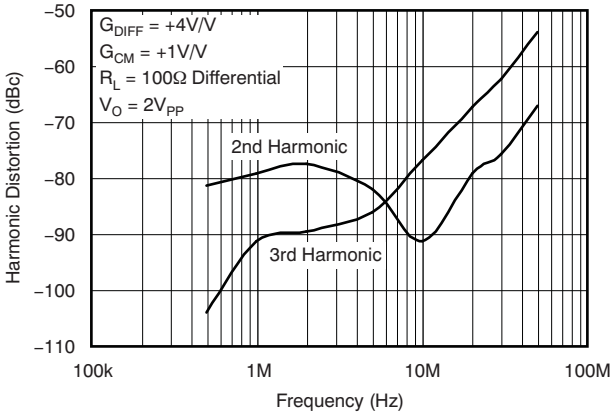


Figure 50.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

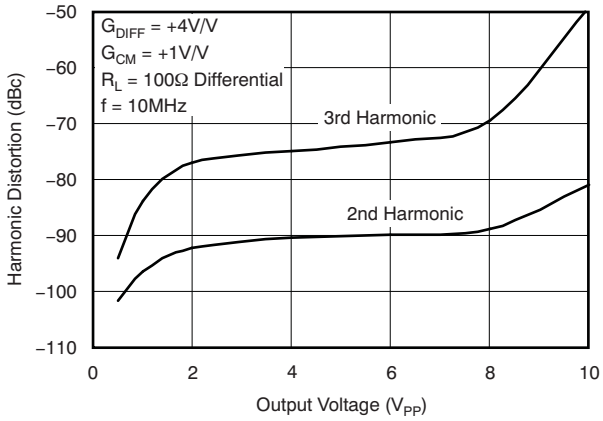


Figure 51.

HARMONIC DISTORTION vs LOAD RESISTANCE

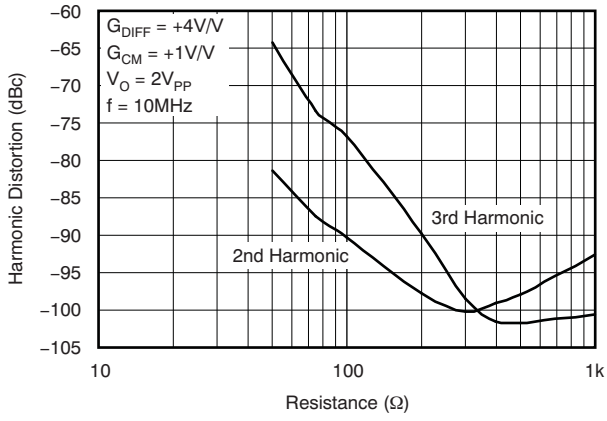


Figure 52.

TYPICAL CHARACTERISTICS: V_S = ±6V Differential, 75% Bias (continued)

At T_A = +25°C, R_F = 511Ω, R_L = 100Ω Differential, G_{DIFF} = +4V/V, and G_{CM} = +1V/V, unless otherwise specified.

HARMONIC DISTORTION vs NONINVERTING GAIN

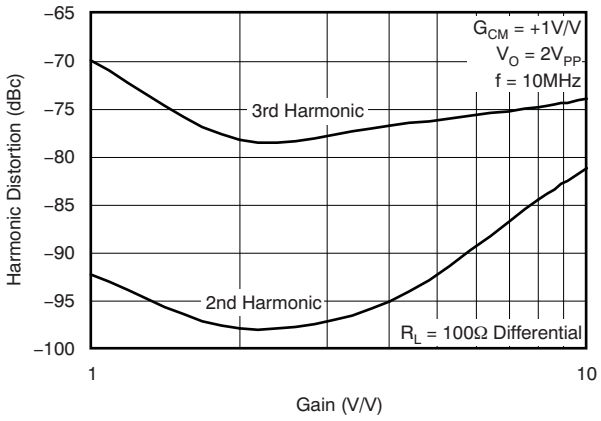


Figure 53.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

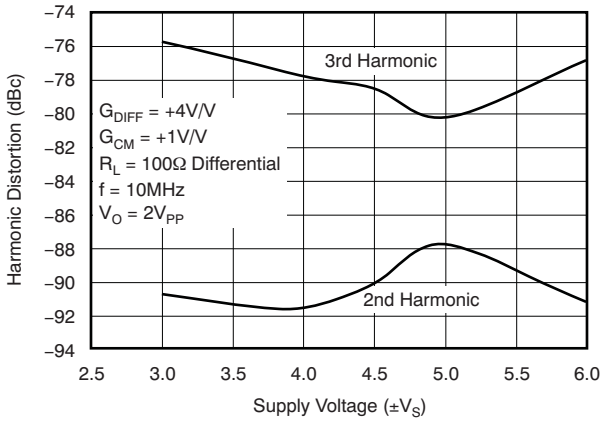


Figure 54.

TYPICAL CHARACTERISTICS: V_S = ±6V, 50% Bias

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

SMALL-SIGNAL FREQUENCY RESPONSE

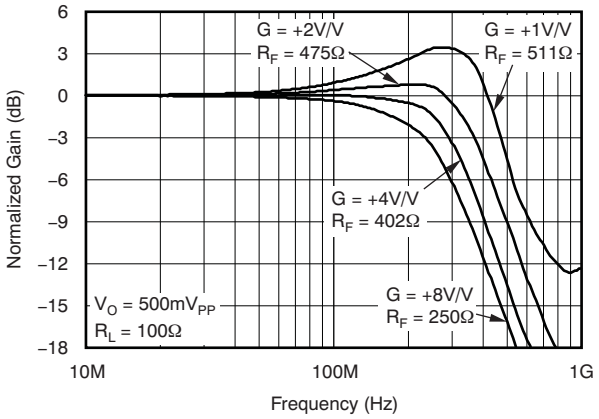


Figure 55.

LARGE-SIGNAL FREQUENCY RESPONSE

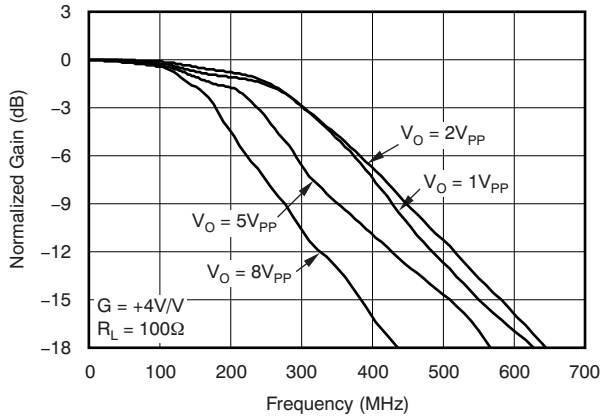


Figure 56.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSES

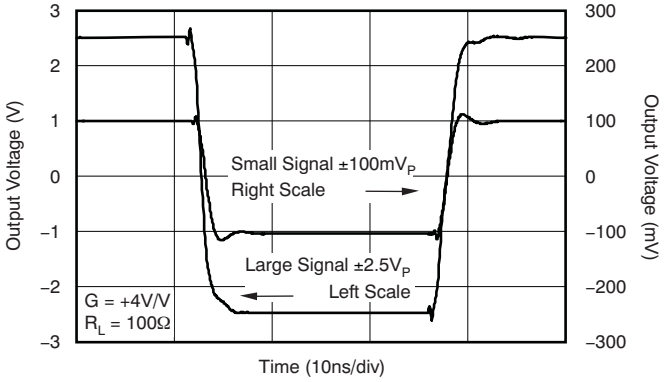


Figure 57.

OVERDRIVE RECOVERY

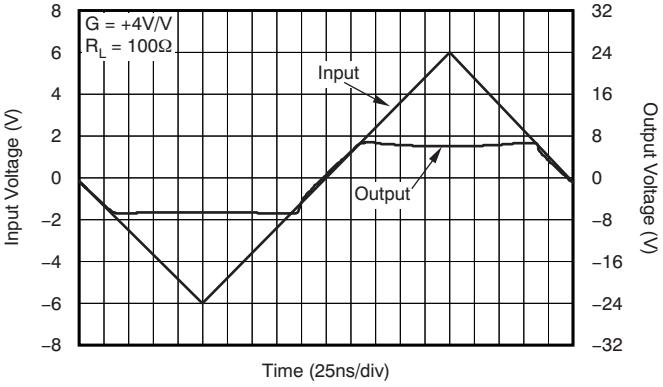


Figure 58.

COMPOSITE VIDEO (dG/dϕ)

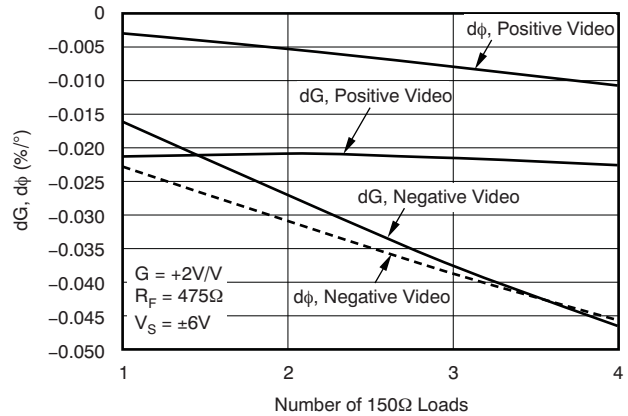


Figure 59.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

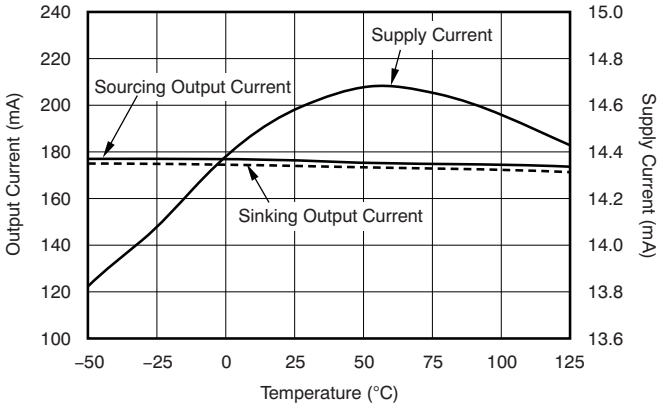


Figure 60.

TYPICAL CHARACTERISTICS: V_S = ±6V, 50% Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

HARMONIC DISTORTION vs FREQUENCY

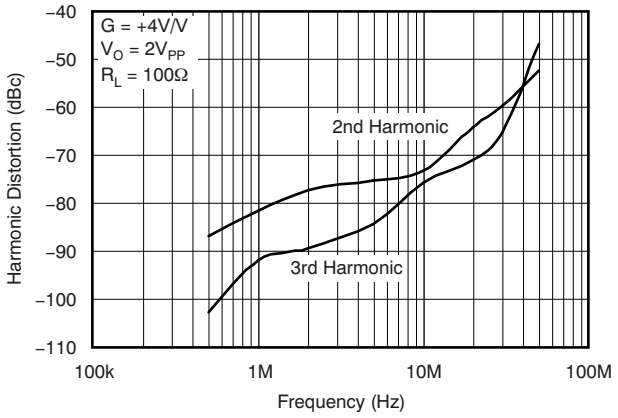


Figure 61.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

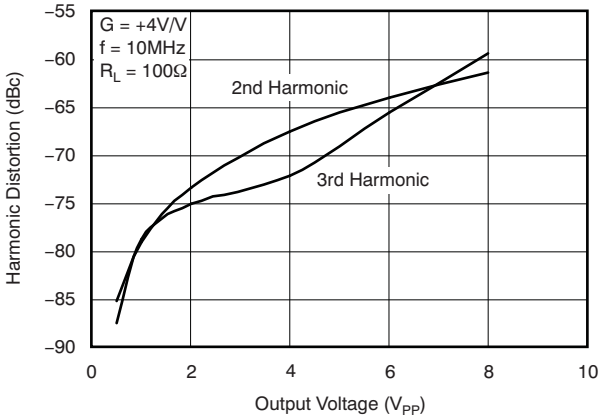


Figure 62.

HARMONIC DISTORTION vs LOAD RESISTANCE

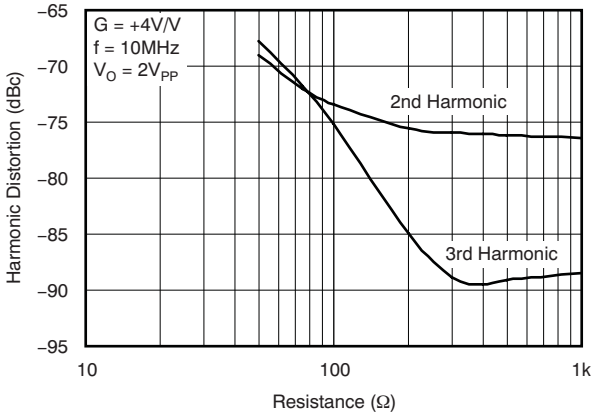


Figure 63.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

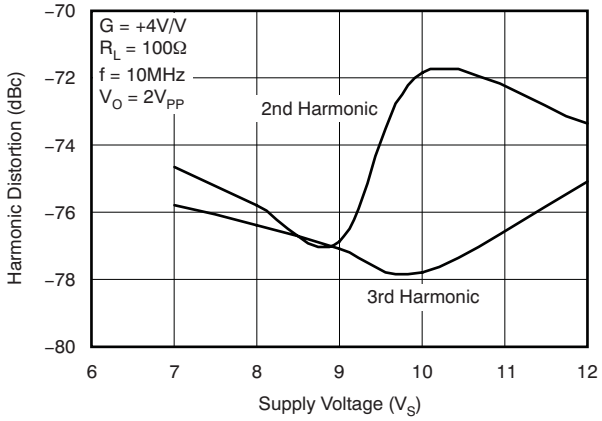


Figure 64.

HARMONIC DISTORTION vs NONINVERTING GAIN

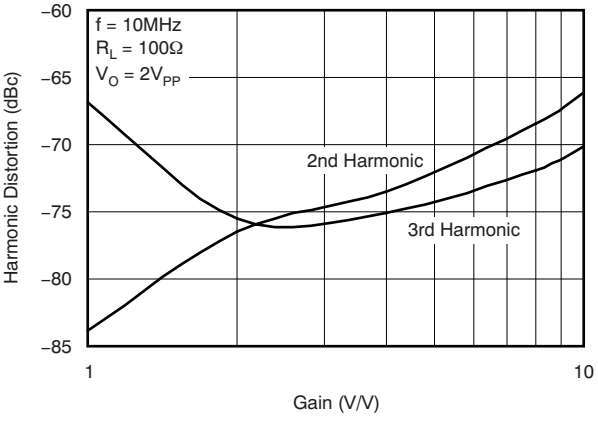


Figure 65.

TWO-TONE, THIRD-ORDER INTERMODULATION INTERCEPT

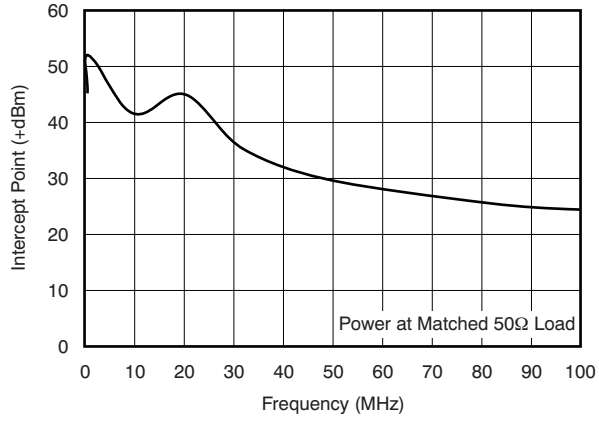


Figure 66.

TYPICAL CHARACTERISTICS: V_S = ±6V, 50% Bias (continued)

At T_A = +25°C, G = +4V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise specified.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

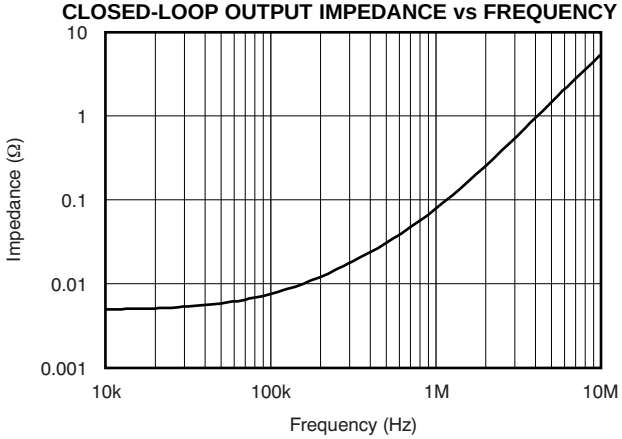


Figure 67.

TYPICAL CHARACTERISTICS: V_S = ±6V Differential, 50% Bias

At T_A = +25°C, R_F = 511Ω, R_L = 100Ω Differential, G_{DIFF} = +4V/V, and G_{CM} = +1V/V, unless otherwise specified.

SMALL-SIGNAL FREQUENCY RESPONSE

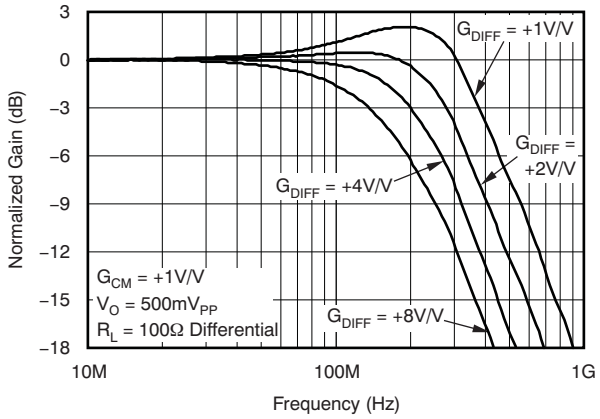


Figure 68.

LARGE-SIGNAL FREQUENCY RESPONSE

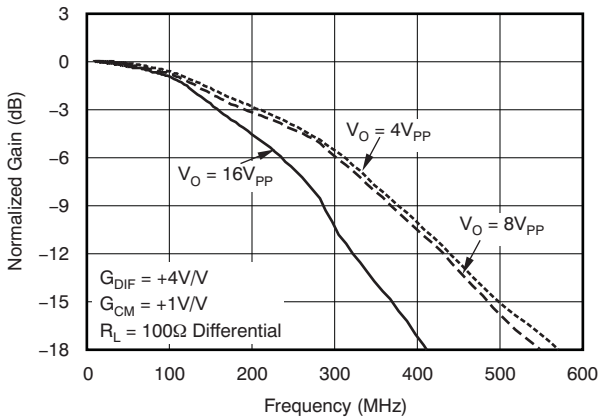


Figure 69.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSES

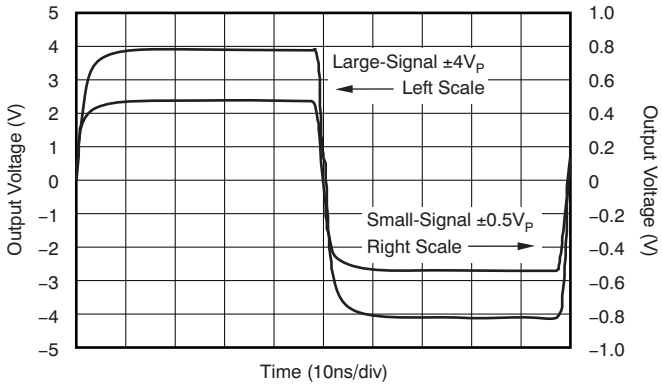


Figure 70.

HARMONIC DISTORTION vs FREQUENCY

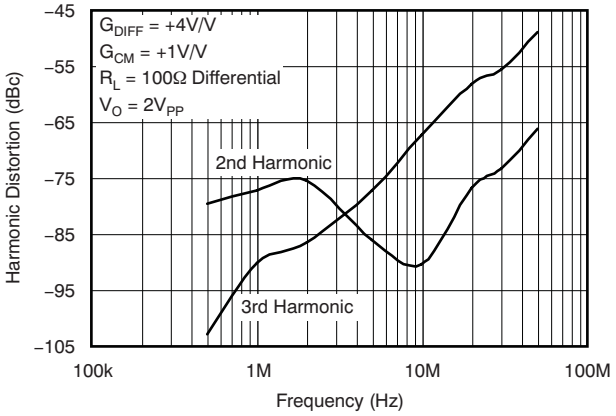


Figure 71.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

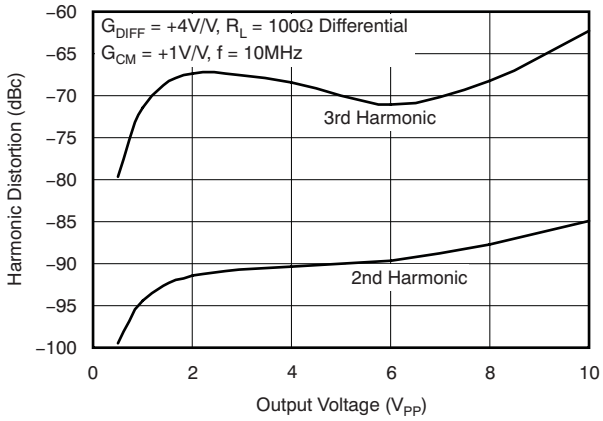


Figure 72.

HARMONIC DISTORTION vs LOAD RESISTANCE

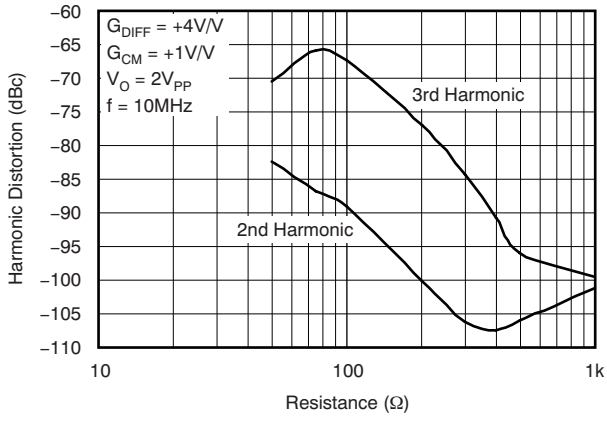


Figure 73.

TYPICAL CHARACTERISTICS: V_S = ±6V Differential, 50% Bias (continued)

At T_A = +25°C, R_F = 511Ω, R_L = 100Ω Differential, G_{DIFF} = +4V/V, and G_{CM} = +1V/V, unless otherwise specified.

HARMONIC DISTORTION vs NONINVERTING GAIN

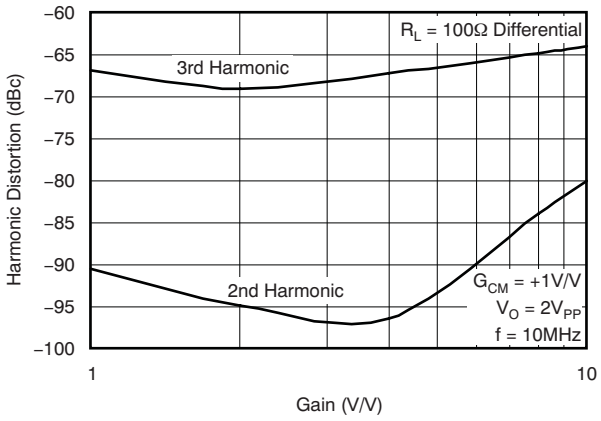


Figure 74.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

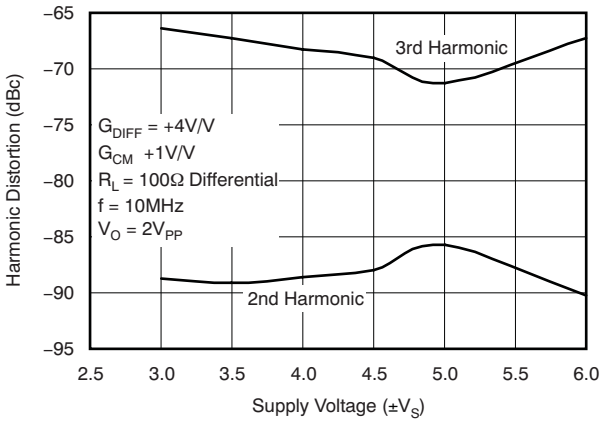


Figure 75.

APPLICATION INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2673 gives the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring 16mA/ch quiescent current, the OPA2673 swings to within 1.1V of either supply rail and delivers in excess of 460mA at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable dual (±6V) supply operation. The OPA2673 delivers greater than 450MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a single +12V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The OPA2673 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. Figure 76 shows the dc-coupled, gain of +4V/V, dual power-supply circuit configuration used as the basis of the ±6V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins, while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 76, the total effective load is 100Ω || 402Ω = 80Ω.

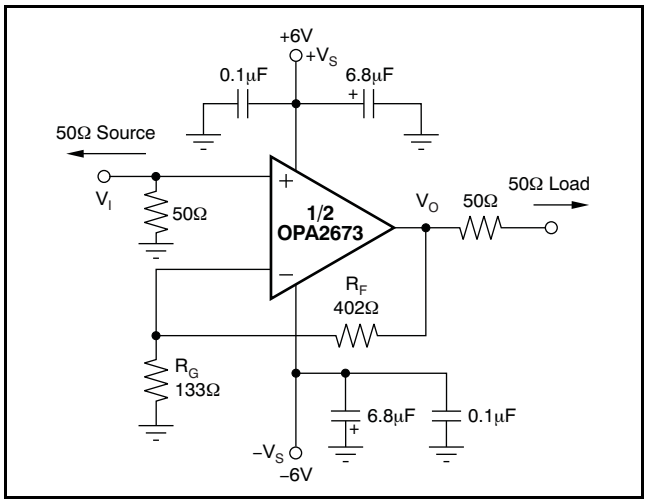


Figure 76. DC-Coupled, G = +4V/V, Bipolar Supply, Specification and Test Circuit

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers that include a disable pin is to wire multiple amplifier outputs together, then select one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OPA2673, as Figure 77 illustrates.

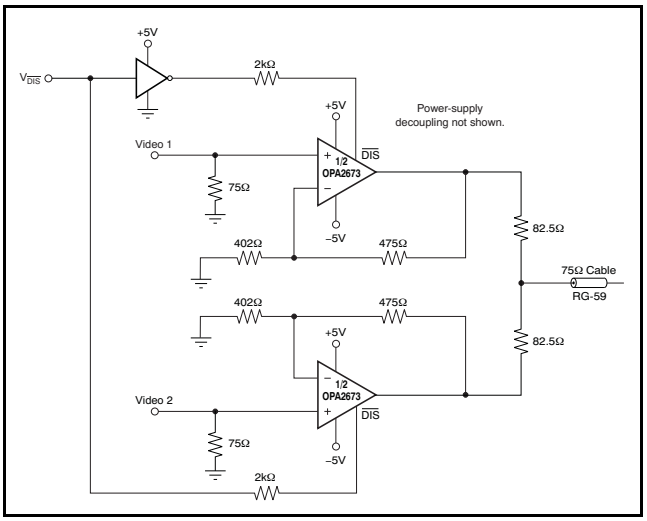


Figure 77. Two-Channel Video Multiplexer

Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this time. The *make-before-break* disable characteristic of the OPA2673 ensures that there is always one amplifier controlling the line when using a wired-OR circuit similar to that shown in Figure 77. Because both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (82.5Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The gain and output matching resistors have been slightly increased to get a signal gain of +1V/V at the matched load and provide a 75Ω output impedance to the cable. The video multiplexer connection (as shown in Figure 77) also ensures that the maximum differential voltage across the inputs of the unselected channel do not exceed the rated ±1.2V maximum for standard video signal levels. The active-off line circuitry integrated within the OPA2673 ensures that the off-channel will stay off independently of the signal amplitude present at the output.

Where two outputs are switched (see Figure 77), the output line is always under the control of one amplifier or the other as a result of the *make-before-break* disable timing. In this case, the switching glitches for two 0V inputs drop to less than 20mV.

HIGH-SPEED ACTIVE FILTERS

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as a fixed gain block inside a passive RC circuit network. The relatively constant bandwidth versus gain provides low interaction between the actual filter poles and the required gain for the amplifier. Figure 78 shows an example single-supply buffered filter application. In this case, one of the OPA2673 channels is used to set up the dc operating point and provide impedance isolation from the signal source into the second-stage filter. That stage is set up to implement a 20MHz, maximally flat Butterworth frequency response and provide an ac gain of +4V/V.

The 51Ω input matching resistor is optional in this case. The input signal is ac-coupled to the 5V dc reference voltage developed through the resistor divider from the +10V power supply. This first stage acts as a gain of +1V/V voltage buffer for the signal where the 600Ω feedback resistor is required for stability. This first stage easily drives the low input resistors required at the input of this high-frequency filter. The second stage is set for a dc gain of +1V/V, carrying the 5V operating point through to the output pin, and an ac gain of +4V/V. The feedback resistor has been adjusted to optimize bandwidth for the amplifier itself. As the single-supply frequency response plots show, the OPA2673 in this configuration gives greater than 400MHz small-signal bandwidth. The capacitor values were chosen as low as possible but adequate to override the parasitic input capacitance of the amplifier. The resistor values were slightly adjusted to give the desired filter frequency response while accounting for the approximate 1ns propagation delay through each channel of the OPA2673.

HIGH-POWER TWISTED-PAIR DRIVER

A very demanding application for a high-speed amplifier is to drive a low load impedance while maintaining a high output voltage swing to high frequencies. Using the dual current-feedback op amp OPA2673, an $8V_{PP}$ output signal swing into a twisted-pair line with a typical impedance of 50Ω can be realized. Configured as shown on the front page, the two amplifiers of the OPA2673 drive the output transformer in a push-pull configuration, thus doubling the peak-to-peak signal swing at each op amp output to $8V_{PP}$. The transformer has a turns ratio of 1.4. The total load seen by the amplifier is 35Ω.

Line driver applications usually have a high demand for transmitting the signal with low distortion. Current-feedback amplifiers such as the OPA2673 are ideal for delivering low-distortion performance to higher gains. The example shown is set for a differential gain of 4V/V. This circuit can deliver the maximum $8V_{PP}$ signal with over 200MHz bandwidth.

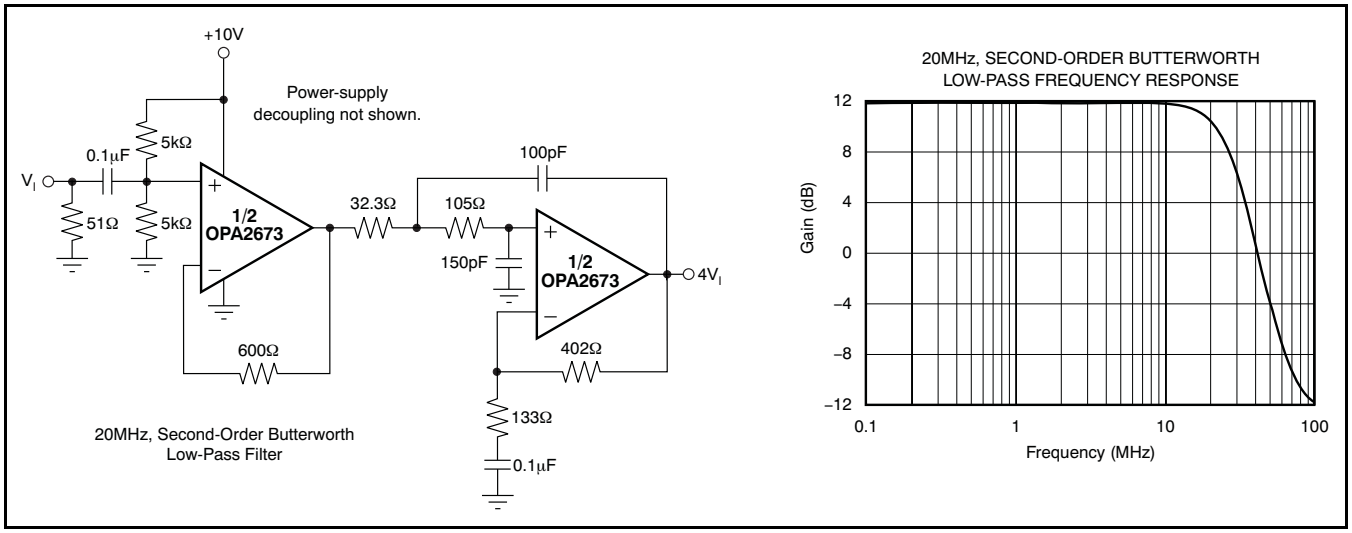


Figure 78. Buffered Single-Supply Active Filter

LINE DRIVER HEADROOM MODEL

The first step in a driver design is to compute the peak-to-peak output voltage from the target specifications. This calculation is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \quad (1)$$

With P_L power and V_{RMS} voltage at the load, and R_L load impedance, this calculation gives:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (2)$$

$$V_P = \text{CrestFactor} \times V_{RMS} = CF \times V_{RMS} \quad (3)$$

With V_P peak voltage at the load and the crest factor, CF:

$$V_{LPP} = 2 \times CF \times V_{RMS} \quad (4)$$

with V_{LPP}: peak-to-peak voltage at the load.

Consolidating Equation 1 through Equation 4 allows the required peak-to-peak voltage at the load function of the crest factor, the load impedance, and the power in the load to be expressed. Thus:

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (5)$$

This V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step for the driver is to compute the individual amplifier output voltage and currents as a function of V_{PP} on the line and transformer turns ratio. As the turns ratio changes, the minimum allowed supply voltage also changes. The peak current in the amplifier is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_M} \quad (6)$$

With V_{LPP} defined in Equation 5 and R_M defined in Equation 7.

$$R_M = \frac{Z_{LINE}}{2n^2} \quad (7)$$

The peak current is computed in Figure 79 by noting that the total load is $4R_M$ and that the peak current is half of the peak-to-peak calculated using V_{LPP}.

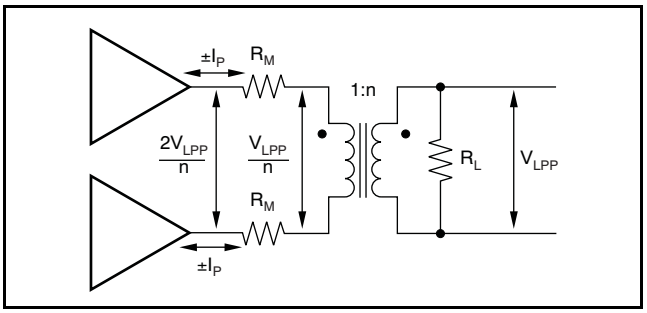


Figure 79. Driver Peak Output Model

With the required output voltage and current versus turns ratio set, an output stage headroom model allows the required supply voltage versus turns ratio to be developed.

The headroom model (see Figure 80) can be described with the following set of equations:

First, as available output voltage for each amplifier:

$$V_{OPP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (8)$$

Or, second, as required single-supply voltage:

$$V_{CC} = V_{OPP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (9)$$

The minimum supply voltage for a set of power and load requirements is given by Equation 9.

Table 1 gives V_1, V_2, R_1, and R_2 for +12V operation of the OPA2673.

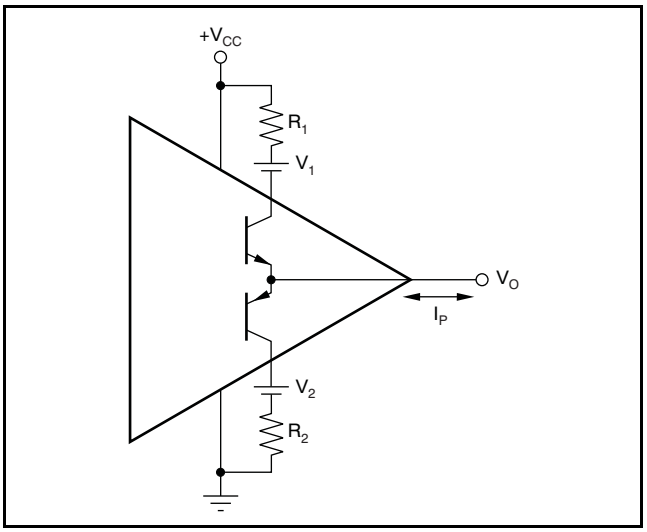


Figure 80. Line Driver Headroom Model

Table 1. Line Driver Headroom Model Values

	V_1	R_1	V_2	R_2
+12V	0.9V	2Ω	0.9V	2Ω

TOTAL DRIVER POWER FOR LINE DRIVER APPLICATIONS

The total internal power dissipation for the OPA2673 in a line driver application is the sum of the quiescent power and the output stage power. The OPA2673 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage is greater than the solution given in Equation 9). The total output stage power may be computed with reference to Figure 81.

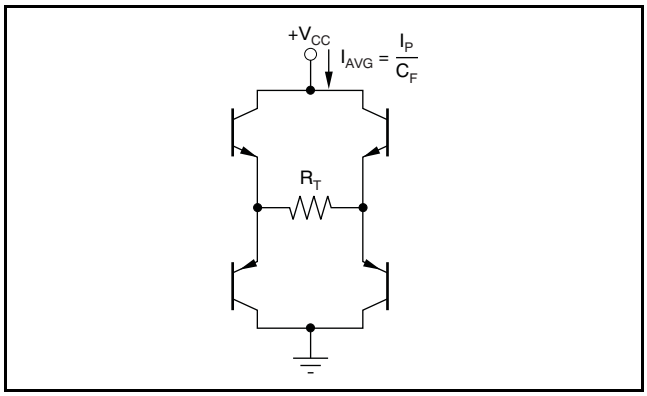


Figure 81. Output Stage Power Model

The two output stages used to drive the load of Figure 79 can be seen as an H-Bridge in Figure 81. The average current drawn from the supply into this H-Bridge and load is the peak current in the load given by Equation 6 divided by the crest factor (CF). This total power from the supply is then reduced by the power in R_T to leave the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 7 plus the power lost in the matching elements (R_M). In the examples here, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 10.

$$P_{OUT} = \frac{I_P}{C_F} \times V_{CC} - 2P_L \quad (10)$$

The total amplifier power is then:

$$P_{TOT} = I_Q \times V_{CC} + \frac{I_P}{C_F} \times V_{CC} - 2P_L \quad (11)$$

DESIGN-IN TOOLS

Demonstration Fixture

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA2673 in its QFN package option. This demo board is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 2.

Table 2. Demonstration Fixture by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2673IRGV	QFN-16	DEM-OPA-QFN-2A	SBOU067

This demonstration fixture can be requested through the Texas Instruments web site (www.ti.com).

Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This technique is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2673 is available through the TI web site (www.ti.com). This model does a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions, but does not do as well in predicting the harmonic distortion or dG/dΦ characteristics. This model does not attempt to distinguish between the package types in small-signal ac performance, nor does it attempt to simulate channel-to-channel coupling.

OPERATING SUGGESTIONS

Setting Resistor Values to Optimize Bandwidth

A current-feedback op amp such as the OPA2673 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values, which are shown in the Typical Characteristics; the small-signal bandwidth decreases only slightly with increasing gain. These characteristic curves also show that the feedback resistor is changed for each gain setting. The resistor values on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements, whereas the ratios set the signal gain.

Figure 82 shows the small-signal frequency response analysis circuit for the OPA2673.

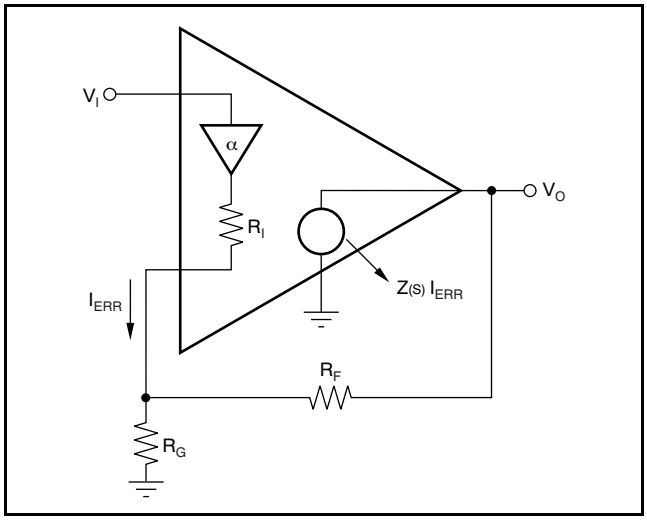


Figure 82. Current-Feedback Transfer Function Analysis Circuit

The key elements of this current-feedback op amp model are:

α = buffer gain from the noninverting input to the inverting input

R_I = buffer output impedance

I_{ERR} = feedback error current signal

Z(s) = frequency-dependent open-loop transimpedance gain from I_{ERR} to V_O

$$NG = \text{Noise Gain} = 1 + \frac{R_F}{R_G} \tag{12}$$

The buffer gain is typically very close to 1.00V/V and is normally neglected from signal gain considerations. This gain, however, sets the CMRR for a single op amp differential amplifier configuration. For a buffer gain of $\alpha < 1.0$, the CMRR = $-20 \times \log(1 - \alpha)$dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2673 inverting output impedance is typically 32Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response, which is analogous to the open-loop voltage gain curve for a voltage-feedback op amp.

Developing the transfer function for the circuit of Figure 82 gives Equation 13:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1 + \frac{R_F}{R_G}\right)}{1 + \frac{R_F + R_I\left(1 + \frac{R_F}{R_G}\right)}{Z(s)}} = \frac{\alpha \times NG}{1 + \frac{R_F + R_I \times NG}{Z(s)}} \tag{13}$$

This formula is written in a loop-gain analysis format, where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) is infinite over all frequencies, the denominator of Equation 13 reduces to 1 and the ideal desired signal gain shown in the numerator is achieved. The fraction in the denominator of Equation 13 determines the frequency response. Equation 14 shows this as the loop-gain equation:

$$\frac{Z(s)}{R_F + R_I \times NG} = \text{Loop Gain} \tag{14}$$

If $20\log(R_F + NG \times R_I)$ is drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 14, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop frequency response given by Equation 13 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 14 may be controlled somewhat separately from the desired signal gain (or NG). The OPA2673 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 4V/V on ±6V supplies. Evaluating the denominator of Equation 14 (which is the feedback transimpedance) gives an optimal target of 530Ω. As the signal gain changes, the contribution of the NG × R_I term in the feedback transimpedance changes, but the total can be held constant by adjusting R_F. Equation 15 gives an approximate equation for optimum RF over signal gain:

$$R_F = 530 - NG \times R_I \tag{15}$$

As the desired signal gain increases, this equation eventually suggests a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values load both the buffer stage at the input and the output stage if R_F gets too low—actually decreasing the bandwidth. Figure 83 shows the recommended R_F versus N_G for ±6V operation. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical

Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitic not considered in the simplified analysis leading to Equation 15. The values shown in Figure 83 give a good starting point for designs where bandwidth optimization is desired.

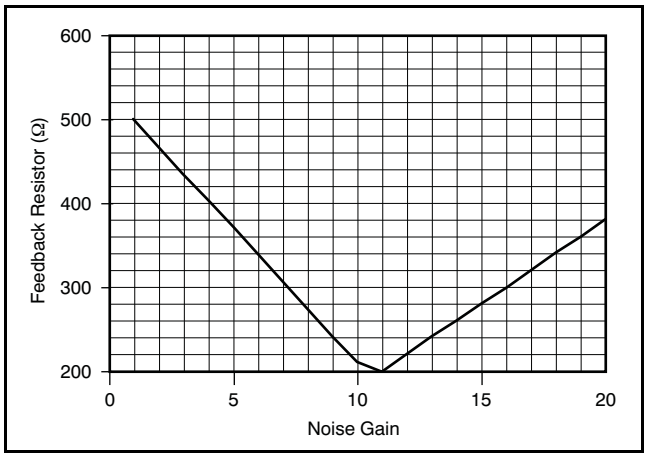


Figure 83. Feedback Resistor vs Noise Gain

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (the denominator of Equation 14), decreasing the bandwidth. The internal buffer output impedance for the OPA2673 is slightly influenced by the source impedance coming from of the noninverting input terminal. High-source resistors also have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications that develop a midpoint bias at the noninverting input through high valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, noninverting input noise current shunting, and to minimize the high-frequency value for R_I in Figure 82.

Output Current and Voltage

The OPA2673 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1.1V to either supply rail; the tested (+25°C) swing limit is within 1.2V of either rail. Into a 4Ω load (the minimum tested load), it delivers more than ±460mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V-I product) that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics (Figure 6). The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2673 output drive capabilities, noting that the graph is bounded by a safe operating area of 2W maximum internal power dissipation (in this case, for one channel only). Superimposing resistor load lines onto the plot shows that the OPA2673 can drive ±4V into 10Ω or ±4.5V into 25Ω without exceeding the output capabilities or the 2W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±4.8V output swing capability, as stated in the Electrical Characteristics table. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the Electrical Characteristics table. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature specifications because the output stage junction temperatures is higher than the minimum specified operating ambient.

Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an analog-to-digital converter (ADC)—including additional external capacitance that may be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA2673 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This approach does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the *Differential R_S vs Capacitive Load* (Figure 27) and the resulting

frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2673. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2673 output pin (see the *Board Layout Guidelines* section).

Distortion Performance

The OPA2673 provides good distortion performance into a 100Ω load on ±6V supplies. Generally, until the fundamental signal reaches very high frequency or power levels, the second harmonic dominates the distortion with a negligible third harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 76), this network is the sum of $R_F + R_G$; in the inverting configuration, it is R_F. Also, providing an additional supply decoupling capacitor (0.01μF) between the supply pins (for bipolar operation) improves the second-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing directly increases harmonic distortion. The Typical Characteristics show the second harmonic increasing at a little less than the expected 2x rate, whereas the third harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the second harmonic decreases less than the expected 6dB, while the difference between it and the third harmonic decreases by less than the expected 12dB. This factor also shows up in the two-tone, third-order intermodulation spurious (IM3) response curves. The third-order spurious levels are extremely low at low-output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 40MHz, with 10dBm/tone into a matched 50Ω load (that is, $2V_{PP}$ for each tone at the load, which requires $8V_{PP}$ for the overall two-tone envelope at the output pin), the Typical Characteristics show 69dBc difference between the test-tone power and the third-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

Noise Performance

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2673 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (35pA/√Hz) is lower than earlier solutions, whereas the input voltage noise (2.4nV/√Hz) is lower than most unity-gain stable, wideband voltage-feedback op amps. This low input voltage noise is achieved at the price of higher noninverting input current noise (5.2pA/√Hz). As long as the ac source impedance from the noninverting node is less than 100Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 84 shows the op amp noise analysis model with all noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 16 shows the general form for the output noise voltage using the terms given in Figure 84.

$$E_O = \sqrt{\left[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right] \times NG + (I_{BI}R_F)^2 + 4kTR_F NG} \quad (16)$$

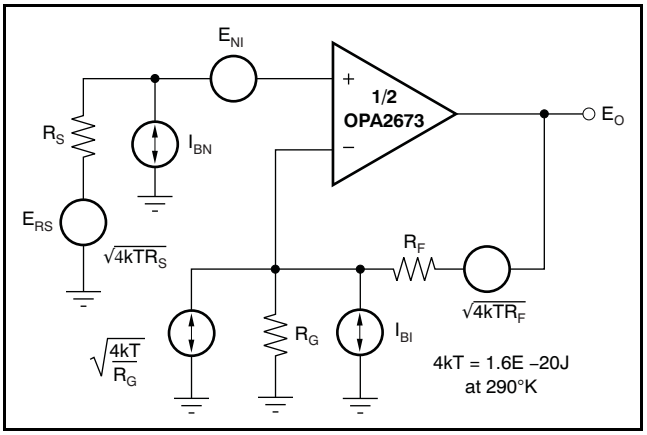


Figure 84. Op Amp Noise Analysis Model

Dividing this expression by the noise gain [NG = (1 + R_F/R_G)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 17.

$$E_I = \sqrt{E_{NI}^2 + (I_{BN} \times R_S)^2 + 4kTR_S + \frac{(I_{BI} \times R_F)^2}{NG^2} + \frac{4kTR_F}{NG}} \quad (17)$$

Evaluating these two equations for the OPA2673 circuit and component values of Figure 76 gives a total output spot noise voltage of 18nV/√Hz and a total equivalent input spot noise voltage of 4.5nV/√Hz. This total input-referred spot noise voltage is higher than the 2.4nV/√Hz specification for the op amp voltage noise alone. This result reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input-referred voltage noise given by Equation 17 approaches only the 2.4nV/√Hz of the op amp. For example, going to a gain of +8V/V using R_F = 250Ω gives a total input-referred noise of 2.8nV/√Hz.

Differential Noise Performance

Because the OPA2673 is used as a differential driver in PLC applications, it is important to analyze the noise in such a configuration. See Figure 85 for the op amp noise model for the differential configuration.

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (18)$$

The output noise voltage can be expressed as shown below:

$$E_O^2 = \sqrt{2 \times G_D^2 \times \left[E_N^2 + (I_N \times R_S)^2 + 4kTR_S\right] + 2(I_I R_F)^2 + 2(4kTR_F G_D)} \quad (19)$$

Dividing this expression by the differential noise gain, $G_D = (1 + 2R_F/R_G)$, gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 20.

$$E_I = \sqrt{2 \times \left[E_N^2 + (I_N \times R_S)^2 + 4kTR_S\right] + 2\left[I_I \frac{R_F}{G_D}\right]^2 + 2\left[\frac{4kTR_F}{G_D}\right]} \quad (20)$$

Evaluating this equation for the OPA2673 circuit and component values shown on the front page gives a total output spot noise voltage of 72.3nV/√Hz and a total equivalent input spot noise voltage of 18.4nV/√Hz.

In order to minimize the noise contributed by I_N, it is recommended to keep the noninverting source impedance as low as possible.

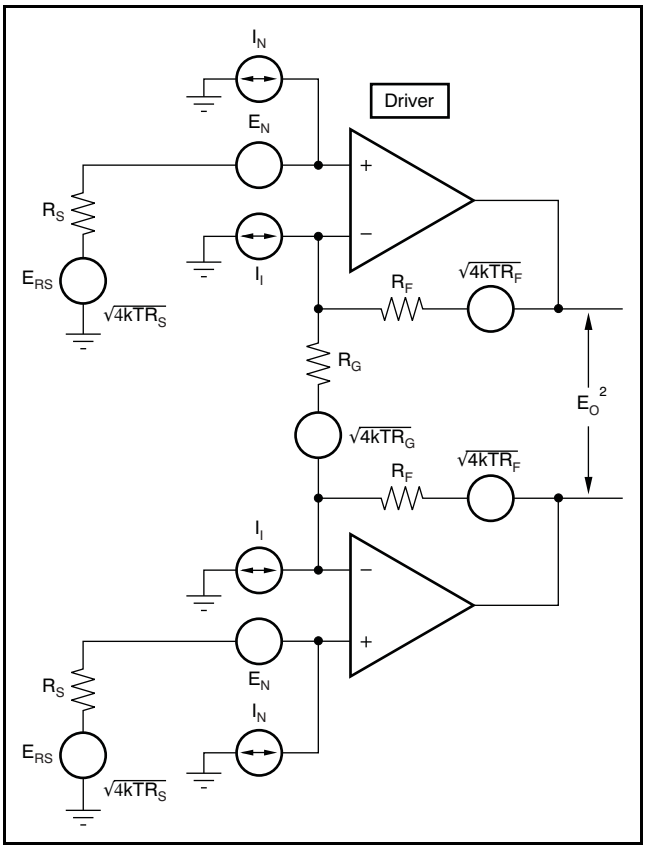


Figure 85. Differential Op Amp Noise Analysis Model

DC Accuracy and Offset Control

A current-feedback op amp such as the OPA2673 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate dc accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. While bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 76, using a worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$V_{OS} = \pm(NG \times V_{IO(MAX)}) \pm (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$

where NG = noninverting signal gain

$= \pm(4 \times 7mV) + (25\mu A \times 25\Omega \times 4) \pm (402\Omega \times 48\mu A)$

$= \pm 28mV \pm 2.5mV \pm 19.3mV$

$V_{OS} = \pm 49.8mV$ (max at +25°C) (21)

Power Control Operation

The OPA2673 provides a power control feature that may be used to reduce system power. The four modes of operation for this power control feature are 100% bias, 75% bias, 50% bias, and power shutdown. These four operating modes are set through two logic lines A0 and A1. Table 3 shows the different modes of operation.

Table 3. Operating Modes

MODE OF OPERATION	A1	A0
100% bias	0	0
75% bias	0	1
50% bias	1	0
Shutdown	1	1

The 100% bias mode is used for normal operating conditions. The 75% bias mode brings the quiescent power to 24mA. The 50% bias mode brings the quiescent power to 16mA. The shutdown mode has a high output impedance as well as the lowest quiescent power (5.5mA).

If the A0 and A1 pins are left unconnected, the OPA2673 operates normally (100% bias).

To change the power mode, the control pins (either A0 or A1) must be asserted low. This logic control is referenced to the ground supply, as shown in the simplified circuit of Figure 86.

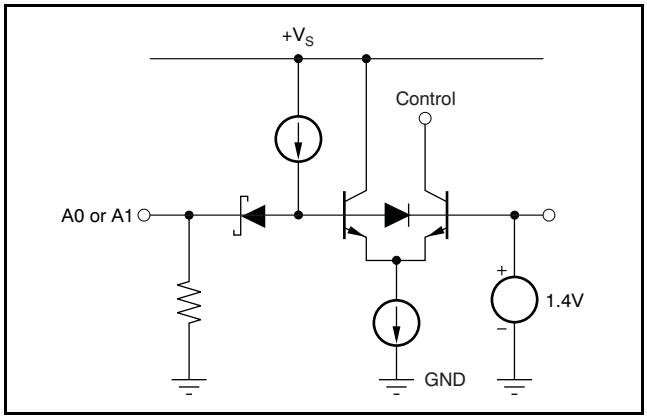


Figure 86. Supply Power Control Circuit

The shutdown feature for the OPA2673 is a ground-supply referenced, current-controlled interface. For voltage output logic interfaces, the on/off voltage levels described in the Electrical Characteristics apply only for either the ground pin RGV package or the $-V_S$ pin used for the single-supply specifications.

THERMAL ANALYSIS

As a result of the high output power capability of the OPA2673, heat-sinking or forced airflow may be required under extreme operating conditions. The maximum desired junction temperature sets the maximum allowed internal power dissipation, described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S{}^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2673 QFN-16 in the circuit of Figure 76 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 20Ω load to +2.5V.

$P_D = 12V \times 32mA + 2 \times [5^2/(4 \times [20\Omega \quad 535\Omega])]$
$= 1.03W$

Maximum $T_J = +85°C + (1.03 \times 45°C/W) = 131°C$

Although this value is still well below the specified maximum junction temperature, system, reliability considerations may require lower tested junction temperatures.The highest possible internal dissipation occurs if the load requires current to be forced into the output for positive output voltages, or sourced from the output for negative output voltages. This condition puts a high current through a large internal drop in the output transistors. The output V-I plot in the Typical Characteristics (Figure 6) includes a boundary for 2W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA2673 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25in, or 6,350mm) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 7 and 14 for a QFN package) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These can be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2673. Resistors should be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it gives a more peaked frequency response. The 402Ω feedback resistor used in the Typical Characteristics at a gain of +4V/V on ±6V supplies is a good starting point for design. Note that a 511Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils, or 1,27mm to 2,54mm) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Differential R_S vs Capacitive Load* (Figure 27). Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA2673 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard. In fact, a higher impedance environment improves distortion; see the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2673 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2673 allows multiple destination devices to be handled as separate transmission lines, each with respective series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of *Differential R_S vs Capacitive Load* (Figure 27). However, this approach does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation because of the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part such as the OPA2673 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2673 directly onto the board.

INPUT AND ESD PROTECTION

The OPA2673 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices and are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 87.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2673), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, because high values degrade both noise performance and frequency response.

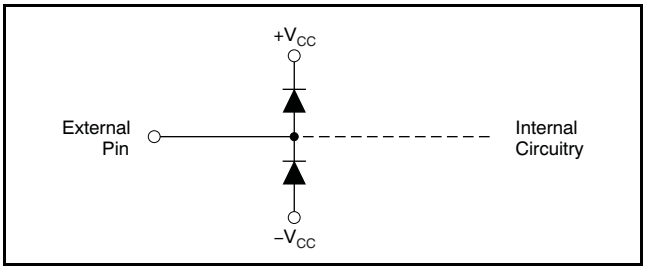


Figure 87. ESD Steering Diodes

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April, 2010) to Revision F **Page**

- Added *minimum operating voltage (single supply)* parameter 5

Changes from Revision D (January, 2010) to Revision E **Page**

- Revised *Absolute Maximum Ratings* table; deleted lead temperature specification, changed storage temperature range from –40°C to –65°C 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2673IRGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2673	Samples
OPA2673IRGVT	ACTIVE	VQFN	RGV	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2673	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

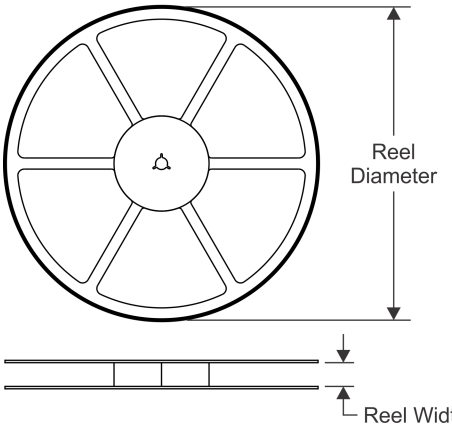
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

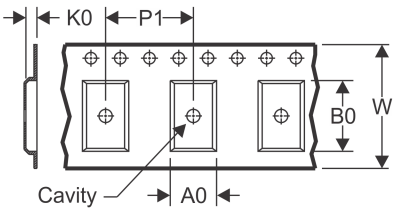
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

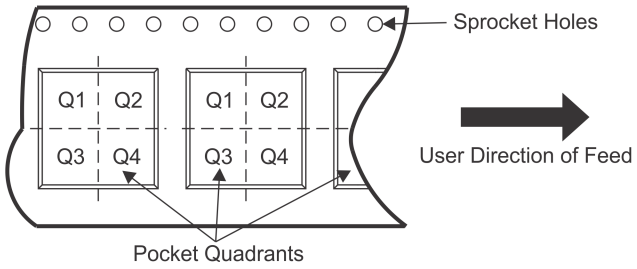


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

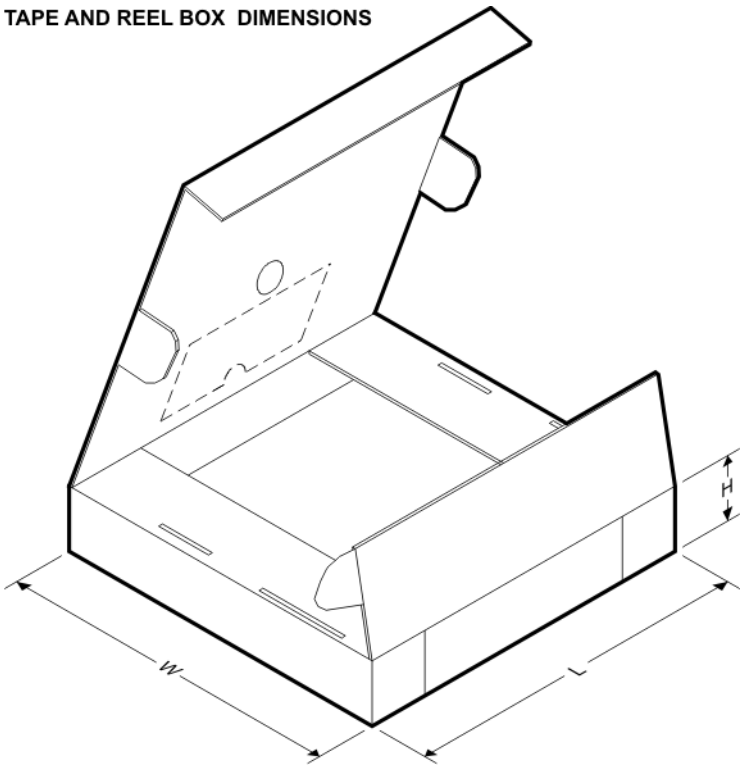
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2673IRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2673IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

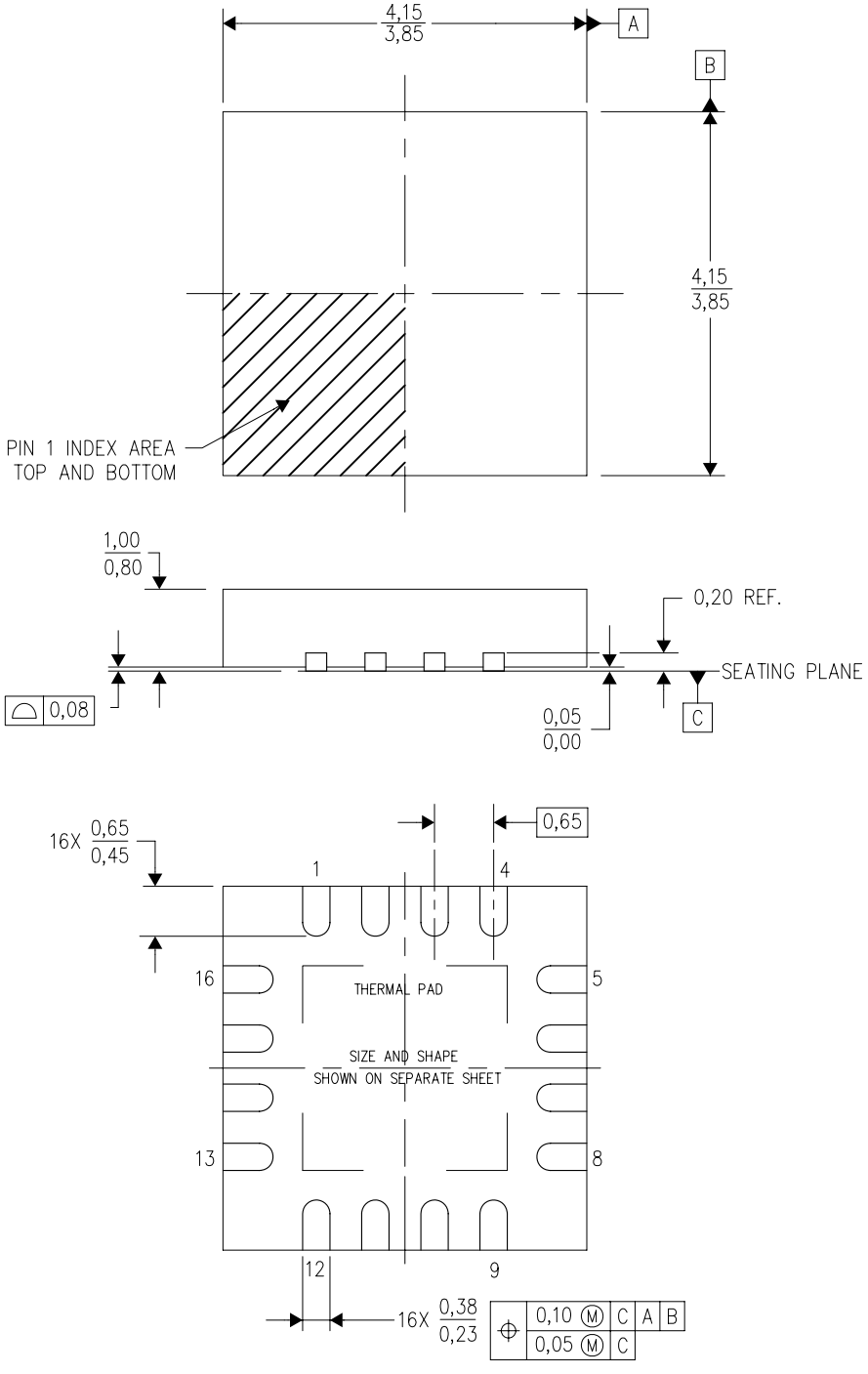
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2673IRGVR	VQFN	RGV	16	2500	853.0	449.0	35.0
OPA2673IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

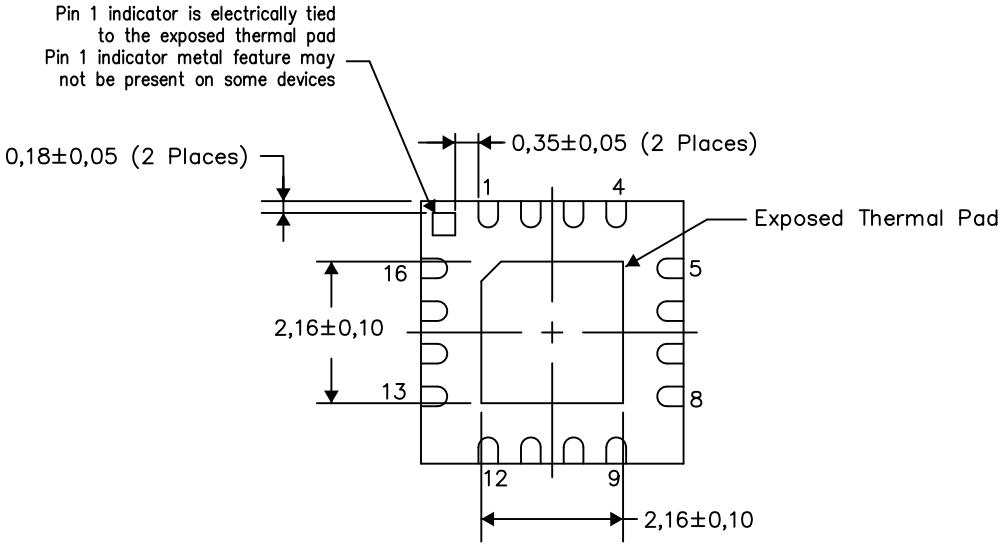
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



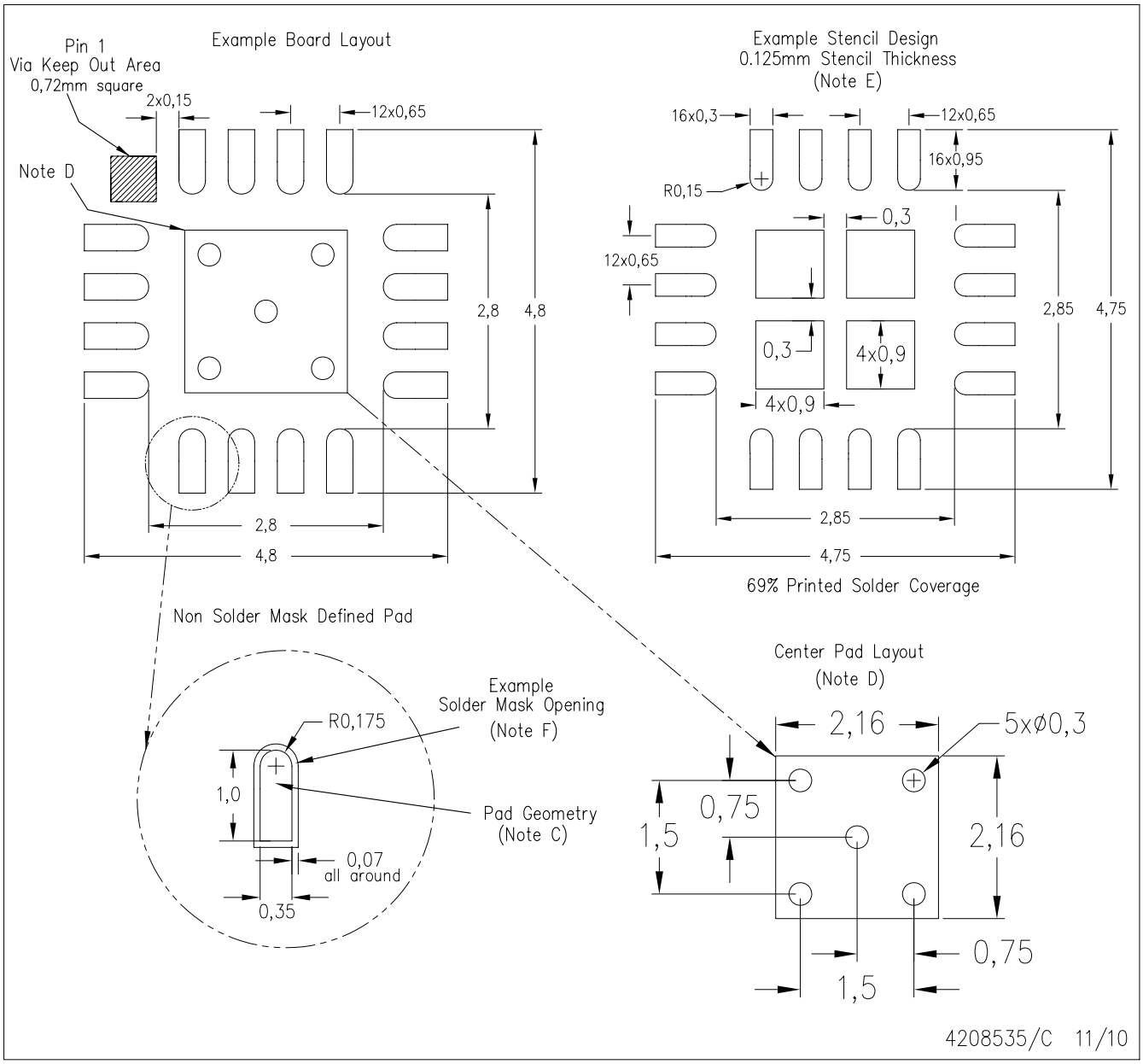
Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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