TPS40054: Not Recommended For New Designs

TPS4005x Wide-Input Synchronous Buck Controller

1 Features

- Operating Input Voltage 8 V to 40 V
- Input Voltage Feed-Forward Compensation
- < 1% Internal 0.7-V Reference
- Programmable Fixed-Frequency up to 1-MHz Voltage Mode Controller
- Internal Gate-Drive Outputs for High-Side and Synchronous N-Channel MOSFETs
- 16-Pin PowerPAD™ Package (θ_{JC} = 2°C/W)
- Thermal Shutdown
- Externally Synchronizable
- Programmable High-Side Sense Short-Circuit Protection
- Programmable Closed-Loop Soft-Start
- TPS40054 Source Only
- TPS40055 Source and Sink
- TPS40057 Source and Sink With V_O Prebias

2 Applications

- Power Modules
- Networking and Telecom
- Industrial and Servers

3 Description

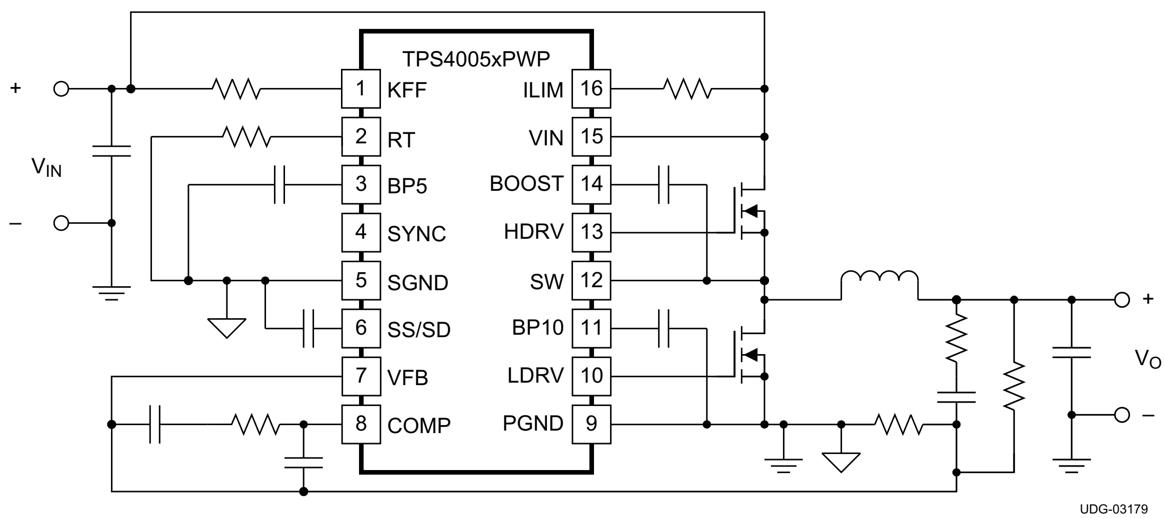
The TPS4005x is a family of high-voltage, wide-input (8 V to 40 V), synchronous, step-down controllers. The TPS4005x family offers design flexibility with a variety of user-programmable functions, including soft-start, UVLO, operating frequency, voltage feed-forward, high-side current limit, and loop compensation.

The TPS4005x uses voltage feed-forward control techniques to provide good line regulation over the wide (4:1) input voltage range, and fast response to input line transients. Near-constant modulator gain with input variation eases loop compensation. The externally programmable current limit provides pulse-by-pulse current limit, as well as hiccup mode operation using an internal fault counter for longer duration overloads.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS4005x	HTSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (July 2012) to Revision I — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 3

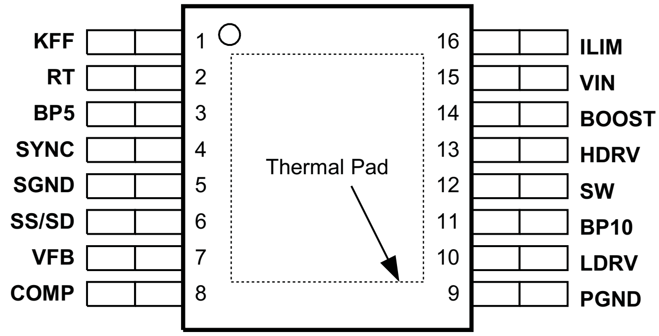
Changes from Revision G (September 2011) to Revision H — **Page**

- Added the Thermal Information table ... 4

Changes from Revision F (September 2008) to Revision G — **Page**

- Deleted errors in schematic. ... 1
- Changed I_{LIM} to I_{ILIM} (corrected typographical error) ... 12
- Added clarity to *Loop Compensation* section ... 13
- Changed $V_{IN(UVLO)}$ to $V_{IN(min)}$ in two places (corrected typographic errors) ... 13
- Changed corrected Equation 46 ... 20
- Changed corrected reference designator values in Figure 15 ... 20
- Changed corrected Equation 56 ... 22
- Changed corrected Equation 67 ... 23
- Changed corrected Equation 69 ... 23

5 Pin Configuration and Functions



A. For more information on the PWP package, refer to the application report, PowerPAD™ Thermally Enhanced Package (SLMA002).

B. PowerPAD™ heat slug must be connected to SGND (pin 5) or electrically isolated from all other pins.

Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
BOOST	14	O	Gate drive voltage for the high side N-channel MOSFET. The BOOST voltage is 9 V greater than the SW voltage. A 0.1-µF ceramic capacitor should be connected from this pin to the drain of the lower MOSFET.
BP5	3	O	5-V reference. This pin should be bypassed to ground with a 0.1-µF ceramic capacitor. This pin may be used with an external DC load of 1 mA or less.
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1-µF ceramic capacitor. This pin may be used with an external DC load of 1 mA or less.
COMP	8	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The comp pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Current limit pin, used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VCC. The voltage on this pin is compared to the voltage drop (VIN – SW) across the high-side MOSFET during conduction.
KFF	1	I	A resistor is connected from this pin to VIN to program the amount of voltage feed-forward and UVLO level. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9		Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5		Signal ground reference for the device.
SS/SD	6	I	Soft-start programming and shutdown pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 µA. The resulting voltage ramp on the SS/SD pin is used as a second non-inverting input to the error amplifier. The output voltage begins to rise when $V_{SS/SD}$ is approximately 0.85 V. The output continues to rise and reaches regulation when $V_{SS/SD}$ is approximately 1.55 V. The controller is considered shut down when $V_{SS/SD}$ is 125 mV or less. The internal circuitry is enabled when $V_{SS/SD}$ is 210 mV or greater. When $V_{SS/SD}$ is less than approximately 0.85 V, the outputs cease switching and the output voltage (V_O) decays while the internal circuitry remains active.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing. The TPS40054 also uses this pin for zero current sensing.
SYNC	4	I	Syncronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency. If synchronization is not used, connect this pin to SGND.
VFB	7	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.
VIN	15	I	Supply voltage for the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted[(1)]

			MIN	MAX	UNIT
V_{IN}	Input voltage	VFB, SS/SD, SYNC	–0.3	6	
		VIN, SW	–0.3	45	
		SW, transient < 50 ns		–2.5	
		SW, transient < 50 ns, V_{VIN} < 14 V		–5.0	
		KFF, with $I_{IN(max)}$ = – 5 mA	–0.3	11	
V_O	Output voltage	COMP, RT, SS/SD	–0.3	6	
		KFF		5	mA
I_O	Output current	RT		200	µA
T_J	Maximum junction temperature [(2)]			150	°C
T_J	Operating junction temperature		–40	125	
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device may shut down at junction temperatures below 150°C.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	8	40	V
T_A	Operating free-air temperature	–40	85	°C

6.3 Thermal Information

THERMAL METRIC[(1)]		TPS4005x HTSSOP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	28	
$R_{\theta JB}$	Junction-to-board thermal resistance	9	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	8.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.4 Electrical Characteristics

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		8		40	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching, V_{FB} ≥ 0.75 V		1.5	3.0	mA
BP5						
V_{BP5}	Output voltage	I_O ≤ 1 mA	4.7	5	5.2	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Accuracy	8 V ≤ V_{IN} ≤ 40 V	470	520	570	kHz
V_{RAMP}	PWM ramp voltage (1)	V_{PEAK} – V_{VAL}		2		V
V_{IH}	High-level input voltage, SYNC		2			
V_{IL}	Low-level input voltage, SYNC				0.8	V
I_{SYNC}	Input current, SYNC			5	10	µA
	Pulse width, SYNC		50			ns
V_{RT}	RT voltage		2.38	2.5	2.58	V
D_{MAX}	Maximum duty cycle	V_{FB} = 0 V, f_{SW} ≤ 500 kHz	85%		94%	
		V_{FB} = 0 V, 500 kHz ≤ f_{SW} ≤ 1 MHz (1)	80%			
	Minumum duty cycle	V_{FB} ≥ 0.75 V			0%	
V_{KFF}	Feed-forward voltage		3.35	3.48	3.65	V
I_{KFF}	Feed-forward current operating range (1) (2)		20		1100	µA
SOFT-START						
$I_{SS/SD}$	Soft-start source current		1.65	2.35	2.95	µA
$V_{SS/SD}$	Soft-start clamp voltage			3.7		V
t_{DSCH}	Discharge time	$C_{SS/SD}$ = 220 pF	1.6	2.2	2.8	µs
$t_{SS/SD}$	Soft-start time	$C_{SS/SD}$ = 220 pF, 0 V ≤ $V_{SS/SD}$ ≤ 1.6 V	115	150	215	
BP10						
V_{BP10}	Output voltage	I_O ≤ 1 mA	9.0	9.6	10.3	V
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage	8 V ≤ V_{IN} ≤ 40 V, T_A = 25°C	0.698	0.7	0.704	V
		8 V ≤ V_{IN} ≤ 40 V, 0°C ≤ T_A ≤ 85°C	0.693	0.7	0.707	
		8 V ≤ V_{IN} ≤ 40 V, -40°C≤ T_A ≤ 85°C	0.693	0.7	0.715	
G_{BW}	Gain bandwidth (1)		3.0	5		MHz
A_{VOL}	Open loop gain		60	80		dB
I_{OH}	High-level output source current		2.0	4		mA
I_{OL}	Low-level output sink current		2.0	4		
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	3.2	3.5		V
V_{OL}	Low-level output voltage	I_{SINK} = 500 µA		0.2	0.35	
I_{BIAS}	Input bias current	V_{FB} = 0.7 V		100	200	nA

(1) Ensured by design. Not production tested.
(2) I_{KFF} increases with SYNC frequency, maximum duty cycle decreases with I_{KFF}.

Electrical Characteristics (continued)

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{SINK}	Current limit sink current		8.5	10	11.5	µA
	Propagation delay to output	V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 0.5 V)		300		ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 2 V)		200		
t_{ON}	Switch leading-edge blanking pulse time(1)		100			
t_{OFF}	Off time during a fault (soft-start cycle time)			7		cycles
V_{OS}	Offset voltage SW vs. ILIM	T_A = 25°C	–90	–70	–50	mV
		V_{ILIM} = 23.6 V, 0°C ≤ T_A ≤ 85°C	–120		–38	
		V_{ILIM} = 23.6 V, -40°C ≤ T_A ≤ 85°C	–120		–20	
OUTPUT DRIVER						
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 2200 pF		48	96	ns
t_{LFALL}	Low-side driver fall time			24	48	
t_{HRISE}	High-side driver rise time	C_{LOAD} = 2200 pF (HDRV – SW)		48	96	
t_{HFALL}	High-side driver fall time			36	72	
V_{OH}	High-level ouput voltage, HDRV	I_{HDRV} = –0.1 A (HDRV – SW)	V_{BOOST} –1.5 V	V_{BOOST} –1 V		V
V_{OL}	Low-level ouput voltage, HDRV	I_{HDRV} = 0.1 A (HDRV – SW)			0.75	
V_{OH}	High-level ouput voltage, LDRV	I_{LDRV} = –0.1 A	V_{BP10} –1.4 V	V_{BP10} – 1 V		
V_{OL}	Low-level ouput voltage, LDRV	I_{LDRV} = 0.1 A			0.5	
	Minimum controllable pulse width			100	150	ns
SS/SD SHUTDOWN						
V_{SD}	Shutdown threshold voltage	Outputs off	90	125	160	mV
V_{EN}	Device active threshold voltage		190	210	245	
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{IN}= 24.0 V	31.2	32.2	33.5	V
RECTIFIER ZERO CURRENT COMPARATOR (TPS40054 ONLY)						
V_{SW}	Switch voltage	LDRV output OFF	–10	–5	0	mV
SW NODE						
I_{LEAK}	Leakage current(1) (out of pin)				25	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(1)			165		°C
	Hysteresis(1)			20		
UVLO						
V_{UVLO}	KFF programmable threshold voltage	R_{KFF} = 28.7 kΩ	6.95	7.5	7.95	V
V_{DD}	UVLO, fixed		7.2	7.5	7.9	
V_{DD}	UVLO, hysteresis			0.46		

6.5 Typical Characteristics

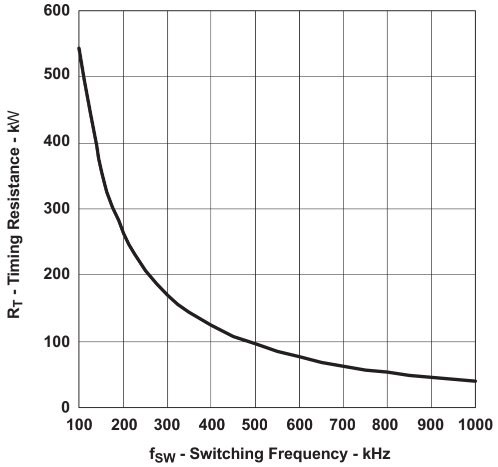


Figure 1. Switching Frequency vs. Timing Resistance

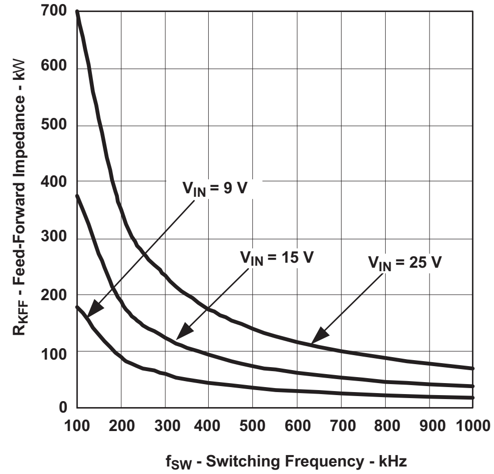


Figure 2. Feed-Forward Impedance vs. Switching Frequency

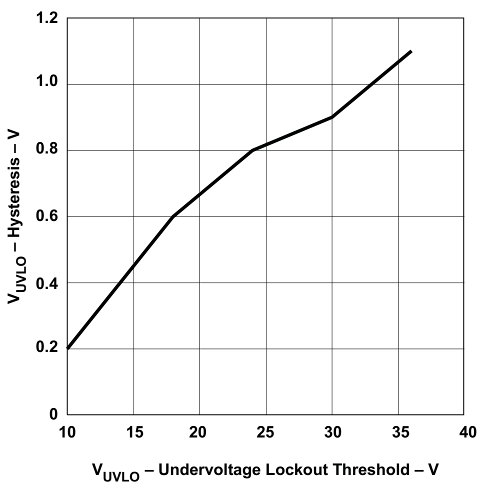


Figure 3. Undervoltage Lockout Threshold vs Hsyteresis

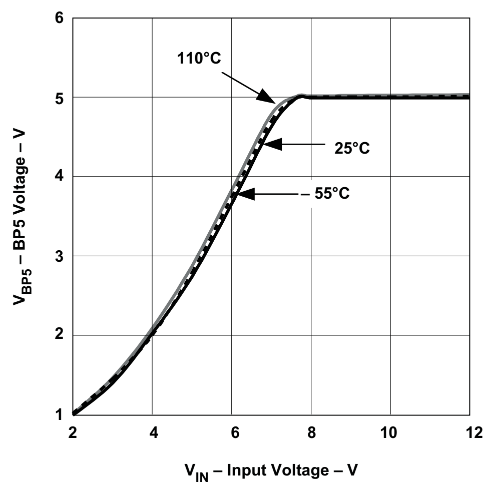


Figure 4. Input Voltage vs BP5 Voltage

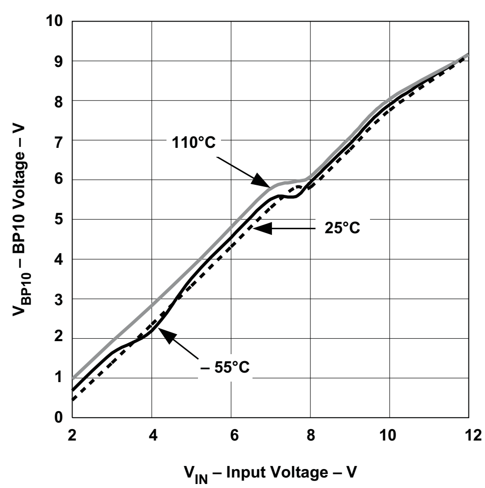


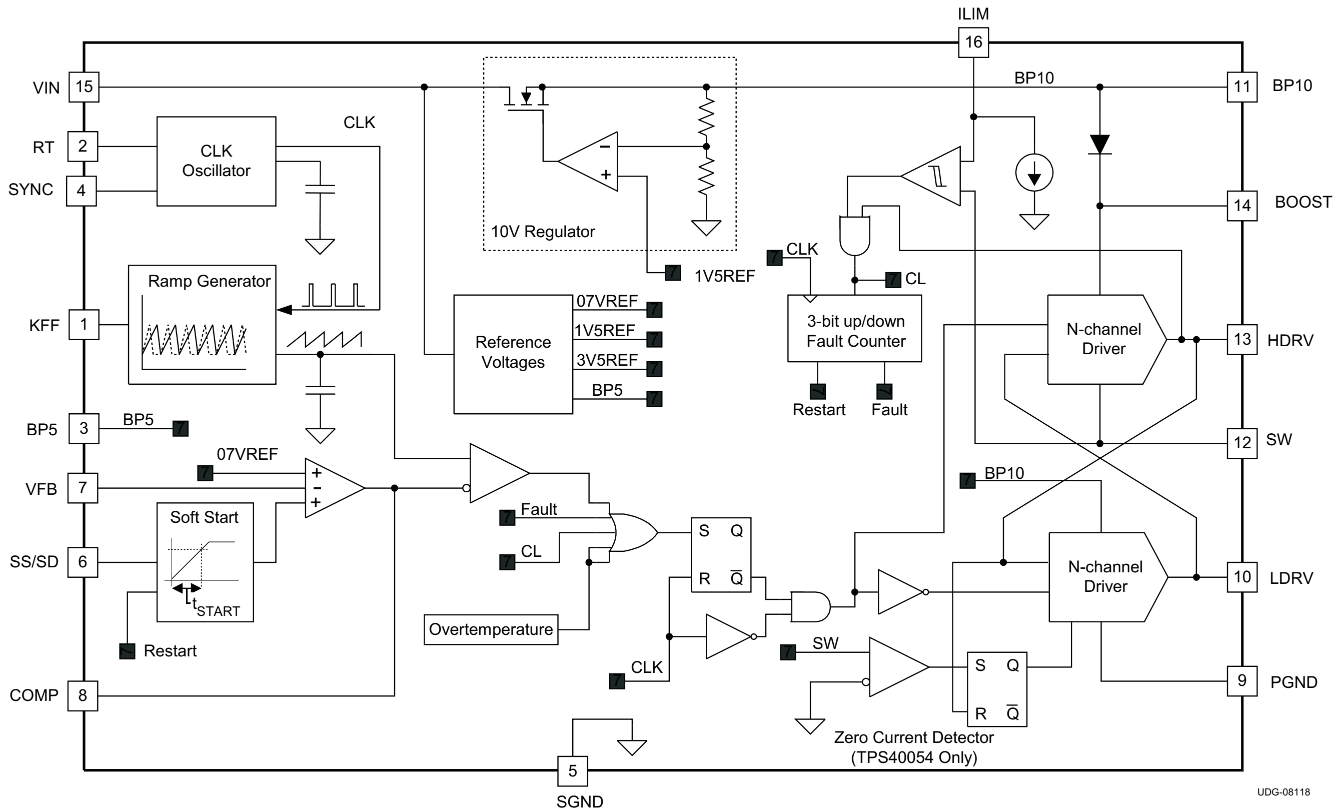
Figure 5. Input Voltage vs BP10 Voltage

7 Detailed Description

7.1 Overview

The TPS4005x family of synchronous buck controllers are designed to operate over a wide range of input voltages (8 V to 40 V). These devices offer a variety of user programmable functions such as operating frequency, soft-start, voltage feed-forward, high-side current limit, and external loop compensation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Setting the Switching Frequency (Programming the Clock Oscillator)

The TPS4005x has independent clock oscillator and ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by Equation 1 and the relationship is charted in Figure 1.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 17 \right) k\Omega \quad (1)$$

7.3.2 Programming The Ramp Generator Circuit

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations because the PWM does not have to wait for loop delays before changing the duty cycle (see Figure 6).

Feature Description (continued)

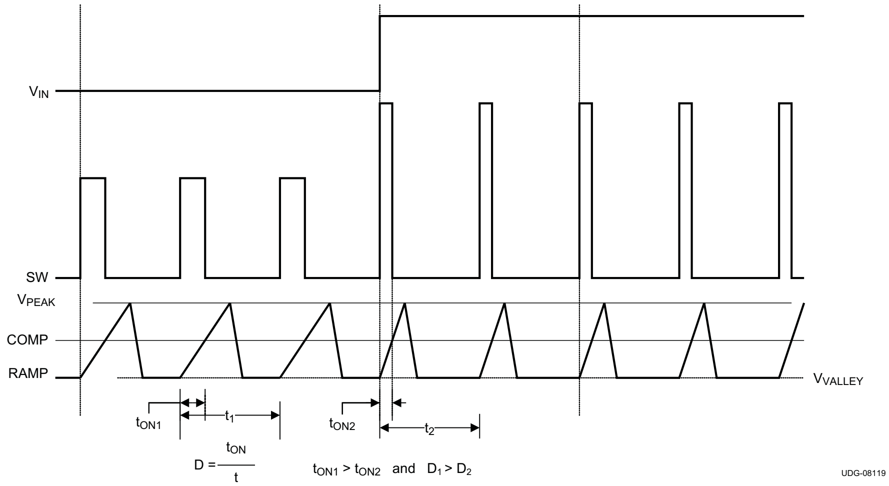


Figure 6. Voltage Feed-Forward Effect On Pwm Duty Cycle

The PWM ramp must be faster than the master clock frequency or the PWM is prevented from starting. The PWM ramp time is programmed via a single resistor (R_{KFF}) pulled up to VIN. R_{KFF} is related to R_T, and the minimum input voltage, $V_{IN(min)}$ through the following:

$$R_{KFF} = \left(V_{IN(min)} - V_{KFF}\right) \times \left(58.14 \times R_T + 1340\right)\ \Omega$$

where

- $V_{IN(min)}$ is the ensured minimum startup voltage (the actual startup voltage is nominally about 10% lower at 25°C). $V_{IN(min)}$ should be programmed equal to or greater than 8.0 V to ensure start-up and shutdown through the programmed UVLO through KFF pin.
- R_T is the timing resistance in kΩ
- V_{KFF} is the voltage at the KFF pin (typical value is 3.48 V) (2)

The curve showing the R_{KFF} required for a given switching frequency, f_{SW}, and V_{UVLO} is shown in Figure 2.

For low-input voltage and high duty-cycle applications, the voltage feed-forward may limit the duty cycle prematurely. This does not occur for most applications. The voltage control loop controls the duty cycle and regulates the output voltage. For more information on large duty cycle operation, refer to Application Note (SLUA310), *Effect of Programmable UVLO on Maximum Duty Cycle*.

7.3.3 UVLO Operation

The TPS4005x uses variable (user-programmable) UVLO protection. See the *Programming the Ramp Generator* section for more information on setting the UVLO voltage. The UVLO circuit holds the soft-start low until the input voltage exceeds the user-programmable undervoltage threshold.

The TPS4005x uses the feed-forward pin, KFF, as a user-programmable low-line UVLO detection. This variable low-line UVLO threshold compares the PWM ramp duration to the oscillator clock period. An undervoltage condition exists if the TPS4005x receives a clock pulse before the ramp has reached 90% of its full amplitude. The ramp duration is a function of the ramp slope, which is directly related to the current into the KFF pin. The KFF current is a function of the input voltage and the resistance from KFF to the input voltage. The KFF resistor can be referenced to the oscillator frequency as descibed in Equation 2.

The programmable UVLO function uses a 3-bit counter to prevent spurious shut-downs or turn-ons due to spikes or fast line transients. When the counter reaches a total of seven counts in which the ramp duration is shorter than the clock cycle, a powergood signal is asserted and a soft-start initiated, and the upper and lower MOSFETS are turned off.

Once the soft-start is initiated, the UVLO circuit must see a total count of seven cycles in which the ramp duration is longer than the clock cycle before an undervoltage condition is declared (see Figure 7).

Feature Description (continued)

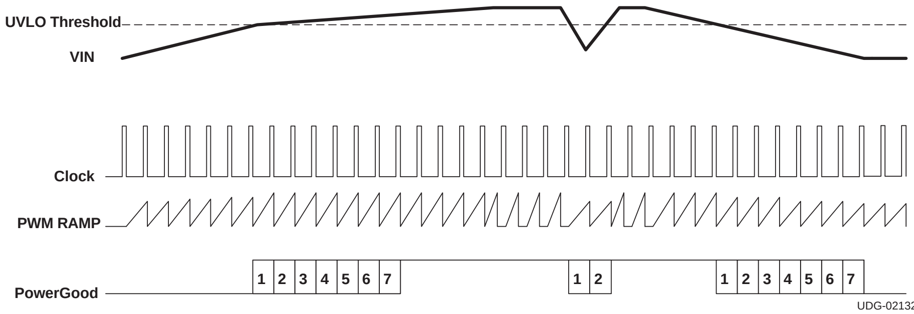


Figure 7. Undervoltage Lockout Operation

The tolerance on the UVLO set point also affects the maximum duty cycle achievable. If the UVLO starts the device at 10% below the nominal startup voltage, the maximum duty cycle is reduced approximately 10% at the nominal startup voltage.

The impedance of the input voltage can cause the input voltage, at the controller, to sag when the converter starts to operate and draw current from the input source. Therefore, there is voltage hysteresis that prevents nuisance shutdowns at the UVLO point. With R_T chosen to select the operating frequency and R_{KFF} chosen to select the startup voltage, the approximate amount of hysteresis voltage is shown in Figure 3.

Some applications may require an additional circuit to prevent false restarts at the UVLO voltage level. This applies to applications which have high impedance on the input voltage line or which have excessive ringing on the V_{IN} line. The input voltage impedance can cause the input voltage to sag enough at startup to cause a UVLO shutdown and subsequent restart. Excessive ringing can also affect the voltage seen by the device and cause a UVLO shutdown and restart. A simple external circuit provides a selectable amount of hysteresis to prevent the nuisance UVLO shutdown.

Assuming a hysteresis current of 10% I_{KFF}, and the peak detector charges to 8 V and $V_{IN(min)}$ = 10 V, the value of R_A is calculated by Equation 3 using a R_{KFF} = 71.5 kΩ.

$$R_A = \frac{R_{KFF} \times (8 - 3.48)}{0.1 \times \left(V_{IN(min)} - 3.48\right)} = 495\,k\Omega = 499\,k\Omega \tag{3}$$

C_A is chosen to maintain the peak voltage between switching cycles to keep the capacitor charge from drooping 0.1 V (from 8 V to 7.9 V).

$$C_A = \frac{(8 - 3.48)}{(R_A \times 7.9 \times f_{SW})} \tag{4}$$

The value of C_A may calculate to less than 10 pF, but some standard value up to 47 pF works adequately. The diode can be a small-signal switching diode or Schottky rated for more then 20 V. Figure 8 shows a typical implementation using a small switching diode.

The tolerance on the UVLO set point also affects the maximum duty cycle achievable. If the UVLO starts the device at 10% below the nominal startup voltage, the maximum duty cycle is reduced approximately 10% at the nominal startup voltage.

Feature Description (continued)

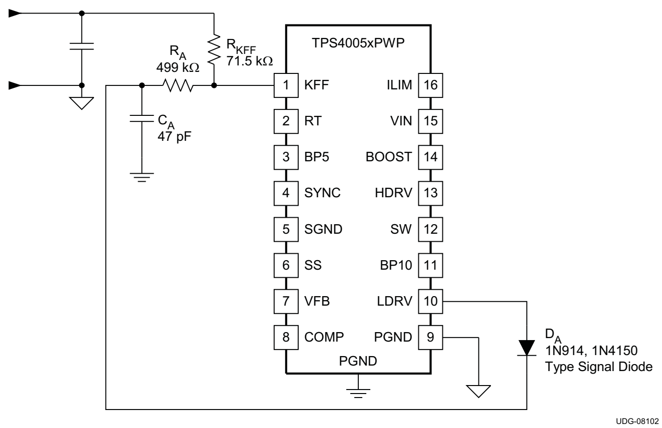


Figure 8. Hysteresis for Programmable UVLO

7.3.4 BP5 and BP10 Internal Voltage Regulators

Startup characteristics of the BP5 and BP10 regulators over different temperature ranges are shown in Figure 4 and Figure 5. Slight variations in the BP5 occurs dependent upon the switching frequency. Variation in the BP10 regulation characteristics is also based on the load presented by switching the external MOSFETs.

7.3.5 Programming Soft-Start

The TPS4005x uses a closed-loop soft-start system to ensure a controlled ramp of the output during startup. The reference voltage used for the startup is derived in the following manner. A capacitor ($C_{SS/SD}$) is connected to the SS/SD pin. There is a ramped voltage generated at this pin by charging $C_{SS/SD}$ with a current source. A value of 0.85 V is subtracted from the voltage at the SS/SSD pin and is applied to a non-inverting input of the error amplifier. This is the effective soft-start ramp voltage, V_{SSRMP}. The error amplifier also has the 0.7-V reference (V_{FB}) voltage applied to a non-inverting input. The structure of the error amplifier input stage is such that the lower of V_{FB} or V_{SSRMP} becomes the dominant voltage that the error amplifier uses to regulate the FB pin. This provides a clean, closed-loop startup while V_{SSRMP} is lower than V_{FB} and a precision reference regulated supply as V_{SSRMP} climbs above V_{FB}. To ensure a controlled ramp-up of the output voltage, the soft-start time should be greater than the L-C_O time constant as described in Equation 5.

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad \text{(seconds)}$$

where

- t_{START} is the startup ramp time in s (5)

There is a direct correlation between t_{START} and the input current required during startup. The faster t_{START}, the higher the input current required during startup. This relationship is described in more detail in the section titled, *Programming the Current Limit* which follows. The soft-start capacitance, $C_{SS/SD}$, is described in Equation 6.

For applications in which the V_{IN} supply ramps up slowly (typically between 50 ms and 100 ms), it may be necessary to increase the soft-start time to between approximately 2 ms and 5 ms to prevent nuisance UVLO tripping. The soft-start time should be longer than the time that the V_{IN} supply transitions between 6 V and 7 V.

$$C_{SS/SD} = \left(\frac{I_{SS/SD}}{V_{FB}}\right) \times t_{START} \ (F)$$

where

- $I_{SS/SD}$ is the soft-start charge current (typical value is 2.35 μA)
- V_{FB} is the feedback reference voltage (typical value is 0.7 V) (6)

Feature Description (continued)

7.3.6 Programming Current Limit

The TPS4005x uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches 7, a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed the output starts up normally. If the output is still present the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See Figure 9 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{ILIM}) is calculated in Equation 7.

$$I_{ILIM} = \left(\frac{C_O \times V_O}{t_{START}} \right) + I_{LOAD} \, (A)$$

where

- I_{LOAD} is the load current at startup (7)

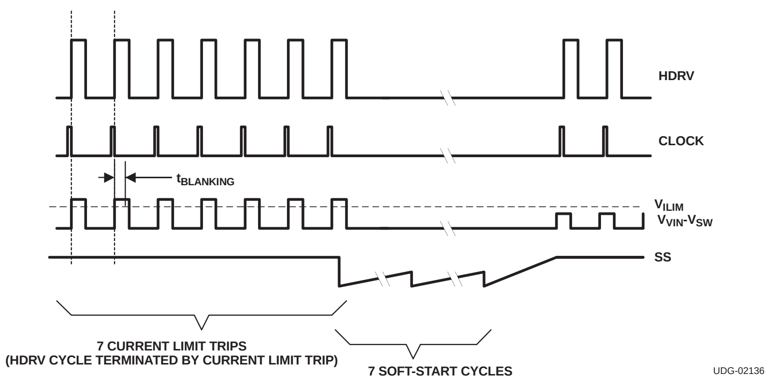


Figure 9. Typical Current Limit Protection Waveforms

The current limit programming resistor (R_{ILIM}) is calculated using Equation 8. Care must be taken in choosing the values used for V_{OS} and I_{SINK} in the equation. To ensure the output current at the overcurrent level, the minimum value of I_{SINK} and the maximum value of V_{OS} must be used. The main purpose is hard fault protection of the power switches.

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]} + V_{OS}}{1.12 \times I_{SINK}} + \frac{42.86 \times 10^{-3}}{I_{SINK}} \, (\Omega)$$

where

- I_{SINK} is the current into the ILIM pin and is 8.5 μA, minimum
- I_{OC} is the overcurrent setpoint which is the DC output current plus one-half of the peak inductor current
- V_{OS} is the overcurrent comparator offset and is –20 mV, maximum (8)

Feature Description (continued)

7.3.7 Synchronizing to an External Supply

The TPS4005x can be synchronized to an external clock through the SYNC pin. Synchronization occurs on the falling edge of the SYNC signal. The synchronization frequency should be in the range of 20% to 30% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the TPS4005x to freely run at the frequency programmed by R_T.

The higher synchronization must be factored in when programming the PWM ramp generator circuit. If the PWM ramp is interrupted by the SYNC pulse, a UVLO condition is declared and the PWM becomes disabled. Typically this is of concern under low-line conditions only. In any case, R_{KFF} needs to be adjusted for the higher switching frequency. In order to specify the correct value for R_{KFF} at the synchronizing frequency, calculate a *dummy* value for R_T that would cause the oscillator to run at the synchronizing frequency. Do not use this value of RT in the design.

$$R_{T(dummy)} = \left(\frac{1}{f_{SYNC} \times 17.82 \times 10^{-6}} - 17 \right) (k\Omega)$$

where

- f_{SYNC} is the synchronizing frequency in kHz (9)

Use the value of $R_{T(dummy)}$ to calculate the value for R_{KFF}.

$$R_{KFF} = \left(V_{IN(min)} - V_{KFF} \right) \times \left(58.14 \times R_{T(dummy)} + 1340 \right) \Omega$$

where

- $R_{T(dummy)}$ is in kΩ (10)

This value of R_{KFF} ensures that UVLO is not engaged when operating at the synchronization frequency.

7.3.8 Loop Compensation

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS4005x uses voltage feedforward control, the gain of the PWM modulator with voltage feedforward circuit must be included. The generic modulator gain is described in Figure 10. Duty cycle, D, varies from 0 to 1 as the control voltage, V_C, varies from the minimum ramp voltage to the maximum ramp voltage, V_S. Also, for a synchronous buck converter, D = V_O / V_{IN}. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage,

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S} \tag{11}$$

With the voltage feedforward function, the ramp slope is proportional to the input voltage. Therefore the moderator DC gain is independent to the change of input voltage.

For the TPS4005x, with $V_{IN(min)}$ being the minimum input voltage required to cause the ramp excursion to reach the maximum ramp amplitude of V_{RAMP}, the modulator dc gain is shown in Equation 12.

$$A_{MOD} = \left(\frac{V_{IN(min)}}{V_{RAMP}} \right) \quad \text{or} \quad A_{MOD(dB)} = 20 \times \log \left(\frac{V_{IN(min)}}{V_{RAMP}} \right) \tag{12}$$

For a buck converter using voltage mode control there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in Equation 13.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hertz)} \tag{13}$$

There is also a zero created by the output capacitance, C_O, and its associated ESR. The ESR zero is located at the frequency calculated in Equation 14.

Feature Description (continued)

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hertz)} \tag{14}$$

Calculate the value of R_{BIAS} to set the output voltage, V_O.

$$R_{BIAS} = \frac{0.7 \times R1}{V_O - 0.7} \ \Omega \tag{15}$$

The maximum crossover frequency (0 dB loop gain) is set by Equation 16.

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hertz)} \tag{16}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a –2 slope (–40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (–20 dB/decade). Figure 11 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

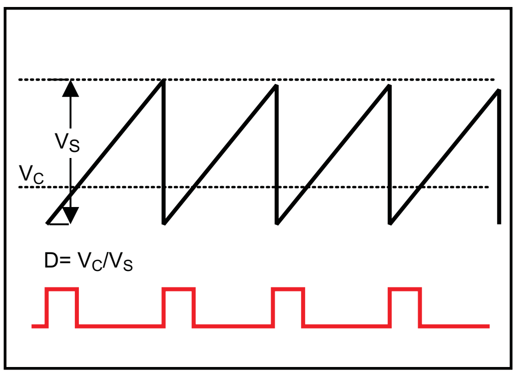


Figure 10. PWM Modulator Relationships

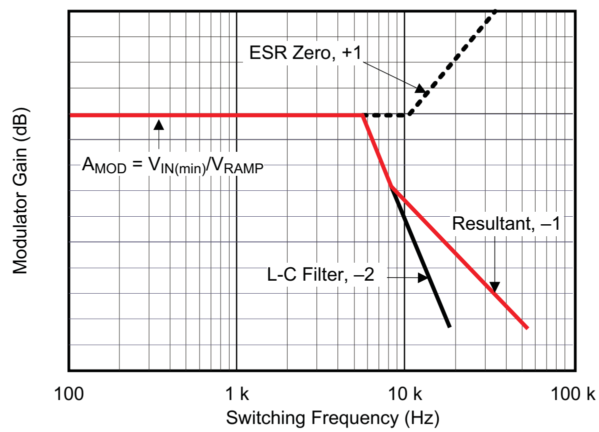


Figure 11. Modulator Gain vs Switching Frequency

A Type III topology, shown in Figure 12, has two zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in Figure 13. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases the second pole can be eliminated and the amplifier's gain roll-off used to roll-off the overall gain at higher frequencies.

Feature Description (continued)

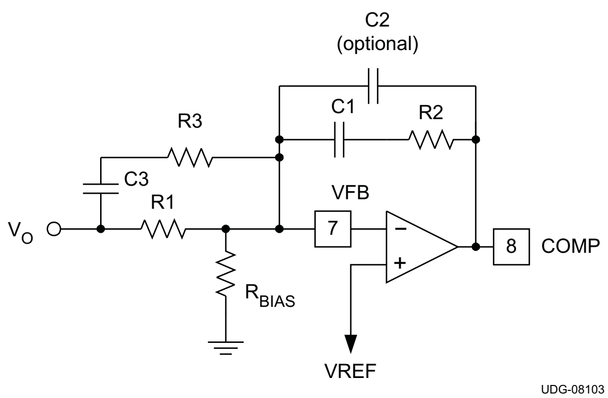


Figure 12. Type III Compensation Configuration

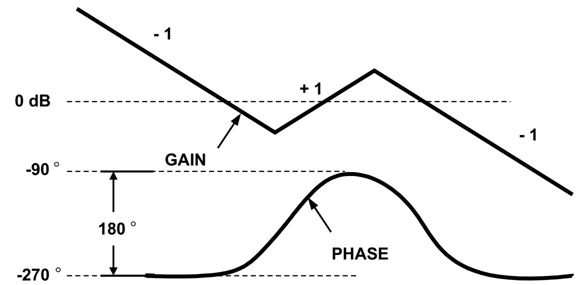


Figure 13. Type III Compensation Gain and Phase

The poles and zeros for a Type III network are described in Equation 17 through Equation 20.

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \ (Hz) \tag{17}$$

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \ (Hz) \tag{18}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \ (Hz) \tag{19}$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \ (Hz) \tag{20}$$

The value of R1 is somewhat arbitrary, but influences other component values. A value between 50 kΩ and 100 kΩ usually yields reasonable values.

The unity gain frequency is described in Equation 21.

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \quad (Hertz)$$

where

- G is the reciprocal of the modulator gain at f_C (21)

The modulator gain as a function of frequency at f_C, is described in Equation 22.

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 \text{ and } G = \frac{1}{A_{MOD(f)}} \tag{22}$$

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current which must be considered when sizing R2. A value that is too small does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\,(max)}}{I_{SOURCE\,(min)}} = \frac{3.5\ V}{2\ mA} = 1750\ \Omega \tag{23}$$

7.4 Device Functional Modes

The TPS40057 is safe for prebiased outputs, not turning on the synchronous rectifier until the high-side FET has already started switching. The TPS40054 operates in one quadrant and sources output current only, allowing for paralleling of converters and ensures that one converter does not sink current from another converter. This controller also emulates a non-synchronous buck converter at light loads where the inductor current goes discontinuous. At continuous output inductor currents the controller operates as a synchronous buck converter to optimize efficiency. The TPS40055 operates in two quadrants, sourcing and sinking output current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS4005x family of synchronous buck controllers are designed to operate over a wide range of input voltages (8 V to 40 V). These devices are used to convert a higher DC input voltage to a lower DC output voltage for a variety of applications. Use the following design procedure to select key component values for this family of devices.

8.1.1 Selecting the Inductor Value

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. An inductance that is too small results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter does not enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in Equation 24.

$$L = \frac{\left(V_{IN} - V_O\right) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad \text{(Henries)}$$

where

- V_O is the output voltage
- ΔI is the peak-to-peak inductor current (24)

8.1.2 Calculating the Output Capacitance

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst-case output ripple is described in Equation 25.

$$\Delta V = \Delta I \times \left(ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right)$$

where

- C_O is the output capacitance
- ESR is the equivalent series resistance of the output capacitance (25)

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light to heavy load step) or absorb excess inductor energy (heavy to light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop and the size of the inductor.

Application Information (continued)

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in Equation 26.

$$E_L = \frac{1}{2} \times L \times I^2 \quad \text{(Joules)} \tag{26}$$

where

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2\right] \quad \left(\text{(Amperes)}^2\right)$$

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions (27)

Energy in the capacitor is described in Equation 28.

$$E_C = \frac{1}{2} \times C \times V^2 \quad \text{(Joules)} \tag{28}$$

where

$$V^2 = \left[\left(V_f\right)^2 - \left(V_i\right)^2\right] \quad \left(\text{Volts}^2\right)$$

where

- V_f is the final peak capacitor voltage
- V_i is the initial capacitor voltage (29)

Substituting Equation 27 into Equation 26, then substituting Equation 29 into Equation 28, then setting Equation 28 equal to Equation 26, and then solving for C_O yields the capacitance described in Equation 30.

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2\right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2\right]} \quad \text{(Farads)} \tag{30}$$

8.1.3 Calculating the Boost and BP10 Bypass Capacitor

The BOOST capacitance provides a local, low impedance source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BOOST capacitance is described in Equation 31.

$$C_{BOOST} = \frac{Q_g}{\Delta V} \quad \text{(Farads)} \tag{31}$$

The 10-V reference pin, BP10V provides energy for both the synchronous MOSFET and the high-side MOSFET via the BOOST capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in Equation 32.

$$C_{BP10} = \frac{\left(Q_{gHS} + Q_{gSR}\right)}{\Delta V} \quad \text{(Farads)} \tag{32}$$

8.1.4 DV-DT Induced Turn-On

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage, on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore, the SR MOSFET should be chosen so that the Q_{GD} charge is smaller than the Q_{GS} charge.

Application Information (continued)

8.1.5 High-Side MOSFET Power Dissipation

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by Equation 33.

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25^\circ C\right]\right) \quad \text{(Watts)}$$

where

- TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$ (33)

The TC_R varies depending on MOSFET technology and manufacturer, but typically ranges between 3500 ppm/°C and 7000 ppm/°C.

The I_{RMS} current for the high-side MOSFET is described in Equation 34.

$$I_{RMS} = I_{OUT} \times \sqrt{d} \quad \left(A_{RMS}\right) \tag{34}$$

The switching losses for the high-side MOSFET are descibed in Equation 35.

$$P_{SW(fsw)} = \left(V_{IN} \times I_{OUT} \times t_{SW}\right) \times f_{SW} \quad \text{(Watts)}$$

where

- I_O is the DC output current
- t_{SW} is the switching rise time, typically < 20 ns
- f_{SW} is the switching frequency (35)

Typical switching waveforms are shown in Figure 14.

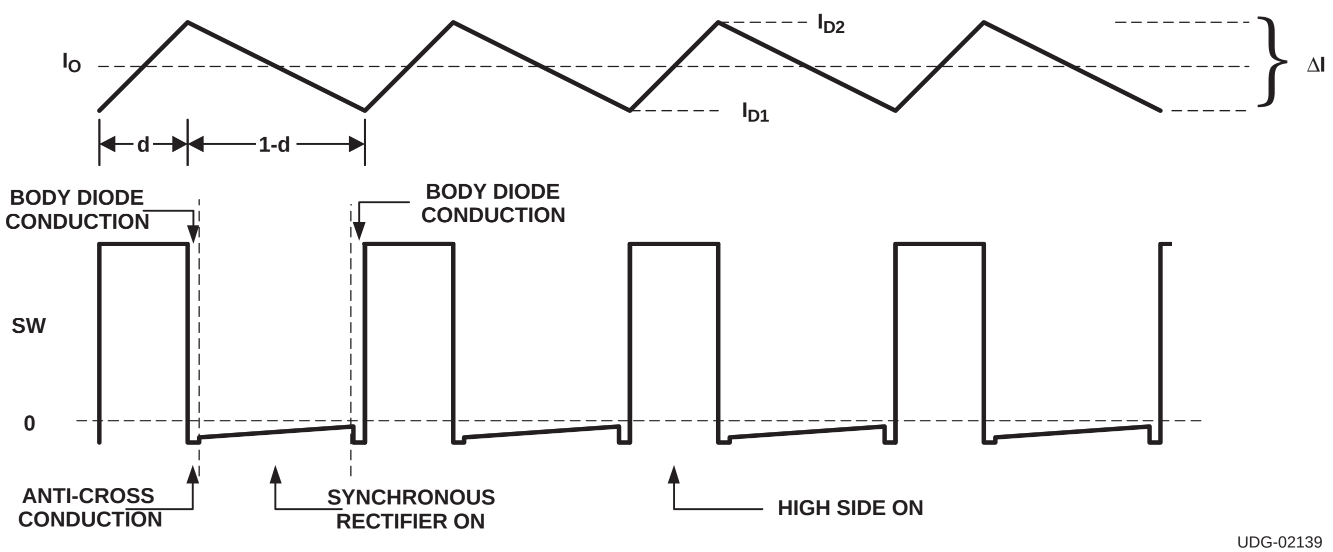


Figure 14. Inductor Current and SW Node Waveforms

The maximum allowable power dissipation in the MOSFET is determined by Equation 36.

$$P_T = \frac{\left(T_J - T_A\right)}{\theta_{JA}} \quad \text{(Watts)}$$

where

- $P_T = P_{COND} + P_{SW(fsw)}$ (W)
- θ_{JA} is the package thermal impedance (36)

Application Information (continued)

8.1.6 Synchronous Rectifier MOSFET Power Dissipation

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$ conduction losses can be defined using Equation 31 and the RMS current through the synchronous rectifier MOSFET is described in Equation 37.

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad \left(\text{Amperes}_{RMS}\right) \tag{37}$$

The body-diode conduction losses are due to forward conduction of the body diode during the anti-cross conduction delay time. The body diode conduction losses are described by Equation 38.

$$P_{DC} = 2 \times I_O \times V_F \times t_{DELAY} \times f_{SW} \quad (\text{Watts})$$

where

- V_F is the body diode forward voltage
- t_{DELAY} is the delay time just before the SW node rises (38)

The 2-multiplier is used because the body diode conducts twice during each cycle (once on the rising edge and once on the falling edge). The reverse recovery losses are due to the time it takes for the body diode to recover from a forward bias to a reverse blocking state. The reverse recovery losses are described in Equation 39.

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad (\text{Watts})$$

where

- Q_{RR} is the reverse recovery charge of the body diode (39)

The Q_{RR} is not always described in a MOSFET data sheet, but may be obtained from the MOSFET vendor. The total synchronous rectifier MOSFET power dissipation is described in Equation 40.

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad (\text{Watts}) \tag{40}$$

8.1.7 TPS4005x Power Dissipation

The power dissipation in the TPS4005x is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance, (refer to *PowerPAD Thermally Enhanced Package* [2]) can be calculated from Equation 41.

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad (\text{Watts/driver}) \tag{41}$$

And the total power dissipation in the TPS4005x, assuming the same MOSFET is selected for both the high-side and synchronous rectifier, is described in Equation 42.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad (\text{Watts}) \tag{42}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad (\text{Watts})$$

where

- I_Q is the quiescent operating current (neglecting drivers) (43)

The maximum power capability of the PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2 oz. copper trace and thermal pad with solder and no air flow,

$$\theta_{JA} = 36.515°C/W \tag{44}$$

The maximum allowable package power dissipation is related to ambient temperature by Equation 45.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \quad (\text{Watts}) \tag{45}$$

Application Information (continued)

Substituting Equation 38 into Equation 43 and solving for f_{SW} yields the maximum operating frequency for the TPS4005x. The result is described in Equation 46.

$$f_{SW} = \left(\frac{\left(\frac{(T_J - T_A)}{\theta_{JA} \times V_{IN}} \right) - I_Q}{2 \times Qg} \right) \ (Hz) \tag{46}$$

8.2 Typical Application

Figure 15 shows component selection for the 10-V to 24-V to 3.3-V at 8 A dc-to-dc converter specified in the design example. For an 8-V input application, it may be necessary to add a Schottky diode from BP10 to BOOST to get sufficient gate drive for the upper MOSFET. As seen in Figure 4, the BP10 output is about 6 V with the input at 8 V so the upper MOSFET gate drive may be less than 5 V.

A Schottky diode is shown connected across the synchronous rectifier MOSFET as an optional device that may be required if the layout causes excessive negative SW node voltage, greater than or equal to 2 V.

TPS40054-Q1, TPS40055-Q1, and TPS40057-Q1 automotive qualified versions TPS40055-EP Enhanced product 4.5 to 18V controller with power good TPS40195 4.5 to 18V controller with synchronization power good TPS40200 Wide input nonsynchronous DC-DC controller

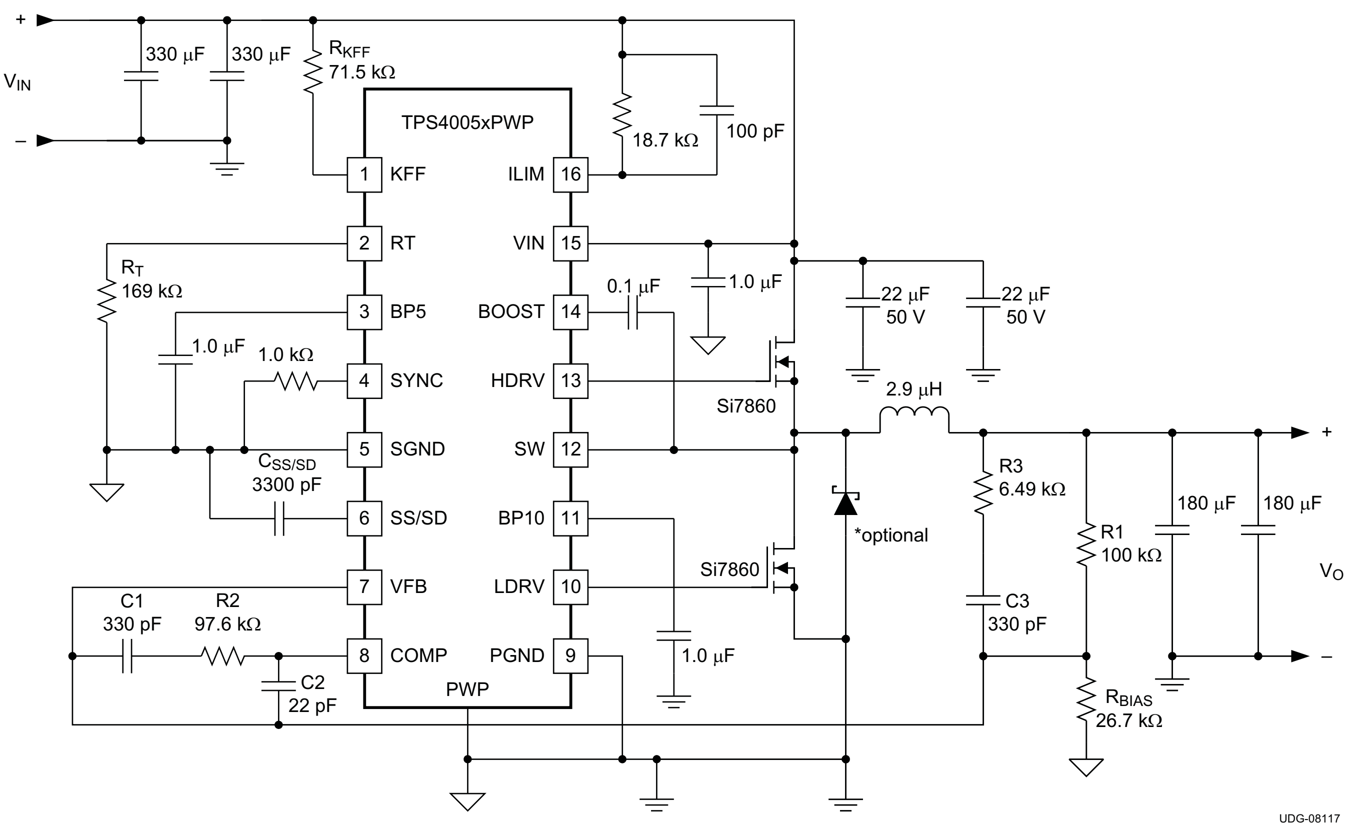


Figure 15. 24-V to 3.3-V at 8-A DC-DC Converter Design Example

8.2.1 Design Requirements

- Input voltage: 10 Vdc to 24 Vdc
- Output voltage: 3.3 V ±2% (3.234 ≤ V_O ≤ 3.366)
- Output current: 8 A (maximum, steady state), 10 A (surge, 10 ms duration, 10% duty cycle maximum)

Typical Application (continued)

- Output ripple: 33 mV_{PP} at 8 A
- Output load response: 0.3 V ≥ 10% to 90% step load change, from 1 A to 7 A
- Operating temperature: -40°C to 85°C
- f_{SW} = 300 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Calculate Maximum and Minimum Duty Cycles

$$D_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = \frac{3.234}{24} = 0.135 \qquad D_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = \frac{3.366}{10} = 0.337 \tag{47}$$

8.2.2.2 Select Switching Frequency

The switching frequency is based on the minimum duty cycle ratio and the propagation delay of the current limit comparator. In order to maintain current limit capability, the on time of the upper MOSFET, t_{ON}, must be greater than 300 ns (see *Electrical Characteristics Table*). Therefore:

$$\left(\frac{V_{O(min)}}{V_{IN(max)}}\right) = \left(\frac{t_{ON}}{t_{SW}}\right) \text{ or } \frac{1}{t_{SW}} = f_{SW} = \left(\frac{\left(\frac{V_{O(min)}}{V_{IN(max)}}\right)}{t_{ON}}\right) \tag{48}$$

Using 400 ns to provide margin,

$$f_{SW} = \frac{0.135}{400\text{ ns}} = 337\text{ kHz} \tag{49}$$

Since the oscillator can vary by 10%, decrease f_{SW}, by 10%

$$f_{SW} = 0.9 \times 337\text{ kHz} = 303\text{ kHz}$$

and therefore choose a frequency of 300 kHz.

8.2.2.3 Select Δi

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 8 \times 2 \times 0.2 = 3.2\text{ A} \tag{50}$$

8.2.2.4 Calculate the High-Side MOSFET Power Losses

Power losses in the high-side MOSFET (Si7860DP) at 24-V_{IN} where switching losses dominate can be calculated from Equation 51.

$$I_{RMS} = I_O \times \sqrt{d} = 8 \times \sqrt{0.135} = 2.93\text{ A} \tag{51}$$

Substituting Equation 34 into Equation 33 yields

$$P_{COND} = 2.93^2 \times 0.008 \times (1 + 0.007 \times (150 - 25)) = 0.129\text{ W} \tag{52}$$

and from Equation 35, the switching losses can be determined.

$$P_{SW(fsw)} = \left(V_{IN} \times I_O \times t_{SW}\right) \times f_{SW} = 24\text{ V} \times 8\text{ A} \times 20\text{ ns} \times 300\text{ kHz} = 1.152\text{ W} \tag{53}$$

The MOSFET junction temperature can be found by substituting Equation 52 and Equation 53 into Equation 36:

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A = (0.129 + 1.152) \times 40 + 85 = 136°\text{C} \tag{54}$$

Typical Application (continued)

8.2.2.5 Calculate Synchronous Rectifier Losses

The synchronous rectifier MOSFET has two loss components, conduction, and diode reverse recovery losses. The conduction losses are due to I_{RMS} losses as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The I_{RMS} current through the synchronous rectifier from Equation 37:

$$I_{RMS} = I_O \times \sqrt{1 - d} = 8 \times \sqrt{1 - 0.135} = 7.44\ A_{RMS} \quad (55)$$

The synchronous MOSFET conduction loss from Equation 33 is:

$$P_{COND} = 7.44^2 \times 0.008 \times (1 + 0.007 \times (150 - 25)) = 0.83\ W \quad (56)$$

The body diode conduction loss from Equation 38 is:

$$P_{DC} = 2 \times I_O \times V_{FD} \times t_{DELAY} \times f_{SW} = 2 \times 8.0\ A \times 0.8\ V \times 100\ ns \times 300\ kHz = 0.384 \quad (57)$$

The body diode reverse recovery loss from Equation 39 is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} = 0.5 \times 30\ nC \times 24\ V \times 300\ kHz = 0.108\ W \quad (58)$$

The total power dissipated in the synchronous rectifier MOSFET from Equation 40 is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.108 + 0.83 + 0.384 = 1.322\ W \quad (59)$$

The junction temperature of the synchronous rectifier at 85°C is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (1.322) \times 40 + 85 = 139^oC \quad (60)$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

8.2.2.6 Calculate the Inductor Value

The inductor value is calculated from Equation 24.

$$L = \frac{(24 - 3.3\ V) \times 3.3\ V}{24\ V \times 3.2\ A \times 300\ kHz} = 2.96\ \mu H \quad (61)$$

A 2.9-µH Coev DXM1306-2R9 or 2.6-µH Panasonic ETQ-P6F2R9LFA can be used.

8.2.2.7 Set the Switching Frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be found from Equation 1, with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 17 \right) k\Omega = 170\ k\Omega \quad \therefore\ \text{use } 169\ k\Omega \quad (62)$$

8.2.2.8 Program the Ramp Generator Circuit

The PWM ramp is programmed through a resistor (R_{KFF}) from the KFF pin to V_{IN}. The ramp generator also controls the input UVLO voltage. For an undervoltage level of 10 V, R_{KFF} can be calculated from Equation 2:

$$R_{KFF} = (V_{IN(min)} - 3.48) \times (58.14 \times R_T + 1340) = 72.8 k\Omega \quad \therefore \text{use } 71.5 k\Omega \quad (63)$$

8.2.2.9 Calculate the Output Capacitance (C_O)

In this example the output capacitance is determined by the load response requirement of ΔV = 0.3 V for a 1-A to 8-A step load. C_O can be calculated using Equation 30:

Typical Application (continued)

$$C_O = \frac{2.9\,\mu \times \left((8\text{ A})^2 - (1\text{ A})^2\right)}{\left((3.3)^2 - (3.0)^2\right)} = 97\,\mu\text{F} \tag{64}$$

Using Equation 25 calculate the ESR required to meet the output ripple requirements.

$$33\,\text{mV} = 3.2\,\text{A}\left(\text{ESR} + \left(\frac{1}{8 \times 97\,\mu\text{F} \times 300\,\text{kHz}}\right)\right) \tag{65}$$

$$\text{ESR} = 10.3\,\text{m}\Omega - 4.3\,\text{m}\Omega = 6.0\,\text{m}\Omega \tag{66}$$

For this design example two Panasonic SP EEFUEOJ1B1R capacitors, (6.3 V, 180 µF, 12 mΩ) are used.

8.2.2.10 Calculate the Soft-Start Capacitor ($C_{SS/SD}$)

This design requires a soft-start time (t_{START}) of 1 ms. $C_{SS/SD}$ can be calculated using Equation 6:

$$C_{SS/SD} = \frac{2.35\,\mu\text{A}}{0.7\,\text{V}} \times 1\,\text{ms} = 3.36\,\text{nF} \cong 3300\,\text{pF} \tag{67}$$

8.2.2.11 Calculate the Current Limit Resistor (R_{ILIM})

The current limit set point depends on t_{START}, V_O,C_O and I_{LOAD} at startup as shown in Equation 7. For this design,

$$I_{ILIM} > \frac{360\,\mu\text{F} \times 3.3\,\text{V}}{1\,\text{ms}} + 8.0\,\text{A} = 9.2\,\text{A} \tag{68}$$

For this design, add I_{ILIM} (9.2 A) to one-half the ripple current (1.6 A) and increase this value by 30% to allow for tolerances. This yields a overcurrent setpoint (I_{OC}) of 14 A. $R_{DS(on)}$ is increased 30% (1.3 × 0.008) to allow for MOSFET heating. Using Equation 8 to calculate R_{ILIM}.

$$R_{ILIM} = \frac{14 \times 0.0104 - 0.020}{1.12 \times 8.5 \times 10^{-6}} + \frac{42.86 \times 10^{-3}}{8.5 \times 10^{-6}} = 18.24\,\text{k}\Omega \cong 18.7\,\text{k}\Omega \tag{69}$$

8.2.2.12 Calculate Loop Compensation Values

Calculate the DC modulator gain (A_{MOD}) from Equation 12:

$$A_{MOD} = \frac{10}{2} = 5.0 \qquad A_{MOD(dB)} = 20 \times \log(5) = 14\text{ dB} \tag{70}$$

Calculate the output filter L-C_O poles and C_OESR zeros from Equation 13 and Equation 14:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_O}} = \frac{1}{2\pi\sqrt{2.9\,\mu\text{H} \times 360\,\mu\text{F}}} = 4.93\text{ kHz} \tag{71}$$

and

$$f_Z = \frac{1}{2\pi \times \text{ESR} \times C_O} = \frac{1}{2\pi \times 0.006 \times 360\,\mu\text{F}} = 73.7\text{ kHz} \tag{72}$$

Select the close-loop 0 dB crossover frequency, f_C. For this example f_C = 20 kHz.

Select the double zero location for the Type III compensation network at the output filter double pole at 4.93 kHz.

Select the double pole location for the Type III compensation network at the output capacitor ESR zero at 73.7 kHz.

The amplifier gain at the crossover frequency of 20 kHz is determined by the reciprocal of the modulator gain AMOD at the crossover frequency from Equation 22:

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 = 5 \times \left(\frac{4.93\text{ kHz}}{20\text{ kHz}}\right)^2 = 0.304 \tag{73}$$

Typical Application (continued)

And also from Equation 22:

$$G = \frac{1}{A_{MOD(f)}} = \frac{1}{0.304} = 3.29 \tag{74}$$

Choose R1 = 100 kΩ

The poles and zeros for a type III network are described in Equation 17 through Equation 21.

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \therefore C3 = \frac{1}{2\pi \times 100\ k\Omega \times 4.93\ kHz} = 323\ pF,\ \text{choose } 330\ pF \tag{75}$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \therefore R3 = \frac{1}{2\pi \times 330\ pF \times 73.3\ kHz} = 6.55\ k\Omega,\ \text{choose } 6.49\ k\Omega \tag{76}$$

$$f_{C} = \frac{1}{2\pi \times R1 \times C2 \times G} \therefore C2 = \frac{1}{2\pi \times 100\ k\Omega \times 3.29 \times 20\ kHz} = 24.2\ pF,\ \text{choose } 22\ pF \tag{77}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \therefore R2 = \frac{1}{2\pi \times 22\ pF \times 73.3\ kHz} = 98.2\ k\Omega,\ \text{choose } 97.6\ k\Omega \tag{78}$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \therefore C1 = \frac{1}{2\pi \times 97.6\ k\Omega \times 4.93\ kHz} = 331\ pF,\ \text{choose } 330\ pF \tag{79}$$

Calculate the value of R_{BIAS} from Equation 15 with R1 = 100 kΩ.

$$R_{BIAS} = \frac{0.7\ V \times R1}{V_O - 0.7\ V} = \frac{0.7\ V \times 100k\Omega}{3.3\ V - 0.7\ V} = 26.9\ k\Omega,\ \text{choose } 26.7\ k\Omega \tag{80}$$

8.2.2.13 Calculate the Boost and BP10V Bypass Capacitance

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass capacitor. The BOOST capacitance for the Si7860DP, allowing for a 0.5 voltage droop on the BOOST pin from Equation 31 is:

$$C_{BOOST} = \frac{Q_g}{\Delta V} = \frac{18\ nC}{0.5\ V} = 36\ nF \tag{81}$$

and the BP10V capacitance from Equation 32 is

$$C_{BP(10\ V)} = \frac{Q_{gHS} + Q_{gSR}}{\Delta V} = \frac{2 \times Q_g}{\Delta V} = \frac{36\ nC}{0.5\ V} = 72\ nF \tag{82}$$

For this application, a 0.1-µF capacitor is used for the BOOST bypass capacitor and a 1.0-µF capacitor is used for the BP10V bypass.

Typical Application (continued)

8.2.3 Application Curves

The TPS40055EVM-001 application curves are shown in Figure 16 to Figure 20 for reference.

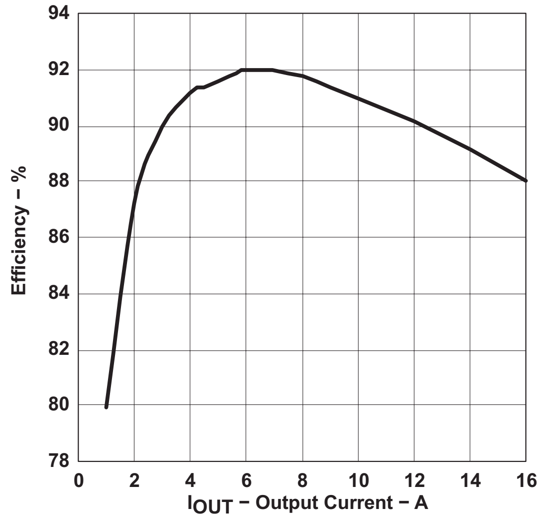


Figure 16. Efficiency vs. Load

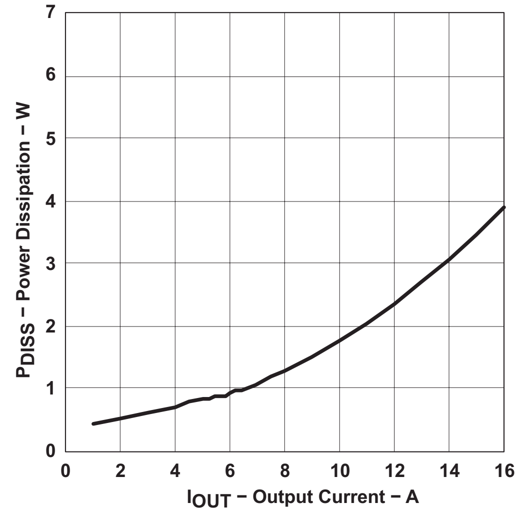


Figure 17. Power Dissipation vs. Load

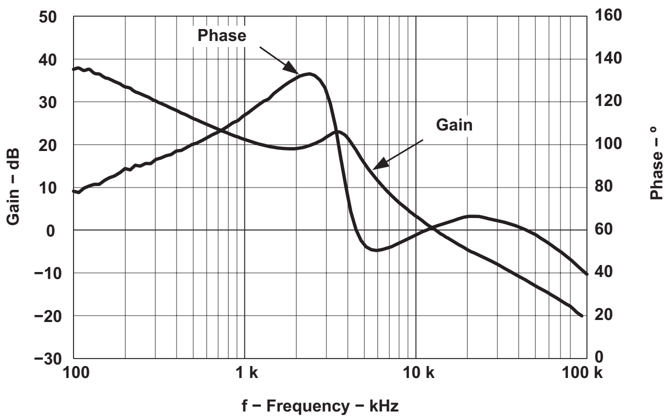


Figure 18. Overall Gain and Phase vs. Frequency

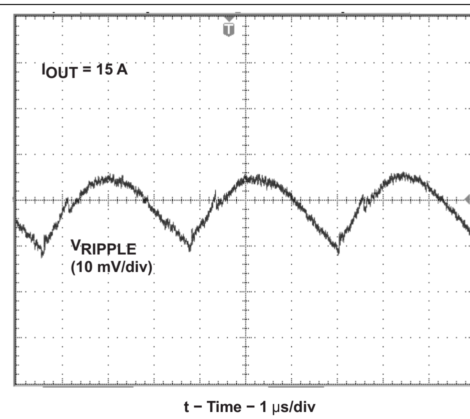


Figure 19. Output Voltage Ripple

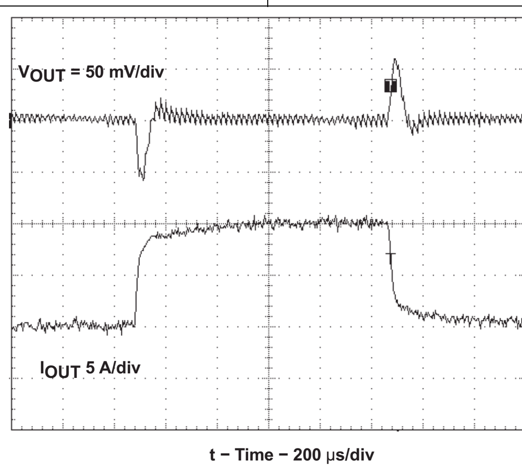


Figure 20. Transient Response

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 8 V and 40 V. This supply must be well regulated. Proper bypassing of input supplies and internal regulators is critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

10 Layout

10.1 Layout Guidelines

The TPS4005x provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor should be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10 and BP5) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW).

10.2 Layout Example

The TPS40055EVM-001 layout is shown in Figure 21 to Figure 25 for reference.

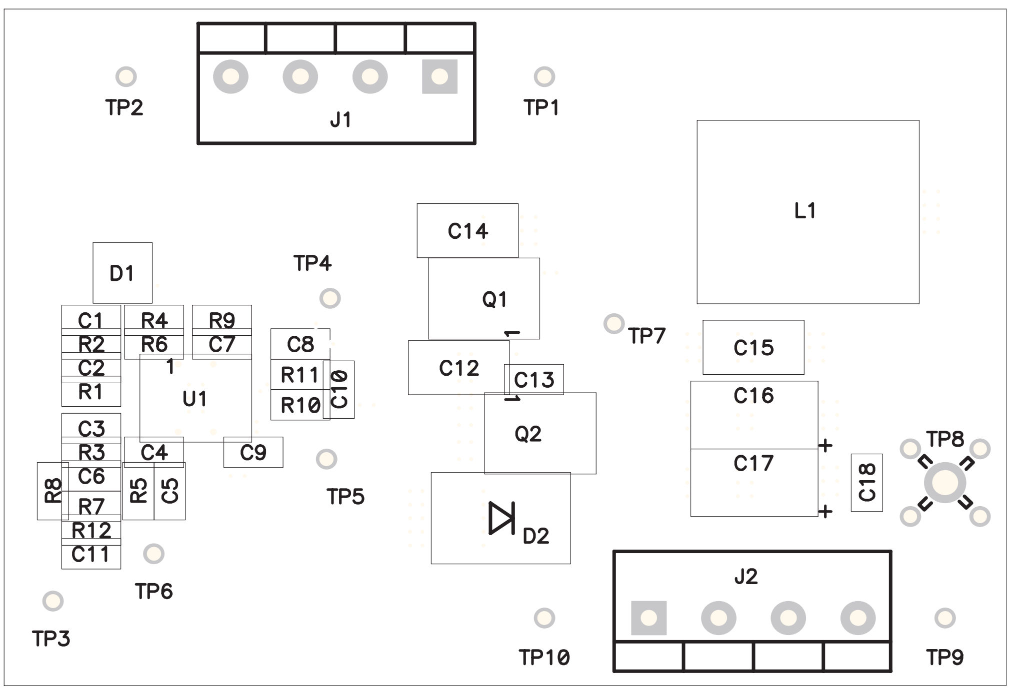


Figure 21. Top Side Component Assembly

Layout Example (continued)

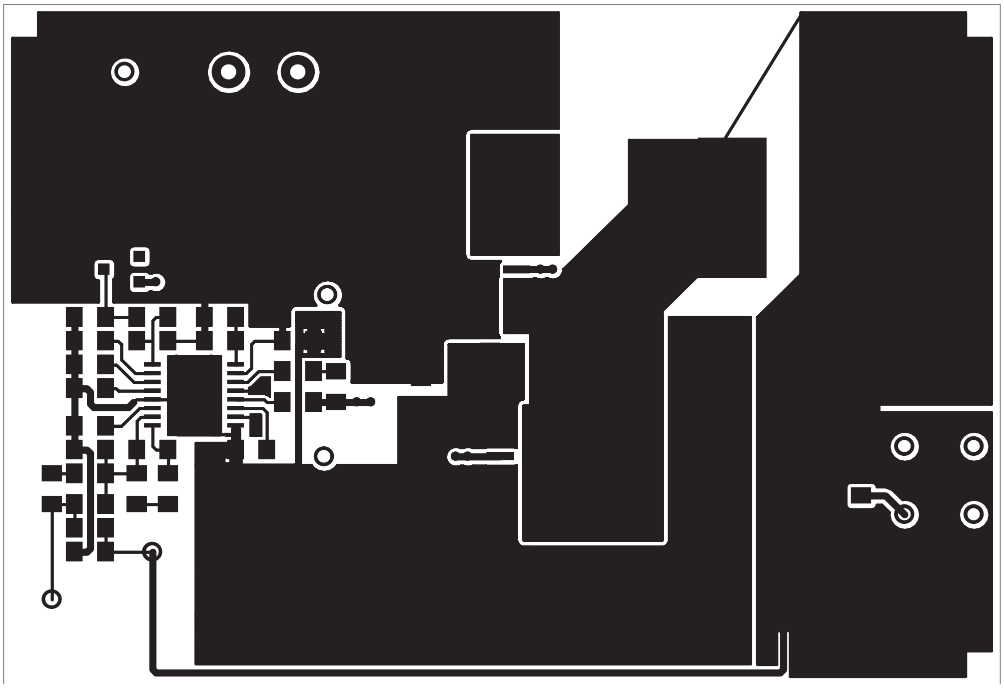


Figure 22. Top Side Copper

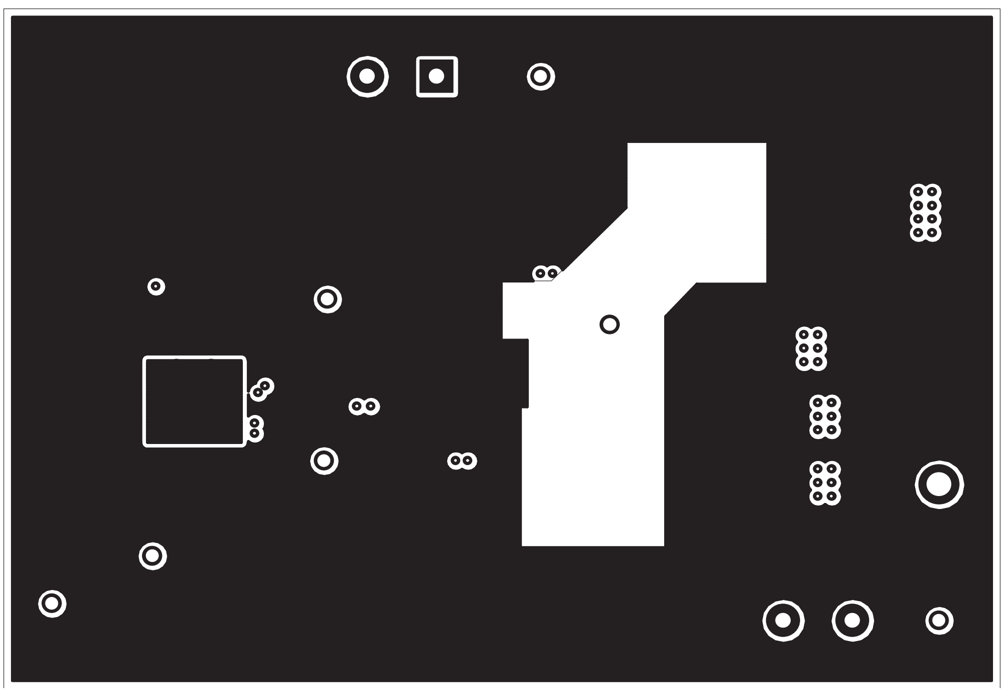


Figure 23. Internal Layer 1 Copper

Layout Example (continued)

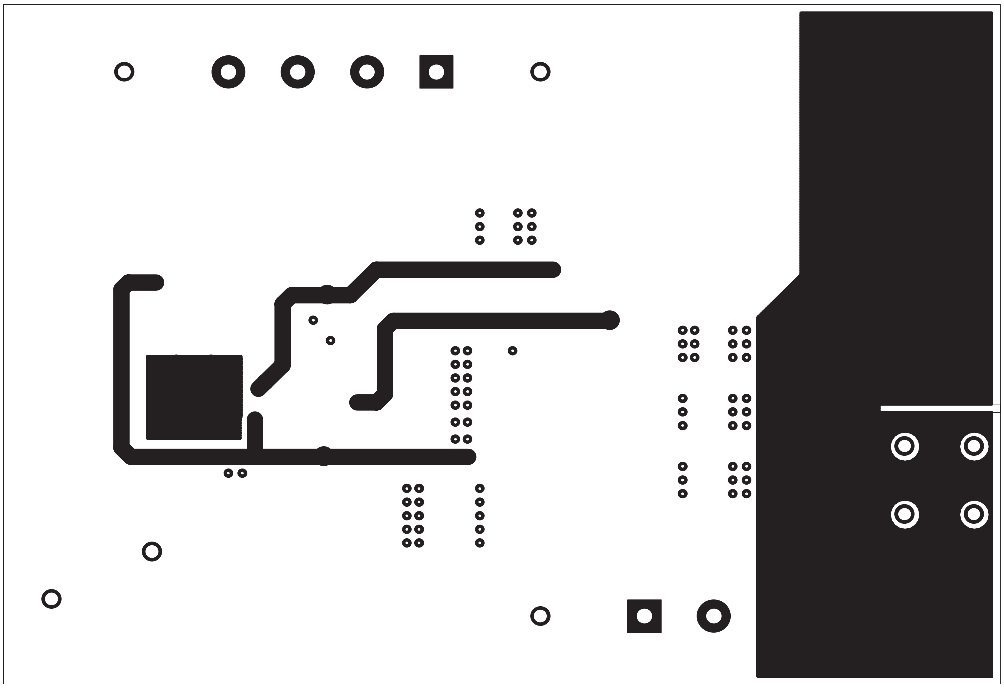


Figure 24. Internal Layer 2 Copper

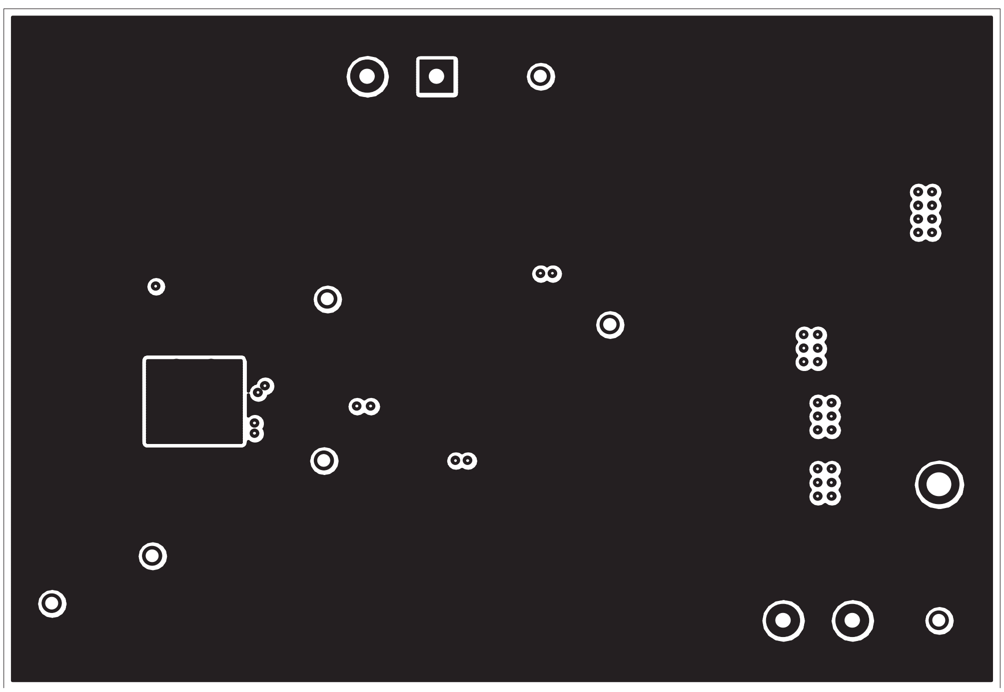


Figure 25. Bottom Layer Copper

10.3 MOSFET Packaging

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA} specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a lowest thermal impedance of 40°C/W requires one square inch of 2-ounce copper on a G-10/FR-4 board. Lower thermal impedances can be achieved at the expense of board area. Please refer to the selected MOSFET's data sheet for more information regarding proper mounting.

11 Device and Documentation Support

11.1 Device Support

The following devices have characteristics similar to the TPS40054/5/7 and may be of interest.

Table 1. Related Devices

DEVICE	DESCRIPTION
TPS40055-EP	Enhanced performance TPS40055.
TPS40054-Q1	Automotive qualified versions of the TPS4005x series.
TPS40057-Q1	
TPS40055-Q1	
TPS40192	4.5-V to 18-V Controller with Synchronization Power Good
TPS40193	
TPS40200	Wide-Input Nonsynchronous DC-DC Controller

11.2 Documentation Support

11.2.1 Related Documentation

- Balogh, Laszlo, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM-1400 Topic 2.
- *PowerPAD Thermally Enhanced Package* Texas Instruments, Semiconductor Group, Technical Brief (SLMA002)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS40054	Click here	Click here	Click here	Click here	Click here
TPS40055	Click here	Click here	Click here	Click here	Click here
TPS40057	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40054PWP	NRND	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054	
TPS40054PWPG4	NRND	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054	
TPS40054PWPR	NRND	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054	
TPS40054PWPRG4	NRND	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40054	
TPS40055PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055	Samples
TPS40055PWPG4	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055	Samples
TPS40055PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055	Samples
TPS40055PWPRG4	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40055	Samples
TPS40057PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057	Samples
TPS40057PWPG4	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057	Samples
TPS40057PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057	Samples
TPS40057PWPRG4	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40057	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS40055 :

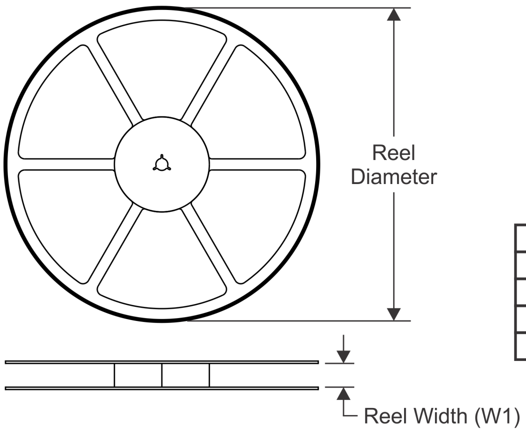
- Enhanced Product : TPS40055-EP

NOTE: Qualified Version Definitions:

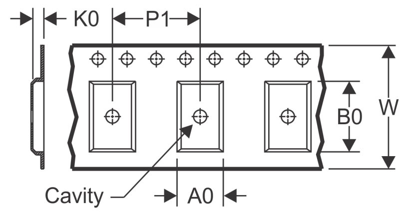
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

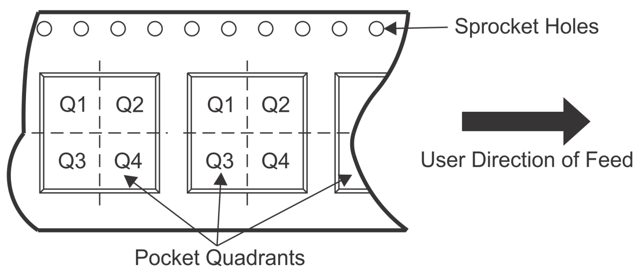


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

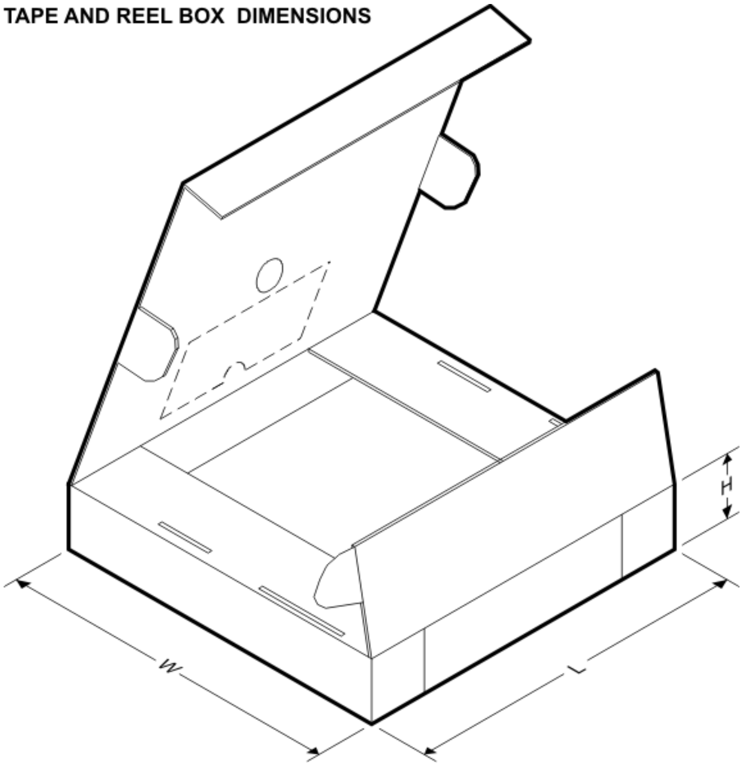
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40054PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS40055PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS40057PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

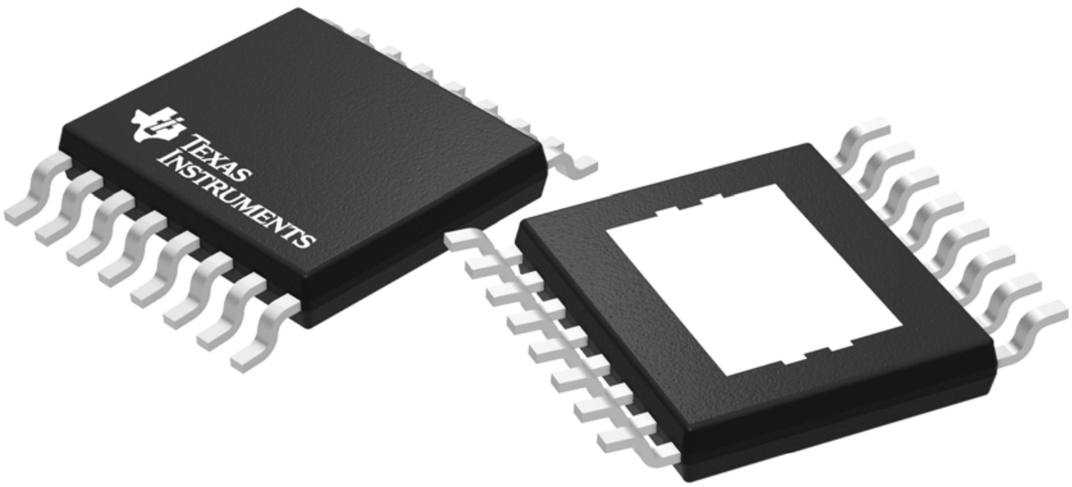


*All dimensions are nominal

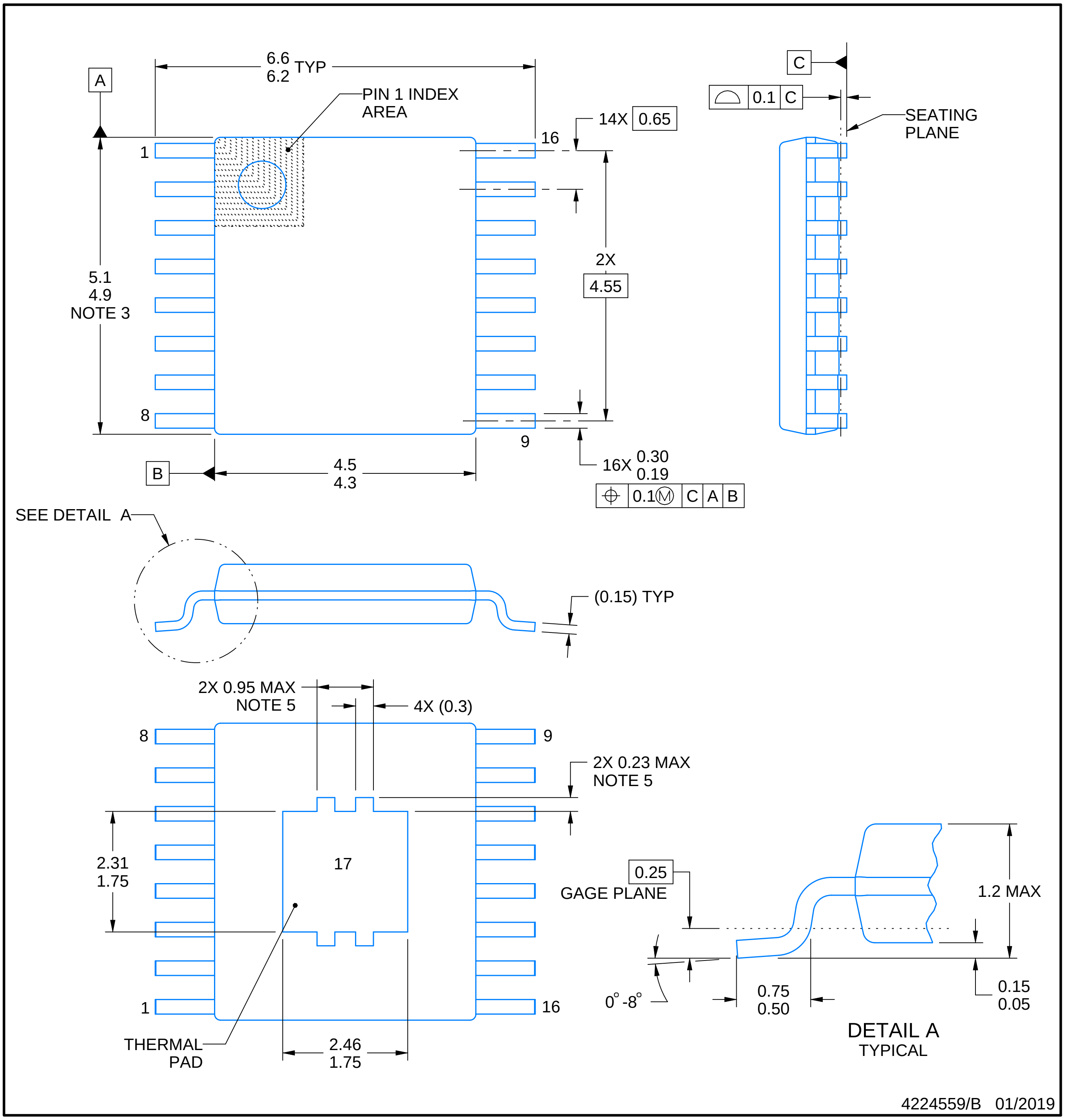
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40054PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS40055PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS40057PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

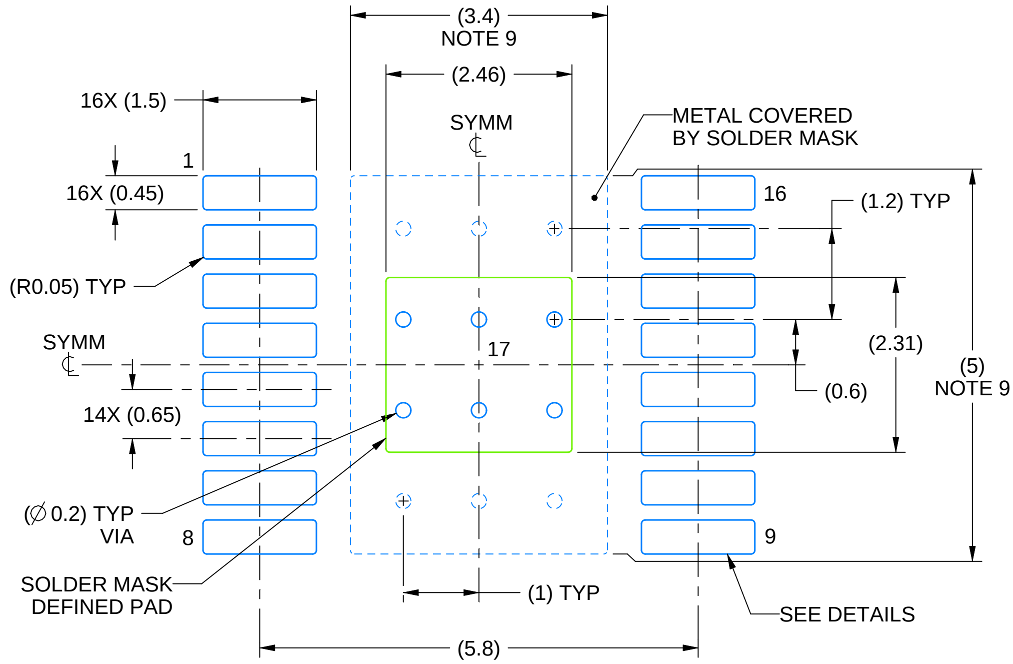


4224559/B 01/2019

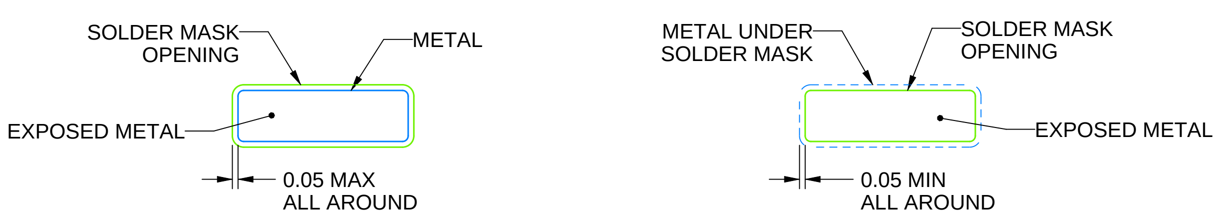
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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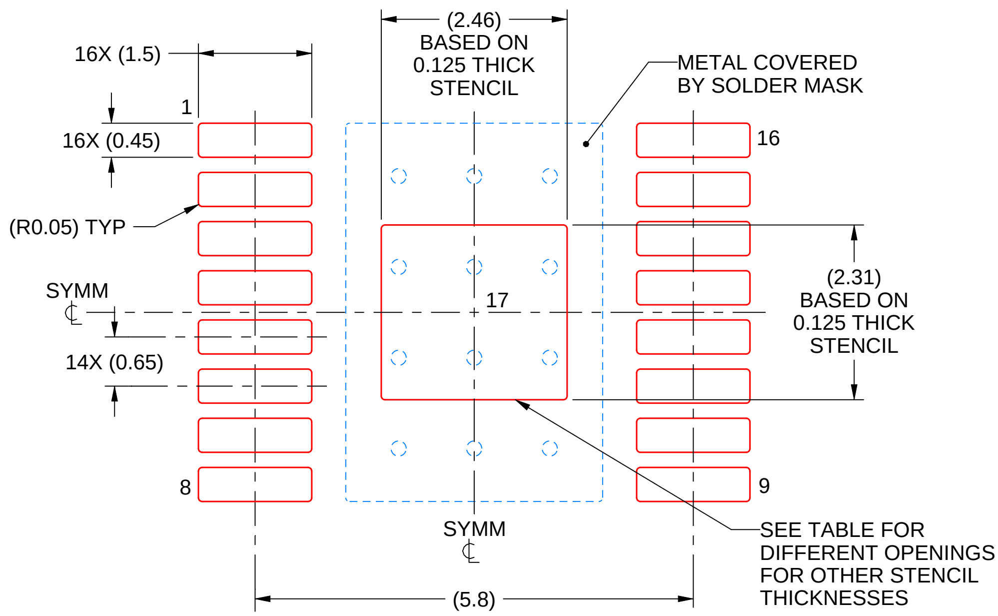
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

单击下面可查看定价，库存，交付和生命周期等信息

[>>TI(德州仪器)]