TPS715 50-mA, 24-V, 3.2-µA Supply Current Low-Dropout Linear Regulator in SC70 Package

1 Features

- 24-V Maximum Input Voltage
- Low 3.2-µA Quiescent Current at 50 mA
- Stable With Any Capacitor ≥ 0.47 µF
- 50-mA Low-Dropout Regulator
- Available in 1.8 V, 1.9 V, 2.3 V, 2.5 V, 3 V, 3.3 V, 3.45 V, 5 V, and Adjustable (1.2 V to 15 V)
- Designed to Support MSP430 Families:
  - 1.9-V Version Ensured to be Higher Than Minimum V_{IN} of 1.8 V
  - 2.3-V Version Ensured to Meet 2.2-V Minimum V_{IN} for Flash on MSP430F2xx
  - 3.45-V Version Ensured to be Lower Than Maximum V_{IN} of 3.6 V
  - Wide Variety of Fixed-Output Voltage Options to Match V_{IN} to the Minimum Required for Desired MSP430 Speed
- Minimum and Maximum Specified Current Limit
- 5-Pin SC70 (DCK)
- –40°C to +125°C Specified Junction Temperature Range
- For 80-mA Rated Current and Higher Power Package, see TPS715A

2 Applications

- Ultralow Power Microcontrollers
- Cellular and Cordless Handsets
- Portable and Battery-Powered Equipment

3 Description

The TPS715 low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor greater than or equal to 0.47 µF. The low dropout voltage and low quiescent current allow operation at extremely low power levels. Therefore, the devices are ideal for powering battery management ICs. Specifically, because the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery charging ICs.

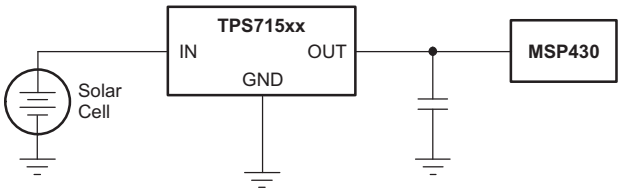
The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the low dropout voltage, typically 415 mV at 50 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 µA typically) is stable over the entire range of output load current (0 mA to 50 mA).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS715	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Q (January 2014) to Revision R — **Page**

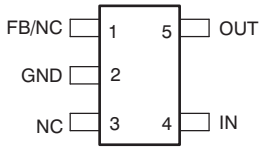
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed front-page figure ... 1
- Changed *Pin Configuration and Functions* section; updated table format ... 3
- Deleted *Continuous total power dissipation* row in *Absolute Maximum Ratings* ... 4

Changes from Revision P (November 2008) to Revision Q — **Page**

- Changed test condition for V_{OUT} accuracy parameter ... 5

5 Pin Configuration and Functions

DCK PACKAGE
5-Pin SC70
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70			
	FIXED	ADJUSTABLE		
FB	—	1	I	Adjustable version only. This terminal is used to set the output voltage.
GND	2	2	—	Ground
IN	4	4	I	Input supply
NC	1, 3	3	—	No connection
OUT	5	5	O	Output of the regulator. Any output capacitor ≥ 0.47 µF can be used for stability.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted).(1)(2)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	24	V
	V_{OUT}	–0.3	16.5	
Peak output current		Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
I_{OUT}	Output current	0		50	mA
C_{IN}	Input capacitor	0	0.047		µF
C_{OUT}	Output capacitor	0.47	1		µF

6.4 Thermal Information

THERMAL METRIC(1)		TPS715 DCK [SC70] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	84.6	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	83.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)		I_O = 10 mA	2.5		24	V
			I_O = 50 mA	3		24	
V_{OUT}	Output voltage (TPS71501)			1.2		15	V
V_{OUT}	Accuracy(1)	Over V_{IN}, I_{OUT}, and T	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V 100 µA ≤ I_{OUT} ≤ 50 mA	–4%		4%	
I_{GND}	Ground pin current(2)		0 ≤ I_{OUT} ≤ 50 mA, T_J = –40°C to 85°C		3.2	4.2	µA
			0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.8	
			0 mA ≤ I_{OUT} ≤ 50 mA, V_{IN} = 24 V			5.8	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		I_{OUT} = 100 µA to 50 mA		22		mV
$\Delta V_{OUT(\Delta VIN)}$	Output voltage line regulation (1)		V_{OUT} + 1 V < V_{IN} ≤ 24 V		20	60	mV
V_n	Output noise voltage		BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
I_{CL}	Output current limit		V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		750	mA
			V_{OUT} = 0 V, V_{IN} < 3.5 V	90		750	mA
PSRR	Power-supply ripple rejection		f = 100 kHz, C_{OUT} = 10 µF		60		dB
V_{DO}	Dropout voltage V_{IN} = $V_{OUT(nom)}$ – 0.1 V		I_{OUT} = 50 mA		415	750	mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) See Figure 10. The TPS715 family employs a leakage null control circuit. This circuit is active only if output current is less than pass FET leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.

6.6 Typical Characteristics

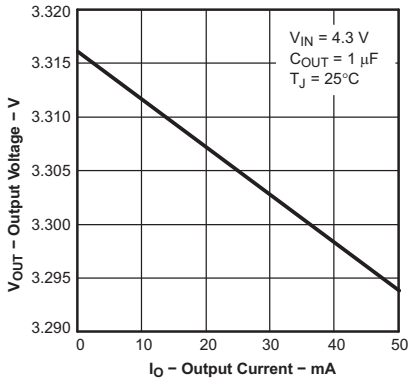


Figure 1. Output Voltage vs Output Current

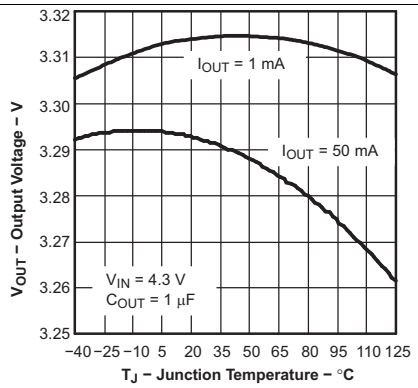


Figure 2. Output Voltage vs Junction Temperature

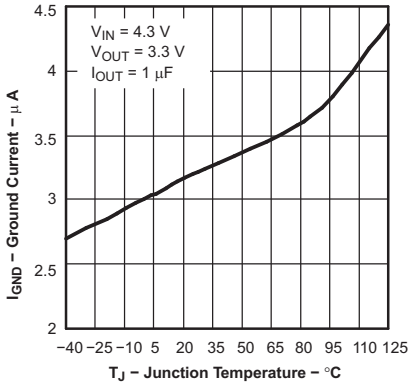


Figure 3. Quiescent Current vs Junction Temperature

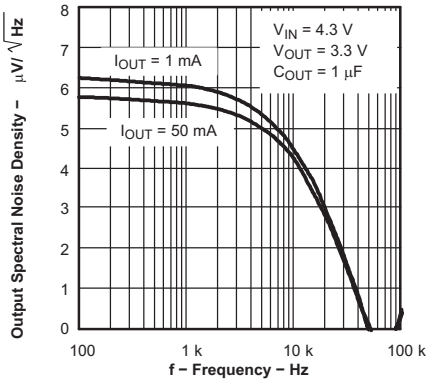


Figure 4. Output Spectral Noise Density vs Frequency

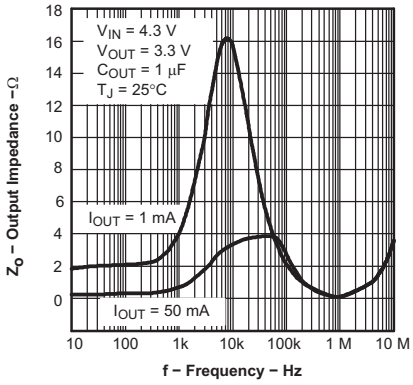


Figure 5. Output Impendence vs Frequency

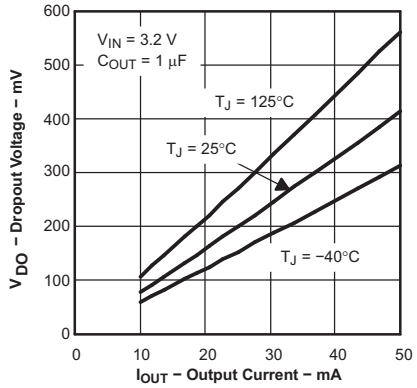


Figure 6. Dropout Voltage vs Output Current

Typical Characteristics (continued)

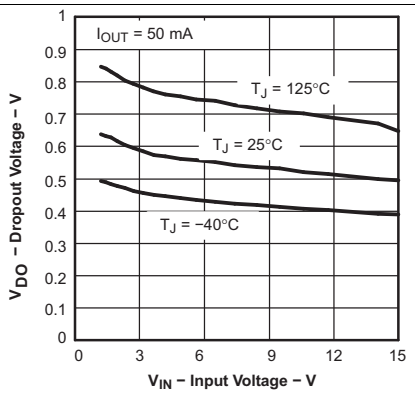


Figure 7. TPS71501 Dropout Voltage vs Input Voltage

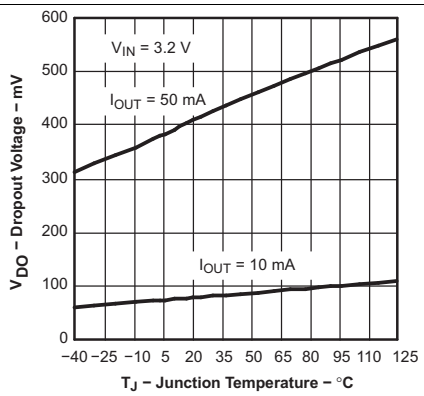


Figure 8. Dropout Voltage vs Junction Temperature

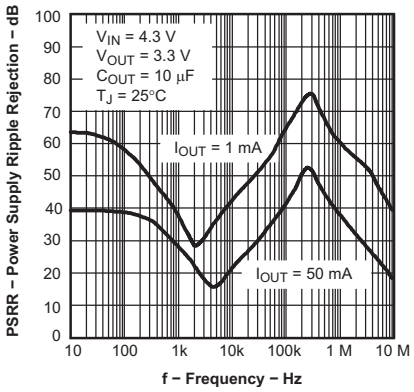


Figure 9. Power Supply Ripple Rejection vs Frequency

7 Detailed Description

7.1 Overview

The TPS715 family of LDOs consume only 3.2 µA of current while offering a wide input voltage range and low-dropout voltage in a small package. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor greater than or equal to 0.47 µF. The low quiescent current makes the TPS715 ideal for powering battery management ICs. Specifically, because the TPS715 is enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery charging ICs.

7.2 Functional Block Diagrams

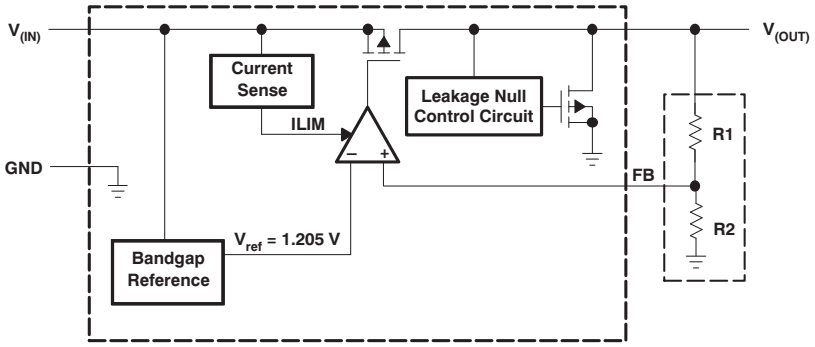


Figure 10. Functional Block Diagram—Adjustable Version

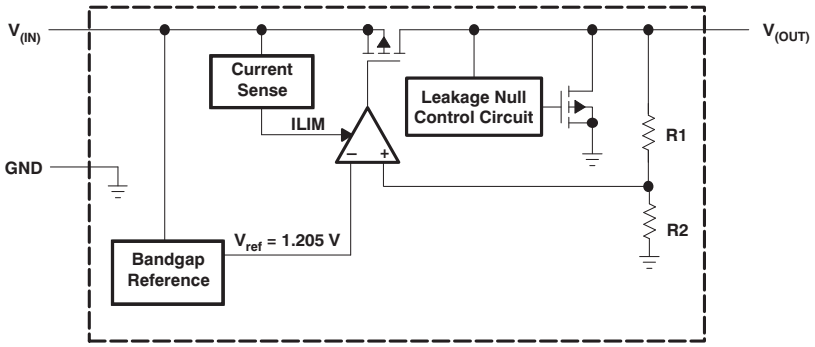


Figure 11. Functional Block Diagram—Fixed Version

7.3 Feature Description

7.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is ideal for applications that have either large transients or high DC voltage supplies.

7.3.2 Low Supply Current

This device only requires 3.2 µA (typical) of supply current from –40°C to 85°C and has a maximum current consumption of 5.8 µA at –40°C to 125°C.

7.3.3 Stable With Any Capacitor ≥ 0.47 µF

Any capacitor, including both ceramic and tantalum, greater than or equal to 0.47 µF properly stabilizes this loop.

Feature Description (continued)

7.3.4 Internal Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases.

NOTE

if a current limit occurs and the resulting output voltage is low, excessive power is dissipated across the LDO, resulting in possible damage to the device.

7.3.5 Reverse Current

The TPS715 PMOS-pass transistor has a built-in back diode that conducts current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be required.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Disabled	—	—

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than 125°C.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS715 family of LDO regulators has been optimized for ultralow-power applications such as the MSP430 microcontroller. The ultralow-supply current of the TPS715 device maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

8.2 Typical Application

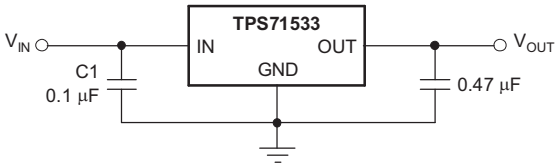
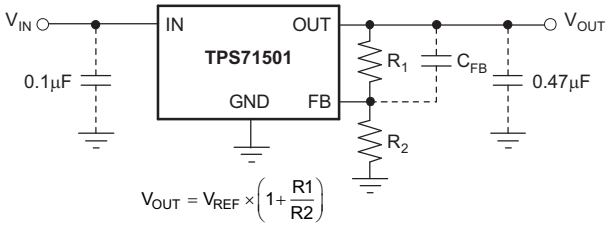


Figure 12. Typical Application Circuit (Fixed-Voltage Version)



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

Figure 13. TPS71501 Adjustable LDO Regulator Programming

8.2.1 Design Requirements

8.2.1.1 Power the MSP430 Microcontroller

Several versions of the TPS715 are ideal for powering the MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (TYP)	APPLICATION
TPS71519	1.9 V	$V_{OUT(min)}$ > 1.8 V required by many MSP430s. Allows lowest power consumption operation.
TPS71523	2.3 V	$V_{OUT(min)}$ > 2.2 V required by some MSP430s flash operation.
TPS71530	3 V	$V_{OUT(min)}$ > 2.7 V required by some MSP430s Flash operation.
TPS715345	3.45 V	$V_{OUT(max)}$ < 3.6 V required by some MSP430s. Allows highest speed operation.

The TPS715 family offers many output voltage versions to allow designers to optimize the supply voltage for the MSP430, thereby minimizing the supply current consumed by the MSP430.

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) greater than or equal to 0.47 µF properly stabilizes this loop. X7R or X5R type capacitors are recommended due to their wider temperature spec and lower temperature coefficient, but other types of capacitors may be used.

8.2.2.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$). However, in the *Electrical Characteristics*, V_{DO} is defined as the $V_{IN} – V_{OUT}$ voltage at the rated current, where the pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(on)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(on)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. $R_{DS(on)}$ can be calculated using Equation 1:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

8.2.2.3 Setting V_{OUT} for the TPS71501 Adjustable LDO

The TPS715 family contains an adjustable-version, TPS71501, which sets the output voltage using an external resistor divider as shown in Figure 13. The output voltage operating range is 1.2 V to 15 V, and is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \tag{2}$$

where

- V_{REF} = 1.205 V (typical)

Resistors R1 and R2 should be chosen to allow approximately 1.5-µA of current through the resistor divider. Lower value resistors can be used for improved noise performance, but will consume more power. Higher resistor values should be avoided as leakage current into or out of FB across R1/R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 3:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times 2 \tag{3}$$

Figure 13 shows this configuration.

8.2.3 Application Curves

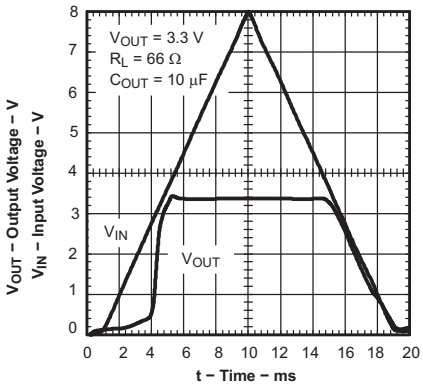


Figure 14. Power Up and Power Down

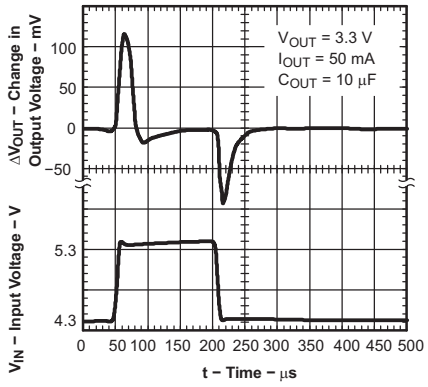


Figure 15. Line Transient Response

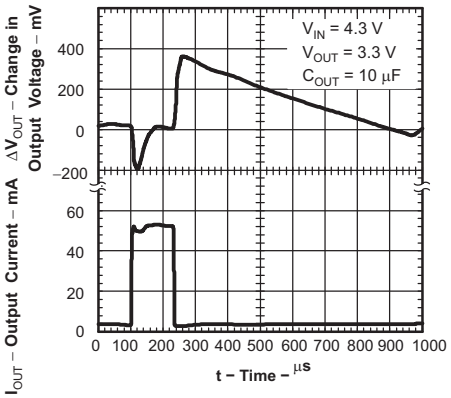


Figure 16. Load Transient Response

8.3 Do's and Don'ts

Place at least one 0.47-µF capacitor as close as possible to the OUT and GND terminals of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor as close as possible to the IN and GND terminals of the regulator for best performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The TPS715 is designed to operate from an input voltage supply range between 2.5 V and 24 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. TI strongly discourages using vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because that will negatively affect system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage and shield the LDO from noise.

10.2 Layout Example

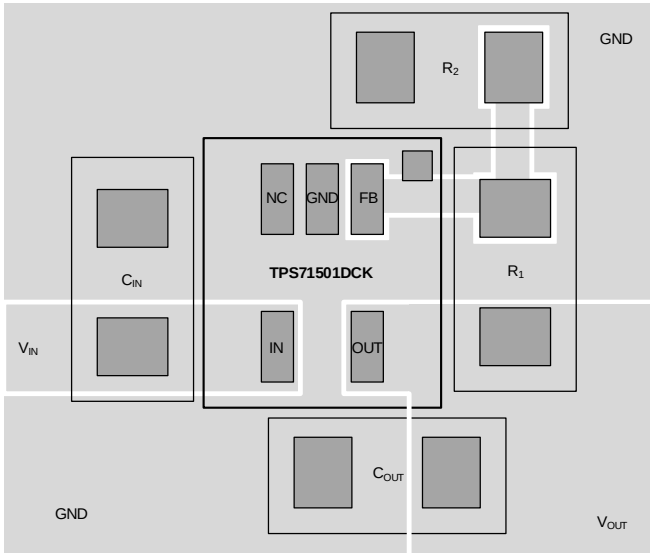


Figure 17. Example Layout for TPS71501DCK

10.3 Power Dissipation

To ensure reliable operation, worst-case junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 4:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (4)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

For a higher power package version of the TPS715, see the TPS715A.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715. The TPS71533EVM evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}(2)
TPS715**xx** ***yyy*** **z**	**XX** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 1.25 V to 5.4 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS71533EVM LDO Evaluation Module User Guide*, SLVU061
- *TPS735: High Input Voltage, Micropower SON-Packaged, 80-mA LDO Linear Regulators*, SBVS047

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00328DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AQI	Samples
HPA00423DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARB	Samples
HPA00681DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARB	Samples
TPS71501DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARB	Samples
TPS71501DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARB	Samples
TPS71518DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARD	Samples
TPS71518DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARD	Samples
TPS71519DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BOX	Samples
TPS71523DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BNX	Samples
TPS71525DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQL	Samples
TPS71525DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQL	Samples
TPS71530DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQM	Samples
TPS71530DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQM	Samples
TPS71533DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQI	Samples
TPS71533DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQI	Samples
TPS715345DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BNY	Samples
TPS71550DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	T48	Samples
TPS71550DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	T48	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS715 :

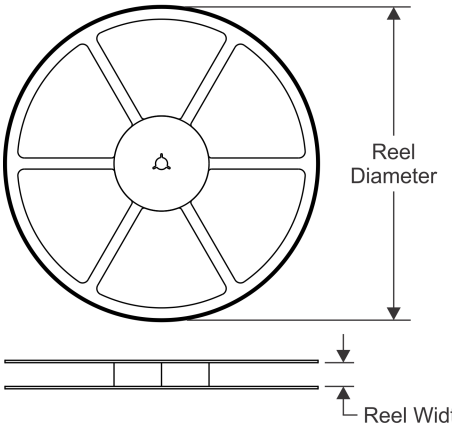
- Automotive : TPS715-Q1

NOTE: Qualified Version Definitions:

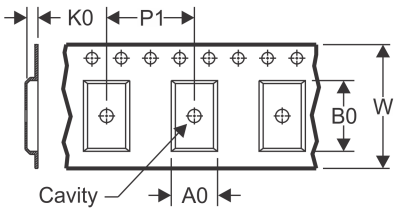
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

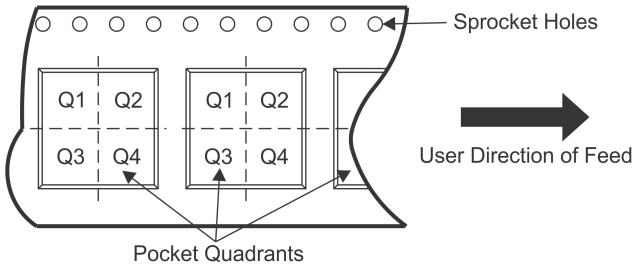


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

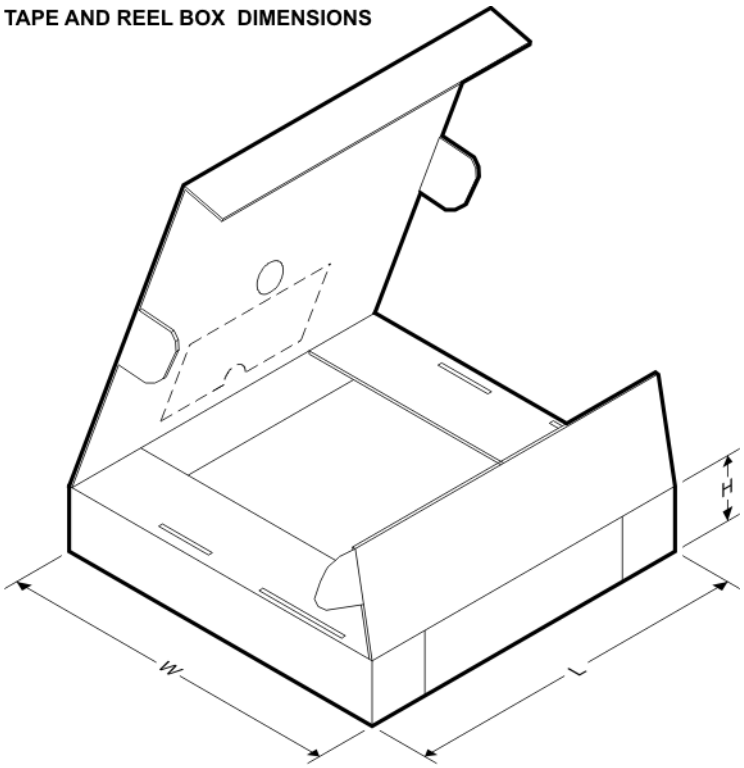
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71501DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71501DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71518DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71519DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71523DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71523DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71525DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71525DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71530DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71530DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71533DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71533DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS715345DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71550DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71550DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

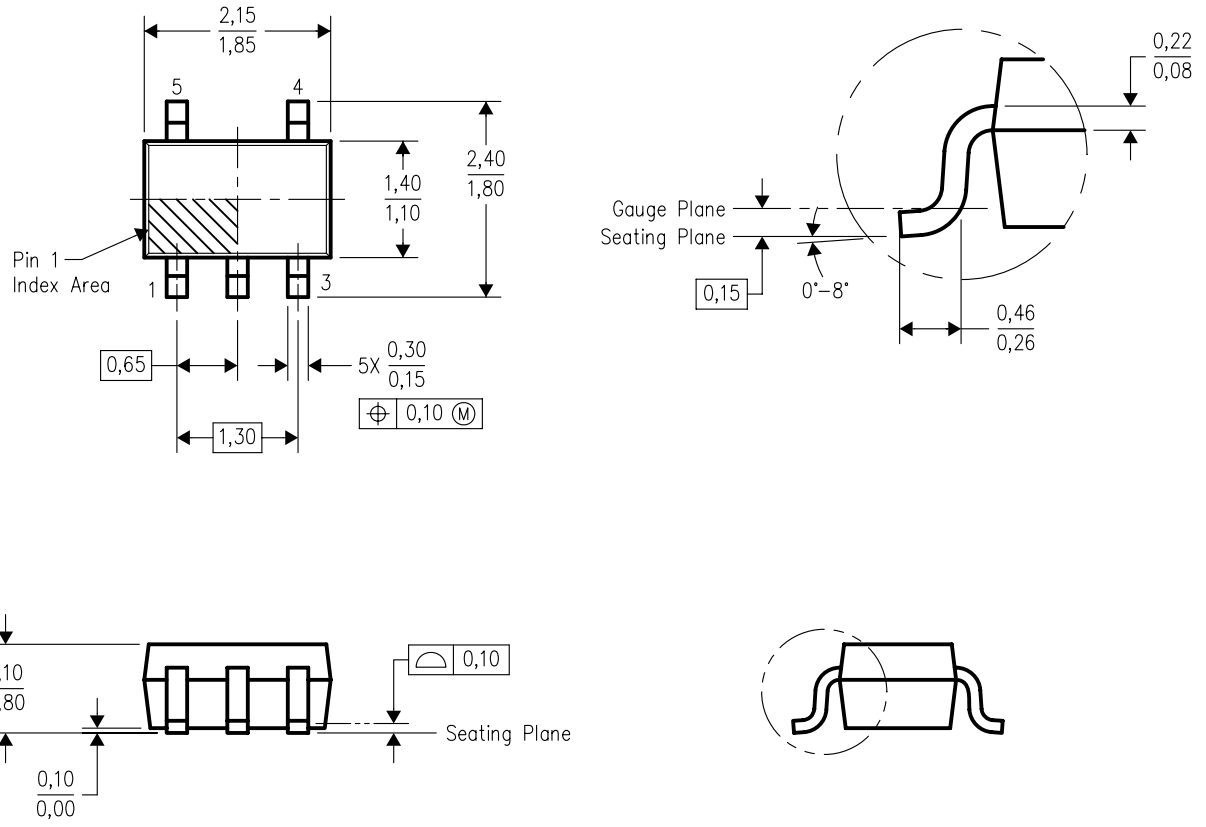
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71501DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71501DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71518DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71519DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71523DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71523DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71525DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71525DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71530DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71530DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71533DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71533DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS715345DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71550DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71550DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

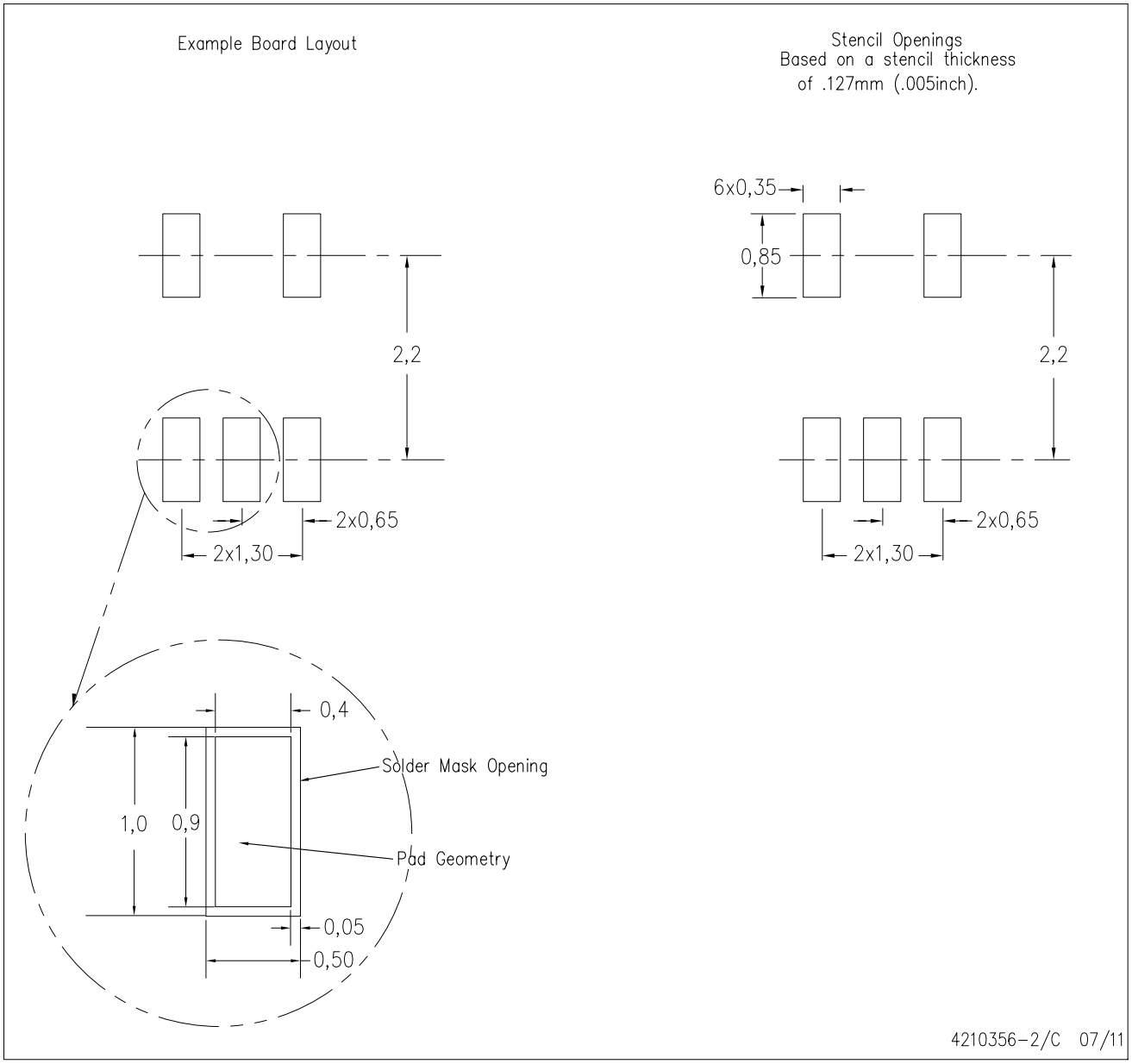
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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