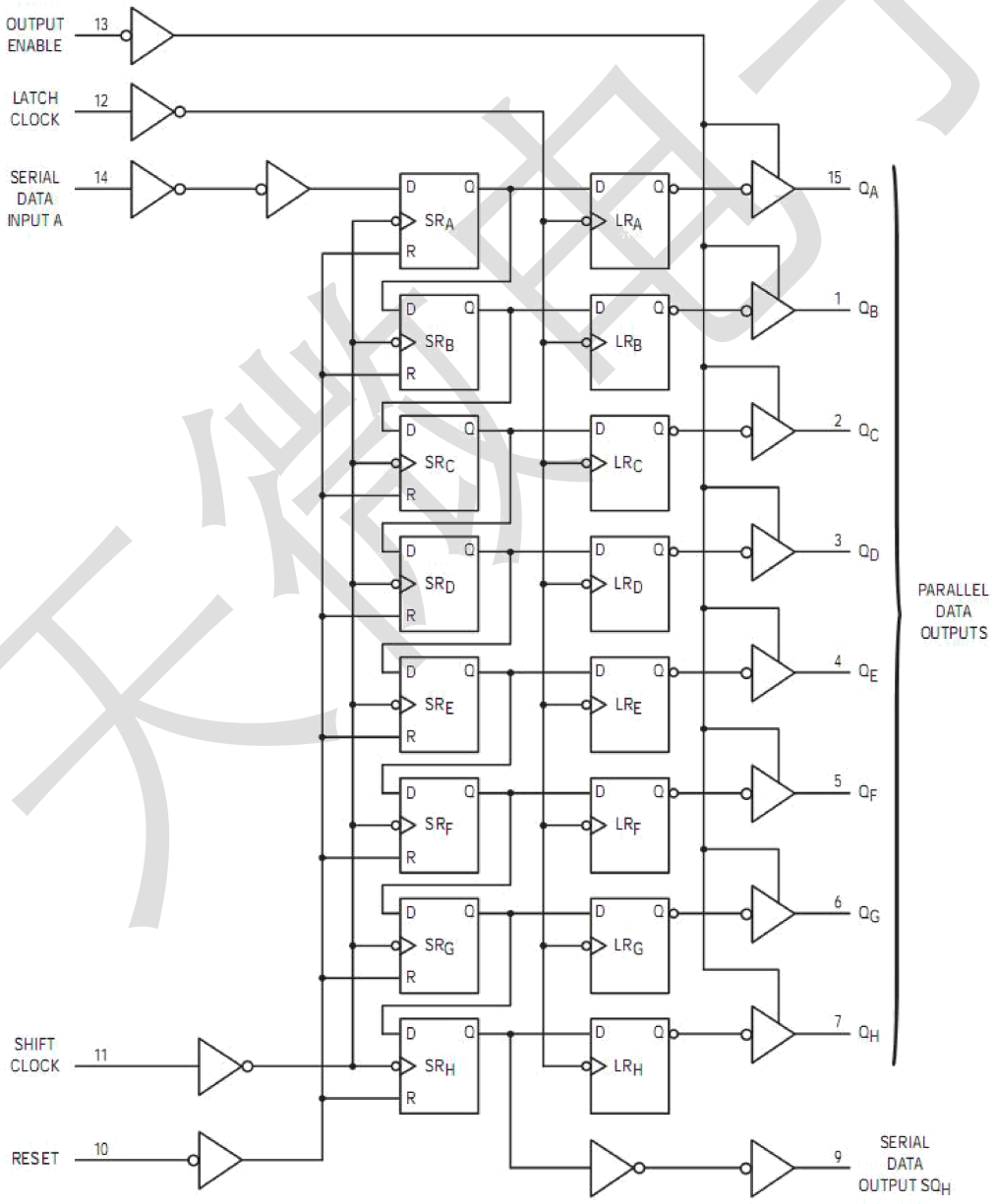
Characterization

TM74HC595 is an open-drain output CMOS shift register which is designed with controllable tri-state output terminals and, when in serial output configuration, can control cascade chip of next stage. This product is excellent in performance and reliable in quality.

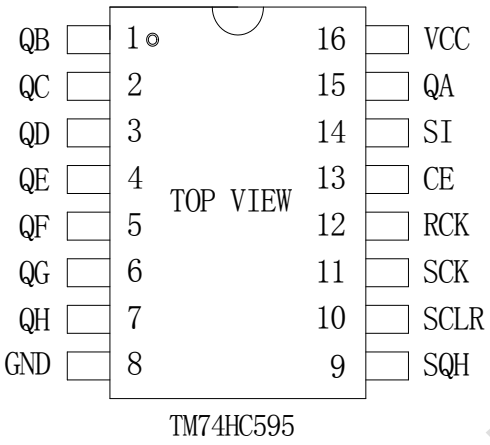
Features

- High-speed shift clock frequency Fmax> 25MHz
- Standard SPI
- CMOS serial output, capable of cascading multiple devices
- Low power consumption: Icc = 4μA (MAX) when TA = 25 ℃

Block diagram of internal structure



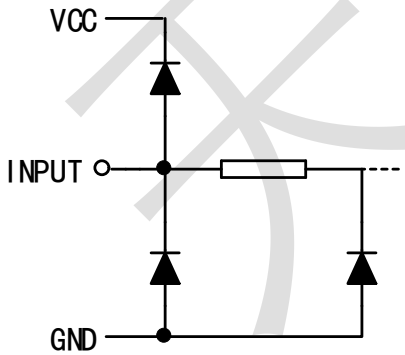
Pin arrangement



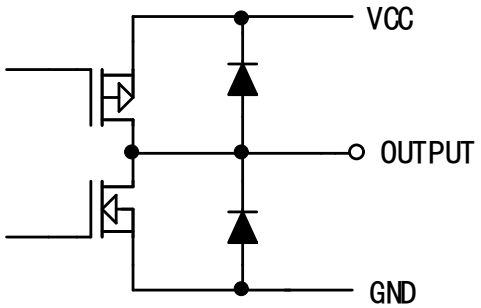
Pin Function

Pin Name	Pin No.	Function Description
QA—QH	15、1、2、3、4、5、6、7	Tri-state output pin
GND	8	Negative power
SQH	9	Serial data output pin
SCLR	10	Clear pin of shift register
SCK	11	Input pin of data shift clock
RCK	12	Input pin of Latch clock
OE	13	Output enable pin
SI	14	Input pin of serial data
VCC	16	Positive power

Input and output equivalent circuit



Input pins



Output pins

ESD protection

An integrated circuit is a static sensitive device. Since a considerable amount of static electricity is likely to be generated in a dry season or a dry environment and electrostatic discharge will damage integrated circuits, it is the advise of Titan that preventive measures should be taken for all appropriate ICs are. Improper operation and welding may cause ESD damage or performance degradation, and put the chip out of service.

Recommended Operating Conditions

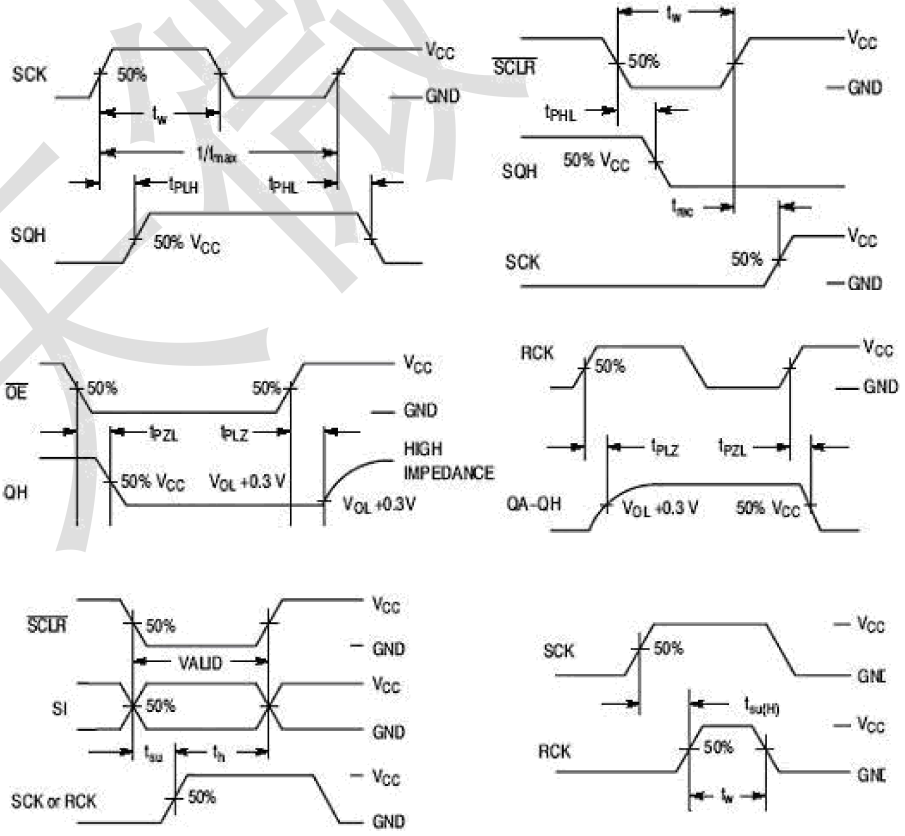
Tested at -45 ℃ ~ + 85 ℃ , unless otherwise stated		TM74HC595			Unit
Parameter Name	Parameter Symbol	Test Conditions	Minimum	Maximum	
DC VDD	V_{CC}		2.0	5.5	V
DC input voltage	V_{IN}		0	5.5	V
DC output voltage	V_{OUT}		0	V_{CC}	V
Operating temperature	T_A	V_{CC} =5V	-55	125	℃

Electrical Characteristics

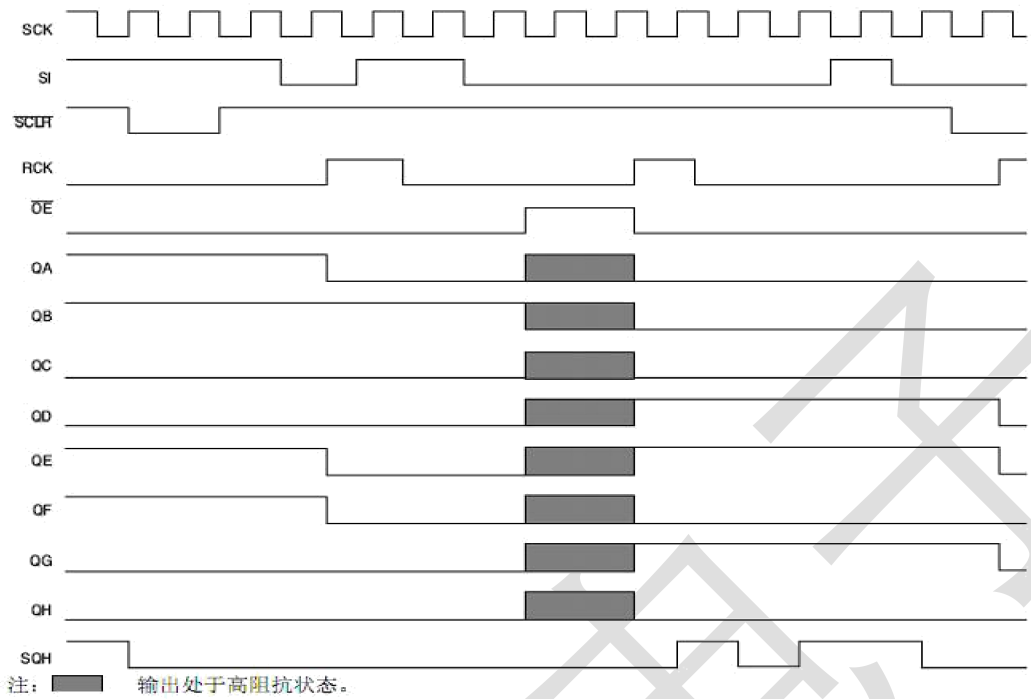
Unless otherwise stated, tested at VDD = 3.0V ~ 5.5V and the operating temperature of -40 ℃ ~ + 85 ℃		TM74HC595										Unit
Parameter Name	Parameter Symbol	Test Conditions			Value							
		VDD			25℃			-40℃—85 ℃		-55℃—125 ℃		
					Min	Typ	Max	Min	Max	Min	Max	
Input high level	V_{IH}	2.0			1.46			1.46		1.46		V
		4.5			3.23			3.23		3.23		
		6.0			4.30			4.30		4.30		
Input low level	V_{IL}	2.0					0.52		0.52		0.52	V
		4.5					1.32		1.32		1.32	
		6.0					1.77		1.77		1.77	
Output high level (SQH)	V_{OH}	2.0	$V_I=V_{IH}$ or V_{IL}	I_O=-20μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2mA	5.68	5.8		5.63		5.60		
Output high level (QA- QH)	V_{OH}	2.0	$V_I=V_{IH}$ or V_{IL}	I_O=-20μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8mA	5.68	5.8		5.63		5.60		
Output low level (SQH)	V_{OL}	2.0	$V_I=V_{IH}$ or V_{IL}	I_O=20μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O=4.0mA		0.17	0.26		0.33		0.40	
		6.0		I_O=5.2mA		0.18	0.26		0.33		0.40	
Output low level (QA- QH)	V_{OL}	2.0	$V_I=V_{IH}$ or V_{IL}	I_O=20μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O=6.0mA		0.17	0.26		0.33		0.40	
		6.0		I_O=7.8mA		0.18	0.26		0.33		0.40	
Quiescent Current	I_{CC}	6.0	$V_I=V_{CC}$ or GND				4		40		80	μA

Switching characteristics

Unless otherwise stated, tested at VDD = 3.0V ~ 5.5V and the operating temperature of -40 ℃ ~ + 85 ℃			TM74HC595			Unit
Parameter Name	Parameter Symbol	Test Conditions	T_A=25℃ Range	T_A=–40 ～ 85℃ Range	T_A=-55 ～ 125℃ Range	
SI-to-SCK ON time	t_{su}	VDD=3.3 VDD=5.0	3.5 3.0	3.5 3.0	3.5 3.0	ns
SCK-to-RCK ON time	$t_{su(H)}$	VDD=3.3 VDD=5.0	8.0 5.0	8.5 5.0	8.5 5.0	ns
SCLR-to-RCK ON time	$t_{su(L)}$	VDD=3.3 VDD=5.0	9.0 5.0	9.0 5.0	9.0 5.0	ns
SI-to-SCK OFF time	t_h	VDD=3.3 VDD=5.0	1.5 2.0	1.5 2.0	1.5 2.0	ns
SCLR-to-RCK OFF time	$t_{h(L)}$	VDD=3.3 VDD=5.0	0 0	0 0	1.0 1.0	ns
SCLR-to-SCK recovery time	t_{rec}	VDD=3.3 VDD=5.0	3.0 2.5	3.0 2.5	3.0 2.5	ns
Pulse width of SCK or RCK	t_W	VDD=3.3 VDD=5.0	5.0 5.0	5.0 5.0	5.0 5.0	ns
SCLR pulse width	$t_{W(L)}$	VDD=3.3 VDD=5.0	5.0 5.0	5.0 5.0	5.0 5.0	ns



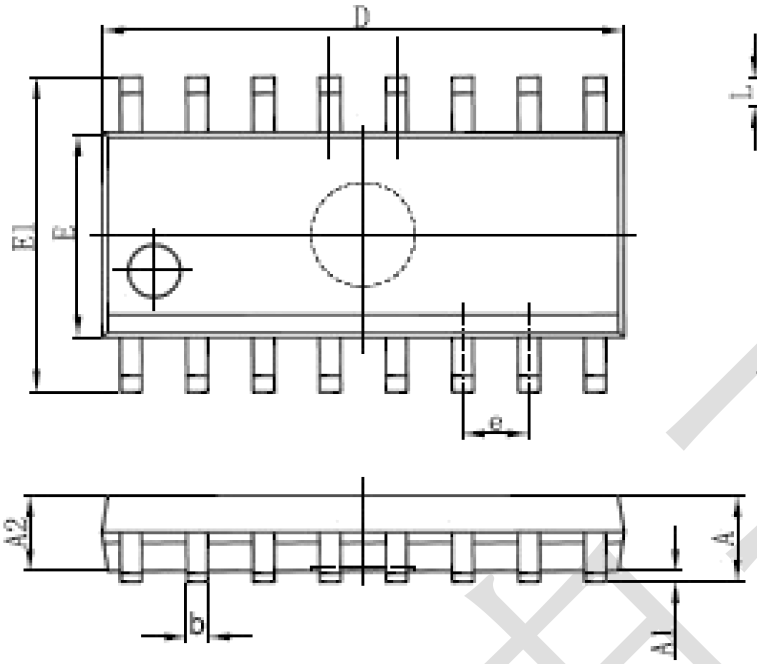
Timing Characteristics



Function Description

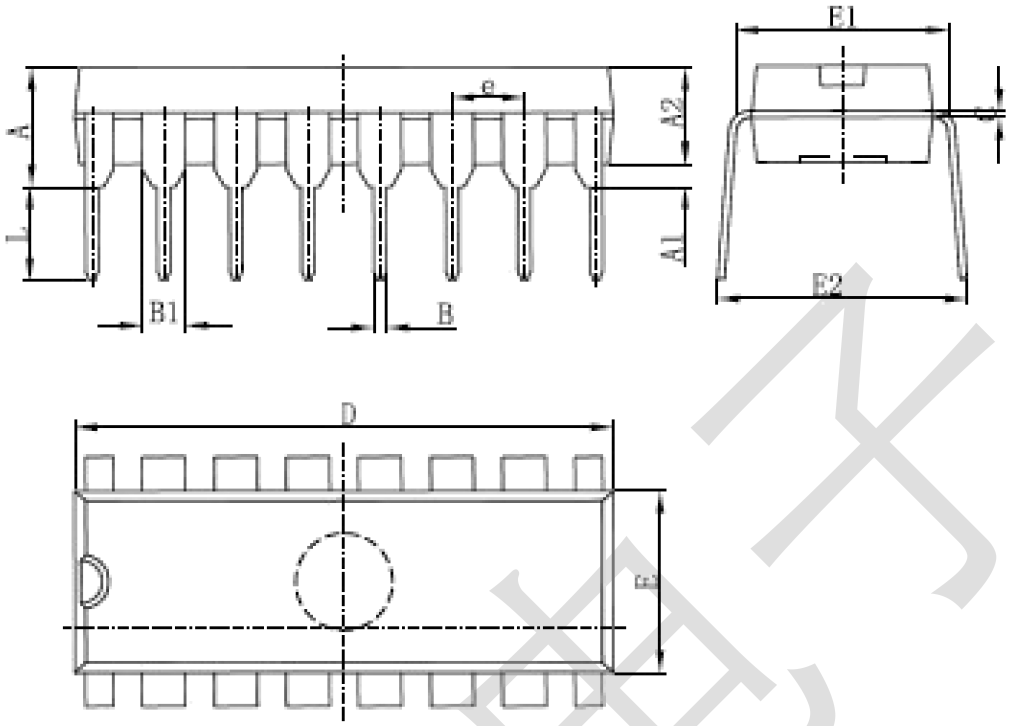
Input pin					Output pin
SI	SCK	SCLR	RCK	OE	
X	X	X	X	H	QA-QH output high impedance
X	X	X	X	L	QA-QH output RMS
X	X	L	X	X	The shift register is cleared
L	Rising edge	H	X	X	L is stored into the shift register
H	Rising edge	H	X	X	H is stored into the shift register
X	Falling edge	H	X	X	Hold the shift register state
X	X	X	Rising edge	X	Output the status value latched in the shift register
X	X	X	Falling edge	X	Hold the output status of the shift register

Schematic diagram of packaging (SOP16)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Schematic diagram of packaging (DIP16)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

All specs and applications shown above are subject to change without prior notice.

单击下面可查看定价，库存，交付和生命周期等信息

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