XD9267/XD9268 Series

36V Operation 600mA Synchronous Step-Down DC/DC Converters

ETR05075-001

☆AEC-Q100 Grade2

■GENERAL DESCRIPTION

The XC9268 series are 36V operation synchronous step-down DC/DC converter ICs with a built-in P-channel MOS driver transistor and N-channel MOS switching transistor. The XD9267 / XD9268 series has an operating voltage range of 3 V to 36 V, a switching frequency of 2.2 MHz, and the circuit scheme of synchronous rectification to be a highly efficient and stable power supply. An internal reference voltage source of 0.75 V is available, and the output voltage can be set to 1 V to 25 V by external resistors (R_{FB1} and R_{FB2}).

The soft-start time is internally set to 2.0ms (TYP.), but can be adjusted to set a longer time using an external resistor and capacitor.
With the built-in UVLO function, the driver transistor is forced OFF when input voltage becomes 2.7V or lower.
The output state can be monitored using the power good function.
Over-current protection and thermal shutdown are built in as protection function, and it can be used safely even in the case of short circuit. Internal protection circuits include over current protection and thermal shutdown circuits to enable safe use.

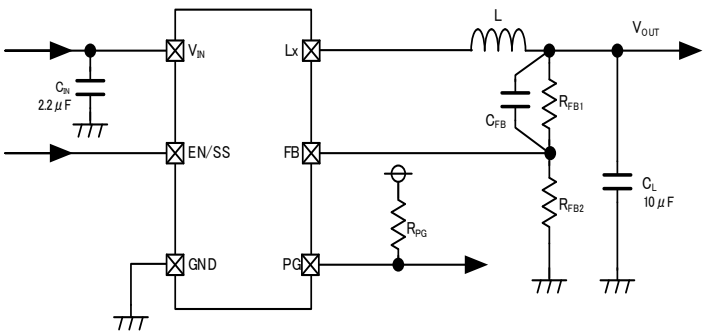
■APPLICATIONS

- ●Automotive Body Control
- ●Automotive Infotainment
- ●Automotive accessories
  - ・Drive recorder
  - ・Car-mounted camera
  - ・ETC
- ●Industrial Equipment

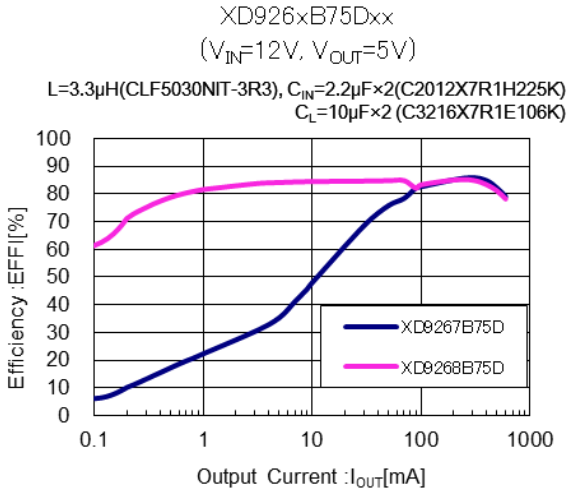
■FEATURES

Input Voltage Range	:	3.0 ~ 36V (Absolute Max 40V)
Output Voltage Range	:	1.0 ~ 25V
FB Voltage	:	0.75V ± 1.5%
Oscillation Frequency	:	2.2MHz
Output Current	:	600mA
Quiescent Current	:	13.5μA (XD9268)
Control Methods	:	PWM control(XD9267)
	:	PWM/PFM Auto(XD9268)
	:	Efficiency 88%@12V→5V,300mA
Soft-start Time	:	Adjustable by RC
Protection functions	:	Over Current Protection (Automatic Recovery) Thermal Shutdown
Output Capacitor	:	Ceramic Capacitor
Operating Ambient Temperature	:	- 40℃ ~ + 105℃
Packages	:	SOT-89-5 (Without Power Good)
	:	USP-6C (With Power Good)
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

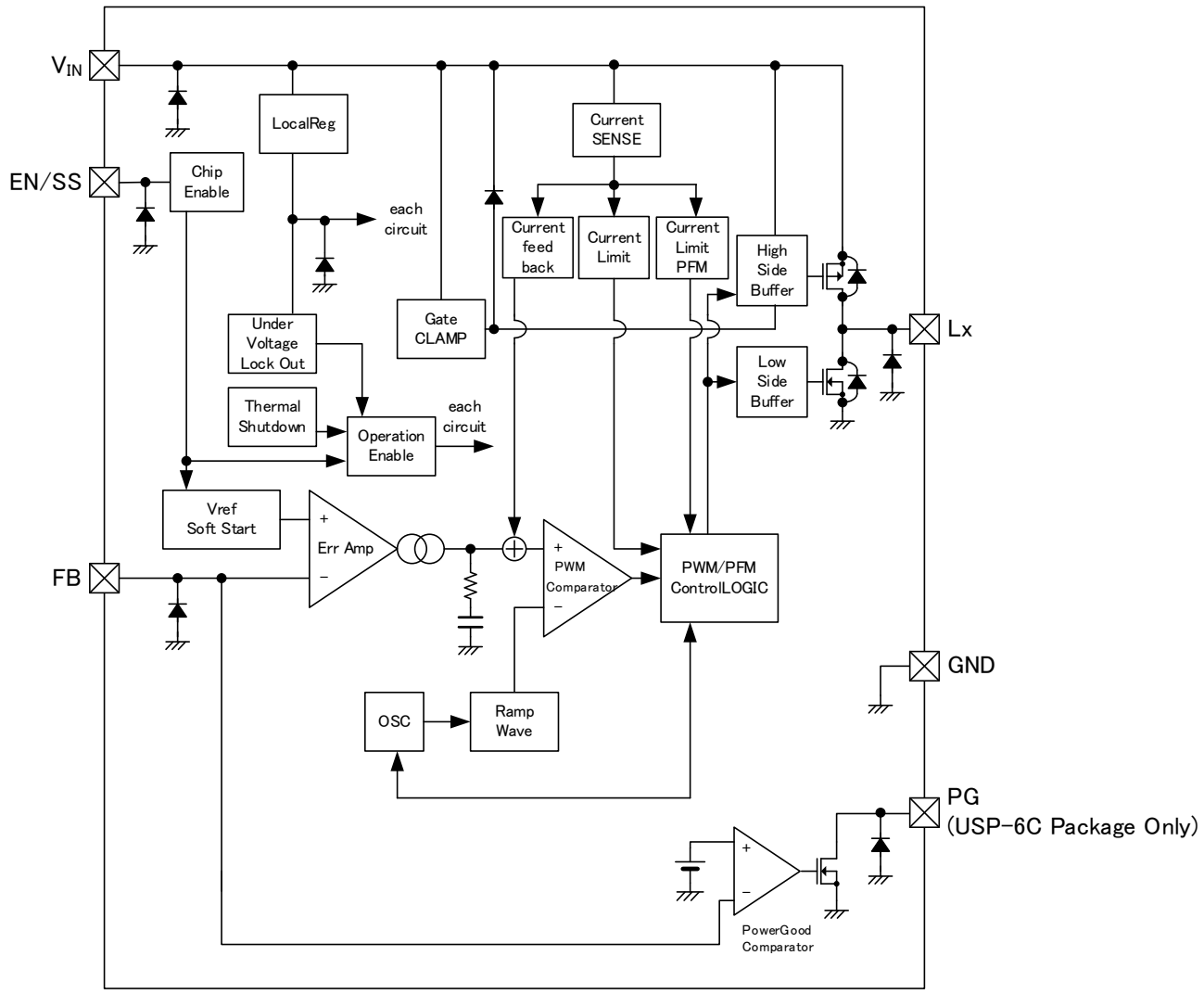


■TYPICAL PERFORMANCE CHARACTERISTICS



■BLOCK DIAGRAM

XD9267/XD9268 Series



*Diodes inside the circuit are an ESD protection diodes and a parasitic diodes.

■PRODUCT CLASSIFICATION

● Ordering Information

XD9267①②③④⑤⑥-⑦(*1) PWM control

XD9268①②③④⑤⑥-⑦(*1) PWM/PFM Auto

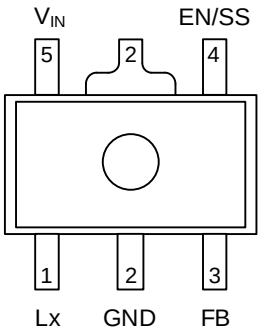
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	Refer to Selection Guide
②③	FB Voltage	75	Output voltage can be adjusted in 1V to 25V
④	Oscillation Frequency	D	2.2MHz
⑤⑥−⑦	Packages	PR-Q(*1)	SOT-89-5 (1000pcs/Reel)
		ER-Q(*1)	USP-6C (3000pcs/Reel)

(*1) The “-Q” suffix denotes “AEC-Q100” and “Halogen and Antimony free” as well as being fully EU RoHS compliant.

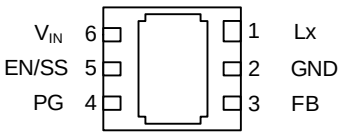
● Selection Guide

FUNCTION	B TYPE	
	SOT-89-5	USP-6C
Chip Enable	Yes	Yes
UVLO	Yes	Yes
Thermal Shutdown	Yes	Yes
Soft Start	Yes	Yes
Power-Good	-	Yes
Current Limitter (Automatic Recovery)	Yes	Yes

■PIN CONFIGURATION



SOT-89-5
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-89-5	USP-6C		
1	1	Lx	Switching Output
2	2	GND	Ground
3	3	FB	Output Voltage Sense
-	4	PG	Power-good Output
4	5	EN/SS	Enable Soft-start
5	6	V_{IN}	Power Input

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	L	Stand-by
	H	Active
	OPEN	Undefined State(*1)

(*1) Please do not leave the EN/SS pin open. Each should have a certain voltage

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ($VIN < V_{UVLO1}$)	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	-0.3 ~ +40	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ~ +40	V
FB Pin Voltage		V_{FB}	-0.3 ~ +6.2	V
PG Pin Voltage(*1)		V_{PG}	-0.3 ~ +6.2	V
PG Pin Current(*1)		I_{PG}	8	mA
Lx Pin Voltage		V_{Lx}	-0.3 ~ V_{IN} + 0.3 or +40 (*2)	V
Lx Pin Current		I_{Lx}	1800	mA
Power Dissipation	SOT-89-5	Pd	1750 (JESD51-7 board) (*4)	mW
	USP-6C		1250 (JESD51-7 board) (*4)	
Surge Voltage		V_{SURGE}	+46(*3)	V
Operating Ambient Temperature		Topr	-40 ~ +105	℃
Storage Temperature		Tstg	-55 ~ +125	℃

* All voltages are described based on the GND pin.

(*1) For the USP-6C Package only.

(*2) The maximum value should be either V_{IN}+0.3 or 40 in the lowest.

(*3) Applied Time≦400ms

(*4) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

■ELECTRICAL CHARACTERISTICS

XD9267/XD9268 Series

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB Voltage	V_{FBE}	V_{FB}=0.731V→0.769V, V_{FB} Voltage when Lx pin voltage changes from"H" level to "L" level		0.739	0.750	0.761	V	②
			-40℃≦Ta≦105℃	0.731	-	0.769		
Setting Output Voltage Range (*1)	V_{OUTSET}	-		1	-	25	V	-
Operating Input Voltage Range (*1)	V_{IN}	-		3	-	36	V	-
UVLO Detect Voltage	V_{UVLOD}	$V_{EN/SS}$=12V,V_{IN}:2.87V→2.53V,V_{FB}=0V V_{IN} Voltage which Lx pin voltage holding "H" level		2.6	2.7	2.8	V	②
			-40℃≦Ta≦105℃	2.53	-	2.87		
UVLO Release Voltage	V_{UVLOR}	$V_{EN/SS}$=12V,V_{IN}:2.63V→2.97V,V_{FB}=0V V_{IN} Voltage which Lx pin voltage holding "L" level		2.7	2.8	2.9	V	②
			-40℃≦Ta≦105℃	2.63	-	2.97		
Quiescent Current	I_q	V_{FB}=0.825V	XD9267	-	290	500	μA	④
			-40℃≦Ta≦105℃	-	-	550		
			XD9268	-	13.5	22.0		
			-40℃≦Ta≦105℃	-	-	30		
Stand-by Current	I_{STBY}	V_{IN}=12V, $V_{EN/SS}$=V_{FB}=0V		-	1.65	2.50	μA	④
			-40℃≦Ta≦105℃	-	-	3.90		
Oscillation Frequency	f_{OSC}	Connected to external components, I_{OUT}=200mA		2.013	2.200	2.387	MHz	①
			-40℃≦Ta≦105℃	1.936	-	2.464		
Minimum On Time	t_{ONMIN}	Connected to external components		-	85 (*2)	-	ns	①
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.825V	-40℃≦Ta≦105℃	-	-	0	%	②
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V	-40℃≦Ta≦105℃	100	-	-	%	②
Lx SW "H" On Resistance	R_{LxH}	V_{FB}=0.675V, I_{Lx}=200mA		-	1.20	1.38	Ω	⑤
Lx SW "L" On Resistance	R_{LxL}	-		-	0.60 (*2)	-	Ω	⑤
High side Current Limit (*3)	I_{LIMH}	V_{FB}=V_{FBE}×0.98		1.00	1.30	-	A	⑤
Internal Soft-Start Time	t_{SS1}	V_{FB}=0.675V		1.0	2.0	4.0	ms	②
External Soft-Start Time	t_{SS2}	V_{FB}=0.675V R_{SS}=430KΩ, C_{SS}=0.47μF		21	26	33	ms	③

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V, V_{PG}=OPEN(*4)

Peripheral parts connection conditions：L=3.3μH,R_{FB1}=680kΩ,R_{FB2}=120kΩ,C_{FB}=12pF,C_L=10μF×2,C_{IN}=2.2μF

(*1) Please use within the range of V_{OUT}/V_{IN}≧t_{ONMIN}[ns]×f_{OSC}[MHz]×10^{-3}

(*2)Design reference value. This parameter is provided only for reference.

(*3)Current limit denotes the level of detection at peak of coil current.

■ELECTRICAL CHARACTERISTICS

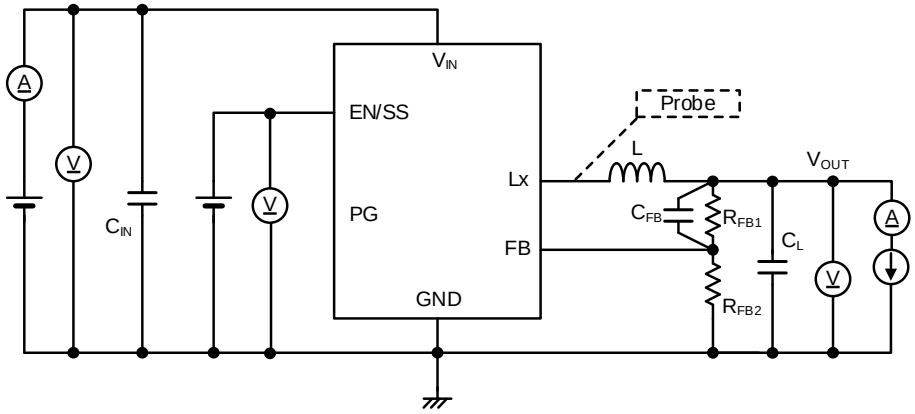
XD9267/XD9268 Series Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
PG detect voltage (*4)	V_{PGDET}	V_{FB}=0.72V→0.63V, R_{PG}:100kΩ pull-up to 5V V_{FB} Voltage when PG pin voltage changes from"H" level to "L" level		0.638	0.675	0.712	V	⑤
			-40℃≦Ta≦105℃	0.630	-	0.720		
PG Output voltage (*4)	V_{PG}	V_{FB}=0.6V, I_{PG}=1mA	-40℃≦Ta≦105℃	-	-	0.3	V	②
PFM Switch Current	IPFM	Connected to external components, V_{IN}=$V_{EN/SS}$=12V、I_{OUT}=1mA		-	400	-	mA	①
Efficiency (*5)	EFFI	Connected to external components, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=300mA		-	88	-	%	①
FB Voltage Temperature Characteristics	ΔV_{FB}/(ΔT_{opr}・V_{FBE})	-40℃≦T_{opr}≦105℃		-	±100	-	ppm/℃	②
FB "H" Current	I_{FBH}	V_{IN}=$V_{EN/SS}$=36V, V_{FB}=3.0V	-40℃≦Ta≦105℃	-0.1	-	0.1	μA	③
FB "L" Current	I_{FBL}	V_{IN}=$V_{EN/SS}$=36V, V_{FB}=0V	-40℃≦Ta≦105℃	-0.1	-	0.1	μA	④
EN/SS "H" Voltage	$V_{EN/SSH}$	$V_{EN/SS}$=0.3V→2.5V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "L" level to "H" level		2.5	-	36	V	③
			-40℃≦Ta≦105℃					
EN/SS "L" Voltage	$V_{EN/SSL}$	$V_{EN/SS}$=2.5V→0.3V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "H" level to "L" level		-	-	0.3	V	②
			-40℃≦Ta≦105℃					
EN/SS "H" Current	$I_{EN/SSH}$	V_{IN}=$V_{EN/SS}$=36V, V_{FB}=0.825V	-40℃≦Ta≦105℃	-	0.1	0.3	μA	④
EN/SS "L" Current	$I_{EN/SSL}$	V_{IN}=36V, $V_{EN/SS}$=0V, V_{FB}=0.825V	-40℃≦Ta≦105℃	-0.1	-	0.1	μA	④
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature		-	150	-	℃	−
Hysteresis Width	T_{HYS}	Junction Temperature		-	25	-	℃	−

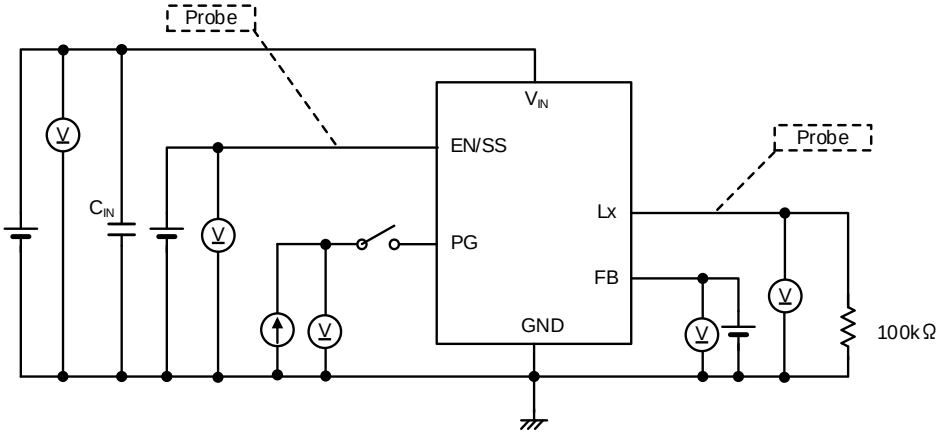
Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V, V_{PG}=OPEN(*4)
Peripheral parts connection conditions：L=3.3μH,R_{FB1}=680kΩ,R_{FB2}=120kΩ,C_{FB}=12pF,C_L=10μF×2,C_{IN}=2.2μF
(*4) For the USP-6C Package only.
(*5) EFFI = {(output voltage) x (output current)} / {(input voltage) x (input current)} x 100

■TEST CIRCUITS

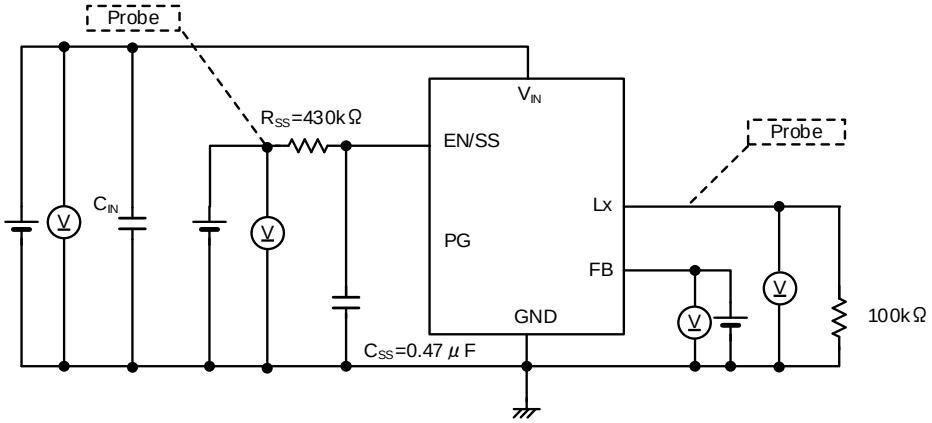
CIRCUIT①



CIRCUIT②



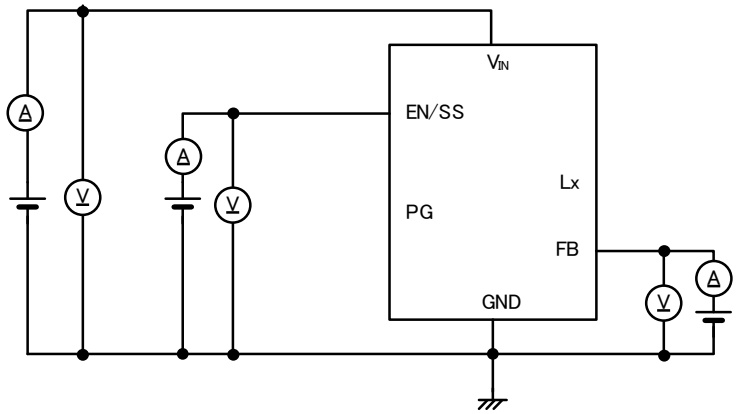
CIRCUIT③



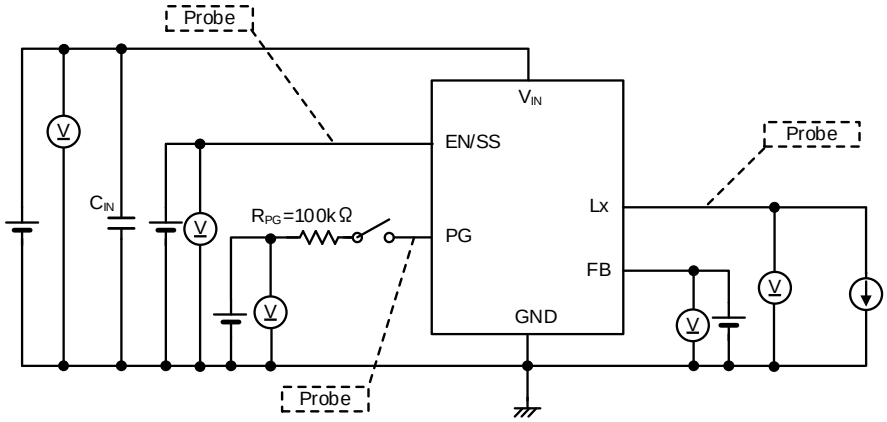
* PG Pin is USP-6C Package only.

■TEST CIRCUITS

CIRCUIT④

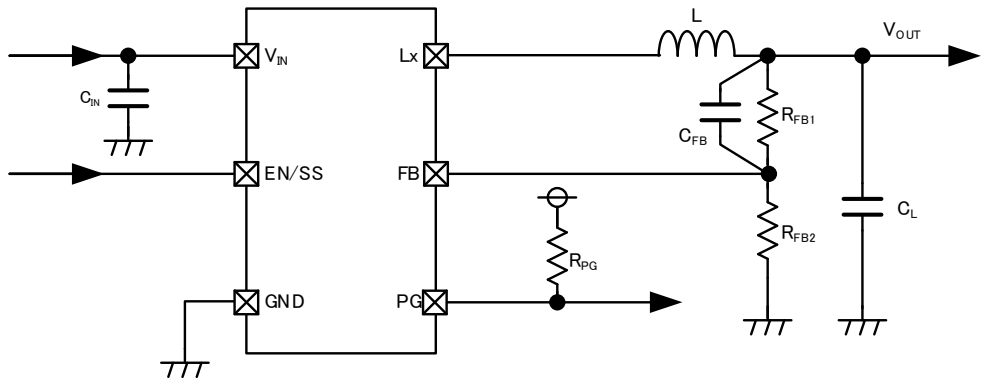


CIRCUIT⑤



* PG Pin is USP-6C Package only.

■TYPICAL APPLICATION CIRCUIT



＜Inductance value setting＞

For the XD9267/XD9268 Series, operation is optimized by setting the following inductance value according to the setting output voltage.

V_{OUTSET}: Output voltage setting

【Typical Examples】

	conditions	MANUFACTURER	PRODUCT NUMBER	VALUE
L	1V＜V_{OUTSET}≦2V	TDK	CLF5030NIT-1R5N-D	1.5μH
		Coilcraft	XEL4030-152ME	
		Taiyo Yuden	NRS4018T1R5NDGJV	
	2V＜V_{OUTSET}≦3.3V	TDK	CLF5030NIT-2R2N-D	2.2μH
		Coilcraft	XEL4030-222ME	
		Taiyo Yuden	NRS4018T2R2MDGJV	
	3.3V＜V_{OUTSET}≦6V	TDK	CLF5030NIT-3R3N-D	3.3μH
		Coilcraft	XEL4030-332ME	
		Taiyo Yuden	NRS4018T3R3MDGJV	
	6V＜V_{OUTSET}≦25V	TDK	CLF5030NIT-4R7N-D	4.7μH
		Coilcraft	XEL4030-472ME	
		Taiyo Yuden	NRS5024T4R7MMGJV	
C_{IN}	V_{IN}＜20V	TDK	CGA4J3X7R1H225K125AB	2.2μF/50V
	V_{IN}≧20V	TDK	CGA4J3X7R1H225K125AB	2.2μF/50V 2parallel
C_L	-	TDK	CGA5L1X7R1C106K160AC	10μF/16V 2parallel
			CGA5L1X7R1V106K160AC	10μF/35V 2parallel
		Murata	GCM21BR71A106KE21	10μF/10V 2parallel

■TYPICAL APPLICATION CIRCUIT(Continued)

< Output voltage setting >

The output voltage can be set by adding an external dividing resistor.
The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUT}=0.75V \times (R_{FB1}+R_{FB2})/R_{FB2}$$
With $R_{FB2} \leqq 200k\Omega$ and $R_{FB1}+R_{FB2} \leqq 1M\Omega$

<C_{FB} setting>

Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB}=\frac{1}{2\pi \times fzfb \times R_{FB1}}$$

A target value for fzfb of about $fzfb=\frac{1}{2\pi\sqrt{C_L \times L}}$ is optimum.

【Setting Example】

To set output voltage to 5V, C_L=10μF×2, L=3.3μH

When R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUTSET}=0.75V× (680kΩ+120kΩ) / 120kΩ=5.0V
And fzfb is set to a target of 19.6 kHz using the above equation,
C_{FB}=1/ (2×π×19.6 kHz×680kΩ) =11.95pF. A capacitor of E24 series is 12pF.

XD9267B75Dxx/XD9268B75Dxx					
V_{OUTSET}	R_{FB1}	R_{FB2}	L	C_{FB}	fzfb
1.2V	120kΩ	200kΩ	1.5μH	47pF	29.1kHz
3.3V	510kΩ	150kΩ	2.2μH	13pF	24.0kHz
5.0V	680kΩ	120kΩ	3.3μH	12pF	19.6kHz
12V	360kΩ	24kΩ	4.7μH	27pF	16.4kHz

<Soft-start Time Setting>

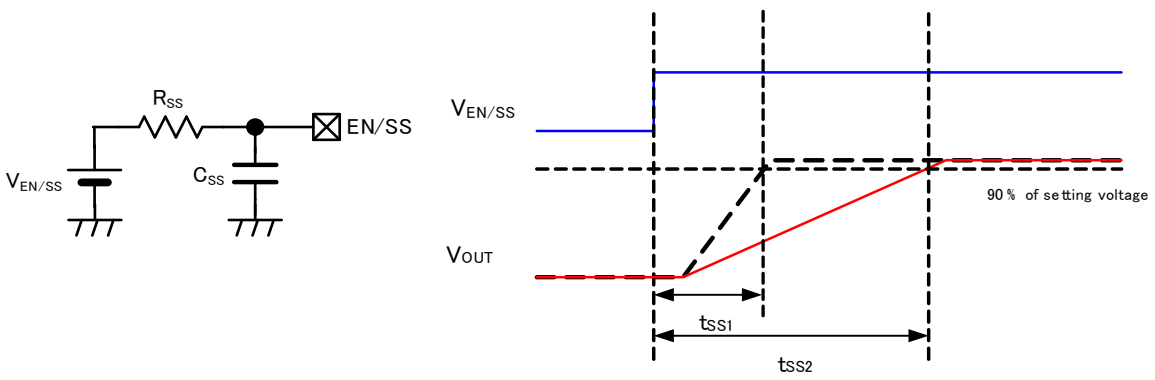
The soft-start time can be adjusted by adding a capacitor and a resistor to the EN/SS pin.
Soft-start time (t_{SS2}) is approximated by the equation below according to values of $V_{EN/SS}$, R_{SS}, and C_{SS}.

$$t_{ss2}=C_{ss} \times R_{ss} \times \ln (V_{EN/SS} / (V_{EN/SS}-1.45))$$

【Setting Example】

When C_{SS}=0.47μF, R_{SS}=430kΩ and $V_{EN/SS}$=12V, $t_{SS2}=0.47\times10^{-6} \times 430 \times 10^{3} \times (\ln (12/ (12-1.45))$ =26ms (Approx.)

*The soft-start time is the time from the start of $V_{EN/SS}$ until the output voltage reaches 90% of the set voltage.
If the EN/SS pin voltage rises steeply without connecting C_{SS} and R_{SS} (R_{SS}=0Ω), Output rises with taking the soft-start time of t_{SS1}=2.0ms (TYP.) which is fixed internally.



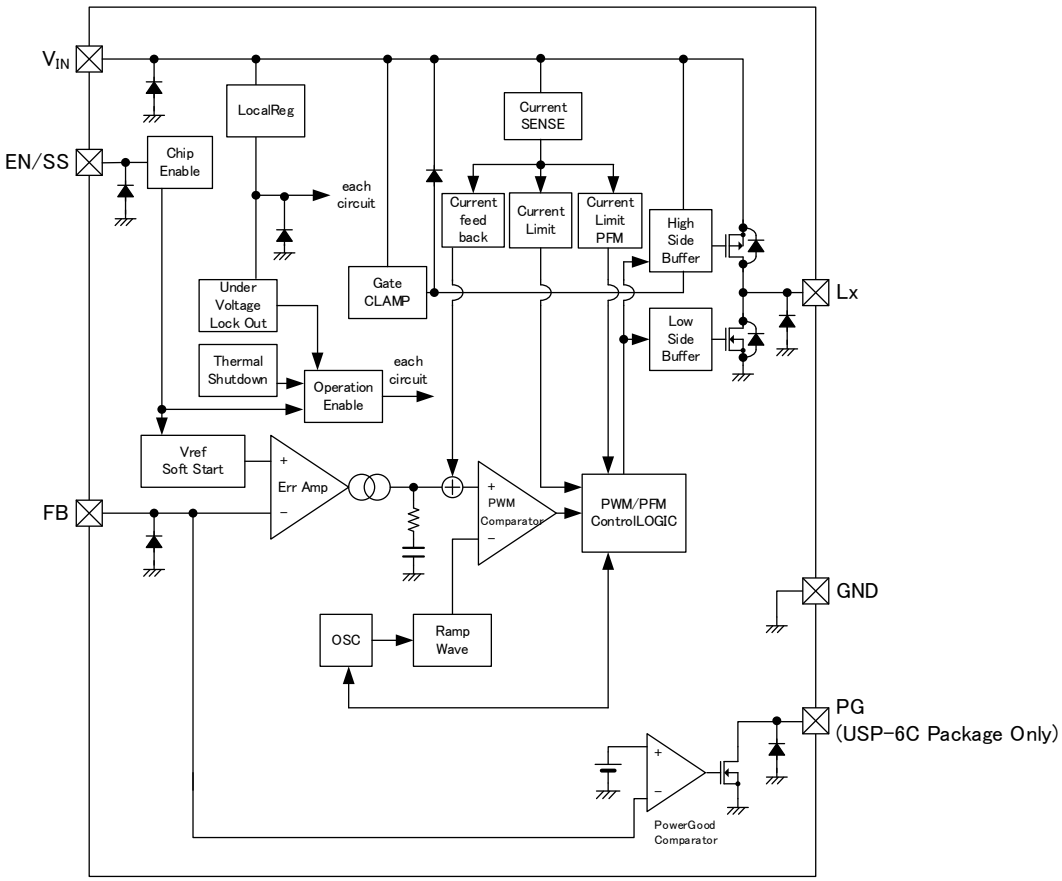
■OPERATIONAL EXPLANATION

The XD9267 / XD9268 series consists internally of a reference voltage supply with soft-start function, error amplifier, PWM comparator, ramp circuit, oscillator (OSC) circuit, phase compensation (current feedback) circuit, current limit circuit, current limiting-PFM circuit , High-side driver Tr., Low-side driver Tr., buffer drive circuit, internal power supply (Local Reg) circuit, under voltage lockout (UVLO) circuit, gate clamp (CLAMP) circuit, thermal shutdown (TSD) circuit, power good comparator, PWM/PFM control block.

The voltage feedback from the FB pin is compared to the internal reference voltage by the error amp, the output from the error amp is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation. The output signal from the error amp is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the LX pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.

The driver transistor current is monitored at each switching by the phase compensation (Current feedback) circuit, and the output signal from the error amp is modulated as a multi-feedback signal. This allows a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage

XD9267/XD9268 Series



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

<Reference voltage source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Oscillator circuit>

The switching frequency is determined by this circuit. The frequency is internally fixed at 2.2 MHz.
Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation.

<Error amplifier>

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal voltage divider, R_{FB1} and R_{FB2}. When a voltage is lower than the reference voltage, then the voltage is fed back, the output voltage of the error amplifier increases. The error amplifier output is fixed internally to deliver an optimized signal to the mixer.

■OPERATIONAL EXPLANATION(Continued)

<Current limiting>
The current limiting circuit of the XD9267/XD9268 series monitors the current that flows through the High-side driver transistor and Low-side driver transistor, and when over-current is detected, the current limiting function activates.

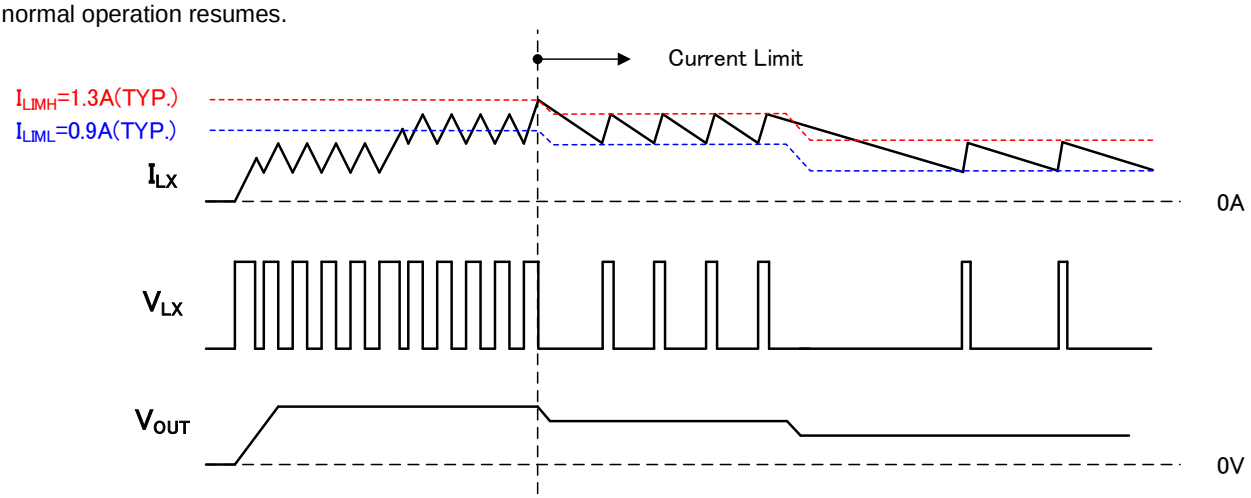
(1) High-side driver Tr. current limiting
The current in the High-side driver Tr. is detected to equivalently monitor the peak value of the coil current. The High-side driver Tr. current limiting function forcibly turns off the High-side driver Tr. when the peak value of the coil current reaches the High-side driver current limit value I_{LIMH}.

High-side driver Tr. current limit value I_{LIMH}=1.3A (TYP.)

(2) Low-side driver Tr. current limiting
The current in the Low-side driver Tr. is detected to equivalently monitor the bottom value of the coil current. The Low-side driver Tr. current limiting function operates when the High-side driver Tr. current limiting value reaches I_{LIMH}. The Low-side driver Tr. current limiting function prohibits the High-side driver Tr. from turning on in an over-current state where the bottom value of the coil current is higher than the Low-side driver Tr. current limit value I_{LIML}.

Low side driver Tr. current limit value I_{LIML}=0.9A (TYP.)

The current foldback circuit operates control to lower the switching frequency f_{OSC}. When the over-current state is released, normal operation resumes.



■OPERATIONAL EXPLANATION(Continued)

<Soft-start function>

The output voltage of XD9267/XD9268 rises with soft start by slowly raising the reference voltage. The rise time of this reference voltage is the soft start time. The soft-start time is set to t_{ss1} (TYP. 2.0ms) which is fixed internally or to the time set by adding a capacitor and a resistor to the EN / SS pin whichever is later.

<Thermal shutdown>

The thermal shutdown (TSD) as an over temperature limit is built in the XD9267/XD9268 series.
When the junction temperature reaches the detection temperature, the driver transistor is forcibly turned off. When the junction temperature falls to the release temperature while in the output stop state, restart takes place by soft-start.

<UVLO>

When the V_{IN} pin voltage falls below V_{UVLO1} (TYP. 2.7V), the driver transistor is forcibly turned off to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above V_{UVLO2} (TYP. 2.8V), the UVLO function is released, the soft-start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

<Power good>

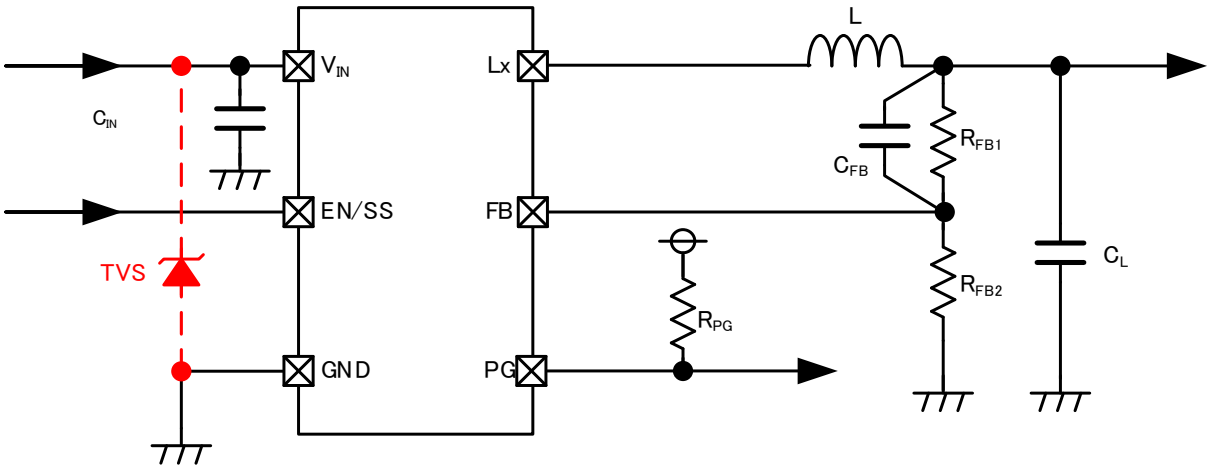
On USP-6C Package, the output state can be monitored using the power good function. The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin.

CONDITIONS		SIGNAL
EN/SS=H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ($V_{IN} < V_{UVLO1}$)	Undefined State
EN/SS=L	Stand-by	L (Low impedance)

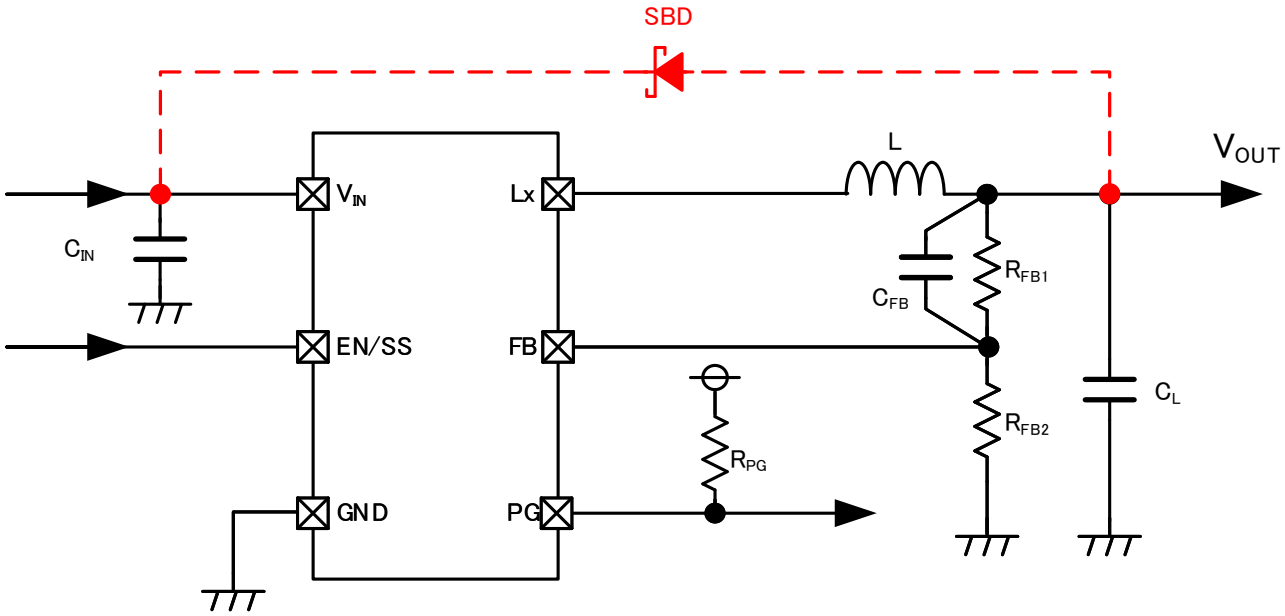
■NOTE ON USE

1) In the case of a temporary and transient voltage drop or voltage rise.
If the absolute maximum ratings are exceeded, the IC may be deteriorate or destroyed.

Case 1
If a voltage exceeding the absolute maximum voltage is applied to the IC due to chattering caused by a mechanical switch or an external surge voltage, please use a protection element such as TVS and a protection circuit as a countermeasure.



Case 2
Under conditions where the input voltage drops below the output voltage, overcurrent may flow to the parasitic diode inside the IC, and the absolute maximum rating of the Lx pin may be exceeded. If current is drawn to the input side with low impedance between Vin and GND, please take measures such as adding an SBD between V_{OUT} and V_{IN}.



2) Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.

3) The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select.
Be especially careful of the capacitor characteristics and use X7R or X5R (EIA standard) ceramic capacitors.
The capacitance decrease caused by the bias voltage may become remarkable depending on the external size of the capacitor.

■NOTE ON USE(Continued)

4) The DC/DC converter of this IC uses a current-limiting circuit to monitor the coil peak current. If the potential dropout voltage is large or the load current is large, the peak current will increase, which makes it easier for current limitation to be applied which in turn could cause the operation to become unstable. When the peak current becomes large, adjust the coil inductance and sufficiently check the operation.

The following formula is used to show the peak current.
Peak Current: $Ipk = (V_{IN} – V_{OUT}) \times V_{OUT} / V_{IN} / (2 \times L \times f_{OSC}) + I_{OUT}$

L: Coil Inductance [H]
f_{OSC}: Oscillation Frequency [Hz]
I_{OUT}: Load Current [A]

5) If there is a large dropout voltage, a circuit delay could create the ramp-up of coil current with staircase waveform exceeding the current limit.

6) Even in the PWM control, the intermittent operation occurs and the ripple voltage becomes higher, when the minimum On Time is faster than 85ns (TYP.) as well as the dropout voltage is large.

7) The ripple voltage could be increased when switching from discontinuous conduction mode to continuous conduction mode and at switching to 100% Duty cycle. Please evaluate IC well on customer's PCB.

8) XD9268(PWM/PFM auto) series may cause superimposed ripple voltage by continuous pulses if it uses in high temperature and no load. It is necessary to set an idle current of higher than 100 μA from VOUT if it uses at no load.
It can make an effect as same as RFB2 is lower than 7.5 kΩ, Please refer to the < Output voltage setting > in the TYPCAL APPLICATION CIRCUIT.

9) If the voltage at the EN/SS Pin does not start from 0V but it is at the midpoint potential when the power is switched on, the soft start function may not work properly and it may cause the larger inrush current and bigger ripple voltages.

10) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

11) Instructions of pattern layouts
The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

(1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} and GND pins.

(2) Please mount each external component as close to the IC as possible.

(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.

(4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

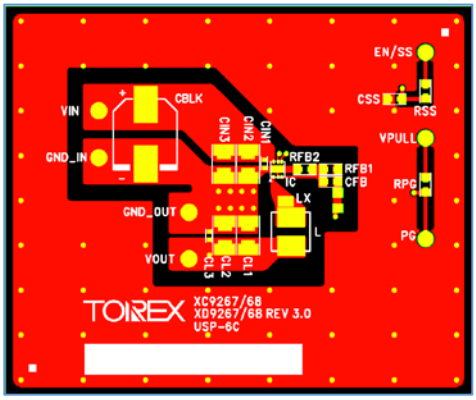
(5) Please note that internal driver transistors bring on heat because of the load current and ON resistance of High side driver transistor, Low side driver transistor. Please make sure that the heat is dissipated properly, especially at higher temperatures.

■NOTE ON USE(Continued)

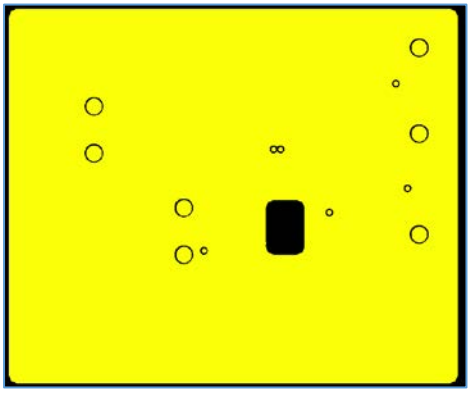
<Reference Pattern Layout>

USP-6C

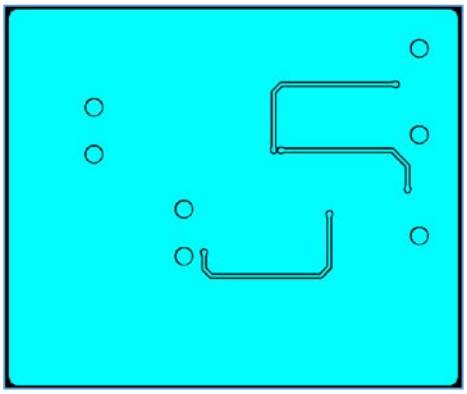
Layer 1



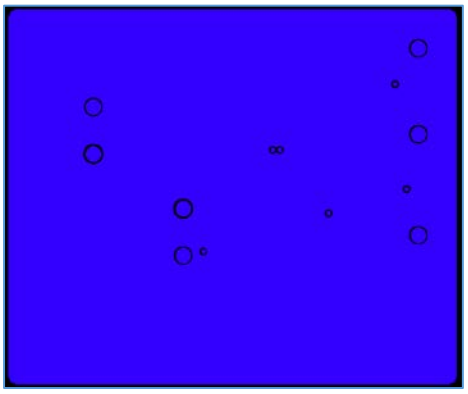
Layer 2



Layer 3

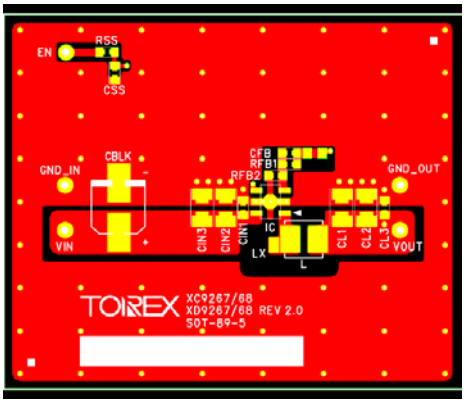


Layer 4



SOT-89-5

Layer 1



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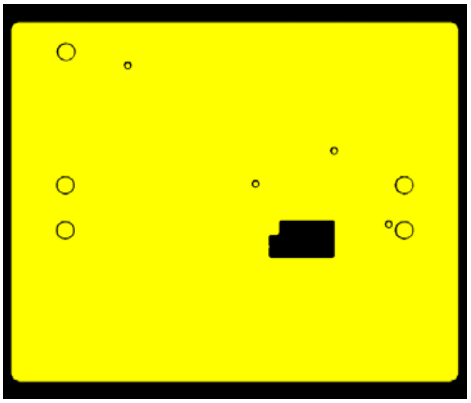
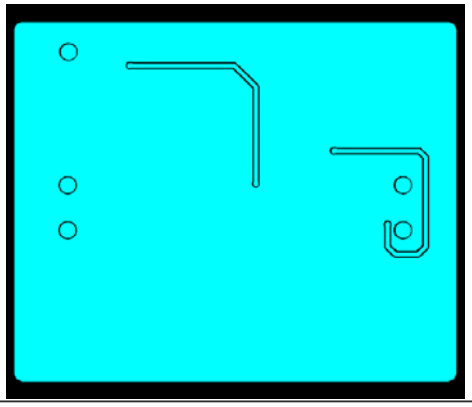
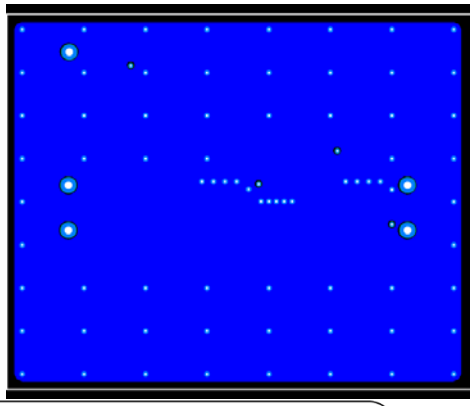


Layer 3

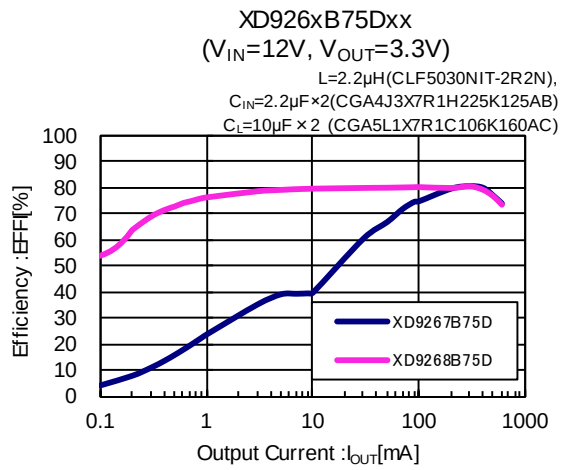


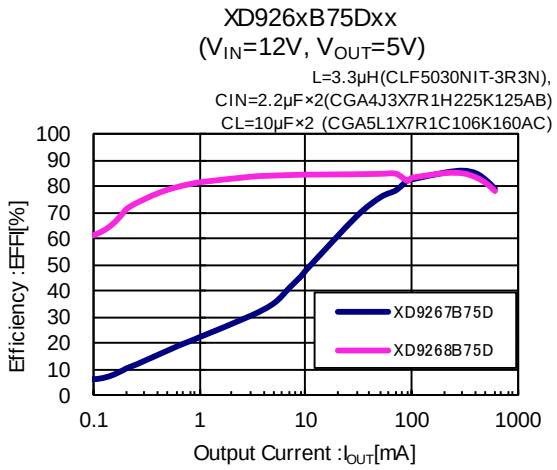
Layer 4



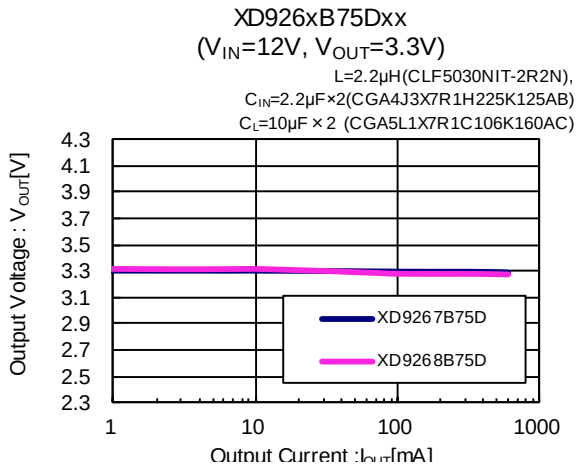
■TYPICAL PERFORMANCE CHARACTERISTICS

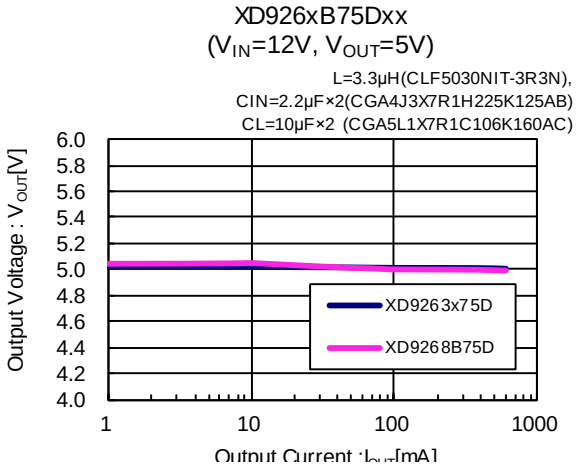
(1) Efficiency vs. Output current



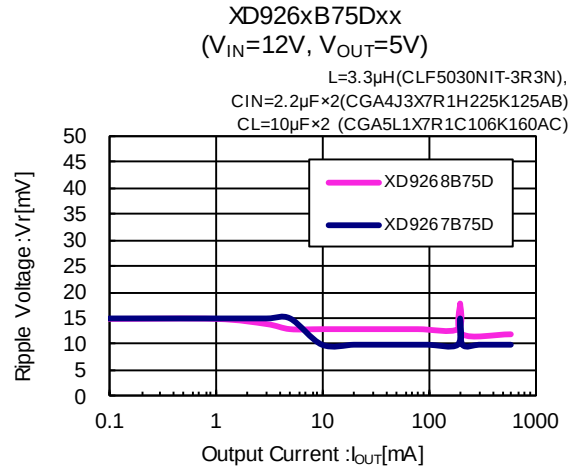


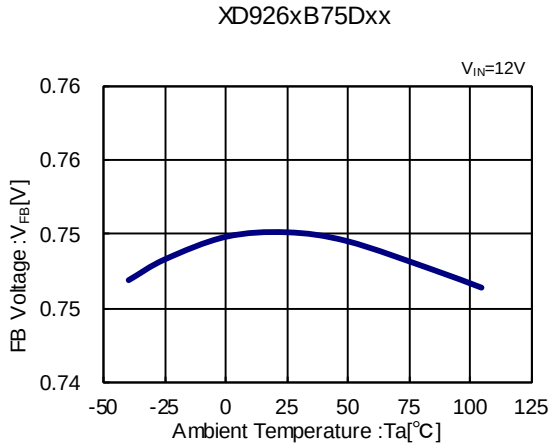
(2) Output Voltage vs. Output Current





(3) Ripple Voltage vs. Output Current

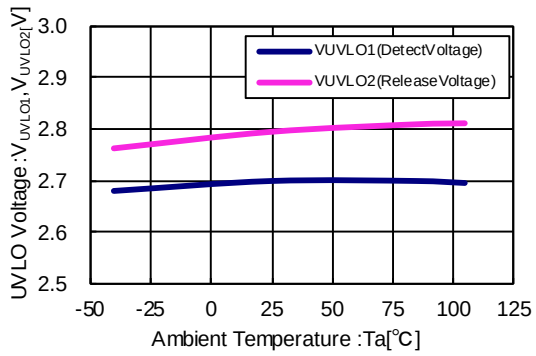




■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

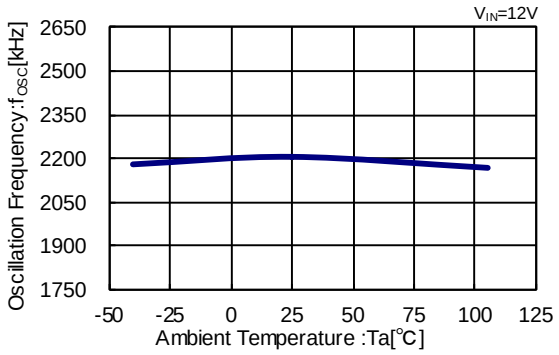
(5) UVLO Voltage vs. Ambient Temperature

XD926xB75xxx



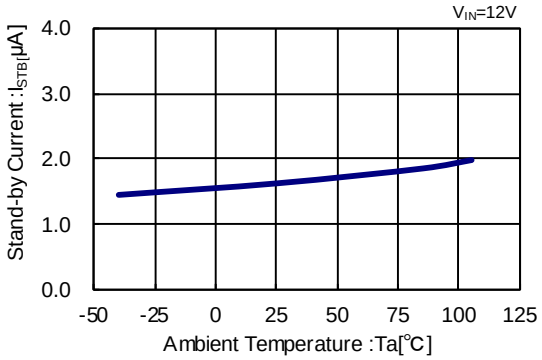
(6) Oscillation Frequency vs. Ambient Temperature

XD926xB75Dxx



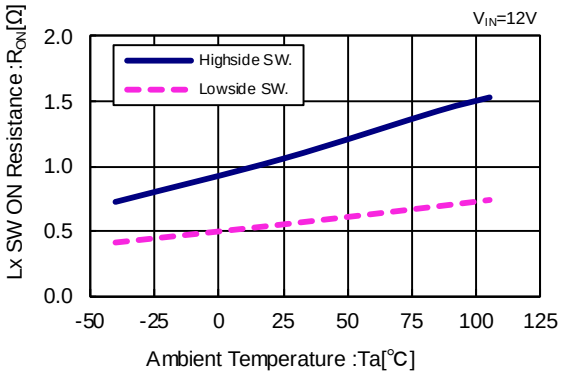
(7) Stand-by Current vs. Ambient Temperature

XD926xB75Dxx



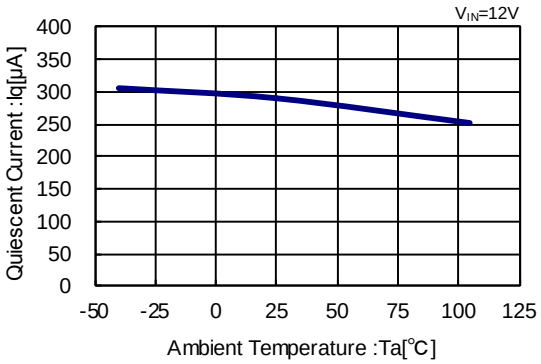
(8) Lx SW ON Resistance vs. Ambient Temperature

XD926xB75Dxx

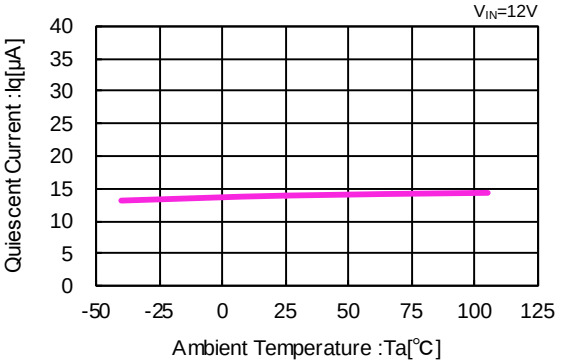


(9) Quiescent Current vs. Ambient Temperature

XD9267B75Dxx



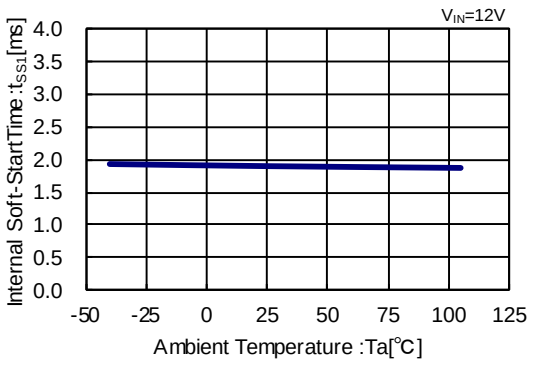
XD9268B75Dxx



■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

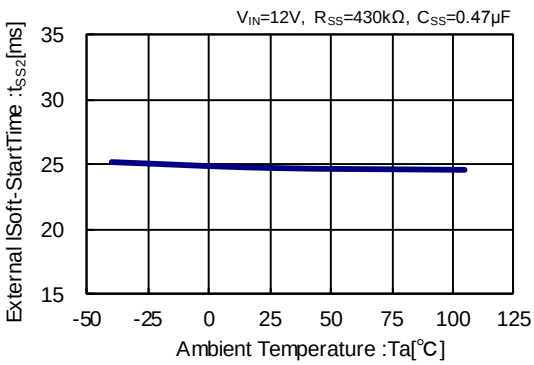
(10) Internal Soft-Start Time vs. Ambient Temperature

XD926xB75Dxx



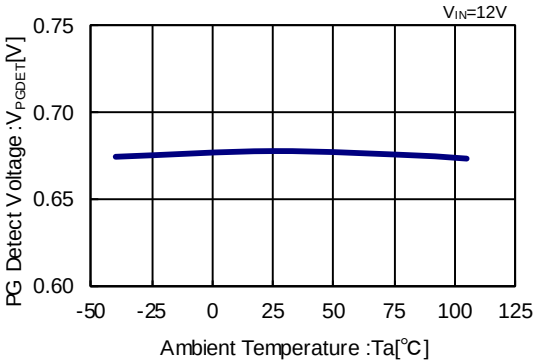
(11) External Soft-Start Time vs. Ambient Temperature

XD926xB75Dxx



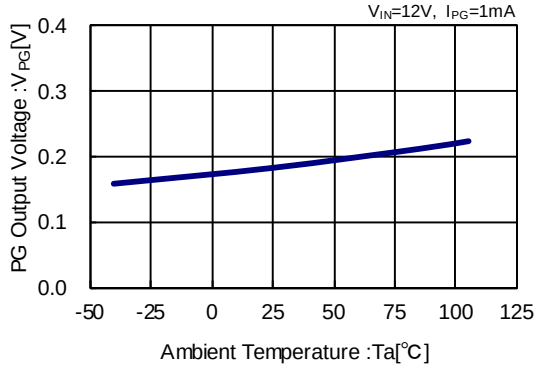
(12) PG Detect Voltage vs. Ambient Temperature

XD926xB75Dxx



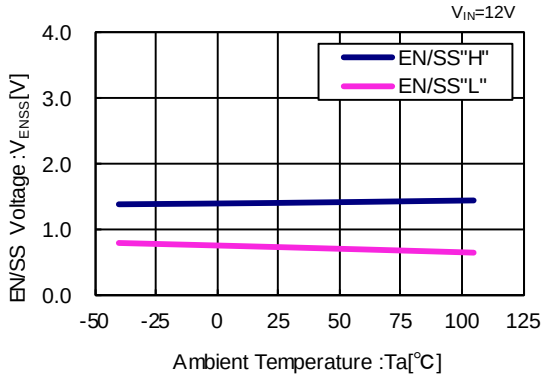
(13) PG Output Voltage vs. Ambient Temperature

XD926xB75Dxx



(14) EN/SS Voltage vs. Ambient Temperature

XD926xB75Dxx



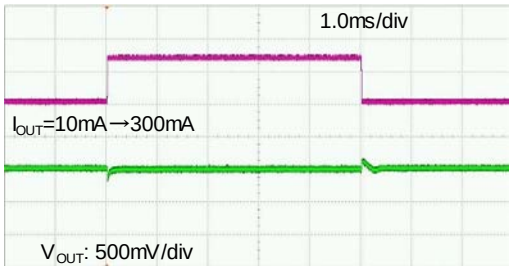
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(15) Load Transient Response

XD9267B75Dxx

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA

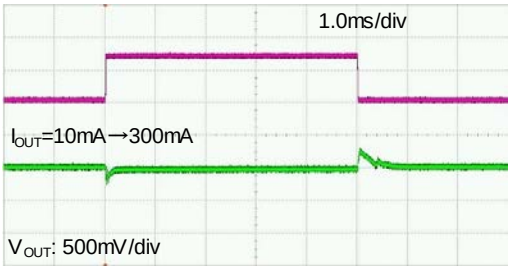
L=2.2μH(CLF5030NIT-2R2N),
C_{IN}=2.2μF×2(CGA4J3X7R1H225K125AB)
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



XD9268B75Dxx

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA

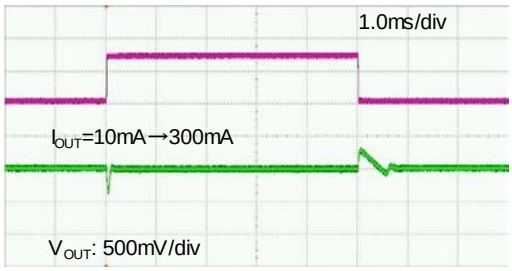
L=2.2μH(CLF5030NIT-2R2N),
C_{IN}=2.2μF×2(CGA4J3X7R1H225K125AB)
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



XD9267B75Dxx

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA

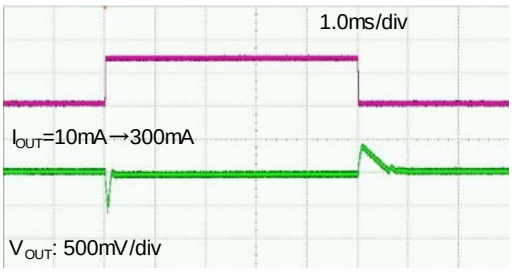
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD9268B75Dxx

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA

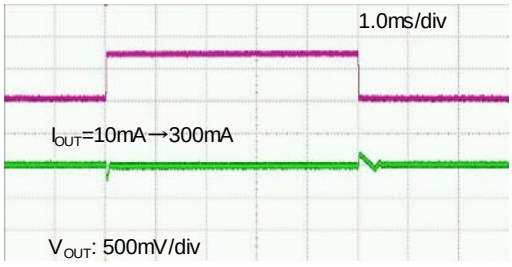
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD9267B75Dxx

V_{IN}=24V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA

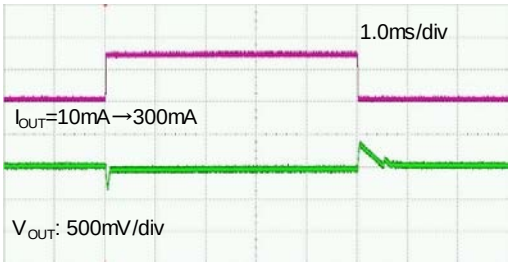
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD9268B75Dxx

V_{IN}=24V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA

L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



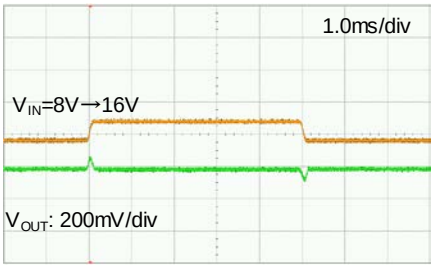
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(16) Input Transient Response

XD926xB75Dxx

V_{IN}=8V→16V, V_{OUT}=5.0V, I_{OUT}=300mA

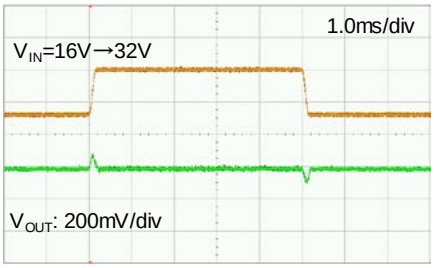
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD926xB75Dxx

V_{IN}=16V→32V, V_{OUT}=5.0V, I_{OUT}=300mA

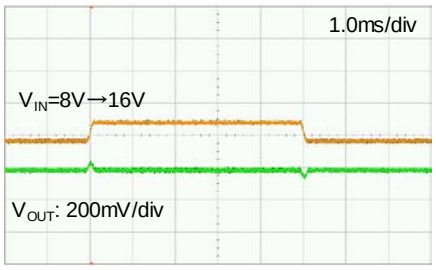
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD926xB75Dxx

V_{IN}=8V→16V, V_{OUT}=3.3V, I_{OUT}=300mA

L=2.2μH(CLF5030NIT-2R2N),
C_{IN}=2.2μF×2(CGA4J3X7R1H225K125AB)
C_L=10μF×2 (CGA5L1X7R1C106K160AC)

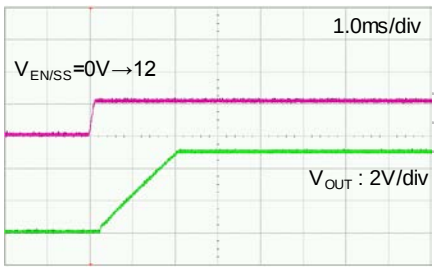


(17) EN/SS Rising Response

XD926xB75Dxx

V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=5V, I_{OUT}=300mA

L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD926xB75Dxx

V_{IN}=24V, V_{ENSS}=0→24V, V_{OUT}=5V, I_{OUT}=300mA

L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)

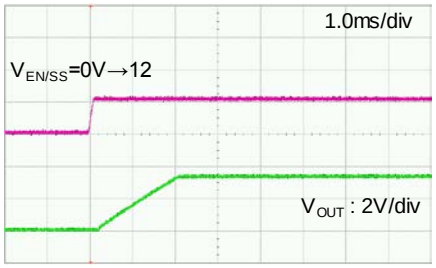
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(17) EN/SS Rising Response

XD926xB75Dxx

V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, I_{OUT}=300mA

L=2.2μH(CLF5030NIT-2R2N),
C_{IN}=2.2μF×2(CGA4J3X7R1H225K125AB)
C_L=10μF×2 (CGA5L1X7R1C106K160AC)

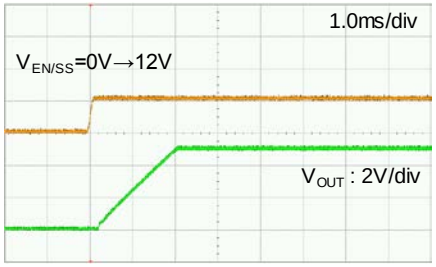


(18) VIN Rising Response

XD926xB75D

V_{IN}=0→12V, V_{ENSS}=0→12V, V_{OUT}=5V, I_{OUT}=300mA

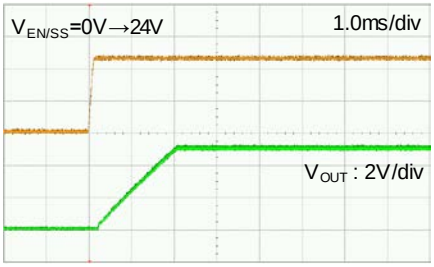
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD926xB75Dxx

V_{IN}=0→24V, V_{ENSS}=0→24V, V_{OUT}=5V, I_{OUT}=300mA

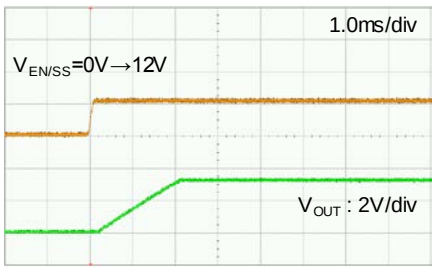
L=3.3μH(CLF5030NIT-3R3N),
CIN=2.2μF×2(CGA4J3X7R1H225K125AB)
CL=10μF×2 (CGA5L1X7R1C106K160AC)



XD926xB75Dxx

V_{IN}=0→12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, I_{OUT}=300mA

L=2.2μH(CLF5030NIT-2R2N),
C_{IN}=2.2μF×2(CGA4J3X7R1H225K125AB)
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



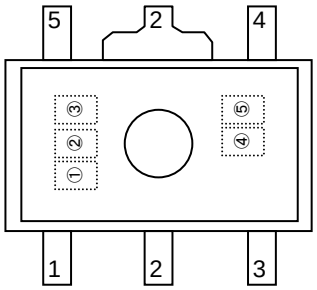
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SOT-89-5	SOT-89-5 PKG	JESD51-7 Board	SOT-89-5 Power Dissipation
USP-6C	USP-6C PKG	JESD51-7 Board	USP-6C Power Dissipation

■MARKING RULE

●SOT-89-5

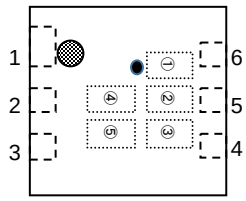


①② represents product series, products type,

MARK		PRODUCT SERIES
①	②	
K	1	XD9267B75***-Q
	2	XD9268B75***-Q

※USP-6C Under dot

●USP-6C(Under dot)



③ presents Oscillation Frequency

MARK	Oscillation Frequency	PRODUCT SERIES
U	2.2MHz	XD926*B75D**-Q

④⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ repeated
(G, I, J, O, Q, W excluded)* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions, excluding when specified for in-vehicle use or other uses.
   Do not use the product for in-vehicle use or other uses unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.