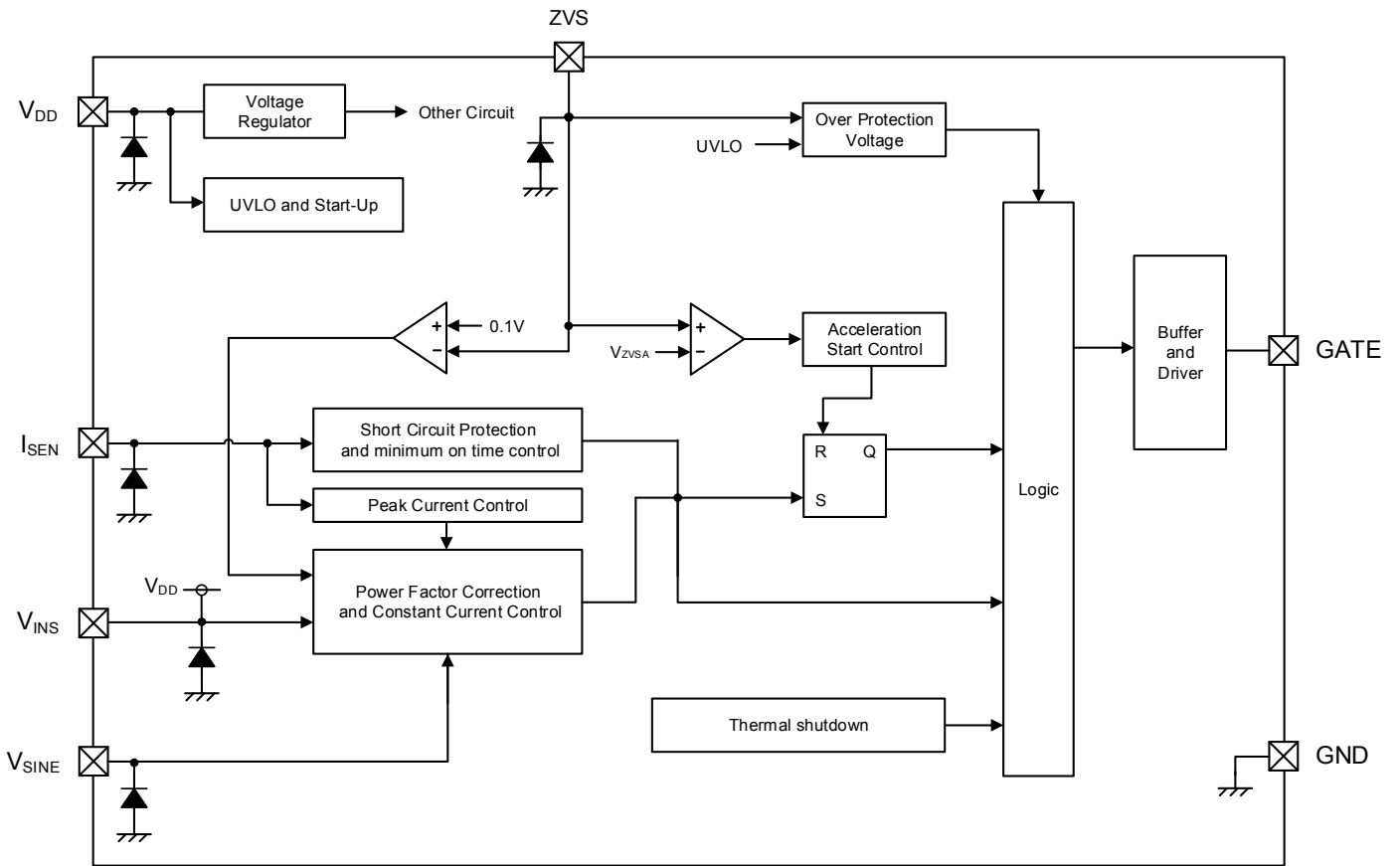


■ BLOCK DIAGRAM

XC9404 Series



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■ PRODUCT CLASSIFICATION

● Ordering Information

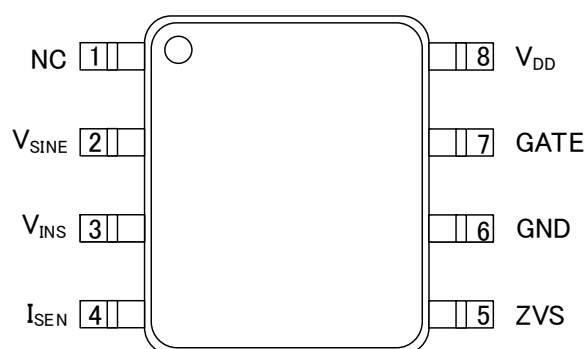
XC9404①②③④⑤⑥-⑦^(*)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	With PFC Function
②	Application	L	For Off-line Driver for LED Lighting
③④	Accuracy	03	LED Current Accuracy is $\pm 3\%$
⑤⑥-⑦	Package (Order Unit)	SR-G	SOP-8D (2,500pcs/Reel) ^(**)

^(*) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

^(**) The XC9404 reels are shipped in a moisture-proof packing.

■ PIN CONFIGURATION



SOP-8D
(TOP VIEW)

■ PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	NC	No connection.
2	V _{SINE}	V _{SINE} pin to detect the rectified sine waveform of input voltage.
3	V _{INS}	V _{INS} pin to detect the rectified sine waveform peak value of input voltage.
4	I _{SEN}	I _{SEN} pin monitors the primary current.
5	ZVS	ZVS pin to detect the feedback voltage from the auxiliary winding. ZVS voltage is used to control Over Voltage Protection and Acceleration Mode.
6	GND	Ground pin.
7	GATE	External power MOSFET drive pin.
8	V _{DD}	Power Input pin.

■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	RATINGS	UNITS
V _{DD} Pin Voltage	V _{DD}	-0.3 ~ +35	V
V _{INS} Pin Voltage	V _{INS}	-0.3 ~ +7.0	V
V _{SINE} Pin Voltage	V _{SINE}	-0.3 ~ +7.0	V
I _{SEN} Pin Voltage	V _{ISEN}	-0.3 ~ +7.0	V
ZVS Pin Voltage	V _{ZVS}	-40.0 ~ +10.0	V
GATE Pin Maximum Current	I _{GATE}	300	mA
Power Dissipation	P _D	0.525	W
Operating Ambient Temperature	T _a	-40 ~ 105	°C
Storage Temperature	T _{stg}	-65 ~ +150	°C

(*1) All voltages are described based on GND.

ELECTRICAL CHARACTERISTICS

XC9404 Series

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
V _{DD} Voltage Range	V _{DD}		9	-	21	V	-
Start-up Threshold Voltage	V _{ST}	V _{SINE} =V _{INS} =3V, V _{ISEN} =2V, V _{ZVS} =0V The voltage which V _{DD} pin current becomes 200uA or more while V _{DD} is increasing.	18	19	20	V	①
UVLO Detect Voltage	V _{UVLO}	V _{SINE} =V _{INS} =3V, V _{ISEN} =2V, V _{ZVS} =0V The voltage which V _{DD} pin current becomes 200uA or less while V _{DD} is decreasing.	7.5	8.0	8.5	V	①
V _{DD} Over Voltage Protection	V _{DD_OVP}	V _{SINE} =V _{INS} =3V, V _{ISEN} =V _{ZVS} =0V, V _{DD} =20V The voltage which GATE Voltage becomes "L" while V _{DD} is increasing.	28	32	34	V	②
Start-up Current	I _{ST}	V _{SINE} =V _{INS} =3V, V _{ISEN} =2V, V _{ZVS} =0V V _{DD} =V _{ST} -0.5V	-	-	20	μA	①
Supply Current	I _{DD1}	V _{SINE} =V _{INS} =3V, V _{ISEN} =1.2V, V _{ZVS} =0V V _{DD} =20V→15V	-	1000	1300	μA	①
GATE "H" level Voltage	V _{GATEH}	V _{SINE} =V _{INS} =3V, V _{ZVS} =V _{ISEN} =0V V _{DD} =20V→12V	10	-	-	V	①
GATE "L" level Voltage	V _{GATEL}	V _{SINE} =V _{INS} =3V, V _{ZVS} =V _{ISEN} =0V, V _{DD} =20V→15V V _{ISEN} is increased until GATE "L" occurs, 20 mA is applied to the GATE pin, and the GATE pin voltage is measured.	-	-	1	V	②
GATE clamp Voltage	V _{GATEC}	V _{SINE} =V _{INS} =3V, V _{ZVS} =V _{ISEN} =0V, V _{DD} =20V	12	13	15	V	①
(V _{SINE} /V _{INS}) maximum Value	(V _{SINE} /V _{INS}) _{max}	V _{SINE} =V _{INS} =3V, V _{ZVS} =0V, V _{DD} =20V→15V The voltage which GATE voltage becomes "L" while V _{ISEN} is increasing.	0.8	1.0	1.2	V	②
(V _{SINE} /V _{INS}) minimum Value	(V _{SINE} /V _{INS}) _{min}	V _{SINE} =0V, V _{INS} =3V, V _{ZVS} =0V, V _{DD} =20V→15V The voltage which GATE voltage becomes "L" while V _{ISEN} is increasing.	-	-	0.2	V	②
Minimum On Time	t _{ONMIN}	V _{SINE} =V _{INS} =3V, V _{ZVS} =0V, V _{ISEN} =2V V _{DD} is raised from 0V to 20V, and the GATE signal pulse width is measured.	500	750	1000	ns	①
Short Circuit Protection Voltage	V _{OCP}	V _{SINE} =3V, V _{INS} =0.5V, V _{ZVS} =V _{ISEN} =0V, V _{DD} =20V→15V The voltage which GATE voltage becomes "L" while V _{ISEN} is increasing.	3.0	4.0	-	V	②
ZVS Leakage Current	I _{ZVS}	V _{DD} =20V→15V, V _{ZVS} =4V	-	2	8	μA	③
ZVS Acceleration Threshold Voltage	V _{ZVSA}	V _{SINE} =1V, V _{INS} =3V, V ₆ =1.5V, V _{DD} =20V→15V The V ₆ voltage is raised, and the voltage at which the GATE pin voltage oscillation period slows is measured.	1.4	1.8	2.2	V	④
ZVS CV Threshold Voltage	V _{ZVSN}	V _{SINE} =1V, V _{INS} =3V, V ₆ =2.8V, V _{DD} =20V→15V The V ₆ voltage is raised, and the voltage at which the GATE pin voltage oscillation stops is measured.	3.8	4.0	4.4	V	④
ZVS Over Voltage Threshold Voltage	V _{OVP}	V _{SINE} =V _{INS} =3V, V _{ZVS} =V _{ISEN} =0V, V _{DD} =20V→15V The voltage which GATE voltage becomes "L" while V _{ISEN} is increasing.	5.6	6.0	6.9	V	②

OPERATIONAL EXPLANATION

The internal circuitry of the XC9404 series consists of a power factor improvement circuit, buffer drive circuit, over-current protection circuit, over-voltage protection circuit, UVLO circuit and Thermal shutdown circuit. (Refer to the block diagram)

<Operation description>

The operation of the XC9404 series is described below using an isolated flyback type circuit.

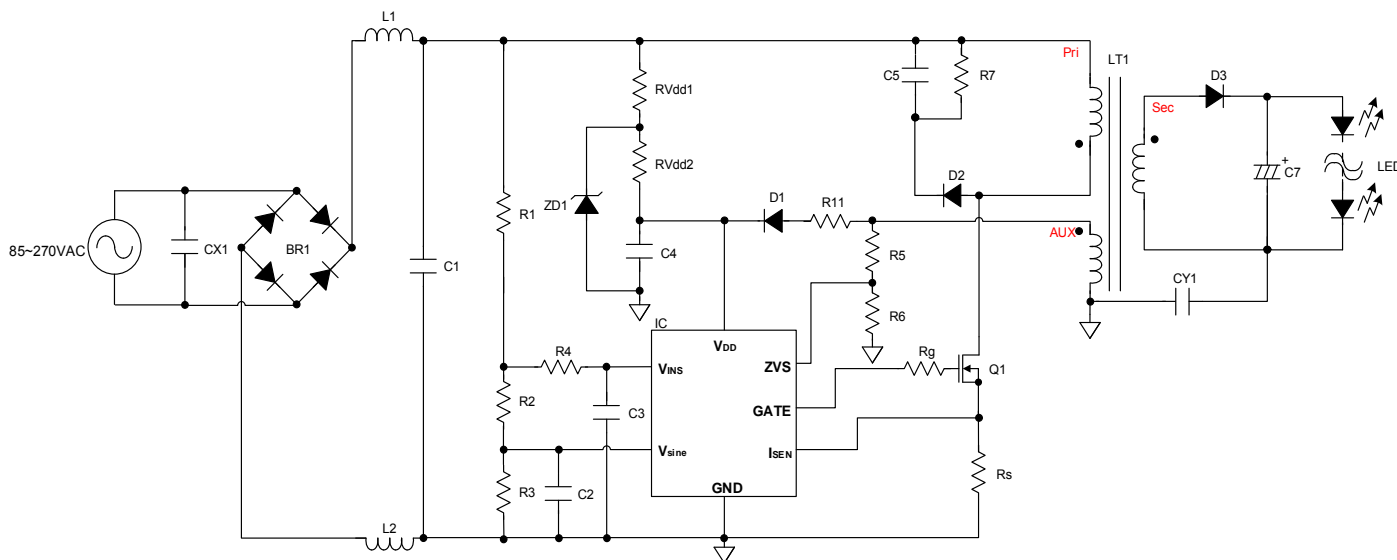


Fig.1 XC9404 Isolated flyback circuit

By controlling the primary peak current of the transformer so that it matches the V_{ISEN} voltage, which has the same phase as the input voltage, the IC improves the power factor. (Refer to Fig. 2)

In addition, by controlling the on-time/off-time so that it is optimum for the input voltage, phase and LED voltage, a stable constant current can be supplied within the input voltage range 85VAC to 270VAC.

The on-time,off-time can be adjusted with external resistances R1 to R3, enabling the optimum constant to be set for the input voltage, LED voltage, LED current. Operation in discontinuous mode (DCM) is recommended for this IC, so the external resistances R1 to R3 should be adjusted to enable discontinuous mode.

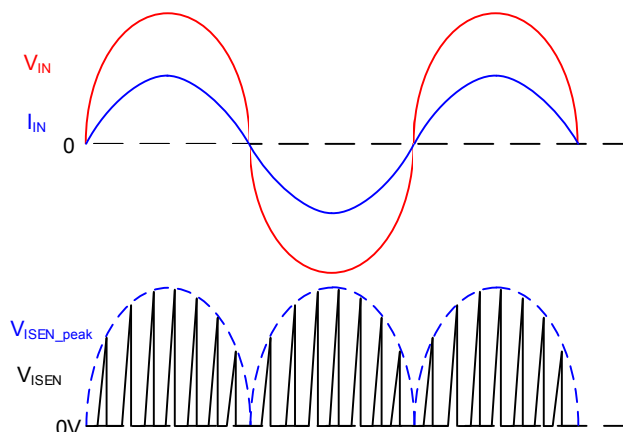


Fig.2 XC9404 Operation Waveform

OPERATIONAL EXPLANATION

<Operation modes>

The XC9404 series operates in modes (a) to (d) based on the ZVS pin voltage.

(a) Acceleration Mode

Acceleration Mode is used for fast startup.

To shorten the startup time, the output voltage is low, and when the ZVS pin voltage is below the ZVS Acceleration Threshold Voltage, the IC operates in critical mode rather than Discontinuous Current Mode to reduce the startup time.

When the ZVS pin voltage rises above the ZVS Acceleration Threshold Voltage, the mode changes to CC Mode.

(b) CC Mode

CC mode provides the high power factor and low THD that are desirable in a LED lighting power source, and outputs a stable constant current that is not affected by fluctuations of input voltage and LED voltage. While in CC Mode, the IC operates in Discontinuous Current Mode.

(c) CV Mode

CV Mode prevents the output voltage from exceeding a set voltage. In the event that the output voltage reaches the over-voltage state, the ZVS pin voltage rises. When the ZVS pin voltage rises above the ZVS CV Threshold Voltage, the GATE pin outputs "L" voltage, and maintains "L" voltage until the ZVS pin voltage drops below the ZVS CV Threshold Voltage.

(d) Over-Voltage Protection

This mode prevents damage to peripheral devices in the event that the output voltage reaches the over-voltage state. When the output voltage reaches the over-voltage state, the ZVS pin voltage rises. When the ZVS pin voltage rises above the ZVS Over-Voltage Threshold Voltage, the GATE pin voltage is forcibly latched to the "L" state. To release the voltage from the latched state and return to normal operation, the V_{DD} pin voltage is lowered below the latch release at 5.6V voltage and then raised above the Start-up Threshold Voltage.

Even when the LED is in the open state, this function can suppress destruction of external components.

<Minimum On Time>

Because the charge stored on the capacitance between Q1 Drain-Source flows to the sense resistance R_s immediately after power MOSFET Q1 turns on, a spike occurs in the I_{SEN} pin voltage. To prevent this spike noise from causing malfunctioning of the internal circuitry, a minimum on-time t_{ONMIN} is established. The GATE pin voltage is forcibly held in the "L" state until the minimum on-time elapses.

<GATE pin Voltage>

When in the GATE pin "H" state, the GATE pin Voltage is controlled so as not to exceed the GATE clamp voltage. This prevents over-voltage between Gate-Source of FET Q1 that may destroy the FET.

The GATE pin voltage in the GATE pin "H" state varies depending on the V_{DD} pin voltage.

(a) V_{DD} pin Voltage < GATE clamp Voltage + (12V - GATE "H" level Voltage)
GATE "H" Voltage = V_{DD} - (12V - GATE "H" level Voltage)

(b) V_{DD} pin Voltage > GATE clamp Voltage + (12V - GATE "H" level Voltage)
GATE "H" Voltage = GATE clamp Voltage

■ OPERATIONAL EXPLANATION

<UVLO>

If the V_{DD} pin voltage drops below the UVLO detect voltage (V_{UVLO}), the GATE pin voltage is forcibly put in the “L” state to prevent IC malfunctioning. When the V_{DD} pin voltage rises above the Start-up Threshold Voltage, the UVLO state is released and normal operation starts. The IC quiescent current is held below 20 μ A in the UVLO state, enabling reduction of standby power and the need for high resistances for $R_{VDD1, 2}$.

When a LED short circuits, the V_{DD} pin voltage drops below the UVLO detect voltage, and thus the UVLO function can suppress destruction of external components.

< V_{DD} Over Voltage Protection>

This prevents IC destruction caused by V_{DD} pin over-voltage. When the V_{DD} pin voltage rises above the V_{DD} Over-Voltage Protection voltage, the GATE pin voltage is forcibly kept in the “L” state to suppress any further increases of the V_{DD} pin voltage.

<Short Circuit Protection Voltage>

This prevents peripheral component destruction in the event that excessive current flows to the sense resistance R_s due to short-circuiting of an external component or otherwise.

This function protects external components in the event that excessive current flows to the sense resistance R_s due to short-circuiting of an external component or otherwise.

When excessive current flows to the sense resistance R_s and the I_{SEN} pin voltage rises above the Short Circuit Protection Voltage, the GATE pin voltage is forcibly latched to the “L” state. This suppresses damage to external components due to over-current.

The latched state is released and normal operation resumes when the V_{DD} pin voltage is lowered below the latch release voltage at 5.6V and then raised above the Start-up Threshold Voltage.

<Thermal shutdown>

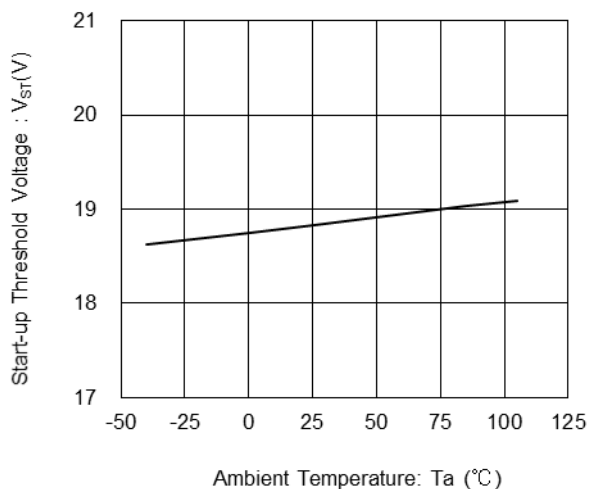
To protect the IC from thermal destruction, the thermal shutdown function activates when the chip temperature reaches 170°C and forcibly puts the GATE pin voltage in the “L” state. When the chip temperature drops down to 145°C, normal operation resumes.

■ NOTES ON USE

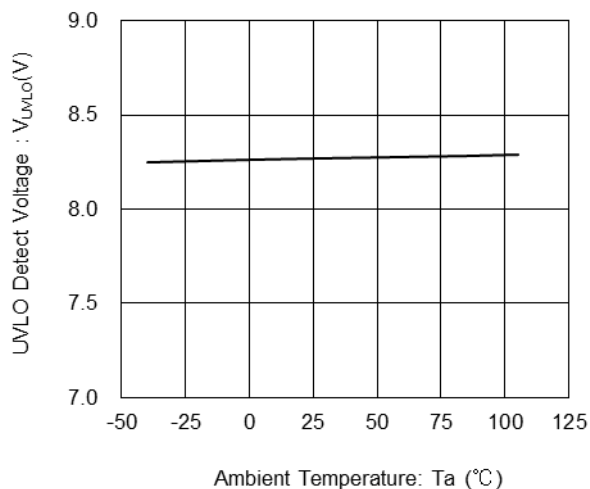
- 1) Take care that the absolute maximum ratings of external components and the IC are not exceeded.
- 2) External components and the circuit board layout have a large effect on characteristics.
Test sufficiently with the actual device before use.
- 3) Give consideration to derating when selecting external components.
In particular, external components may become hot due to heat generated by LEDs and other components.
Select components and design for heat radiation.
- 4) Select external components and design the test circuit board so as to satisfy applicable regulations and standards.
- 5) Torex places an importance on improving our products and their reliability.
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

TYPICAL PERFORMANCE CHARACTERISTICS

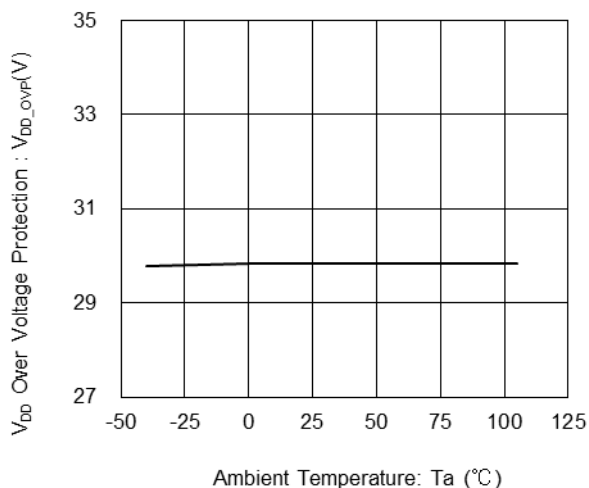
(1) Start-up Threshold Voltage vs. Ambient Temperature



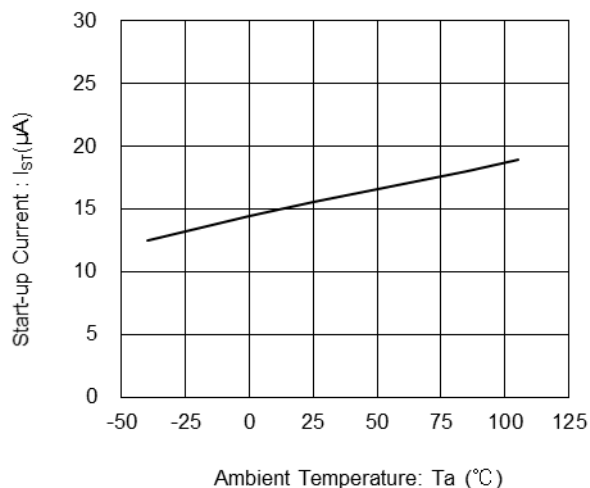
(2) UVLO Detect Voltage vs. Ambient Temperature



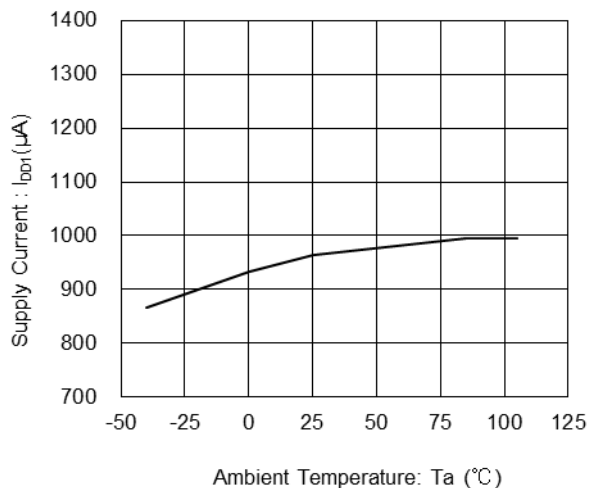
(3) V_{DD} Over Voltage Protection vs. Ambient Temperature



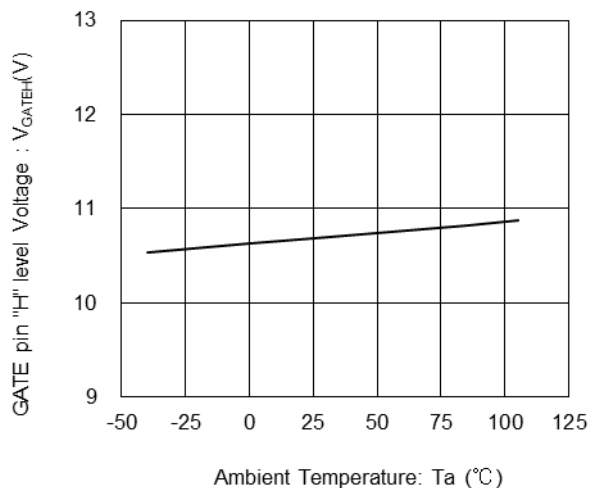
(4) Start-up Current vs. Ambient Temperature



(5) Supply Current vs. Ambient Temperature

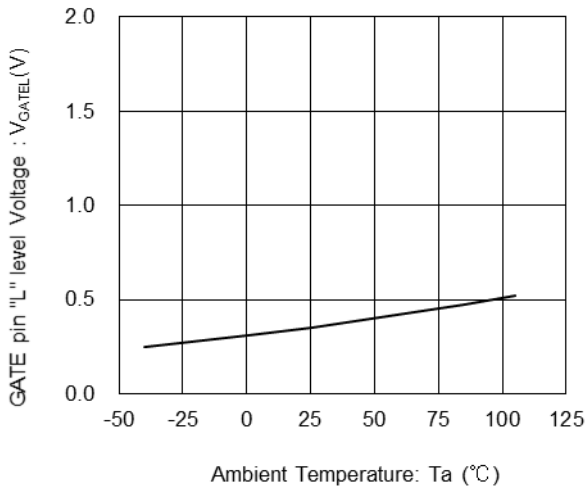


(6) GATE pin "H" level Voltage vs. Ambient Temperature

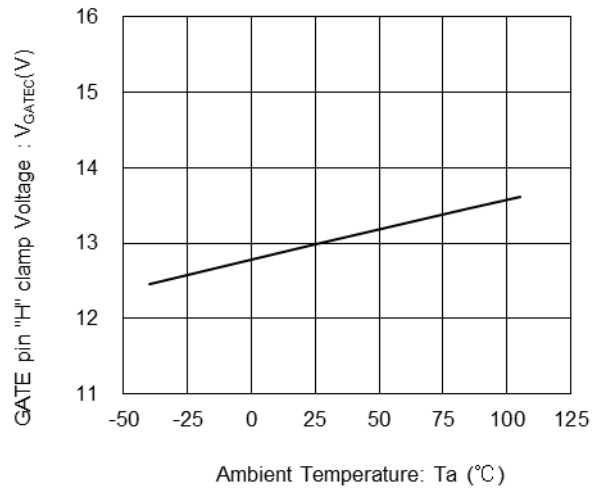


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

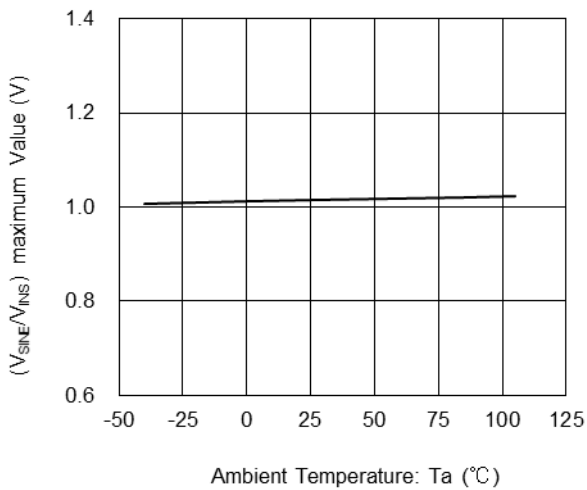
(7) GATE pin "L" level Voltage vs. Ambient Temperature



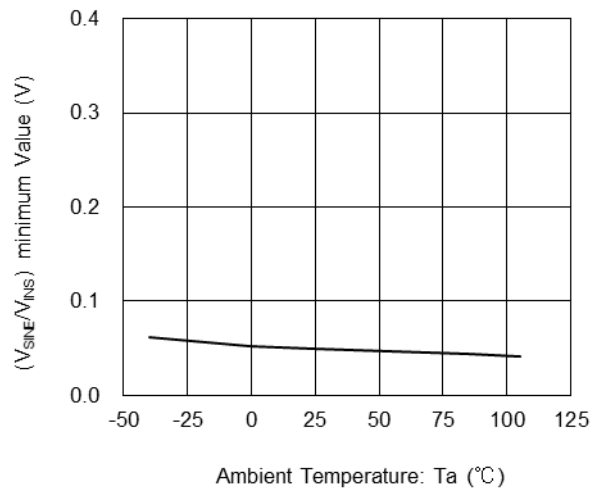
(8) GATE pin clamp Voltage vs. Ambient Temperature



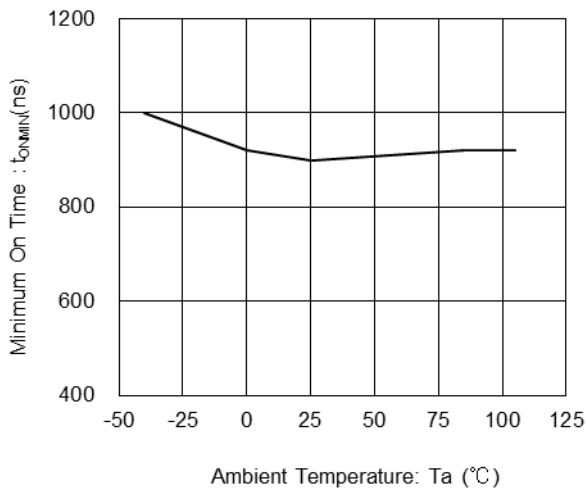
(9) (V_{SINE}/V_{INS}) maximum Value vs. Ambient Temperature



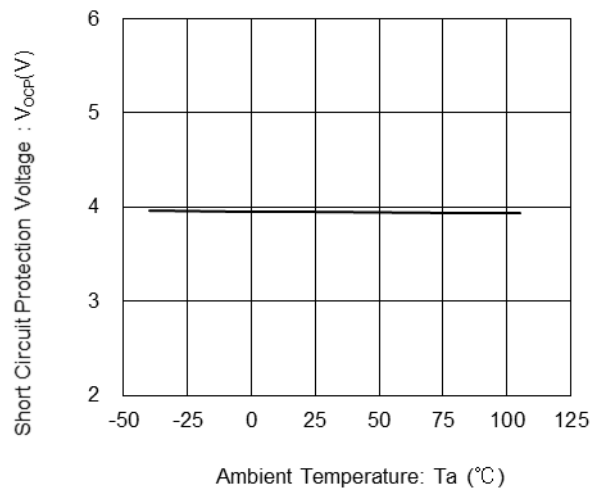
(10) (V_{SINE}/V_{INS}) minimum Value vs. Ambient Temperature



(11) Minimum On Time vs. Ambient Temperature

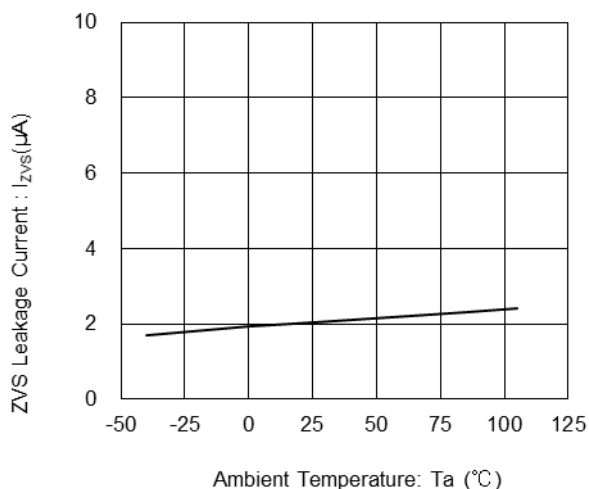


(12) Short Circuit Protection Voltage vs. Ambient Temperature

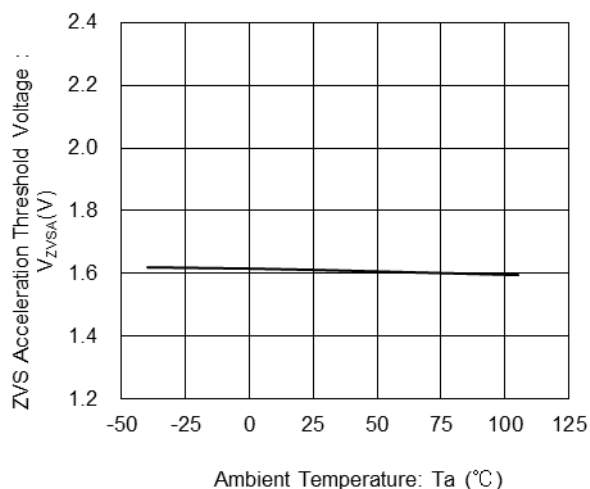


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

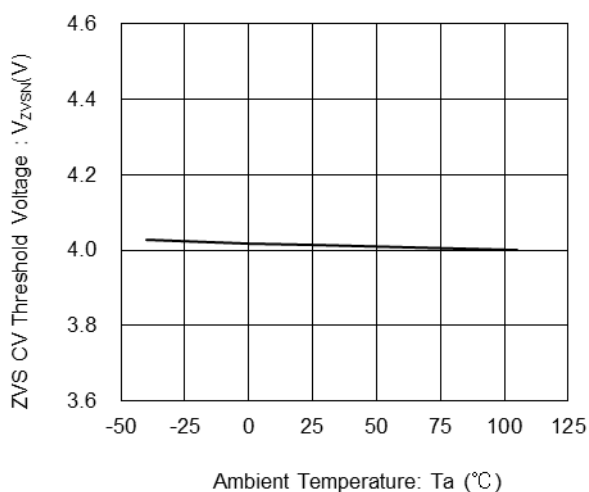
(13) ZVS Leakage Current vs. Ambient Temperature



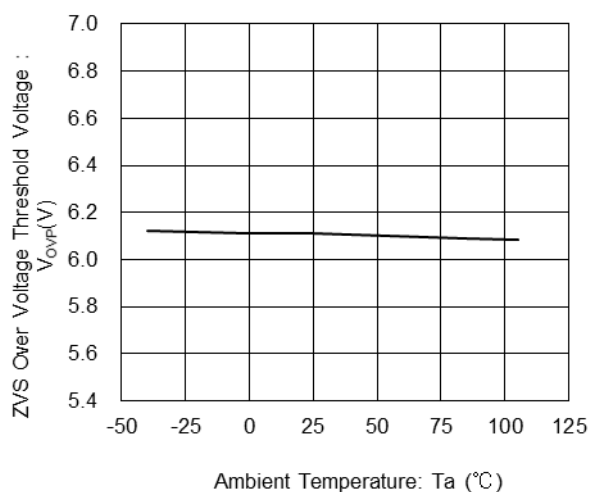
(14) ZVS Acceleration Threshold Voltage vs. Ambient Temperature



(15) ZVS CV Threshold Voltage vs. Ambient Temperature

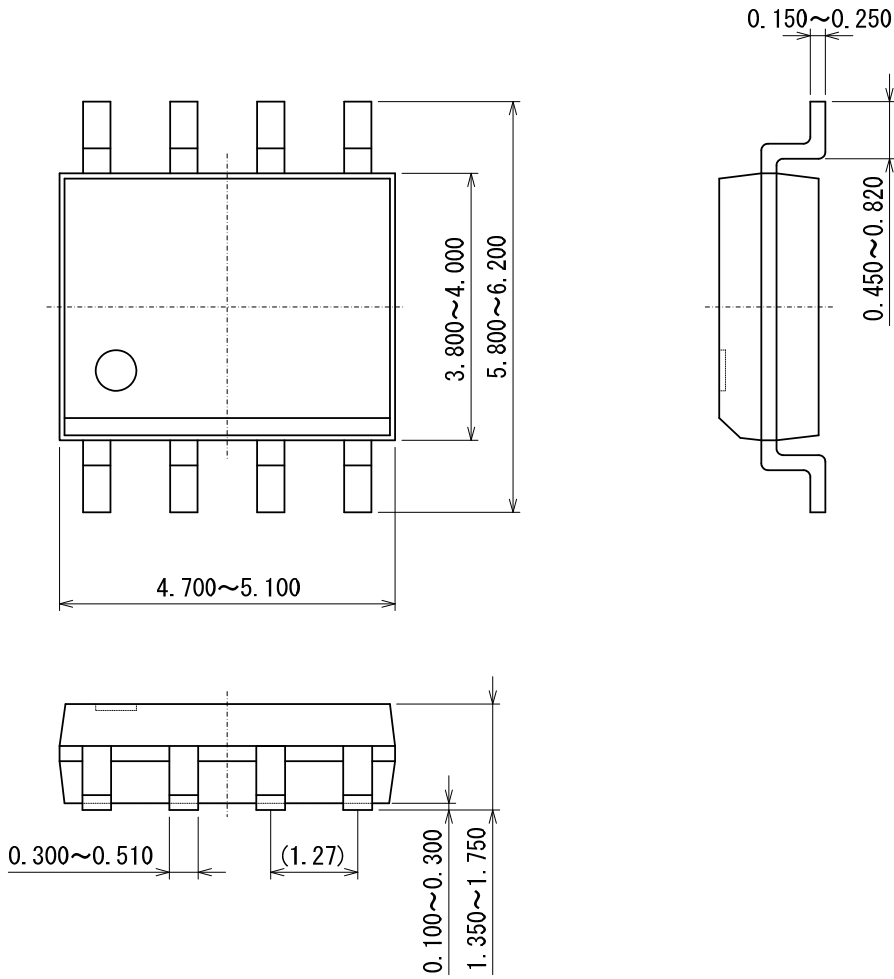


(16) ZVS Over Voltage Threshold Voltage vs. Ambient Temperature

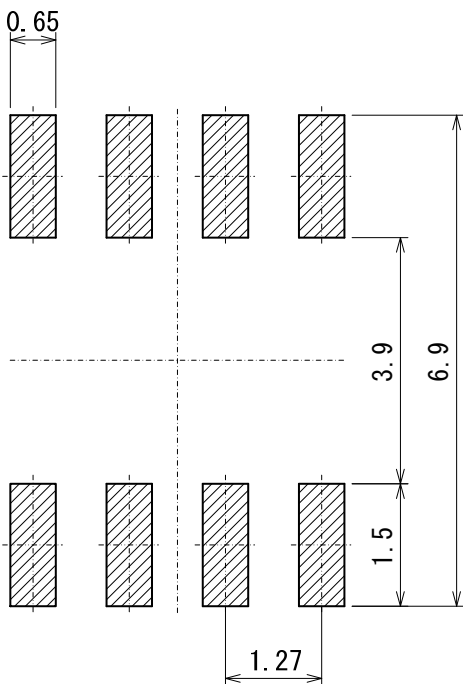


PACKAGING INFORMATION

●SOP-8D (unit:mm)

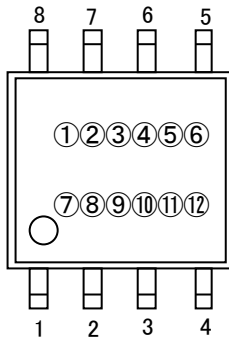


●SOP-8D Reference Pattern Layout (unit:mm)



MARKING RULE

● SOP-8D



①~⑥ represents Marking ID

MARK						PRODUCT SERIES
①	②	③	④	⑤	⑥	
X	C	9	4	0	4	XC9404*****-G

⑦ represents Last digit of manufacture year

Example

MARK	MANUFACTURE YEAR
5	Y2015

⑧,⑨ represents working week at molding process

⑩ represents Assembly Site Code

N: Nantong Fujitsu

⑪,⑫ represents Batch No.

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