Toshiba BiCD process integrated circuit silicon monolithic

TB67S285FTG

Active Gain Control Serial Control Bipolar stepping motor driver

The TB67S285FTG is a 3-wire serial controlled bipolar stepping motor driver with a built-in Active Gain Control architecture.
The TB67S285FTG also has an internal current feedback control (ACDS) which enables the driver to control the motor current without using a sense resistor.
Using the BiCD process, the TB67S285FTG is rated at 50 V, 3.0 A.

P-VQFN48-0707-0.50-004
Weight: 0.14 g (typ.)

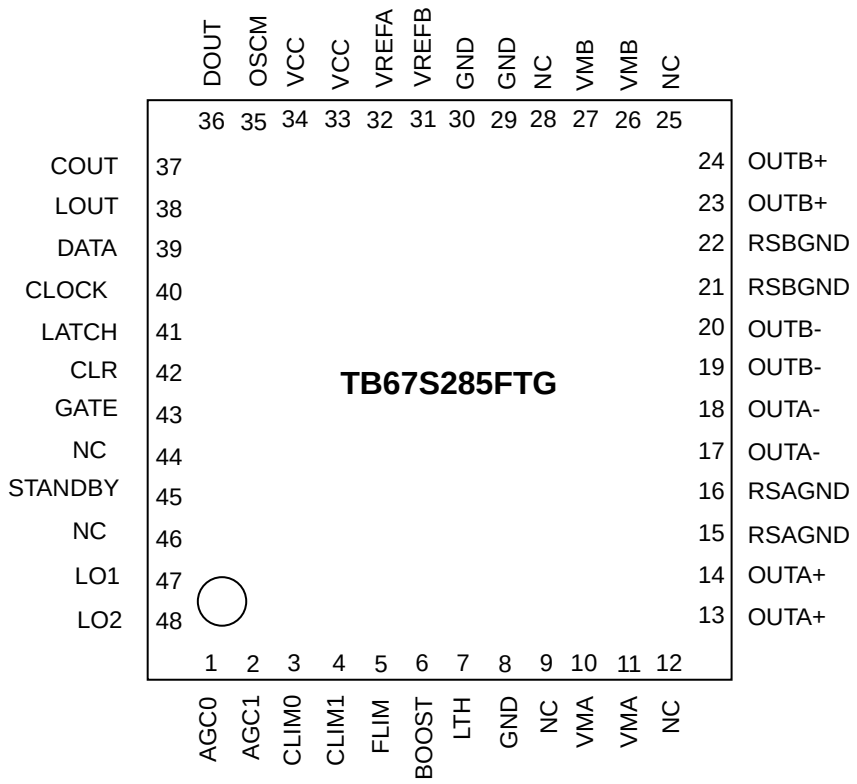
Features

- Built-in Anti-stall architecture (AGC: Active Gain Control)
- Built-in sense resistor less current control architecture (ACDS: Advanced Current Detection System)
- Low Rds (on) MOSFET (High side+ Low side=0.4 Ω (typ.))
- Built-in serial-parallel convert circuit
- Serial output function for cascade connection
- 4 bit (16 steps) adjustable torque function
- Multi error detect functions (Thermal shutdown (TSD), Over current detection (ISD), Power-on-reset (POR), Motor load open (OPD))
- Error detection status output (Error Output)
- Internal VCC (5 V) regulator enables the driver to operate with a single power supply (VM).
- Adjustable constant current PWM frequency using external components
- Small package with thermal pad on back side (QFN48: 7.0 mm x 7.0 mm)

Note: Please consider the heat condition when using the TB67S285FTG.

Pin assignment

(Top View)



Note Please solder the corner pad and the rear thermal pad of the QFN package, to the GND pattern of the PCB.

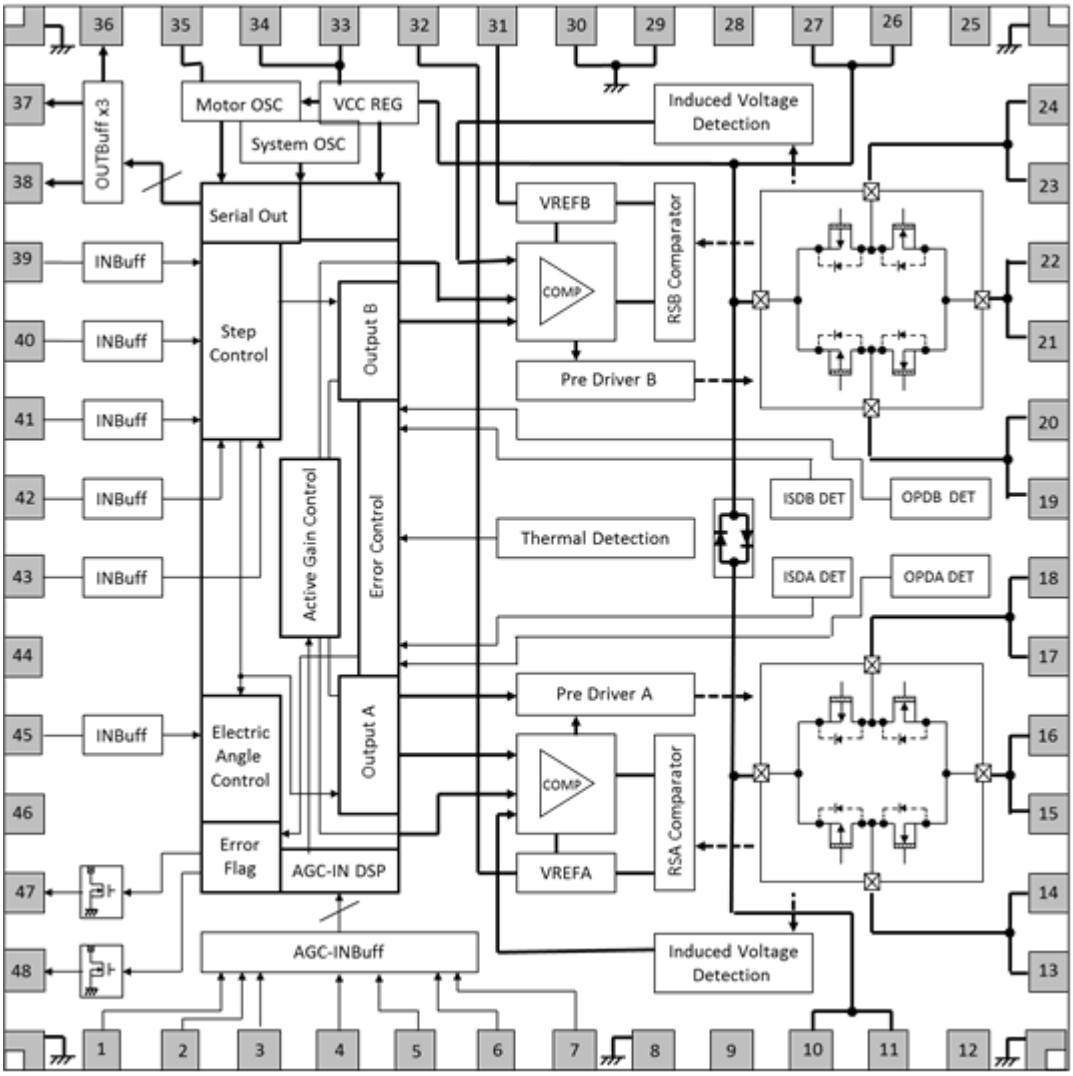
Pin description

Pin No	Pin name	Pin function
1	AGC0	Active Gain Control setup pin No.0
2	AGC1	Active Gain Control setup pin No.1
3	CLIM0	AGC current limiter setup pin No.0
4	CLIM1	AGC current limiter setup pin No.1
5	FLIM	AGC frequency limiter setup pin
6	BOOST	AGC current boost setup pin
7	LTH	AGC threshold setup pin
8	GND	Ground pin
9	NC	Non connection
10	VMA	Motor power supply input pin
11	VMA	Motor power supply input pin
12	NC	Non connection
13	OUTA+	Ach motor output (+) pin
14	OUTA+	Ach motor output (+) pin
15	RSAGND	Ach motor power ground pin
16	RSAGND	Ach motor power ground pin
17	OUTA-	Ach motor output (-) pin
18	OUTA-	Ach motor output (-) pin
19	OUTB-	Bch motor output (-) pin
20	OUTB-	Bch motor output (-) pin
21	RSBGND	Bch motor power ground pin
22	RSBGND	Bch motor power ground pin
23	OUTB+	Bch motor output (+) pin
24	OUTB+	Bch motor output (+) pin
25	NC	Non connection
26	VMB	Motor power supply input pin
27	VMB	Motor power supply input pin
28	NC	Non connection
29	GND	Ground pin
30	GND	Ground pin
31	VREFB	Bch current threshold reference pin
32	VREFA	Ach current threshold reference pin
33	VCC	Internal regulator voltage monitor pin
34	VCC	Internal regulator voltage monitor pin
35	OSCM	Internal oscillator frequency monitor and setting pin
36	DOUT	Serial data output pin
37	COUT	Serial clock output pin
38	LOUT	Serial latch output pin
39	DATA	Serial data input pin
40	CLOCK	Serial clock input pin
41	LATCH	Serial latch input pin
42	CLR	Serial register clear pin
43	GATE	Serial gate setup pin
44	NC	Non connection
45	STANDBY	Standby setup pin
46	NC	Non connection
47	LO1	Error flag output pin No.1
48	LO2	Error flag output pin No.2

Note: Please leave the NC pins open and do not connect any PCB pattern.

Note: For pins with the same pin name; connect the pins together at the nearest point of the driver.

Block diagram



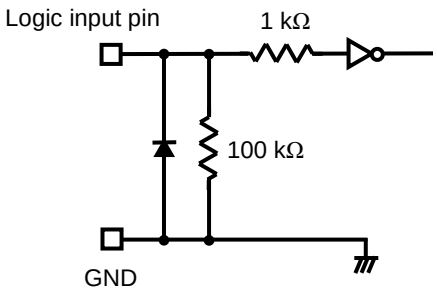
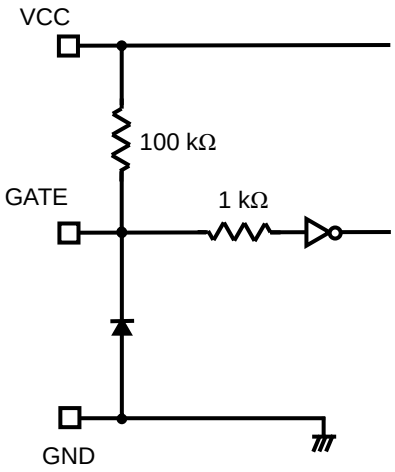
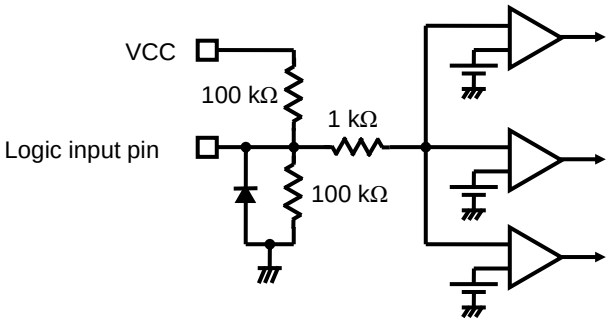
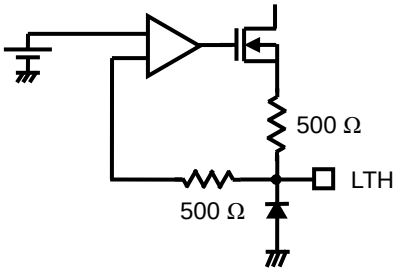
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

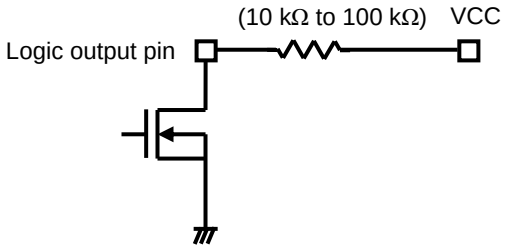
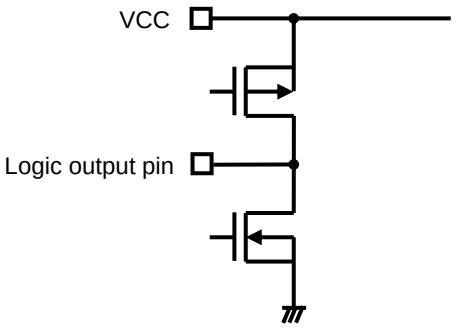
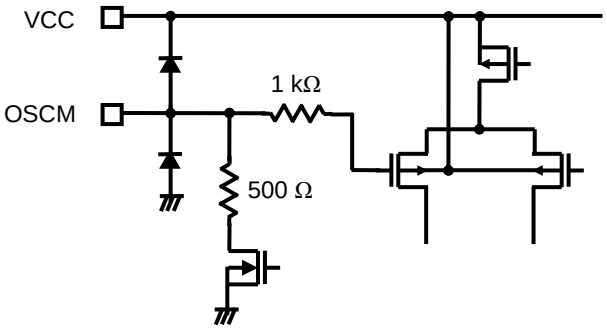
Note: All the grounding wires of the TB67S285FTG should run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.

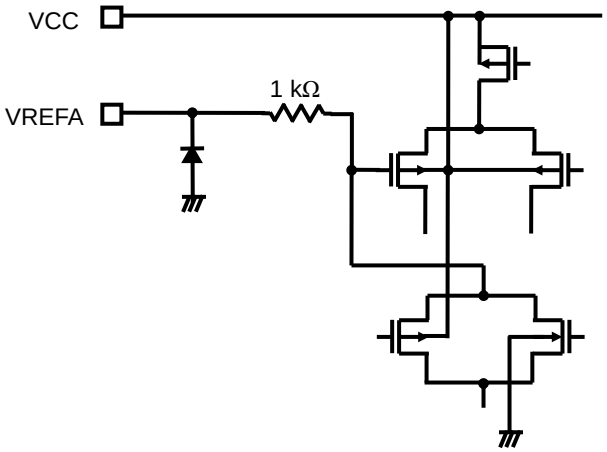
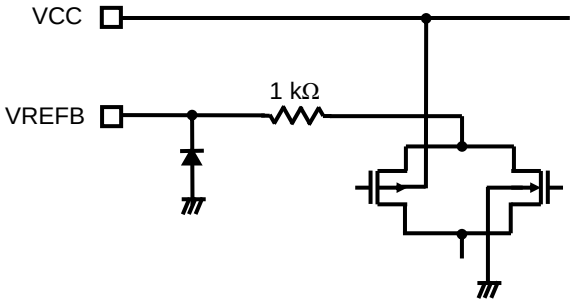
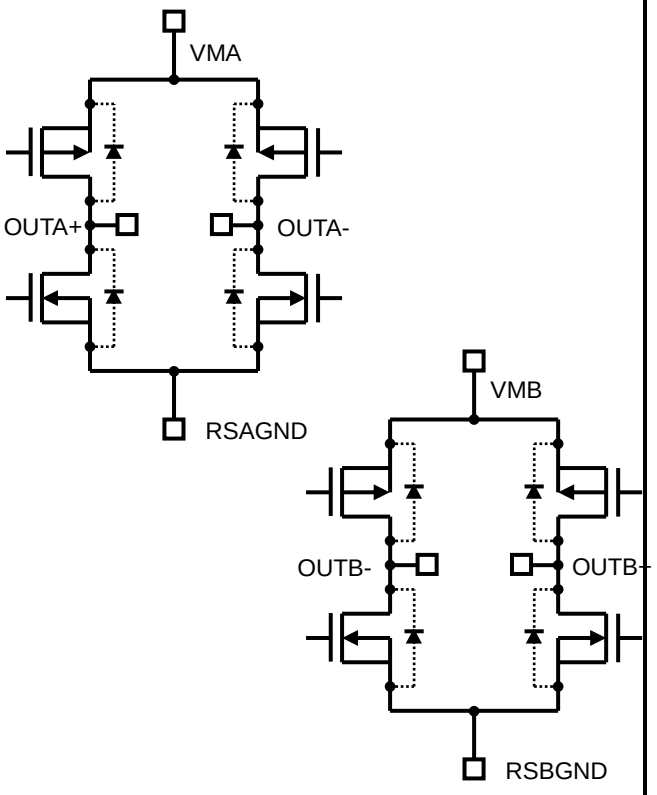
Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.
Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RSGND line, OUT line, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.

The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

Input-Output equivalent circuit

Pin name	Input-Output signal	Input-Output equivalent circuit
CLOCK DATA LATCH CLR STANDBY AGC0 AGC1 CLIM0	Logic input pin voltage GND ≤ VIN1(L) ≤ 2.0 V 3.0 V ≤ VIN1(H) ≤ 5.5 V	
GATE	Logic input pin voltage GND ≤ VIN1(L) ≤ 2.0 V 3.0 V ≤ VIN1(H) ≤ 5.5 V	
CLIM1 FLIM BOOST	Multi state input pin voltage VCC, GND, VCC-100 kΩ pull-up, or GND-100 kΩ pull-down (Resistance accuracy should be within ±20 %.)	
LTH	100 kΩ pull-down (Resistance accuracy should be within ±20 %.)	

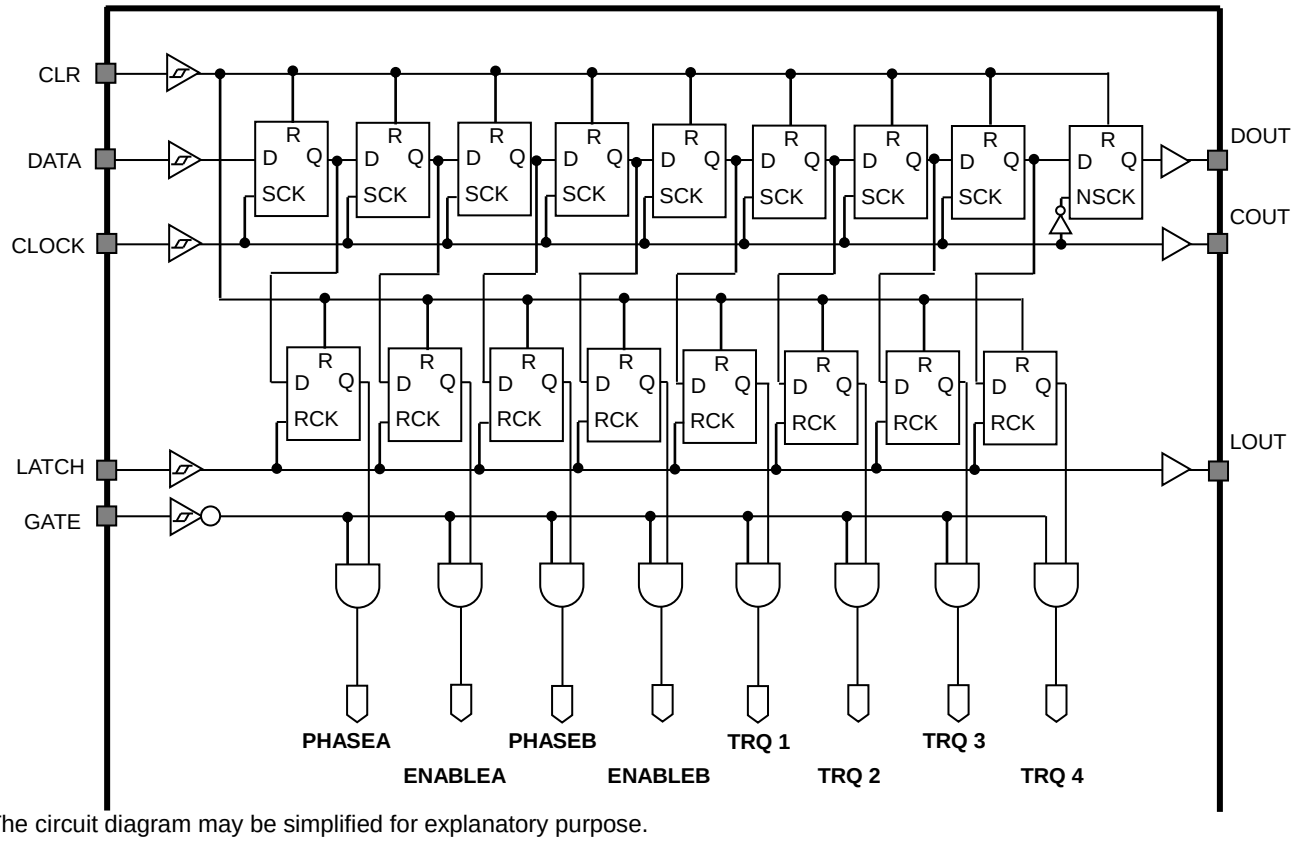
Pin name	Input-Output signal	Input-Output equivalent circuit
LO1 LO2	Logic output pin 0V ≤ VOUT(L) ≤ 0.5 V 4.75 V ≤ VOUT(H) ≤ 5.25 V	
DOUT COUT LOUT	Logic output Low level: GND+0.15 V(typ.) High level: VCC-0.15 V(typ.)	
OSCM	OSCM frequency range 0.64 MHz ≤ fOSCM ≤ 2.4 MHz	

Pin name	Input-Output signal	Input-Output equivalent circuit
VCC VREFA	VCC voltage range 4.75 V ≤ VCC ≤ 5.25 V	
VREFB	VREF input voltage range GND ≤ VREF ≤ 3.6 V	
VMA VMB OUT A+ OUT A- OUT B+ OUT B- RSAGND RSBGND	VM operation voltage range 10 V ≤ VM ≤ 47 V Output pin voltage range 10 V ≤ VM ≤ 47 V	

The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

♦ Basic function of stepping motor control

1. Serial function



The circuit diagram may be simplified for explanatory purpose.

	[LSB]	—	—	—	—	—	—	[MSB]
Internal signal	PHASEA	ENABLEA	PHASEB	ENABLEB	TRQ1	TRQ2	TRQ3	TRQ4

Note: DOUT outputs a signal at the CLOCK down-edge to keep the setup hold time with the COUT signal. Therefore, for example, when fixing the CLOCK signal to High before the serial data input, please configure it after inputting the CLOCK down edges. In this case, the number of the CLOCK down edges should be equal to that of the up edges, which are inputted during data transfer.

Truth table of serial input

GATE	CLR	DATA	CLOCK	LATCH	Function
High	Don't care				TRQ4, TRQ3, TRQ2, TRQ1, ENABLEB, PHASEB, ENABLEA, and PHASEA: Disable
Low	Low	Don't care			TRQ4, TRQ3, TRQ2, TRQ1, ENABLEB, PHASEB, ENABLEA, and PHASEA: Enable
	High	Low	↑	Don't care	The first data of the shift register is L, and the other register will be stored with the data before.
		High	↑		The first data of the shift register is H, and the other register will be stored with the data before.
		Don't care	↓		The shift register data maintains its state. The data after the shift register (Qh) is outputted from DOUT pin.
			Don't care	↑	Shift register data is stored to the storage register.
				↓	The storage register data maintains its state.

2. Internal signal (TRQ1, TRQ2, TRQ3, and TRQ4) function

Constant current PWM threshold can be adjusted by switching the TRQ configuration. The current ratio of the constant current PWM threshold (IOUT) can be configured to 100 % by applying VREF voltage externally. Moreover, this current ratio can be switched arbitrary by using TRQ function.

TRQ1	TRQ2	TRQ3	TRQ4	Current ratio (%)
High	High	High	High	100
			Low	94
		Low	High	86
			Low	80
	Low	High	High	74
			Low	67
		Low	High	60
			Low	52
Low	High	High	High	43
			Low	38
		Low	High	29
			Low	25
	Low	High	High	15
			Low	10
		Low	High	5
			Low	0

3. Internal signal (ENABLEA and ENABLEB) function

Each output block is turned on and off by this function. The operation of the corresponding channel is started by switching ON and stopped by switching OFF. (In the state of OFF, all of the output MOSFET are turned off and become high impedance state (below is written Hi-Z)).

ENABLEA	Function
High	Ach output: ON (Ach output operation)
Low	Ach output: OFF (Ach output stop)

ENABLEB	Function
High	Bch output: ON (Bch output operation)
Low	Bch output: OFF (Bch output stop)

4. Internal signal (PHASEA and PHASEB) function

Current direction for each output block is switched by this function. When the signal is set to High, the current direction is from OUT (+) to OUT (-) in charging. When the signal is set to Low, the current direction is from OUT (-) to OUT (+) in charging.

PHASEA	Function
High	Current direction in Charge: OUTA+ → OUTA-
Low	Current direction in Charge: OUTA- → OUTA+

PHASEB	Function
High	Current direction in Charge: OUTB+ → OUTB-
Low	Current direction in Charge: OUTB- → OUTB+

Internal signal and step resolution

Stepping motor can be driven with full-step or half-step resolution by switching the internal signal one by one with the serial inputs.

[Full step resolution]

Ach			Bch		
Internal signal		Output	Internal signal		Output
PHASEA	ENABLEA	IOUT(A)	PHASEB	ENABLEB	IOUT(B)
High	High	+100%	High	High	+100%
Low		-100%	High		+100%
Low		-100%	Low		-100%
High		+100%	Low		-100%

[Half step resolution]

Ach			Bch		
Internal signal		Output	Internal signal		Output
PHASEA	ENABLEA	IOUT(A)	PHASEB	ENABLEB	IOUT(B)
Don't care	Low	±0%	High	High	+100%
Low	High	-100%	Don't care	Low	±0%
Don't care	Low	±0%	Low	High	-100%
High	High	+100%	Don't care	Low	±0%
			High	High	+100%

5. GATE function

Inputted serial data are kept in the shift register or the storage register, or reflected on the actual IC operation by this function. While GATE signal is High, all signals of TRQ1, TRQ2, TRQ3, TRQ4, PHASEA, PHASEB, ENABLEA, and ENABLEB become Low.

GATE	Function
High	TRQ1, TRQ2, TRQ3, TRQ4, PHASEA, PHASEB, ENABLEA, and ENABLEB= All Low
Low	Data in register are reflected on the IC operation

6. CLR function (low active)

Data in the shift register or the storage register are cleared by CLR signal.

CLR	Function
High	Keep data in shift register or storage register (not initialized)
Low	Data in shift register or storage register are initialized

7. STANDBY function (low active)

Standby function is switched between on and off. When standby function is ON, all of the internal oscillator (OSCM) circuit and output MOSFET are turned off. Error detect states can be also released by this standby function because the internal logic circuits are initialized. When standby function is OFF, the operation is returned to the normal mode.

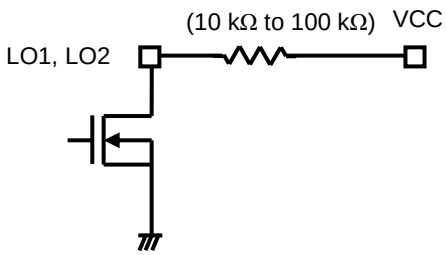
STANDBY	Function
High	Standby mode: OFF (normal operation)
Low	Standby mode: ON (oscillator circuit and output block: OFF, internal logic circuits: initialized)

8. LO1, LO2 (Error Output: error detect flag output) function

The LO1 and LO2 are signals that are flagged when the error status is detected. Both pins are open drain type, therefore to use the function properly, the LO1 and LO2 pins should be pulled up to the VCC. (Set the pull-up resistor in the range of 10 kΩ to 100 kΩ.) During normal operation, the pin is high-impedance (Internal MOSFET is turned off and the pin voltage is VCC). Once the error detect function (thermal shutdown (TSD), over current detection (ISD), or motor load open (OPD)) operates, the pins will output Low level (Internal MOSFET is turned ON) as follows.

Reasserting the VM power or using the standby mode to release the error detection status, the LO1 and LO2 pins will show “normal operation” status again. If function of LO1 or LO2 is not used, leave the pins open.

LO1	LO2	Function
VCC(Hi-Z)	VCC(Hi-Z)	Normal status (Normal operation)
VCC(Hi-Z)	Low	Detected motor load open (OPD)
Low	VCC(Hi-Z)	Detected over current (ISD)
Low	Low	Detected over thermal (TSD)



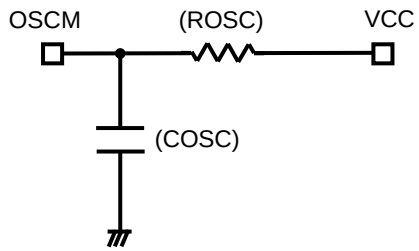
Once the error detection operates, internal MOSFETs of both or either LO1 or LO2 is turned on. (Pin voltage is low level.)

During normal status, internal MOSFETs of both LO1 and LO2 are OFF. (The pin will output High level (pull-up voltage of VCC).

The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

9. OSCM (internal oscillator) function

OSCM is used to set the internal oscillator frequency for constant current PWM control. The values of the resistor and the capacitor connected to this pin will set the OSCM frequency. Please connect the pull-up resistor to the VCC when PWM frequency is set by the external components. Also, to use an internal 'fixed value OSCM frequency' (not using any external components), disconnect the ROSC resistor and short the OSCM pin to the GND. Note that when using the internal 'fixed value OSCM frequency', do not input any control signal for 20 μs (typ.) after power on or standby release. (It takes 20 μs to judge the existence of the external components and switch to the 'fixed value OSCM frequency' mode.) The 'fixed value OSCM frequency' will be around 0.92 MHz, so the fchop will be around 57 kHz.



When using the internal 'fixed value OSCM frequency' (not using any external components), disconnect the ROSC resistor and short the COSC capacitor (short the OSCM pin to the GND).

Note: The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

Note: The oscillator frequency can be adjusted by controlling the values of resistor (ROSC) and capacitor (COSC). When conforming the frequency, it is recommended to fix the capacitor to 270 pF and change the ROSC value. For details, please refer to the following descriptions.

OSCM oscillator frequency (chopping frequency) calculation

OSCM oscillator frequency can be calculated by using the external component values (ROSC and COSC), and the formula is shown below. (COSC is fixed to 270 pF.)

$$fOSCM = 4.0 \times ROSC^{(-0.8)}$$

COSC and ROSC are external components to set the oscillator frequency. When adjusting the oscillator frequency with components, it is recommended to fix COSC to 270 pF and change the constant number of ROSC.

Moreover, the relation between the chopping frequency for constant current PWM (fchop) and the OSCM oscillator frequency (fOSCM) is as follows;

$$fchop = fOSCM / 16$$

For normal operation, setting the frequency in the range of 50 kHz to 70 kHz and adjusting suitably as needed is recommended

When the chopping frequency is set high, the current ripple will be smaller, which will lead to a higher reproducibility of a waveform. However, the chopping frequency per unit time is increased and so the gate loss and the switching loss of the integrated MOSFET will be larger, which will lead to an additional heat generation. On the other hand, when the chopping frequency is set low, the current ripple will be larger but the heat generation is reduced. Please set the frequency according to the usage conditions and environment.

♦ Stepping motor application features (anti-stall, sense resistor less PWM)

10. Active Gain Control (Anti-stall) function

AGC0, AGC1 pins control the Active Gain Control to turn on or off. When both pins are set to High, the AGC is turned on. The PWM current threshold will be reduced in a phased manner where the upper limited current is determined by VREF. When both pins are set to Low, the AGC is turned off and the current, which is set by VREF, flows.
Note: Built-in digital filter of 0.625 μs (±20 %) is adopted to AGC0 and AGC1 pins.

AGC0	AGC1	Function
High	High	AGC: ON
High	Low	(Note 1)
Low	Low	AGC: OFF

Normally, set these pins as follows; AGC0, AGC1= (High, High) or (Low, Low). Please do not switch the AGC0 pin level during operation.
Note 1: Use this configuration when switching ON or OFF of AGC during operation. As for concrete usage method, refer to the application note.

11. CLIM (AGC bottom current limit) function

The CLIM0 and CLIM1 pins set the bottom current limit of the AGC. When AGC is active, the PWM current threshold will be reduced in a phased manner. By using the CLIM function, the motor current will not go below the bottom limit. The CLIM0 is a 2 stated logic input, and the CLIM1 is a 4 stated logic input.
Note: Built-in digital filter of 0.625 μs (±20 %) is adopted to CLIM0 and CLIM1 pins.

CLIM0	CLIM1	Function
High	VCC short	AGC bottom current limit: IOUT x 80 %
	VCC-100 kΩ pull-up	AGC bottom current limit: IOUT x 75 %
	GND-100 kΩ pull-down	AGC bottom current limit: IOUT x 70 %
	GND short	AGC bottom current limit: IOUT x 65 %
Low	VCC short	AGC bottom current limit: IOUT x 60 %
	VCC-100 kΩ pull-up	AGC bottom current limit: IOUT x 55 %
	GND-100 kΩ pull-down	AGC bottom current limit: IOUT x 50 %
	GND short	AGC bottom current limit: IOUT x 45 %

Note: Resistance accuracy should be within ±20 %.

12. BOOST (current boost) function

The BOOST pin sets the current boost level when the load torque is increased. When AGC is turned on, the PWM current threshold will be reduced in a phased manner. However, once the load torque is increased, the device will then boost the PWM current threshold to prevent the motor from stalling. The BOOST pin is a 4 stated logic input pin.
Note: Built-in digital filter of 0.625 μs (±20 %) is adopted to BOOST pin.

BOOST	Function
VCC short	Takes 5 steps maximum to reach 100 % current (design value)
VCC-100 kΩ pull-up	Takes 7 steps maximum to reach 100 % current (design value)
GND-100 kΩ pull-down	Takes 9 steps maximum to reach 100 % current (design value)
GND short	Takes 11 steps maximum to reach 100 % current (design value)

Note: Resistance accuracy should be within ±20 %.
Note: Current boost step is largest when BOOST is shorted to VCC, and smallest when shorted to the GND.

13. FLIM (AGC Frequency limit) function

The FLIM pin sets the bottom frequency limit for the AGC to be active. It can reduce the resonance frequency of the motor start in using AGC. The FLIM pin is a 4 stated logic input.
Note: Built-in digital filter of 0.625 μs (±20%) is adopted to FLIM pin.

FLIM	Function
VCC short	Frequency limit: ON, AGC is invalid when fCLK is below 675 Hz
VCC-100 kΩ pull-up	Frequency limit: ON, AGC is invalid when fCLK is below 450 Hz
GND-100 kΩ pull-down	Frequency limit: ON, AGC is invalid when fCLK is below 225 Hz
GND short	FLIM: OFF

Note: Resistance accuracy should be within ±20 %.

The frequency in the below table is in the case of full step resolution. Frequency limit threshold depends on the step resolution setting.

FLIM	1/1	1/2 (a)	1/2 (b)	1/4	1/8	1/16	1/32
VCC short	675 Hz	1.35 kHz	1.35 kHz	2.7 kHz	5.4 kHz	10.8 kHz	21.6 kHz
VCC-100 kΩ pull-up	450 Hz	900 Hz	900 Hz	1.8 kHz	3.6 kHz	7.2 kHz	14.4 kHz
GND-100 kΩ pull-down	225 Hz	450 Hz	450 Hz	900 Hz	1.8 kHz	3.6 kHz	7.2 kHz
GND short	FLIM: OFF						

Note: Resistance accuracy should be within ±20 %.

14. LTH (AGC detection threshold) function

The LTH pin sets the AGC detection threshold. Connect a 100 kΩ pull-down resistor to GND.

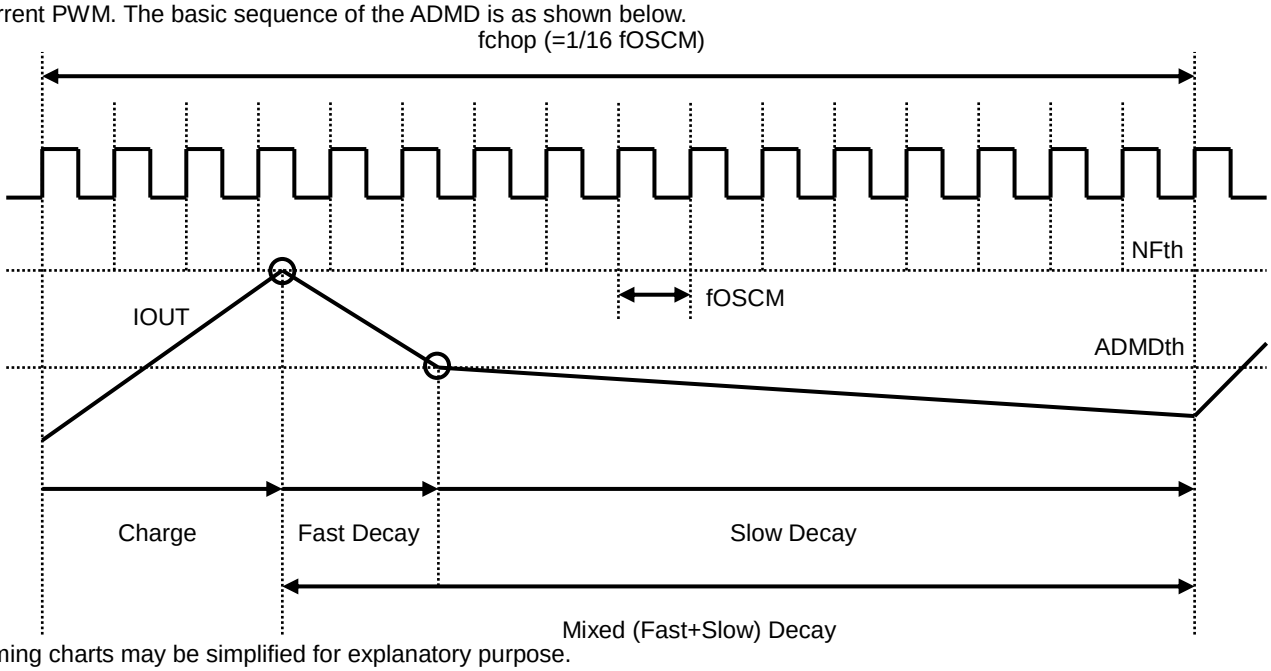
LTH	Function
GND-100 kΩ pull-down	Standard configuration for AGC detection threshold

Note: Resistance accuracy should be within ±20 %.

15. ADMD+ACDS (sense-resistor less PWM) control

ADMD (Advanced Dynamic Mixed Decay)

The TB67S285FTG applied the ADMD architecture which monitors both charge and recirculating current during constant current PWM. The basic sequence of the ADMD is as shown below.

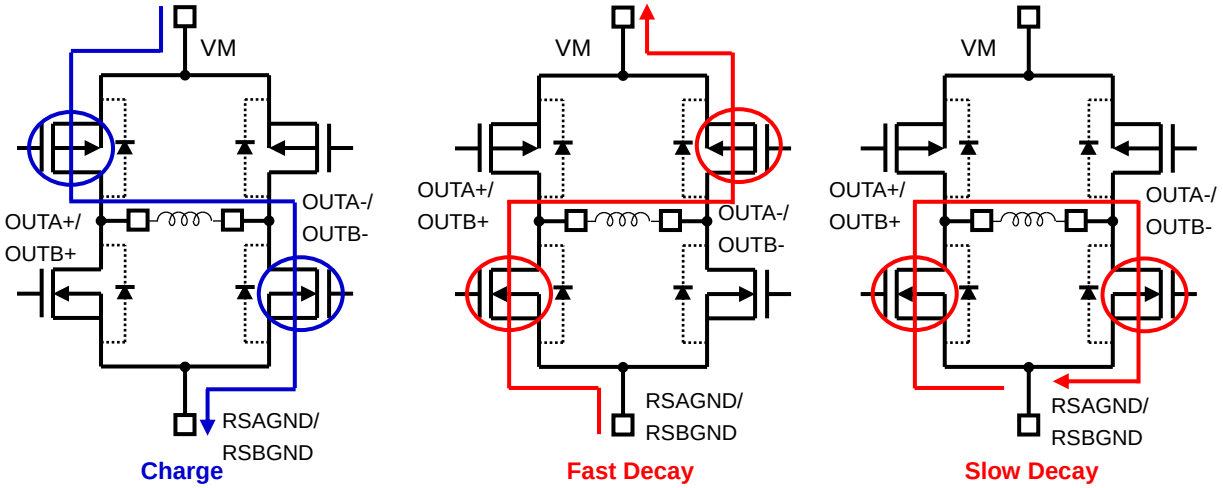


Timing charts may be simplified for explanatory purpose.

The basic constant current PWM sequence is a loop of Charge→Fast Decay→Slow Decay→Charge→･･･ to keep the peak current below the threshold. The chopping frequency (fchop) is a period of 16 counts per cycle of OSCM oscillator frequency (fOSCM). The sequence of Charge, Fast Decay, and Slow Decay is switched within this fchop cycle.

First, the motor current is charged (Charge sequence) until it reaches the constant current threshold (NFth), which is set by the VREF reference voltage. Once the motor current reaches the constant current threshold (NFth), a partial motor current recirculates back to the power supply (Fast Decay sequence). When the motor current reaches the fixed value (ADMDth) during recirculation; for the rest of the fchop cycle, the motor is controlled to naturally discharge and hold the motor current as much as possible (Slow Decay sequence).

Motor output MOSFET operation mode (Advanced Dynamic Mixed Decay)



Note: Fixed value of 400 ns (design value) is prepared at the switching timing of MOSFET output to avoid any flow-through current. The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

Constant current threshold calculation

The constant current PWM threshold can be set by applying voltage to the VREF pin and adjusting TRQ function.

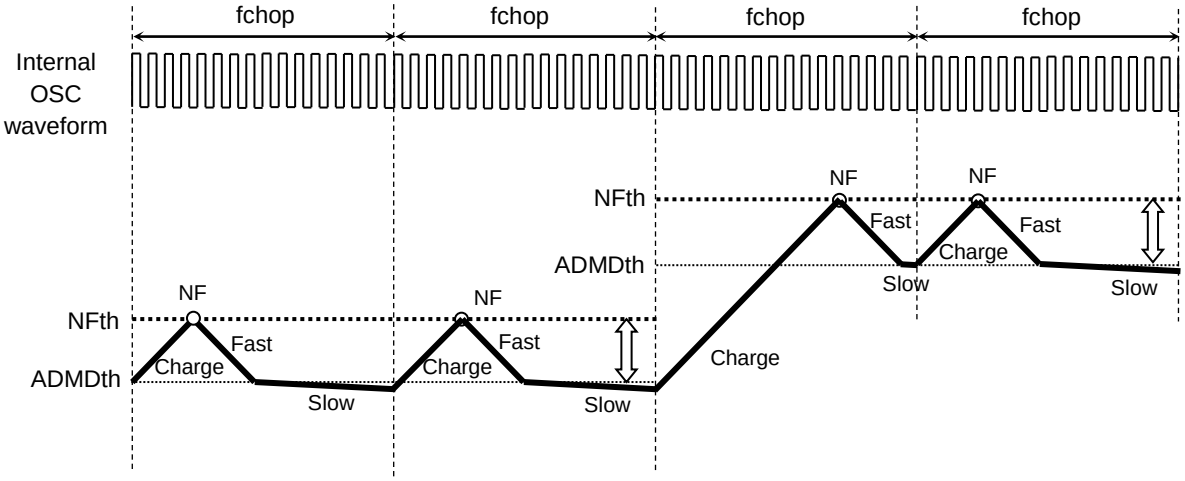
IOUT=VREF × 0.833 × TRQ setting

Example: When Current ratio is 100 %, VREF voltage is 2.0 V, and TRQ setting is 100%, the constant current PWM threshold is calculated from following formula.

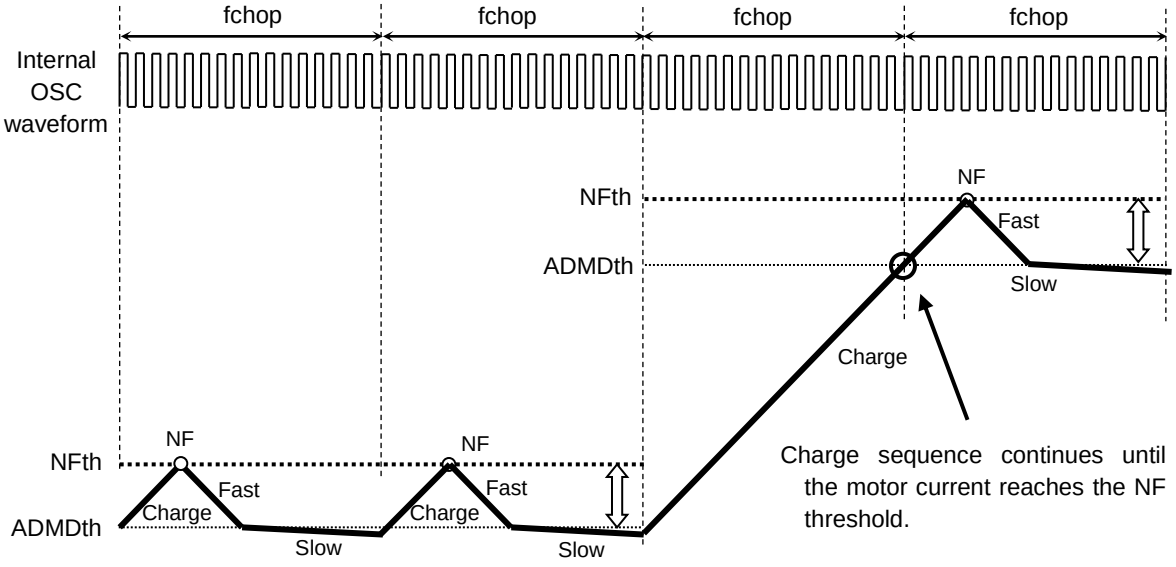
IOUT = 2.0 × 0.833 × 1 = 1.67 A

ADMD current waveform

・When the next current step/ratio is higher than the previous step

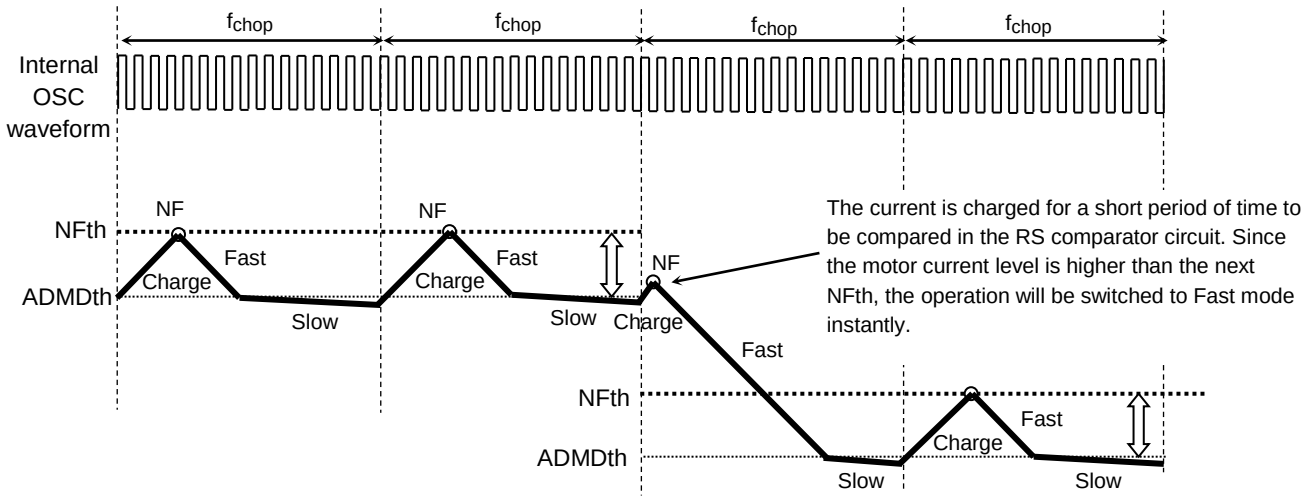


・When the Charge period continues beyond 1 fchop cycle

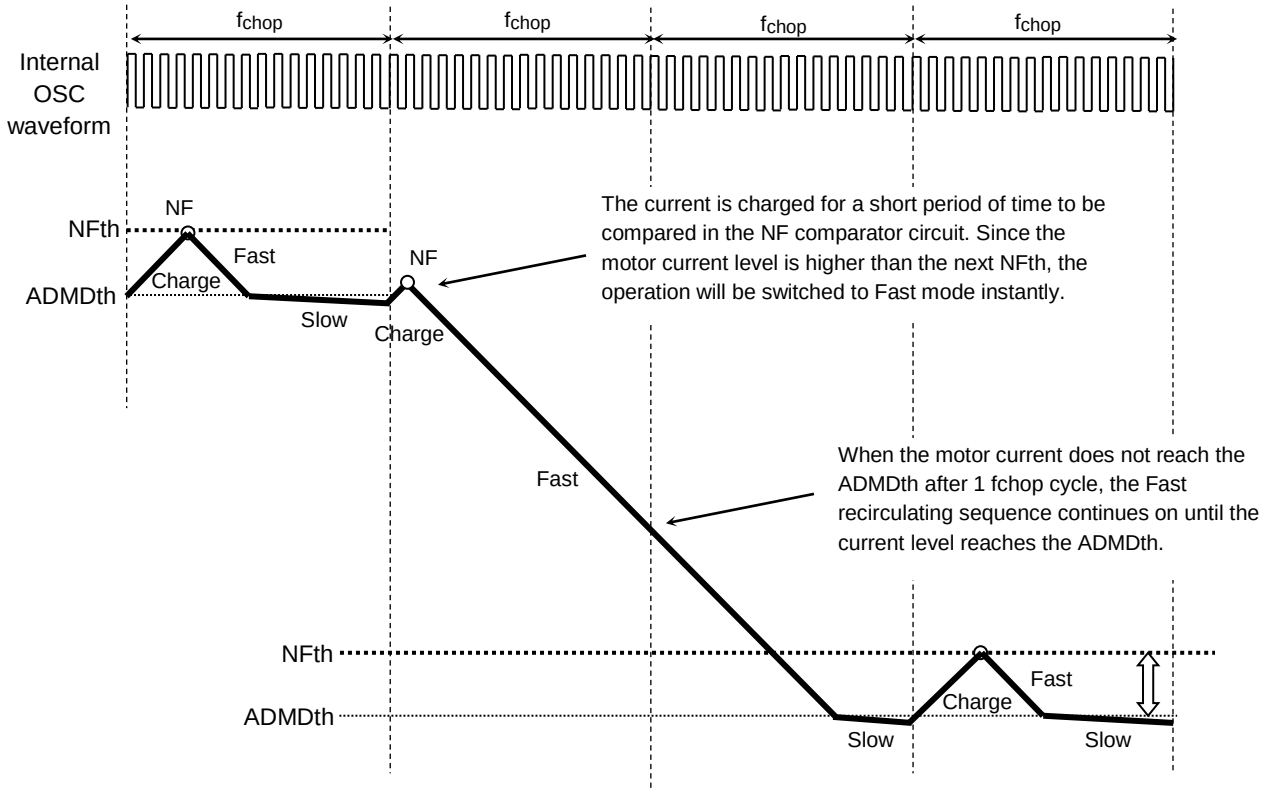


Timing charts may be simplified for explanatory purpose.

・When the next current step/ratio is lower than the previous step



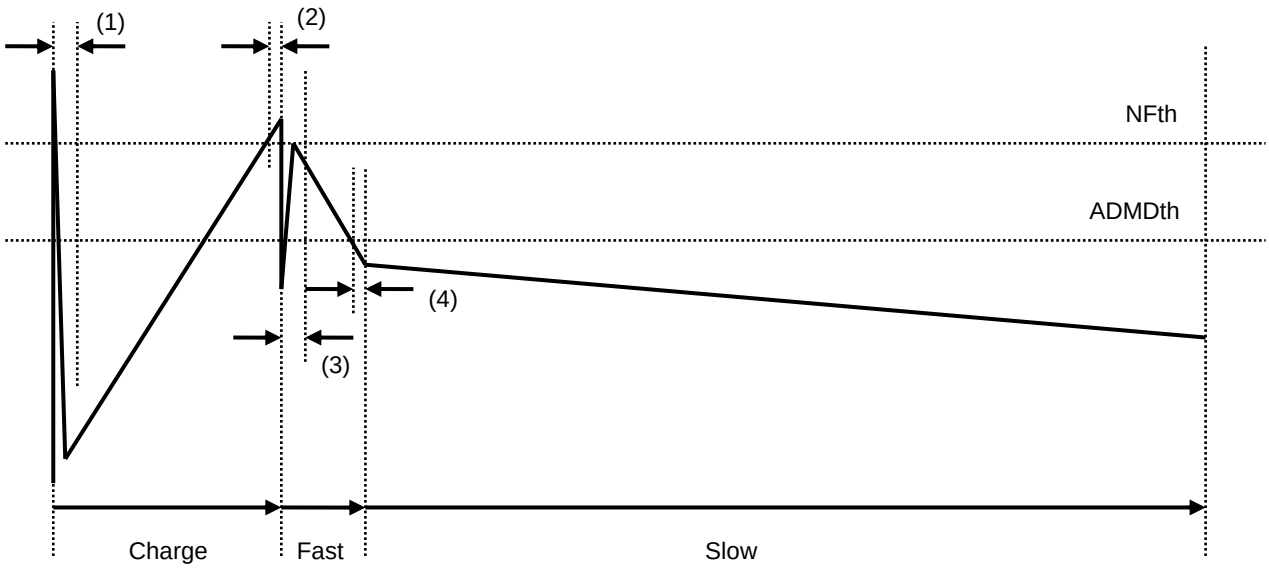
・When the Fast period continues beyond 1 fchop cycle (Current does not reach ADMDth within 1 fchop cycle.)



Timing charts may be simplified for explanatory purpose.

Constant current PWM blank/mask time

The TB67S285FTG has multi filter time to reject incoming noise or spike (inrush) current, which is generated during motor operation, to avoid miss detection.



Timing charts may be simplified for explanatory purpose.

(1) Digital NFblank (Filtering time to avoid spike current, which is generated before Charge): 1.25 μs (typ.)
(2) Analog NFblank (Filtering time to avoid pulse noise for NFth): 0.35 μs (typ.)
(3) Digital ADMDblank (Filtering time to avoid spike current, which is generated between Charge and Decay for ADMDth: 2.2 μs (typ.)
(4) Analog ADMDblank (Filtering time to avoid pule noise for ADMDth): 0.35 μs (typ.)

Note: Above periods are design values. They are not guaranteed.

Absolute maximum ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	VM	50	V	—
Motor output voltage	VOUT	50	V	—
Motor output current	IOUT	3.0	A	(Note 1)
Internal Logic power supply	VCC	6.0	V	—
Logic input voltage	VIN(H)	6.0	V	—
	VIN(L)	-0.4	V	—
LO output voltage	VLO	6.0	V	—
LO Inflow current	ILO	6.0	mA	—
Power dissipation	PD	1.3	W	(Note 2)
Operating temperature	Topr	-20 to 85	°C	—
Storage temperature	Tstg	-55 to 150	°C	—
Junction temperature	Tj(max)	150	°C	—

Note 1: For normal usage, the maximum current value should be determined by heat calculation.
The maximum output current may be further limited depending on ambient temperature and board conditions (heat conditions).
Note 2: Device alone (Ta =25°C)

Ta: Ambient temperature
Topr: Ambient temperature while the IC is active
Tj: Junction temperature while the IC is active. Tj (max) is limited by the thermal shutdown (TSD) threshold.
Please set the usage conditions so that the peak Tj is kept under 120°C for indication.

Caution) Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. All voltage ratings, including supply voltages, must always be followed. Other notes and considerations described in the datasheet should also be referred to.

Operation ranges (Ta=-20 to 85°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	VM	10	24	47	V	—
Motor output current	IOUT	—	1.5	3.0	A	(Note 1)
LO output pin voltage	VLO	—	3.3	VCC	V	Pull-up voltage
Serial clock input frequency	fCLOCK	—	—	1000	kHz	(Note 2)
Chopping frequency	fchop(range)	40	70	150	kHz	—
VREF input voltage	VREF	GND	2.0	3.6	V	—

Note 1: The actual maximum current may be limited due to operating circumstances (operating conditions of step resolution, continuous operation time, etc. and thermal conditions of ambient temperature, PCB layout, etc.)

Note 2: The actual maximum frequency may be limited due to operating circumstances (operating conditions of step resolution, continuous operation time, etc. and thermal conditions of ambient temperature, PCB layout, etc.)

Electrical characteristics 1 (Ta = 25°C and VM = 24 V, unless otherwise specified)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage 1 (Except BOOST, CLIM1, and FLIM)		VIN1(H)	High level	3.0	—	5.5	V
		VIN1(L)	Low level	0	—	2.0	V
Logic input hysteresis voltage		VIN(HYS)	Hysteresis voltage	0.2	—	0.4	V
Logic input voltage 2 (BOOST, CLIM1, and FLIM)		VIN2(H)	VCC short	4.2	—	VCC	V
		VIN2(PU)	VCC-100 kΩ pull-up	2.8	—	3.55	V
		VIN2(PD)	GND-100 kΩ pull-down	1.45	—	2.2	V
		VIN2(L)	GND short	0	—	0.8	V
Logic input current 1 (Except BOOST, CLIM1, and FLIM)		IIN1(H)	Input voltage =3.3 V	—	33	—	μA
		IIN1(L)	Input voltage =0 V	—	—	1	μA
Serial output voltage (COUT,DOUT, and LOUT)		VOS(H)	IOH=-5 mA, VCC (reference voltage)	-0.2	-0.15	-0.1	V
		VOS(L)	IOL=5 mA, GND (reference voltage)	0.1	0.15	0.2	V
LO output pin voltage		VOL(LO)	IOL=5 mA LO=Low	—	0.2	0.5	V
Current consumption		IM1	Standby mode	—	2	—	mA
		IM2	OUT: OPEN, ENABLE: Low, Standby mode: Release	3	5	7	mA
		IM3	OUT: OPEN, ENABLE: High, Standby mode: Release	4	6	8	mA
Output leakage current	High-side	IOH	VM=50 V, VOUT=0 V	—	—	1	μA
	Low-side	IOL	VM=VOUT=50 V	1	—	—	μA
Motor current channel differential		ΔIout1	Current differential between channels	-5	0	5	%
Motor current setting differential		ΔIout2	IOUT=1.5 A	-5	0	5	%
Motor output ON-resistance (High-side + Low-side)		Ron(H+L)	Tj=25°C, Forward direction (High + Low side)	—	0.4	0.5	Ω

Note: VIN (H) is defined as the VIN voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when a pin under test is gradually raised from 0 V. VIN (L) is defined as the VIN voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when the pin is then gradually lowered. The difference between VIN (H) and VIN (L) is defined as the VIN (HYS).

Electrical characteristics 2 (Ta = 25°C and VM = 24 V, unless otherwise specified)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
VREF input current	IREF	VREF=2.0 V	—	0	1	μA
VCC voltage	VCC	ICC=5.0 mA	4.75	5.0	5.25	V
VCC current	ICC	VCC=5.0 V	—	2.5	5.0	mA
VREF gain	VREF(gain)	VREF=2.0 V	—	0.833	—	A/V
Thermal shutdown (TSD) threshold (Note 1)	T_jTSD	—	145	160	175	°C
VM power-on-reset threshold	VMPOR(H)	POR release	6.5	7.5	8.5	V
	VMPOR(L)	POR detect	6.0	7.0	8.0	V
Over current detection (ISD) threshold (Note 2)	ISD	—	3.3	4.3	5.5	A

Note 1: Thermal shutdown (TSD)

When the IC detects an over temperature, the internal circuit turns off the output MOSFETs. It has a dead band time to avoid TSD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode by STANDBY pin to release this function. The TSD is triggered when the device is over heated irregularly. Make sure not to use the TSD function aggressively.

Note 2: Over current detection (ISD)

When the IC detects an over current, the internal circuits turns off the output MOSFETs. It has a dead band time to avoid ISD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode by STANDBY pin to release this function. The ISD is triggered when the motor current is over rated irregularly. Make sure not to use the ISD function aggressively.

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB67S285FTG or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

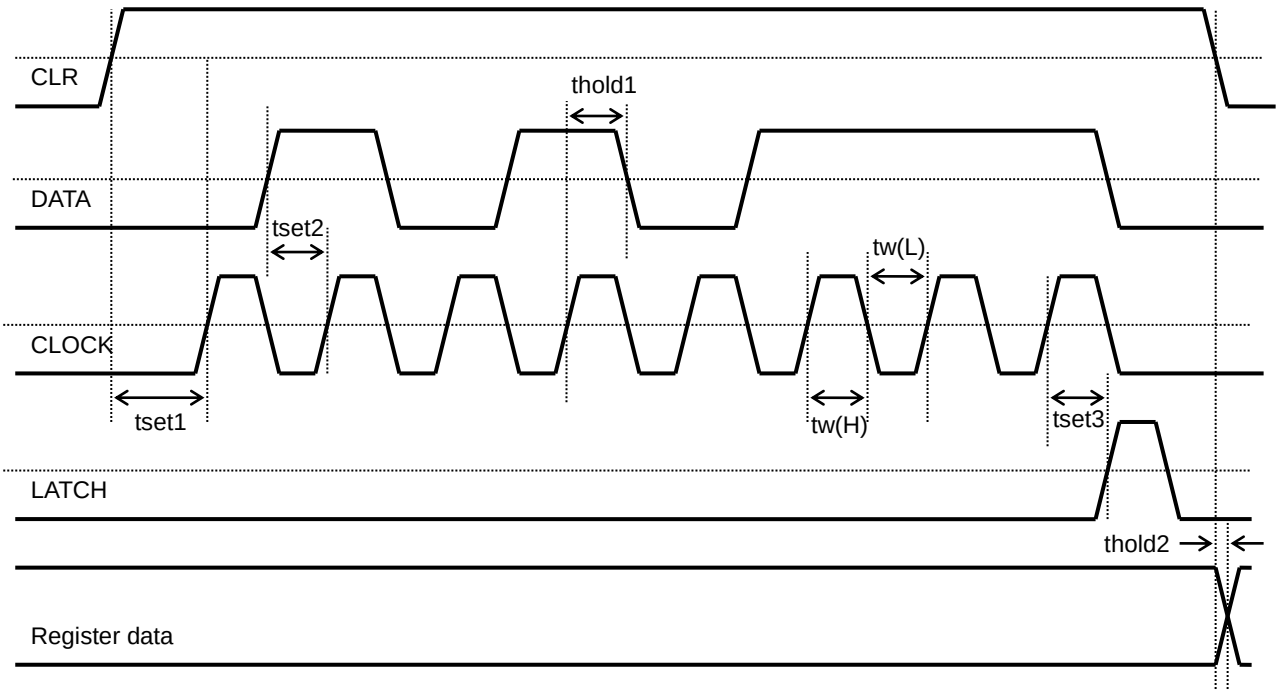
IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

AC electrical characteristics (Ta = 25°C and VM = 24 V, unless otherwise specified)

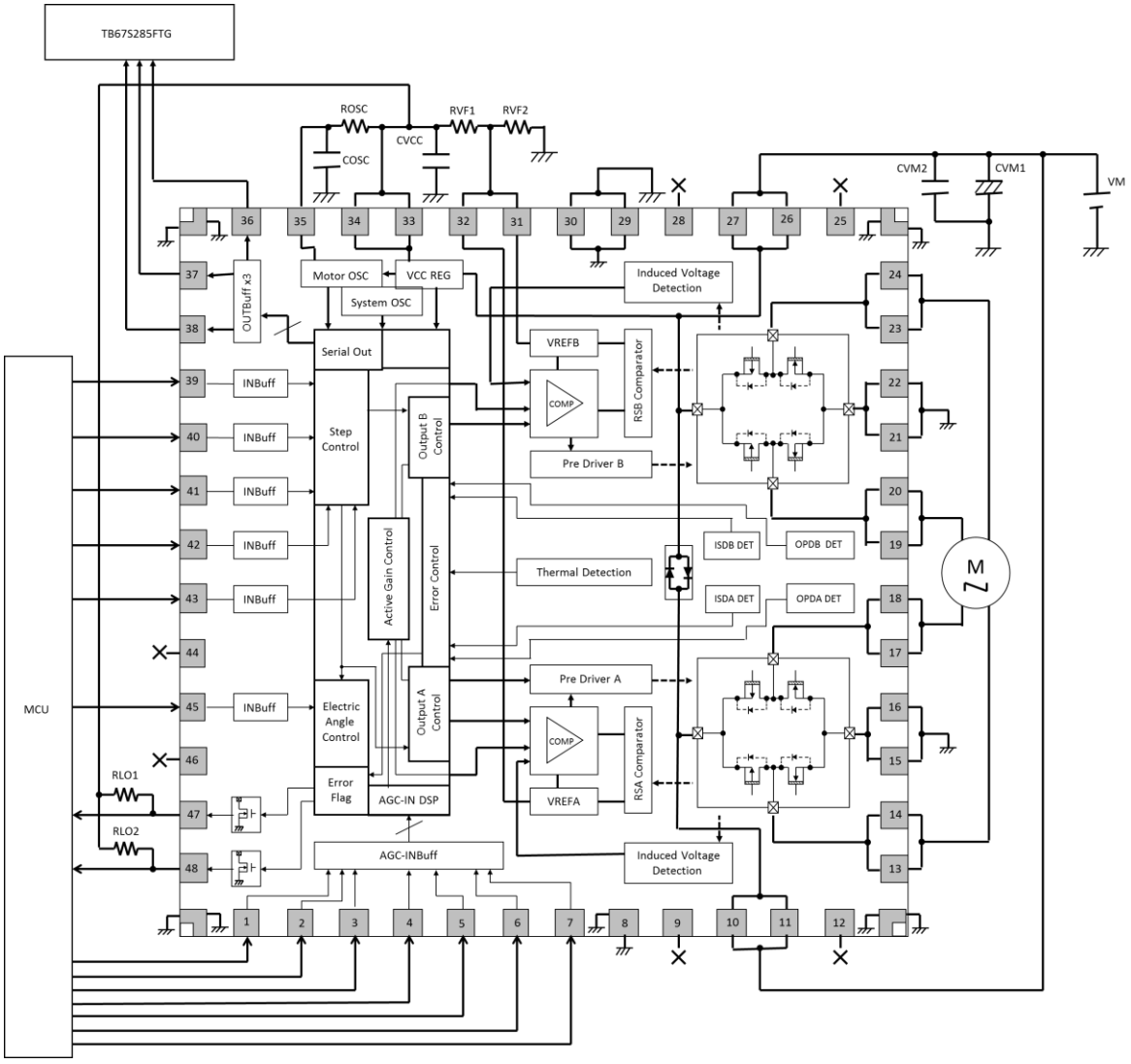
Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Minimum serial input 'High' pulse width	tw(H)	DATA,CLOCK, and LATCH signals	500	—	—	ns
Minimum serial input 'Low' pulse width	tw(L)	DATA,CLOCK, and LATCH signals	500	—	—	ns
Minimum serial input setup time	tset1	CLR to CLOCK	50	—	—	ns
	tset2	DATA to CLOCK	50	—	—	ns
	tset3	CLOCK to LATCH	50	—	—	ns
Minimum serial input hold time	thold1	CLOCK to DATA	50	—	—	ns
	thold2	CLR to serial register data	50	—	—	ns
Output MOSFET switching specifications	tr	—	30	80	130	ns
	tf	—	40	90	140	ns
OSCM oscillator accuracy	ΔfOSCM1	COSC=270 pF, ROSC=5.1 kΩ	-15	—	+15	%
	ΔfOSCM2	COSC: GND short, ROSC: Open	-20	—	+20	%
PWM chopping frequency	fchop1	COSC=270 pF, ROSC=5.1 kΩ	—	67	—	kHz
	fchop2	COSC: GND short, ROSC: Open	—	57	—	kHz

AC characteristics timing chart



The timing chart may be simplified for explanatory purpose.

Application circuit example



The application circuit shown in this document is provided for reference purposes only. The data for mass production are not guaranteed.

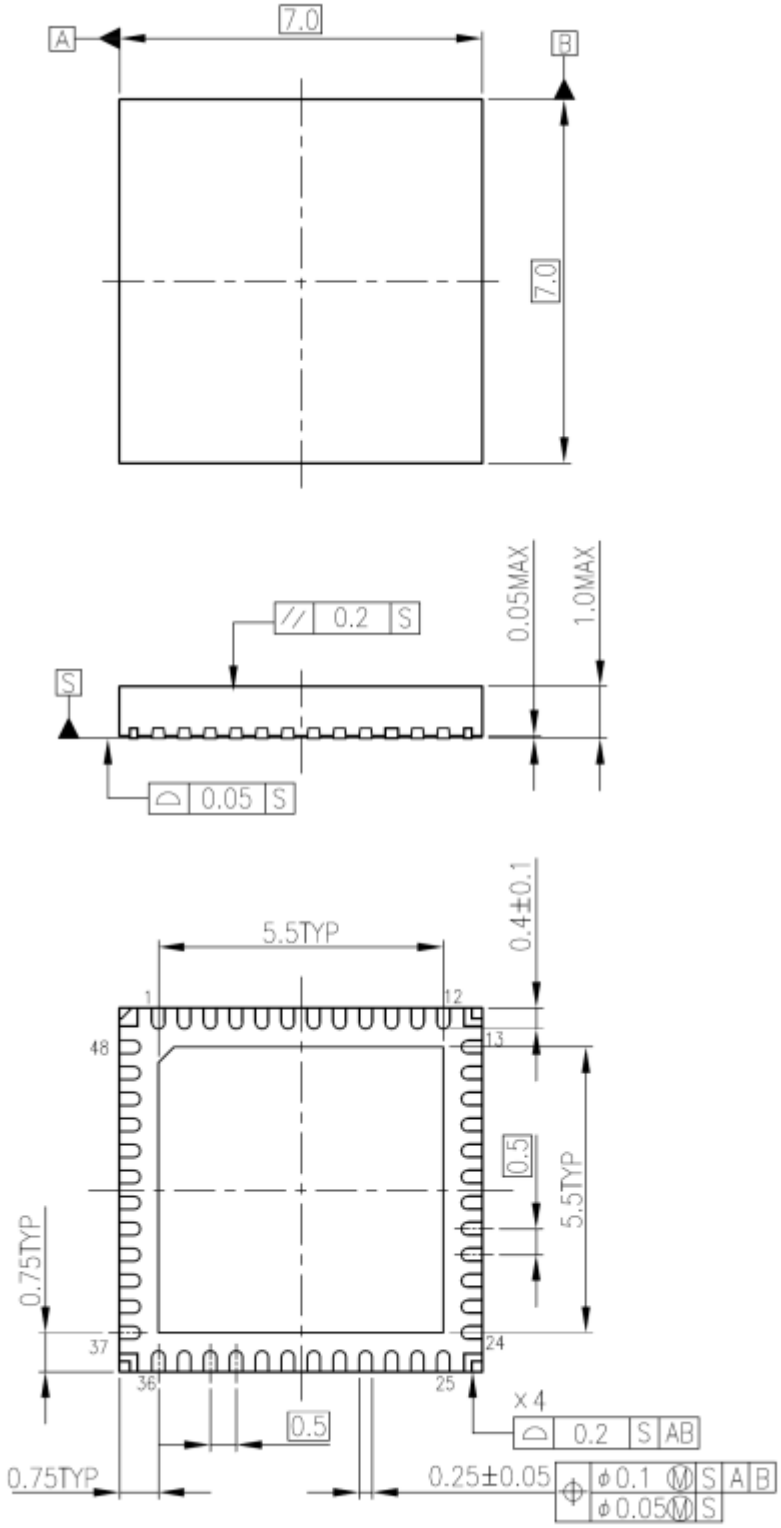
Constant numbers of components (for reference only)

Symbol	Component	Reference constant number
CVM1	Electrolytic capacitor	100 μF (CVM1 ≥ 10 μF)
CVM2	Ceramic capacitor	(0.1 μF)
RVF1,RVF2	Resistor	Arbitrary (10 kΩ ≤ RVF1+RVF2 ≤ 50 kΩ)
CVCC	Ceramic capacitor	0.1 μF
ROSC	Resistor	5.1 kΩ (1.8 kΩ to 8.2 kΩ)
COSC	Ceramic capacitor	270 pF
RLO1,RLO2	Resistor	10 kΩ (10 kΩ to 100 kΩ)

Constant numbers in above table are for reference only. Some components outside of the recommendation range can be adopted depending on the usage conditions.

Package dimensions (Unit: mm)

P-VQFN48-0707-0.50-004



Weight: 0.14 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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