

TPN11003NL

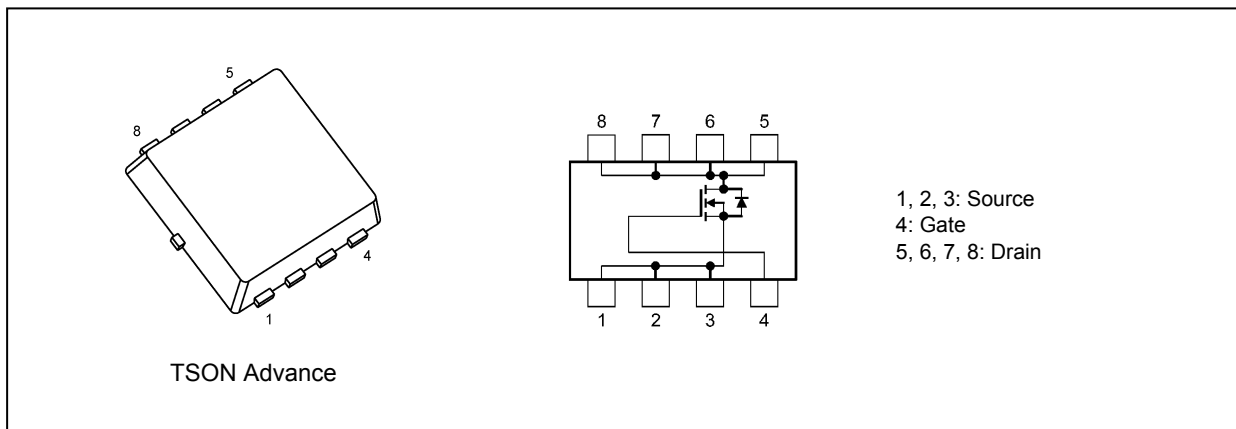
1. Applications

- Switching Voltage Regulators
- DC-DC Converters

2. Features

- (1) High-speed switching
- (2) Small gate charge: $Q_{SW} = 2.0 \text{ nC (typ.)}$
- (3) Low drain-source on-resistance: $R_{DS(ON)} = 12.6 \text{ m}\Omega \text{ (typ.)}$ ($V_{GS} = 4.5 \text{ V}$)
- (4) Low leakage current: $I_{DSS} = 10 \text{ }\mu\text{A (max)}$ ($V_{DS} = 30 \text{ V}$)
- (5) Enhancement mode: $V_{th} = 1.3 \text{ to } 2.3 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 0.1 \text{ mA}$)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25 \text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	30	V	
Gate-source voltage	V_{GSS}	± 20		
Drain current (DC)	(Silicon limit) (Note 1), (Note 2)	I_D	31	A
Drain current (DC)	($T_c = 25 \text{ }^\circ\text{C}$) (Note 1)	I_D	11	
Drain current (pulsed)	($t = 1 \text{ ms}$) (Note 1)	I_{DP}	62	
Power dissipation	($T_c = 25 \text{ }^\circ\text{C}$)	P_D	19	W
Power dissipation	($t = 10 \text{ s}$) (Note 3)	P_D	1.9	
Power dissipation	($t = 10 \text{ s}$) (Note 4)	P_D	0.7	
Single-pulse avalanche energy	(Note 5)	E_{AS}	26	mJ
Avalanche current		I_{AR}	11	A
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2013-06

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance (T _c = 25 °C)	R _{th(ch-c)}	6.57	°C/W
Channel-to-ambient thermal resistance (t = 10 s) (Note 3)	R _{th(ch-a)}	65.7	
Channel-to-ambient thermal resistance (t = 10 s) (Note 4)	R _{th(ch-a)}	178	

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Limited by silicon chip capability.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_{DD} = 24 V, T_{ch} = 25 °C (initial), L = 170 μH, I_{AR} = 11 A



Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)



Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

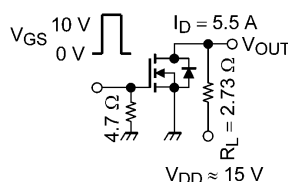
6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 0.1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	15	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}, I_D = 0.1\text{ mA}$	1.3	—	2.3	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	—	12.6	16	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$	—	9.4	11	

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	510	660	pF
Reverse transfer capacitance	C_{rss}		—	18	50	
Output capacitance	C_{oss}		—	300	—	
Gate resistance	r_g	—	—	1.3	2.0	Ω
Switching time (rise time)	t_r	See Fig. 6.2.1	—	2.1	—	ns
Switching time (turn-on time)	t_{on}		—	7.5	—	
Switching time (fall time)	t_f		—	1.9	—	
Switching time (turn-off time)	t_{off}		—	14	—	



Duty $\leq 1\%$, $t_w = 10\text{ }\mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit

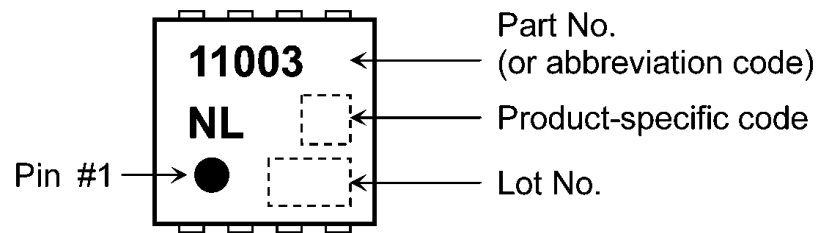
6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 11\text{ A}$	—	7.5	—	nC
		$V_{DD} \approx 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 11\text{ A}$	—	3.3	—	
Gate-source charge 1	Q_{gs1}	$V_{DD} \approx 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 11\text{ A}$	—	2.0	—	
Gate-drain charge	Q_{gd}		—	1.0	—	
Gate switch charge	Q_{sw}		—	2.0	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed)	(Note 6) I_{DRP}	—	—	—	62	A
Diode forward voltage	V_{DSF}	$I_{DR} = 11\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V

Note 6: Ensure that the channel temperature does not exceed $150\text{ }^\circ\text{C}$.

7. Marking**Fig. 7.1 Marking**

8. Characteristics Curves (Note)

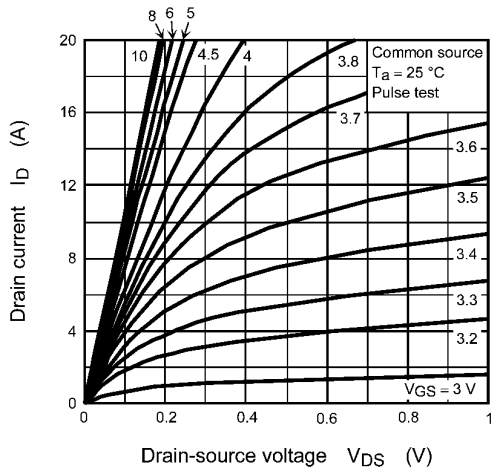


Fig. 8.1 ID - VDS

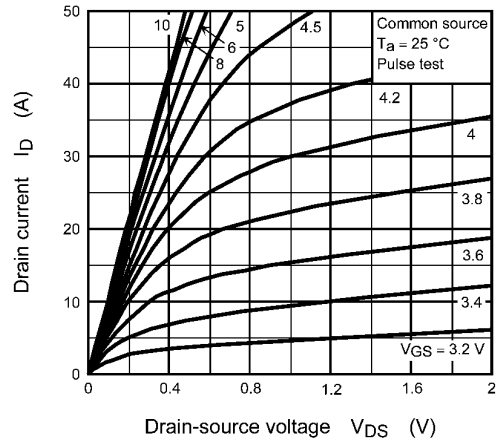


Fig. 8.2 ID - VDS

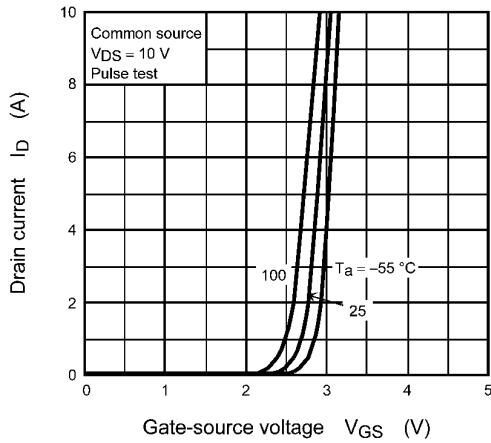


Fig. 8.3 ID - VGS

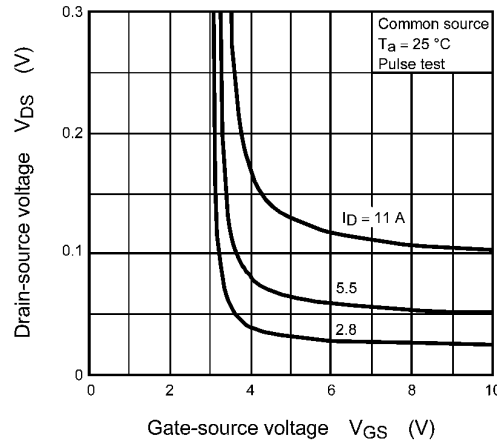


Fig. 8.4 VDS - VGS

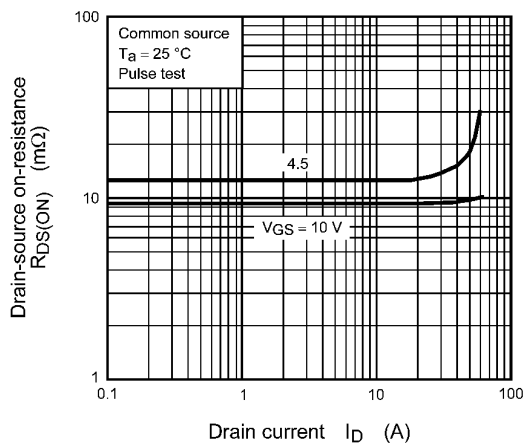


Fig. 8.5 RDS(ON) - ID

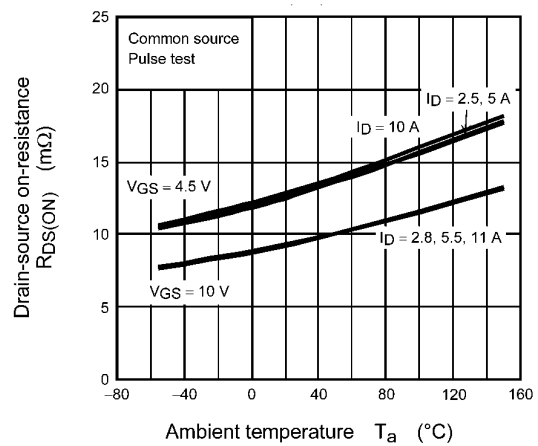


Fig. 8.6 RDS(ON) - Ta

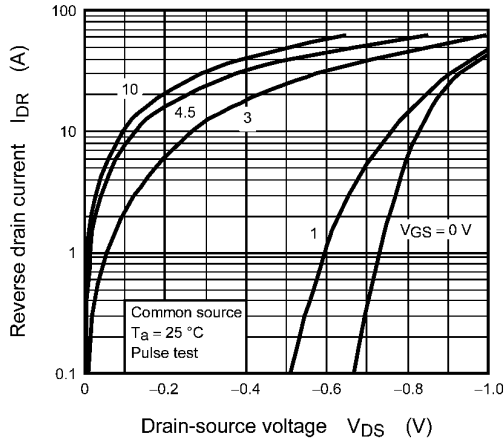


Fig. 8.7 $I_{DR} - V_{DS}$

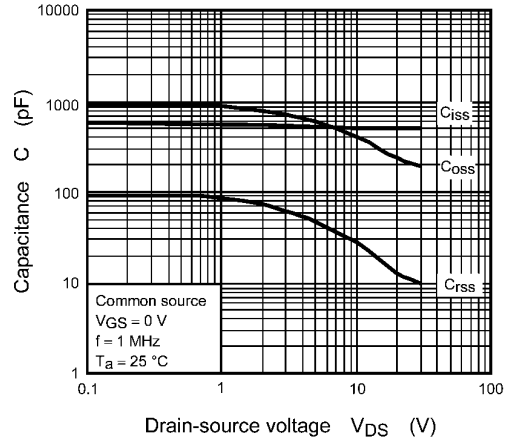


Fig. 8.8 Capacitance - V_{DS}

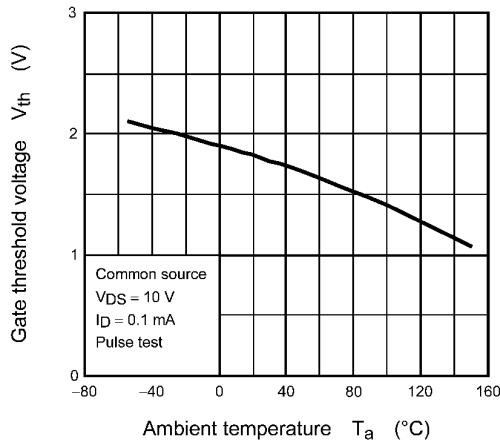


Fig. 8.9 $V_{th} - T_a$

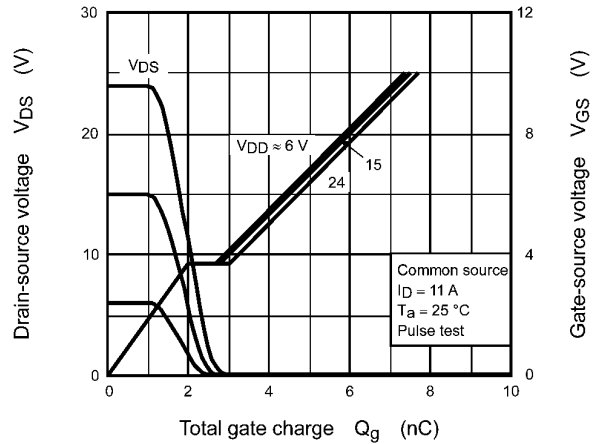
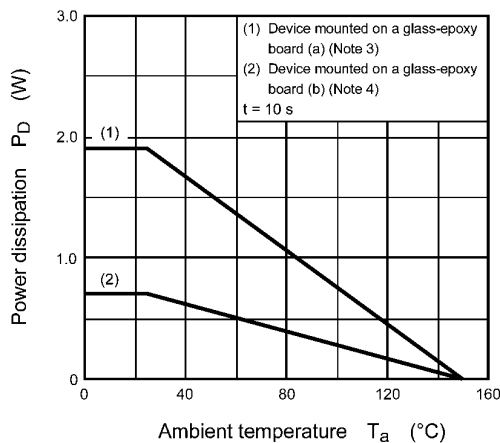
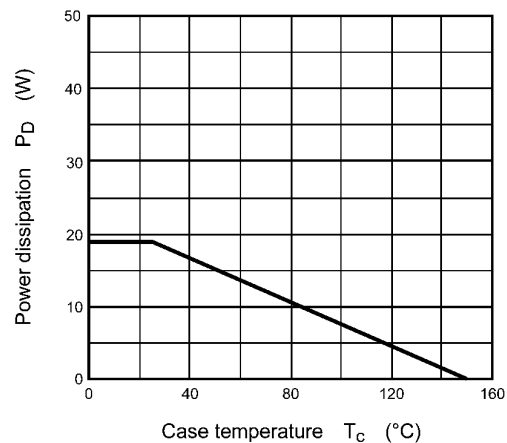


Fig. 8.10 Dynamic Input/Output Characteristics



**Fig. 8.11 $P_D - T_a$
(Guaranteed Maximum)**



**Fig. 8.12 $P_D - T_c$
(Guaranteed Maximum)**

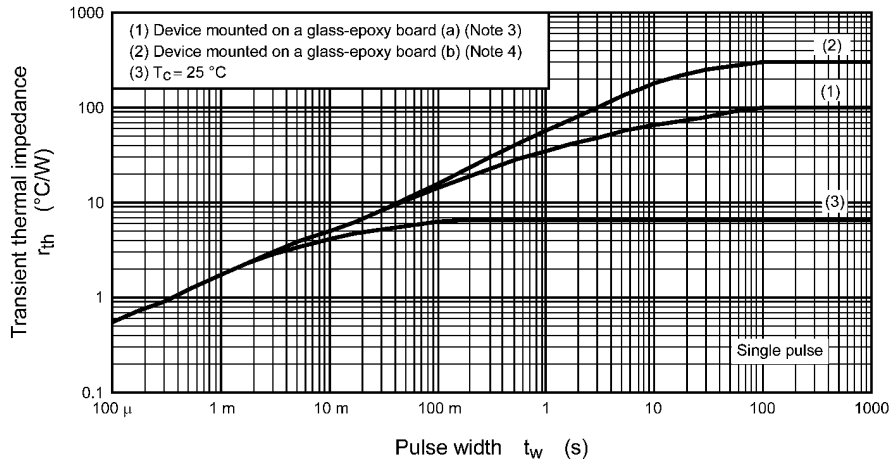


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

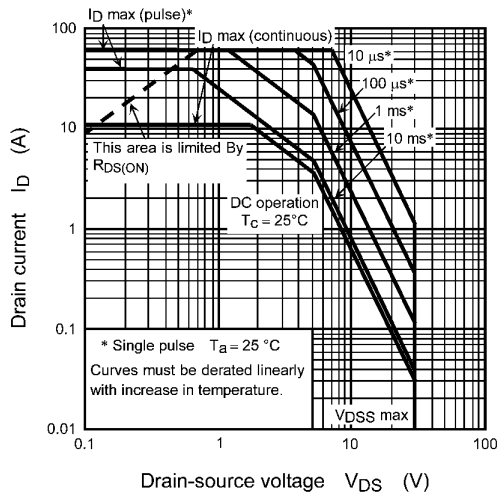


Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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