Unit: mm

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N44FE

High Speed Switching Applications Analog Switching Applications

Compact package suitable for high-density mounting

 $R_{DS(ON)} = 4.0 \Omega \text{ (max) (@V}_{GS} = 4 \text{ V)}$ $R_{DS(ON)} = 7.0 \Omega \text{ (max) (@V}_{GS} = 2.5 \text{ V)}$ Low ON-resistance

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	30	V	
Gate-Source voltage		V _{GSS}	±20	V	
Drain current	DC	I _D	100	mA	
	Pulse	I _{DP}	200		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the

absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

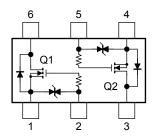
Note 1: Total rating, mounted on FR4 board $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 0.135 \text{ mm}^2 \times 6)$

1.6±0.05 1.2±0.05 $.6\pm0.05$ 1.0±0.05 12±0. 1.Source1 4.Source2 2.Gate1 5.Gate2 3.Drain2 6.Drain1 ES₆ **JEDEC** JEITA **TOSHIBA** 2-2N1D

Weight: 3 mg (typ.)

Marking

Equivalent Circuit (top view)



Handling Precaution

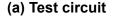
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

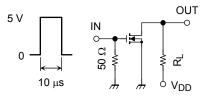
> Start of commercial production 2009-04

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage current		I _{GSS}	$V_{GS} = \pm 14 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА	
Drain-Source breakdown voltage		V (BR) DSS	I _D = 0.1 mA, V _{GS} = 0 V	30	_	_	V	
Drain cut-off current		I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	_	_	1	μΑ	
Gate threshold voltage	e	V _{th}	V _{DS} = 3 V, I _D = 0.1 mA	0.8	_	1.5	V	
Forward transfer admi	ttance	Y _{fs}	V _{DS} = 3 V, I _D = 10 mA	25	_	_	mS	
Drain-Source ON resistance		R _{DS (ON)}	I _D = 10 mA, V _{GS} = 4 V	_	2.2	4.0		
			I _D = 10 mA, V _{GS} = 2.5 V	_	4.0	7.0	Ω	
Input capacitance		C _{iss}	V _{DS} = 3 V, V _{GS} = 0 V, f = 1 MHz	_	8.5	_	pF	
Reverse transfer capacitance		C _{rss}		_	5.3	_		
Output capacitance		Coss			9.4	_		
Switching time	Turn-on time	t _{on}	$V_{DD} = 5 \text{ V}, I_D = 10 \text{ mA},$ $V_{GS} = 0 \text{ to } 5 \text{ V}$	_	50	_	ns	
	Turn-off time	t _{off}		_	200	_		

Switching Time Test Circuit

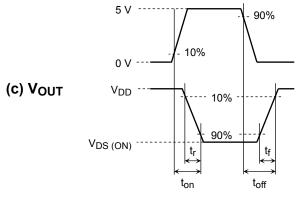




 $\begin{aligned} & \text{V}_{DD} = 5 \text{ V} \\ & \text{Duty} \leq 1\% \\ & \text{V}_{\text{IN}}\text{: } t_{\text{r}}, \, t_{\text{f}} < 5 \text{ ns} \\ & (Z_{\text{out}} = 50 \; \Omega) \\ & \text{Common Source} \end{aligned}$

Ta = 25°C

(b) V_{IN}



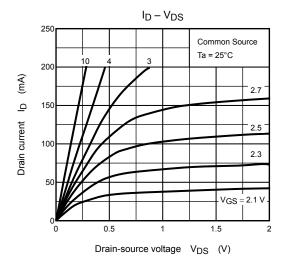
Precaution

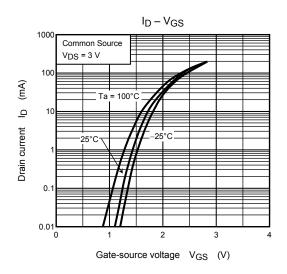
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.1mA for the SSM6N44FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

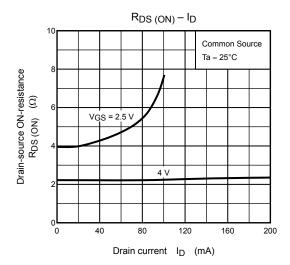
Take this into consideration when using the device

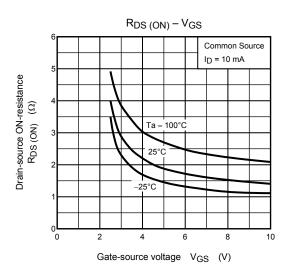
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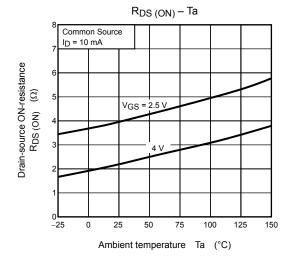
(Q1, Q2 Common)

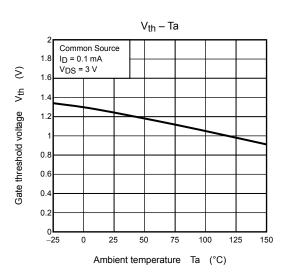




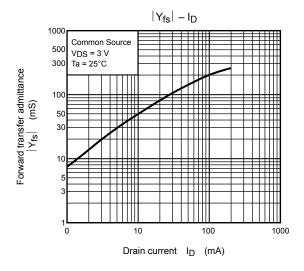


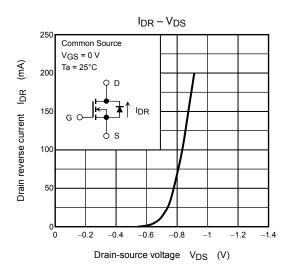


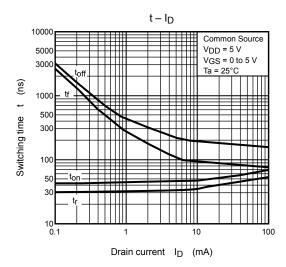


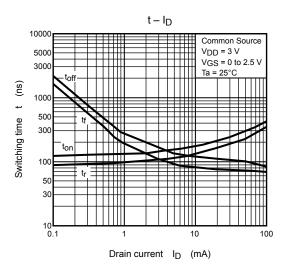


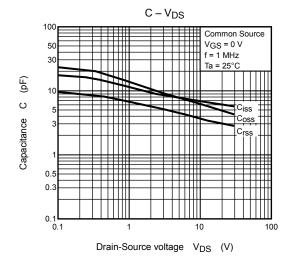
(Q1, Q2 Common)

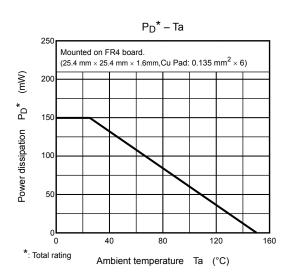












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