TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K44MFV

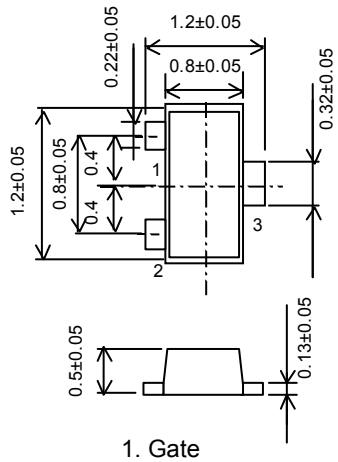
High Speed Switching Applications

Analog Switch Applications

Unit: mm

- AEC-Q101 qualified (Note 1)
- Compact package suitable for high-density mounting
- Low ON-resistance : $R_{DS(ON)}$ = 4.0 Ω (max) (@V_{GS} = 4 V)
  : $R_{DS(ON)}$ = 7.0 Ω (max) (@V_{GS} = 2.5 V)

Note 1: For detail information, please contact to our sales.



1. Gate
2. Source
3. Drain

VESM

JEDEC	—
JEITA	—
TOSHIBA	2-1L1B

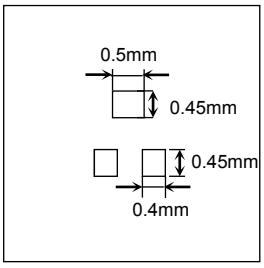
Weight: 1.5 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

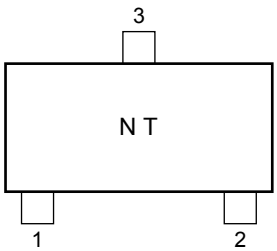
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Drain power dissipation (Ta = 25°C)		P_D (Note 1)	150	mW
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

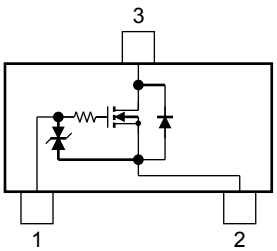
Note 1: Total rating, mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 mm)



Marking



Equivalent Circuit



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2009-12

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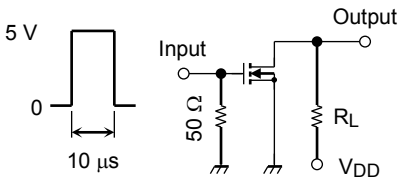
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±14 V, V_{DS} = 0 V	—	—	±1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0 V	30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.8	—	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	—	—	mS
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4 V	—	2.2	4.0	Ω
			I_D = 10 mA, V_{GS} = 2.5 V	—	4.0	7.0	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	8.5	—	pF
Reverse transfer capacitance		C_{rss}		—	5.3	—	
Output capacitance		C_{oss}		—	9.4	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0 to 5 V	—	50	—	ns
	Turn-off time	t_{off}		—	200	—	

Switching Time Test Circuit

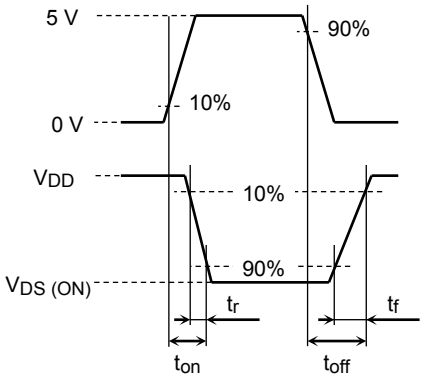
(a) Test circuit



V_{DD} = 5 V
Duty ≤ 1%
Input: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) VIN

(c) VOUT



Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)}$ < V_{th} < $V_{GS\ (on)}$)
Please take this into consideration when using the device.

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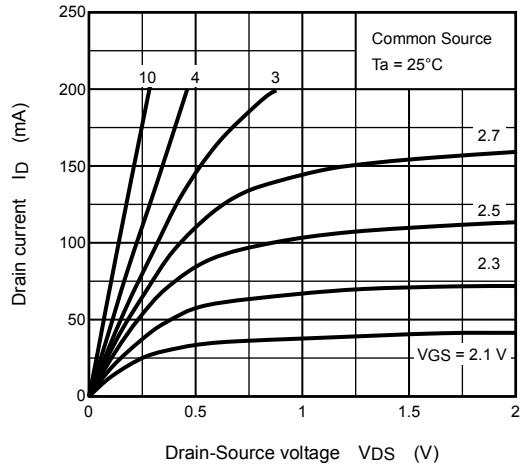
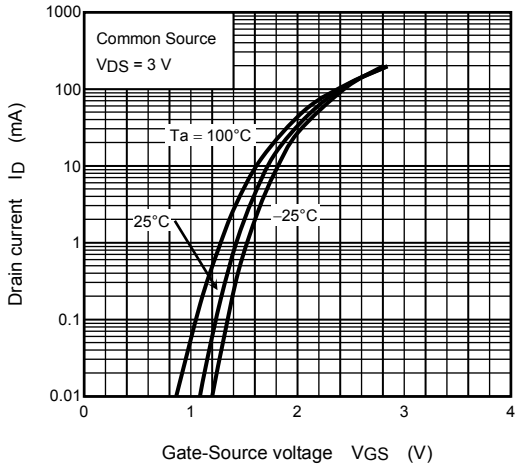
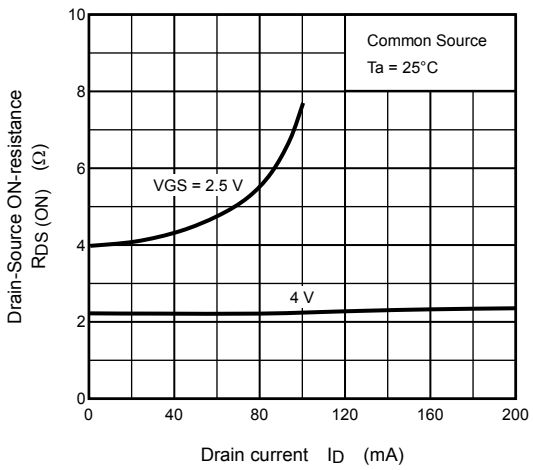
I_D – V_{DS}



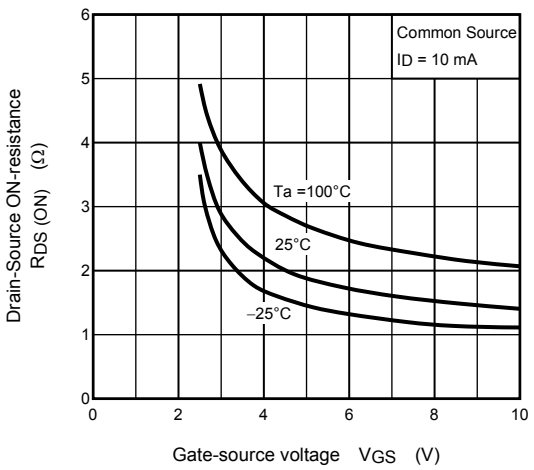
I_D – V_{GS}



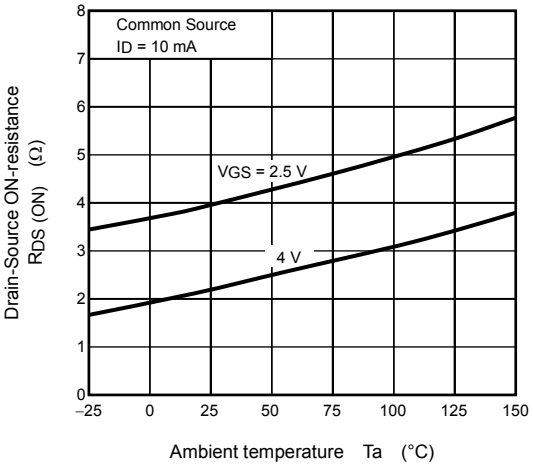
$R_{DS\ (ON)}$ – I_D



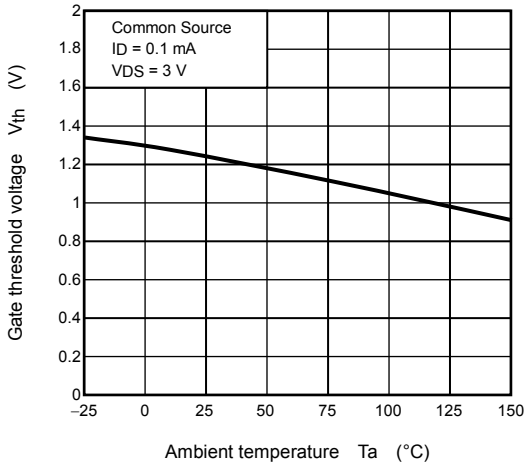
$R_{DS\ (ON)}$ – V_{GS}



$R_{DS\ (ON)}$ – Ta



V_{th} – Ta



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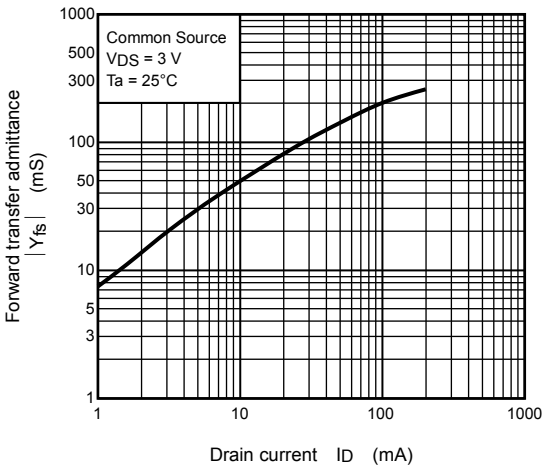
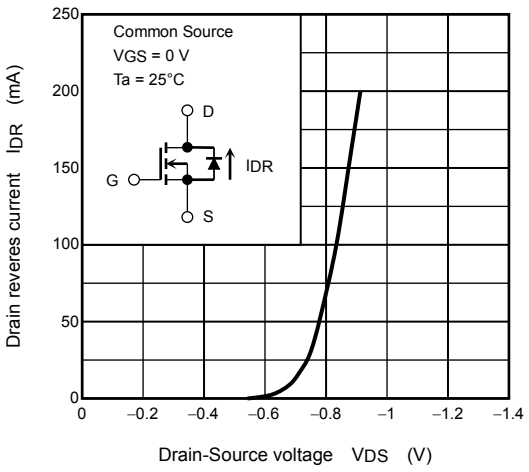
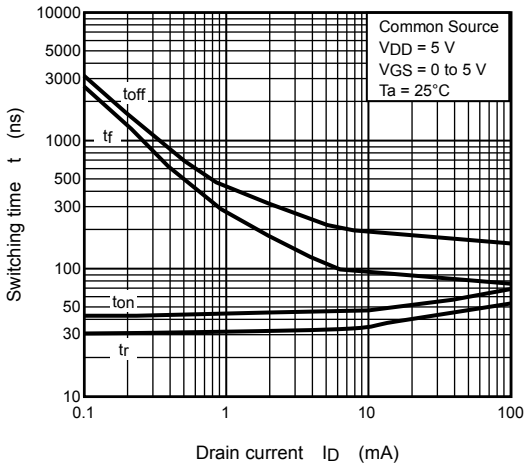
$|Y_{fs}| - I_D$



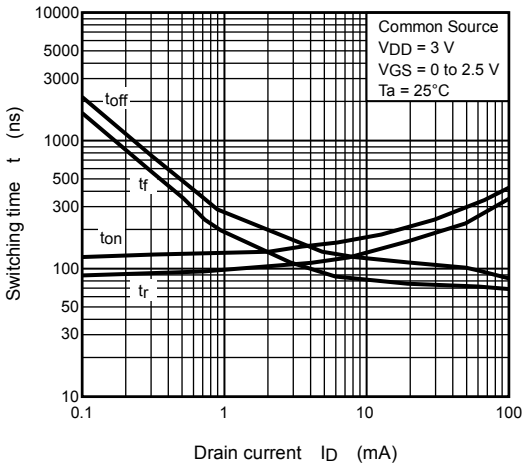
$I_{DR} - V_{DS}$



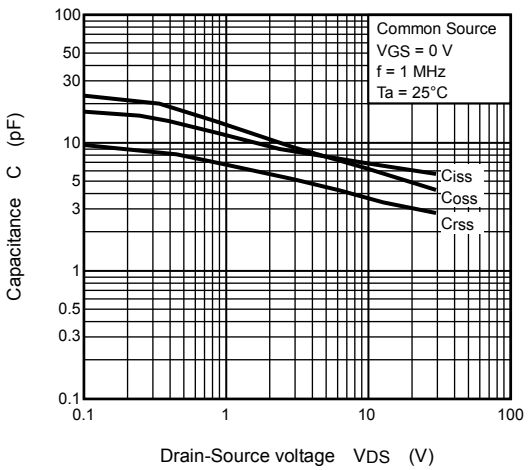
$t - I_D$



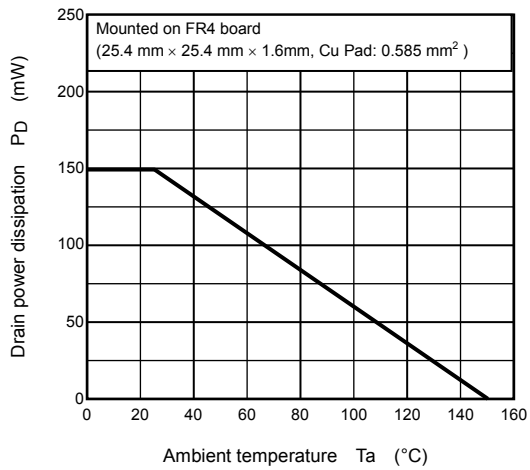
$t - I_D$



$C - V_{DS}$



$P_D - Ta$



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