

# 74HC86D

## 1. Functional Description

- Quad Exclusive OR Gate

## 2. General

The 74HC86D is a high speed CMOS EXCLUSIVE OR GATE fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

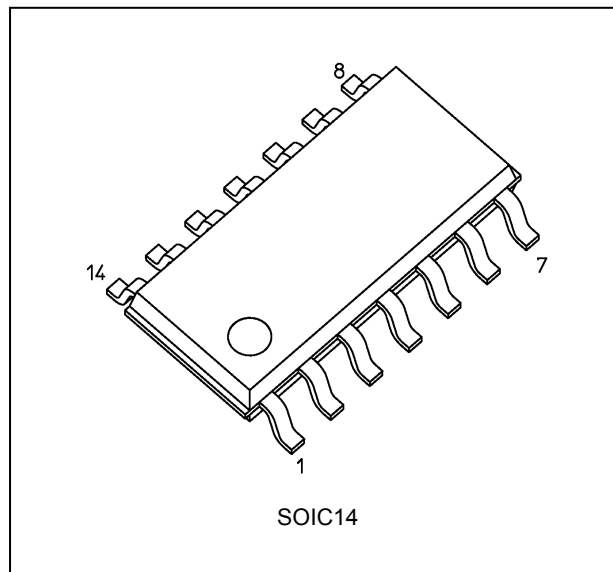
Input and output buffers are provided which offer high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) High speed:  $t_{pd} = 10 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- (2) Low power dissipation:  $I_{CC} = 1.0 \mu\text{A}$  (max) at  $T_a = 25 \text{ }^\circ\text{C}$
- (3) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (4) Wide operating voltage range:  $V_{CC(opr)} = 2.0 \text{ to } 6.0 \text{ V}$

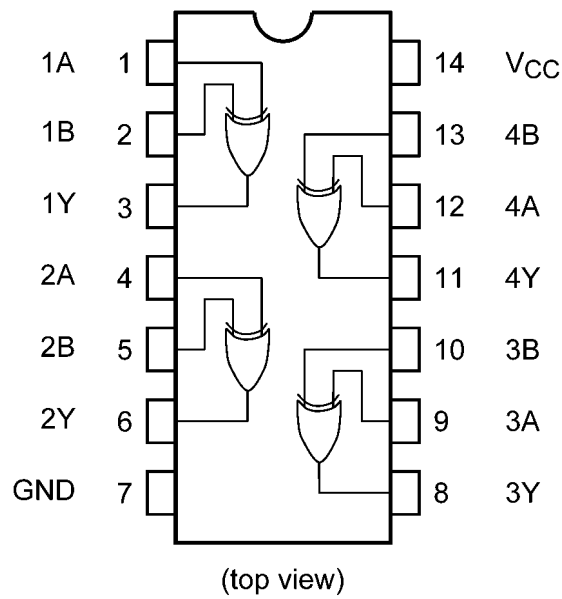
## 4. Packaging



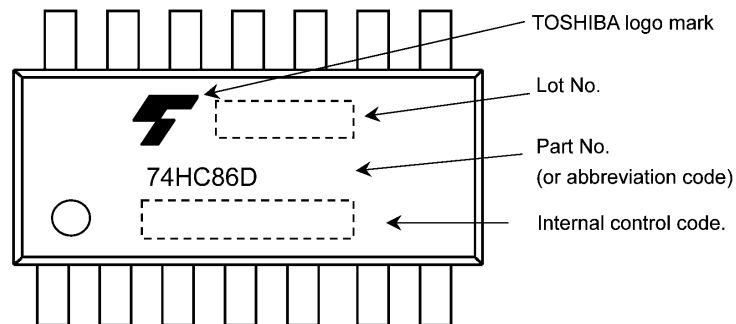
Start of commercial production

2016-02

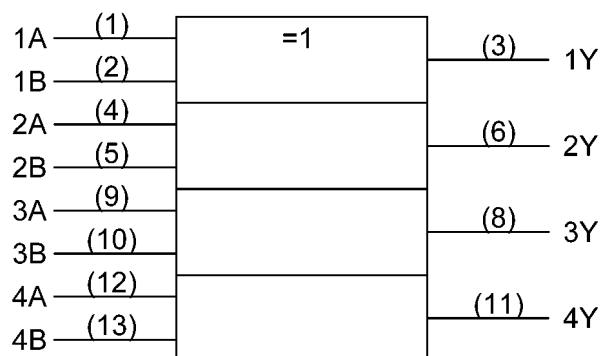
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



**8. Truth Table**

A	B	Y
H	H	L
L	H	H
H	L	H
L	L	L

**9. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	500	mW
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:  $P_D$  derates linearly with -8 mW/ $^{\circ}C$  above 85  $^{\circ}C$

**10. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$	—	2.0 to 6.0	V
Input voltage	$V_{IN}$	—	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	—	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	—	-40 to 125	$^{\circ}C$
Input rise and fall times	$t_r, t_f$	—	0 to 50	$\mu s$

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND.

**11. Electrical Characteristics**

**11.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			4.5	3.15	—	—		
			6.0	4.20	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			4.5	—	—	1.35		
			6.0	—	—	1.80		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	6.0	5.9	6.0	—	
				6.0	5.68	5.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.17	0.26	
				6.0	—	0.18	0.26	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	1.0	$\mu\text{A}$	

**11.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V	
			4.5	3.15	—		
			6.0	4.20	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V	
			4.5	—	1.35		
			6.0	—	1.80		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	—	V
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	6.0	5.9	—	
				6.0	5.63	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.33	
				6.0	—	0.33	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	10.0	$\mu\text{A}$	

**11.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125$  °C)**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20$ $\mu$ A	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			$I_{OH} = -4$ mA	4.5	3.7	—	
				6.0	5.2	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20$ $\mu$ A	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			$I_{OL} = 4$ mA	4.5	—	0.4	
				6.0	—	0.4	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	$\pm 1.0$	$\mu$ A
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	40.0	$\mu$ A

**11.4. AC Characteristics**

(Unless otherwise specified,  $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	—	4	8	ns
Propagation delay time	$t_{PLH}, t_{PHL}$	—	—	10	17	

**11.5. AC Characteristics**

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Note	$V_{CC}$ (V)	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$		2.0	—	30	75	ns
			4.5	—	8	15	
			6.0	—	7	13	
Propagation delay time	$t_{PLH}, t_{PHL}$		2.0	—	45	100	ns
			4.5	—	13	20	
			6.0	—	11	17	
Input capacitance	$C_{IN}$		—	—	3	—	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—	—	8	—	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4 \text{ (per gate)}$$

**11.6. AC Characteristics**

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 85 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	$V_{CC}$ (V)	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	2.0	—	95	ns
		4.5	—	19	
		6.0	—	16	
Propagation delay time	$t_{PLH}, t_{PHL}$	2.0	—	125	ns
		4.5	—	25	
		6.0	—	21	

**11.7. AC Characteristics**

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 125 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	$V_{CC}$ (V)	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	2.0	—	110	ns
		4.5	—	22	
		6.0	—	19	
Propagation delay time	$t_{PLH}, t_{PHL}$	2.0	—	180	ns
		4.5	—	36	
		6.0	—	31	

Package Dimensions

Unit: mm



Weight: 0.13 g (typ.)

Package Name(s)
Nickname: SOIC14

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