TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π -MOSVII)

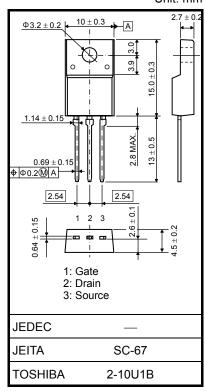
TK15A60D

Switching Regulator Applications

- Low drain-source ON-resistance: RDS (ON) = 0.31Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 8.5 \text{ S} (typ.)$
- Low leakage current: $I_{DSS} = 10 \ \mu A \ (max) \ (V_{DS} = 600 \ V)$
- Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Characte	ristics	Symbol	Rating	Unit				
Drain-source voltage		V _{DSS}	600	V				
Gate-source voltage		V _{GSS}	±30	V				
Drain current	DC (Note 1) I _D	15	А				
	Pulse (Note 1) I _{DP}	60	~				
Drain power dissipati	on (Tc = 25° C)	PD	50	W				
Single pulse avalancl	ne energy (Note 2	E _{AS}	527	mJ				
Avalanche current		I _{AR}	15	А				
Repetitive avalanche	energy (Note 3	E _{AR}	5.0	mJ				
Channel temperature		T _{ch}	150	°C				
Storage temperature	range	T _{stg}	-55 to 150	°C				

Absolute Maximum Ratings (Ta = 25°C)



Weight: 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

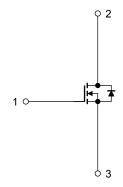
Characteristics	Symbol	Max	Unit	
Thermal resistance, channel to case	R _{th (ch-c)}	2.5	°C/W	
Thermal resistance, channel to ambient	R _{th (ch-a)}	62.5	°C/W	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: $V_{DD} = 90 \text{ V}, \text{ T}_{ch} = 25^{\circ}C(\text{initial}), \text{ L} = 4.1 \text{ mH}, \text{ R}_{G} = 25 \Omega, \text{ I}_{AR} = 15 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.



Start of commercial production 2009-01

Unit: mm

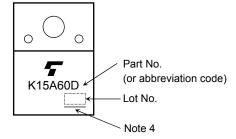
Electrical Characteristics (Ta = 25°C)

Char	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS}=\pm 30~V,~V_{DS}=0~V$	_		±1	μA
Drain cut-off curr	rent	I _{DSS}	$V_{DS} = 600 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			10	μA
Drain-source bre	akdown voltage	V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	600			V
Gate threshold v	oltage	V _{th}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$	2.0		4.0	V
Drain-source ON	I resistance	R _{DS (ON)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$	_	0.31	0.37	Ω
Forward transfer	admittance	Y _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$	2.4	8.5	_	S
Input capacitance		C _{iss}		_	2600	_	
Reverse transfer capacitance		C _{rss}	$V_{DS} = 25 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$		11	_	pF
Output capacitance		C _{oss}			280		
Switching time	Rise time	tr	V_{GS} $0 V$ V_{GS} $0 V$	_	50	_	- ns
	Turn-on time	t _{on}		_	100	_	
	Fall time	t _f			25	_	
	Turn-off time	t _{off}	Duty \leq 1%, t _w = 10 µs	_	150	_	
Total gate charge		Qg			45		
Gate-source charge		Q _{gs}	V _{DD} ≈ 400 V, V _{GS} = 10 V, I _D = 15 A		28		nC
Gate-drain charge		Q _{gd}]		17	_	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	_	—	_	15	A
Pulse drain reverse current (Note 1)	I _{DRP}	—	_	_	60	А
Forward voltage (diode)	V _{DSF}	I _{DR} = 15 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 15 A, V _{GS} = 0 V,	_	1700	_	ns
Reverse recovery charge	Q _{rr}	dl _{DR} /dt = 100 A/μs		26	_	μC

Marking

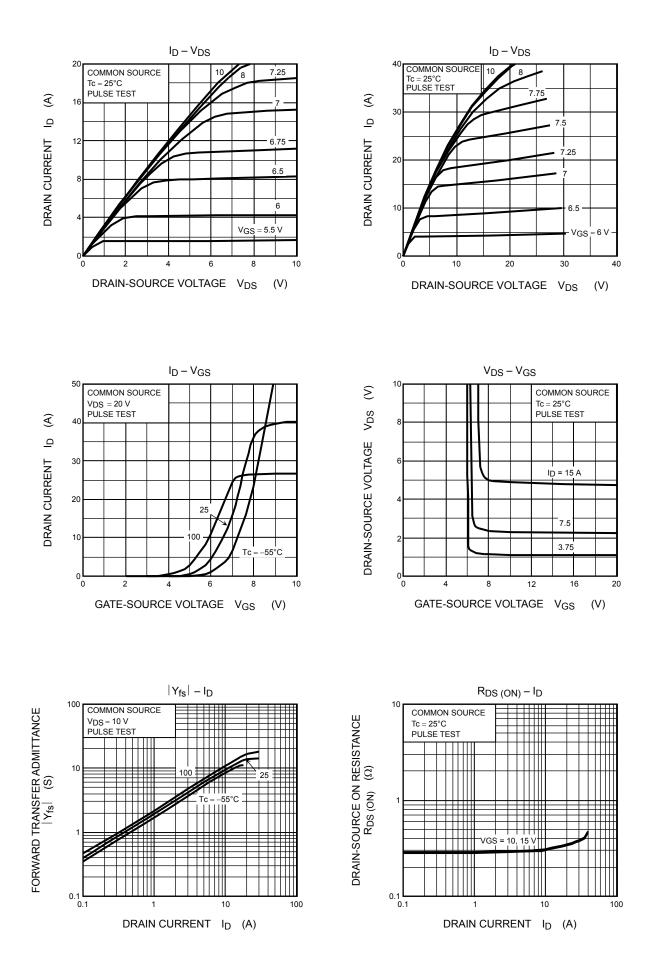


Note 4 : A line under a Lot No. identifies the indication of product Labels [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

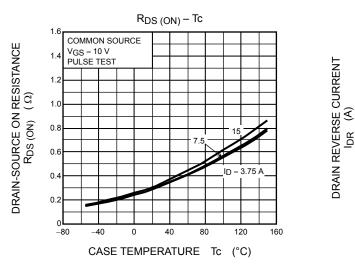
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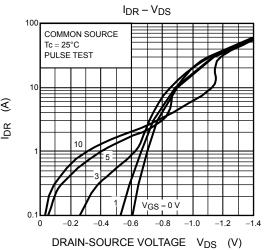
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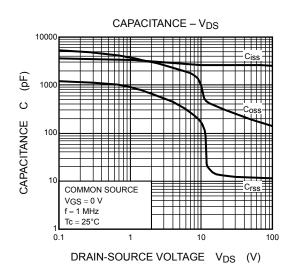
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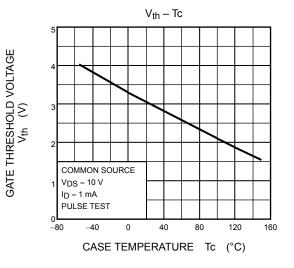


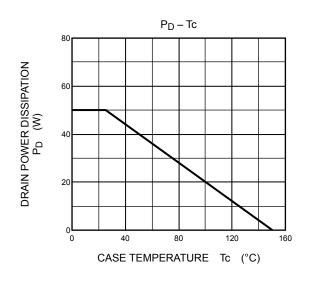
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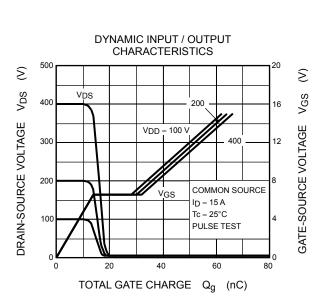


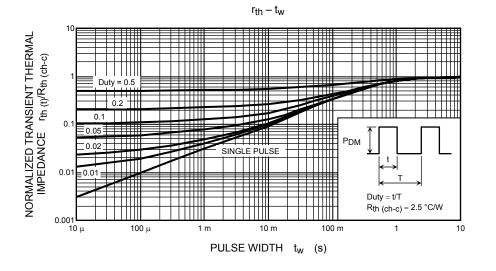


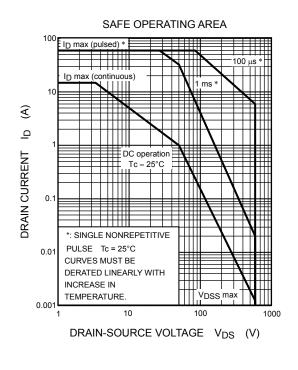


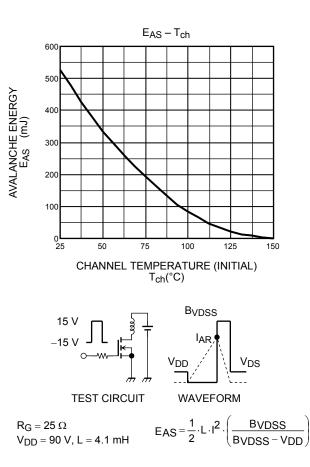












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