TOSHIBA BiCD Integrated Circuit Silicon Monolithic

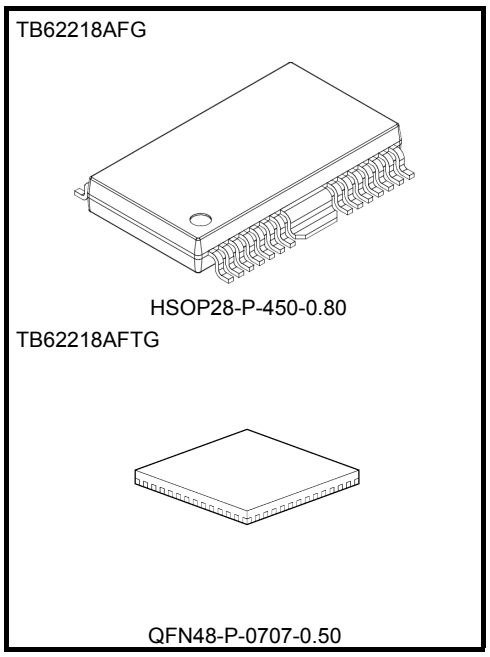
TB62218AFG, TB62218AFTG

BiCD Constant-Current Two-Phase Bipolar Stepping Motor Driver IC

The TB62218AFG/AFTG is a two-phase bipolar stepping motor driver using a PWM chopper.

Fabricated with the BiCD process, the TB62218AFG/AFTG is rated at 40 V/2.0 A.

The on-chip voltage regulator allows control of a stepping motor with a single V_M power supply.



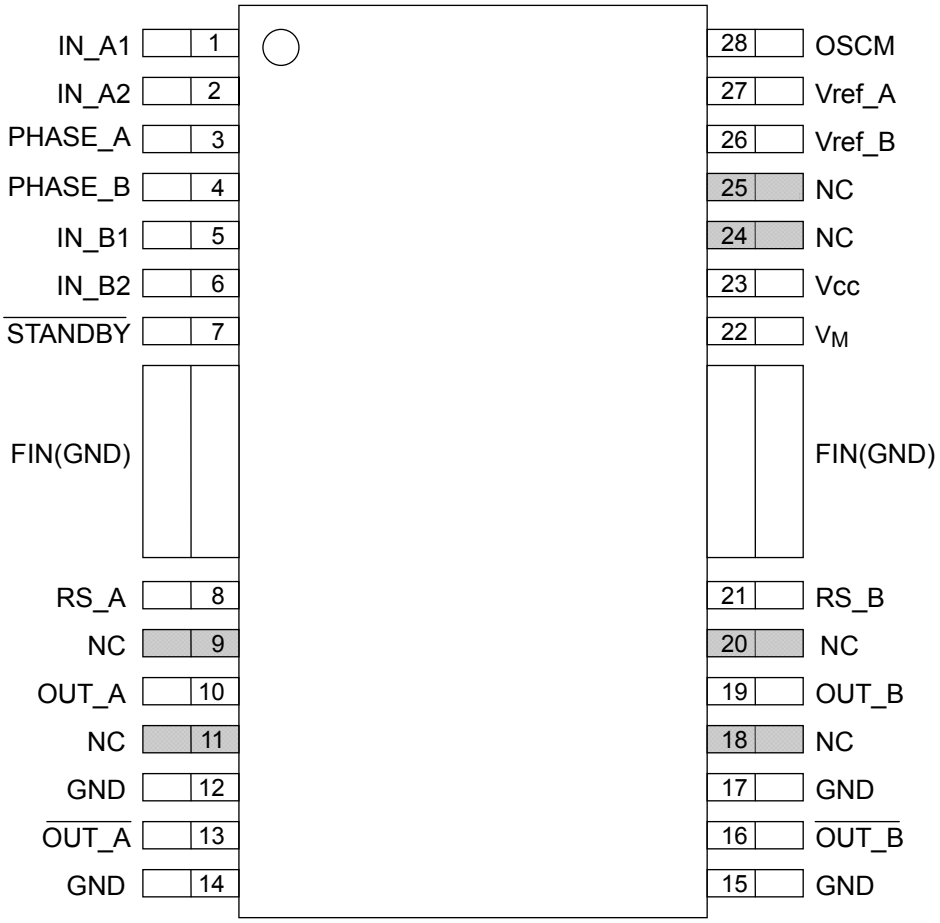
Weight
HSOP28-P-0450-0.80: 0.79 g (typ.)
QFN48-P-0707-0.50: 0.14 g (typ.)

Features

- Bipolar stepping motor driver
- PWM constant-current drive
- Allows two-phase, 1-2-phase and W1-2 phase excitations.
- BiCD process: Uses DMOS FETs as output power transistors.
- High voltage and current: 40 V/2.0 A (absolute maximum ratings)
- Thermal shutdown (TSD), overcurrent shutdown (ISD), and power-on resets (PORs)
- Packages: HSOP28-P-0450-0.8
  QFN48-P-0707-0.50

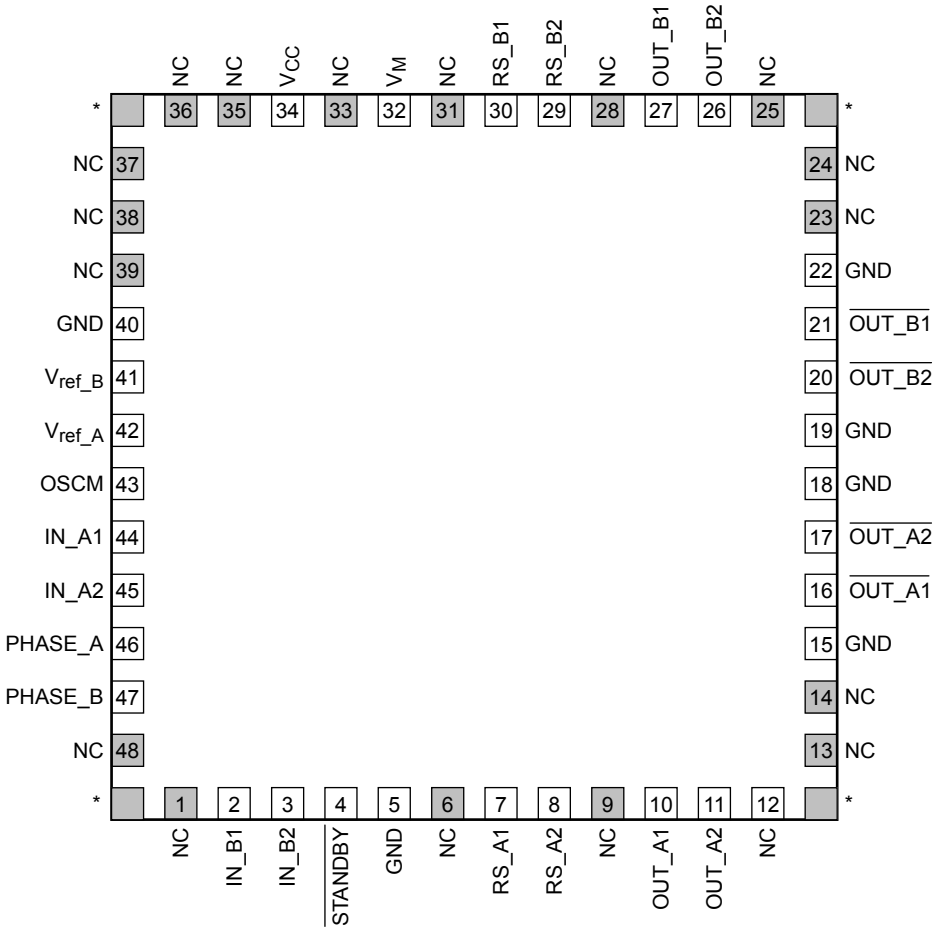
Pin Assignment

TB62218AFG (HSOP28)



Pin Assignment

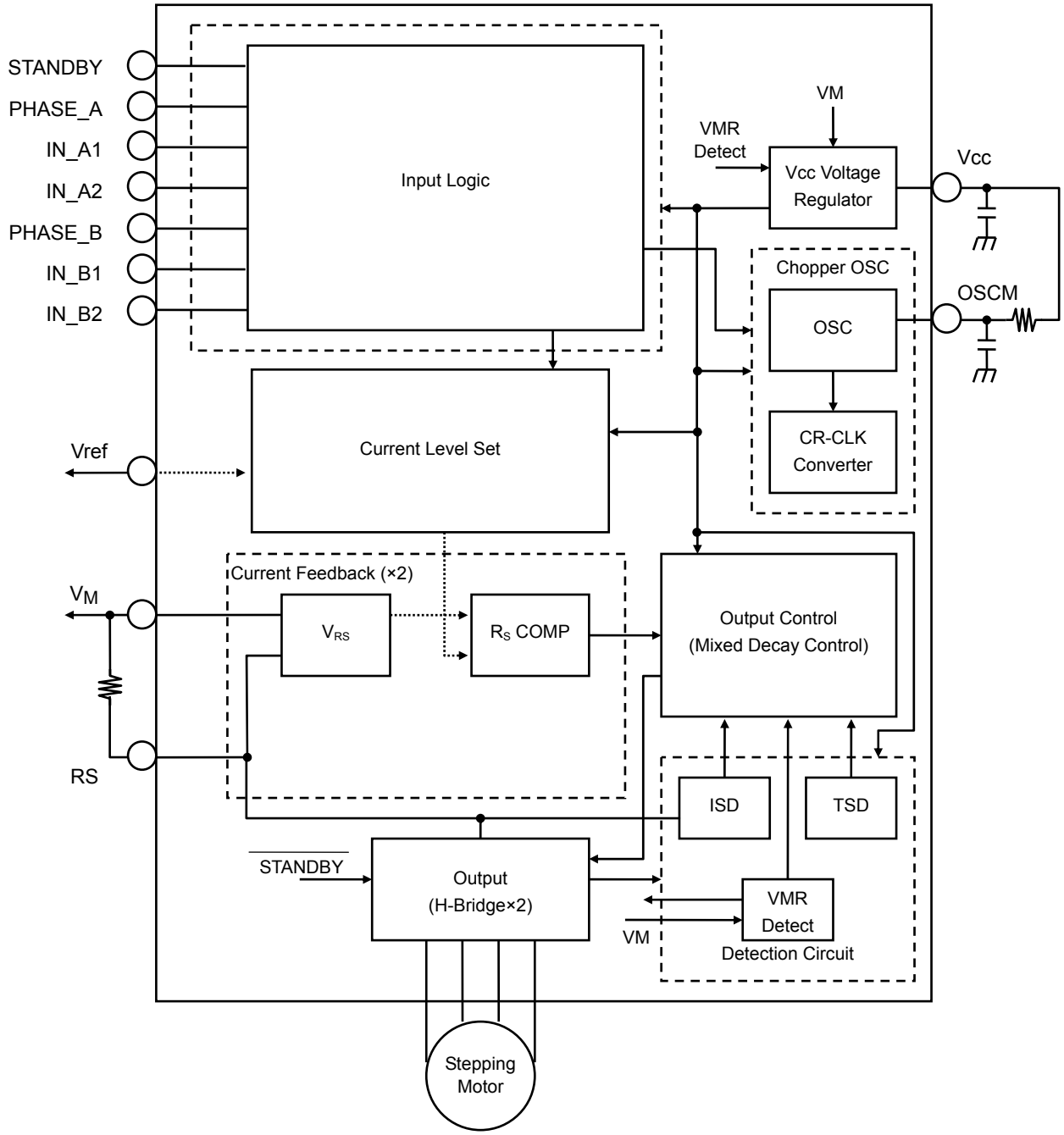
TB62218AFTG (QFN48)



*Mark PAD: It must be connected to GND

Block Diagram

In the block diagram, part of the functional blocks or constants may be omitted or simplified for explanatory purposes.



Note: All the grounding wires of the TB62218AFG/AFTG must run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.

Careful attention should be paid to the layout of the output, V_{DD} (V_M) and GND traces, to avoid short-circuits across output pins or to the power supply or ground. If such a short-circuit occurs, the TB62218AFG/AFTG may be permanently damaged.

Also, utmost care should be taken for pattern designing and implementation of the TB62218AFG/AFTG since it has the power supply pins (V_M, RS_A, RS_B, OUT_A, $\overline{\text{OUT\_A}}$, OUT_B, $\overline{\text{OUT\_B}}$, GND) particularly a large current can run through. If these pins are wired incorrectly, an operation error or even worse a destruction of the TB62218AFG/AFTG may occur.

The logic input pins must be correctly wired, too; otherwise, the TB62218AFG/AFTG may be damaged due to a current larger than the specified current running through the IC.

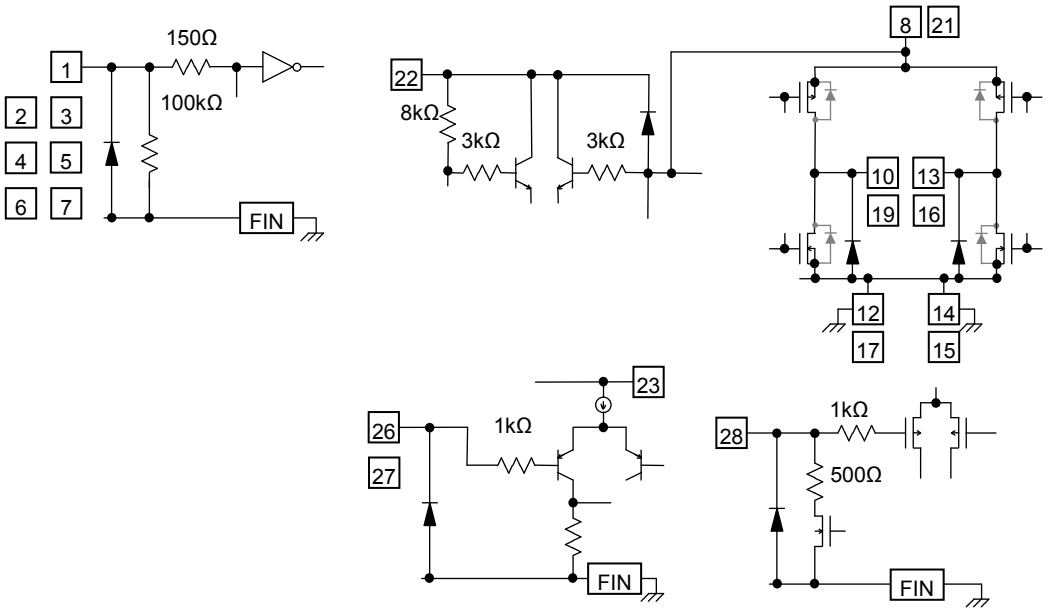
Please note the avbove when designing and implementing IC patterns.

Pin Function

TB62218AFG (HSOP28)

Pin No.	Pin Name	Function
1	IN_A1	A-phase excitation control input
2	IN_A2	A-phase excitation control input
3	PHASE_A	Current direction signal input for A phase
4	PHASE_B	Current direction signal input for B phase
5	IN_B1	B-phase excitation control input
6	IN_B2	B-phase excitation control input
7	$\overline{\text{STAND BY}}$	Output; Wait for power saving by disabling OSCM
8	RS_A	The sink current sensing of A-phase motor coil
9	NC	No-connect
10	OUT_A	A-phase positive driver output
11	NC	No-connect
12	GND	Motor power ground
13	$\overline{\text{OUT\_A}}$	A-phase negative driver output
14	GND	Motor power ground
15	GND	Motor power ground
16	$\overline{\text{OUT\_B}}$	B-phase negative driver output
17	GND	Motor power ground
18	NC	No-connect
19	OUT_B	B-phase positive driver output
20	NC	No-connect
21	RS_B	The sink current sensing of B-phase motor coil
22	V_M	Power supply
23	V_{CC}	Smoothing filter for logic power supply
24	NC	No-connect
25	NC	No-connect
26	V_{ref_B}	Tunes the current level for B-phase motor drive.
27	V_{ref_A}	Tunes the current level for A-phase motor drive.
28	OSCM	Oscillator pin for PWM choppers

Pin Interfaces (HSOP28)

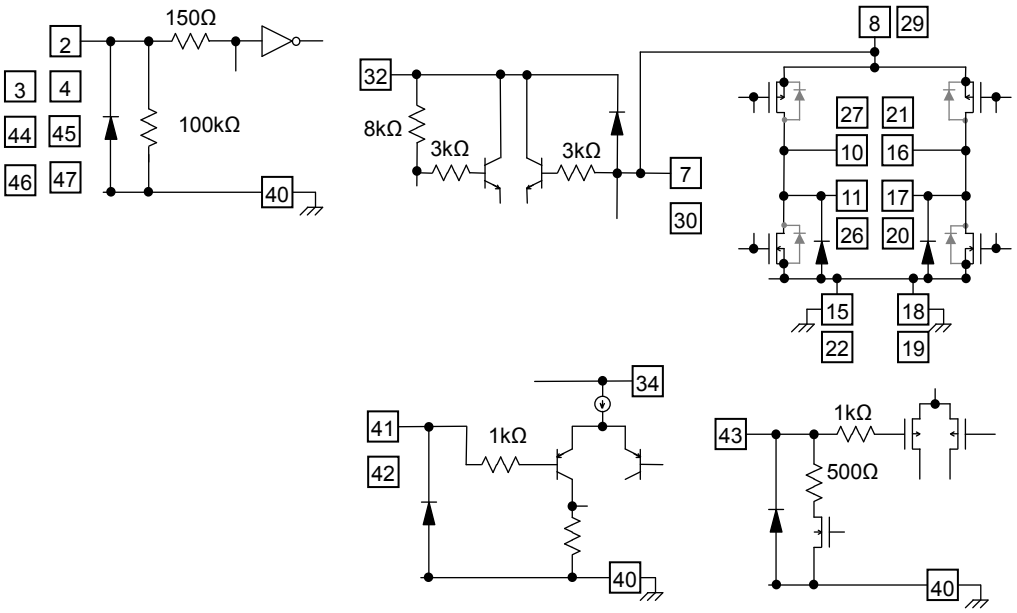


The equivalent circuit diagrams may be simplified or some parts of them may be omitted fo explanatory purposes. Absolute precision of the chip internal resistance is +/-30%.

TB62218AFTG (QFN48)

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	NC	No-connect	25	NC	No-connect
2	IN_B1	B-phase excitation control input	26	OUT_B2	B-phase positive driver output
3	IN_B2	B-phase excitation control input	27	OUT_B1	
4	$\overline{\text{STAND BY}}$	High: Normal operation mode Low: Standby mode	28	NC	No-connect
5	GND	Logic ground	29	RS_B2	Power supply pin of B-phase motor coil and the sink current sensing of B-phase motor coil
6	NC	No-connect	30	RS_B1	
7	RS_A1	Power supply pin of A-phase motor coil and the sink current sensing of A-phase motor coil	31	NC	No-connect
8	RS_A2		32	V_M	Power supply
9	NC	No-connect	33	NC	No-connect
10	OUT_A1	A-phase positive driver output	34	V_{CC}	Smoothing filter for logic power supply
11	OUT_A2		35	NC	No-connect
12	NC	No-connect	36	NC	No-connect
13	NC	No-connect	37	NC	No-connect
14	NC	No-connect	38	NC	No-connect
15	GND	Motor power ground	39	NC	No-connect
16	$\overline{\text{OUT_A1}}$	A-phase negative driver output	40	GND	Logic ground
17	$\overline{\text{OUT_A2}}$		41	V_{ref_B}	Tunes the current level for B-phase motor drive.
18	GND	Motor power ground	42	V_{ref_A}	Tunes the current level for A-phase motor drive.
19	GND	Motor power ground	43	OSCM	Oscillator pin for PWM choppers
20	$\overline{\text{OUT_B2}}$	B-phase negative driver output	44	IN_A1	A-phase excitation control input
21	$\overline{\text{OUT_B1}}$		45	IN_A2	A-phase excitation control input
22	GND	Motor power ground	46	PHASE_A	Current direction signal input for A phase
23	NC	No-connect	47	PHASE_B	Current direction signal input for B phase
24	NC	No-connect	48	NC	No-connect

Pin Interfaces (QFN48)



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.
Absolute precision of the chip internal resistance is +/-30%.

Output Function Table

Input signal			Output		
PHASE_A PHASE_B	IN_A1 IN_B1	IN_A2 IN_B2	OUT_X	$\overline{\text{OUT\_X}}$	IOUT
H	H	H	H	L	100%
	H	L	H	L	71%
	L	H	H	L	38%
	L	L	Outputs disabled	Outputs disabled	0%
L	H	H	L	H	-100%
	H	L	L	H	-71%
	L	H	L	H	-38%
	L	L	Outputs disabled	Outputs disabled	0%

IOUT: The current which flows OUT_X to $\overline{\text{OUT\_X}}$ is defined plus current. The current which flows $\overline{\text{OUT\_X}}$ to OUT_X is defined as minus current.

Input signals to IN_X and PHASE_X after the voltage range of the motor being used is attained.

(*X: A1, A2, B1. B2)

Other Functions

Pin Name	H	L	Notes
$\overline{\text{STAND BY}}$	Normal operation mode	Standby mode	When $\overline{\text{STAND BY}}$ is Low, both the oscillator and output drivers are disabled. The TB62218AFG/AFTG can not drive a motor.

Detection Features

(1) Thermal shutdown (TSD)

The thermal shutdown circuit turns off all the outputs when the junction temperature (T_j) exceeds 150°C (typ.). The outputs retain the current states.

The TB62218AFG/AFTG exits TSD mode and resume normal operation when the TB62218AFG/AFTG is rebooted or the $\overline{\text{STAND BY}}$ pin is changed from High to Low and then to High.

(2) Power-ON-resets (PORs) for VMR and VCCR (V_M and V_{CC} voltage monitor)

The outputs are forced off until V_M and V_{CC} reach the rated voltages.

(3) Overcurrent shutdown (ISD)

Each phase has an overcurrent shutdown circuit, which turns off the corresponding outputs when the output current exceeds the shutdown trip threshold (above the maximum current rating: 2.0A minimum).

The TB62218AFG/AFTG exits ISD mode and resume normal operation when the $\overline{\text{STAND BY}}$ pin is changed from High to Low and then to High.

This circuit provides protection against a short-circuit by temporarily disabling the device. Important notes on this feature will be provided later.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	Remarks
Motor power supply		V_M	40	V	—
Motor output voltage		V_{OUT}	40	V	—
Motor output current		I_{OUT}	2.0	A per phase	(Note 1)
Logic input voltage		V_{IN}	-0.5 to 6.0	V	—
Vref standard voltage		V_{ref}	5.0	V	—
Power dissipation	QFN48	P_D	1.3	W	(Note 2)
	HSOP28	P_D	1.3	W	(Note 2)
Operating temperature		T_{opr}	−20 to 85	°C	—
Storage temperature		T_{stg}	−55 to 150	°C	—
Junction temperature		$T_{j\ (MAX)}$	150	°C	—

Note 1: As a guide, the maximum output current should be kept below 1.4 A per phase. The maximum output current may be further limited by thermal considerations, depending on ambient temperature and board conditions.

Note 2: Stand-alone (Ta = 25°C)
If Ta is over 25°C, derating is required at 10.4 mW/°C.
Ta: Ambient temperature
T_{opr}: Ambient temperature while the TB62218AFG/AFTG is active
T_j: Junction temperature while the TB62218AFG/AFTG is active. The maximum junction temperature is limited
by the thermal shutdown (TSD) circuitry.
It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, $T_{j\ (max)}$, will not exceed 120°C.

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The TB62218AFG/AFTG does not have overvoltage protection. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.

All voltage ratings including supply voltages must always be followed. The other notes and considerations described later should also be referred to.

Operating Ranges (Ta = 0 to 85°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	V_M	10.0	24.0	38.0	V	—
Motor output voltage	I_{OUT}	—	1.4	2.0	A	Per phase (Note 1)
Logic input voltage	$V_{IN(H)}$	2.0	—	5.5	V	Logic high level
	$V_{IN(L)}$	-0.4	—	1.0	V	Logic low level
Chopper frequency	f_{chop}	40	100	150	kHz	—
V_{ref} reference voltage	V_{ref}	GND	—	3.6	V	—
Voltage across the current-sensing resistor pins	V_{RS}	0.0	±1.0	±1.5	V	Referenced to the V_M pin (Note 2)

Note 1: The actual maximum current may be limited by the operating environment (operating conditions such as excitation mode or operating duration, or by the surrounding temperature or board heat dissipation). Determine a realistic maximum current by calculating the heat generated under the operating environment.

Note 2: The maximum V_{RS} voltage should not exceed the maximum rated voltage.

Electrical Characteristics 1 (Ta = 25°C, V_M = 24 V, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input hysteresis voltage		$V_{IN\ (HIS)}$	DC	Digital input pins (Note)	100	200	300	mV
Digital input current	High	$I_{IN\ (H)}$	DC	V_{IN} = 5 V at the digital input pins under test	35	50	75	μA
	Low	$I_{IN\ (L)}$		V_{IN} = 0 V at the digital input pins under test	—	—	1	μA
Power consumption		I_{M1}	DC	Outputs open, $\overline{\text{STAND BY}}$ = Low	—	2	3	mA
		I_{M2}		Outputs open, $\overline{\text{STAND BY}}$ = High	—	3.5	5	mA
		I_{M3}		Outputs open (two-phase excitation)	—	5	7	mA
Output leakage current	High-side	I_{OH}	DC	V_{RS} = V_M = 40 V: V_{OUT} = 0 V	—	—	1	μA
	Low-side	I_{OL}		V_{RS} = V_M = V_{OUT} = 40 V	1	—	—	μA
Chanel-to-channel current differential		ΔI_{OUT1}	DC	Channel-to-channel error	−5	0	5	%
Output current error relative to the predetermined value		ΔI_{OUT2}	DC	I_{OUT} = 1 A	−5	0	5	%
RS pin current		I_{RS}	DC	V_{RS} = V_M = 24 V	0	—	10	μA
Drain-source ON-resistance of the output transistors (upper and lower sum)		$R_{ON\ (D-S)}$	DC	I_{OUT} = 2.0 A, T_j = 25°C	—	1.0	1.5	Ω

Note: $V_{IN\ (L \rightarrow H)}$ is defined as the V_{IN} voltage that causes the outputs (OUT_A1, OUT_A2, OUT_B1and OUT_B2 pins) to change when a pin under test is gradually raised from 0 V. $V_{IN\ (H \rightarrow L)}$ is defined as the V_{IN} voltage that causes the outputs (OUT_A1, OUT_A2, OUT_B1and OUT_B2 pins) to change when the pin is then gradually lowered.
The difference between $V_{IN\ (L \rightarrow H)}$ and $V_{IN\ (H \rightarrow L)}$ is defined as the input hysteresis.

Electrical Characteristics 2 (Ta = 25°C, V_M = 24 V, unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
V_{ref} input current	I_{ref}	DC	V_{ref} = 3.0 V	-	0	1	μA
V_{ref} decay rate	$V_{ref\ (GAIN)}$	DC	V_{ref} = 2.0 V	1/4.8	1/5.0	1/5.2	—
TSD threshold (Note 1)	T_jTSD	DC	—	140	150	170	°C
V_M recovery voltage	V_{MR}	DC	—	7.0	8.0	9.0	V
Overcurrent trip threshold (Note 2)	ISD	DC	—	2.0	3.0	4.0	A
Supply voltage for internal circuitry	V_{CC}	DC	I_{CC} = 5.0 mA	4.75	5.00	5.25	V

Note 1: Thermal shutdown (TSD) circuitry
When the junction temperature of the device has reached the threshold, the TSD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors.
The TSD circuitry is tripped at a temperature between 140°C (min) and 170°C (max). Once tripped, the TSD circuitry keeps the output transistors off until $\overline{\text{STANDBY}}$ is deasserted High or the IC is restarted. The thermal shutdown circuit is provided to turn off all the outputs when the IC is overheated. For this reason, please avoid using TSD for other purposes.

Note 2: Overcurrent shutdown (ISD) circuitry
When the output current has reached the threshold, the ISD circuitry is tripped, causing the internal reset circuitry to turn off the output transistors.
To prevent the ISD circuitry from being tripped due to switching noise, it has a masking time of four CR oscillator cycles. Once tripped, it takes a maximum of four cycles to exit ISD mode and resume normal operation.
The ISD circuitry remains active until the $\overline{\text{STANDBY}}$ pin is changed from Low to High again or the IC is restarted.
The TB62218AFG/AFTG remains in Standby mode while in ISD mode.

Note 3: If the supply voltage for internal circuitry (V_{CC}) is split with an external resistor and used as V_{ref} input supply voltage, the accuracy of the output current setting will be at ±8% when the V_{cc} output voltage accuracy and the V_{ref} damping ratio accuracy are combined.

Note 4: The circuit design has been designed so that electromotive force or leak current from signal input does not occur when VM voltage is not supplied, even if the logic input signal is input. Even so, regulate logic input signals before resupply of VM voltage so that the motor does not operate when voltage is reapplied.

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.

If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB62218AFG/AFTG or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

- The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
- If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
- The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

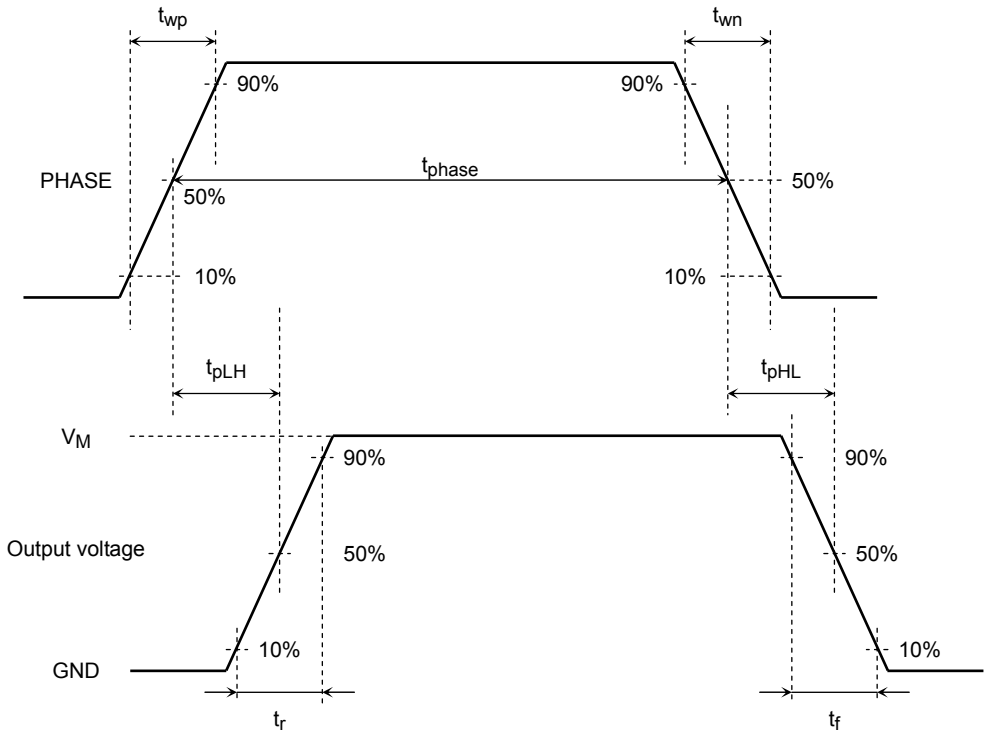
IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause the breakdown, damage and/or deterioration of the device.

AC Electrical Characteristics (Ta = 25°C, V_M = 24 V, 6.8 mH/5.7 Ω)

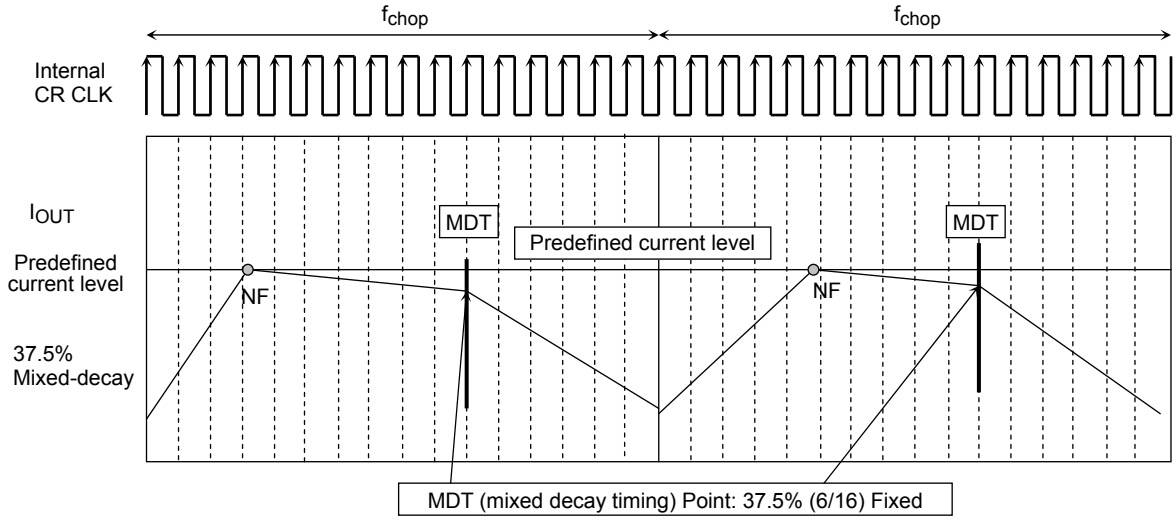
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Phase frequency	f_{PHASE}	AC	f_{OSC} = 1600 kHz	—	—	400	kHz
Minimum phase pulse width	t_{PHASE}	AC	—	100	—	—	ns
	t_{wp}	AC	—	50	—	—	ns
	t_{wn}	AC	—	50	—	—	ns
Output transistor switching characteristics	t_r	AC	—	100	150	200	ns
	t_f	AC	—	100	150	200	ns
	$t_{pLH\ (P)\ MAX}$	AC	PHASE to OUT	500	850	1200	ns
	$t_{pHL\ (P)\ MAX}$	AC	PHASE to OUT	500	850	1200	ns
	$t_{pLH\ (P)\ MIN}$	AC	PHASE to OUT	250	600	950	ns
	$t_{pHL\ (P)\ MIN}$	AC	PHASE to OUT	250	600	950	ns
Blanking time for current spike prevention	t_{BLANK}	AC	I_{OUT} = 1.0 A	200	300	500	ns
OSC oscillation reference frequency	f_{CR}	AC	C_{OSC} = 270 pF, R_{OSC} = 3.6 kΩ	1200	1600	2000	kHz
Chopper frequency range	$f_{chop\ (RANGE)}$	AC	V_M = 24 V, outputs enabled ACTIVE (I_{OUT} = 1.0 A)	40	100	150	kHz
Predefined chopper frequency	f_{chop}	AC	Outputs enabled (I_{OUT} = 1.0 A), C_R = 1600 kHz	—	100	—	kHz
ISD masking time	TISD (Mask)	AC	After ISD threshold is exceeded due to an output short-circuit to power or ground	—	4	—	CR-CLK
ISD on-time	tISD	AC	After ISD threshold is exceeded due to an output short-circuit to power or ground	4	—	8	CR-CLK

Timing Charts of Output Transistors Switching



● Current Waveform in Mixed Decay Mode

Mixed-Decay mode, the purpose of which is constant-current control, starts out in Fast-Decay mode for 37.5% of the whole period and then is followed by Slow-Decay mode for the remainder of the period.

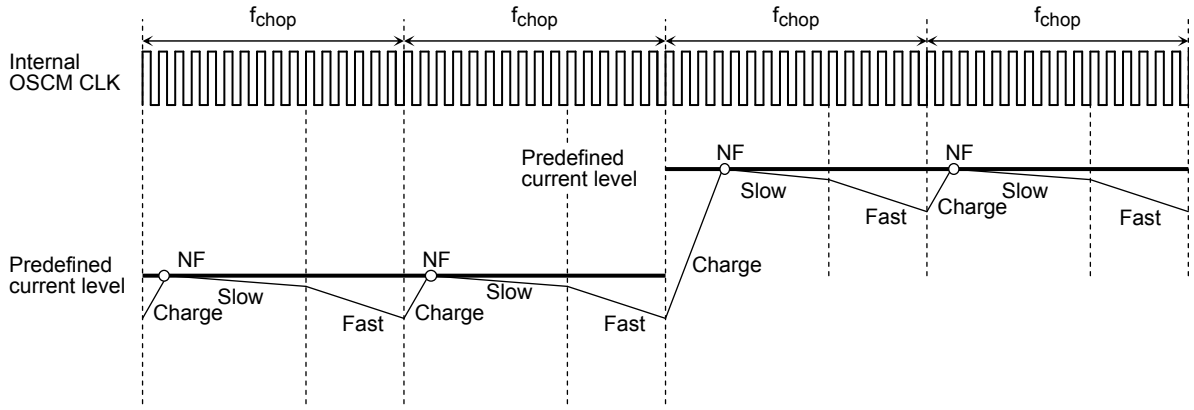


Timing charts may be simplified for explanatory purposes.

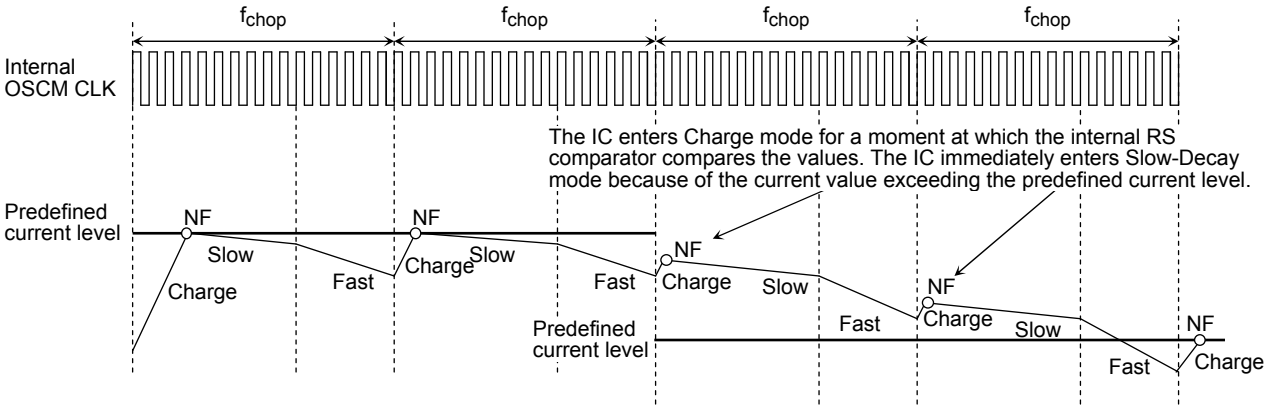
● Current Waveform in Mixed (Slow + Fast) Decay Mode

Timing charts may be simplified for explanatory purposes.

- When a current value increases (Mixed-Decay point is fixed to 37.5%)



- When a current value decreases (Mixed-Decay point is fixed to 37.5%)



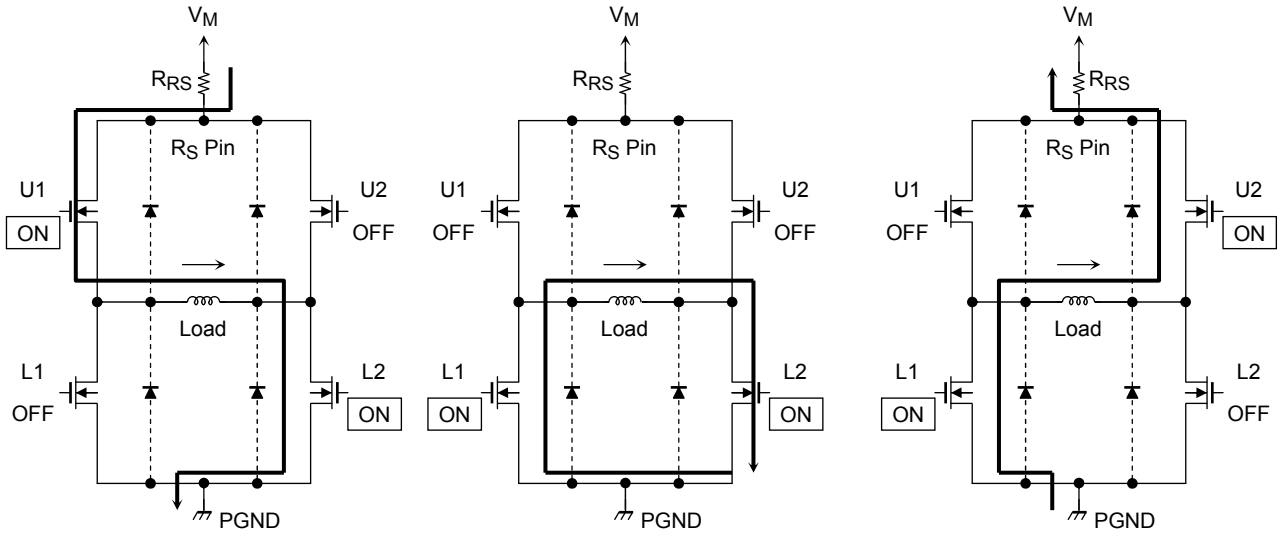
The Charge period starts as the internal oscillator clock starts counting. When the output current reaches the predefined current level, the internal RS comparator detects the predefined current level (NF); as a result, the IC enters Slow-Decay mode.

The TB62218AFG/AFTG transits from Slow-Decay mode to Fast-Decay mode at the point 37.5 of a PWM frequency (one chopping frequency) remains in a whole PWM frequency period (on the rising edge of the 11th clock of the OSCM clock).

When the OSCM pin clock counter clocks 16 times, the Fast-Decay mode ends; and at the same time, the counter is reset, which brings the TB62218AFG/AFTG into Charge mode again.

Note: These figures are intended for illustrative purposes only. If designed more realistically, they would show transient response curves.

● Output Transistor Operating Modes



Output Transistor Operating Modes

CLK	U1	U2	L1	L2
Charge	ON	OFF	OFF	ON
Slow-Decay Mode	OFF	OFF	ON	ON
Fast-Decay Mode	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above. If the current flows in the opposite direction, refer to the following table.

CLK	U1	U2	L1	L2
Charge	OFF	ON	ON	OFF
Slow-Decay Mode	OFF	OFF	ON	ON
Fast-Decay Mode	ON	OFF	OFF	ON

The TB62218AFG/AFGT switches among Charge, Slow-Decay and Fast-Decay modes automatically for constant-current control.

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Calculation of the Predefined Output Current

For PWM constant-current control, the TB62218AFG/AFTG uses a clock generated by the CR oscillator. The peak output current can be set via the current-sensing resistor (R_{RS}) and the reference voltage (V_{ref}), as follows:

$$I_{OUT} = V_{ref}/5 \div R_{RS}\ (\Omega)$$

where, 1/5 is the V_{ref} decay rate, V_{ref} (GAIN). For the value of V_{ref} (GAIN), see the Electrical Characteristics table.

For example, when V_{ref} = 3 V, to generate an output current (I_{OUT}) of 0.8 A, R_{RS} is calculated as:

$$R_{RS} = (V_{ref}/5) \div I_{OUT} = (3/5) \div 0.8 = 0.75\ \Omega.\ (\geq 0.5\ W)$$

IC Power Consumption

The power consumed by the TB62218AFG/AFTG is approximately the sum of the following two: 1) the power consumed by the output transistors, and 2) the power consumed by the digital logic and pre-drivers.

- The power consumed by the output transistors is calculated, using the R_{ON} (D-S) value of 1.0 Ω.
- Whether in Charge, Fast Decay or Slow Decay mode, two of the four transistors comprising each H-bridge contribute to its power consumption at a given time.

Thus the power consumed by each H-bridge is given by:

$$P\ (out) = I_{OUT}\ (A) \times V_{DS}\ (V) = 2 \times I_{OUT}^2 \times R_{ON} \quad \ldots\ldots (1)$$

In two-phase excitation mode (in which two phases have a phase difference of 90°), the average power consumption in the output transistors is calculated as follows:

R_{ON} = 1.0 Ω (@2.0 A)
I_{OUT} (Peak) = 1.0 A
V_M = 24 V

$$P\ (out) = 2Hsw \times 1.0^2\ (A) \times 1.0\ (\Omega) = 2.0\ (W) \quad \ldots\ldots (2)$$

The power consumption in the IM domain is calculated separately for normal operation and standby modes:

Normal operation mode: I (I_{M3}) = 5.0 mA (typ.)
Standby mode: I (I_{M1}) = 2.0 mA (typ.)

The current consumed in the digital logic portion of the TB62218AFG/AFTG is indicated as I_{Mx}. The digital logic operates off a voltage regulator that is internally connected to the V_M power supply. It consists of the digital logic connected to V_M (24 V) and the network affected by the switching of the output transistors. The total power consumed by I_{Mx} can be estimated as:

$$P\ (I_M) = 24\ (V) \times 0.005\ (A) = 0.12\ (W) \quad \ldots\ldots (3)$$

Hence, the total power consumption of the TB62218AFG/AFTG is:

$$P = P\ (out) + P\ (I_M) = 2.12\ (W)$$

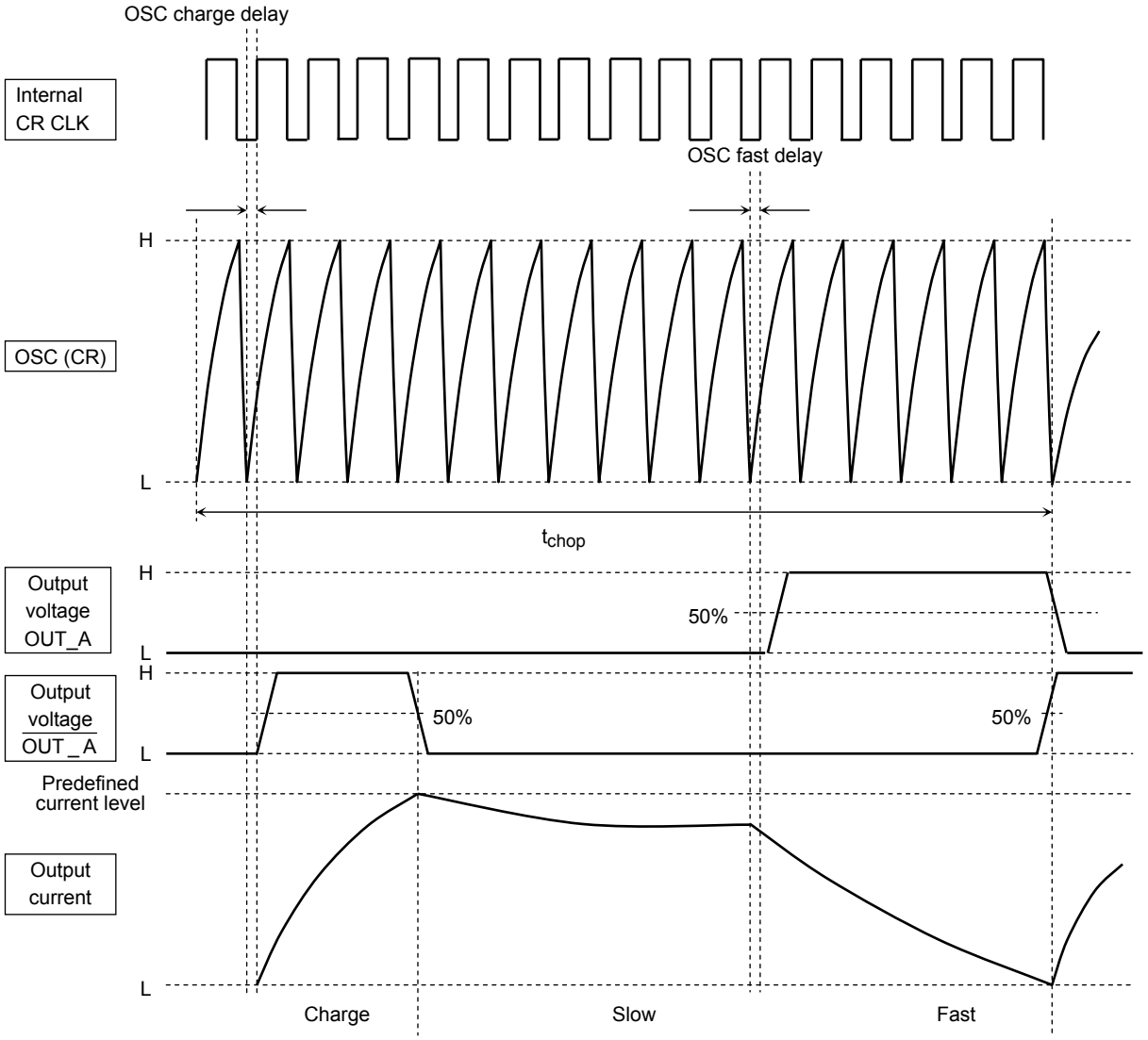
The standby power consumption is given by:

$$P\ (Standby)\ ,\ P\ (out) = 24\ (V) \times 0.002\ (A) = 0.048\ (W)$$

Board design should be fully verified, taking thermal dissipation into consideration.

● OSC-Charge Delay

Since the rising level of the OSC waveform is referenced to convert it into the internal CR CLK waveform, about up to1 us (when CR = 1600 kHz) of a delay occurs between the OSC waveform and internal CR CLK waveform.

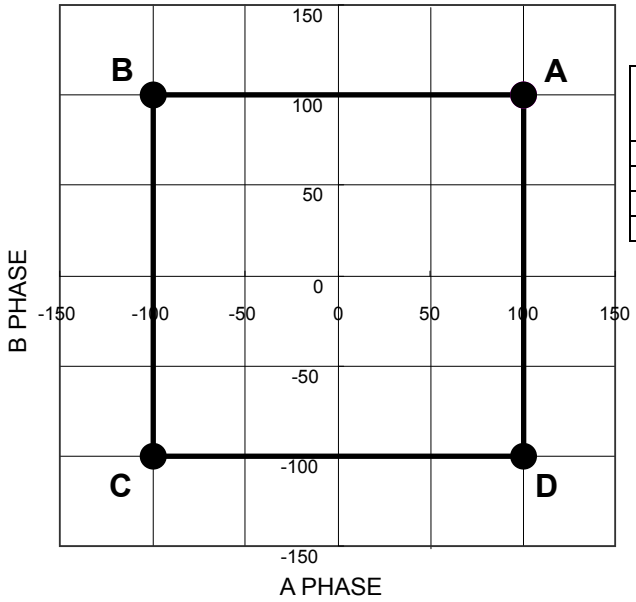


Timing charts may be simplified for explanatory purposes.

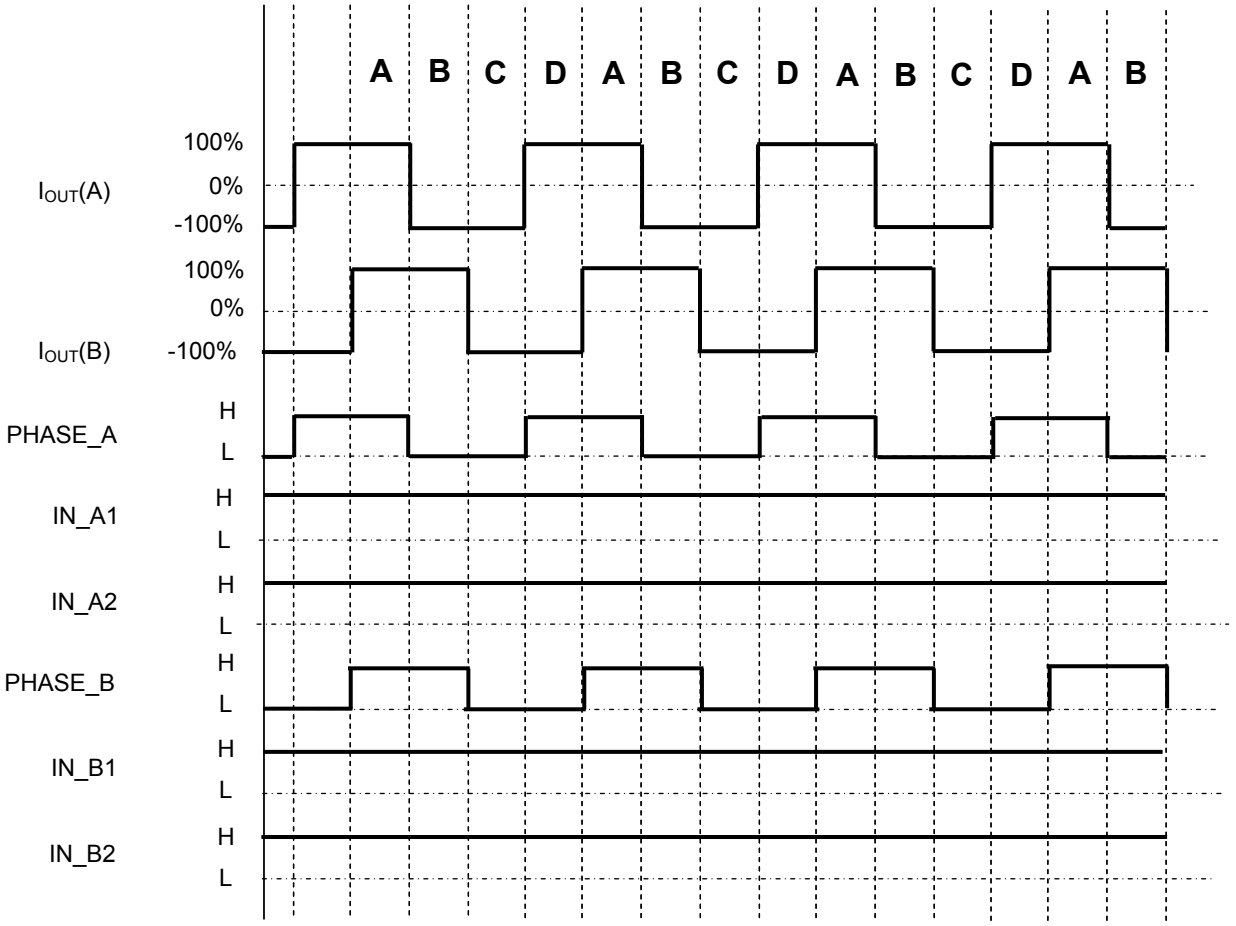
Phase Sequences

Two-Phase Excitation Mode

Timing charts may be simplified for explanatory purposes.

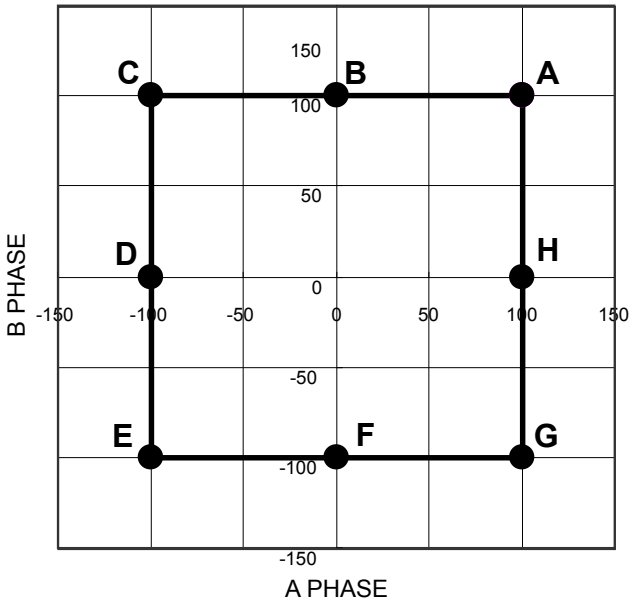


	A PHASE				B PHASE			
	Input			Output	Input			Output
	PHASE A	IN A1	IN A2	IOUT(A)	PHASE B	IN B1	IN B2	IOUT(B)
A	H	H	H	100%	H	H	H	100%
B	L	H	H	-100%	H	H	H	100%
C	L	H	H	-100%	L	H	H	-100%
D	H	H	H	100%	L	H	H	-100%

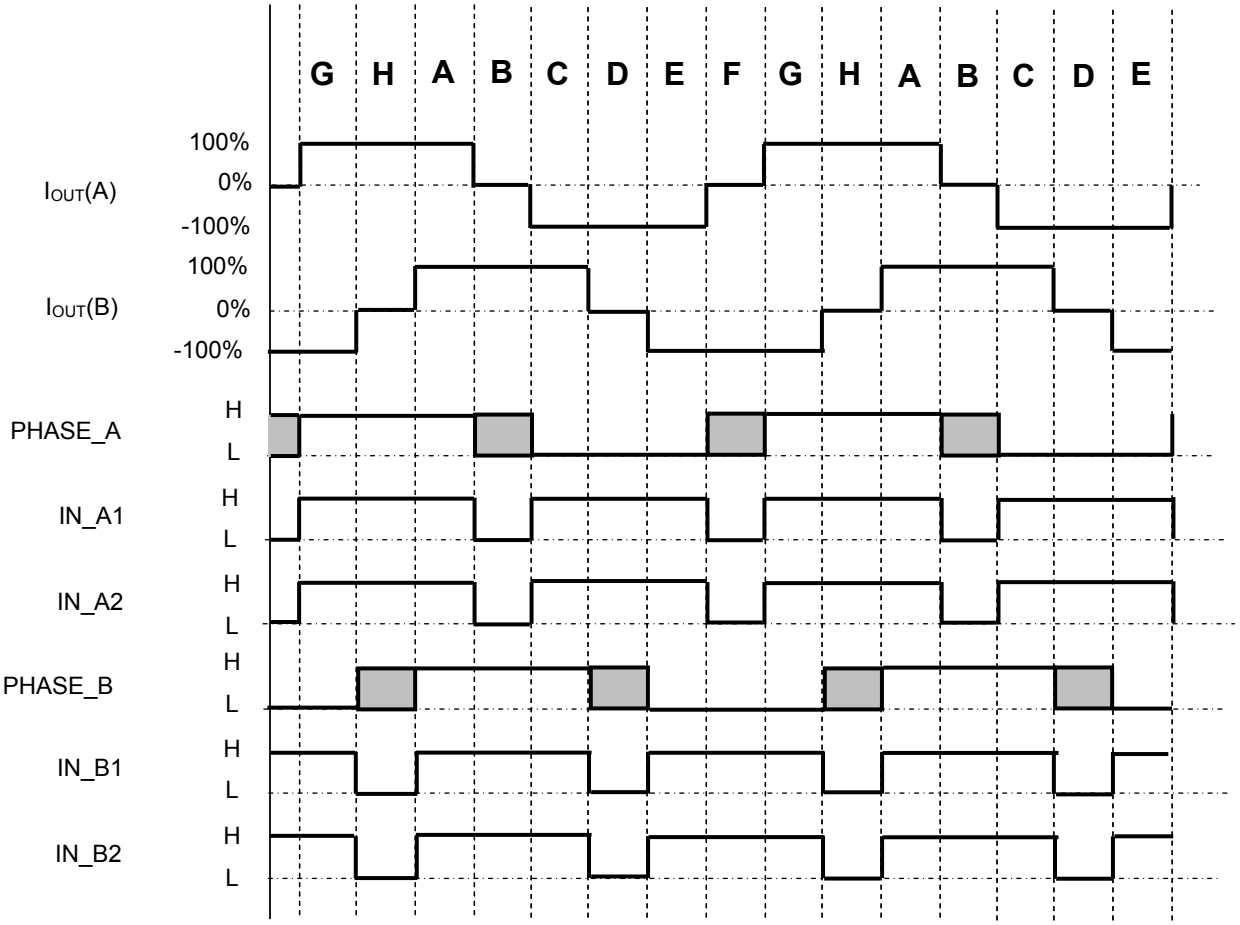


1-2-Phase Excitation

Timing charts may be simplified for explanatory purposes.

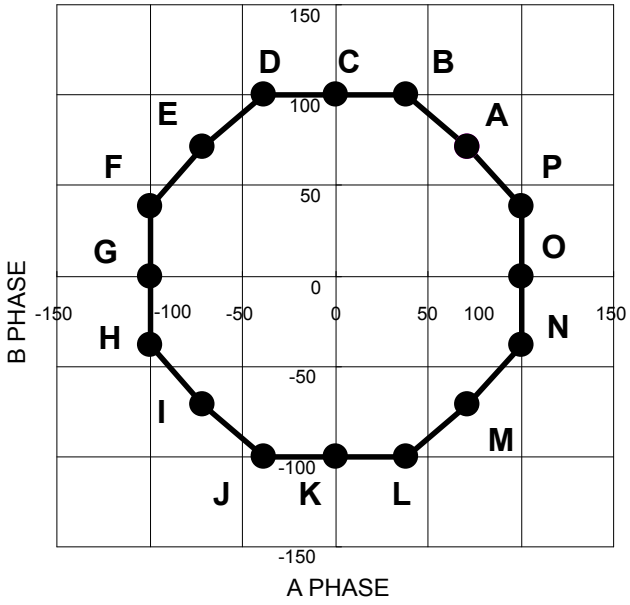


	A PHASE				BPHASE			
	Input			Output	Input			Output
	PHASE A	IN A1	IN A2	IOUT(A)	PHASE B	IN B1	IN B2	IOUT(B)
A	H	H	H	100%	H	H	H	100%
B	X	L	L	0%	H	H	H	100%
C	L	H	H	-100%	H	H	H	100%
D	L	H	H	-100%	X	L	L	0%
E	L	H	H	-100%	L	H	H	-100%
F	X	L	L	0%	L	H	H	-100%
G	H	H	H	100%	L	H	H	-100%
H	H	H	H	100%	X	L	L	0%

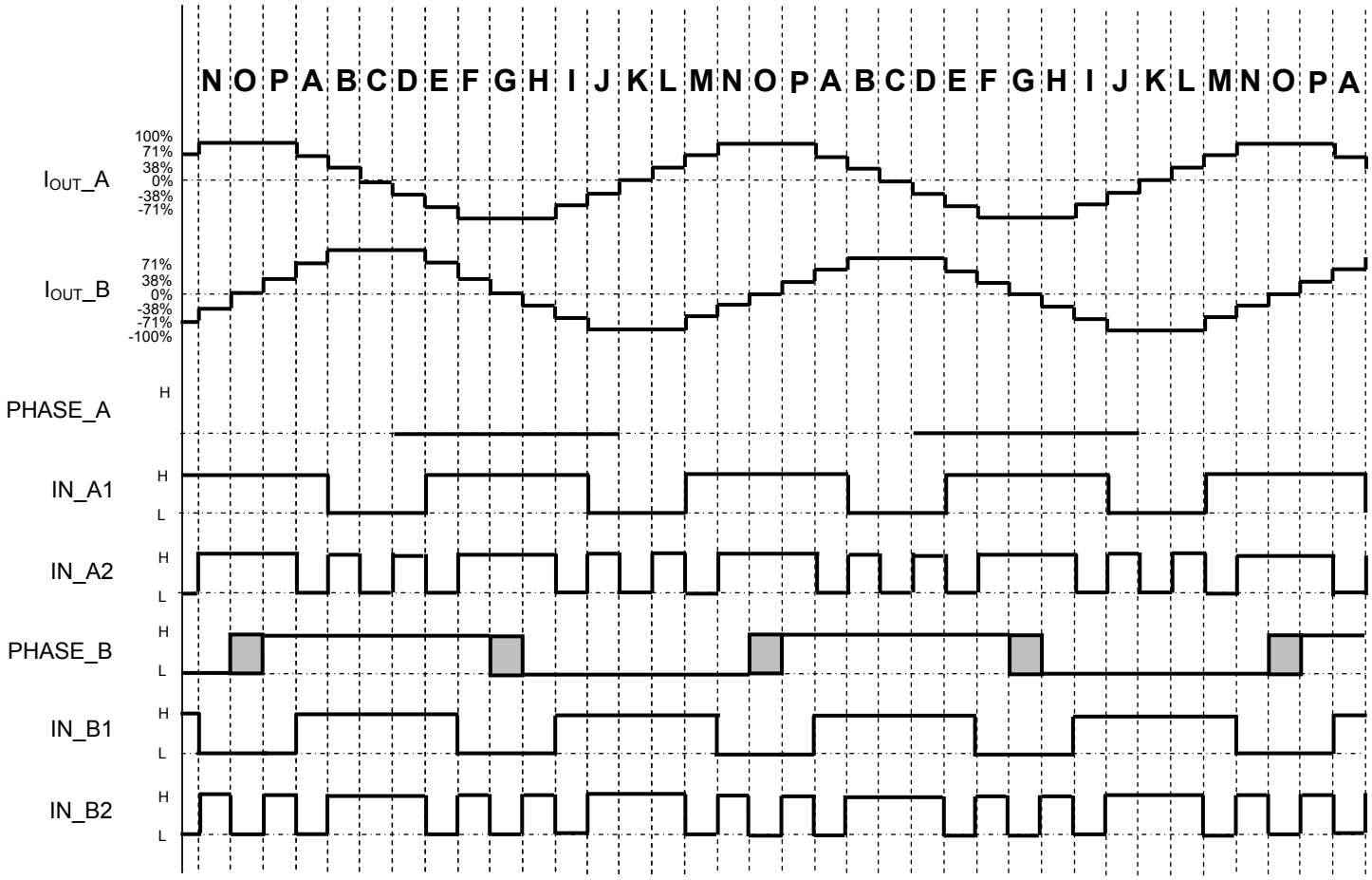


W1-2-Phase Excitation

Timing charts may be simplified for explanatory purposes.

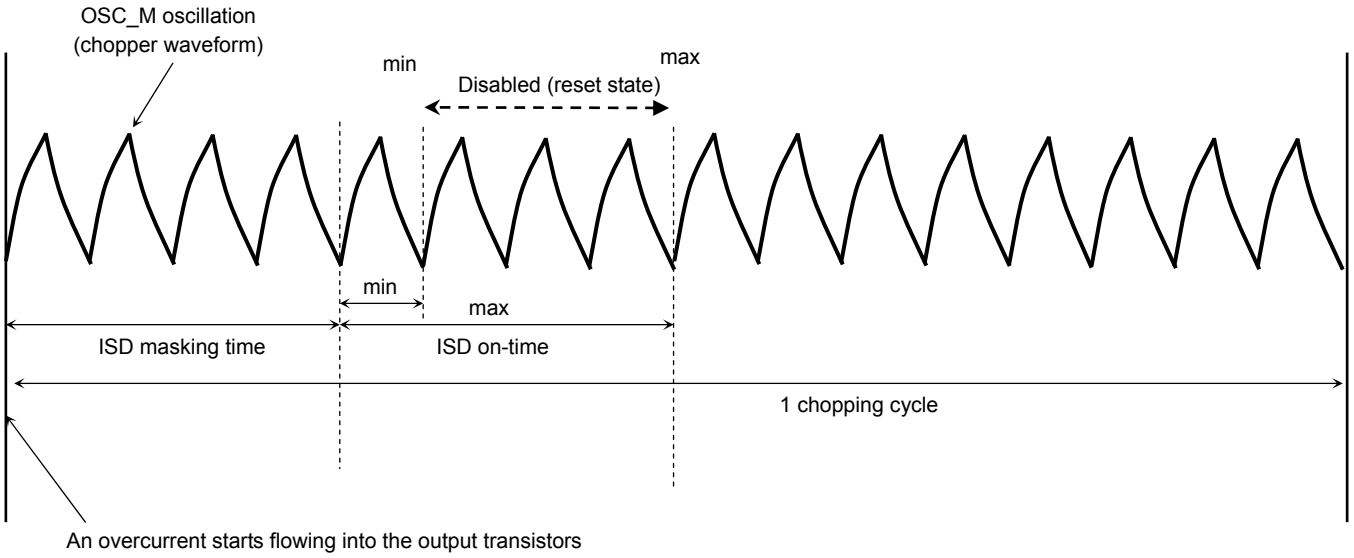


	A PHASE				B PHASE			
	Input			Output	Input			Output
	PHASE A	IN A1	IN A2	IOUT(A)	PHASE B	IN B1	IN B2	IOUT(B)
A	H	H	L	71%	H	H	L	71%
B	H	L	H	38%	H	H	H	100%
C	X	L	L	0%	H	H	H	100%
D	L	L	H	-38%	H	H	H	100%
E	L	H	L	-71%	H	H	L	71%
F	L	H	H	-100%	H	L	H	38%
G	L	H	H	-100%	X	L	L	0%
H	L	H	H	-100%	L	L	H	-38%
I	L	H	L	-71%	L	H	L	-71%
J	L	L	H	-38%	L	H	H	-100%
K	X	L	L	0%	L	H	H	-100%
L	H	L	H	38%	L	H	H	-100%
M	H	H	L	71%	L	H	L	-71%
N	H	H	H	100%	L	L	H	-38%
O	H	H	H	100%	X	L	L	0%
P	H	H	H	100%	H	L	H	38%



Overcurrent Shutdown (ISD) Circuitry

ISD Masking Time and ISD On-Time



The overcurrent shutdown (ISD) circuitry has a masking time to prevent current spikes during Irr and switching from erroneously tripping the ISD circuitry. The masking time is a function of the chopper frequency obtained by CR:

masking_time = 4 × CR_frequency

The minimum and maximum times taken to turn off the output transistors since an overcurrent flows into them are:

Min: 4 × CR_frequency
Max: 8 × CR_frequency

It should be noted that these values assume a case in which an overcurrent condition is detected in an ideal manner. The ISD circuitry might not work, depending on the control timing of the output transistors.

Therefore, a protection fuse must always be added to the V_M power supply as a safety precaution. The optimal fuse capacitance varies with usage conditions, and one that does not adversely affect the motor operation or exceed the power dissipation rating of the TB62218AFG/AFTG should be selected.

Calculating OSCM Oscillating Frequency

The OSCM oscillating frequency can be approximated using the following equation:

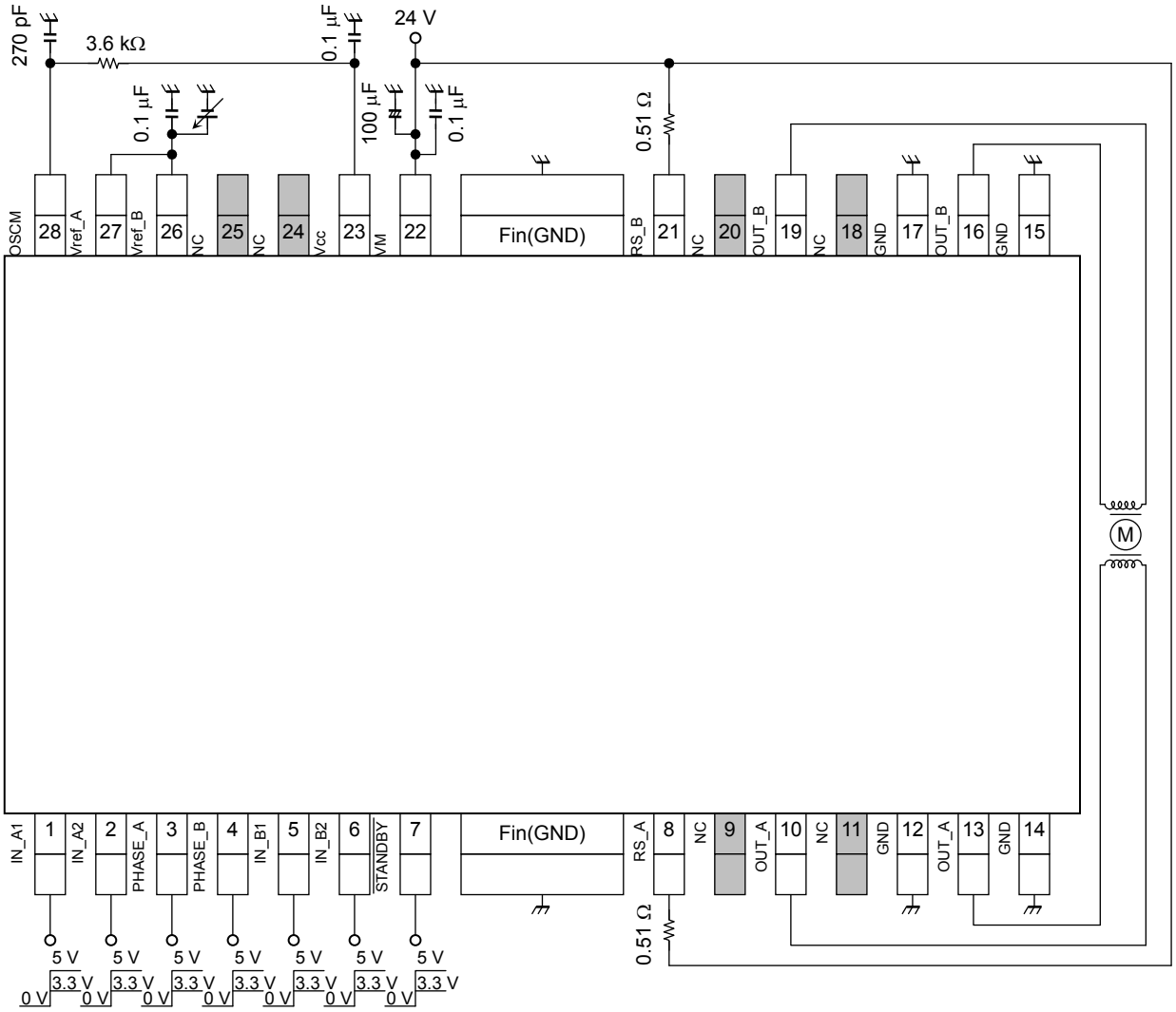
$$f_{OSCM} = \frac{1}{0.56 \times C \times (R_1 + 500)}$$

Where:
C = Capacitor capacity
R1= Resistance
Assigning C = 270 × 10^{-12} [F], R1= 3600 [Ω] to get:
f_{OSCM} = 1.61 × 10^6 ⇒ 1.6 MHz

Example Application Circuits

TB62218AFG

The values shown in the following figure are typical values. For input conditions, see Operating Ranges.



Note: Bypass capacitors should be added as necessary.

It is recommended to use a single ground plane for the entire board whenever possible, and a grounding method should be considered for efficient heat dissipation.

In cases where mode setting pins are controlled via switches, either pull-down or pull-up resistors should be added to them to avoid floating states.

For a description of the input values, see the output function tables.

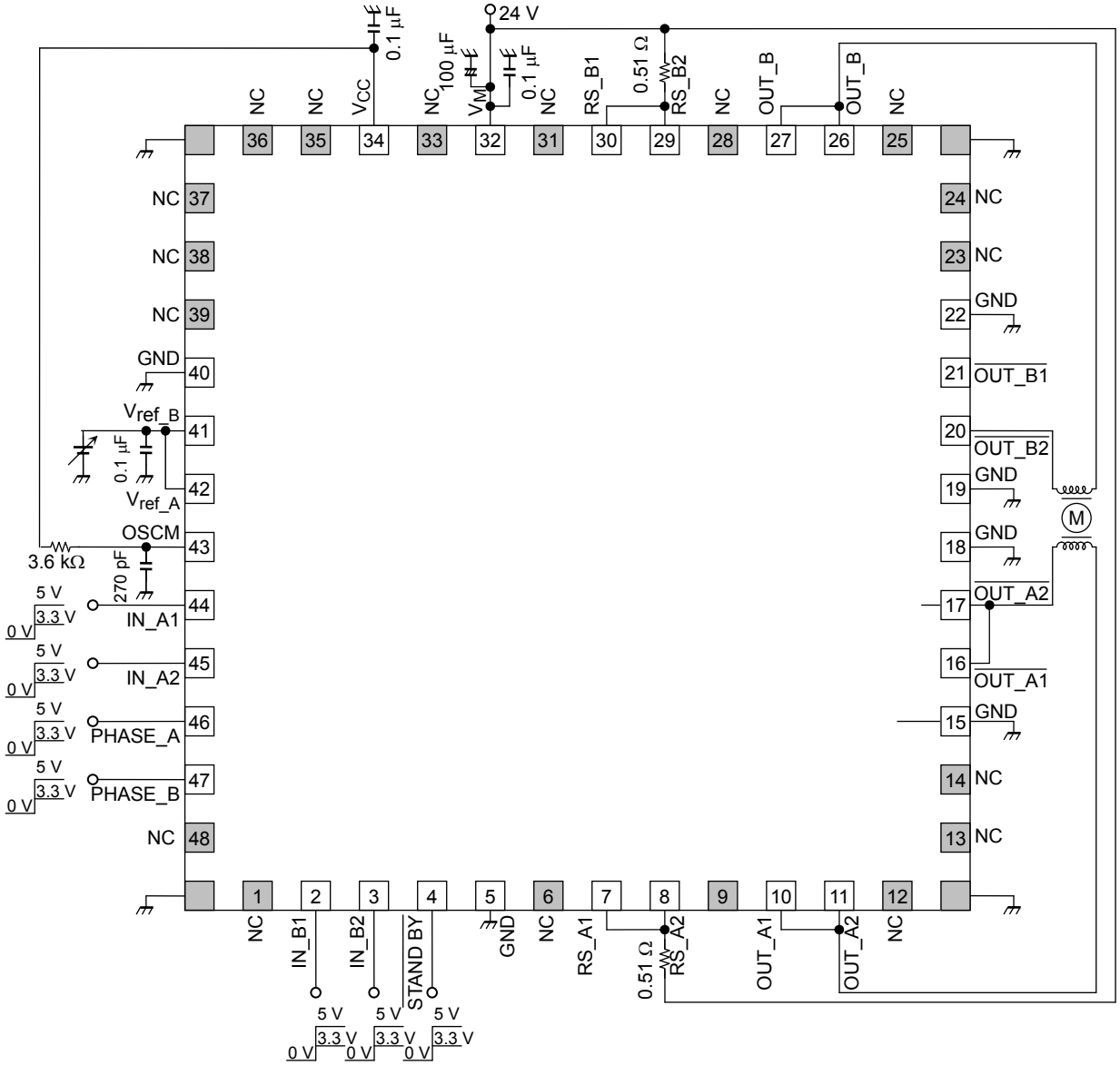
The above application circuit example is presented only as a guide and should be fully evaluated prior to production. Also, no intellectual property right is ceded in any way whatsoever in regard to its use.

The external components in the above diagram are used to test the electrical characteristics of the device: it is not guaranteed that no system malfunction or failure will occur.

Careful attention should be paid to the layout of the output, V_{DD} (V_M) and GND traces to avoid short-circuits across output pins or to the power supply or ground. If such a short-circuit occurs, the TB62218AFG/AFTG may be permanently damaged. Also, if the device is installed in a wrong orientation, a high voltage might be applied to components with lower voltage ratings, causing them to be damaged. The TB62218AFG/AFTG does not have an overvoltage protection circuit. Thus, if a voltage exceeding the rated maximum voltage is applied, the TB62218AFG/AFTG will be damaged; it should be ensured that it is used within the specified operating conditions.

TB62218AFTG

The values shown in the following figure are typical values. For input conditions, see Operating Ranges.



Note: Bypass capacitors should be added as necessary.

It is recommended to use a single ground plane for the entire board whenever possible, and a grounding method should be considered for efficient heat dissipation.

In cases where mode setting pins are controlled via switches, either pull-down or pull-up resistors should be added to them to avoid floating states.

For a description of the input values, see the output function tables.

The above application circuit example is presented only as a guide and should be fully evaluated prior to production. Also, no intellectual property right is ceded in any way whatsoever in regard to its use.

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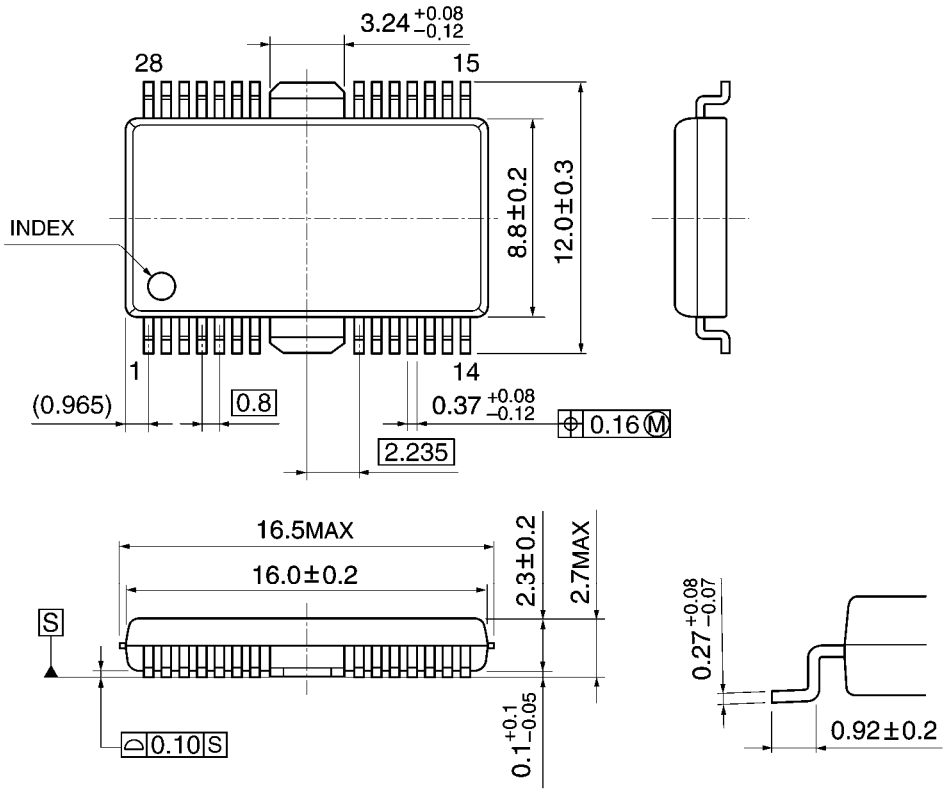
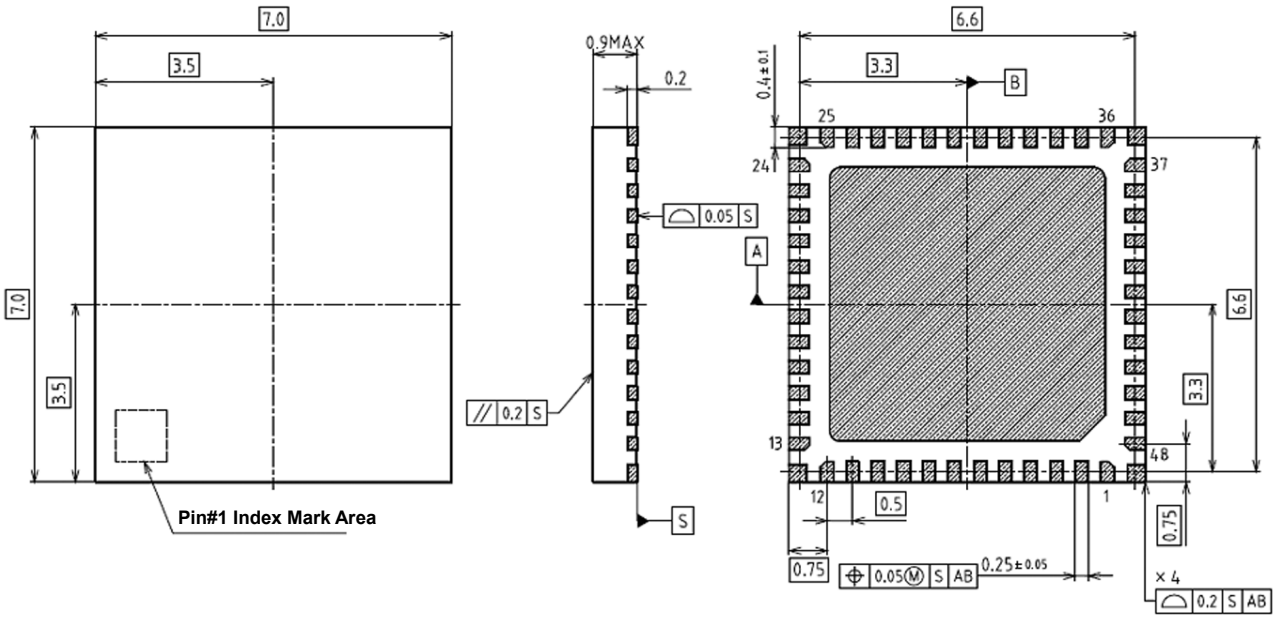
Package Dimensions

HSOP28-P-450-0.80 Unit: mm



Weight: 0.79 g (typ.)

QFN48-P-0707-0.5 **Unit: mm**

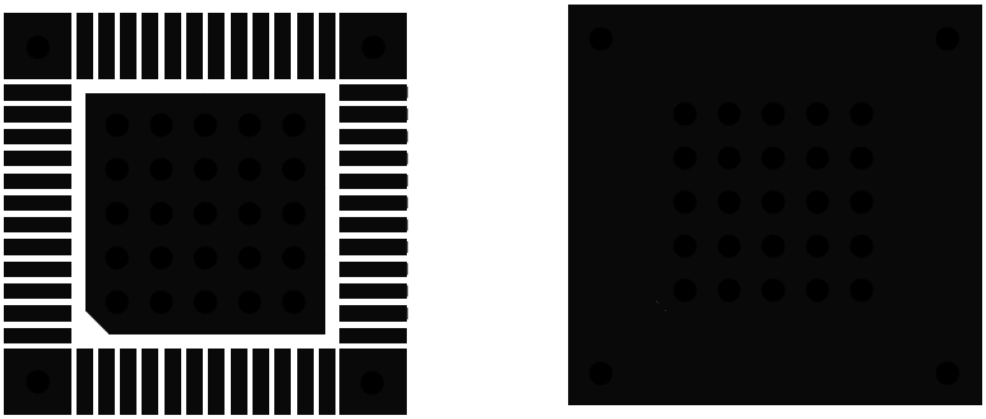


Backside heatsink: 5.4 mm × 5.4 mm
Corner chamfers: C0.5
Chamfer radius: 3-R0.2

Weight: 0.14 g (typ.)

Foot Pattern Example (double-sided board)

Surface **Bottom**



Black dots: 0.2 mm through holes

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Example Application Circuits

The example application circuits shown in this document are provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design. In providing these example application circuits, Toshiba does not grant the use of any industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices incorrectly or in the wrong orientation.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause breakdown, damage or deterioration of the device, and may result in injury by explosion or combustion.
In addition, do not use any device that has had current applied to it while inserted incorrectly or in the wrong orientation even once.

(5) Carefully select power amp, regulator, or other external components (such as inputs and negative feedback capacitors) and load components (such as speakers).
If there is a large amount of leakage current such as input or negative feedback capacitors, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Heat Dissipation Design

In using an IC with large current flow such as a power amp, regulator or driver, please design the device so that heat is appropriately dissipated, not to exceed the specified junction temperature (Tj) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat dissipation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat dissipation on peripheral components..

Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in your system design.

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